TEXAS INSTRUMENTS

OPA2313-Q1

SBOS823 – DECEMBER 2018

OPA2313-Q1 Low-Power, Rail-to-Rail In/Out, 500-µV Typical Offset, 1-MHz Operational Amplifier for Cost-Sensitive Systems

1 Features

- AEC-Q100 Qualified for Automotive Applications
  - Device Temperature Grade 1: –40°C to +125°C T_A
- Precision Amplifier for Cost-Sensitive Systems
- Low I_Q: 50 µA/ch
- Wide Supply Range: 1.8 V to 5.5 V
- Low Noise: 25 nV/√Hz at 1 kHz
- Gain Bandwidth: 1 MHz
- Rail-to-Rail Input/Output
- Low Input Bias Current: 0.2 pA
- Low Offset Voltage: 0.5 mV
- Unity-Gain Stable
- Internal RFI/EMI Filter

2 Applications

- Infotainment
- Engine Control Unit
- Automotive Lighting
- Low-Side Sensing
- Battery Management Systems
- Passive Safety
- Capacitive Sensing
- Fuel Pumps

3 Description

The OPA2313-Q1 dual-channel operational amplifier combines low power consumption with good performance. This enables it to be used in a wide range of applications, such as infotainment, engine control units, automotive lighting and more. The OPA2313-Q1 features rail-to-rail input and output (RRIO) swings, low quiescent current (50 µA, typical), wide bandwidth (1 MHz) and very low noise (25 nV/√Hz at 1 kHz), making it attractive for a variety of applications that require a good balance between cost and performance. Furthermore, low input bias current enables this device to be used in applications with megaohm source impedances.

The robust design of the OPA2313-Q1 provides ease-of-use to the circuit designer: unity-gain stability with capacitive loads of up to 150 pF, integrated RFI/EMI rejection filter, no phase reversal in overdrive conditions, and high electrostatic discharge (ESD) protection (4-kV HBM).

The device is optimized for operation at voltages as low as 1.8 V (±0.9 V) and up to 5.5 V (±2.75 V), and is specified over the extended temperature range of –40°C to +125°C.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA2313-Q1	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

EMIRR IN+ vs Frequency

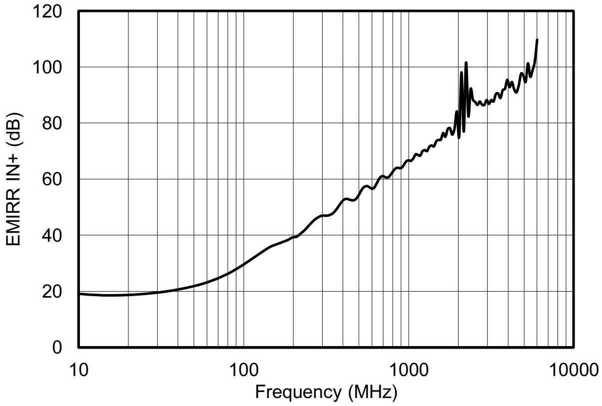


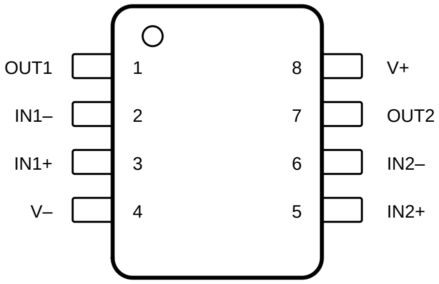
Table of Contents

4 Revision History

DATE	REVISION	NOTES
December 2018	*	Initial release.

5 Pin Configuration and Functions

OPA2313-Q1 D, DGK Packages
8-Pin SOIC, VSSOP
Top View



Not to scale

Pin Functions: OPA2313-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1–	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2–	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V–	4	—	Negative (lowest) supply or ground (for single-supply operation)
V+	8	—	Positive (highest) supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply voltage (V+) – (V–)	0	7	V
	Signal input terminals(2)	(V–) – (0.5)	(V+) + 0.5	
Current	Signal input terminals(2)	–10	10	mA
	Output short circuit(3)	Continuous		
Temperature	Operating, T_A	–40	150	°C
	Junction, T_J		150	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) HBM ESD Classification Level 3A	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2) CDM ESD Classification Level C6	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage (V+) – (V–)	1.8	5.5	V
T_A	Specified temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		OPA2313-Q1		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 Pins	8 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	138.4	191.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	89.5	61.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	78.6	111.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	29.9	5.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	78.1	110.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics: 5.5 V(1)

For V_S= (V+) – (V–) = 5.5 V at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, and V_{CM} = V_{OUT} = V_S / 2, (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				0.5	2.5	mV
dV_{OS}/dT	Input offset voltage vs temperature		T_A = –40°C to 125°C		2		μV/°C
PSRR	Power-supply rejection ratio		T_A = –40°C to 125°C	74	90		dB
	Channel separation, dc	At dc			10		μV/V
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range	No phase reversal, rail-to-rail input		(V–) – 0.2		(V+) + 0.2	V
CMRR	Common-mode rejection ratio	(V–) – 0.2 V < V_{CM} < (V+) – 1.3 V	T_A = –40°C to 125°C	70	85		dB
		V_{CM} = –0.2 V to 5.7 V	T_A = –40°C to 125°C	64	80		
INPUT BIAS CURRENT							
I_B	Input bias current				±0.2	±10	pA
			T_A = –40°C to 85°C(2)			±50	
			T_A = –40°C to 125°C(2)			±600	
I_{OS}	Input offset current				±0.2	±10	pA
			T_A = –40°C to 85°C(2)			±50	
			T_A = –40°C to 125°C(2)			±600	
NOISE							
	Input voltage noise (peak-to-peak)	f = 0.1 Hz to 10 Hz			6		μV_{PP}
e_n	Input voltage noise density	f = 10 kHz			22		nV/√Hz
		f = 1 kHz			25		
i_n	Input current noise density	f = 1 kHz			5		fA/√Hz
INPUT CAPACITANCE							
C_{IN}	Differential				1		pF
	Common-mode				5		
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	0.05 V < V_O < (V+) – 0.05 V, R_L = 100 kΩ		90	104		dB
		0.3 V < V_O < (V+) – 0.3 V, R_L = 2 kΩ		100	110		
		0.1 V < V_O < (V+) – 0.1 V	T_A = –40°C to 125°C	104	116		
	Phase margin	V_S = 5 V, G = +1			65		°
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	V_S = 5 V, C_L = 10 pF			1		MHz
SR	Slew rate	V_S = 5 V, G = +1			0.5		V/μs
t_S	Settling time	To 0.1%, V_S = 5 V, 2-V step, G = +1			5		μs
		To 0.01%, V_S = 5 V, 2-V step, G = +1			6		
	Overload recovery time	V_S = 5 V, V_{IN} × Gain > V_S			3		
THD+N	Total harmonic distortion + noise(3)	V_S = 5 V, V_O = 1 V_{RMS}, G = +1, f = 1 kHz			0.0045%		
OUTPUT							
V_O	Voltage output swing from supply rails	R_L = 100 kΩ(2)			5	20	mV
		R_L = 100 kΩ(2)	T_A = –40°C to 125°C			30	
		R_L = 2 kΩ(2)			75	100	
		R_L = 2 kΩ(2)	T_A = –40°C to 125°C			125	
I_{SC}	Short-circuit current				±15		mA
			T_A = –40°C to 125°C		±12		
R_O	Open-loop output impedance				2300		Ω

(1) Parameters with minimum or maximum specification limits are 100% production tested at 25°C, unless otherwise noted. Over-temperature limits are based on characterization and statistical analysis.
(2) Specified by design and characterization; not production tested.
(3) Third-order filter; bandwidth = 80 kHz at –3 dB.

Electrical Characteristics: 5.5 V(1) (continued)

For V_S= (V+) – (V–) = 5.5 V at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, and V_{CM} = V_{OUT} = V_S / 2, (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY							
V_S	Specified voltage range			1.8 (±0.9)		5.5 (±2.75)	V
I_Q	Quiescent current per amplifier	V_S = 5 V, I_O = 0 mA			50	60	μA
		V_S = 5 V, I_O = 0 mA	T_A = –40°C to 125°C			85	
	Power-on time	V_S = 0 V to 5 V, to 90% I_Q level			10		μs

6.6 Electrical Characteristics: 1.8 V(1)

For V_S= (V+) – (V–) = 1.8 V at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_{S+} – 1.3 V, and V_{OUT} = V_S / 2, (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				0.5	2.5	mV
dV_{OS}/dT	Input offset voltage vs temperature		T_A = –40°C to 125°C		2		µV/°C
PSRR	Power-supply rejection ratio		T_A = –40°C to 125°C	74	90		dB
	Channel separation, dc	At dc			10		µV/V
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range	No phase reversal, rail-to-rail input		(V–) – 0.2		(V+) + 0.2	V
CMRR	Common-mode rejection ratio	(V–) – 0.2 V < V_{CM} < (V+) – 1.3 V	T_A = –40°C to 125°C	70	85		dB
		V_S= 1.8 V, V_{CM} = –0.2 V to 1.8 V		58	73		
		V_{CM} = –0.2 V to 1.6 V	T_A = –40°C to 125°C	58	70		
INPUT BIAS CURRENT							
I_B	Input bias current				±0.2	±10	pA
			T_A = –40°C to 85°C(2)			±50	
			T_A = –40°C to 125°C(2)			±600	
I_{OS}	Input offset current				±0.2	±10	pA
			T_A = –40°C to 85°C(2)			±50	
			T_A = –40°C to 125°C(2)			±600	
NOISE							
	Input voltage noise (peak-to-peak)	f = 0.1 Hz to 10 Hz			6		$µV_{PP}$
e_n	Input voltage noise density	f = 10 kHz			22		nV/√Hz
		f = 1 kHz			25		
i_n	Input current noise density	f = 1 kHz			5		fA/√Hz
INPUT CAPACITANCE							
C_{IN}	Differential				1		pF
	Common-mode				5		
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	0.05 V < V_O < (V+) – 0.05 V, R_L = 100 kΩ		100	110		dB
		0.1 V < V_O < (V+) – 0.1 V	T_A = –40°C to 125°C	90	110		
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	C_L = 10 pF			0.9		MHz
SR	Slew rate	G = +1			0.45		V/µs
t_S	Settling time	To 0.1%, V_S = 5 V, 2-V step, G = +1			5		µs
		To 0.01%, V_S = 5 V, 2-V step, G = +1			6		
	Overload recovery time	V_S = 5 V, V_{IN} × Gain > V_S			3		
THD+N	Total harmonic distortion + noise(3)	V_S = 5 V, V_O = 1 V_{RMS}, G = +1, f = 1kHz			0.0045%		
OUTPUT							
V_O	Voltage output swing from supply rails	R_L = 100 kΩ(2)			5	15	mV
		R_L = 100 kΩ(2)	T_A = –40°C to 125°C			30	
		R_L = 2 kΩ(2)			25	50	
		R_L = 2 kΩ(2)	T_A = –40°C to 125°C			125	
I_{SC}	Short-circuit current				±6		mA
R_O	Open-loop output impedance				2300		Ω

(1) Parameters with minimum or maximum specification limits are 100% production tested at 25°C, unless otherwise noted. Over-temperature limits are based on characterization and statistical analysis.
(2) Specified by design and characterization; not production tested.
(3) Third-order filter; bandwidth = 80 kHz at –3 dB.

Electrical Characteristics: 1.8 V(1) (continued)

For V_S= (V+) – (V–) = 1.8 V at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_{S+} – 1.3 V, and V_{OUT} = V_S / 2, (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_S	Specified voltage range		1.8 (±0.9)		5.5 (±2.75)	V
I_Q	Quiescent current per amplifier	V_S = 5 V, I_O = 0 mA		50	60	µA
	Power-on time	V_S = 0 V to 5 V, to 90% I_Q level		10		µs

6.7 Typical Characteristics: Tables of Graphs

Table 1. Characteristic Performance Measurements

TITLE	FIGURE
Open-Loop Gain and Phase vs Frequency	Figure 1
Open-Loop Gain vs Temperature	Figure 2
Quiescent Current vs Supply Voltage	Figure 3
Quiescent Current vs Temperature	Figure 4
Offset Voltage Production Distribution	Figure 5
Offset Voltage Drift Distribution	Figure 6
Offset Voltage vs Common-Mode Voltage (Maximum Supply)	Figure 7
Offset Voltage vs Temperature	Figure 8
CMRR and PSRR vs Frequency (RTI)	Figure 9
CMRR and PSRR vs Temperature	Figure 10
0.1-Hz to 10-Hz Input Voltage Noise (5.5 V)	Figure 11
Input Voltage Noise Spectral Density vs Frequency (1.8 V, 5.5 V)	Figure 12
Input Voltage Noise vs Common-Mode Voltage (5.5 V)	Figure 13
Input Bias and Offset Current vs Temperature	Figure 14
Open-Loop Output Impedance vs Frequency	Figure 15
Maximum Output Voltage vs Frequency and Supply Voltage	Figure 16
Output Voltage Swing vs Output Current (over Temperature)	Figure 17
Closed-Loop Gain vs Frequency, G = 1, –1, 10 (1.8 V)	Figure 18
Closed-Loop Gain vs Frequency, G = 1, –1, 10 (5.5 V)	Figure 19
Small-Signal Overshoot vs Load Capacitance	Figure 20
Phase Margin vs Capacitive Load	Figure 21
Small-Signal Step Response, Noninverting (1.8 V)	Figure 22
Small-Signal Step Response, Noninverting (5.5 V)	Figure 23
Large-Signal Step Response, Noninverting (1.8 V)	Figure 24
Large-Signal Step Response, Noninverting (5.5 V)	Figure 25
Positive Overload Recovery	Figure 26
Negative Overload Recovery	Figure 27
No Phase Reversal	Figure 28
Channel Separation vs Frequency (Dual)	Figure 29
THD+N vs Amplitude (G = +1, 2 kΩ, 10 kΩ)	Figure 30
THD+N vs Amplitude (G = –1, 2 kΩ, 10 kΩ)	Figure 31
THD+N vs Frequency (0.5 V_{RMS}, G = +1, 2 kΩ, 10 kΩ)	Figure 32
EMIRR IN+ vs Frequency	Figure 33

6.8 Typical Characteristics

At T_A = 25°C, V_S = 5 V, R_L = 10 kΩ connected to V_S / 2, and V_{CM} = V_{OUT} = V_S / 2, unless otherwise noted.

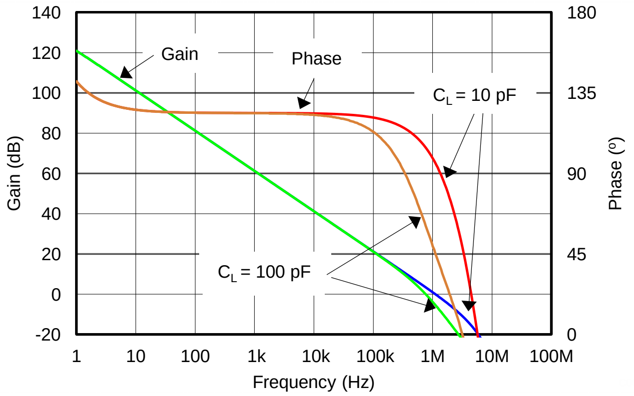


Figure 1. Open-Loop Gain and Phase vs Frequency

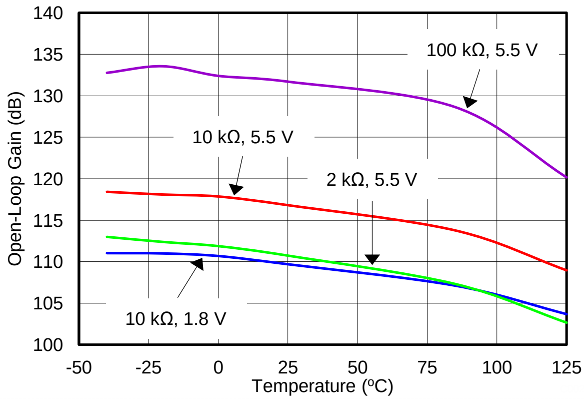


Figure 2. Open-Loop Gain vs Temperature

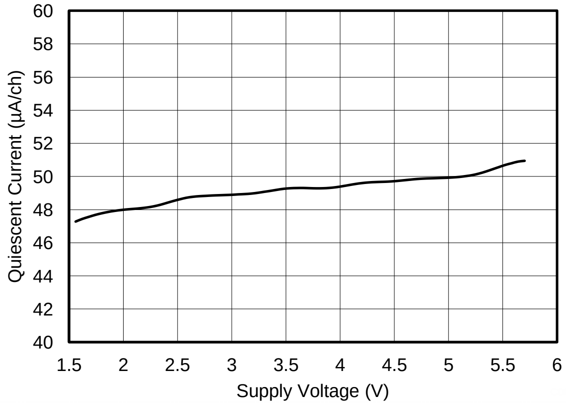


Figure 3. Quiescent Current vs Supply

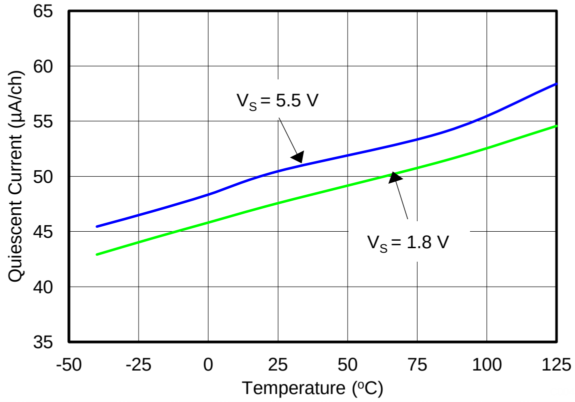


Figure 4. Quiescent Current vs Temperature

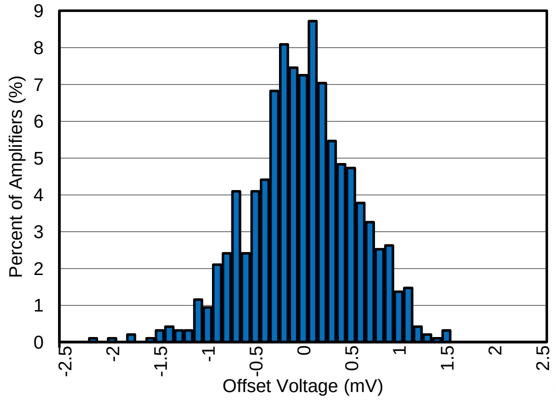


Figure 5. Offset Voltage Production Distribution

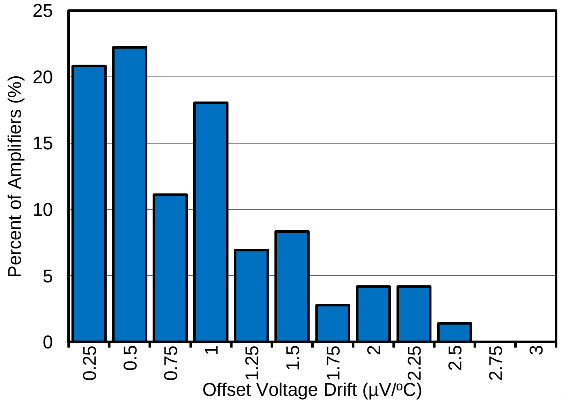


Figure 6. Offset Voltage Drift Distribution

Typical Characteristics (continued)

At T_A = 25°C, V_S = 5 V, R_L = 10 kΩ connected to V_S / 2, and V_{CM} = V_{OUT} = V_S / 2, unless otherwise noted.

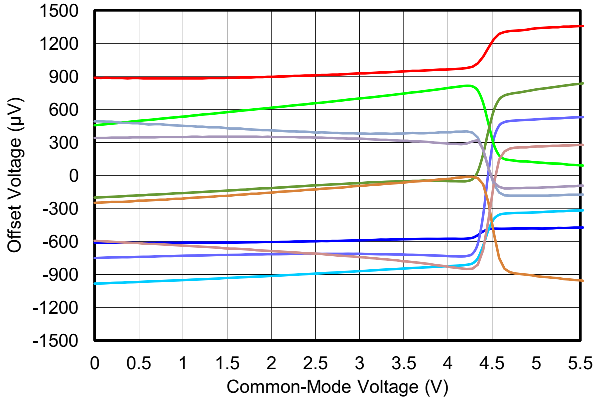


Figure 7. Offset Voltage vs Common-Mode Voltage

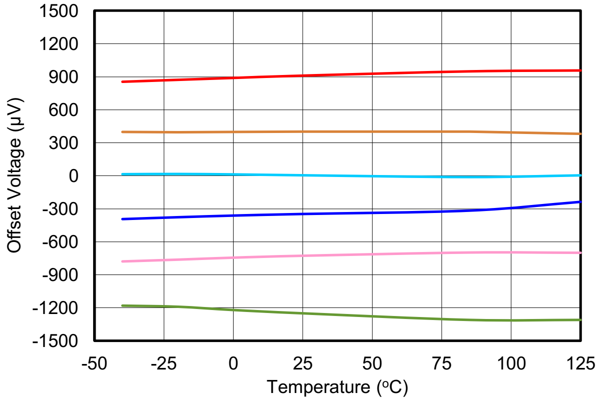


Figure 8. Offset Voltage vs Temperature

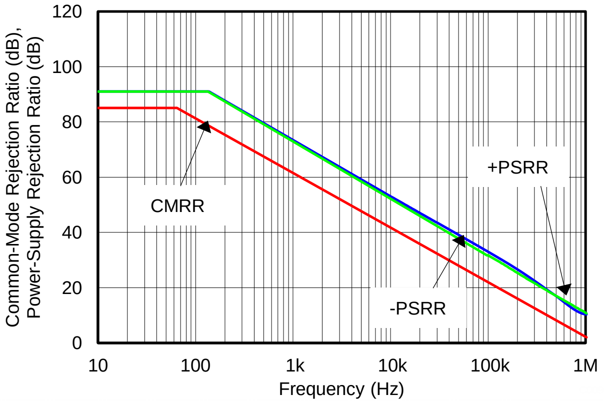


Figure 9. CMRR and PSRR vs Frequency (Referred-to-Input)

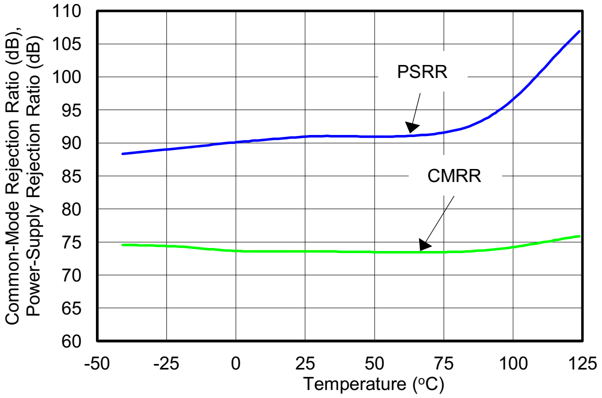


Figure 10. CMRR and PSRR vs Temperature

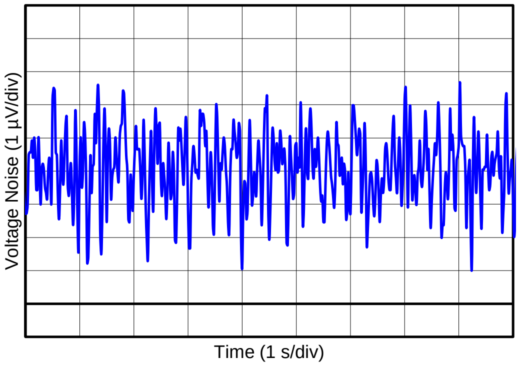


Figure 11. 0.1-Hz to 10-Hz Input Voltage Noise

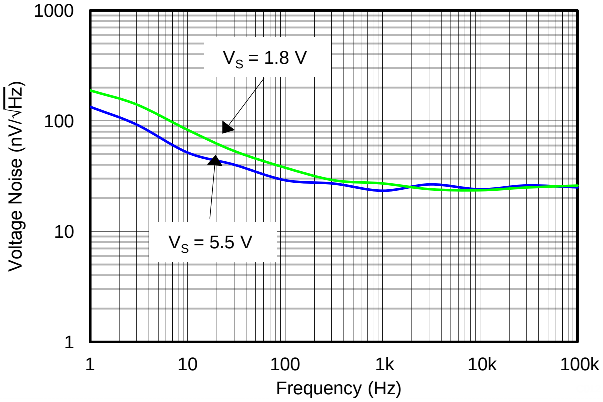


Figure 12. Input Voltage Noise Spectral Density vs Frequency

Typical Characteristics (continued)

At T_A = 25°C, V_S = 5 V, R_L = 10 kΩ connected to V_S / 2, and V_{CM} = V_{OUT} = V_S / 2, unless otherwise noted.

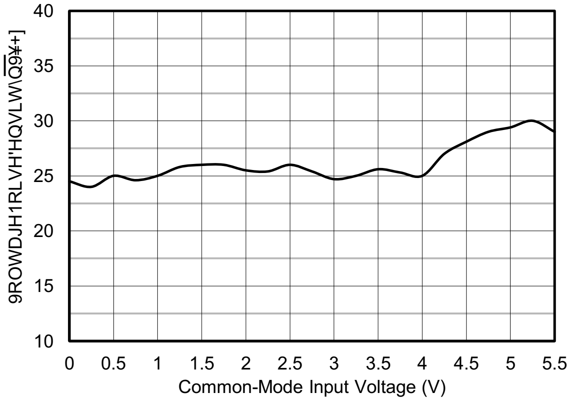


Figure 13. Voltage Noise vs Common-Mode Voltage

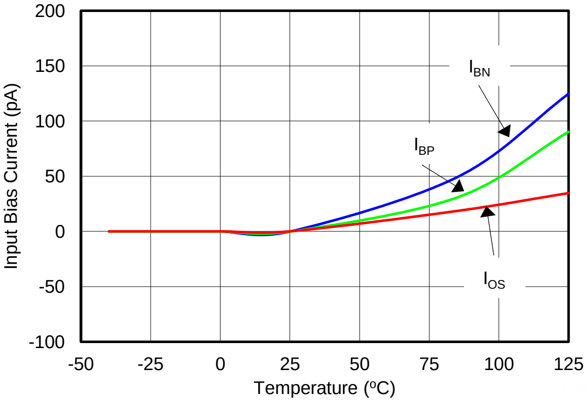


Figure 14. Input Bias and Offset Current vs Temperature

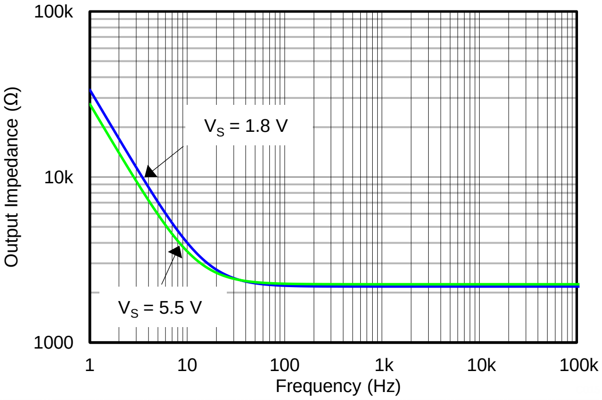


Figure 15. Open-Loop Output Impedance vs Frequency

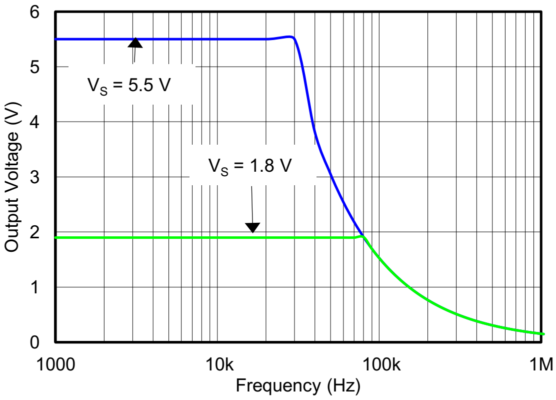


Figure 16. Maximum Output Voltage vs Frequency and Supply Voltage

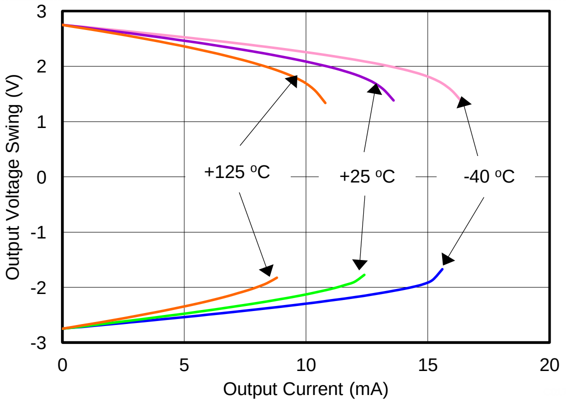


Figure 17. Output Voltage Swing vs Output Current (Over Temperature)

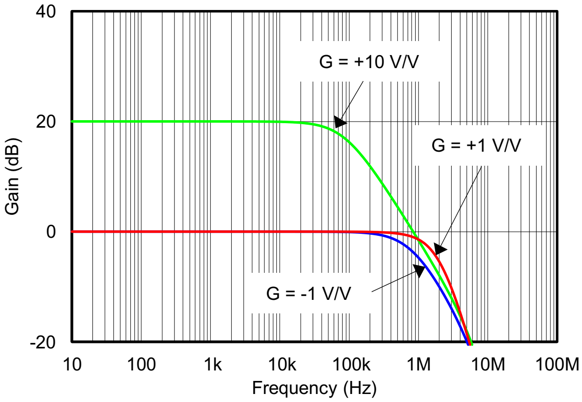


Figure 18. Closed-Loop Gain vs Frequency (Minimum Supply)

Typical Characteristics (continued)

At T_A = 25°C, V_S = 5 V, R_L = 10 kΩ connected to V_S / 2, and V_{CM} = V_{OUT} = V_S / 2, unless otherwise noted.

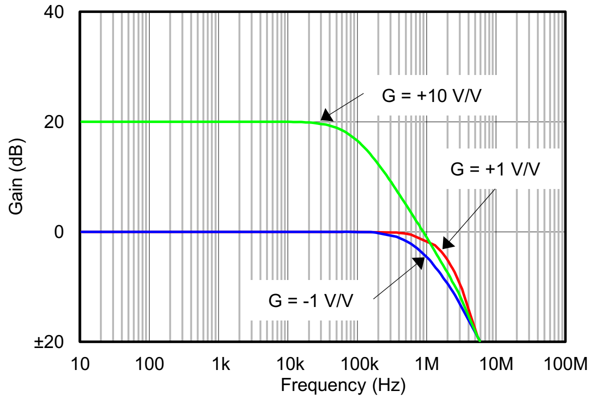


Figure 19. Closed-Loop Gain vs Frequency (Maximum Supply)

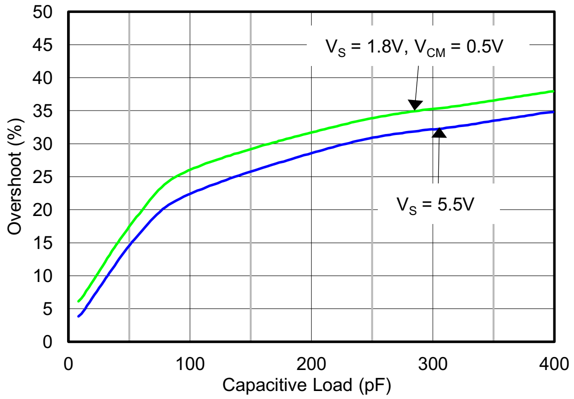


Figure 20. Small-Signal Overshoot vs Load Capacitance

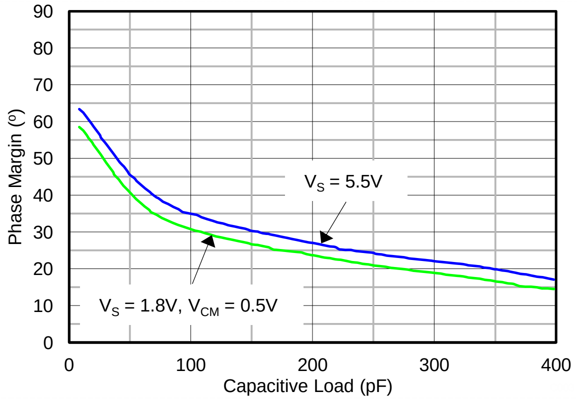


Figure 21. Phase Margin vs Capacitive Load

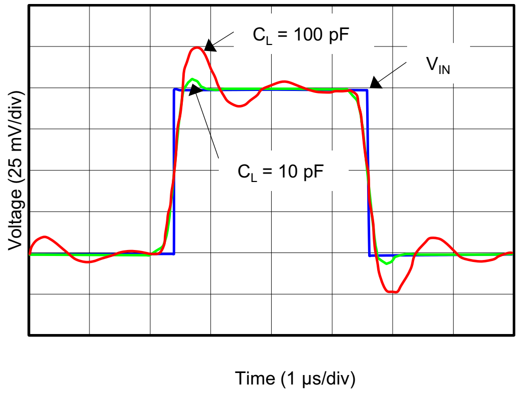


Figure 22. Small-Signal Pulse Response (Minimum Supply)

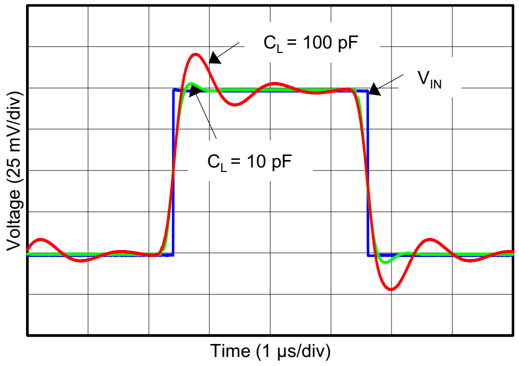


Figure 23. Small-Signal Pulse Response (Maximum Supply)

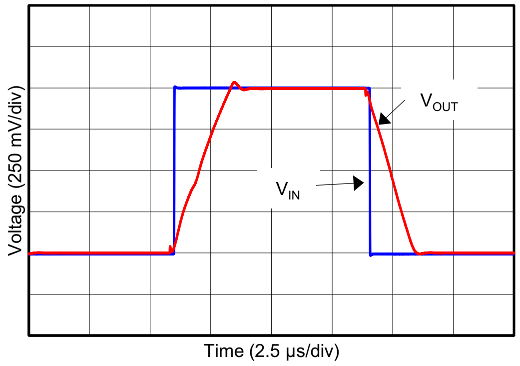


Figure 24. Large-Signal Pulse Response (Minimum Supply)

Typical Characteristics (continued)

At T_A = 25°C, V_S = 5 V, R_L = 10 kΩ connected to V_S / 2, and V_{CM} = V_{OUT} = V_S / 2, unless otherwise noted.

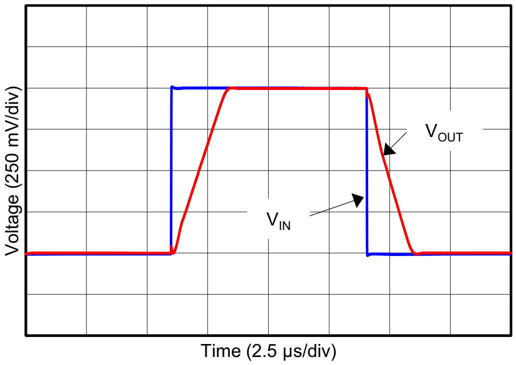


Figure 25. Large-Signal Pulse Response (Maximum Supply)

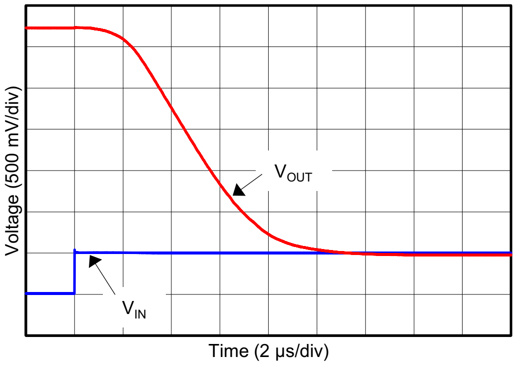


Figure 26. Positive Overload Recovery

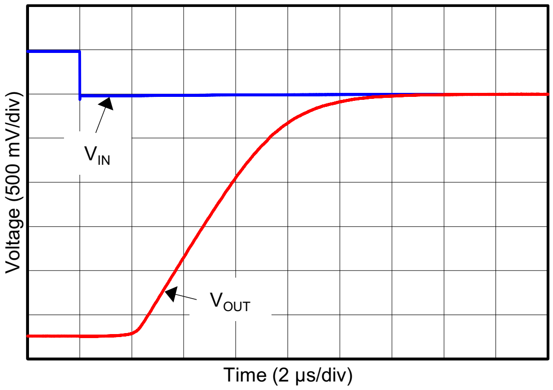


Figure 27. Negative Overload Recovery

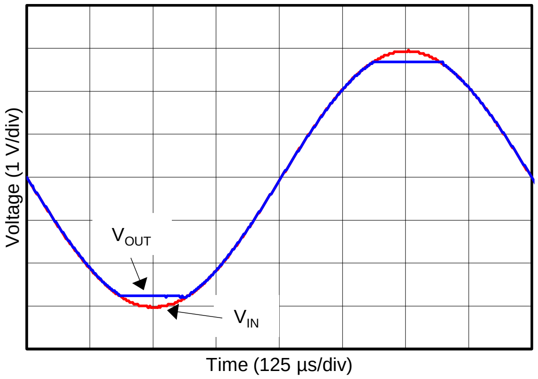


Figure 28. No Phase Reversal

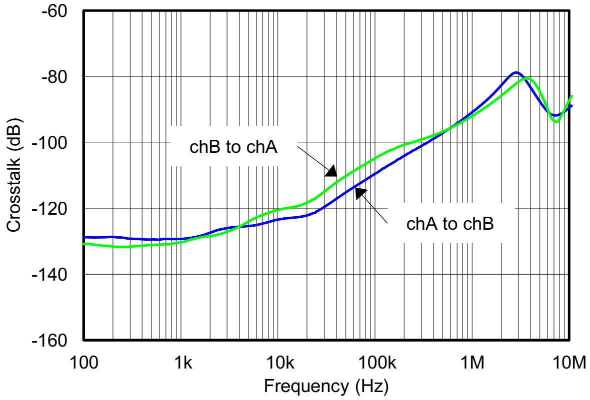


Figure 29. Channel Separation vs Frequency

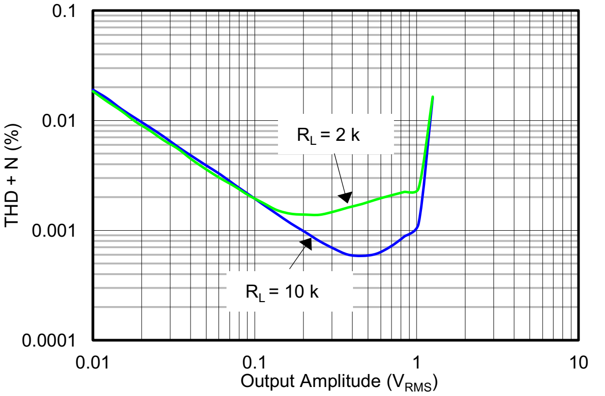


Figure 30. THD+N vs Output Amplitude (Minimum Supply)

Typical Characteristics (continued)

At T_A = 25°C, V_S = 5 V, R_L = 10 kΩ connected to V_S / 2, and V_{CM} = V_{OUT} = V_S / 2, unless otherwise noted.

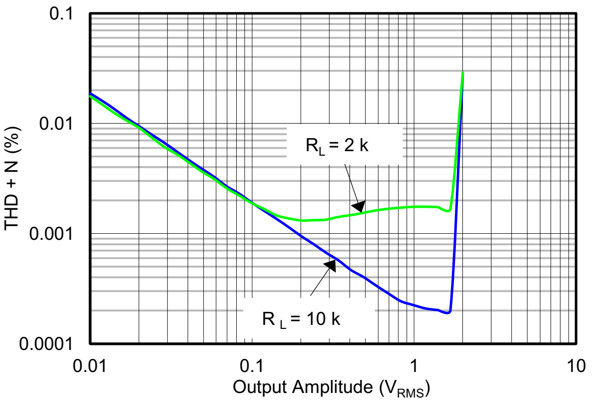


Figure 31. THD+N vs Output Amplitude (Maximum Supply)

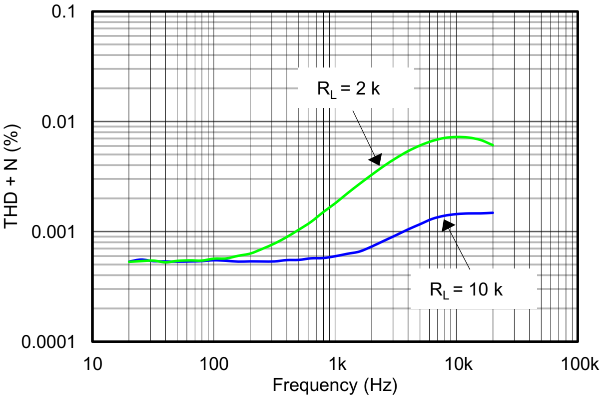


Figure 32. THD+N vs Frequency

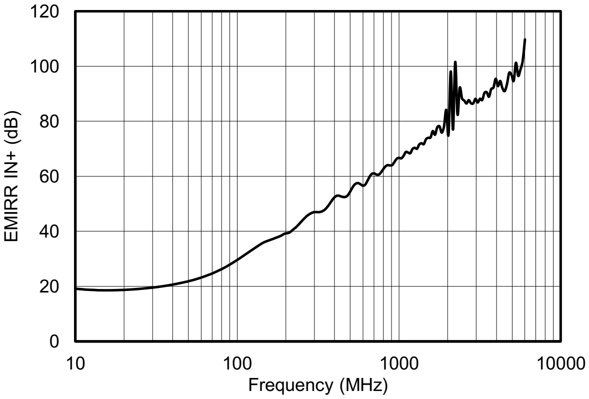


Figure 33. EMIRR IN+ vs Frequency

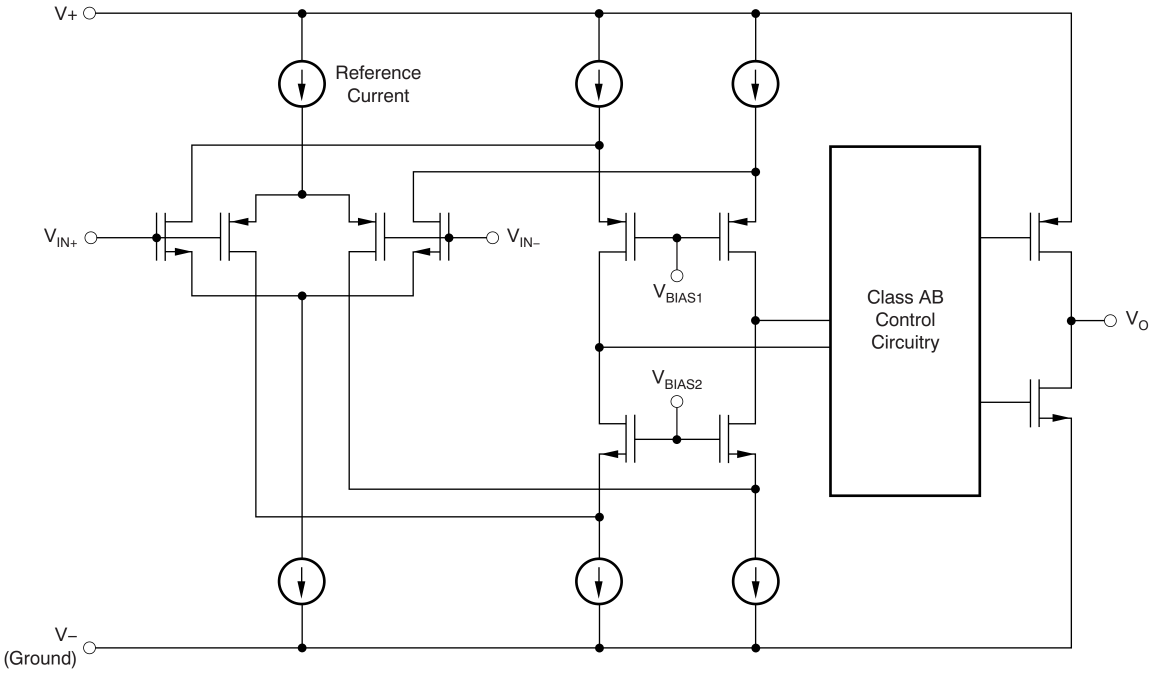
7 Detailed Description

7.1 Overview

The OPA2313-Q1 is a low-power, rail-to-rail input and output operational amplifier designed for cost-constrained applications. This device operates from 1.8 V to 5.5 V, is unity-gain stable, and suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving loads greater than 10-kΩ connected to any point between V+ and ground. The input common-mode voltage range includes both rails, and allows the OPA2313-Q1 to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes this device ideal for driving sampling analog-to-digital converters (ADCs).

The OPA2313-Q1 features 1-MHz bandwidth and 0.5-V/µs slew rate with only 50-µA supply current per channel, providing good ac performance at very low power consumption. Low frequency (dc) applications are also well served with a low input noise voltage of 25 nV/$\sqrt{\text{Hz}}$ at 1 kHz, low input bias current (0.2 pA), and an input offset voltage of 0.5 mV (typical). The typical offset voltage drift is 2 µV/°C; over the full temperature range the input offset voltage changes only 200 µV (0.5 mV to 0.7 mV).

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Voltage

The OPA2313-Q1 device is fully specified and tested from 1.8 V to 5.5 V (±0.9 V to ±2.75 V). Parameters that vary with supply voltage are illustrated in the *Typical Characteristics* section.

7.3.2 Rail-to-Rail Input

The input common-mode voltage range of the OPA2313-Q1 device extends 200 mV beyond the supply rails. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as shown in the *Functional Block Diagram* section. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.3 V to 200 mV above the positive supply, while the P-channel pair is on for inputs from 200 mV below the negative supply to approximately (V+) – 1.3 V. There is a small transition region, typically (V+) – 1.4 V to (V+) – 1.2 V, in which both pairs are on. This 200-mV transition region may vary up to 300 mV with process variation. Thus, the transition region (both stages on) may range from (V+) – 1.7 V to (V+) – 1.5 V on the low end, up to (V+) – 1.1 V to (V+) – 0.9 V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD may be degraded compared to device operation outside this region.

7.3.3 Rail-to-Rail Output

Designed as a micro-power, low-noise operational amplifier, the OPA2313-Q1 delivers a robust output drive capability. A class AB output stage with common-source transistors is used to achieve full rail-to-rail output swing capability. For resistive loads up to 10 kΩ, the output swings typically to within 5 mV of either supply rail regardless of the power-supply voltage applied. Different load conditions change the ability of the amplifier to swing close to the rails, as shown in Figure 17.

7.3.4 Common-Mode Rejection Ratio (CMRR)

CMRR for the OPA2313-Q1 device is specified in several ways so the best match for a given application may be used; see the *Electrical Characteristics*. First, the CMRR of the device in the common-mode range below the transition region (V_{CM} < (V+) – 1.3 V) is given. This specification is the best indicator of the capability of the device when the application requires use of one of the differential input pairs. Second, the CMRR over the entire common-mode range is specified at (V_{CM} = –0.2 V to 5.7 V). This last value includes the variations seen through the transition region, as shown in Figure 7.

7.3.5 Capacitive Load and Stability

The OPA2313-Q1 device is designed to be used in applications where driving a capacitive load is required. As with all op amps, there may be specific instances where the OPA2313-Q1 device may become unstable. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether or not an amplifier is stable in operation. An op amp in the unity-gain (+1-V/V) buffer configuration that drives a capacitive load exhibits a greater tendency to be unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the op amp output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases as the capacitive loading increases. When operating in the unity-gain configuration, the OPA2313-Q1 device remains stable with a pure capacitive load up to approximately 1 nF. The equivalent series resistance (ESR) of some capacitors (C_L greater than 1 µF) is sufficient to alter the phase characteristics in the feedback loop such that the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when observing the overshoot response of the amplifier at higher voltage gains. See the typical characteristic graph, Figure 20.

Feature Description (continued)

One technique for increasing the capacitive load drive capability of the amplifier when it operates in a unity-gain configuration is to insert a small resistor, typically 10 Ω to 20 Ω, in series with the output, as shown in Figure 34. This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. One possible problem with this technique is that a voltage divider is created with the added series resistor and any resistor connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that reduces the output swing.

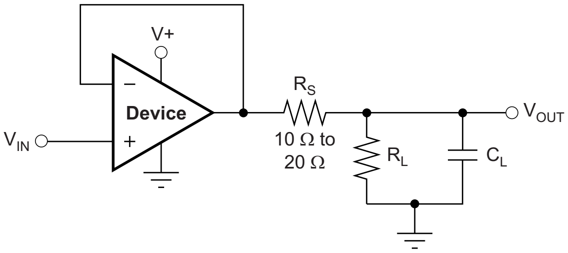


Figure 34. Improving Capacitive Load Drive

7.3.6 EMI Susceptibility and Input Filtering

Operational amplifiers vary with regard to the susceptibility of the device to electromagnetic interference (EMI). If conducted EMI enters the op amp, the DC offset observed at the amplifier output may shift from the nominal value while EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. While all op amp pin functions may be affected by EMI, the signal input pins are likely to be the most susceptible. The OPA2313-Q1 device incorporates an internal input low-pass filter that reduces the amplifiers response to EMI. Both common-mode and differential mode filtering are provided by this filter. The filter is designed for a common-mode cutoff frequency of approximately 35 MHz (–3 dB), with a rolloff of 20 dB per decade.

Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. The EMI rejection ratio (EMIRR) metric allows op amps to be directly compared by the EMI immunity. Figure 33 illustrates the results of this testing on the OPA2313-Q1 device. Detailed information may be found in *EMI Rejection Ratio of Operational Amplifiers*, available for download from www.ti.com.

7.3.7 Input and ESD Protection

The OPA2313-Q1 device incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. The ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in the *Absolute Maximum Ratings*. Figure 35 shows how a series input resistor may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

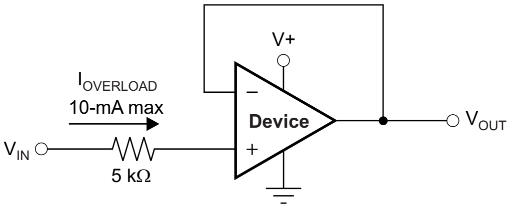


Figure 35. Input Current Protection

7.4 Device Functional Modes

The OPA2313-Q1 device has a single functional mode. The device is powered on as long as the power-supply voltage is between 1.8 V (±0.9 V) and 5.5 V (±2.75 V).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPA2313-Q1 device is a low-power, rail-to-rail input and output operational amplifier. The device operates from 1.8 V to 5.5 V, is unity-gain stable, and is designed for a wide range of general-purpose applications. The class AB output stage is capable of driving loads greater than 10 kΩ connected to any point between V+ and ground. The input common-mode voltage range includes both rails, and allows the OPA2313-Q1 to be used in virtually any single-supply application.

8.2 Typical Application

A typical application for an operational amplifier is an inverting amplifier, as shown in Figure 36. An inverting amplifier takes a positive voltage on the input and outputs a signal inverted to the input, making a negative voltage of the same magnitude. In the same manner, the amplifier also makes negative input voltages positive on the output. In addition, amplification may be added by selecting the input resistor (R_I) and the feedback resistor (R_F.)

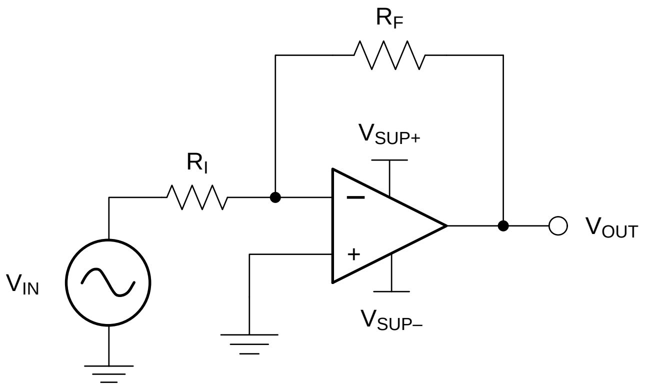


Figure 36. Inverting Amplifier Application

8.2.1 Design Requirements

The supply voltage must be chosen to be larger than the input voltage range and the desired output range. The limits of the input common-mode range (V_{CM}) and the output voltage swing to the rails (V_O) must also be considered. For instance, this application scales a signal of ±0.5 V (1 V) to ±1.8 V (3.6 V). Setting the supply at ±2.5 V is sufficient to accommodate this application.

8.2.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier using Equation 1 and Equation 2:

$$A_V = \frac{V_{OUT}}{V_{IN}} \tag{1}$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \tag{2}$$

Typical Application (continued)

When the desired gain is determined, choose a value for R_I or R_F. Choosing a value in the kilohm range is desirable for general-purpose applications because the amplifier circuit uses currents in the milliamp range. This milliamp current range ensures the device does not draw too much current. The trade-off is that very large resistors (100s of kilohms) draw the smallest current but generate the highest noise. Small resistors (100s of ohms) generate low noise but draw high current. This example uses 10 kΩ for R_I, resulting in a 36-kΩ resistor being used for R_F. The values are determined by Equation 3:

$$A_V = -\frac{R_F}{R_I} \tag{3}$$

8.2.3 Application Curve

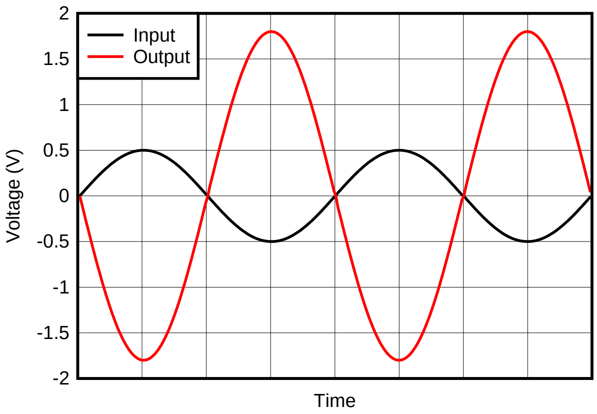
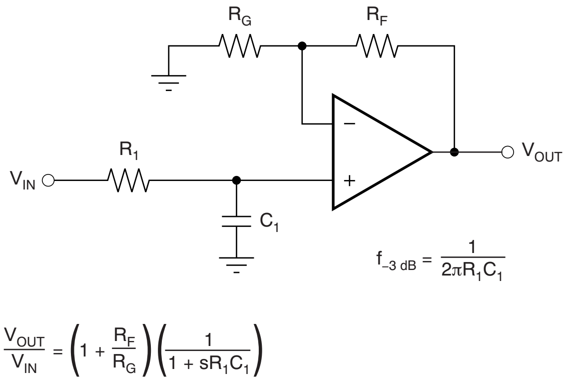


Figure 37. Inverting Amplifier Input and Output

8.3 System Examples

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to establish this limited bandwidth is to place an RC filter at the noninverting terminal of the amplifier, as shown in Figure 38.



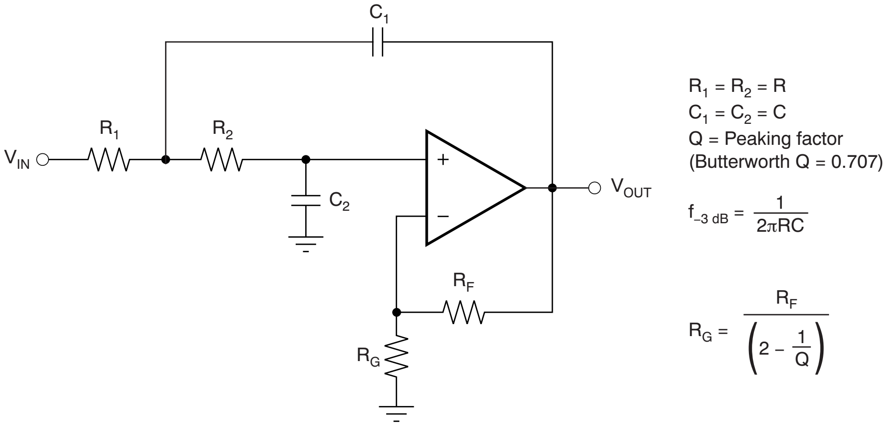
$$f_{-3\ dB} = \frac{1}{2\pi R_1 C_1}$$

$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR_1C_1}\right)$$

Figure 38. Single-Pole Low-Pass Filter

System Examples (continued)

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter may be used for this task, as shown in Figure 39. For best results, the amplifier must have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to follow this guideline may result in phase shift of the amplifier.



$R_1 = R_2 = R$
$C_1 = C_2 = C$
Q = Peaking factor
(Butterworth Q = 0.707)

$$f_{-3\,dB} = \frac{1}{2\pi RC}$$

$$R_G = \frac{R_F}{\left(2 - \frac{1}{Q}\right)}$$

Figure 39. Two-Pole, Low-Pass, Sallen-Key Filter

9 Power Supply Recommendations

The OPA2313-Q1 device is specified for operation from 1.8 V to 5.5 V (±0.9 V to ±2.75 V); many specifications apply from –40°C to +125°C. The *Typical Characteristics* section presents parameters that may exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 7 V can permanently damage the device (see the *Absolute Maximum Ratings* table).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout Guidelines* section.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise may propagate into analog circuitry through the power pins of the circuit and the operational amplifier. Use bypass capacitors to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see *Circuit Board Layout Techniques*.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If the traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than crossing in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keep R_F and R_G close to the inverting input to minimize parasitic capacitance, as shown in Figure 40.
- Keep the length of input traces as short as possible. Remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring may significantly reduce leakage currents from nearby traces that are at different potentials.

10.2 Layout Example

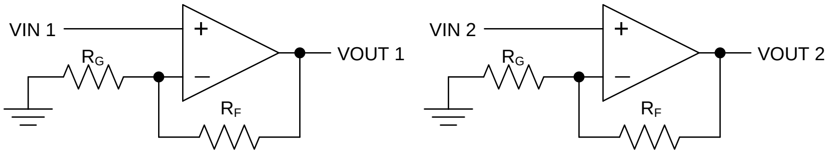


Figure 40. Schematic Representation for Figure 41

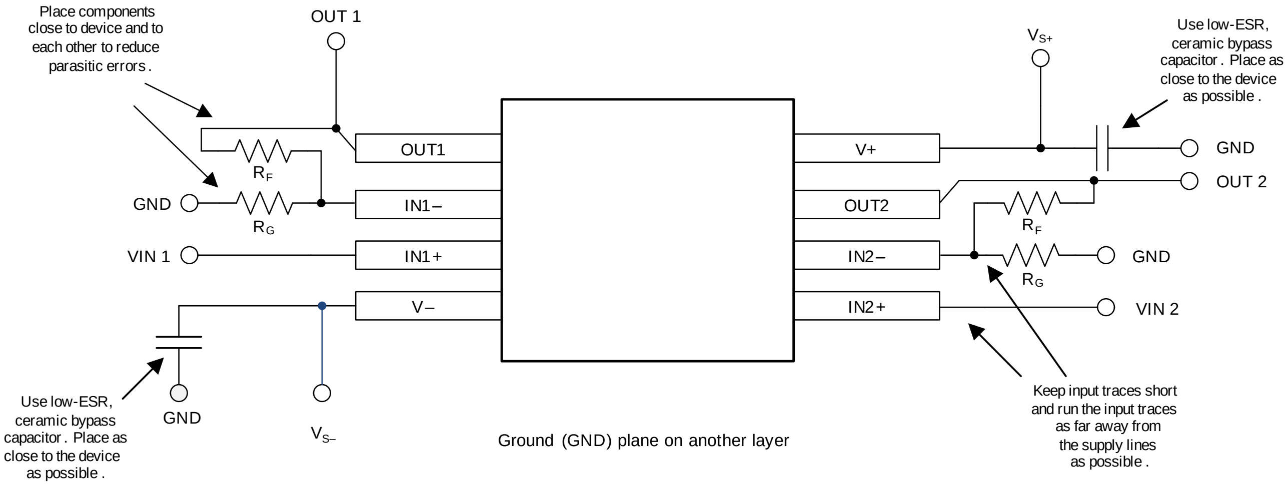


Figure 41. Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- *EMI Rejection Ratio of Operational Amplifiers*
- *Circuit Board Layout Techniques*

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2313QDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	23131
OPA2313QDGKRQ1.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	23131
OPA2313QDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2313Q
OPA2313QDRQ1.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2313Q

[1] **Status:** For more details on status, see our product life cycle.

[2] **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

[3] **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[4] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA2313-Q1 :

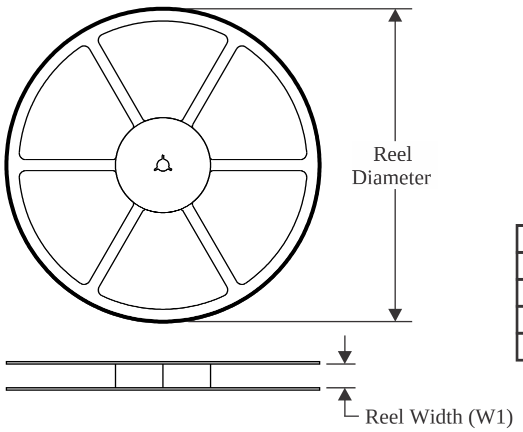
- Catalog : OPA2313

NOTE: Qualified Version Definitions:

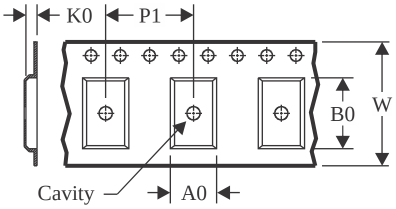
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

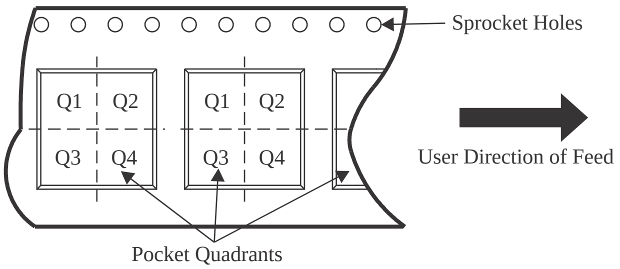


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

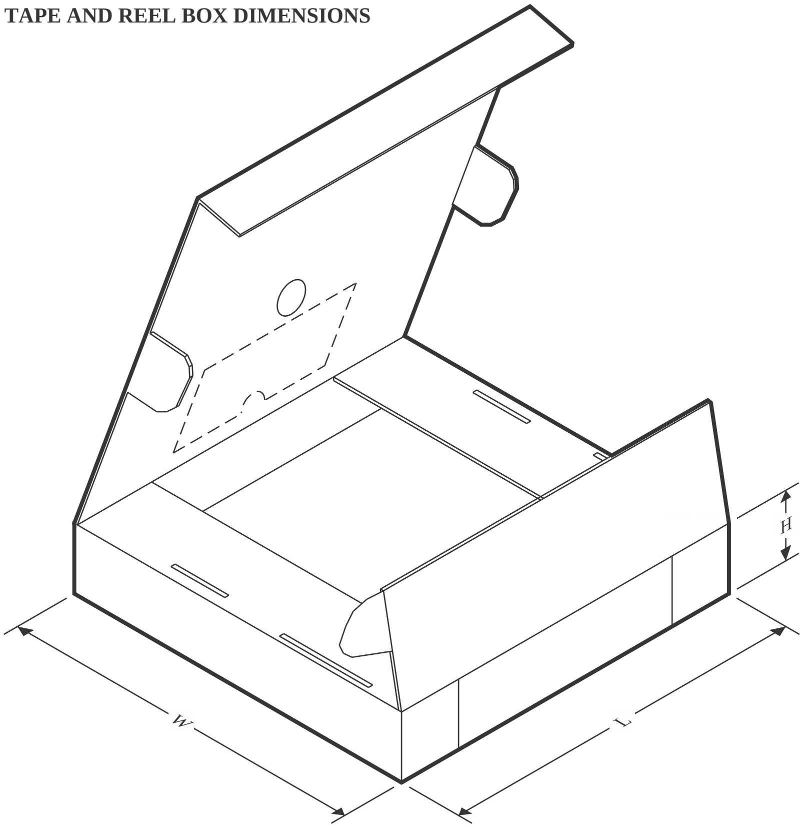
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

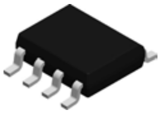
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2313QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2313QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2313QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

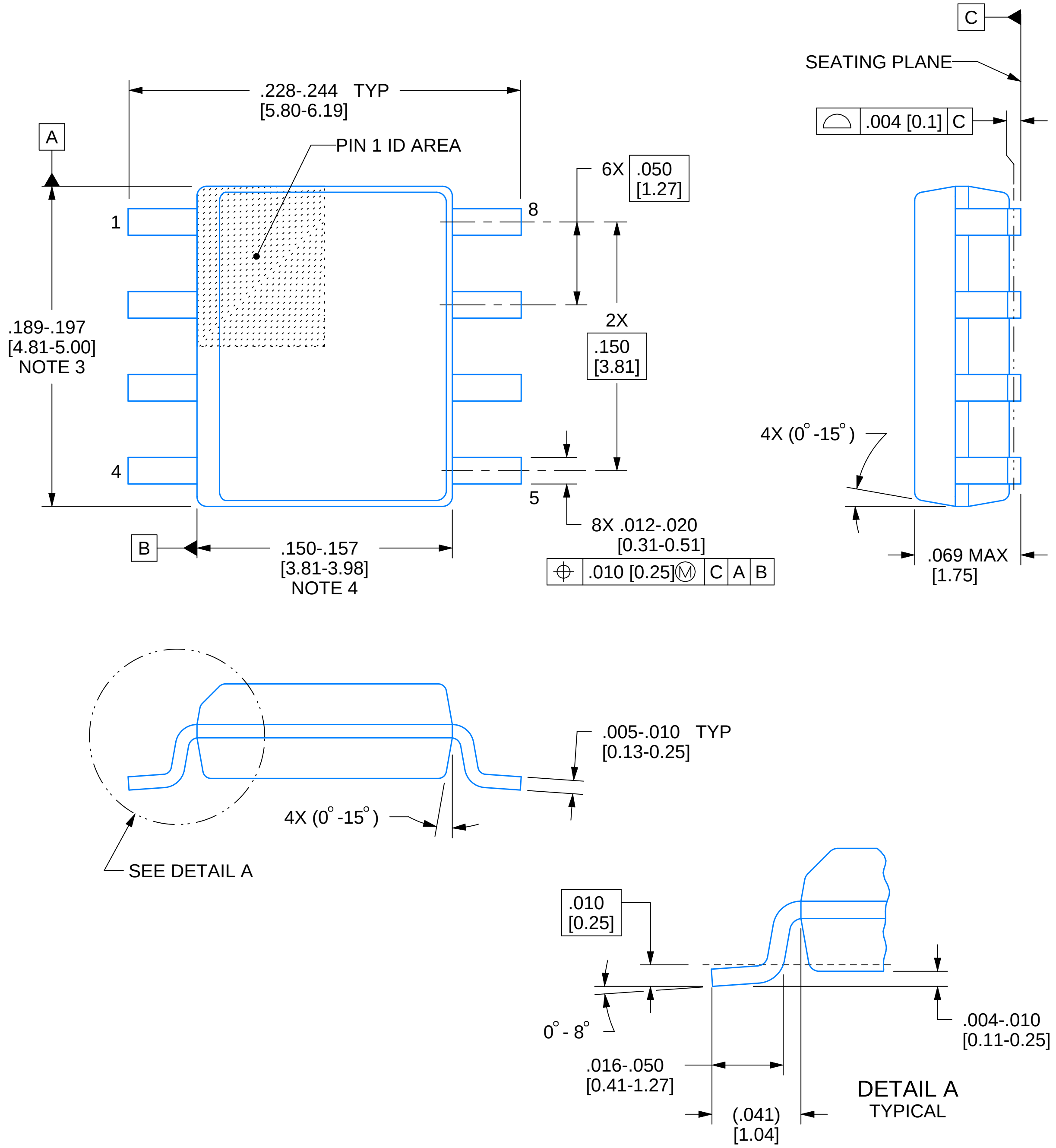
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2313QDGKRQ1	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA2313QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2313QDRQ1	SOIC	D	8	2500	340.5	336.1	25.0



PACKAGE OUTLINE

SOIC - 1.75 mm max height

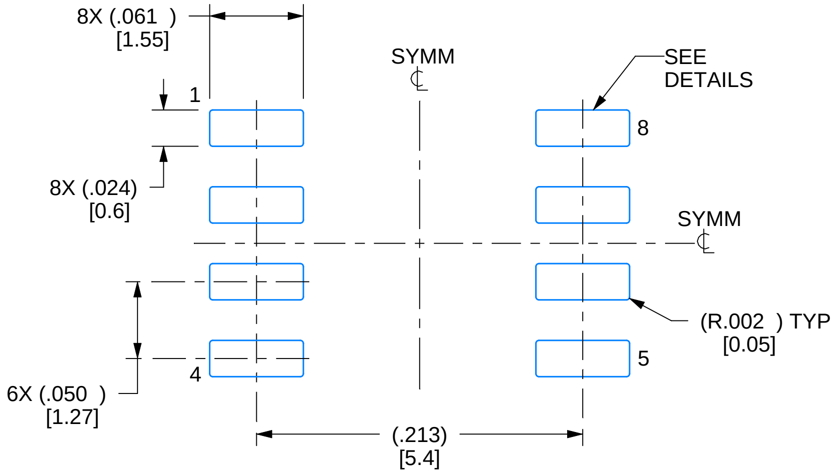
SMALL OUTLINE INTEGRATED CIRCUIT



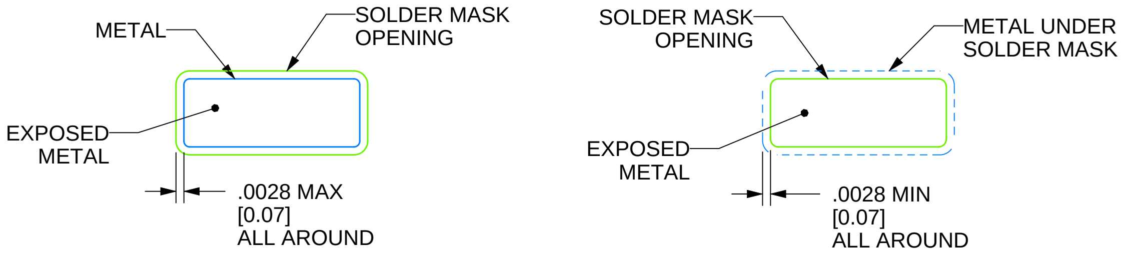
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



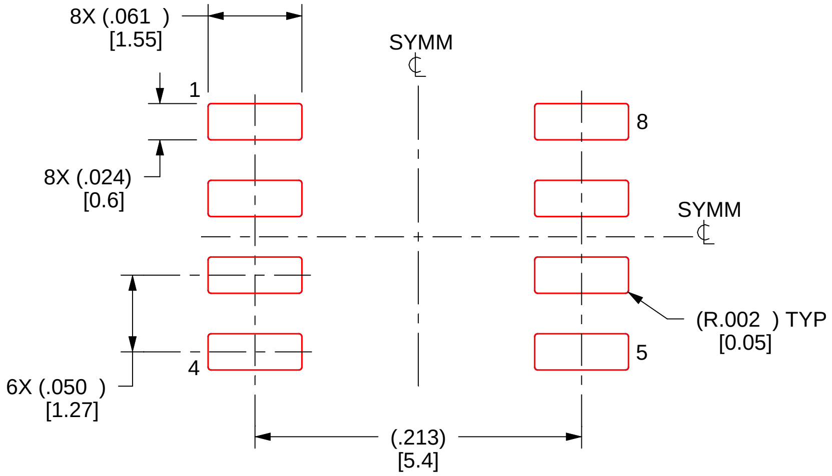
NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

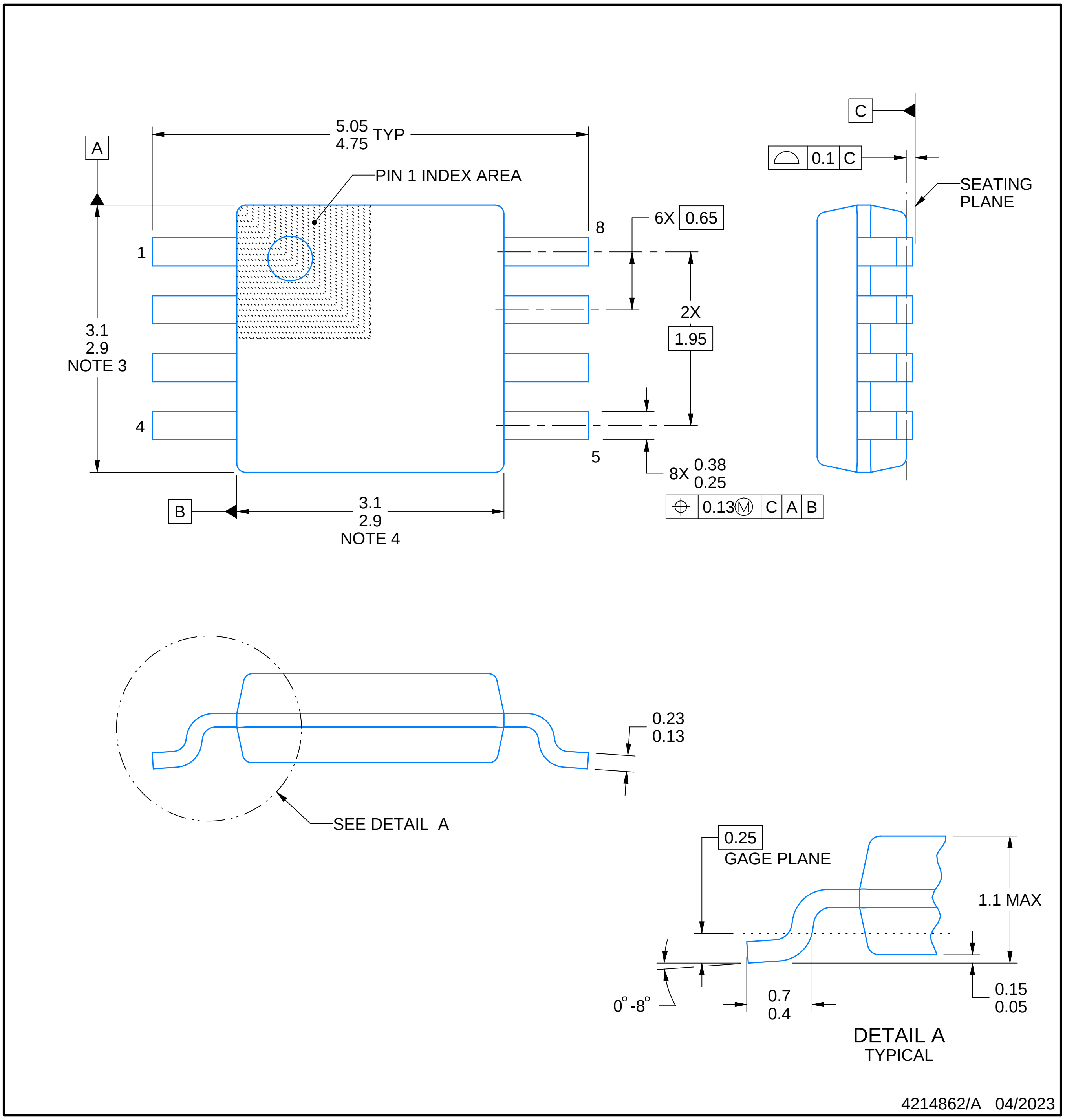
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

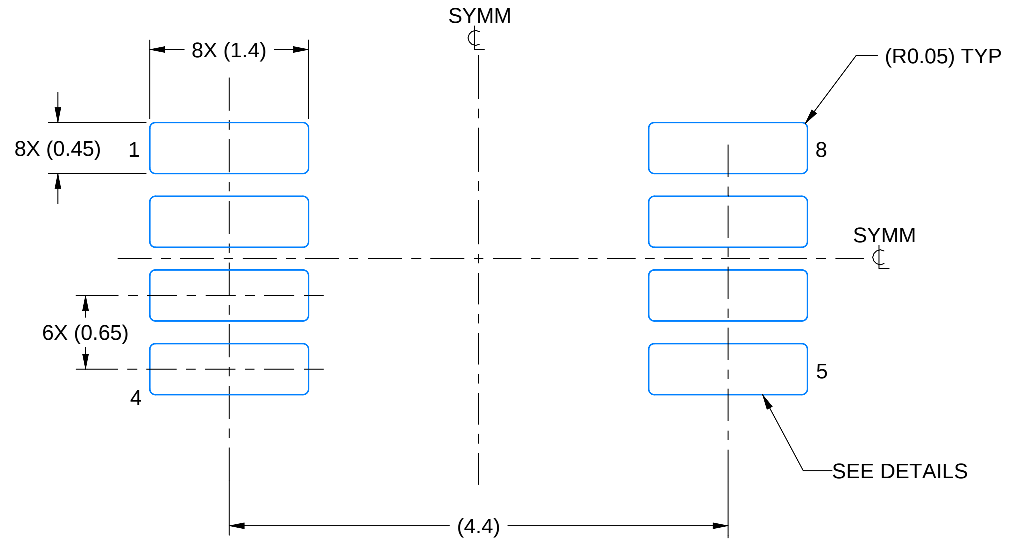


4214862/A 04/2023

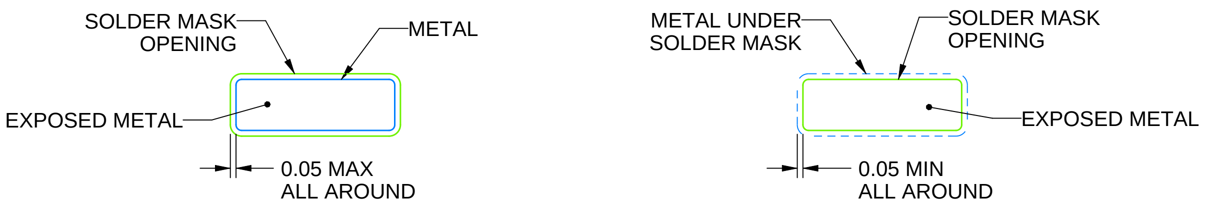
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



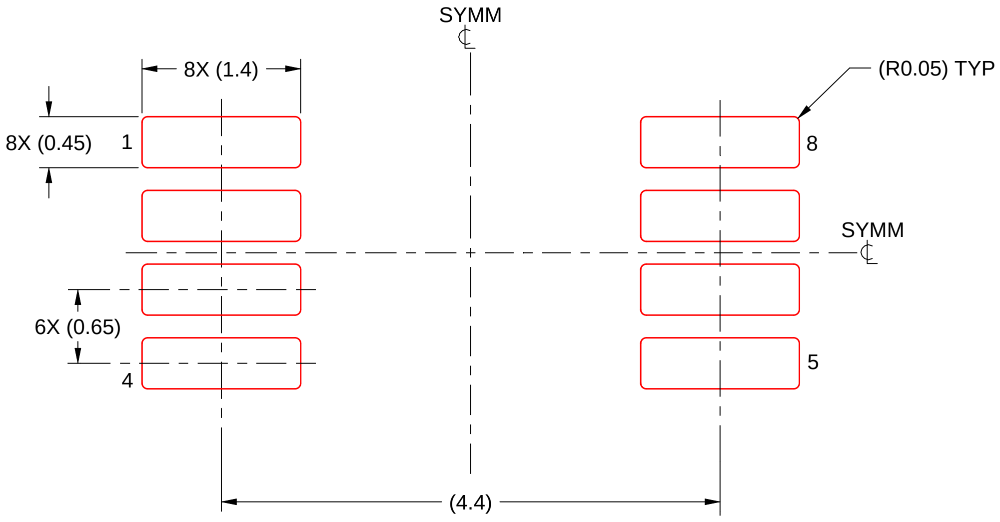
NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated