

OPAx310 High Output Current, Fast Shutdown, Low Voltage (1.5V to 5.5V), RRIO, 3MHz Operational Amplifier

1 Features

- High output current: $\pm 150\text{mA}$ typical I_{SC} at 5.5V
- Fast enable from shutdown: $0.9\mu\text{s}$ typical
- Wide operational supply voltage: 1.5V to 5.5V
- Low input offset voltage: $\pm 250\mu\text{V}$ typical
- Fail-safe inputs: No diode from inputs to $V+$
- Optimized quiescent current: $165\mu\text{A}/\text{ch}$ typical
- Rail-to-rail input and output
- Gain bandwidth product: 3MHz typical at 5.5V
- Thermal noise floor: $16\text{nV}/\sqrt{\text{Hz}}$ typical
- Unity-gain stable
- Drives up to 250pF without sustained oscillations
- Internal RFI and EMI filtered input pins
- Operating temperature range: -40°C to 125°C

2 Applications

- [Optical modules](#)
- [Reference buffers, guard amplifiers](#)
- [Microphone pre-amplifiers](#)
- [Lighting and LED Drivers](#)
- [4-20mA loop drivers](#)
- [Programmable current source](#)
- [Low side current sensing circuitry](#)

3 Description

The OPAx310 family of op amps includes single (OPA310), dual (OPA2310), and quad-channel (OPA4310), low-voltage (1.5V to 5.5V), high output current operational amplifiers (op amps) with rail-to-rail input and output swing capabilities. The OPAx310S also features a very fast shutdown response and has a typical enable time of $0.9\mu\text{s}$ that allows for power savings when the application involves duty cycling the amplifier signal chain. OPAx310 family has a robust ESD performance with fail safe input ESD structure where there are no diodes connected from inputs to the positive power supply rail.

OPAx310 is offered in power pad, standard, small size package variants and has an internal current limit protection, thermal shutdown protection that enables additional robustness when operating with high output current. OPAx310 can swing very close to the rails and has a short-circuit current of 75mA minimum across temperature at 5.5V power supply. Additional output current capability can be achieved by carefully connecting multiple op amps in parallel. OPAx310 devices are an excellent choice for LED driver, LCD driver, laser driver, TEC driver applications and can also be used as a reference buffer, guard amplifier, or as a discrete LDO.

The robust design of the OPAx310 family simplifies circuit design. These op amps feature an integrated RFI and EMI rejection filter with no-phase reversal in input overdrive conditions. These devices also deliver excellent AC performance with a gain bandwidth of 3MHz and can drive up to 250pF of capacitor load with no sustained oscillations, enabling designers to achieve both improved performance and a lower-power consumption.

Device Information

PART NUMBER ⁽¹⁾	CHANNEL COUNT	PACKAGE ⁽²⁾	PACKAGE SIZE ⁽⁴⁾
OPA310	Single	DBV (SOT-23, 5)	$2.9\text{mm} \times 2.8\text{mm}$
		DCK (SC70, 5)	$2.1\text{mm} \times 1.25\text{mm}$
		DPW (X2SON, 5) ⁽³⁾	$0.8\text{mm} \times 0.8\text{mm}$
		DRL (SOT-5X3, 5) ⁽³⁾	$1.6\text{mm} \times 1.6\text{mm}$
OPA310S	Single, Shutdown	DBV (SOT-23, 6)	$2.9\text{mm} \times 2.8\text{mm}$
		DCK (SC70, 6)	$2\text{mm} \times 1.25\text{mm}$
OPA2310	Dual	D (SOIC, 8)	$4.9\text{mm} \times 6\text{mm}$
		DDF (SOT-23, 8) ⁽³⁾	$2.9\text{mm} \times 2.8\text{mm}$
		DSG (WSON, 8)	$2\text{mm} \times 2\text{mm}$
		DGK (VSSOP, 8)	$3\text{mm} \times 4.9\text{mm}$
		PW (TSSOP, 8) ⁽³⁾	$3\text{mm} \times 6.4\text{mm}$
OPA2310S	Dual, Shutdown	RUG (X2QFN, 10)	$1.5\text{mm} \times 2\text{mm}$
		DGQ (HVSSOP, 10) ⁽³⁾	$3\text{mm} \times 4.9\text{mm}$
OPA4310	Quad	D (SOIC, 14)	$8.65\text{mm} \times 6\text{mm}$
		PW (TSSOP, 14)	$5\text{mm} \times 6.4\text{mm}$
		RUC (X2QFN, 14) ⁽³⁾	$2\text{mm} \times 2\text{mm}$
OPA4310S	Quad, Shutdown	RTE (WQFN, 16)	$3\text{mm} \times 3\text{mm}$
		DYY (SOT-23, 16) ⁽³⁾	$4.2\text{mm} \times 2\text{mm}$

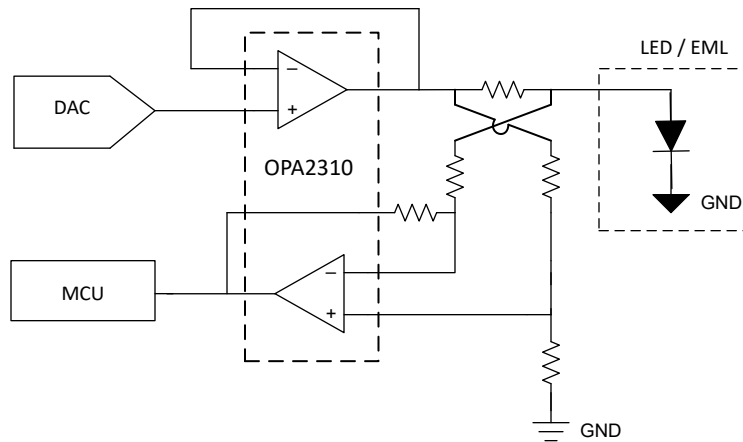
(1) See [Section 4](#)

(2) For more information, [Section 11](#).

(3) Package is for preview only.

(4) The package size (length \times width) is a nominal value and includes pins, where applicable.





LED / EML Biasing With Current Sense

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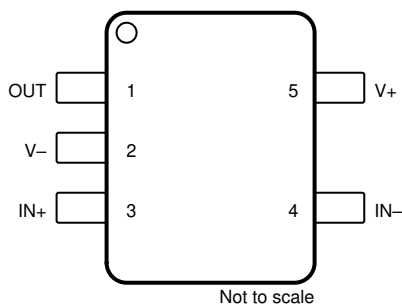
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4 Device Comparison Table

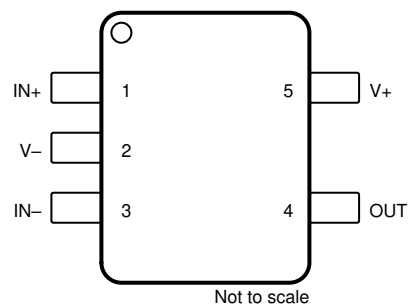
DEVICE	NO. OF CHANNELS	SHDN	PACKAGE LEADS													
			SC70 DCK	SOIC D	SOT-23 DBV	SOT-23 DDF ⁽¹⁾	SOT-553 DRL ⁽¹⁾	SOT-23 DYY ⁽¹⁾	TSSOP PW	VSSOP DGK	HVSSOP DGQ ⁽¹⁾	WQFN RTE	WSON DSG	X2QFN RUC ⁽¹⁾	X2SON DPW ⁽¹⁾	X2QFN RUG
OPA310	1	NO	5	—	5		5	—	—	—	—	—	—	—	5	—
OPA310S	1	YES	6	—	6		—	—	—	—	—	—	—	—	—	—
OPA2310	2	NO	—	8	—	8	—	—	8	8	—	—	8	—	—	—
OPA2310S	2	YES	—	—	—	—	—	—	—	—	10	—	—	—	—	10
OPA4310	4	NO	—	14	—	—	—	—	14	—	—	—	—	14	—	—
OPA4310S	4	YES	—	—	—	—	—	16	—	—	—	16	—	—	—	—

(1) Packages are preview only.

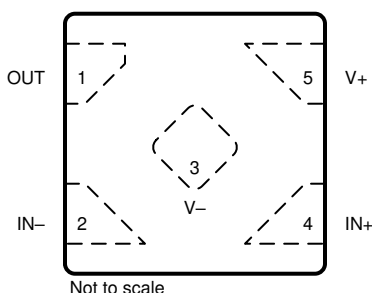
5 Pin Configuration and Functions



**Figure 5-1. OPA310 DBV Package,
5-Pin SOT-23
(Top View)**



**Figure 5-2. OPA310 DCK and DRL Package,
5-Pin SC70 and 5-Pin SOT-5X3
(Top View)**

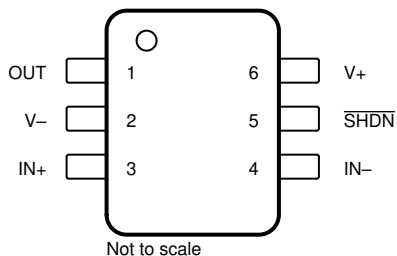


**Figure 5-3. OPA310 DPW Package,
5-Pin X2SON
(Top View)**

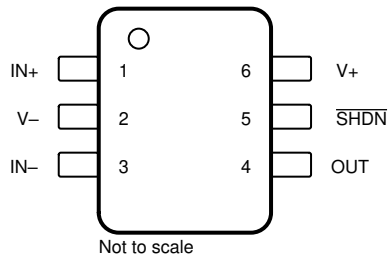
Table 5-1. Pin Functions: OPA310

NAME	PIN			(1) TYPE	DESCRIPTION
	SOT-23	SC70, SOT-5X3	X2SON		
IN–	4	3	2	I	Inverting input
IN+	3	1	4	I	Noninverting input
OUT	1	4	1	O	Output
V–	2	2	3	I	Negative (low) supply or ground (for single-supply operation)
V+	5	5	5	I	Positive (high) supply

(1) I = input, O = output



**Figure 5-4. OPA310S DBV Package,
6-Pin SOT-23
(Top View)**



**Figure 5-5. OPA310S DCK Package,
6-Pin SC70
(Top View)**

Table 5-2. Pin Functions: OPA310S

PIN			(1)TYPE	DESCRIPTION
NAME	SOT-23	SC70		
IN–	4	3	I	Inverting input
IN+	3	1	I	Noninverting input
OUT	1	4	O	Output
SHDN	5	5	I	Shutdown: low = amp disabled, high = amp enabled See Shutdown Function for more information
V–	2	2	I	Negative (low) supply or ground (for single-supply operation)
V+	6	6	I	Positive (high) supply

(1) I = input, O = output

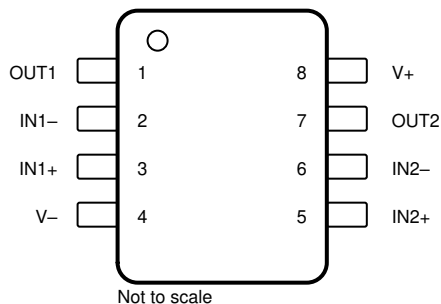
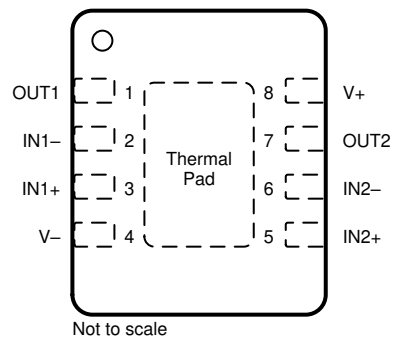


Figure 5-6. OPA2310 D, DDF, DGK, and PW Package, 8-Pin SOIC, SOT-23-THIN, VSSOP, and TSSOP (Top View)



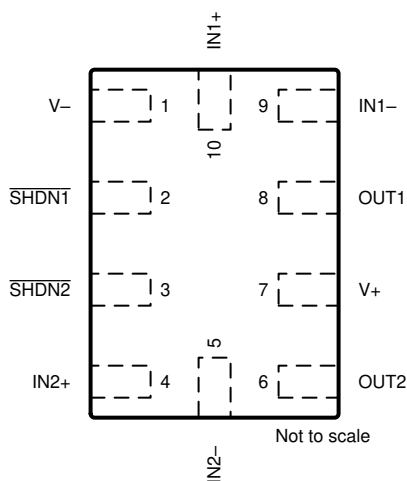
Connect exposed thermal pad to V-. See [Section 7.3.10](#) for more information.

Figure 5-7. OPA2310 DSG Package, 8-Pin WSON with Exposed Thermal Pad (Top View)

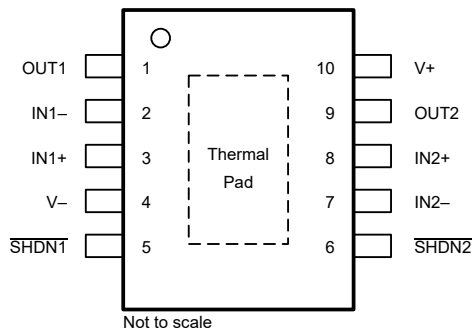
Table 5-3. Pin Functions: OPA2310

PIN		(1) TYPE	DESCRIPTION
NAME	NO.		
IN1–	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2–	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V–	4	I	Negative (low) supply or ground (for single-supply operation)
V+	8	I	Positive (high) supply

(1) I = input, O = output



**Figure 5-8. OPA2310S RUG Package,
10-Pin X2QFN
(Top View)**

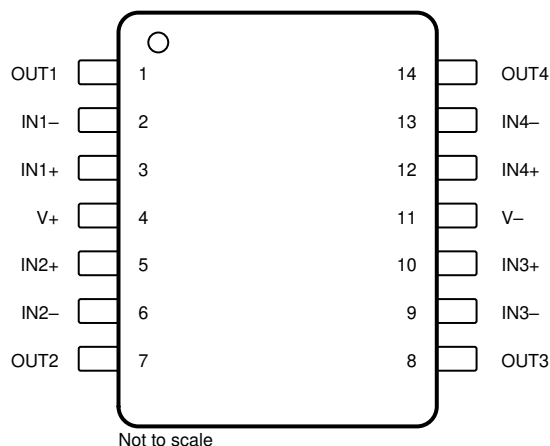


**Figure 5-9. OPA2310S DGQ Package,
10-Pin HVSSOP
(Top View)**

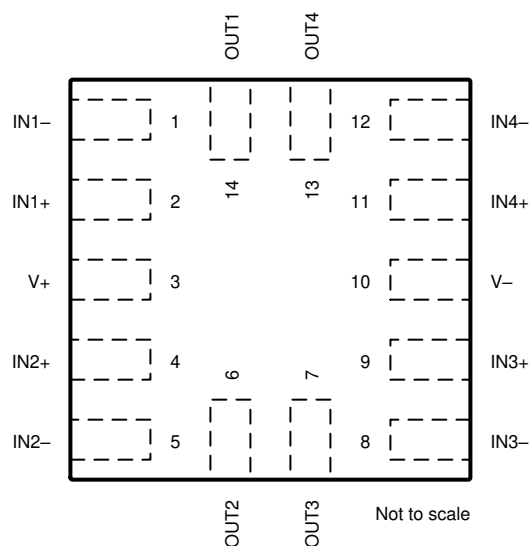
Table 5-4. Pin Functions: OPA2310S

PIN			(1) TYPE	DESCRIPTION
NAME	X2QFN	HVSSOP		
IN1–	9	2	I	Inverting input, channel 1
IN1+	10	3	I	Noninverting input, channel 1
IN2–	5	7	I	Inverting input, channel 2
IN2+	4	8	I	Noninverting input, channel 2
OUT1	8	1	O	Output, channel 1
OUT2	6	9	O	Output, channel 2
SHDN1	2	5	I	Shutdown: low = amp disabled, high = amp enabled, channel 1 See Shutdown Function for more information
SHDN2	3	6	I	Shutdown: low = amp disabled, high = amp enabled, channel 2 See Shutdown Function for more information
V–	1	4	I	Negative (low) supply or ground (for single-supply operation)
V+	7	10	I	Positive (high) supply

(1) I = input, O = output



**Figure 5-10. OPA4310 D and PW Package,
14-Pin SOIC and TSSOP
(Top View)**

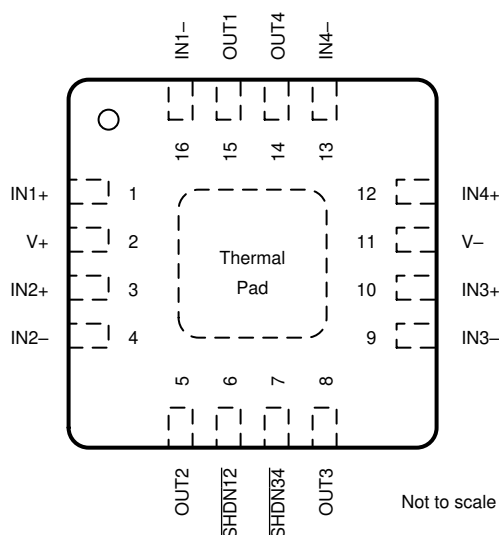


**Figure 5-11. OPA4310 RUC Package,
14-Pin X2QFN
(Top View)**

Table 5-5. Pin Functions: OPA4310

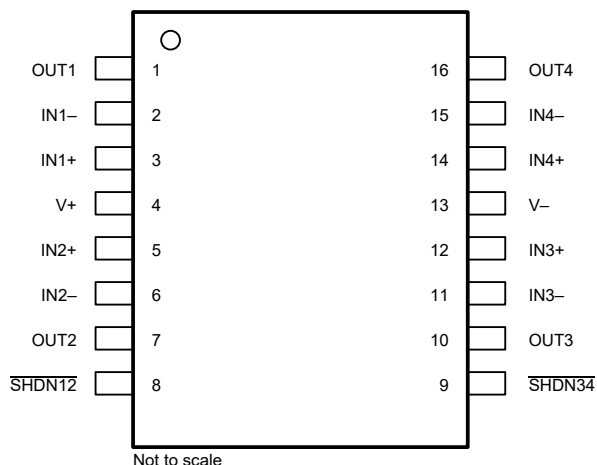
NAME	PIN		(1)TYPE	DESCRIPTION
	SOIC, TSSOP	X2QFN		
IN1–	2	1	I	Inverting input, channel 1
IN1+	3	2	I	Noninverting input, channel 1
IN2–	6	5	I	Inverting input, channel 2
IN2+	5	4	I	Noninverting input, channel 2
IN3–	9	8	I	Inverting input, channel 3
IN3+	10	9	I	Noninverting input, channel 3
IN4–	13	12	I	Inverting input, channel 4
IN4+	12	11	I	Noninverting input, channel 4
OUT1	1	14	O	Output, channel 1
OUT2	7	6	O	Output, channel 2
OUT3	8	7	O	Output, channel 3
OUT4	14	13	O	Output, channel 4
V–	11	10	I	Negative (low) supply or ground (for single-supply operation)
V+	4	3	I	Positive (high) supply

(1) I = input, O = output



A. Connect thermal pad to V–.

**Figure 5-12. OPA4310S RTE Package,
16-Pin WQFN With Exposed Thermal Pad
(Top View)**



A. Connect thermal pad to V–.

**Figure 5-13. OPA4310S DYY Package,
16-Pin SOT-23-THIN
(Top View)**

Table 5-6. Pin Functions: OPA4310S

NAME	PIN		(1)TYPE	DESCRIPTION
	WQFN	SOT-23-THIN		
IN1+	1	3	I	Noninverting input, channel 1
IN1–	16	2	I	Inverting input, channel 1
IN2+	3	5	I	Noninverting input, channel 2
IN2–	4	6	I	Inverting input, channel 2
IN3+	10	12	I	Noninverting input, channel 3
IN3–	9	11	I	Inverting input, channel 3
IN4+	12	14	I	Noninverting input, channel 4
IN4–	13	15	I	Inverting input, channel 4
SHDN12	6	8	I	Shutdown: low = amp disabled, high = amp enabled, channel 1 and 2. See Shutdown Function for more information
SHDN34	7	9	I	Shutdown: low = amp disabled, high = amp enabled, channel 3 and 4. See Shutdown Function for more information
OUT1	15	1	O	Output, channel 1
OUT2	5	7	O	Output, channel 2
OUT3	8	10	O	Output, channel 3
OUT4	14	16	O	Output, channel 4
V–	11	13	I	Negative (low) supply or ground (for single-supply operation)
V+	2	4	I	Positive (high) supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
Supply voltage, $V_S = (V+) - (V-)$	Supply voltage, $V_S = (V+) - (V-)$	0	7	V
Signal input pins	Common-mode voltage ^{(2) (3)}	– 0.5	6.0	V
	Differential voltage ^{(2) (3)}		±6.0	V
	Current ⁽³⁾	–10	10	mA
Output short-circuit ⁽⁴⁾		Continuous		
Operating ambient temperature, T_A		–55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) Input pins can swing beyond (V+) as long as they stay within 6.0 V. No diode structure from input pins to (V+).
- (3) Input pins are diode-clamped to (V–). Input signals that 0.3 V below (V–) must be current-limited to 10 mA or less.
- (4) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

PART NUMBER				VALUE	UNIT
OPA2310	$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±4000	V
OPA2310	$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JS-002 ⁽²⁾	±1500	V
OPA310, OPA4310	$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±8000	V
OPA310, OPA4310	$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JS-002 ⁽²⁾	±1500	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	1.5	5.5	V
V_I	Input voltage range	– 0.1	5.6	V
T_A	Specified temperature	–40	125	°C

6.4 Thermal Information for Single Channel

THERMAL METRIC ⁽¹⁾		OPA310				OPA310S		UNIT
		DBV (SOT-23)	DCK (SC70)	DPW ⁽²⁾ (X2SON)	DRL ⁽²⁾ (X2SON)	DBV (SOT-23)	DCK (SC70)	
		5 PINS	5 PINS	5 PINS	5 PINS	6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	211.5	214.6	TBD	TBD	190.7	195.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	109.4	110.0	TBD	TBD	110.5	122.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	77.8	60.7	TBD	TBD	70.8	55.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	45.2	32.1	TBD	TBD	47.4	38.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	77.5	60.4	TBD	TBD	70.5	55.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	TBD	TBD	n/a	n/a	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) This package option is on preview.

6.5 Thermal Information for Dual Channel

THERMAL METRIC ⁽¹⁾		OPA2310					OPA2310S		UNIT
		DSG (WSON)	D (SOIC)	DDF ⁽²⁾ (SOT-23-8)	DGK (VSSOP)	PW ⁽²⁾ (TSSOP)	DGQ ⁽²⁾ (HVSSOP)	RUG (X2QFN)	
		8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	10 PINS	10 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	90.1	139.0	TBD	187.7	TBD	TBD	179.4	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	112.1	81.2	TBD	78.1	TBD	TBD	66.7	°C/W
R _{θJB}	Junction-to-board thermal resistance	56.3	82.4	TBD	109.5	TBD	TBD	104.5	°C/W
ψ _{JT}	Junction-to-top characterization parameter	9.2	31.3	TBD	17.9	TBD	TBD	1.4	°C/W
ψ _{JB}	Junction-to-board characterization parameter	56.3	81.6	TBD	107.9	TBD	TBD	104.2	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	31.8	N/A	TBD	N/A	TBD	TBD	n/a	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) This package option is on preview.

6.6 Thermal Information for Quad Channel

THERMAL METRIC ⁽¹⁾		OPA4310			OPA4310S		UNIT
		RUC ⁽²⁾ (X2QFN)	D (SOIC)	PW (TSSOP)	RTE (WQFN)	DYY ⁽²⁾ (SOT)	
		14 PINS	14 PINS	14 PINS	16 PINS	16 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	TBD	101.5	128.2	57.6	TBD	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	TBD	57.8	58.7	62.4	TBD	°C/W
R _{θJB}	Junction-to-board thermal resistance	TBD	58.0	71.4	32.9	TBD	°C/W
ψ _{JT}	Junction-to-top characterization parameter	TBD	20.9	13.0	3.4	TBD	°C/W
ψ _{JB}	Junction-to-board characterization parameter	TBD	57.6	70.8	32.9	TBD	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	TBD	n/a	n/a	16.6	TBD	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) This package option is on preview.

6.7 Electrical Characteristics

For $V_S = (V+) - (V-) = 1.5\text{ V to }5.5\text{ V}$ ($\pm 0.75\text{ V to } \pm 2.75\text{ V}$) at $T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V _{OS}	Input offset voltage	V _{CM} = V−		±0.25		±1.3	mV
		V _{CM} = V−	T _A = −40°C to 125°C			±1.4	
dV _{OS} /dT	Input offset voltage drift	V _{CM} = V−	T _A = −40°C to 125°C		±0.5		µV/°C
PSRR	Input offset voltage versus power supply	V _S = 1.5 V to 5.5 V , V _{CM} = V−			±10	±50	µV/V
	Channel separation	f = 10 kHz			±1		µV/V
INPUT BIAS CURRENT							
I _B	Input bias current ⁽¹⁾	V _S = 1.8 V and V _S = 5 V			±1	±30	pA
I _{OS}	Input offset current ⁽¹⁾	V _S = 1.8 V and V _S = 5 V			±0.5	±25	pA
NOISE							
E _N	Input voltage noise	f = 0.1 to 10 Hz			4		µV _{PP}
e _N	Input voltage noise density	f = 100 Hz			32		nV/√Hz
		f = 1 kHz			16		
		f = 10 kHz			13		
i _N	Input current noise ⁽³⁾	f = 1 kHz			10		fA/√Hz
INPUT VOLTAGE RANGE							
V _{CM}	Common-mode voltage range ⁽¹⁾	V _S = 1.8 V	T _A = −40°C to 125°C	(V−)		(V+)	V
	Common-mode voltage range ⁽¹⁾	V _S = 5.5 V	T _A = −40°C to 125°C	(V−) − 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	V _S = 1.8 V, (V−) ≤ V _{CM} ≤ (V+) − 0.6 V		75	85		dB
		V _S = 1.8 V, (V−) ≤ V _{CM} ≤ (V+) − 0.6 V	T _A = −40°C to 125°C	65	78		dB
		V _S = 5.5 V, (V−) ≤ V _{CM} ≤ (V+) − 0.6 V		83	95		dB
		V _S = 5.5 V, (V−) ≤ V _{CM} ≤ (V+) − 0.6 V	T _A = −40°C to 125°C	75	85		dB
		Full Range: V _S = 1.8 V, (V−) ≤ V _{CM} ≤ (V+)	T _A = −40°C to 125°C	57.5	70		
		Full Range: V _S = 5.5 V (V−) − 0.1 V ≤ V _{CM} ≤ (V+) + 0.1 V	T _A = −40°C to 125°C	66.5	80		
INPUT IMPEDANCE							
Z _{ID}	Differential Input Impedance				80 1.4		GΩ pF
Z _{ICM}	Common-mode Input Impedance				100 0.5		GΩ pF

6.7 Electrical Characteristics (continued)

For $V_S = (V_+) - (V_-) = 1.5 \text{ V to } 5.5 \text{ V}$ ($\pm 0.75 \text{ V to } \pm 2.75 \text{ V}$) at $T_A = 25^\circ\text{C}$, $R_L = 10 \text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{O\ UT} = V_S / 2$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	$V_S = 1.8 \text{ V}$, $(V_-) + 0.05 \text{ V} < V_O < (V_+) - 0.05 \text{ V}$, $R_L = 10 \text{ k}\Omega$ to $V_S / 2$	102	115		dB
	Open-loop voltage gain ⁽²⁾	$V_S = 1.8 \text{ V}$, $(V_-) + 0.10 \text{ V} < V_O < (V_+) - 0.10 \text{ V}$, $R_L = 2 \text{ k}\Omega$ to $V_S / 2$	95	105		dB
		$V_S = 5.5 \text{ V}$, $(V_-) + 0.10 \text{ V} < V_O < (V_+) - 0.10 \text{ V}$, $R_L = 10 \text{ k}\Omega$ to $V_S / 2$	109	125		dB
	Open-loop voltage gain	$V_S = 5.5 \text{ V}$, $(V_-) + 0.15 \text{ V} < V_O < (V_+) - 0.15 \text{ V}$, $R_L = 2 \text{ k}\Omega$ to $V_S / 2$	105	115		dB
		$T_A = -40^\circ\text{C to } 125^\circ\text{C}$	90	100		dB
				90		
				105		
			90	100		
	Open-loop voltage gain ⁽⁶⁾	$V_S = 3.3 \text{ V}$, $(V_-) + 0.25 \text{ V} < V_O < (V_+) - 0.25 \text{ V}$, $I_L = \pm 50 \text{ mA}$, $T_A = 25^\circ\text{C}$	80	102		dB
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	$V_S = 1.8 \text{ V}$, $G = +1$, $R_L = 10 \text{ k}\Omega$, $C_L = 100 \text{ pF}$		2.5		MHz
		$V_S = 5.5 \text{ V}$, $G = +1$, $R_L = 10 \text{ k}\Omega$, $C_L = 100 \text{ pF}$		3		MHz
SR	Slew rate	$V_S = 1.8 \text{ V}$, $G = +1$, $R_L = 10 \text{ k}\Omega$		2.8		V/ μs
		$V_S = 5.5 \text{ V}$, $G = +1$, $R_L = 10 \text{ k}\Omega$		3		V/ μs
THD+N	Total harmonic distortion + noise ⁽⁴⁾	$V_S = 5.5 \text{ V}$, $G = +1$, $V_O = 1 \text{ V}_{RMS}$, $f = 1 \text{ kHz}$, $R_L = 10 \text{ k}\Omega$ to $V_S / 2$		0.0005		%
		$V_S = 5.5 \text{ V}$, $G = +1$, $V_O = 1 \text{ V}_{RMS}$, $f = 1 \text{ kHz}$, $R_L = 2 \text{ k}\Omega$ to $V_S / 2$		0.0035		%
		$V_S = 5.5 \text{ V}$, $G = +1$, $V_O = 1 \text{ V}_{RMS}$, $f = 1 \text{ kHz}$, $R_L = 600 \Omega$ to $V_S / 2$		0.0080		%
t_s	Settling time	To 0.1%, $V_S = 5.5 \text{ V}$, $V_{STEP} = 4 \text{ V}$, $G = +1$, $C_L = 10 \text{ pF}$		1.8		μs
		To 0.1%, $V_S = 5.5 \text{ V}$, $V_{STEP} = 2 \text{ V}$, $G = +1$, $C_L = 10 \text{ pF}$		1.3		
		To 0.01%, $V_S = 5.5 \text{ V}$, $V_{STEP} = 4 \text{ V}$, $G = +1$, $C_L = 10 \text{ pF}$		2.3		
		To 0.01%, $V_S = 5.5 \text{ V}$, $V_{STEP} = 2 \text{ V}$, $G = +1$, $C_L = 10 \text{ pF}$		1.6		
PM	Phase margin	$G = +1$, $R_L = 10 \text{ k}\Omega$ connected to $V_S / 2$, $C_L = 10 \text{ pF}$		60		°
C_L Drive	Cap Load Drive	$G = +1$, $R_L = 10 \text{ k}\Omega$ connected to $V_S / 2$, Phase Margin = 40°		75		pF
		$G = +1$, $R_L = 10 \text{ k}\Omega$ connected to $V_S / 2$, No Sustained Oscillations		250		pF
$t_{overload}$	Overload recovery time	$V_{IN} \times \text{gain} > V_S$		0.6		μs
EMIRR	Electro-magnetic interference rejection ratio	$f = 1.8 \text{ GHz}$, $V_{IN_EMIRR} = 100 \text{ mV}$		75		dB

6.7 Electrical Characteristics (continued)

For $V_S = (V_+) - (V_-) = 1.5 \text{ V to } 5.5 \text{ V}$ ($\pm 0.75 \text{ V to } \pm 2.75 \text{ V}$) at $T_A = 25^\circ\text{C}$, $R_L = 10 \text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
V _{OH}	Voltage output swing from positive rail	V _S = 1.8 V, R _L = 2 kΩ to V _S / 2			10	21	mV
		V _S = 1.8 V, R _L = 10 kΩ to V _S / 2			2	11	
		V _S = 1.8 V, R _L = 2 kΩ to V _S / 2	T _A = −40°C to 125°C			51	
		V _S = 1.8 V, R _L = 10 kΩ to V _S / 2	T _A = −40°C to 125°C			26	
		V _S = 5.5 V, R _L = 2 kΩ to V _S / 2			3.5	20	
		V _S = 5.5 V, R _L = 10 kΩ to V _S / 2			0.75	9	
		V _S = 5.5 V, R _L = 2 kΩ to V _S / 2	T _A = −40°C to 125°C			30	
		V _S = 5.5 V, R _L = 10 kΩ to V _S / 2	T _A = −40°C to 125°C			14	
V _{OL}	Voltage output swing from negative rail	V _S = 1.8 V, R _L = 2 kΩ to V _S / 2			5.5	15	
		V _S = 1.8 V, R _L = 10 kΩ to V _S / 2			1.2	10	
		V _S = 1.8 V, R _L = 2 kΩ to V _S / 2	T _A = −40°C to 125°C			45	
		V _S = 1.8 V, R _L = 10 kΩ to V _S / 2	T _A = −40°C to 125°C			25	
		V _S = 5.5 V, R _L = 2 kΩ to V _S / 2			3.5	17.5	
		V _S = 5.5 V, R _L = 10 kΩ to V _S / 2			0.75	10	
		V _S = 5.5 V, R _L = 2 kΩ to V _S / 2	T _A = −40°C to 125°C			27.5	
		V _S = 5.5 V, R _L = 10 kΩ to V _S / 2	T _A = −40°C to 125°C			11	
I _{SC}	Short-circuit current ⁽⁵⁾	V _S = 1.8 V			±20		mA
	Short-circuit current ^{(2) (5)}	V _S = 1.8 V, T _A = −40°C to 125°C			±6		mA
	Short-circuit current ⁽⁵⁾	V _S = 5.5 V, OPA2310			±75	±150	mA
I _{SC}	Short-circuit current ⁽⁵⁾	V _S = 5.5 V, OPA310 and OPA4310			±110		mA
Z _O	Open-loop output impedance	f = 10 kHz			1000		Ω
POWER SUPPLY							
I _Q	Quiescent current per amplifier	V _S = 1.5 V, I _O = 0 A, $\overline{\text{SHDN}}$ = V+ for shutdown devices			165	190	μA
		V _S = 1.5 V, I _O = 0 A, $\overline{\text{SHDN}}$ = V+ for shutdown devices	T _A = −40°C to 125°C		165	210	μA
		V _S = 5.5 V, I _O = 0 A, $\overline{\text{SHDN}}$ = V+ for shutdown devices			165	200	μA
			T _A = −40°C to 125°C			215	
	Power-on time	At T _A = 25°C, V _S = 5.5 V, V _S ramp rate > 0.3 V/μs			125		μs
SHUTDOWN							
I _{Q_SHDN}	Shutdown current per amplifier	All amplifiers disabled, $\overline{\text{SHDN}}$ = V−, OPA4310S			0.100	0.150	μA
		All amplifiers disabled, $\overline{\text{SHDN}}$ = V−, OPA310S			0.265	0.475	μA
I _{Q_SHDN}	Shutdown current per amplifier	All amplifiers disabled, $\overline{\text{SHDN}}$ = V−, OPA2310S			0.200	0.375	μA
I _{Q_SHDN}	Shutdown current per amplifier ⁽¹⁾	All amplifiers disabled, $\overline{\text{SHDN}}$ = V−, T _A = −40°C to 85°C, OPA4310S				0.300	μA
		All amplifiers disabled, $\overline{\text{SHDN}}$ = V−, T _A = −40°C to 85°C, OPA310S				0.700	μA
I _{Q_SHDN}	Shutdown current per amplifier ⁽¹⁾	All amplifiers disabled, $\overline{\text{SHDN}}$ = V−, T _A = −40°C to 85°C, OPA2310S				0.600	μA
Z _{OUT_SHDN}	Output impedance during shutdown	Amplifier disabled			43 11.5		GΩ pF

6.7 Electrical Characteristics (continued)

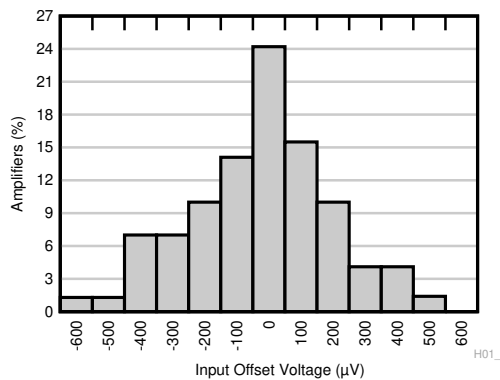
For $V_S = (V+) - (V-) = 1.5\text{ V to }5.5\text{ V}$ ($\pm 0.75\text{ V to } \pm 2.75\text{ V}$) at $T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SHDN_IH}	Logic high voltage (amplifier enabled)		$(V-) + 1.2$			V
V_{SHDN_IL}	Logic low voltage (amplifier disabled)			$(V-) + 0.2$		V
t_{ON}	Amplifier enable time (full shutdown) (7) (1)	$G = +1$, $V_{CM} = V_S / 2$, $V_O = 0.9 \times V_S / 2$, R_L connected to $V-$		1	1.6	μs
t_{OFF}	Amplifier disable time (7)	$G = +1$, $V_{CM} = V_S / 2$, $V_O = 0.1 \times V_S / 2$, R_L connected to $V-$		1		μs
I_{B_SHDN}	SHDN pin input bias current (per pin)	$(V+) \geq \overline{\text{SHDN}} \geq (V-) + 1\text{ V}$		50		nA
		$(V-) \leq \overline{\text{SHDN}} \leq (V-) + 0.2\text{ V}$		100		

- (1) Max data is specified based on characterization results.
- (2) Min data is specified based on characterization results.
- (3) Typical input current noise data is specified based on design simulation results.
- (4) Third-order filter; bandwidth = 80 kHz at -3 dB.
- (5) Short circuit current specified here is the average of sourcing and sinking short circuit currents.
- (6) A_{OL} is measured as the difference between $(V_{OSA} - V_{OSB}) / (V_{OUTA} - V_{OUTB})$. V_{OSA} is the offset measured when the OUT pin is biased at $(V+) - 0.25\text{ V}$ while the device sources 50 mA and V_{OSB} is the offset measured when the OUT pin is biased at $(V-) + 0.25\text{ V}$ while the device sinks 50 mA.
- (7) Disable time (t_{OFF}) and enable time (t_{ON}) are defined as the time interval between the 50% point of the signal applied to the $\overline{\text{SHDN}}$ pin and the point at which the output voltage reaches the 10% (disable) or 90% (enable) level.

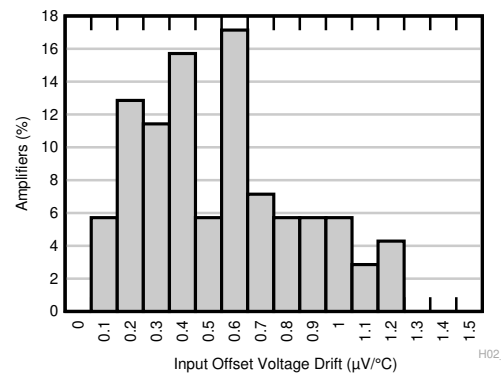
6.8 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_+ = 2.75\text{V}$, $V_- = -2.75\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)



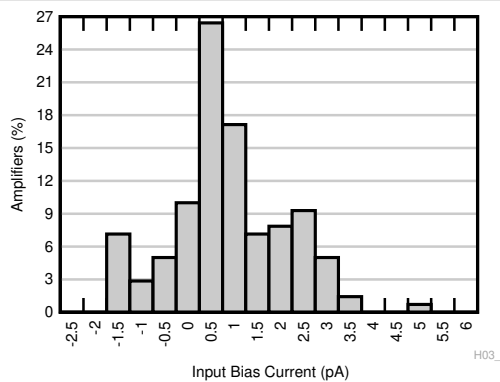
$V_S = 5.5\text{V}$ $V_{CM} = V_S / 2$ $T_A = 25^\circ\text{C}$
No. of devices = 70 Mean = $-36\mu\text{V}$ Sigma = $215\mu\text{V}$

Figure 6-1. Offset Voltage Distribution Histogram



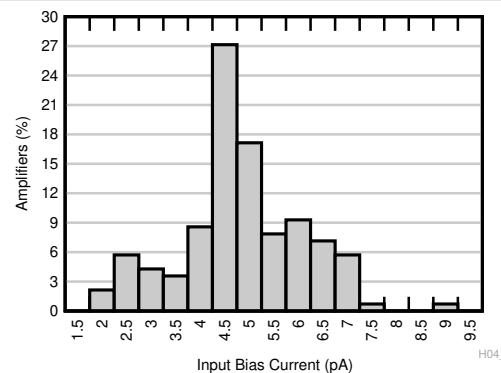
$V_S = 5.5\text{V}$ $V_{CM} = V_S / 2$ $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$
No. of devices = 70
Mean = $0.5\mu\text{V}/^\circ\text{C}$ Sigma = $0.3\mu\text{V}/^\circ\text{C}$

Figure 6-2. Offset Voltage Drift Distribution Histogram



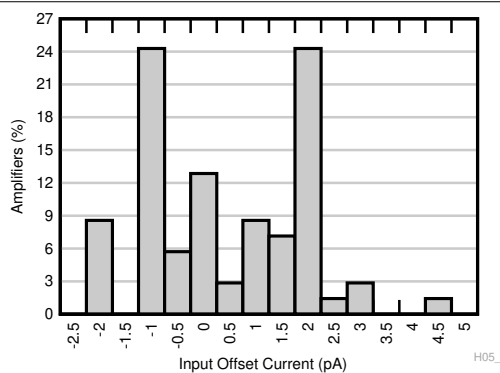
$V_S = 5.5\text{V}$ $V_{CM} = V_S / 2$ $T_A = 25^\circ\text{C}$
No. of devices = 140 Mean = 0.6pA Sigma = 1.2pA

Figure 6-3. Input Bias Current Distribution Histogram



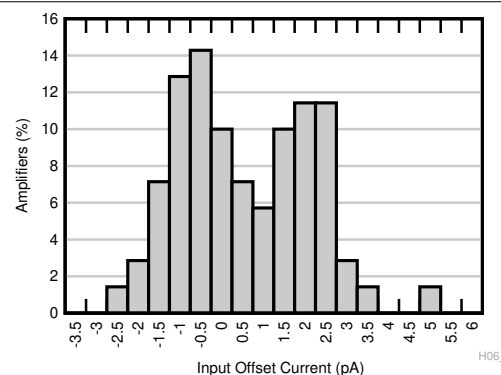
$V_S = 5.5\text{V}$ $V_{CM} = V_S / 2$ $T_A = 85^\circ\text{C}$
No. of devices = 140 Mean = 4.6pA Sigma = 1.3pA

Figure 6-4. Input Bias Current Distribution Histogram



$V_S = 5.5\text{V}$ $V_{CM} = V_S / 2$ $T_A = 25^\circ\text{C}$
No. of devices = 140 Mean = 0.2pA Sigma = 1.5pA

Figure 6-5. Input Offset Current Distribution Histogram



$V_S = 5.5\text{V}$ $V_{CM} = V_S / 2$ $T_A = 85^\circ\text{C}$
No. of devices = 70 Mean = 0.3pA Sigma = 1.6pA

Figure 6-6. Input Offset Current Distribution Histogram

6.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_+ = 2.75\text{V}$, $V_- = -2.75\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

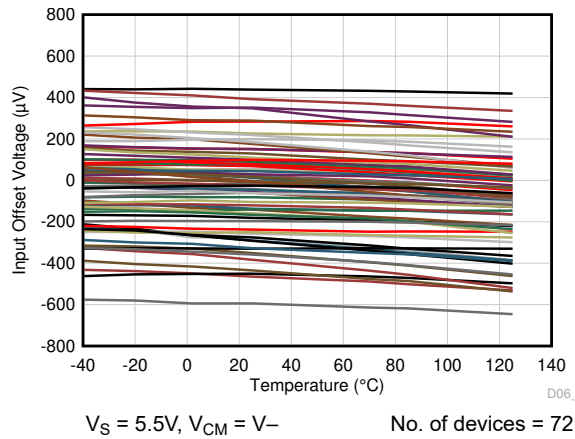


Figure 6-7. Input Offset Voltage vs Temperature

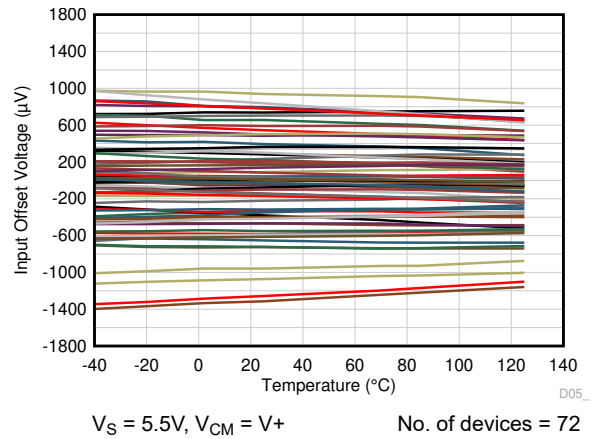


Figure 6-8. Input Offset Voltage vs Temperature

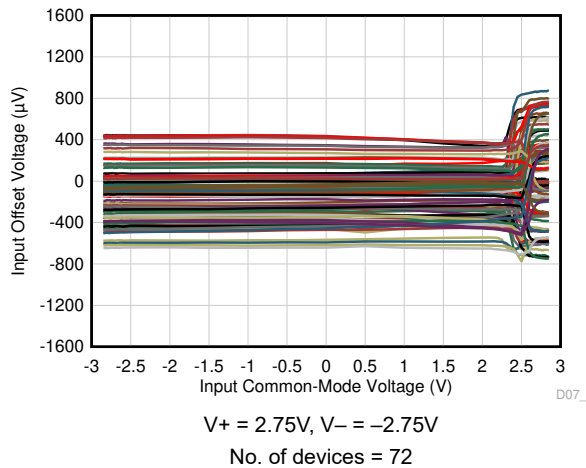


Figure 6-9. Offset Voltage vs Common-Mode

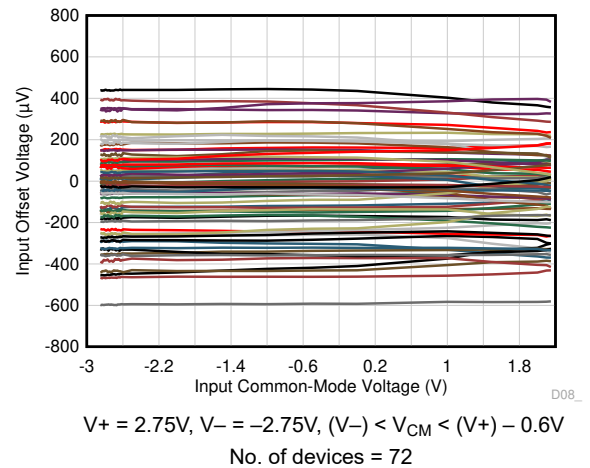


Figure 6-10. Offset Voltage vs Common-Mode

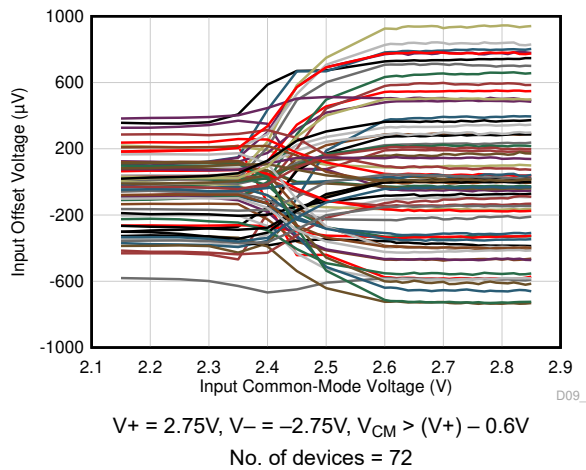


Figure 6-11. Offset Voltage vs Common-Mode

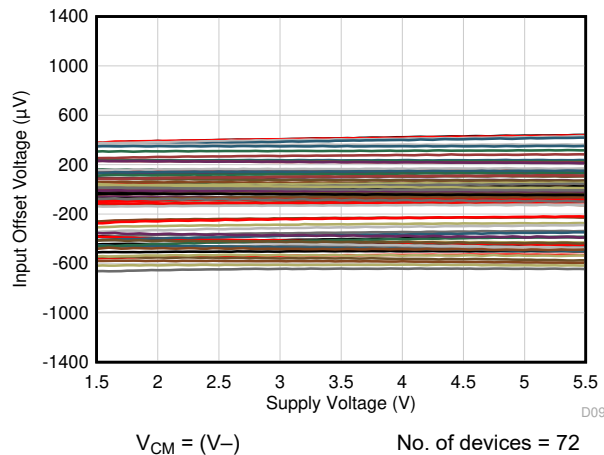


Figure 6-12. Offset Voltage vs Supply Voltage

6.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_+ = 2.75\text{V}$, $V_- = -2.75\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

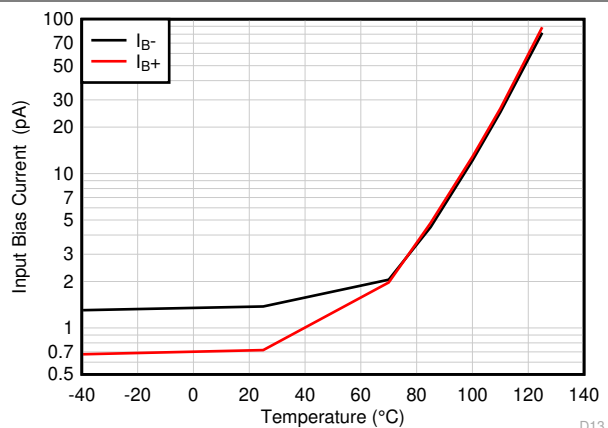


Figure 6-13. I_B vs Temperature

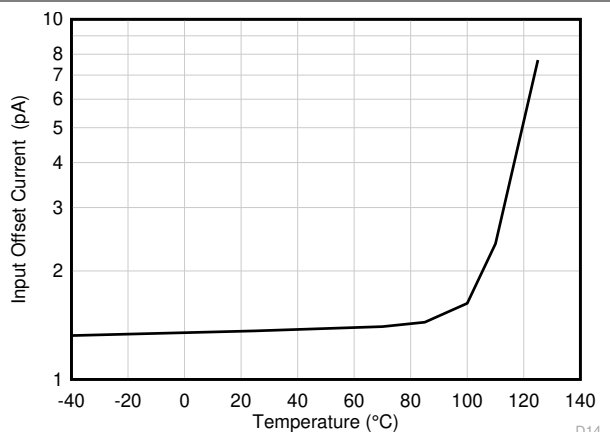


Figure 6-14. I_{OS} vs Temperature

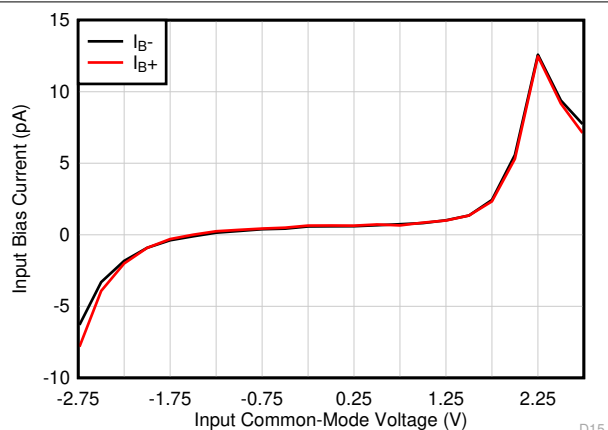


Figure 6-15. I_B vs Common-Mode Voltage

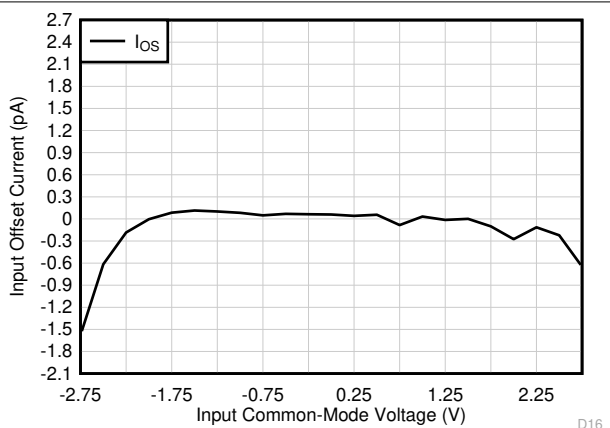


Figure 6-16. I_{OS} vs Common-Mode Voltage

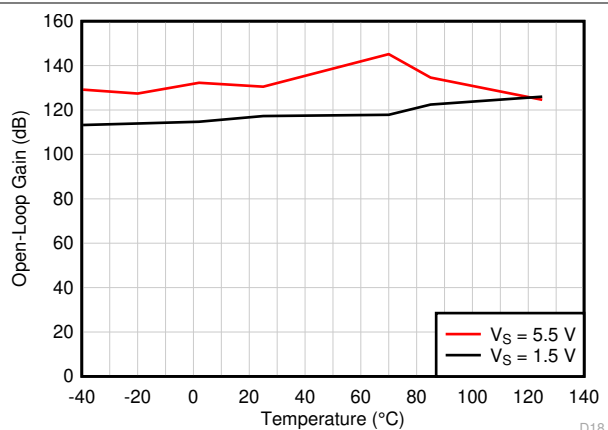


Figure 6-17. Open-Loop Gain vs Temperature

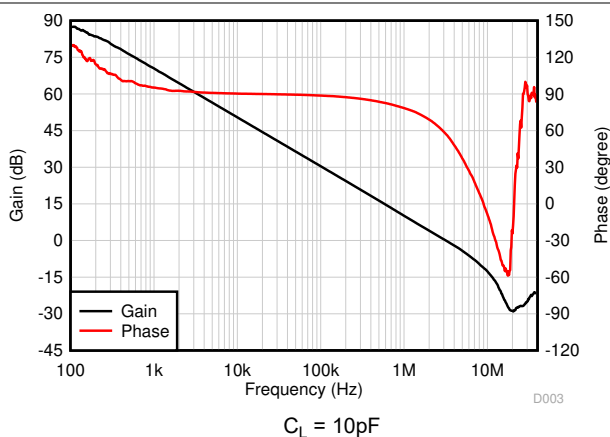


Figure 6-18. Open-Loop Gain and Phase vs Frequency

6.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_+ = 2.75\text{V}$, $V_- = -2.75\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

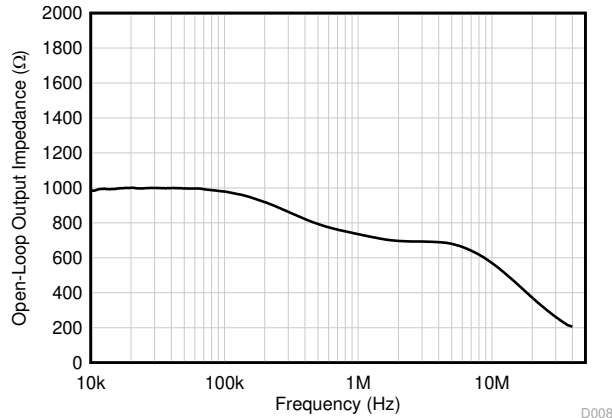


Figure 6-19. Open-Loop Output Impedance vs Frequency

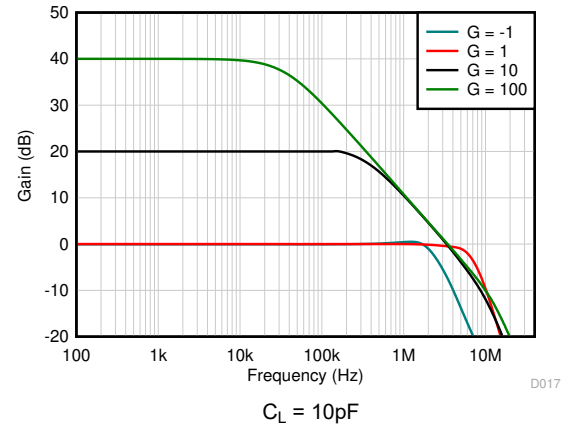
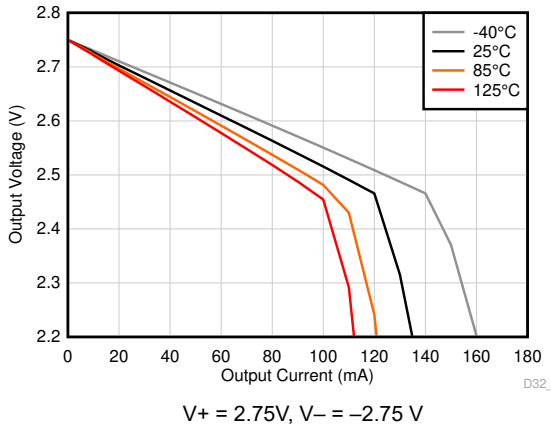
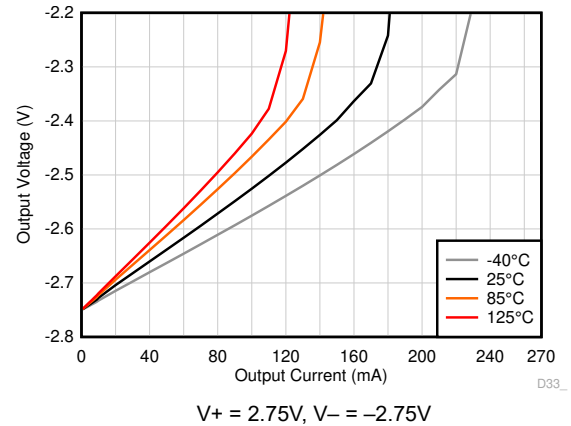


Figure 6-20. Closed-Loop Gain vs Frequency



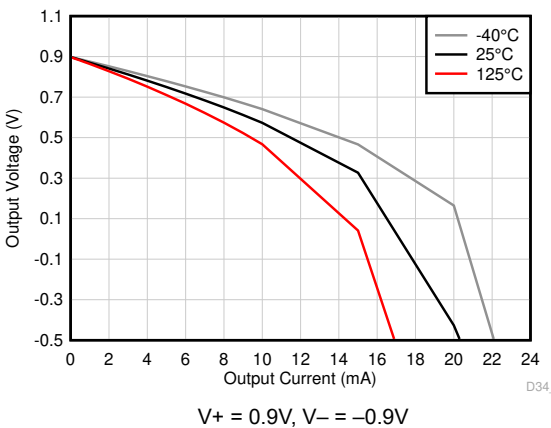
$V_+ = 2.75\text{V}$, $V_- = -2.75\text{V}$

Figure 6-21. Output Voltage Swing vs Output Current (Sourcing)



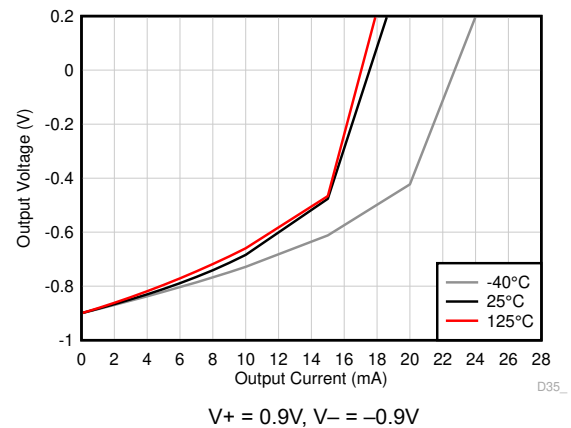
$V_+ = 2.75\text{V}$, $V_- = -2.75\text{V}$

Figure 6-22. Output Voltage Swing vs Output Current (Sinking)



$V_+ = 0.9\text{V}$, $V_- = -0.9\text{V}$

Figure 6-23. Output Voltage Swing vs Output Current (Sourcing)



$V_+ = 0.9\text{V}$, $V_- = -0.9\text{V}$

Figure 6-24. Output Voltage Swing vs Output Current (Sinking)

6.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_+ = 2.75\text{V}$, $V_- = -2.75\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

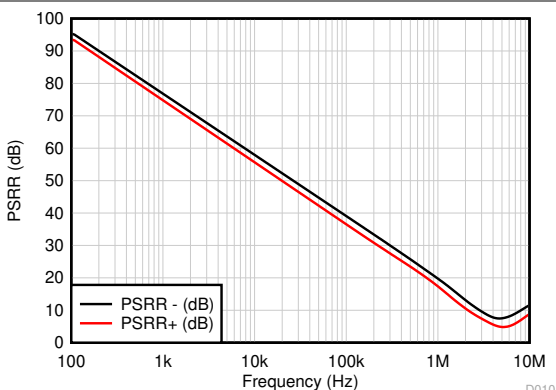
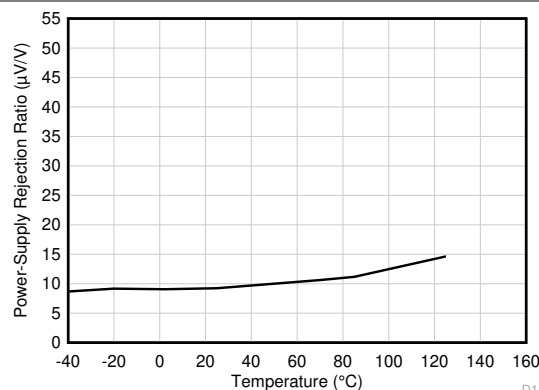


Figure 6-25. PSRR vs Frequency



$V_S = 1.5\text{V to } 5.5\text{V}$

Figure 6-26. DC PSRR vs Temperature

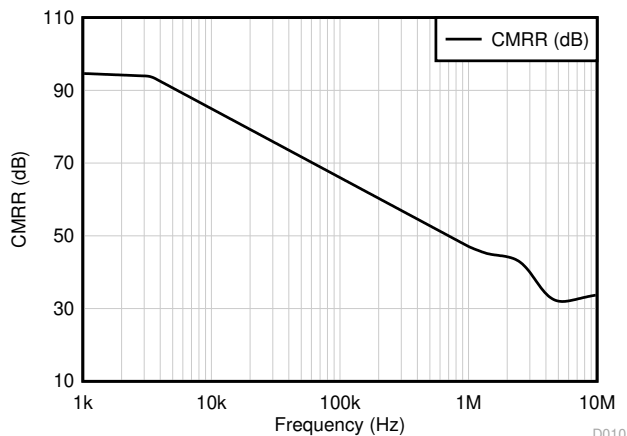
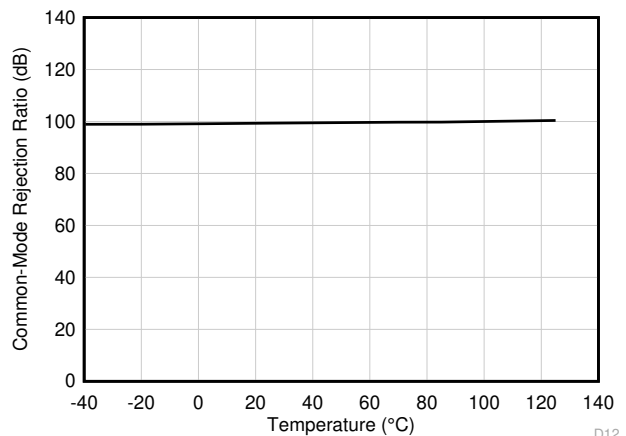


Figure 6-27. CMRR vs Frequency



$V_S = 5.5\text{V}$, $(V_-) < V_{CM} < (V_+) - 0.6\text{V}$

Figure 6-28. DC CMRR vs Temperature

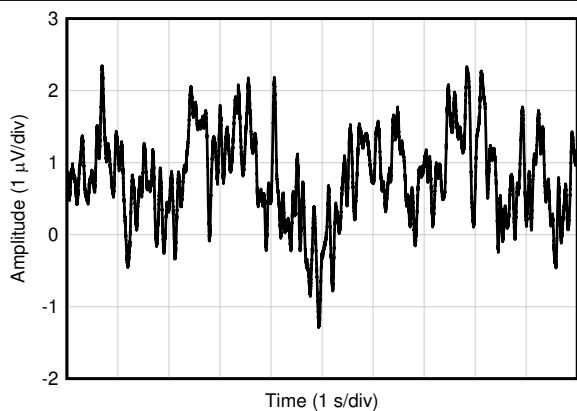


Figure 6-29. 0.1Hz to 10Hz Voltage Noise in Time Domain

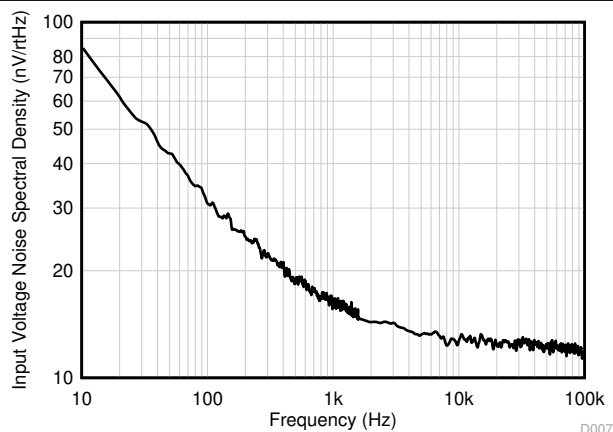


Figure 6-30. Input Voltage Noise Spectral Density

6.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_+ = 2.75\text{V}$, $V_- = -2.75\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

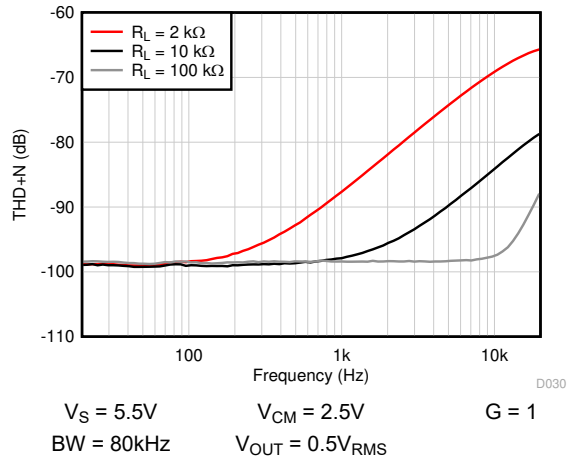


Figure 6-31. THD + N vs Frequency

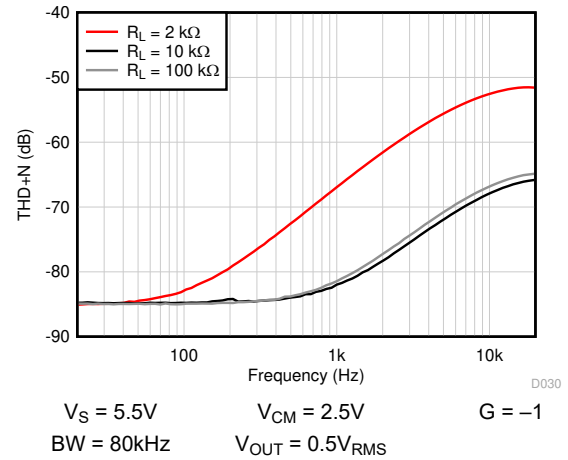


Figure 6-32. THD + N vs Frequency

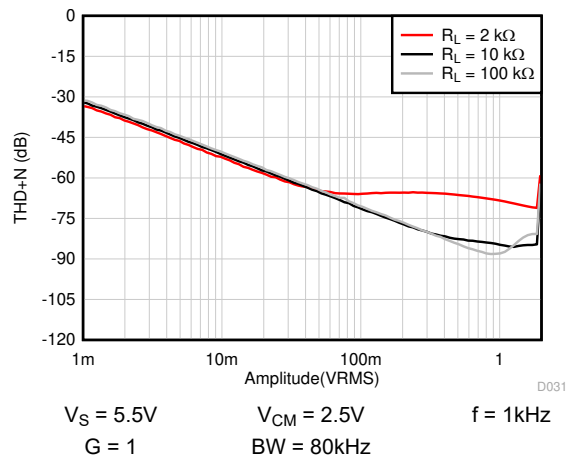


Figure 6-33. THD + N vs Amplitude

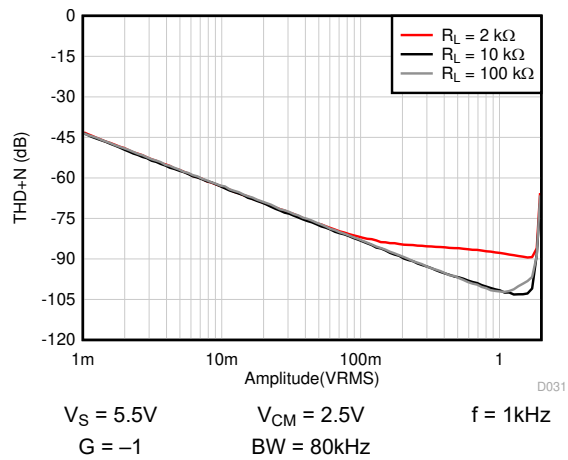


Figure 6-34. THD + N vs Amplitude

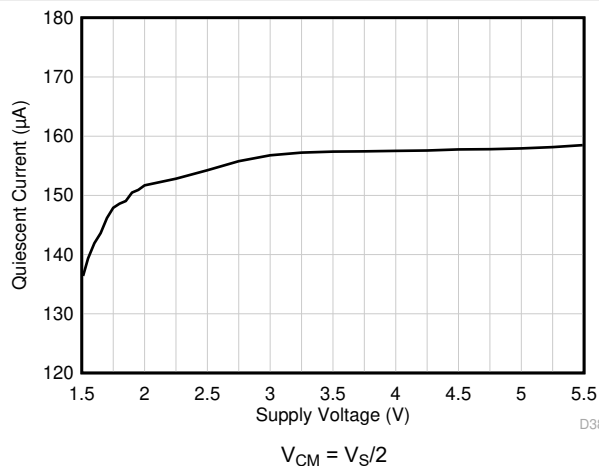


Figure 6-35. Quiescent Current vs Supply Voltage

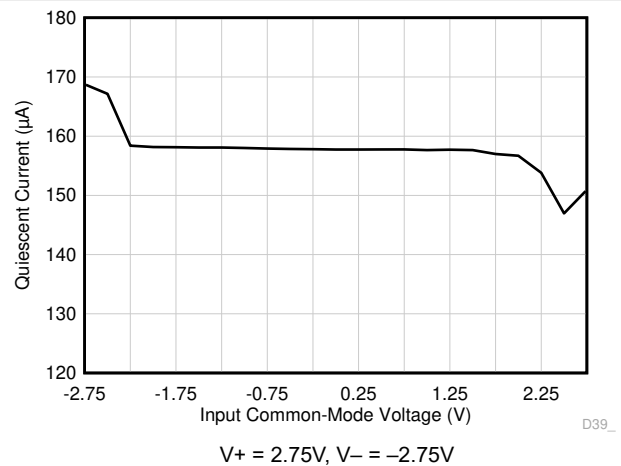


Figure 6-36. Quiescent Current vs Common-Mode Voltage

6.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_+ = 2.75\text{V}$, $V_- = -2.75\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

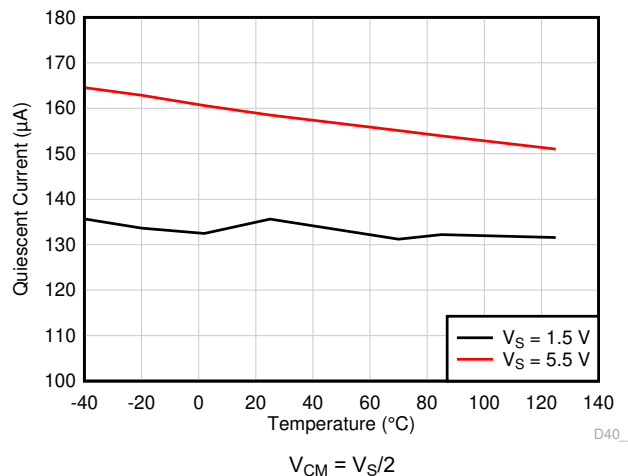


Figure 6-37. Quiescent Current vs Temperature

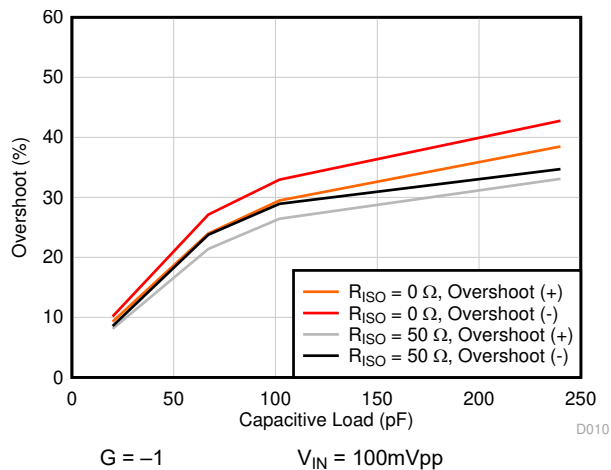


Figure 6-38. Small Signal Overshoot vs Capacitive Load

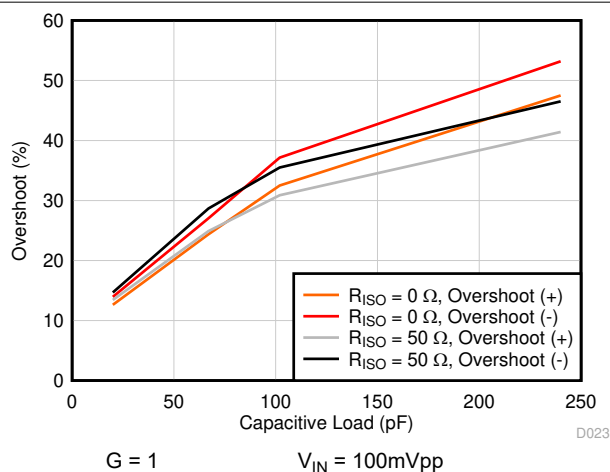


Figure 6-39. Small Signal Overshoot vs Capacitive Load

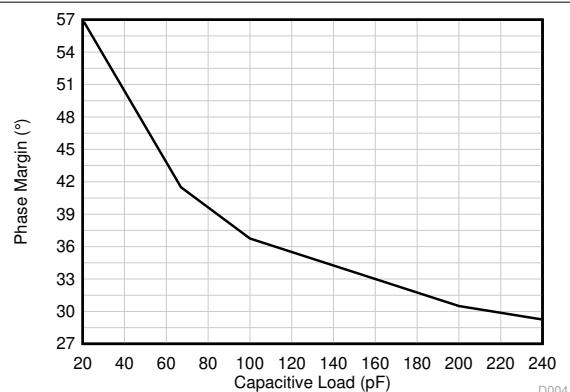


Figure 6-40. Phase Margin vs Capacitive Load

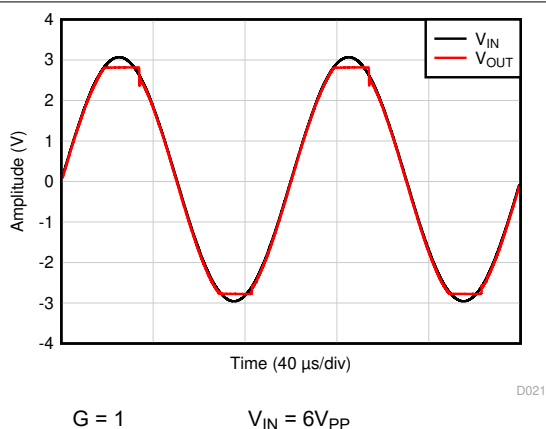


Figure 6-41. No Phase Reversal

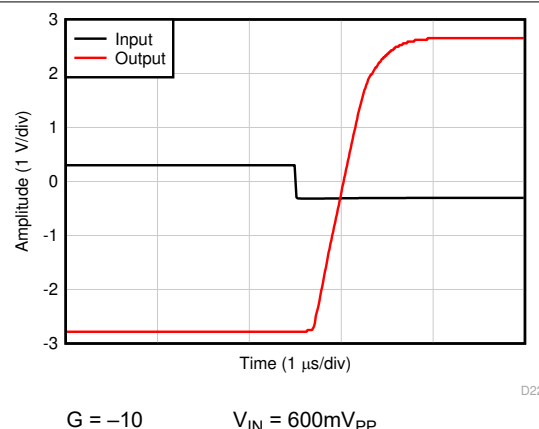
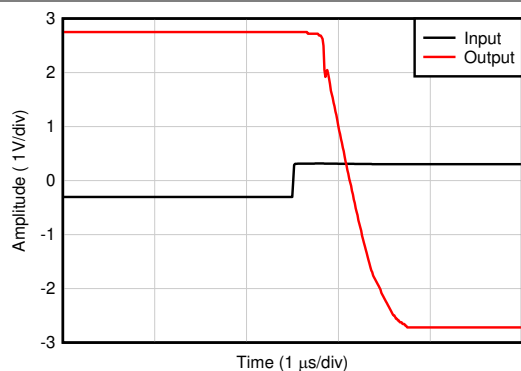


Figure 6-42. Overload Recovery

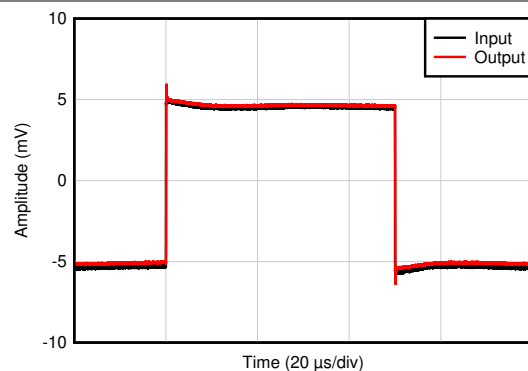
6.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_+ = 2.75\text{V}$, $V_- = -2.75\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)



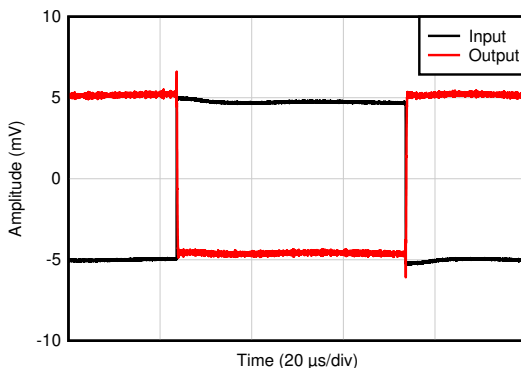
$G = -10$ $V_{IN} = 600\text{mV}_{PP}$

Figure 6-43. Overload Recovery



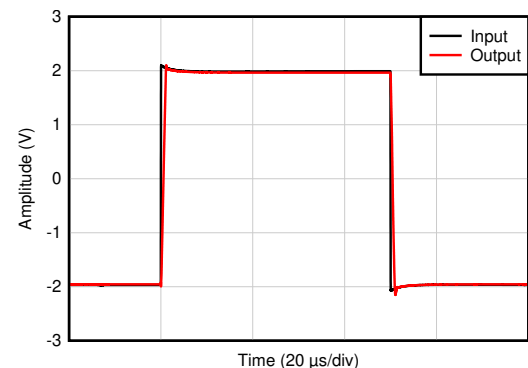
$G = 1$ $V_{IN} = 10\text{mV}_{PP}$ $C_L = 10\text{pF}$

Figure 6-44. Small-Signal Step Response



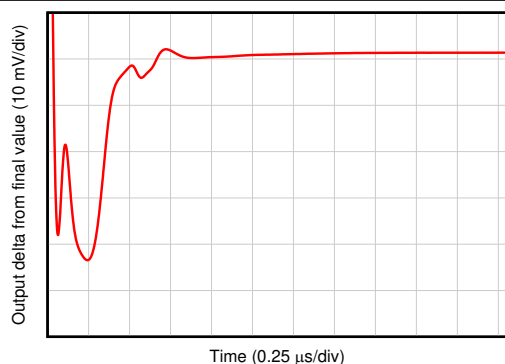
$G = -1$ $V_{IN} = 10\text{mV}_{PP}$ $C_L = 10\text{pF}$

Figure 6-45. Small-Signal Step Response



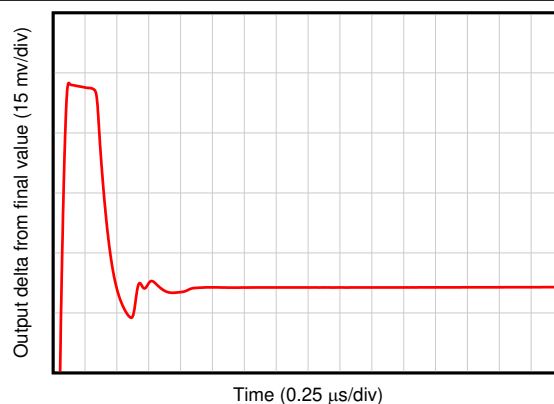
$G = 1$ $V_{IN} = 4\text{V}_{PP}$ $C_L = 10\text{pF}$

Figure 6-46. Large-Signal Step Response



$G = 1$ $V_{IN} = 4\text{V}_{PP}$ $C_L = 10\text{pF}$

Figure 6-47. Large-Signal Settling Time (Negative)

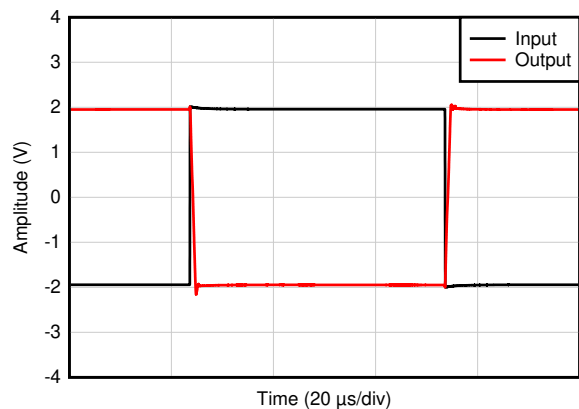


$G = 1$ $V_{IN} = 4\text{V}_{PP}$ $C_L = 10\text{pF}$

Figure 6-48. Large-Signal Settling Time (Positive)

6.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_+ = 2.75\text{V}$, $V_- = -2.75\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)



$$G = -1$$

$$V_{IN} = 4V_{PP}$$

$$C_L = 10\text{pF}$$

Figure 6-49. Large-Signal Step Response

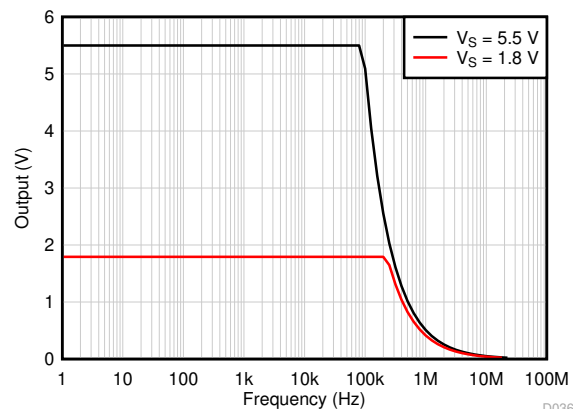
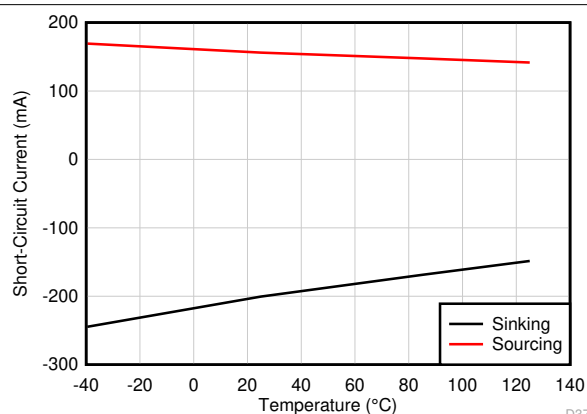


Figure 6-50. Maximum Output Voltage vs Frequency



$$V_S = 5.5\text{V}$$

Figure 6-51. Short-Circuit Current vs Temperature

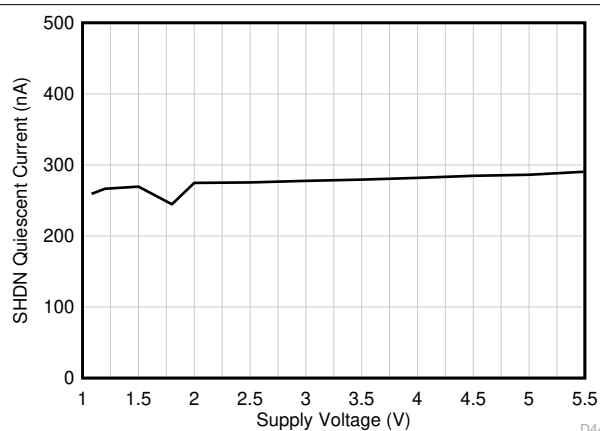


Figure 6-52. Shutdown Mode Quiescent Current vs Supply Voltage

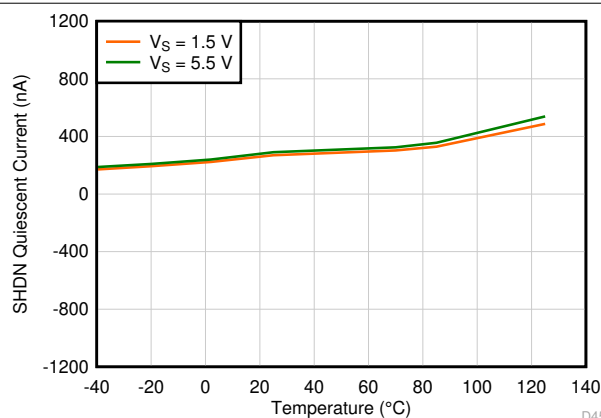
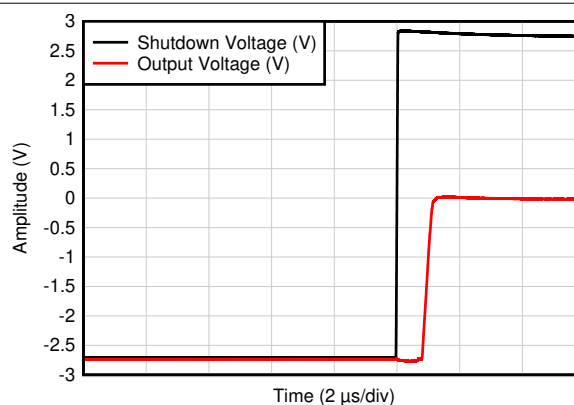


Figure 6-53. Shutdown Mode Quiescent Current vs Temperature

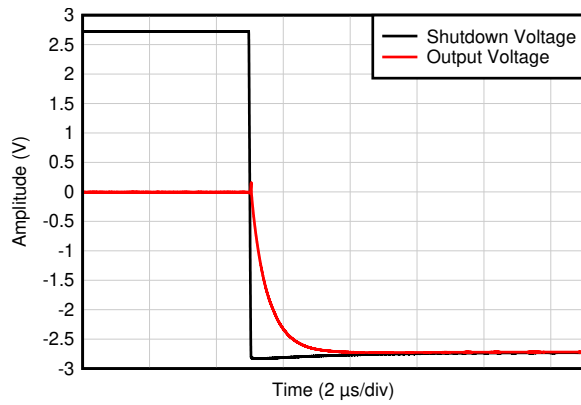


$$V_+ = 2.75\text{V}, V_- = -2.75\text{V}$$

Figure 6-54. Amplifier Enable Response

6.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_+ = 2.75\text{V}$, $V_- = -2.75\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)



$V_+ = 2.75\text{V}$, $V_- = -2.75\text{V}$

Figure 6-55. Amplifier Disable Response

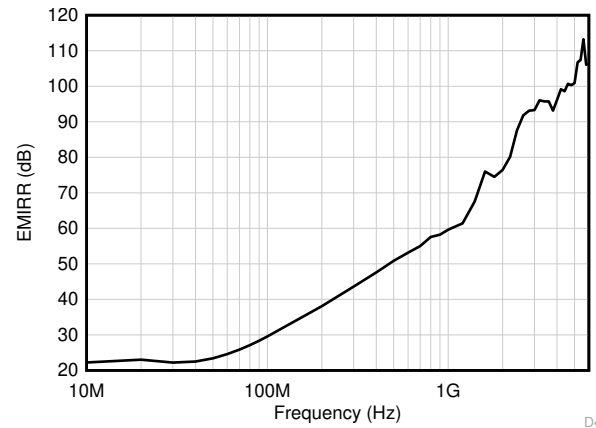


Figure 6-56. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency

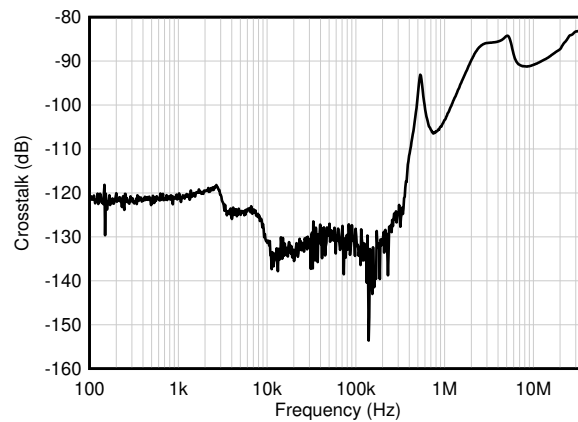


Figure 6-57. Channel Separation

7 Detailed Description

7.1 Overview

The OPAx310 family of op amps includes single (OPA310), dual (OPA2310), and quad-channel (OPA4310), ultra-low-voltage (1.5V to 5.5V), high output current operational amplifiers (op amps) with rail-to-rail input and output swing capabilities. The OPAx310 also features a very fast shutdown response and has an enable time specification of just 0.9 μ s typical. This feature allows for power savings when the application involves duty cycling the amplifier signal chain. OPAx310 has robust ESD performance with fail safe input ESD structure where there are no diodes connected from inputs to the positive power supply rail.

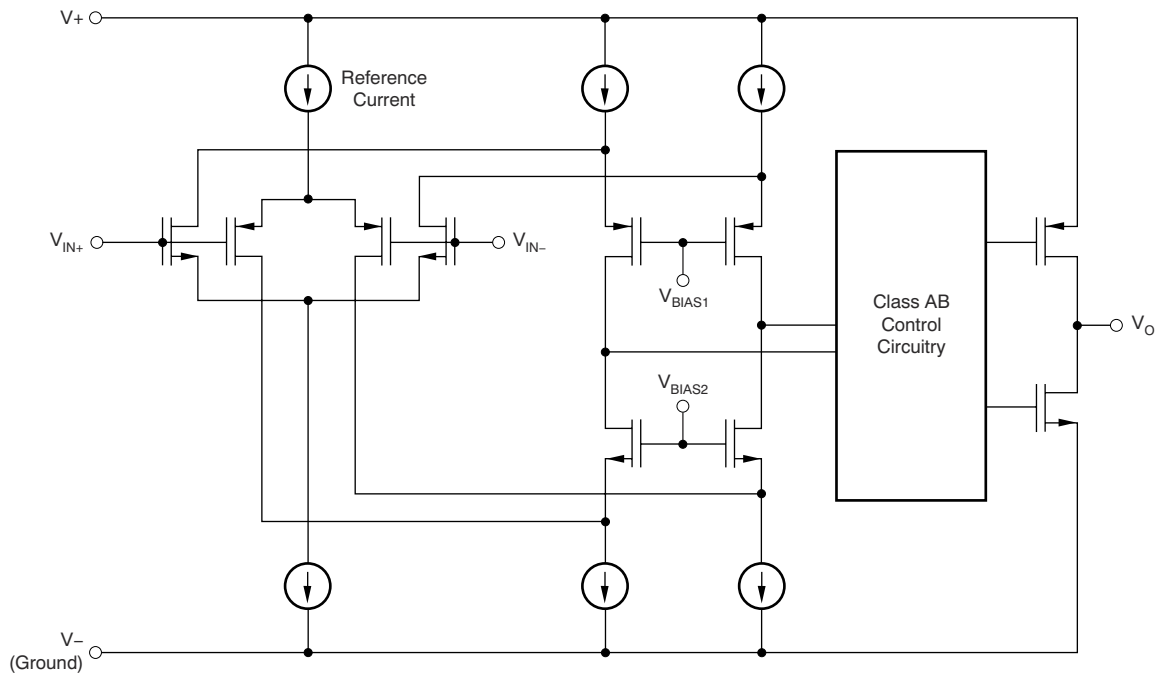
OPAx310 is offered in power pad, standard, small size packages and has an internal current limit, thermal shutdown protection that enables additional robustness when operating with high output current. OPAx310 can swing very close to the rails and has a short circuit current of ± 75 mA minimum across temperature at 5.5V power supply while consuming just 165 μ A of quiescent current. This combination of low voltage, low I_Q , and high output current capability makes this device quite unique and an excellent choice for a wide range of general-purpose and high current applications. Additional output current capability can be easily achieved by connecting multiple op amps in parallel. These devices are excellent choice for LED driver, LCD driver, Laser driver, TEC driver applications and can also be used as a reference buffer, guard amplifier or as a discrete LDO.

The input common-mode voltage range includes both rails, and allows the OPAx310 series to be used in many single-supply or dual supply configurations. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes these devices an excellent choice for driving low speed sampling analog-to-digital converters (ADCs). Further, the class AB output stage is capable of driving smaller resistive loads connected to any point between V+ and ground.

The OPAx310 can drive up to 75pF with a typical phase margin of 40° and features 3MHz gain bandwidth product, 3V/ μ s slew rate with 4 μ V_{p-p} integrated noise (0.1Hz to 10Hz) while consuming only 165 μ A supply current per channel, thus providing a good AC performance at a very low power consumption. DC applications are also well served with a low input bias current (1pA typical), a good input offset voltage (0.25mV typical) and a good PSRR (10 μ V/V typical), CMRR (80dB typical), and A_{OL} (125dB typical).

The robust design of the OPAx310 family simplifies circuit design. These op amps feature an integrated radio frequency immunity (RFI) and electro-magnetic interference (EMI) rejection filter, unity-gain stability, and no-phase reversal in input overdrive conditions.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Voltage

The OPAX310 series of operational amplifiers is fully specified from 1.8V to 5.5V and is tested for amplifier operation from 1.5V to 1.8V. In addition, many specifications apply from -40°C to 125°C . Parameters that vary significantly with operating voltages or temperature are provided in the [Typical Characteristics](#). TI highly recommends to bypass power-supply pins with at least $0.01\mu\text{F}$ ceramic capacitors.

7.3.2 Rail-to-Rail Input

The input common-mode voltage range of the OPAX310 series extends to either supply rails. This is true even when operating at the ultra-low supply voltage of 1.5V, all the way up to the standard supply voltage of 5.5V. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair. Refer to the [Functional Block Diagram](#) for more details.

For most amplifiers with a complementary input stage, one of the input pairs, usually the P-channel input pair, is designed to deliver slightly better performance in terms of input offset voltage, offset drift over the N-channel pair. Consequently, the P-channel pair is designed to cover the majority of the common mode range with the N-channel pair slated to slowly take over at a certain threshold voltage from the positive rail. Just after the threshold voltage, both the input pairs are in operation for a small range referred to as the transition region. Beyond this region, the N-channel pair completely takes over. Within the transition region, PSRR, CMRR, offset voltage, offset drift, and THD can be degraded compared to device operation outside this region. Hence, most applications generally prefer operating in the P-channel input range where the performance is slightly better.

For the OPAX310, the P-channel pair is typically active for input voltages from (V_-) to $(V_+) - 0.4\text{V}$ and the N-channel pair is typically active for input voltages from the positive supply to $(V_+) - 0.4\text{V}$. The transition region occurs typically from $(V_+) - 0.5\text{V}$ to $(V_+) - 0.3\text{V}$, in which both pairs are on. These voltage levels mentioned above can vary with process variations associated with threshold voltage of transistors. In the OPAX310, 200mV transition region mentioned above can vary up to 200mV in either direction. Thus, the transition region (both stages on) can range from $(V_+) - 0.7\text{V}$ to $(V_+) - 0.5\text{V}$ on the low end, up to $(V_+) - 0.3\text{V}$ to $(V_+) - 0.1\text{V}$ on the high end.

Recollecting the fact that a P-channel input pair usually offers better performance over a N-channel input pair, the OPAX310 is designed to offer a much wider P-channel input pair range, in comparison to most complimentary input amplifiers in the industry. A side-by-side comparison of the OPAX310 and the TLV900x is provided below. Note that the TLV900x is designed for P-channel pair operation only until 1.4V from the positive rail, while the OPAX310 is designed for P-channel pair operation until 0.7V from the positive rail. This additional 700mV of P-channel input pair range for the OPAX310 is particularly useful when operating at lower supply voltages (1.5V, 1.8V, and so forth) where the P-channel input range usually gets limited to a great extent.

Thus the wide common mode swing of input signal can be accommodated more easily within the P-channel input pair of the OPAX310, while likely avoiding the transition region, thereby maintaining linearity.

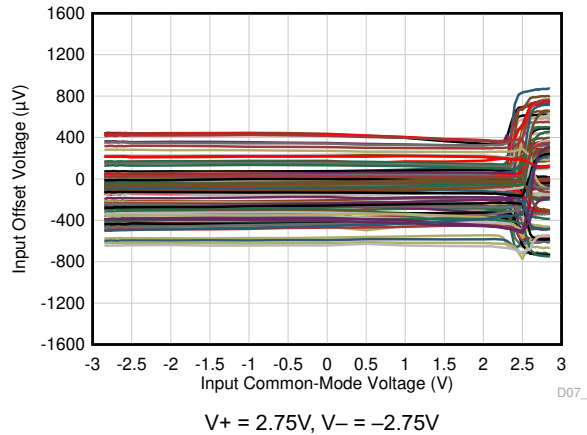


Figure 7-1. OPAx310 Offset Voltage vs Common-Mode

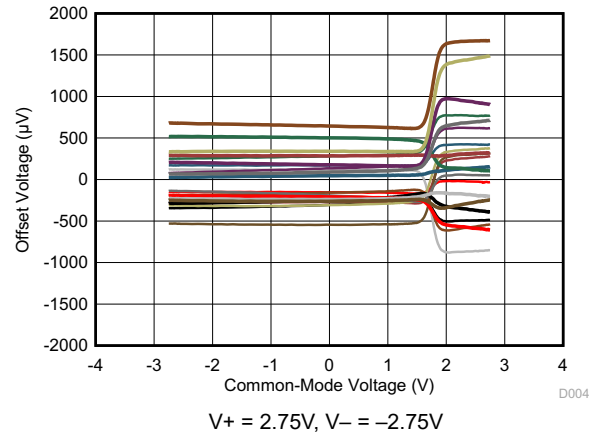


Figure 7-2. TLV900x Offset Voltage vs Common-Mode

7.3.3 Rail-to-Rail Output

Designed as a micro-power, high output current operational amplifier, the OPAx310 delivers a robust output drive capability. A class AB output stage with common-source transistors is used to achieve full rail-to-rail output swing capability. At room temperature and for resistive loads up to 2k Ω , the output swings to within a maximum of 20mV of either supply rail at 5.5V power supply. Different load conditions change the ability of the amplifier to swing close to the rails.

7.3.4 Capacitive Load and Stability

The OPAx310 is designed to be used in applications where driving a capacitive load is required. As with all operational amplifiers, there can be specific instances where the OPAx310 can become unstable. The particular operational amplifier circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether or not an amplifier is stable in operation. An operational amplifier in the unity-gain (1 V/V) buffer configuration that drives a capacitive load exhibits a greater tendency to be unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the operational amplifier output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases when capacitive loading increases. When operating in the unity-gain configuration, the OPAx310 remains stable with a pure capacitive load up to approximately 75pF with a good phase margin of 40° typical and has no sustained oscillations up to 250pF. The equivalent series resistance (ESR) of some very large capacitors (C_L greater than 1 μ F) is sufficient to alter the phase characteristics in the feedback loop such that the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when measuring the overshoot response of the amplifier at higher voltage gains.

One technique for increasing the capacitive load drive capability of the amplifier operating in a unity-gain configuration is to insert a small resistor (typically 10 Ω to 20 Ω) in series with the output, as shown in [Figure 7-3](#). This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. One possible problem with this technique, however, is that a voltage divider is created with the added series resistor and any resistor connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that reduces the output swing.

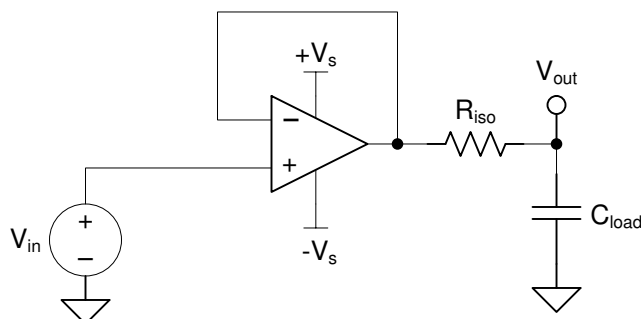


Figure 7-3. Improving Capacitive Load Drive

7.3.5 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, because of the high input voltage or high gain. After one of the output devices enters the saturation region, the output stage requires additional time to return to the linear operating state which is referred to as overload recovery time. After the output stage returns to linear operating state, the amplifier begins to slew at the specified slew rate. Therefore, the propagation delay (in case of an overload condition) is the sum of the overload recovery time and the slew time.

The overload recovery time for the OPAx310 family is approximately 0.75μs typical.

7.3.6 EMI Rejection

The OPAx310 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications (radio frequency interference - RFI) and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAx310 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10MHz to 6GHz. [Figure 7-4](#) shows the results of this testing on the OPAx310. [Table 7-1](#) shows the EMIRR IN+ values for the OPAx310 at particular frequencies commonly encountered in real-world applications. The [EMI Rejection Ratio of Operational Amplifiers application report](#) contains detailed information on the topic of EMIRR performance relating to op amps and is available for download from www.ti.com.

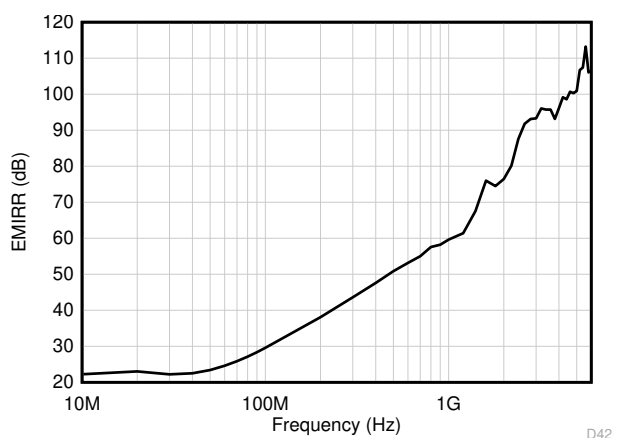


Figure 7-4. EMIRR Testing

Table 7-1. OPAx310 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	48dB
900MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6GHz), GSM, aeronautical mobile, UHF applications	58dB
1.8GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1GHz to 2GHz)	75dB
2.4GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2GHz to 4GHz)	90dB
3.6GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	95dB
5GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4GHz to 8GHz)	102dB

7.3.7 ESD and Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and relevance to an electrical overstress event is helpful. Figure 7-5 shows the ESD circuits contained in the OPAx310 devices. The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power supply lines, where the input and output pins meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

Note that the OPAx310 features no current-steering diodes connected between the input and positive power-supply pin.

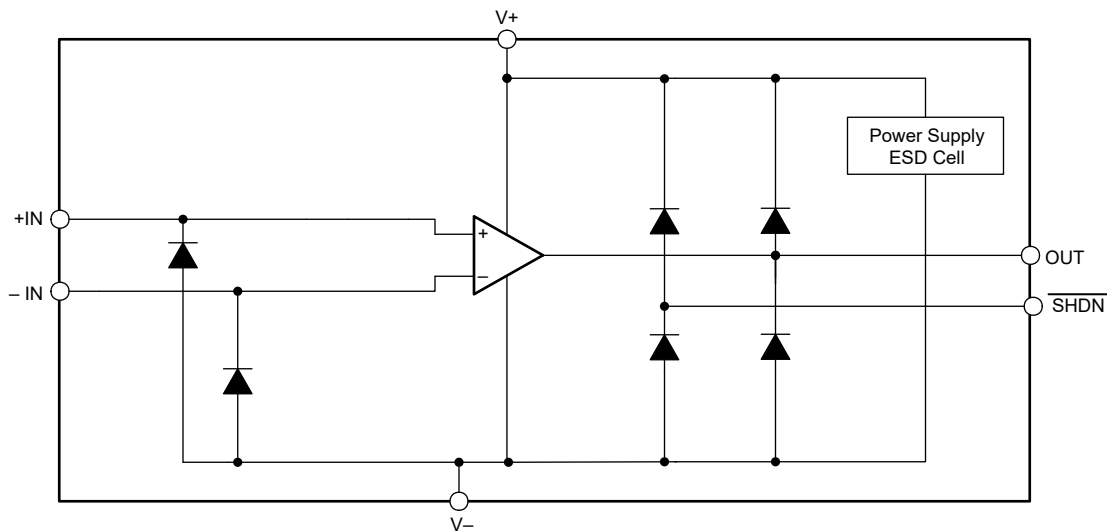


Figure 7-5. Equivalent Internal ESD Circuitry

7.3.8 Input ESD Protection

The OPAx310 family incorporates internal ESD protection circuits on all pins. For inputs, this protection primarily consists of fail safe ESD input structures which feature no current-steering diodes connected between the input and positive power-supply pin as shown in the [Figure 7-5](#). This feature is very useful during power sequencing scenarios where input signal can be present before the positive power supply rail. A fail safe input ESD structure prevents any short between inputs and positive power supply.

7.3.9 Shutdown Function

The OPAx310 S devices feature $\overline{\text{SHDN}}$ pins that disable the op amp, placing the op amp into a low-power standby mode. In this mode, the op amp typically consumes less than 500nA at room temperature. The $\overline{\text{SHDN}}$ pins are active low, meaning that shutdown mode is enabled when the input to the $\overline{\text{SHDN}}$ pin is a valid logic low.

The $\overline{\text{SHDN}}$ pins are referenced to the negative supply voltage of the op amp. The threshold of the shutdown feature lies around 500mV (typical) and does not change with respect to the supply voltage. Hysteresis has been included in the switching threshold to provide for smooth switching characteristics. To make sure of optimal shutdown behavior, the $\overline{\text{SHDN}}$ pins must be driven with valid logic signals. A valid logic low is defined as a voltage between V_- and $(V_-) + 0.2V$. A valid logic high is defined as a voltage between $(V_-) + 1.2V$ and V_+ . To enable the amplifier, the $\overline{\text{SHDN}}$ pins must be driven to a valid logic high. To disable the amplifier, the $\overline{\text{SHDN}}$ pins must be driven to a valid logic low. TI highly recommends that the shutdown pin be connected to a valid high or a low voltage or driven. The maximum voltage allowed at the $\overline{\text{SHDN}}$ pins is $(V_+) + 0.5V$. Exceeding this voltage level damages the device.

The $\overline{\text{SHDN}}$ pins are high-impedance CMOS inputs. Dual op amp versions are independently controlled and quad op amp versions are controlled in pairs with logic inputs. For battery-operated applications, this feature can be used to greatly reduce the average current and extend battery life. The enable and disable time is targeted to be under 1 μ s for full shutdown of all channels. When disabled, the output assumes a high-impedance state. This architecture allows the OPAx310S to be operated as a gated amplifier (or to have the device output multiplexed onto a common analog output bus). Shutdown time (t_{OFF}) depends on loading conditions and increases as load resistance increases. To make sure that shutdown (disable) is within a specific shutdown time, the specified 10-k Ω load to midsupply ($V_S / 2$) is required.

7.3.10 Packages with an Exposed Thermal Pad

The OPAx310 family is available in packages such as the WQFN-16 (RTE), which feature an exposed thermal pad. Inside the package, the die is attached to this thermal pad using an electrically conductive compound. For this reason, when using a package with an exposed thermal pad, the thermal pad must be connected to (V_-) . Attaching the thermal pad to a potential other than (V_-) is not allowed, and the performance of the device may not be consistent with the [Electrical Characteristics](#) table when doing so.

7.4 Device Functional Modes

The OPAx310 devices have one functional mode. These devices are powered on as long as the power-supply voltage is between 1.5V ($\pm 0.75V$) and 5.5V ($\pm 2.75V$).

The OPAx310S devices feature a shutdown pin, which can be used to place the op amp into a low-power mode. See [Shutdown Function](#) for more information.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The OPAx310 family of rail-to-rail input and output operational amplifiers is specifically designed for high output current applications. The devices operate from 1.5V to 5.5V, are unity-gain stable, and are also an excellent choice for a wide range of general-purpose applications. The class AB output stage is capable of driving small resistive loads connected to any point between V+ and V– as long as the device is not forced into short circuit mode or thermal shutdown mode. The input common-mode voltage range includes both rails and allows the OPAx310 series to be used in many single-supply or dual supply configurations.

8.2 Typical Application

8.2.1 OPAx310 Low-Side, Current Sensing Application

Figure 8-1 shows the OPAx310 configured in a low-side current sensing application.

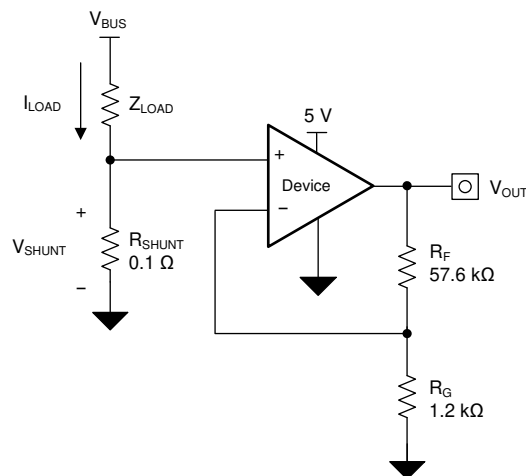


Figure 8-1. OPAx310 in a Low-Side, Current-Sensing Application

8.2.1.1 Design Requirements

The design requirements for this design are:

- Load current: 0A to 1A
- Maximum output voltage: 4.9V
- Maximum shunt voltage: 100mV

8.2.1.2 Detailed Design Procedure

The transfer function of the circuit in [Figure 8-1](#) is given in [Equation 1](#).

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times \text{Gain} \quad (1)$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0A to 1A. To keep the shunt voltage below 100mV at maximum load current, the largest shunt resistor is shown using [Equation 2](#).

$$R_{SHUNT} = \frac{V_{SHUNT_MAX}}{I_{LOAD_MAX}} = \frac{100 \text{ mV}}{1 \text{ A}} = 100 \text{ m}\Omega \quad (2)$$

Using [Equation 2](#), R_{SHUNT} is calculated to be 100m Ω . The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the OPAx310 to produce an output voltage of approximately 0V to 4.9V. The gain needed by the OPAx310 to produce the necessary output voltage is calculated using [Equation 3](#).

$$\text{Gain} = \frac{V_{OUT_MAX} - V_{OUT_MIN}}{V_{IN_MAX} - V_{IN_MIN}} \quad (3)$$

Using [Equation 3](#), the required gain is calculated to be 49V/V, which is set with resistors R_F and R_G . [Equation 4](#) sizes the resistors R_F and R_G , to set the gain of the OPAx310 to 49V/V.

$$\text{Gain} = 1 + \frac{R_F}{R_G} \quad (4)$$

Selecting R_F as 57.6 k Ω and R_G as 1.2 k Ω provides a combination that equals 49V/V. [Figure 8-2](#) shows the measured transfer function of the circuit shown in [Figure 8-1](#). Notice that the gain is only a function of the feedback and gain resistors. This gain is adjusted by varying the ratio of the resistors and the actual resistors values are determined by the impedance levels that the designer wants to establish. The impedance level determines the current drain, the effect that stray capacitance has, and a few other behaviors. There is no optimal impedance selection that works for every system; choose an impedance that is best for the system parameters.

8.2.1.3 Application Curve

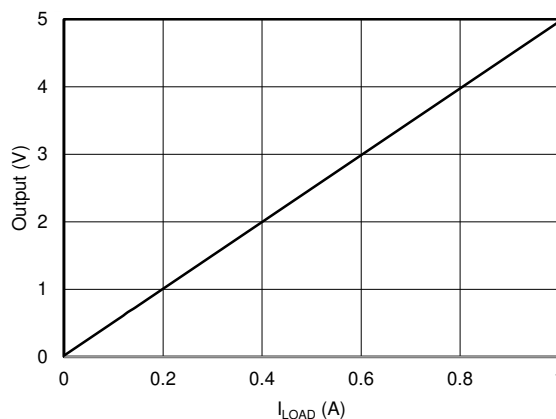


Figure 8-2. Low-Side, Current-Sense Transfer Function

8.3 Power Supply Recommendations

The OPAx310 family is specified for operation from 1.5V to 5.5V ($\pm 0.75\text{V}$ to $\pm 2.75\text{V}$); many specifications apply from -40°C to 125°C . [Electrical Characteristics](#) presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 7V can permanently damage the device; see the [Absolute Maximum Ratings](#) table.

Place 0.1 μF bypass capacitors close to the power-supply pins to reduce coupling errors from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see [Layout Guidelines](#).

8.4 Layout

8.4.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power connections of the board and propagate to the power pins of the op amp itself. Bypass capacitors are used to reduce the coupled noise by providing a low-impedance path to ground.
 - Connect low-ESR, 0.1 μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. One bypass capacitor from V+ to ground is adequate for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace at a 90 degree angle is much better as opposed to running the traces in parallel with the noisy trace.
- Place the external components as close to the device as possible, as shown in [Layout Example](#). Keeping R_1 and R_2 close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- TI recommends cleaning the PCB following board assembly for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, TI recommends baking the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

8.4.2 Layout Example

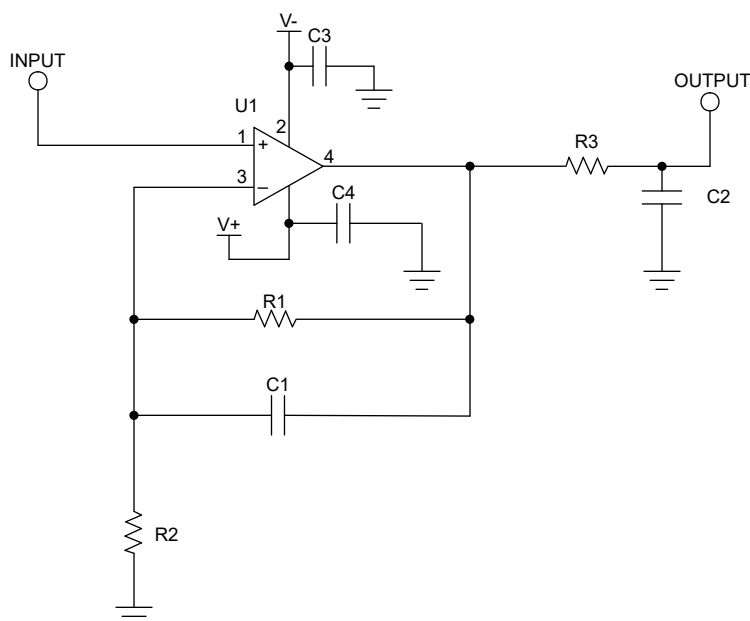


Figure 8-3. Schematic for Noninverting Configuration Layout Example

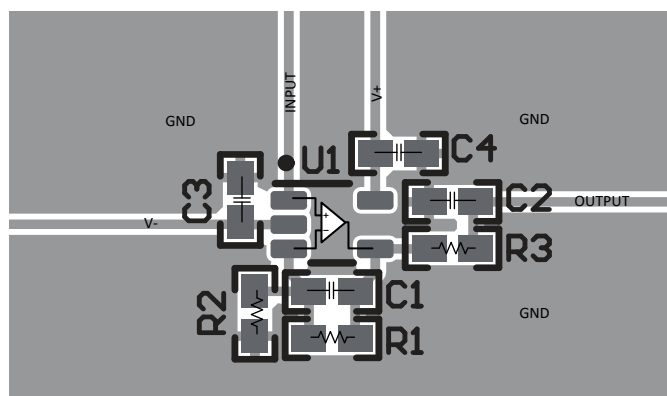


Figure 8-4. Operational Amplifier Board Layout for Noninverting Configuration - SC70 (DCK) Package

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [EMI Rejection Ratio of Operational Amplifiers \(With OPA333 and OPA333-Q1 as an Example\) application report](#)
- Texas Instruments, [QFN/SON PCB Attachment application report](#)
- Texas Instruments, [Quad Flatpack No-Lead Logic Packages application report](#)

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

Trademarks

TI E2E™ is a trademark of Texas Instruments.

Bluetooth® is a registered trademark of Bluetooth SIG, Inc.

All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (January 2024) to Revision H (November 2024)	Page
• Deleted all OPAX310-Q1 mentions in the data sheet.....	1

Changes from Revision F (June 2023) to Revision G (January 2024)	Page
• Updated <i>Power Supply Recommendations</i> to correct 6V to 7V	35

Changes from Revision E (December 2022) to Revision F (June 2023)	Page
• Updated the <i>Device Information</i> table format to include channel count and package leads.....	1

Changes from Revision D (October 2022) to Revision E (December 2022)	Page
• Removed preview tag for the OPA2310S RUG and OPA4310 D, PW packages.....	1
• Removed preview tag for the OPA2310S RTE and OPA4310 D, PW packages.....	3
• Added shutdown quiescent current for OPA2310S in the <i>Specifications</i> section.....	10

Changes from Revision C (September 2022) to Revision D (October 2022)	Page
• Changed OPA310 / OPA310S DBV, DCK packages from "Preview" to "Production".....	1
• Removed preview tag for the OPA310 / OPA310S DBV, DCK packages.....	3
• Changed enable time max limit to 1.6μs in <i>Specifications</i> section.....	10

Changes from Revision B (July 2022) to Revision C (September 2022)	Page
• Updated typical enable time to 0.9μs.....	1
• Removed preview tag for the OPA310 DBV and OPA4310S RTE packages.....	1
• Deleted <i>shutdown section is on preview</i> foot note from the <i>Specifications</i> section.....	10

Changes from Revision A (June 2022) to Revision B (July 2022)	Page
• Changed DGK from "Preview" to "Production".....	1
• Updated <i>Device Comparison</i> section to include information about shutdown.....	3
• Removed preview tag for the DGK package.....	3
• Added <i>shutdown section is on preview</i> foot note to the <i>Specifications</i> section.....	10
• Updated the <i>ESD and Electrical Overstress</i> section to show ESD structures on the shutdown pin.....	31

Changes from Revision * (April 2022) to Revision A (June 2022)	Page
• Changed status from "Advance Information" to "Production Data".....	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2310IDGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	O231
OPA2310IDGKR.A	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	O231
OPA2310IDR	Active	Production	SOIC (D) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2310D
OPA2310IDR.A	Active	Production	SOIC (D) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2310D
OPA2310IDSGR	Active	Production	WSON (DSG) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O23G
OPA2310IDSGR.A	Active	Production	WSON (DSG) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O23G
OPA2310SIRUGR	Active	Production	X2QFN (RUG) 10	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1NZ
OPA2310SIRUGR.A	Active	Production	X2QFN (RUG) 10	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1NZ
OPA310IDBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	O310
OPA310IDBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	O310
OPA310IDCKR	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1NN
OPA310IDCKR.A	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1NN
OPA310SIDBVR	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	O31S
OPA310SIDBVR.A	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	O31S
OPA310SIDCKR	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1NP
OPA310SIDCKR.A	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1NP
OPA4310IDR	Active	Production	SOIC (D) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPA4310D
OPA4310IDR.A	Active	Production	SOIC (D) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPA4310D
OPA4310IPWR	Active	Production	TSSOP (PW) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O4310PW
OPA4310IPWR.A	Active	Production	TSSOP (PW) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O4310PW
OPA4310SIRTER	Active	Production	WQFN (RTE) 16	5000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	O4310S
OPA4310SIRTER.A	Active	Production	WQFN (RTE) 16	5000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	O4310S

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA310 :

- Automotive : [OPA310-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2310IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
OPA2310IDR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2310IDSGR	WSO	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
OPA2310SIRUGR	X2QFN	RUG	10	3000	180.0	8.4	1.75	2.25	0.55	4.0	8.0	Q1
OPA310IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA310IDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
OPA310SIDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA310SIDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA310SIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
OPA4310IDR	SOIC	D	14	3000	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4310IPWR	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4310SIRTER	WQFN	RTE	16	5000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2310IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2310IDR	SOIC	D	8	3000	353.0	353.0	32.0
OPA2310IDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
OPA2310SIRUGR	X2QFN	RUG	10	3000	210.0	185.0	35.0
OPA310IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
OPA310IDCKR	SC70	DCK	5	3000	180.0	180.0	18.0
OPA310SIDBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
OPA310SIDBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
OPA310SIDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
OPA4310IDR	SOIC	D	14	3000	353.0	353.0	32.0
OPA4310IPWR	TSSOP	PW	14	3000	353.0	353.0	32.0
OPA4310SIRTER	WQFN	RTE	16	5000	367.0	367.0	35.0

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

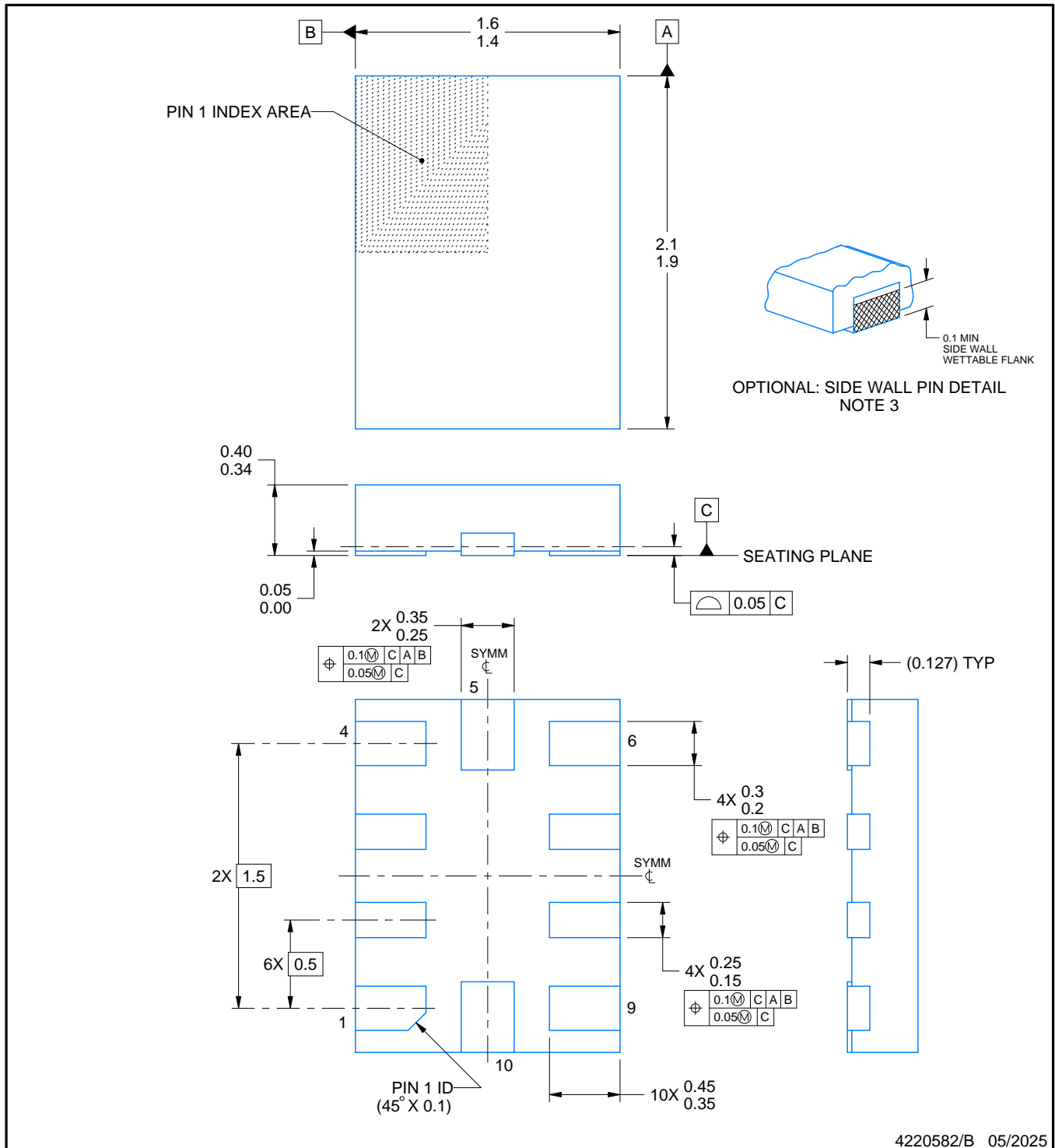
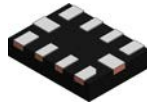


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220582/B 05/2025

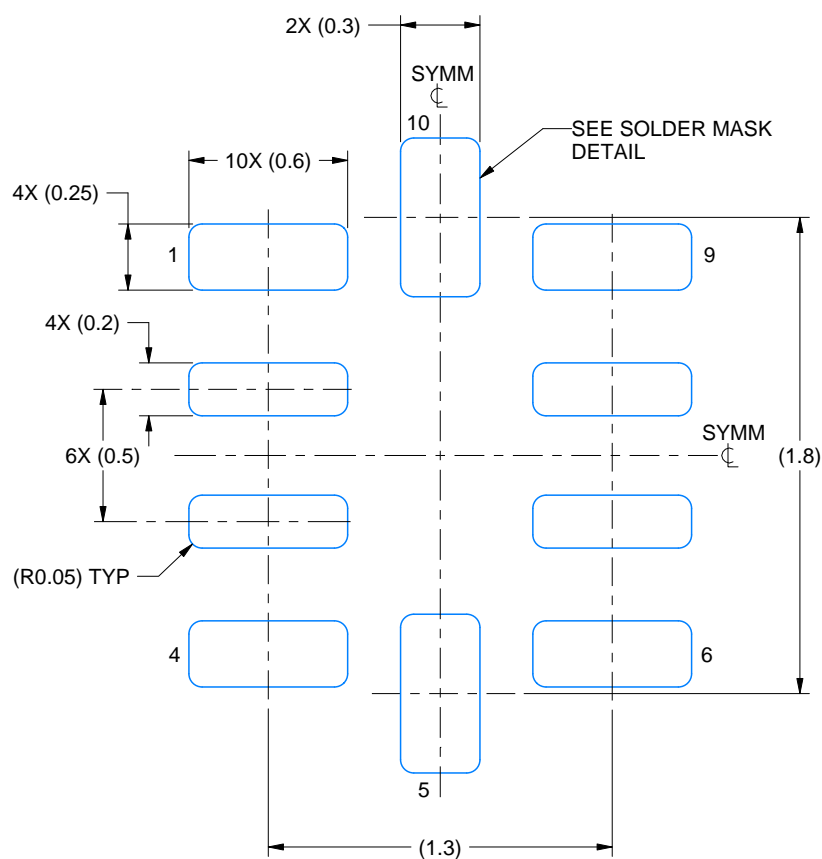
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.

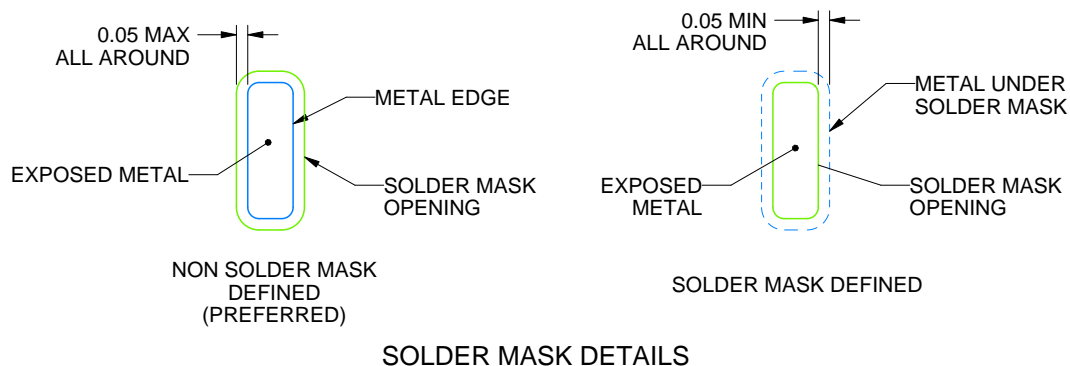
RUG0010B

X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 35X



4220582/B 05/2025

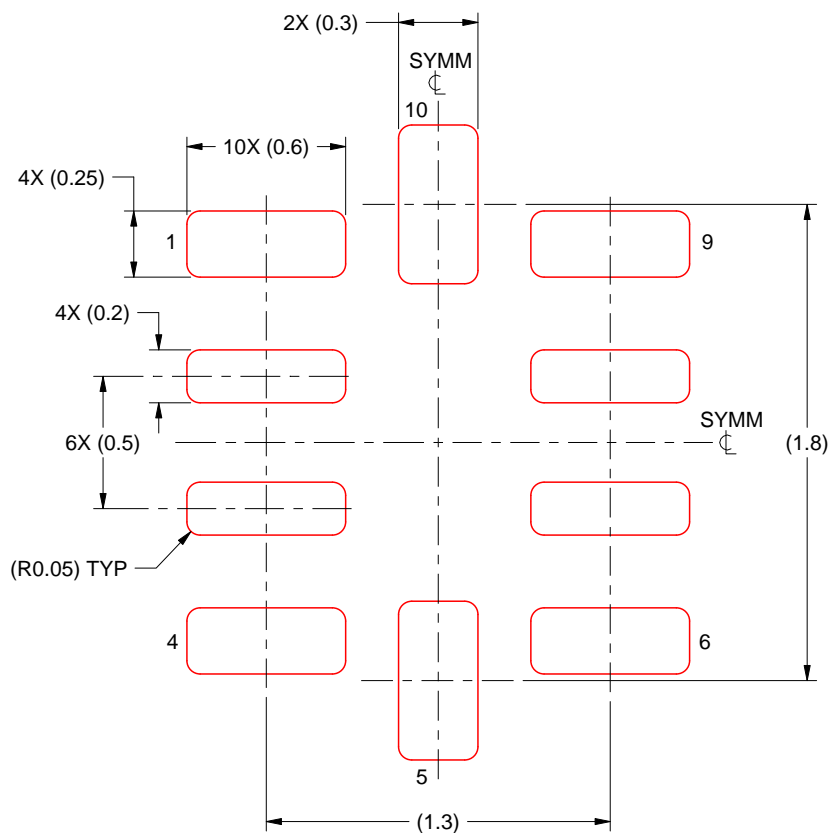
NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sl原因271).

RUG0010B

X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 35X

4220582/B 05/2025

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



SOT - 1.1 max height

[illegible]

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

EXAMPLE BOARD LAYOUT

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE: 18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

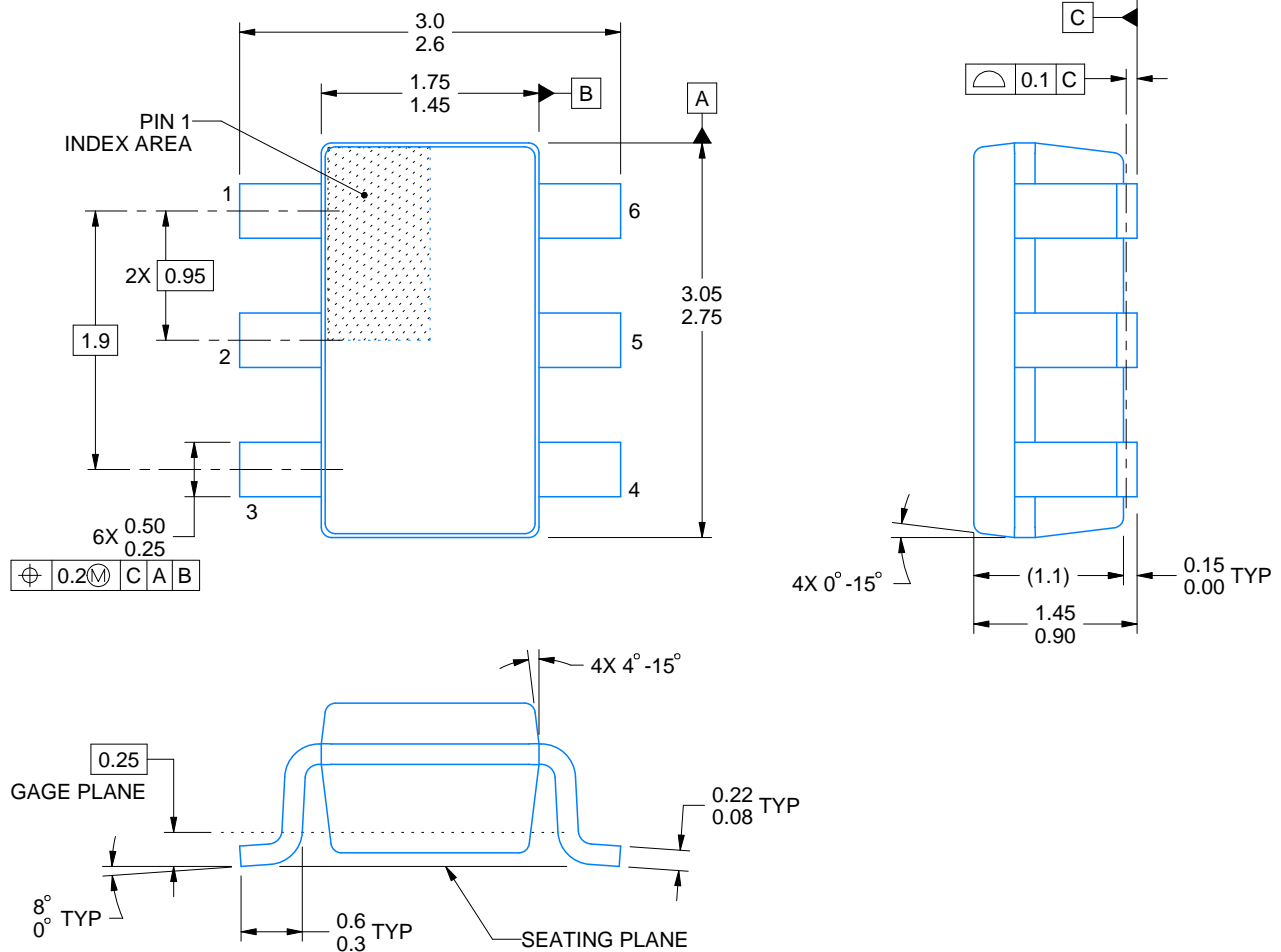
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DBV0006A**PACKAGE OUTLINE****SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224783/A



4218900/E 08/2022

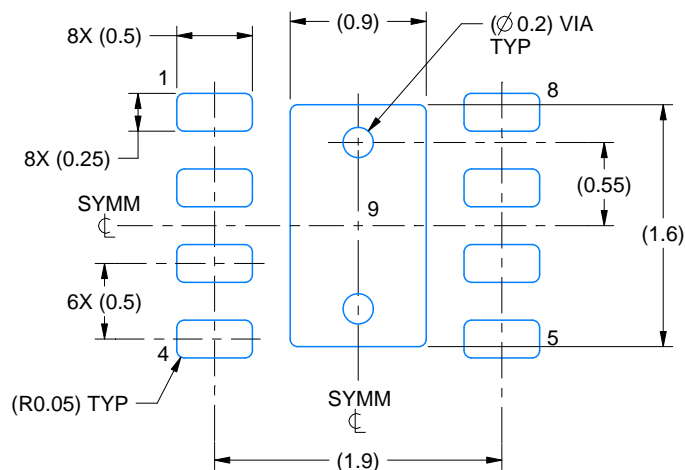
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4218900/E 08/2022

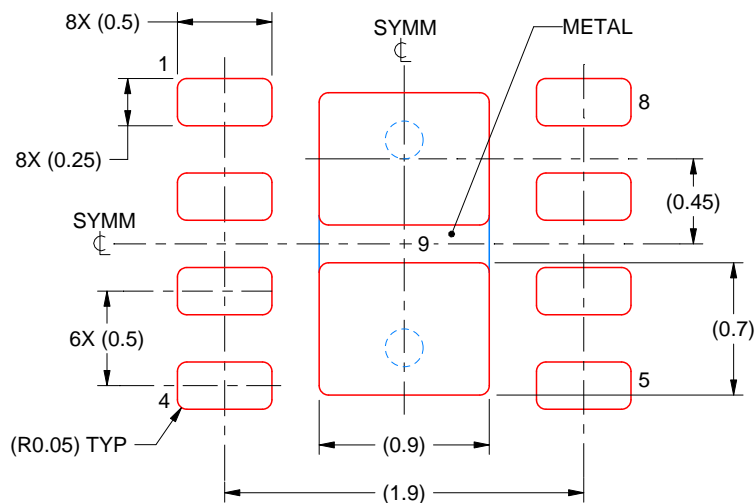
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PW0014A

PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

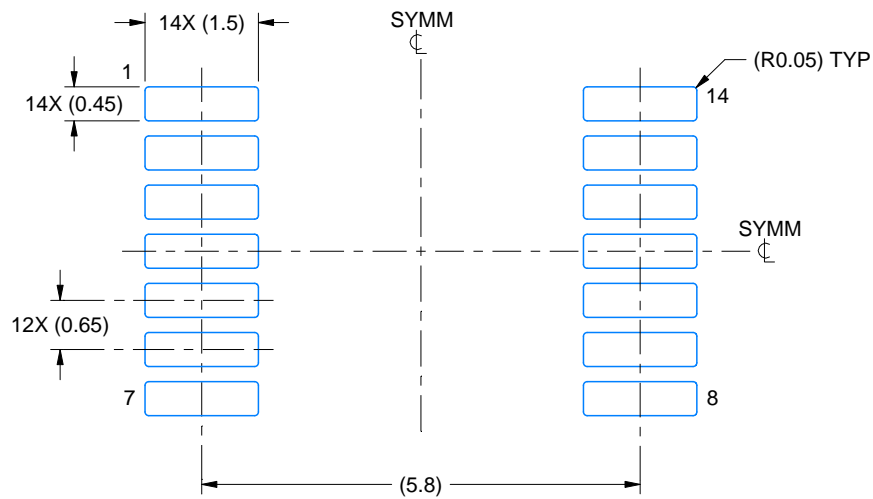
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

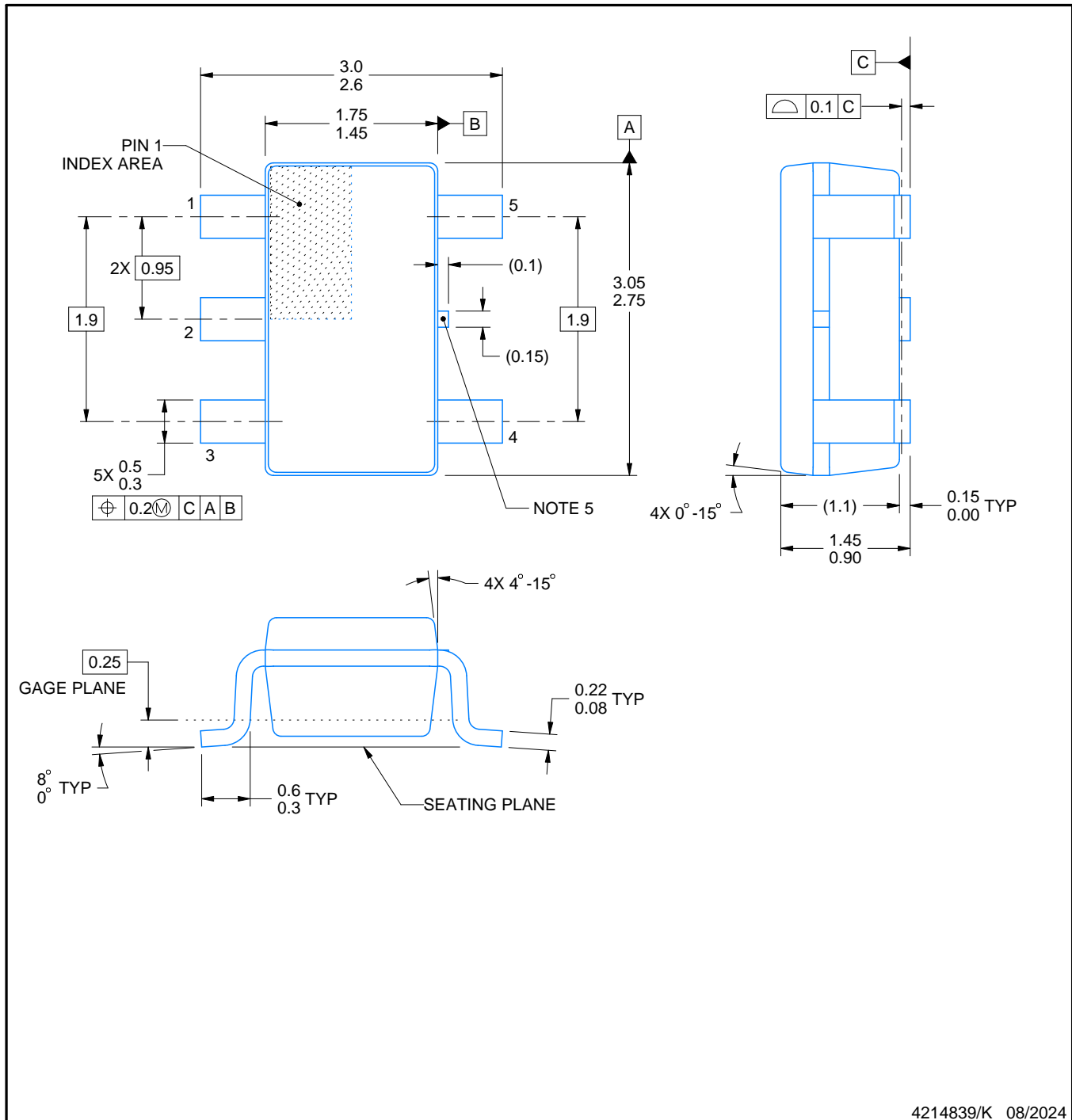
4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DBV0005A**PACKAGE OUTLINE****SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

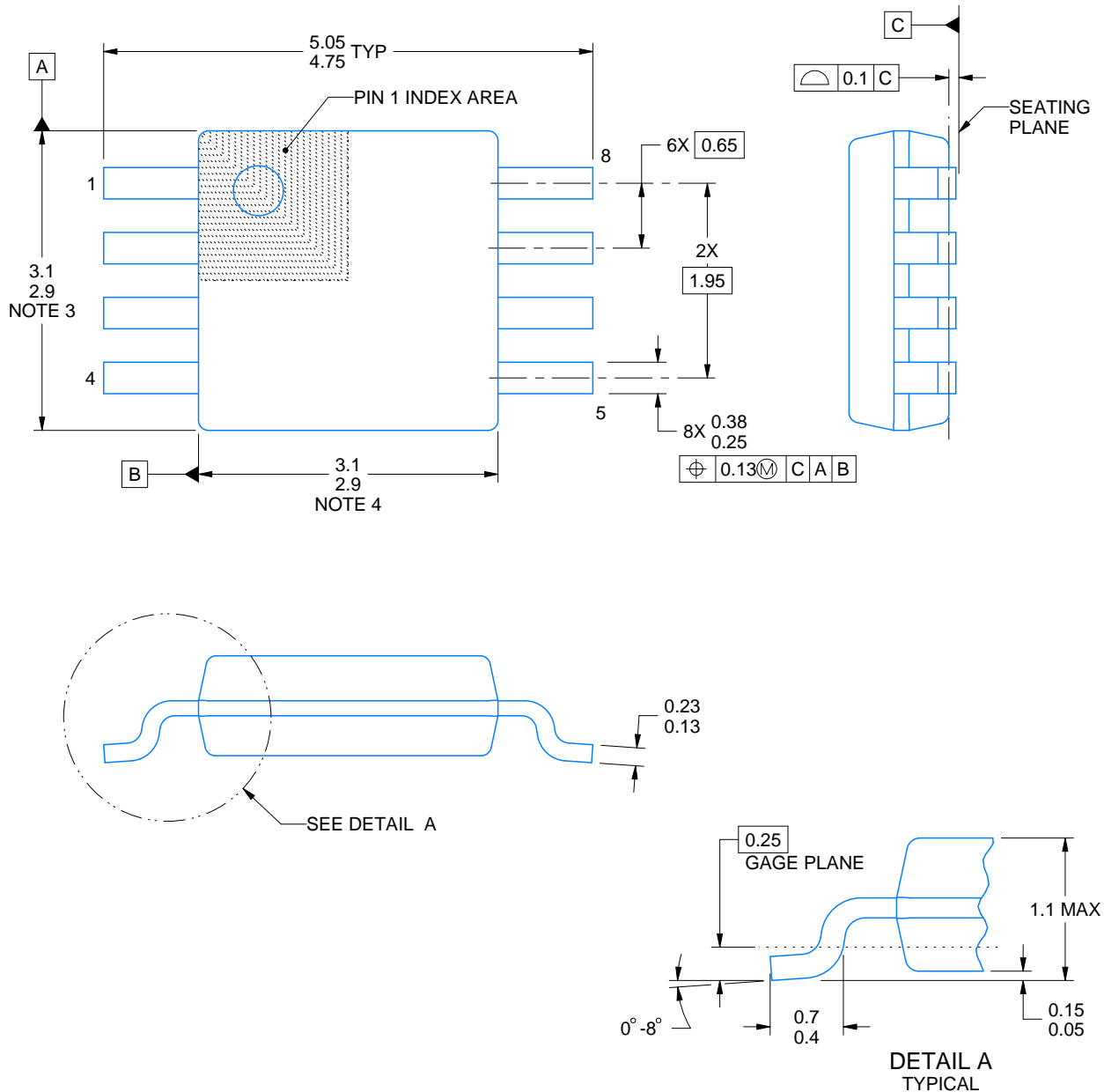
4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK0008A**PACKAGE OUTLINE****VSSOP - 1.1 mm max height**

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



SOT - 1.1 max height

Technical drawing of a connector housing, showing three views: front, side, and cross-section.

Front View:

- Overall width: 2.4
- Pin pitch: 1.8
- Pin width: 1.4
- Pin 1 INDEX AREA (hatched area)
- Pin 1 location: 1.1
- Pin 2 location: 1.1
- Pin 3 location: 1.1
- Pin 4 location: 1.1
- Pin 5 location: 1.1
- Pin 6 location: 1.1
- Pin 1 diameter: 0.30
- Pin 2 diameter: 0.15
- Pin 3 diameter: 0.15
- Pin 4 diameter: 0.15
- Pin 5 diameter: 0.15
- Pin 6 diameter: 0.15
- Pin 1 length: 0.65
- Pin 2 length: 0.65
- Pin 3 length: 0.65
- Pin 4 length: 0.65
- Pin 5 length: 0.65
- Pin 6 length: 0.65
- Pin 1 height: 1.3
- Pin 2 height: 1.3
- Pin 3 height: 1.3
- Pin 4 height: 1.3
- Pin 5 height: 1.3
- Pin 6 height: 1.3
- Pin 1 width: 0.30
- Pin 2 width: 0.15
- Pin 3 width: 0.15
- Pin 4 width: 0.15
- Pin 5 width: 0.15
- Pin 6 width: 0.15
- Pin 1 thickness: 0.65
- Pin 2 thickness: 0.65
- Pin 3 thickness: 0.65
- Pin 4 thickness: 0.65
- Pin 5 thickness: 0.65
- Pin 6 thickness: 0.65

Side View:

- Overall height: 2.15
- Pin pitch: 1.8
- Pin width: 1.4
- Pin 1 location: 1.1
- Pin 2 location: 1.1
- Pin 3 location: 1.1
- Pin 4 location: 1.1
- Pin 5 location: 1.1
- Pin 6 location: 1.1
- Pin 1 diameter: 0.30
- Pin 2 diameter: 0.15
- Pin 3 diameter: 0.15
- Pin 4 diameter: 0.15
- Pin 5 diameter: 0.15
- Pin 6 diameter: 0.15
- Pin 1 length: 0.65
- Pin 2 length: 0.65
- Pin 3 length: 0.65
- Pin 4 length: 0.65
- Pin 5 length: 0.65
- Pin 6 length: 0.65
- Pin 1 height: 1.3
- Pin 2 height: 1.3
- Pin 3 height: 1.3
- Pin 4 height: 1.3
- Pin 5 height: 1.3
- Pin 6 height: 1.3
- Pin 1 width: 0.30
- Pin 2 width: 0.15
- Pin 3 width: 0.15
- Pin 4 width: 0.15
- Pin 5 width: 0.15
- Pin 6 width: 0.15
- Pin 1 thickness: 0.65
- Pin 2 thickness: 0.65
- Pin 3 thickness: 0.65
- Pin 4 thickness: 0.65
- Pin 5 thickness: 0.65
- Pin 6 thickness: 0.65

Cross-section View:

- Overall width: 0.46 TYP
- Pin pitch: 1.8
- Pin width: 1.4
- Pin 1 location: 1.1
- Pin 2 location: 1.1
- Pin 3 location: 1.1
- Pin 4 location: 1.1
- Pin 5 location: 1.1
- Pin 6 location: 1.1
- Pin 1 diameter: 0.30
- Pin 2 diameter: 0.15
- Pin 3 diameter: 0.15
- Pin 4 diameter: 0.15
- Pin 5 diameter: 0.15
- Pin 6 diameter: 0.15
- Pin 1 length: 0.65
- Pin 2 length: 0.65
- Pin 3 length: 0.65
- Pin 4 length: 0.65
- Pin 5 length: 0.65
- Pin 6 length: 0.65
- Pin 1 height: 1.3
- Pin 2 height: 1.3
- Pin 3 height: 1.3
- Pin 4 height: 1.3
- Pin 5 height: 1.3
- Pin 6 height: 1.3
- Pin 1 width: 0.30
- Pin 2 width: 0.15
- Pin 3 width: 0.15
- Pin 4 width: 0.15
- Pin 5 width: 0.15
- Pin 6 width: 0.15
- Pin 1 thickness: 0.65
- Pin 2 thickness: 0.65
- Pin 3 thickness: 0.65
- Pin 4 thickness: 0.65
- Pin 5 thickness: 0.65
- Pin 6 thickness: 0.65

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4214835/D 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 THICK STENCIL
 SCALE:18X

4214835/D 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225944/A



4219117/B 04/2022

NOTES:

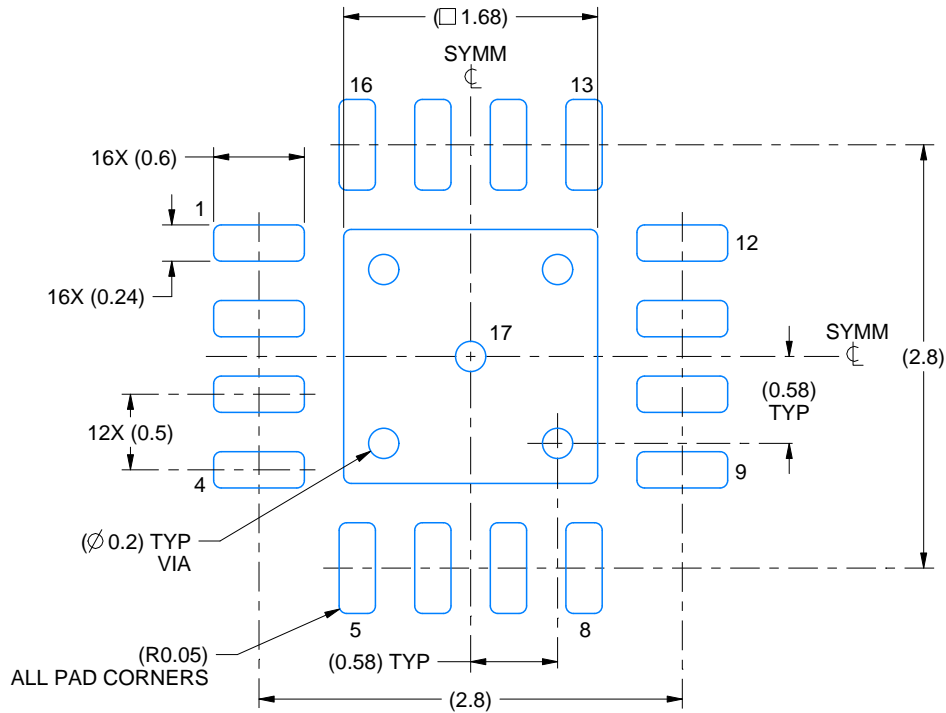
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

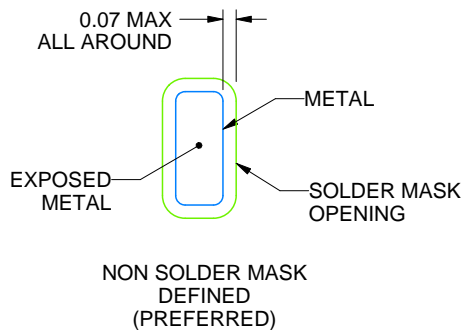
RTE0016C

WQFN - 0.8 mm max height

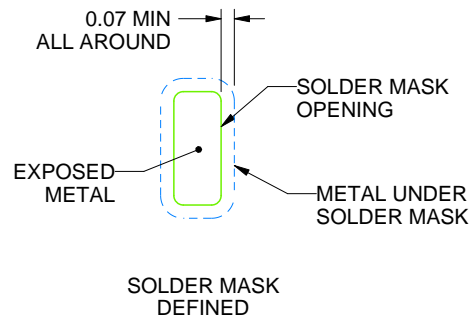
PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



NON SOLDER MASK
DEFINED
(PREFERRED)



SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4219117/B 04/2022

NOTES: (continued)

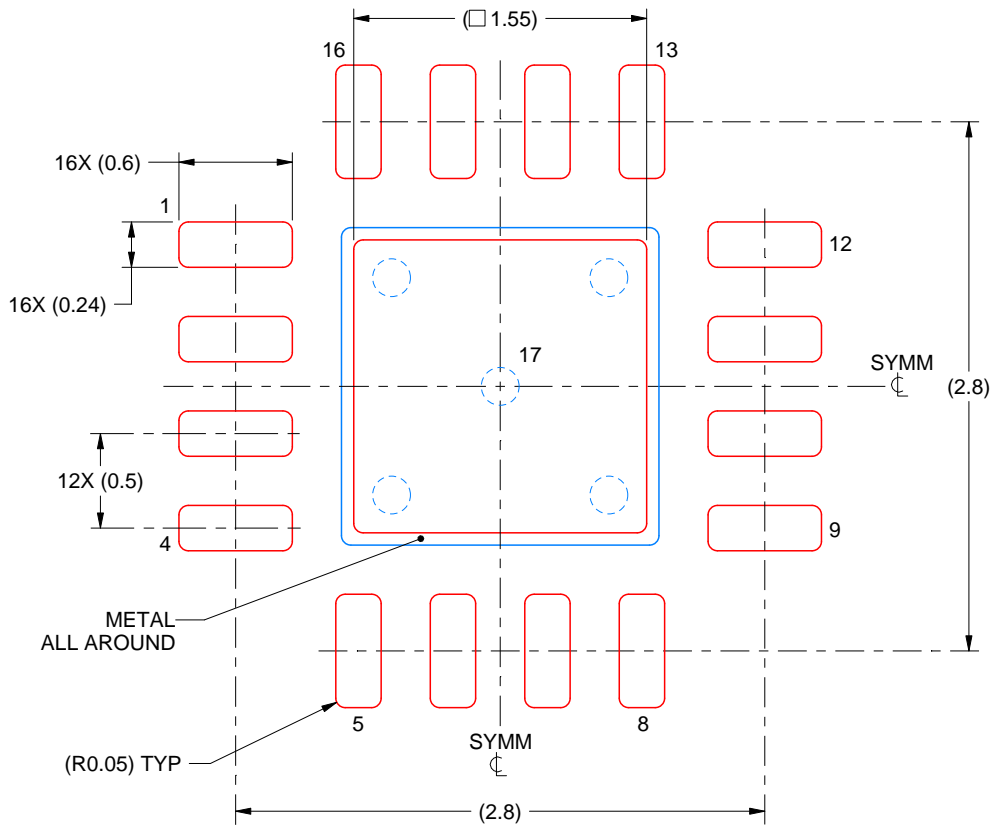
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RTE0016C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219117/B 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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