



## OPA2277-EP High-Precision, Low-Noise Operational Amplifier

### 1 Features

- Ultra-Low Offset Voltage: 10  $\mu\text{V}$
- High Open-Loop Gain: 134 dB
- High Common-Mode Rejection: 140 dB
- High Power Supply Rejection: 130 dB
- Low Bias Current: 1-nA Maximum
- Wide Supply Range:  $\pm 2$  to  $\pm 18$  V
- Low Quiescent Current: 800  $\mu\text{A}$ /Amplifier
- Supports Defense, Aerospace, and Medical Applications
  - Controlled Baseline
  - One Assembly and Test Site
  - One Fabrication Site
  - Available in Military ( $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ) Temperature Range <sup>(1)</sup>
  - Extended Product Life Cycle
  - Extended Product-Change Notification
  - Product Traceability

### 2 Applications

- Transducer Amplifier
- Bridge Amplifier
- Temperature Measurements
- Strain Gage Amplifier
- Precision Integrator
- Battery-Powered Instruments
- Test Equipment

(1) Additional temperature ranges available – contact factory

### 3 Description

The OPA2277 precision operational amplifier replaces the industry standard OP-177. It offers improved noise, wider output voltage swing, and is twice as fast with half the quiescent current. Features include ultra-low offset voltage and drift, low bias current, high common-mode rejection, and high power supply rejection.

OPA2277 operates from  $\pm 2$ -V to  $\pm 18$ -V supplies with excellent performance. Unlike most operational amplifiers, which are specified at only one supply voltage, the OPA2277 is specified for real-world applications; a single limit applies over the  $\pm 5$ -V to  $\pm 15$ -V supply range. High performance is maintained as the amplifiers swing to their specified limit. Because the initial offset voltage ( $\pm 20$   $\mu\text{V}$  max) is so low, user adjustment is usually not required.

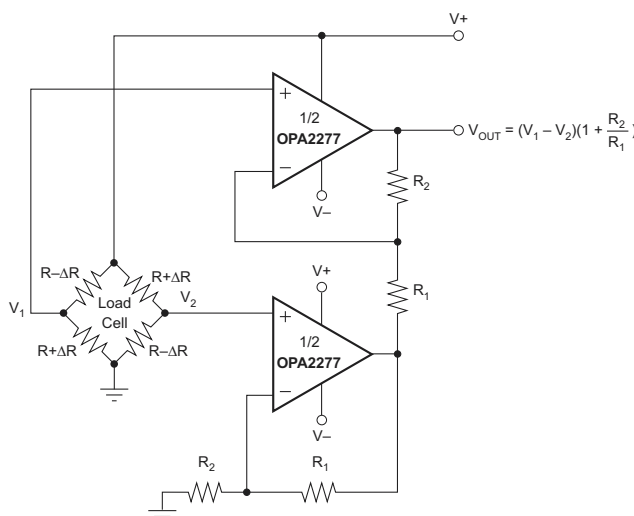
OPA2277 is easy to use and free from phase inversion and overload problems found in some operational amplifiers. It is stable in unity gain and provides excellent dynamic behavior over a wide range of load conditions. OPA2277 features completely independent circuitry for lowest crosstalk and freedom from interaction, even when overdriven or overloaded. Dual versions are available in DIP-8, SO-8. OPA2277 is fully specified and operates from  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

#### Device Information<sup>(1)</sup>

ORDER NUMBER	PACKAGE	BODY SIZE (NOM)
OPA2277MDTEP	SOIC (8)	3.91 mm x 4.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### 4 Load Cell Amplifier Schematic



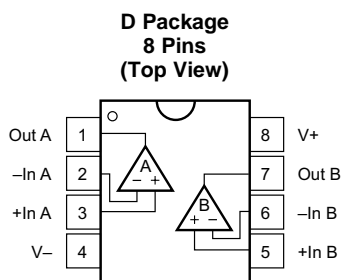
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## 5 Revision History

DATE	REVISION	NOTES
December 2014	*	Initial release.

## 6 Pin Configuration and Functions



**Pin Functions**

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT A	1	O	Amplifier output A
-IN A	2	I	Inverting amplifier input A
+IN A	3	I	Non-inverting amplifier input A
V-	4	I	Negative amplifier power supply input
+IN B	5	I	Non-inverting amplifier input B
-IN B	6	I	Inverting amplifier input B
OUT B	7	O	Amplifier output B
V+	8	I	Positive amplifier power supply input

## 7 Specifications

### 7.1 Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage		36	V
Input voltage	(V <sub>-</sub> ) – 0.7	(V <sub>+</sub> ) + 0.7	V
Output short-circuit (to ground) <sup>(2)</sup>	Continuous		
Operating temperature	–55	125	°C
Junction temperature		150	°C
Lead temperature (soldering, 10 s)		300	°C
T <sub>stg</sub> Storage temperature range	–55	125	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) One channel per package.

### 7.2 ESD Ratings

	VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±2000
	Machine model (MM)	±100

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
V <sub>S</sub> Specified voltage range	±5		±15	V
Operating voltage range	±2		±18	V
T <sub>J</sub> Operating junction temperature	–55		125	°C

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		OPA2277	UNIT
		D	
		8 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	91.9	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	39.9	
R <sub>θJB</sub>	Junction-to-board thermal resistance	40.6	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	3.9	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	39.6	
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Electrical Characteristics

At  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 5\text{ V}$  to  $\pm 15\text{ V}$ ,  $R_L = 2\text{ k}\Omega$  (unless otherwise noted).

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE								
V <sub>OS</sub>	Input offset voltage					±20	±65	μV
	vs temperature, T <sub>J</sub> = −55°C to 125°C						±150	μV
	vs temperature (dV <sub>OS</sub> /dT), T <sub>J</sub> = −55°C to 125°C					±0.15		μV/°C
	vs power supply (PSRR)		V <sub>S</sub> = ±2 V to ±18 V			±0.3	±1	μV/V
	T <sub>J</sub> = −55°C to 125°C		V <sub>S</sub> = ±2 V to ±18 V				±1	
	vs time					0.2		μV/mo
	Channel separation (dual)		dc			0.1		μV/V
INPUT BIAS CURRENT								
I <sub>B</sub>	Input bias current					±0.5	±2.8	nA
	T <sub>J</sub> = −55°C to 125°C						±7	
I <sub>OS</sub>	Input offset current					±0.5	±2.8	nA
	T <sub>J</sub> = −55°C to 125°C						±7	
NOISE								
Input voltage noise, f = 0.1 to 10 Hz					0.22			μVpp
					0.035			μVrms
e <sub>n</sub>	Input voltage noise density	f = 10 Hz			12			nV/√Hz
		f = 100 Hz			8			
		f = 1 Hz			8			
		f = 10 Hz			8			
i <sub>n</sub>	Current noise density	f = 1 kHz			0.2			pA/√Hz
INPUT VOLTAGE RANGE								
V <sub>CM</sub>	Common-mode voltage range				(V−) + 2		(V+) − 2	V
CMRR	Common-mode rejection T <sub>J</sub> = −55°C to 125°C		V <sub>CM</sub> = (V−) + 2 V to (V+) − 2 V		115	140		dB
			V <sub>CM</sub> = (V−) + 2 V to (V+) − 2 V		115			dB
INPUT IMPEDANCE								
Differential				100    3			MΩ    pF	
Common-mode		V <sub>CM</sub> = (V−) + 2 V to (V+) − 2 V		250    3			GΩ    pF	
OPEN-LOOP GAIN								
A <sub>OL</sub>	Open-loop voltage gain T <sub>J</sub> = −55°C to 125°C		V <sub>O</sub> = (V−) + 0.5 V to (V+) − 1.2 V, R <sub>L</sub> = 10 kΩ		140			dB
			V <sub>O</sub> = (V−) + 1.5 V to (V+) − 1.5 V, R <sub>L</sub> = 2 kΩ		126	134		
			V <sub>O</sub> = (V−) + 1.5 V to (V+) − 1.5 V, R <sub>L</sub> = 2 Ω		126			
FREQUENCY RESPONSE								
GBW	Gain bandwidth product				1			MHz
SR	Slew rate				0.8			V/μs
	Settling time	0.1%	V <sub>S</sub> = ±15 V, G = 1, 10-V step		14			μs
		0.01%	V <sub>S</sub> = ±15 V, G = 1, 10-V step		16			μs
Overload recovery time			V <sub>IN</sub> × G = V <sub>S</sub>		3			μs
Total harmonic distortion + noise (THD + N)			f = 1 kHz, G = 1, V <sub>O</sub> = 3.5 Vrms		0.002%			

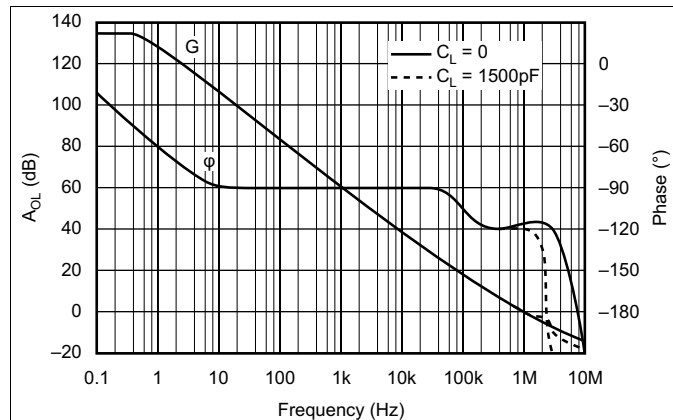
## Electrical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 5\text{ V}$  to  $\pm 15\text{ V}$ ,  $R_L = 2\text{ k}\Omega$  (unless otherwise noted).

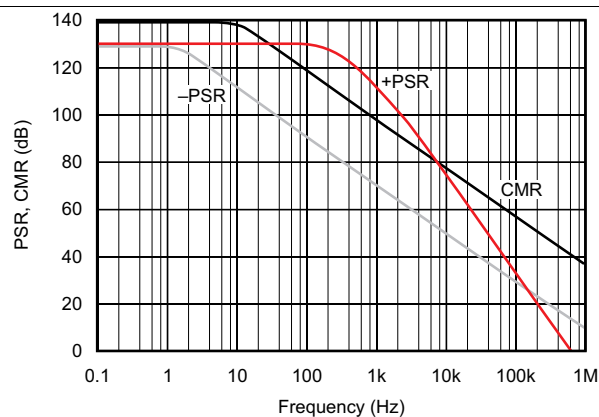
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
V <sub>O</sub>	Voltage output	R <sub>L</sub> = 10 kΩ	(V−) + 0.5		(V+) − 1.2	V
		R <sub>L</sub> = 10 kΩ, T <sub>J</sub> = −55°C to 125°C	(V−) + 0.5		(V+) − 1.2	
		R <sub>L</sub> = 2 kΩ	(V−) + 1.5		(V+) − 1.5	
		R <sub>L</sub> = 2 kΩ, T <sub>J</sub> = −55°C to 125°C	(V−) + 1.5		(V+) − 1.5	
I <sub>SC</sub>	Short-circuit current			±35		mA
C <sub>LOAD</sub>	Capacitive load drive		See <i>Typical Characteristics</i>			
POWER SUPPLY						
V <sub>S</sub>	Specified voltage range		±5		±15	V
	Operating voltage range		±2		±18	V
I <sub>Q</sub>	Quiescent current (per amplifier) T <sub>J</sub> = −55°C to 125°C	I <sub>O</sub> = 0 A		±790	±825	μA
		I <sub>O</sub> = 0 A			±900	μA
TEMPERATURE RANGE						
	Specified temperature range		−55		125	°C
	Operating temperature range		−55		125	°C
T <sub>stg</sub>	Storage temperature range		−55		125	°C

## 7.6 Typical Characteristics

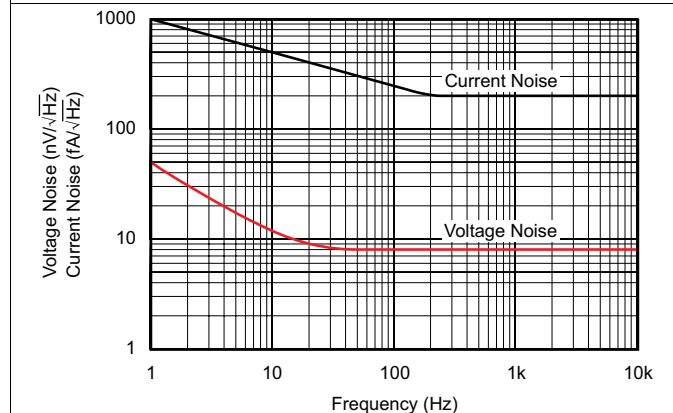
At  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ , and  $R_L = 2\text{ k}\Omega$ , unless otherwise noted.



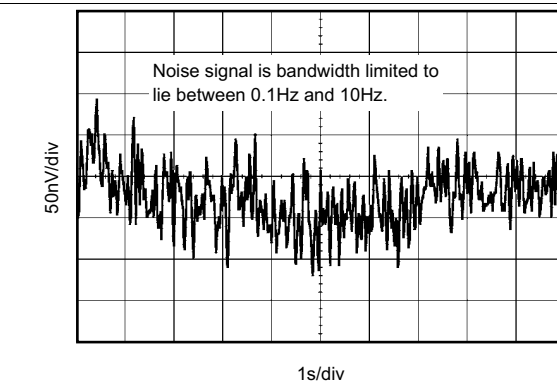
**Figure 1. Open-Loop Gain/Phase vs Frequency**



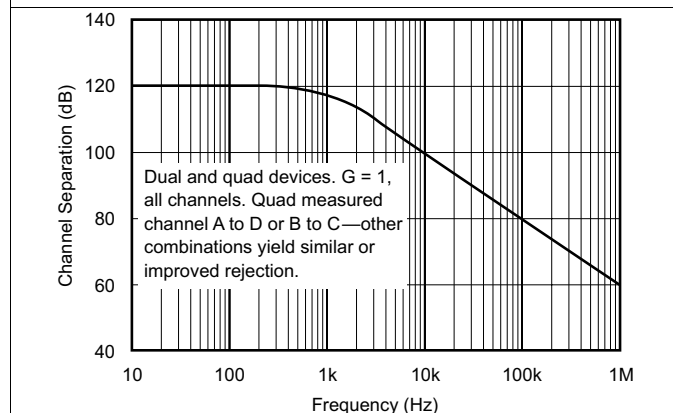
**Figure 2. Power Supply and Common-Mode Rejection vs Frequency**



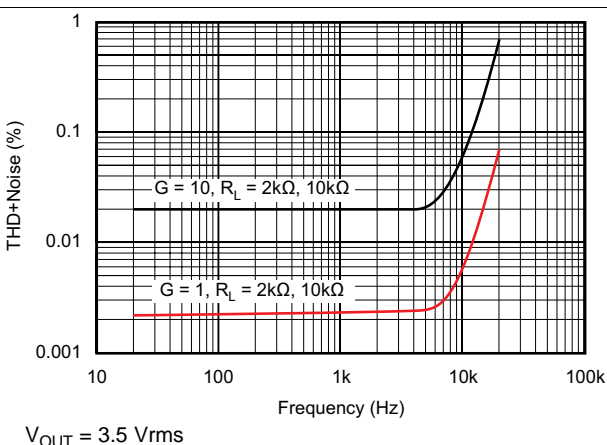
**Figure 3. Input Noise and Current Noise Spectral Density vs Frequency**



**Figure 4. Input Noise Voltage vs Time**



**Figure 5. Channel Separation vs Frequency**



**Figure 6. Total Harmonic Distortion + Noise vs Frequency**

## Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ , and  $R_L = 2\text{ k}\Omega$ , unless otherwise noted.

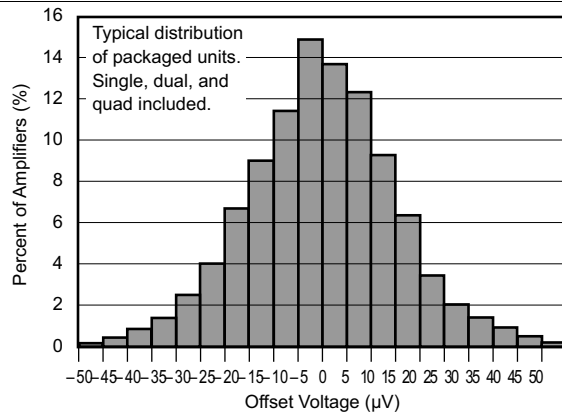


Figure 7. Offset Voltage Production Distribution

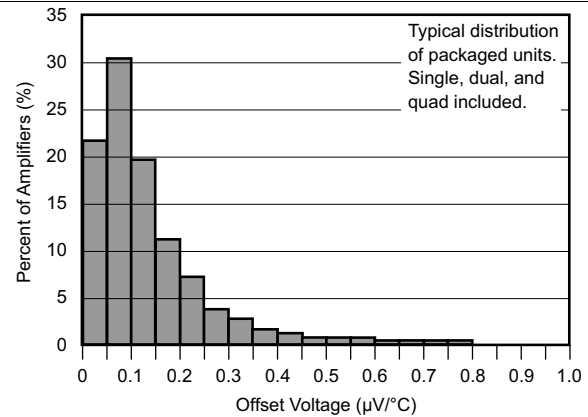


Figure 8. Offset Voltage Drift Production Distribution

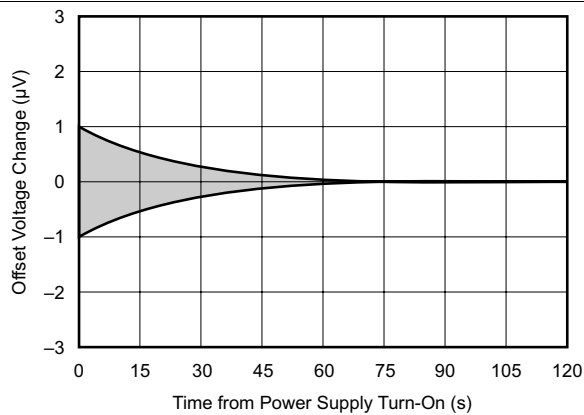


Figure 9. Warm-Up Offset Voltage Drift

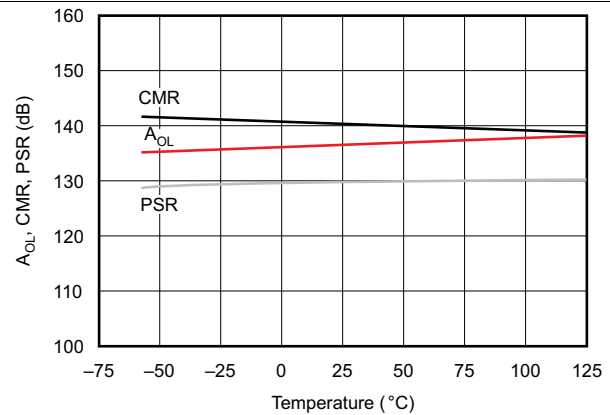


Figure 10.  $A_{OL}$ , CMR, PSR vs Temperature

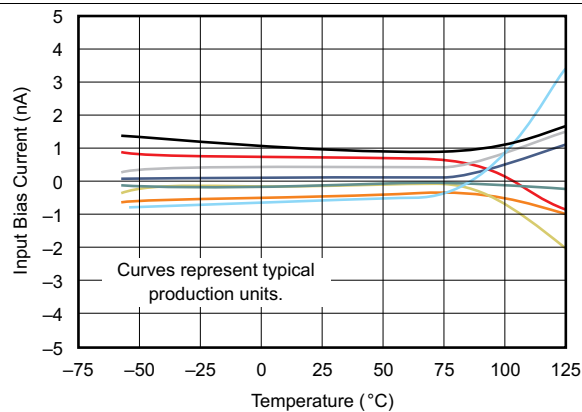


Figure 11. Input Bias Current vs Temperature

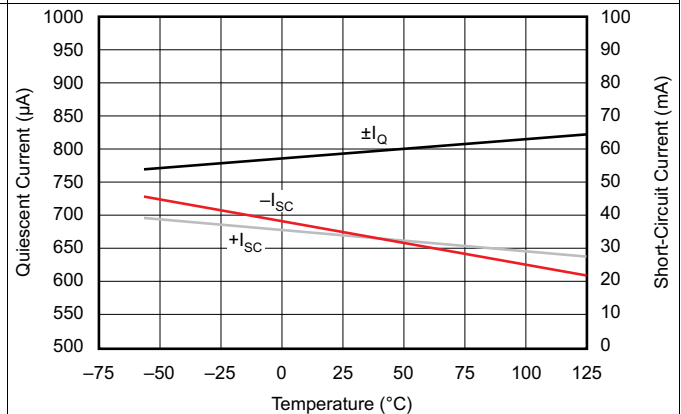
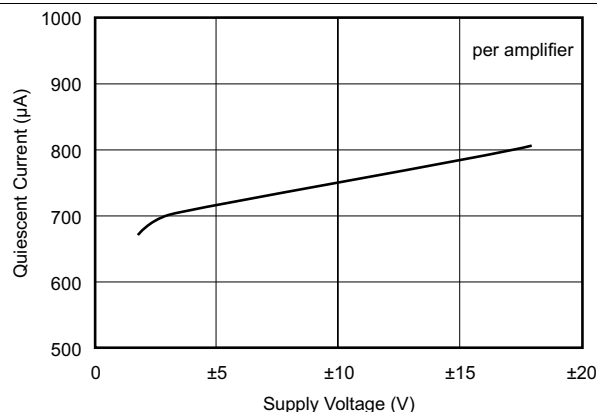


Figure 12. Quiescent Current and Short-Circuit Current vs Temperature

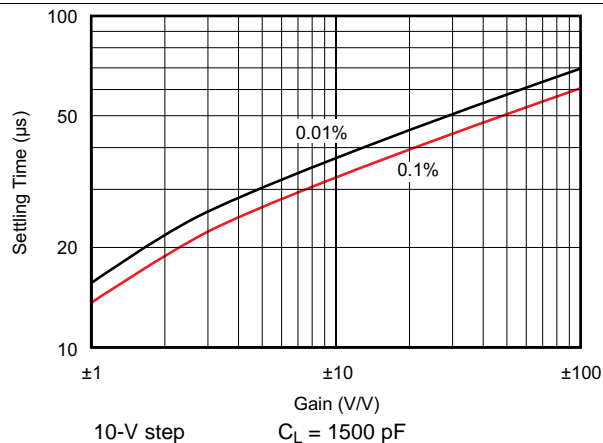


## Typical Characteristics (continued)

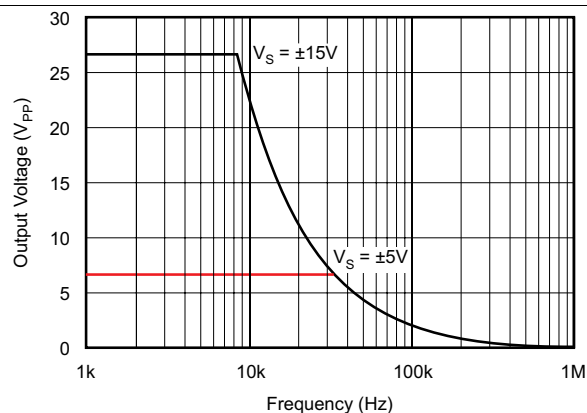
At  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ , and  $R_L = 2\text{ k}\Omega$ , unless otherwise noted.



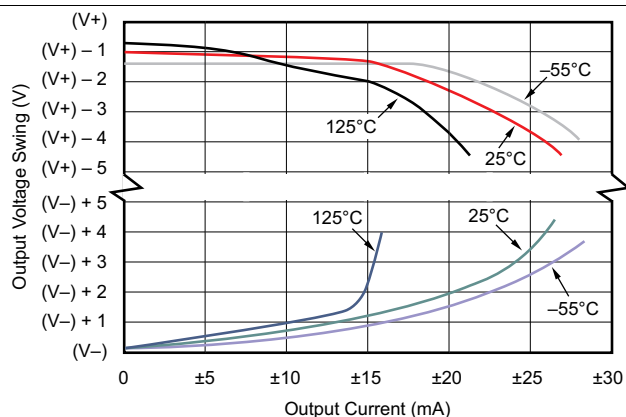
**Figure 13. Quiescent Current vs Supply Voltage**



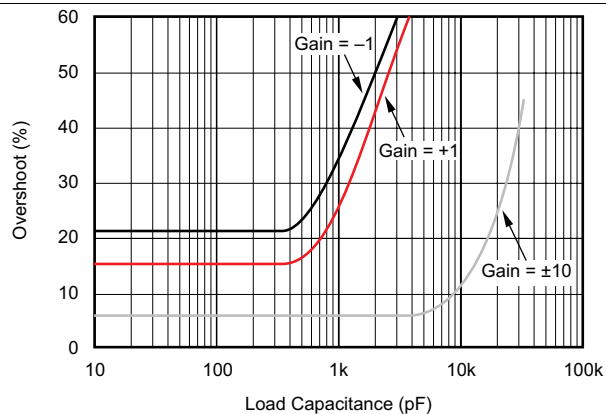
**Figure 14. Settling Time vs Closed-Loop Gain**



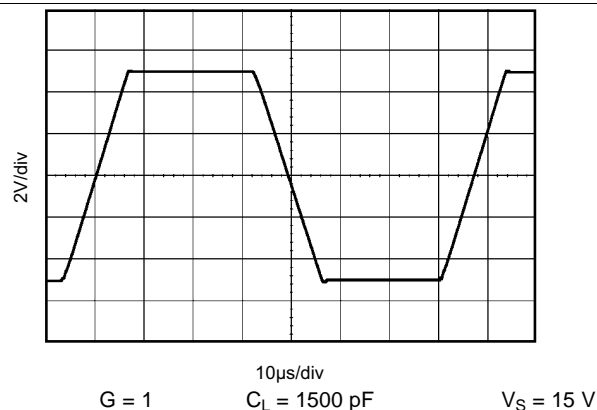
**Figure 15. Maximum Output Voltage vs Frequency**



**Figure 16. Output Voltage Swing vs Output Current**



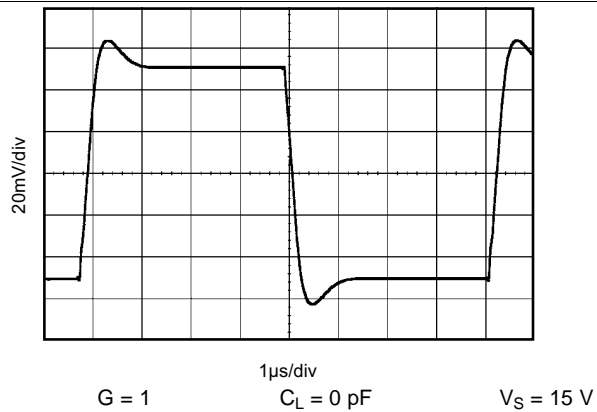
**Figure 17. Small-Signal Overshoot vs Load Capacitance**



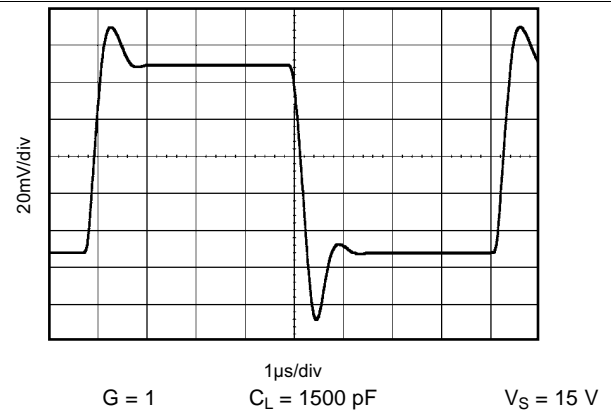
**Figure 18. Large-Signal Step Response**

## Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ , and  $R_L = 2\text{ k}\Omega$ , unless otherwise noted.



**Figure 19. Small-Signal Step Response**



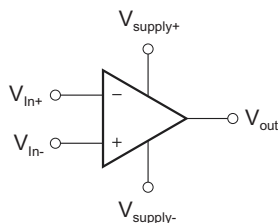
**Figure 20. Small-Signal Step Response**

## 8 Detailed Description

### 8.1 Overview

The OPA2277 is a unity-gain stable, high-precision, and low-noise operational amplifier. OPA2277 operates from  $\pm 2$ - to  $\pm 18$ -V supplies with excellent performance. Unlike most operational amplifiers which are specified at only one supply voltage, the OPA2277 is specified for real-world applications; a single limit applies over the  $\pm 5$ - to  $\pm 15$ -V supply range. High performance is maintained as the amplifiers swing to their specified limit. Because the initial offset voltage ( $\pm 50$ - $\mu$ V max) is so low, user adjustment is usually not required.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

The OPA2277 precision operational amplifier replaces the industry standard OP-177. It offers improved noise, wider output voltage swing, and is twice as fast with half the quiescent current. Features include ultra-low offset voltage and drift, low bias current, high common-mode rejection, and high power-supply rejection.

OPA2277 is easy to use and free from phase inversion and overload problems found in some operational amplifiers. It is stable in unity gain and provides excellent dynamic behavior over a wide range of load conditions. OPA2277 features completely independent circuitry for lowest crosstalk and freedom from interaction, even when overdriven or overloaded.

## 9 Application and Implementation

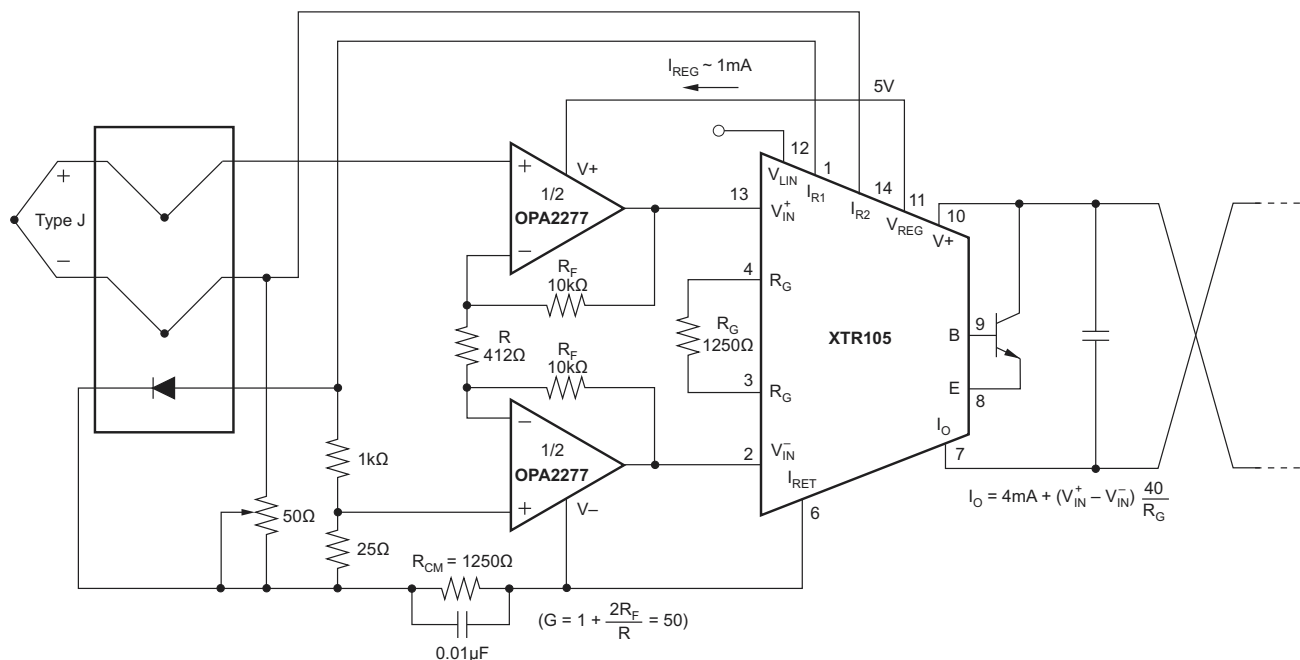
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The OPA2277 is unity-gain stable and free from unexpected output phase reversal, making it easy to use in a wide range of applications. Applications with noisy or high-impedance power supplies may require decoupling capacitors close to the device pins. In most cases, 0.1-μF capacitors are adequate.

### 9.2 Typical Application



**Figure 21. Thermocouple Low-Offset, Low-Drift Loop Measurement With Diode Cold Junction Compensation**

#### 9.2.1 Design Requirements

For the thermocouple low-offset, low-drift loop measurement with diode cold junction compensation (see [Figure 21](#)), [Table 1](#) lists the design parameters needed with gain = 50.

$$G = 1 + \frac{2R_F}{R} = 50 \quad (1)$$

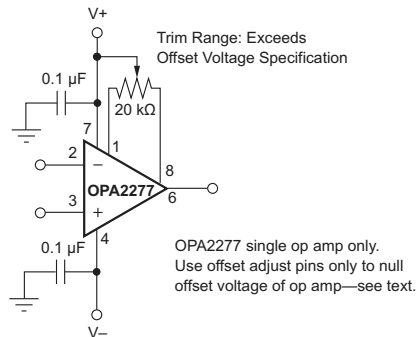
**Table 1. Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUE
R <sub>F</sub>	10 kΩ
R	412 Ω

## 9.2.2 Detailed Design Procedure

### 9.2.2.1 Offset Voltage Adjustment

The OPA2277 is laser-trimmed for very-low offset voltage and drift so most circuits do not require external adjustment. However, offset voltage trim connections are provided on pins 1 and 8. Offset voltage can be adjusted by connecting a potentiometer as shown in Figure 22. Only use this adjustment to null the offset of the operational amplifier. Do not use this adjustment to compensate for offsets created elsewhere in a system because this can introduce additional temperature drift.



**Figure 22. OPA2277 Offset Voltage Trim Circuit**

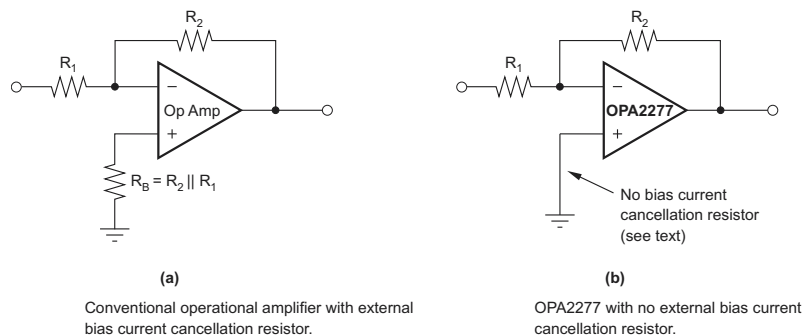
### 9.2.2.2 Input Protection

The inputs of the OPA2277 are protected with 1-kΩ series input resistors and diode clamps. The inputs can withstand  $\pm 30$ -V differential inputs without damage. The protection diodes conduct current when the inputs are overdriven. This may disturb the slewing behavior of unity-gain follower applications, but does not damage the operational amplifier.

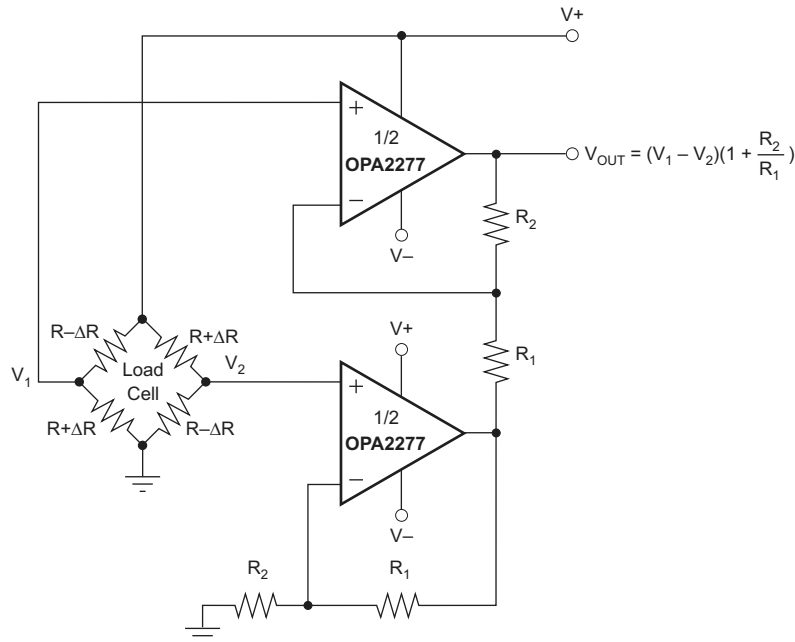
### 9.2.2.3 Input Bias Current Cancellation

The input stage base current of the OPA2277 is internally compensated with an equal and opposite cancellation circuit. The resulting input bias current is the difference between the input stage base current and the cancellation current. This residual input bias current can be positive or negative.

When the bias current is canceled in this manner, the input bias current and input offset current are approximately the same magnitude. As a result, it is not necessary to use a bias current cancellation resistor as is often done with other operational amplifiers (see Figure 23). A resistor added to cancel input bias current errors may actually increase offset voltage and noise.



**Figure 23. Input Bias Current Cancellation**

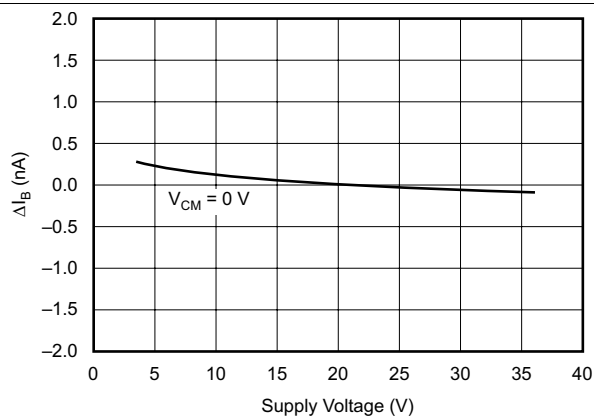


A. For integrated solution see: INA126, INA2126 (dual), INA125 (on-board reference), or INA122 (single-supply).

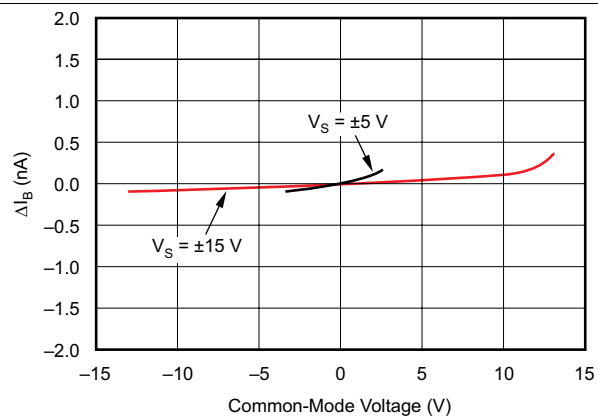
**Figure 24. Load Cell Amplifier**

### 9.2.3 Application Curves

At  $T_J = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ , and  $R_L = 2\text{ k}\Omega$ . **Figure 25** shows Change in input bias current versus power supply voltage. Curve shows normalized change in bias current with respect to  $V_S = \pm 10\text{ V}$  (+20 V). Typical  $I_B$  may range from  $-0.5$  to  $0.5\text{ nA}$  at  $V_S = \pm 10\text{ V}$ . **Figure 26** shows change in input bias current versus common-mode voltage. Curve shows normalized change in bias current with respect to  $V_{CM} = 0\text{ V}$ . Typical  $I_B$  may range from  $-0.5$  to  $0.5\text{ nA}$  at  $V_{CM} = 0\text{ V}$ .



**Figure 25. Change in Input Bias Current vs Power Supply Voltage**



**Figure 26. Change in Input Bias Current vs Common-Mode Voltage**

## 10 Power Supply Recommendations

The OPA2277 operational amplifier operates from  $\pm 2.5$ - to  $\pm 18$ -V supplies with excellent performance. Unlike most operational amplifiers which are specified at only one supply voltage, the OPA2277 is specified for real-world applications. A single set of specifications applies over the  $\pm 5$ - to  $\pm 15$ -V supply range. Specifications are ensured for applications between  $\pm 5$ - and  $\pm 15$ -V power supplies. Some applications do not require equal positive and negative output voltage swing. Power supply voltages do not need to be equal. The OPA2277 can operate with as little as 5 V between the supplies and with up to 36 V between the supplies. For example, the positive supply could be set to 25 V with the negative supply at  $-5$  V, or vice-versa. In addition, key parameters are ensured over the specified temperature range,  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The [Typical Characteristics](#) show parameters which vary significantly with operating voltage or temperature.

## 11 Layout

### 11.1 Layout Guidelines

Solder the lead-frame die pad to a thermal pad on the PCB. Mechanical drawings in [Mechanical, Packaging, and Orderable Information](#) show the physical dimensions for the package and pad.

Soldering the exposed pad significantly improves board-level reliability during temperature cycling, key push, package shear, and similar board-level tests. Even with applications that have low-power dissipation, the exposed pad must be soldered to the PCB to provide structural integrity and long-term reliability.

The OPA2277 has very-low offset voltage and drift. To achieve highest performance, optimize circuit layout and mechanical conditions. Offset voltage and drift can be degraded by small thermoelectric potentials at the operational amplifier inputs. Connections of dissimilar metals generate thermal potential which can degrade the ultimate performance of the OPA2277. These thermal potentials can be made to cancel by assuring that they are equal in both input terminals.

- Keep thermal mass of the connections made to the two input terminals similar.
- Locate heat sources as far as possible from the critical input circuitry.
- Shield operational amplifier and input circuitry from air currents such as cooling fans.

### 11.2 Layout Example

#### 11.2.1 Board Layout

This demonstration fixture is a two-layer PCB. It uses a ground plane on the bottom, and signal and power traces on the top. The ground plane has been opened up around Op Amp pins sensitive to capacitive loading. Power-supply traces are laid out to keep current loop areas to a minimum. The SMA (or SMB) connectors may be mounted either vertically or horizontally.

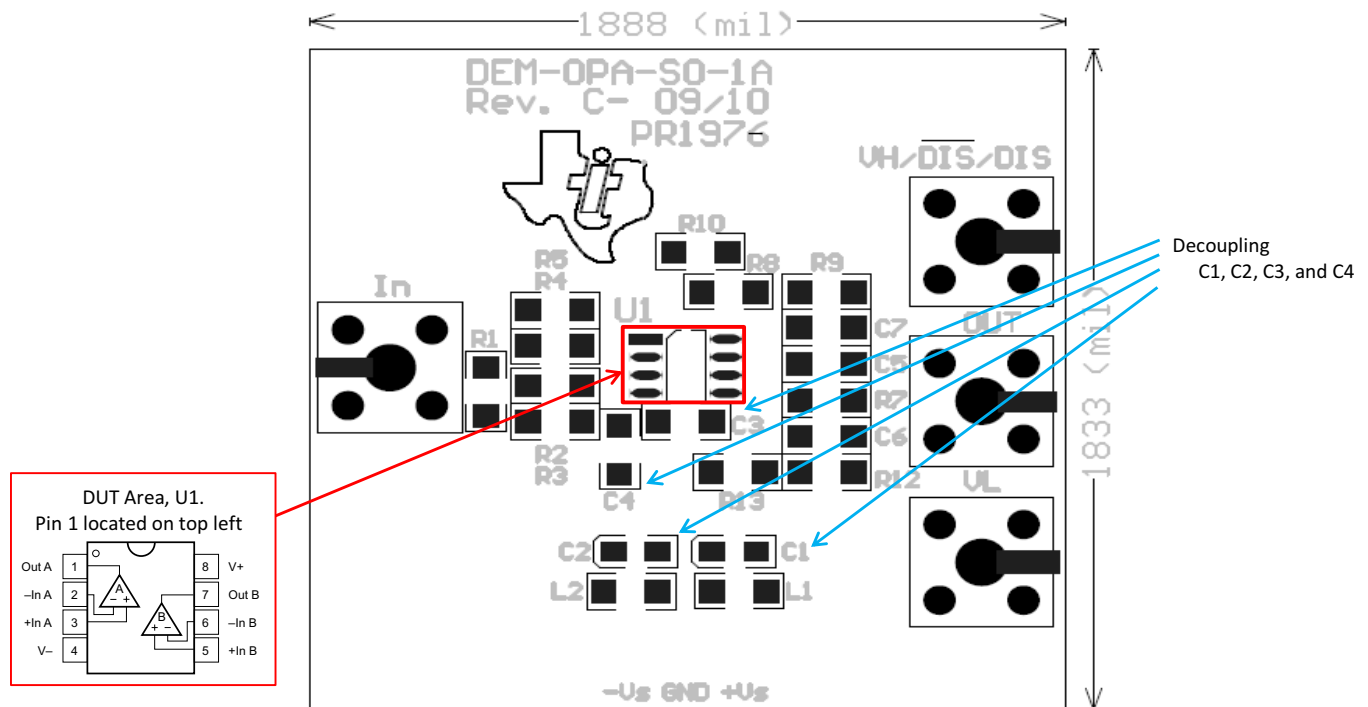
The location and type of capacitors used for power-supply bypassing are crucial to high-frequency amplifiers. The tantalum capacitors,  $C_1$  and  $C_2$ , do not need to be as close to pins 7 and 4 on your PCB, and may be shared with other amplifiers.

#### 11.2.2 Measurement Tips

This demonstration fixture and the component values shown are designed to operate in a  $50\Omega$  environment. Most data sheet plots are obtained in this manner. Change the component values for different input and output impedance levels.

Do not use high-impedance probes; they represent a heavy capacitive load to the Op Amps, and will alter the amplifier response. Instead, use low impedance ( $\leq 500\Omega$ ) probes with adequate bandwidth. The probe input capacitance and resistance set an upper limit on the measurement bandwidth. If a high-impedance probe must be used, place a  $100\Omega$  resistor on the probe tip to isolate its capacitance from the circuit.

## Layout Example (continued)



**Figure 27. Decoupling Capacitors and DUT Area**



## 12 Device and Documentation Support

### 12.1 Trademarks

All trademarks are the property of their respective owners.

### 12.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">OPA2277MDTEP</a>	Active	Production	SOIC (D)   8	250   SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	OPA 2277E
OPA2277MDTEP.A	Active	Production	SOIC (D)   8	250   SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	OPA 2277E

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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**OTHER QUALIFIED VERSIONS OF OPA2277-EP :**

- Catalog : [OPA2277](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**D0008A****PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

**NOTES:**

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

**D0008A**

## SOIC - 1.75 mm max height

## SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



## SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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