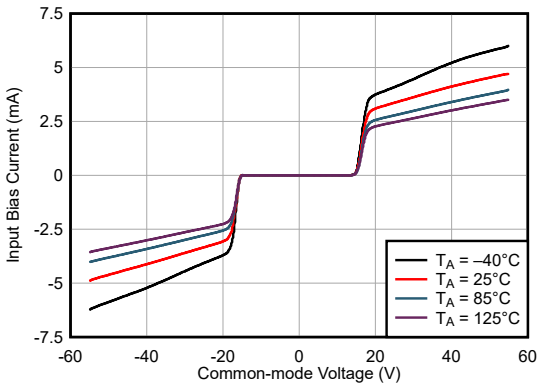
OPAx206 Input-Overvoltage-Protected, 4-µV, 0.08-µV/°C, Low-Power Super Beta, e-trim™ Operational Amplifiers

1 Features

- Integrated input overvoltage protection up to ±40 V beyond supplies
- e-trim™ operational amplifier performance
  - Low offset voltage: 25 µV (max)
  - Low offset voltage drift: ±0.5 µV/°C (max)
- Super beta inputs
  - Input bias current: 500 pA (max)
  - Input current noise: 110 fA/√Hz
- Low noise
  - 0.1-Hz to 10-Hz: 0.2 μV_{PP}
  - Voltage noise: 8 nV/√Hz
- A_{OL}, CMRR, and PSRR: > 124 dB (full temperature range)
- Gain bandwidth product: 3.6 MHz
- Low quiescent current: 240 µA (max)
- Slew rate: 4 V/µs
- Overload power limiter
- Rail-to-rail output
- EMI and RFI filtered inputs
- Wide supply: 4.5 V to 36 V
- Temperature range: –40°C to +125°C

2 Applications

- Analog input module
- Mixed module (AI,AO,DI,DO)
- Lab and field Instrumentation
- Source measurement unit (SMU)
- Digital multimeter (DMM)
- Train control and management
- String inverter
- Data acquisition (DAQ)



OPAx206 Input Overvoltage Protection

3 Description

The OPA206, OPA2206, and OPA4206 (OPAx206) are the next generation of the industry-standard OPAx277 family with the added feature of input overvoltage protection. These precision, bipolar, e-trim™ op amps with super-beta inputs use TI's proprietary trimming technology to achieve an input offset voltage of ±4 µV (typical) and an input offset voltage drift of ±0.08 µV/°C (typical). The input overvoltage protection activates when the input signal exceeds the supply range and protects up to 40 V beyond either supply. This feature eliminates the need for external circuitry to prevent amplifier damage, thereby reducing size and costs.

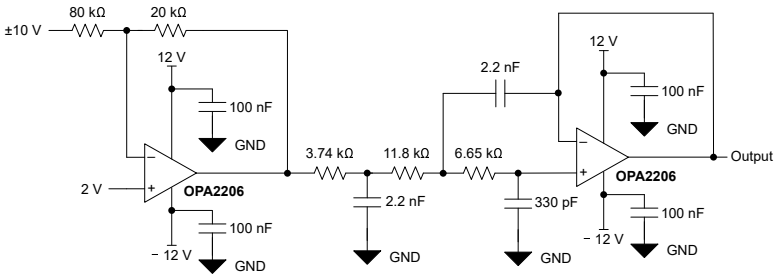
The OPAx206 provide a speed-to-power ratio of 3.6 MHz for a mere 220 µA (typical). These devices also achieve a low voltage noise density of only 8 nV/√Hz at 1 kHz. The super-beta inputs of the OPAx206 have a very low input bias current of 100 pA (typical) and a current noise density of 110 fA/√Hz.

The high performance of the OPAx206 make these devices an excellent choice for systems requiring high precision and low power consumption, such as high-density analog input modules in programmable logic controllers, field and portable instrumentation systems, and source measurement units. The OPA205 and OPA2205 are related devices with the same op amp core without the input protection, but with improved broadband noise (7.2 nV/√Hz).

Device Information

PART NUMBER	CHANNELS	PACKAGE(1)
OPA206	Single	D (SOIC, 8)
OPA2206	Dual	D (SOIC, 8)
		DGK (VSSOP, 8)
OPA4206	Quad	D (SOIC, 14)
		PW (TSSOP, 14)

(1) For more information, see Section 11.



OPAx206 Typical Application

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4 Pin Configuration and Functions

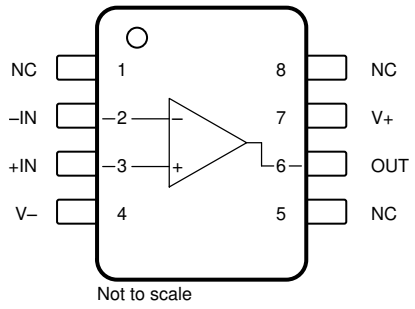

Figure 4-1. OPA206: D Package, 8-Pin SOIC (Top View)

Table 4-1. Pin Functions: OPA206

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN	3	Input	Noninverting input
–IN	2	Input	Inverting input
NC	1, 5, 8	—	No internal connection (can be left floating)
OUT	6	Output	Output
V+	7	Power	Positive (highest) power supply
V–	4	Power	Negative (lowest) power supply

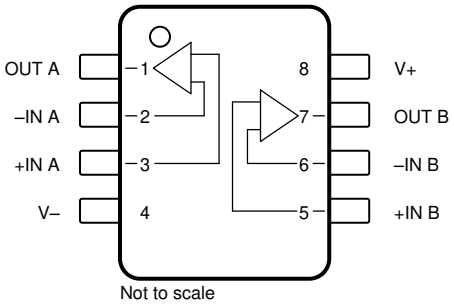

Figure 4-2. OPA2206: D Package, 8-pin SOIC and DGK Package, 8-Pin VSSOP (Top View)

Table 4-2. Pin Functions: OPA2206

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN A	3	Input	Noninverting input, channel A
–IN A	2	Input	Inverting input, channel A
+IN B	5	Input	Noninverting input, channel B
–IN B	6	Input	Inverting input, channel B
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
V+	8	Power	Positive (highest) power supply
V–	4	Power	Negative (lowest) power supply

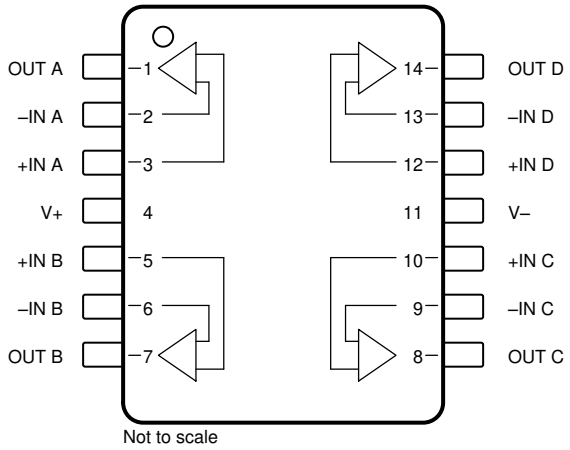

Figure 4-3. OPA4206: D Package, 14-Pin SOIC and PW Package, 14-Pin TSSOP (Top View)

Table 4-3. Pin Functions: OPA4206

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN A	3	Input	Noninverting input, channel A
+IN B	5	Input	Noninverting input, channel B
+IN C	10	Input	Noninverting input, channel C
+IN D	12	Input	Noninverting input, channel D
–IN A	2	Input	Inverting input, channel A
–IN B	6	Input	Inverting input, channel B
–IN C	9	Input	Inverting input,channel C
–IN D	13	Input	Inverting input, channel D
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
OUT C	8	Output	Output, channel C
OUT D	14	Output	Output, channel D
V+	4	Power	Positive (highest) power supply
V–	11	Power	Negative (lowest) power supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	Single supply		40	V
		Dual supply		±20	
	Signal input pin voltage		(V–) – 40	(V+) + 40	V
	Output short-circuit[2]		Continuous		
T_A	Operating temperature		–40	150	°C
T_J	Junction temperature			150	°C
T_{STG}	Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short-circuit to ground, one amplifier per package.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JANSI/ESDA/JEDEC JS-002[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	Single supply	4.5		36	V
		Dual supply	±2.25		±18	
T_A	Operating temperature		–40		125	°C

5.4 Thermal Information: OPA206

THERMAL METRIC[1]		OPA206	UNIT
		D (SOIC)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	129.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	69.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	73.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	21.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	72.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Thermal Information: OPA2206

THERMAL METRIC[1]		OPA2206		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	124.8	175.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	64.9	63.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	68.1	97.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	17.1	7.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	67.4	95.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.6 Thermal Information: OPA4206

THERMAL METRIC[1]		OPA4206		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	71.5	96.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.9	25.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.7	54.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.3	2.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	33.2	53.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.7 Electrical Characteristics: V_S = ±5 V

at T_A = 25°C, V_{CM} = V_{OUT} = midsupply, and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±4	±25	µV
		T_A = –40°C to +125°C				±55	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C			±0.08	±0.5	µV/°C
PSRR	Power supply rejection ratio	V_S = ±2.25 V to ±18 V			±0.05	±0.5	µV/V
			T_A = –40°C to +125°C			±1	
	Channel separation	f = dc			130		dB
		f = 100 kHz			110		
INPUT BIAS CURRENT							
I_B	Input bias current				±0.1	±0.5	nA
		T_A = 0°C to 85°C				±0.75	
		T_A = –40°C to +125°C				±1	
I_{OS}	Input offset current				±0.1	±0.4	nA
		T_A = 0°C to 85°C				±0.5	
		T_A = –40°C to +125°C				±0.6	
NOISE							
	Input voltage noise	f = 0.1 Hz to 10 Hz			0.2		$µV_{PP}$
e_n	Input voltage noise density	f = 10 Hz			8.4		nV/√Hz
		f = 100 Hz			8.1		
		f = 1 kHz			8		
i_n	Input current noise	f = 1 kHz			110		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage			(V–) + 1		(V+) – 1.4	V
CMRR	Common-mode rejection ratio	(V–) + 1 V < V_{CM} < (V+) – 1.4 V, T_A = –40°C to +125°C		124	140		dB
INPUT OVERVOLTAGE							
	Input overvoltage protection	T_A = –40°C to +125°C		(V–) – 40		(V+) + 40	V
	Input current in overvoltage protected mode	V_S = 0 V, (V–) – 40 V < V_{CM} < (V+) + 40 V			4.8	10	mA
			T_A = –40°C to +125°C	See Typical Characteristics			
INPUT IMPEDANCE							
Z_{ID}	Differential				9 || 4.4		MΩ || pF
Z_{ICM}	Common-mode				300 || 4.4		GΩ || pF

5.7 Electrical Characteristics: V_S = ±5 V (continued)

at T_A = 25°C, V_{CM} = V_{OUT} = midsupply, and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	T_A = –40°C to +125°C, (V–) + 200 mV < V_O < (V+) – 200 mV	R_L = 10 kΩ	126	132		dB
			R_L = 2 kΩ	126	130		
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				3.6		MHz
SR	Slew rate	4-V step, gain = –1			3.2		V/µs
	Phase margin	R_L = 10 kΩ, C_L = 25 pF			67		degrees
t_S	Settling time	To 0.024% (12-bit), 4-V step, gain = 1, C_L = 30 pF	Falling		2.2		µs
			Rising		2.8		
	Overload recovery time	Gain = –10			0.3		µs
THD+N	Total harmonic distortion + noise	V_O = 5 V_{PP}, gain = +1, f = 1 kHz, R_L = 2 kΩ			0.0004		%
OUTPUT							
	Voltage output swing from rail	A_{OL} > 126 dB	R_L = 10 kΩ	(V–) + 0.2		(V+) – 0.2	V
			R_L = 2 kΩ	(V–) + 0.2		(V+) – 0.2	
		T_A = –40°C to +125°C, R_L = 10 kΩ		(V–) + 0.2		(V+) – 0.2	
I_{SC}	Short-circuit current				±25		mA
C_{LOAD}	Capacitive load drive			See Typical Characteristics			
R_O	Open-loop output impedance			See Typical Characteristics			
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 mA			220	240	µA
			T_A = –40°C to +125°C			310	

5.8 Electrical Characteristics: V_S = ±15 V

at T_A = 25°C, V_{CM} = V_{OUT} = midsupply and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±4	±25	µV
		T_A = –40°C to +125°C				±55	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C			±0.08	±0.5	µV/°C
PSRR	Power supply rejection ratio	V_S = ±2.25 V to ±18 V			±0.05	±0.5	µV/V
			T_A = –40°C to +125°C			±1	
	Channel separation	f = dc			130		dB
		f = 100 kHz			110		
INPUT BIAS CURRENT							
I_B	Input bias current				±0.1	±0.5	nA
		T_A = 0°C to 85°C				±1	
		T_A = –40°C to +125°C				±1.2	
I_{OS}	Input offset current				±0.1	±0.4	nA
		T_A = 0°C to 85°C				±0.8	
		T_A = –40°C to +125°C				±0.9	
NOISE							
	Input voltage noise	f = 0.1 Hz to 10 Hz			0.2		$µV_{PP}$
e_n	Input voltage noise density	f = 10 Hz			8.4		nV/√Hz
		f = 100 Hz			8.1		
		f = 1 kHz			8		
i_n	Input current noise	f = 1 kHz			110		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage			(V–) + 1		(V+) – 1.4	V
CMRR	Common-mode rejection ratio	(V–) + 1 V < V_{CM} < (V+) – 1.4 V		126	140		dB
			T_A = –40°C to +125°C	124	140		
INPUT OVERVOLTAGE							
	Input overvoltage protection	T_A = –40°C to +125°C		(V–) – 40		(V+) + 40	V
	Input current in overvoltage protected mode	V_S = 0 V, (V–) – 40 V < V_{CM} < (V+) + 40 V			4.8	10	mA
			T_A = –40°C to +125°C	See Typical Characteristics			
INPUT IMPEDANCE							
Z_{ID}	Differential				9 || 4.4		MΩ || pF
Z_{ICM}	Common-mode				300 || 4.3		GΩ || pF

5.8 Electrical Characteristics: V_S = ±15 V (continued)

at T_A = 25°C, V_{CM} = V_{OUT} = midsupply and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	R_L = 10 kΩ, (V–) + 200 mV < V_O < (V+) – 200 mV, T_A = –40°C to +125°C		126	132		dB
		R_L = 2 kΩ, (V–) + 350 mV < V_O < (V+) – 350 mV, T_A = –40°C to +125°C		126	130		
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	C_L = 30 pF			3.6		MHz
SR	Slew rate	10-V step, gain = –1			4		V/µs
	Phase margin	R_L = 10 kΩ, C_L = 25 pF			67		degrees
t_S	Settling time	To 0.024% (12-bit), 10-V step, gain = 1, C_L = 30 pF	Falling		2.8		µs
			Rising		4.5		
	Overload recovery time	Gain = –10			0.2		µs
THD+N	Total harmonic distortion + noise	V_O = 5 V_{PP}, gain = +1, f = 1 kHz, R_L = 2 kΩ			0.0004		%
OUTPUT							
	Voltage output swing from rail	A_{OL} > 126 dB	R_L = 10 kΩ	(V–) + 0.2		(V+) + 0.2	V
			R_L = 2 kΩ	(V–) + 0.35		(V+) + 0.35	
		T_A = –40°C to +125°C, R_L = 10 kΩ		(V–) + 0.2		(V+) + 0.2	
I_{SC}	Short-circuit current				±25		mA
C_{LOAD}	Capacitive load drive			See Typical Characteristics			
R_O	Open-loop output impedance			See Typical Characteristics			
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 mA			220	240	µA
			T_A = –40°C to +125°C			310	

5.9 Typical Characteristics

at T_A = 25°C, V_S = ±15 V, V_{CM} = V_{OUT} = mid-supply, and R_L = 10 kΩ (unless otherwise noted)

Table 5-1. Table of Graphs

DESCRIPTION	FIGURE
Offset Voltage Production Distribution at 25°C	Figure 5-1
Offset Voltage Distribution at 125°C	Figure 5-2
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5.9 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, V_{CM} = V_{OUT} = mid-supply, and R_L = 10 kΩ (unless otherwise noted)

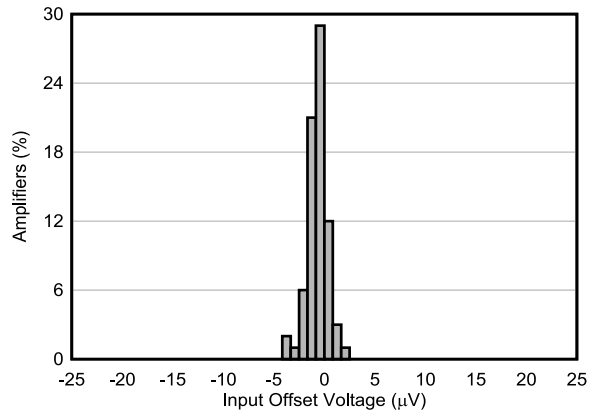


Figure 5-1. Offset Voltage Production Distribution

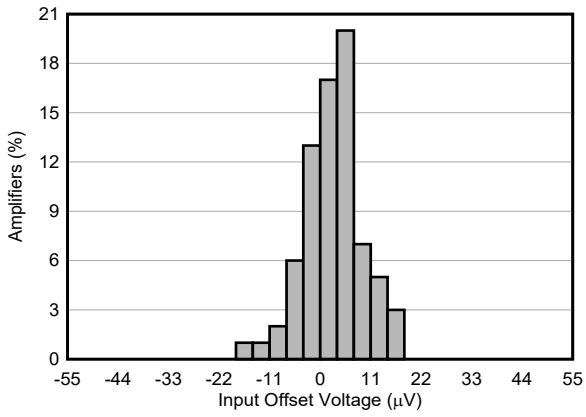


Figure 5-2. Offset Voltage Distribution

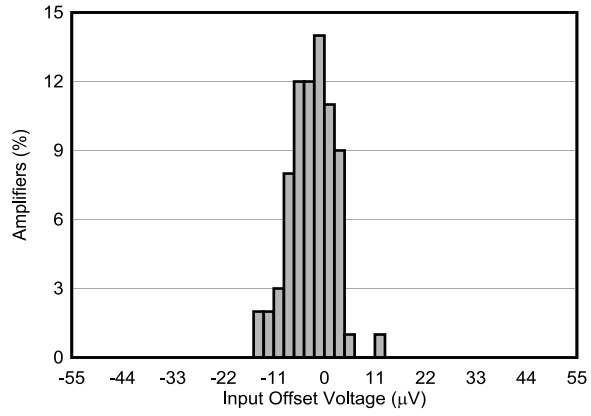


Figure 5-3. Offset Voltage Distribution

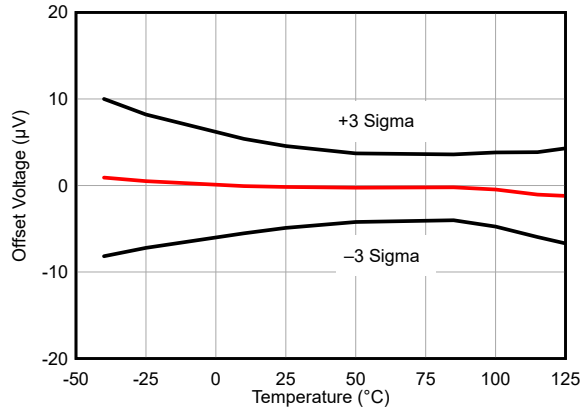


Figure 5-4. Offset Voltage vs Temperature

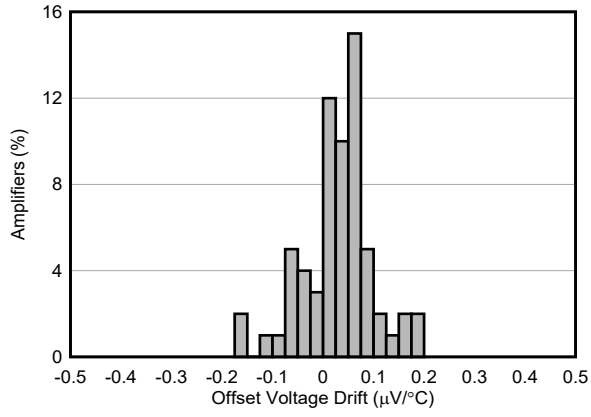


Figure 5-5. Offset Voltage Drift Production Distribution

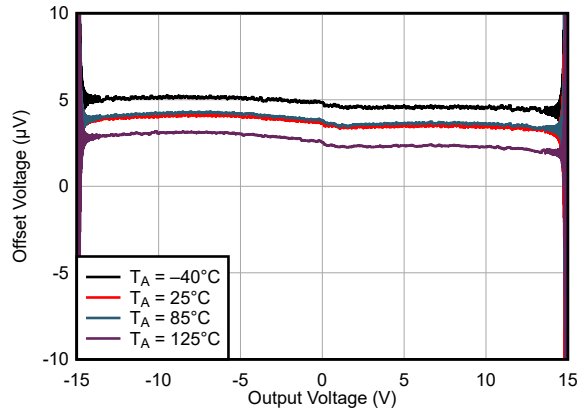


Figure 5-6. Offset Voltage vs Output Voltage

5.9 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, V_{CM} = V_{OUT} = mid-supply, and R_L = 10 kΩ (unless otherwise noted)

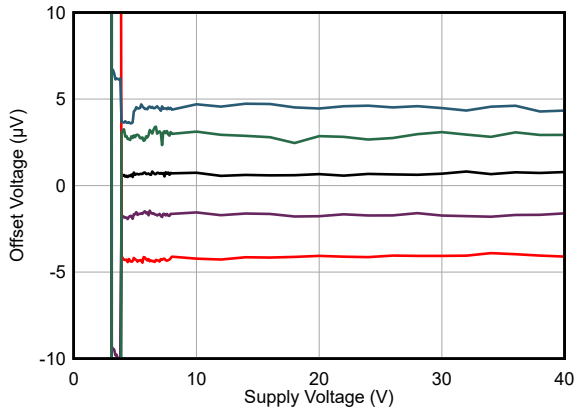


Figure 5-7. Offset Voltage vs Power Supply Voltage

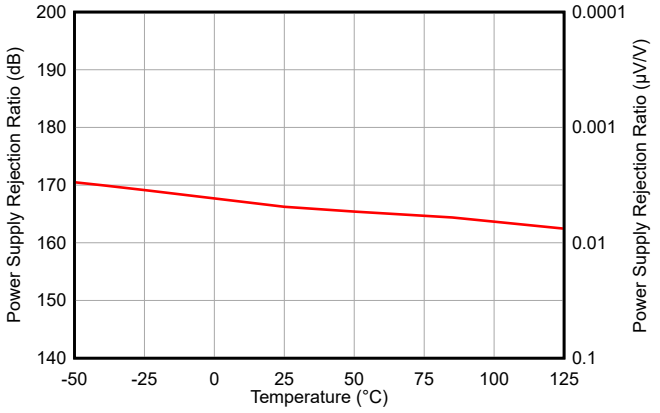


Figure 5-8. Power-Supply Rejection Ratio vs Temperature

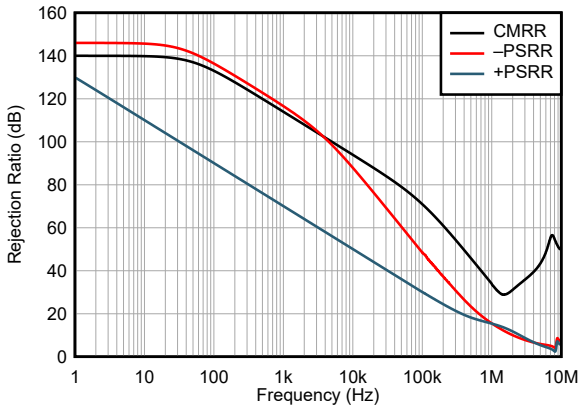


Figure 5-9. Power-Supply and Common-Mode Rejection Ratio vs Frequency

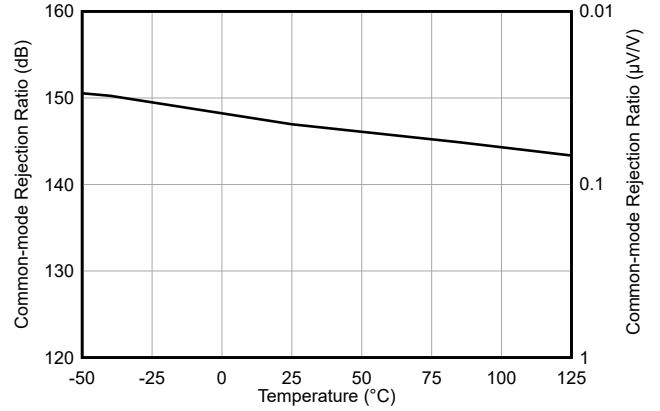


Figure 5-10. Common-Mode Rejection Ratio vs Temperature

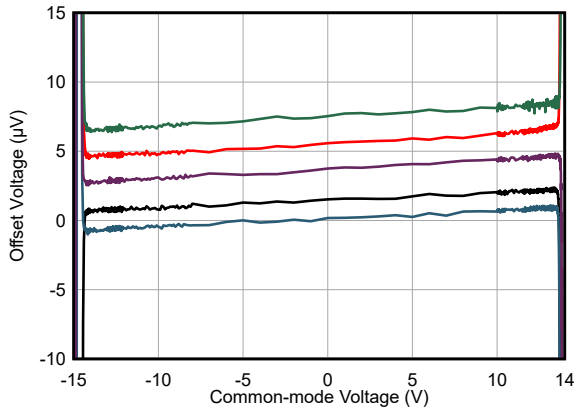


Figure 5-11. Offset Voltage vs Common-Mode Voltage

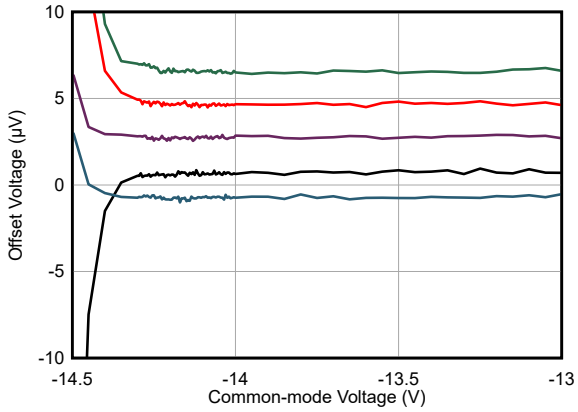


Figure 5-12. Offset Voltage vs V_{CM} at Low Supply

5.9 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, V_{CM} = V_{OUT} = mid-supply, and R_L = 10 kΩ (unless otherwise noted)

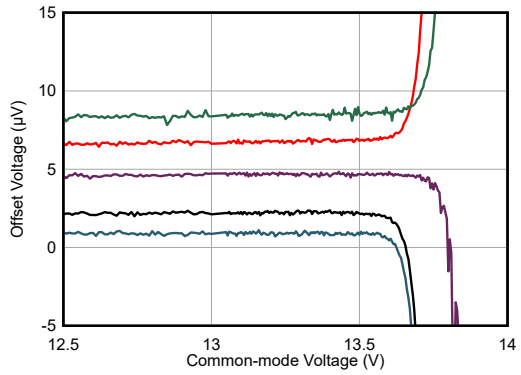


Figure 5-13. Offset Voltage vs V_{CM} at High Supply

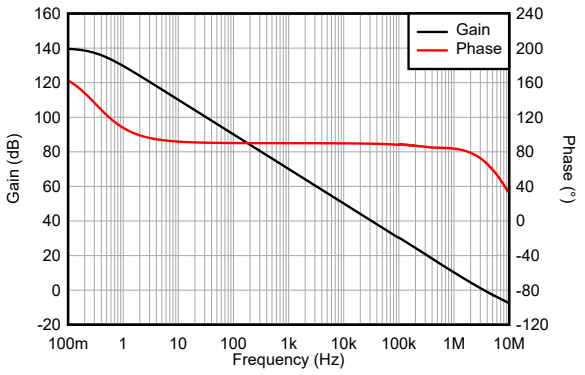


Figure 5-14. Open-Loop Gain and Phase vs Frequency

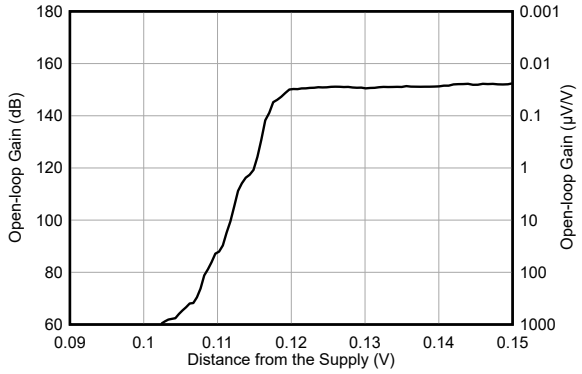


Figure 5-15. Open-Loop Gain vs Distance From Supply

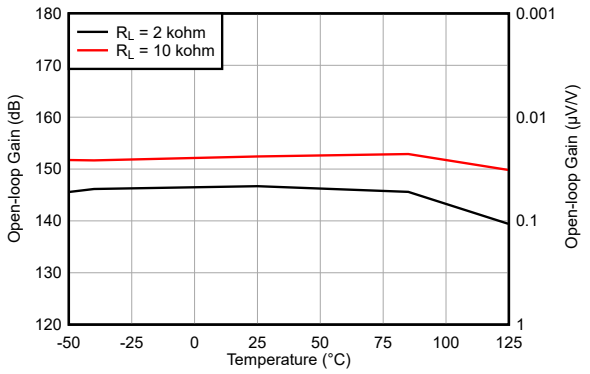


Figure 5-16. Open-Loop Gain vs Temperature

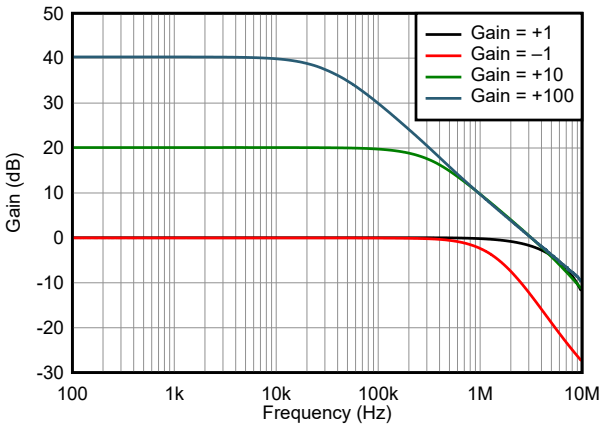


Figure 5-17. Closed-Loop Gain vs Frequency

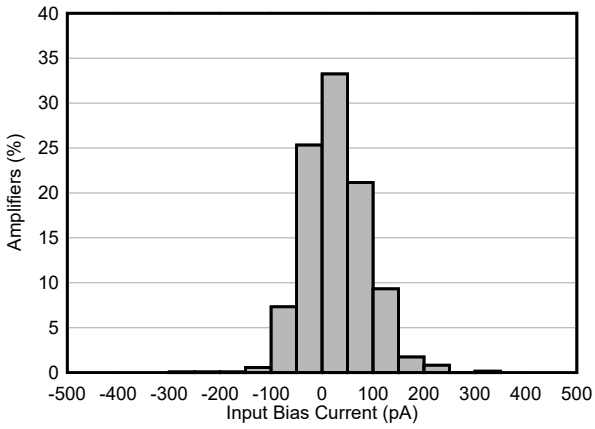


Figure 5-18. Input Bias Production Distribution

5.9 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, V_{CM} = V_{OUT} = mid-supply, and R_L = 10 kΩ (unless otherwise noted)

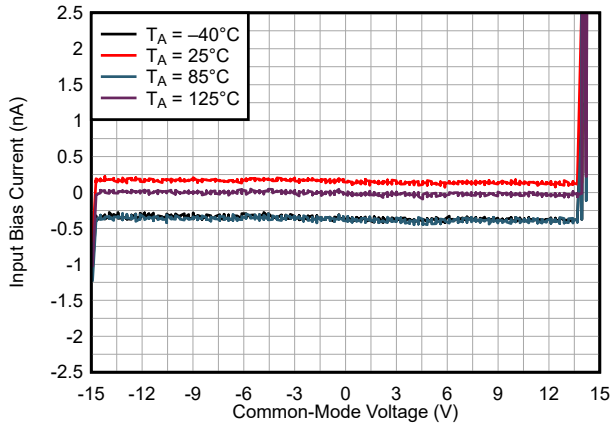


Figure 5-19. Input Bias vs Common-Mode Voltage

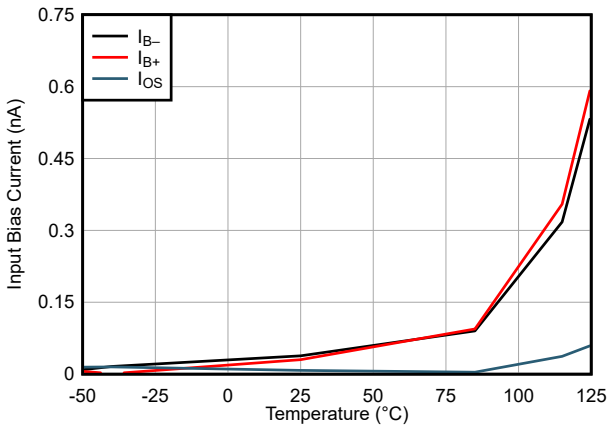


Figure 5-20. Input Bias and Input Offset Current vs Temperature

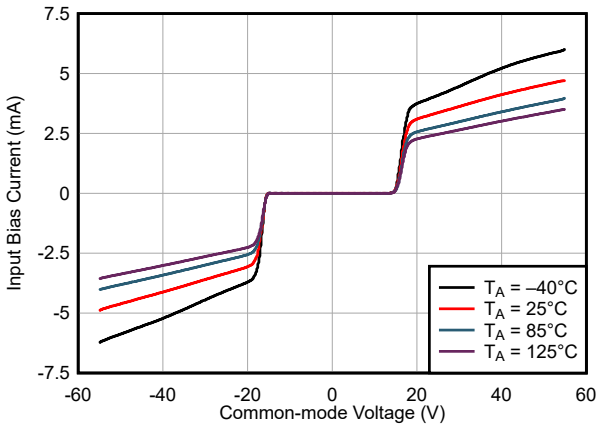


Figure 5-21. Input Bias vs Overvoltage-Protected Common-Mode Range

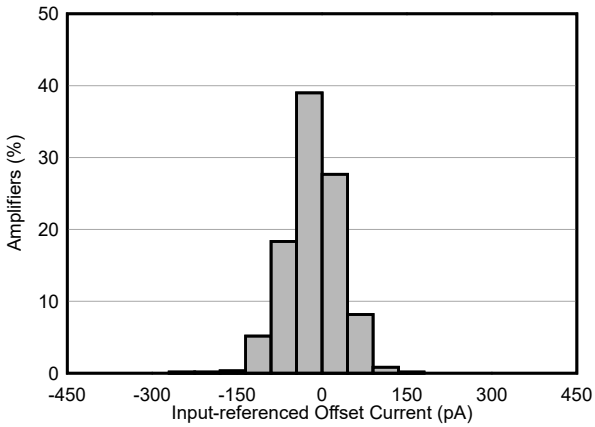


Figure 5-22. Input Offset Current Production Distribution

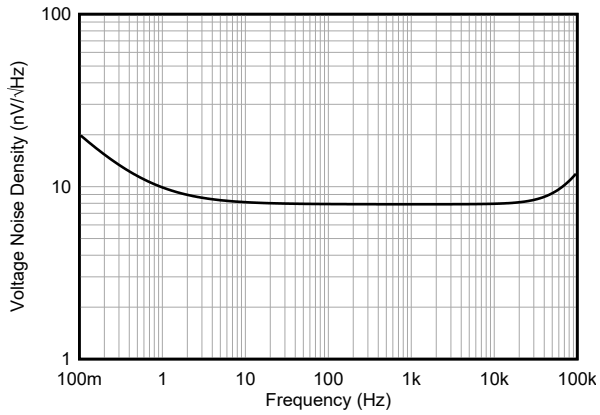


Figure 5-23. Voltage Noise Density vs Frequency

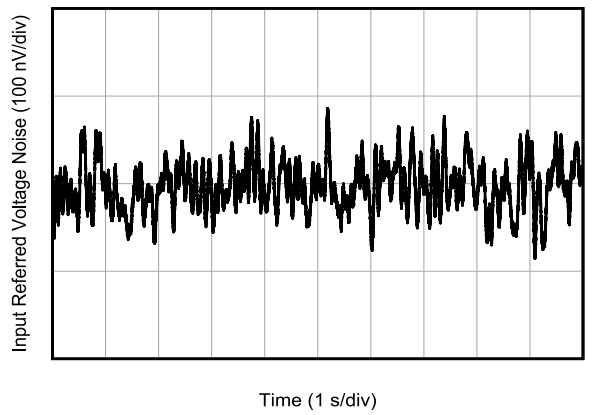


Figure 5-24. 0.1-Hz to 10-Hz Noise

5.9 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, V_{CM} = V_{OUT} = mid-supply, and R_L = 10 kΩ (unless otherwise noted)

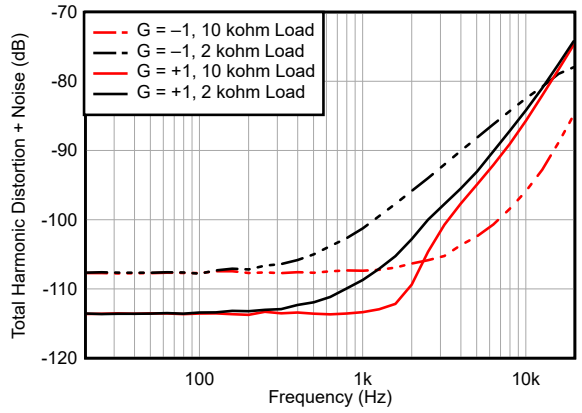


Figure 5-25. Total Harmonic Distortion + Noise Ratio vs Frequency

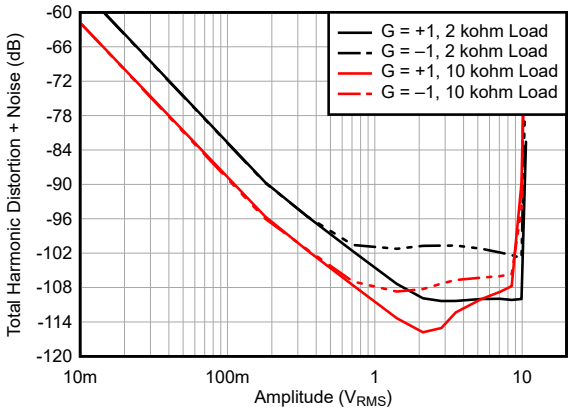


Figure 5-26. Total Harmonic Distortion + Noise Ratio vs Output Amplitude

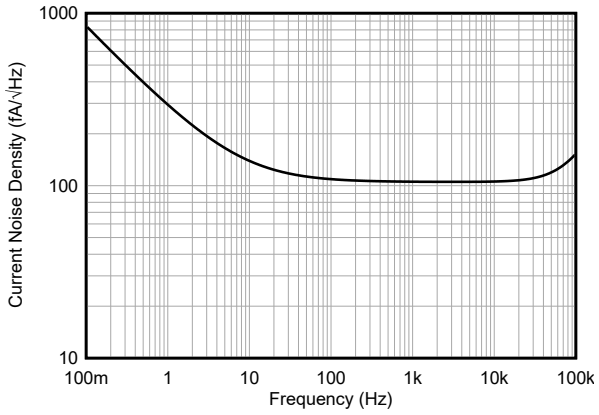


Figure 5-27. Current Noise vs Frequency

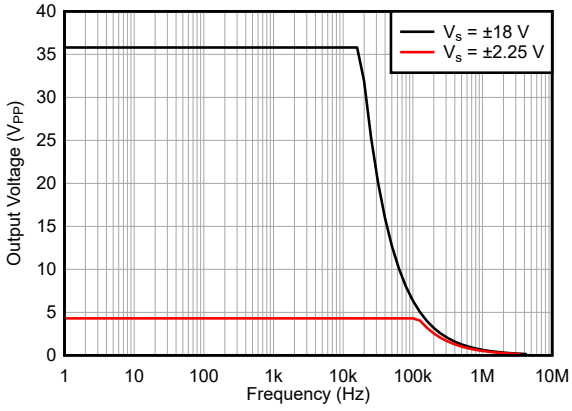


Figure 5-28. Maximum Output Voltage vs Frequency

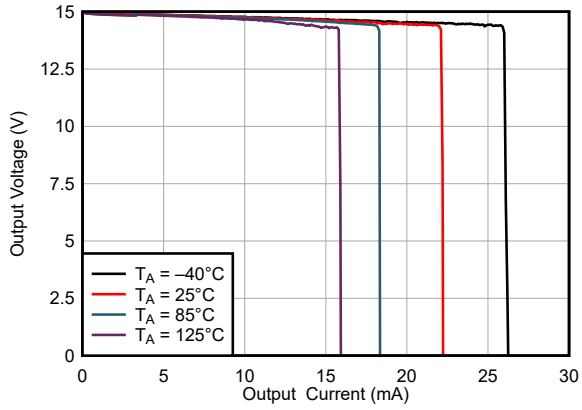


Figure 5-29. Output Voltage Swing vs Output Sourcing Current

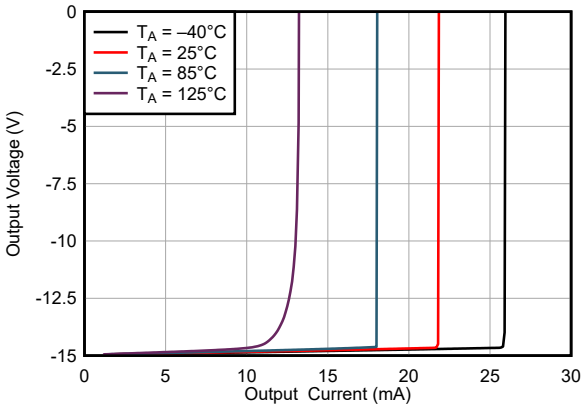


Figure 5-30. Output Voltage Swing vs Output Sinking Current

5.9 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, V_{CM} = V_{OUT} = mid-supply, and R_L = 10 kΩ (unless otherwise noted)

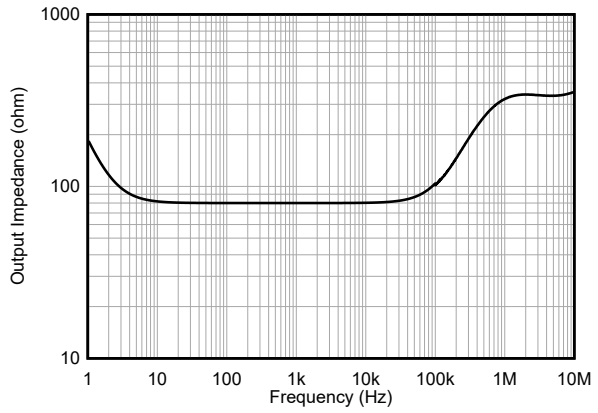


Figure 5-31. Open-Loop Output Impedance vs Frequency

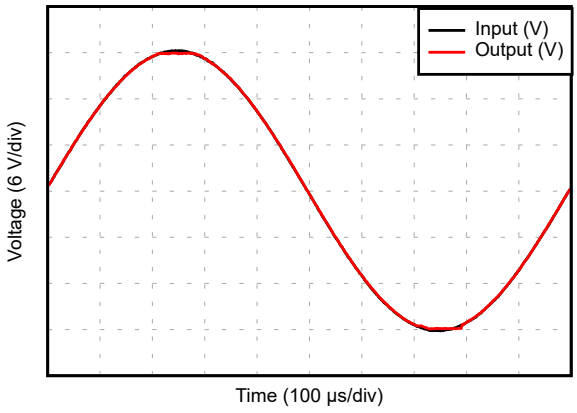


Figure 5-32. No Phase Reversal

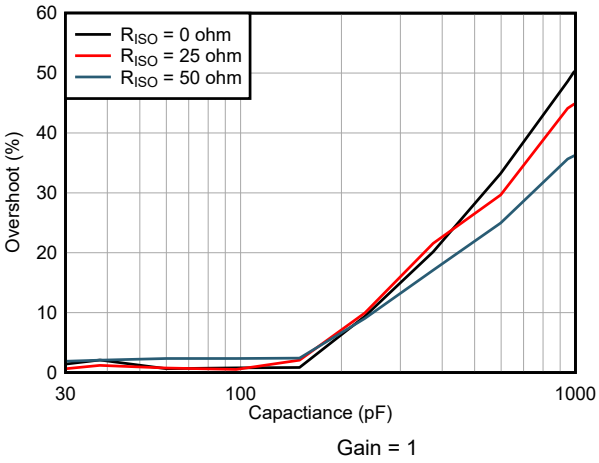


Figure 5-33. Small-Signal Overshoot vs Capacitive Load

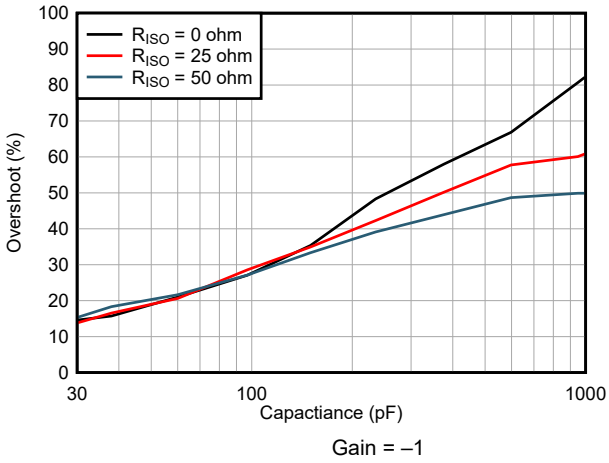


Figure 5-34. Small-Signal Overshoot vs Capacitive Load

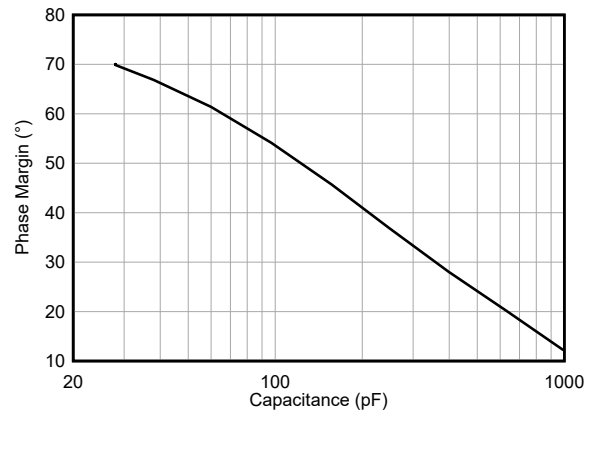


Figure 5-35. Phase Margin vs Capacitive Load

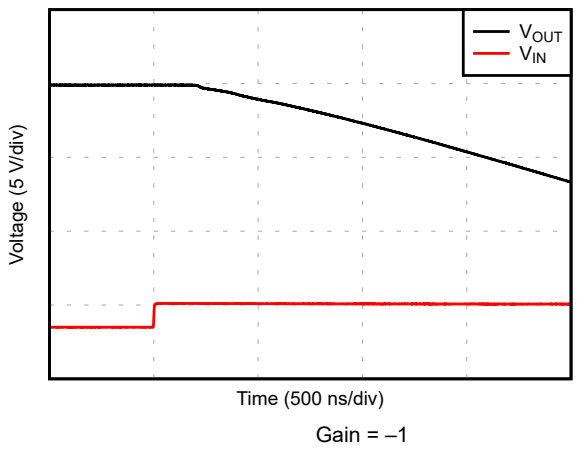


Figure 5-36. Positive Overload Recovery

5.9 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, V_{CM} = V_{OUT} = mid-supply, and R_L = 10 kΩ (unless otherwise noted)

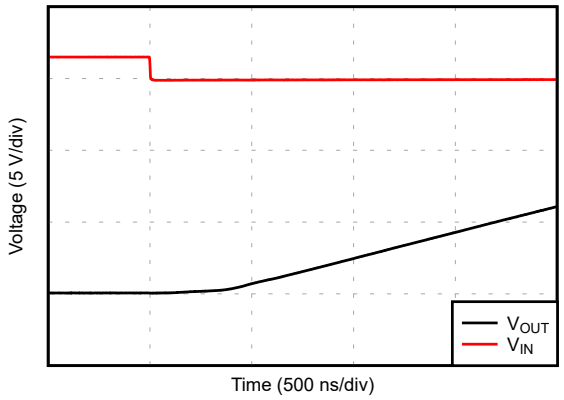


Figure 5-37. Negative Overload Recovery

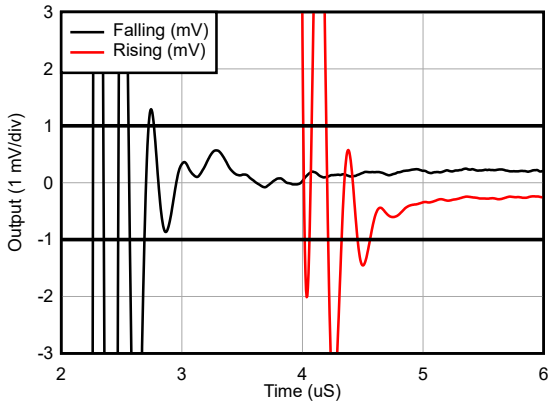


Figure 5-38. Settling Time

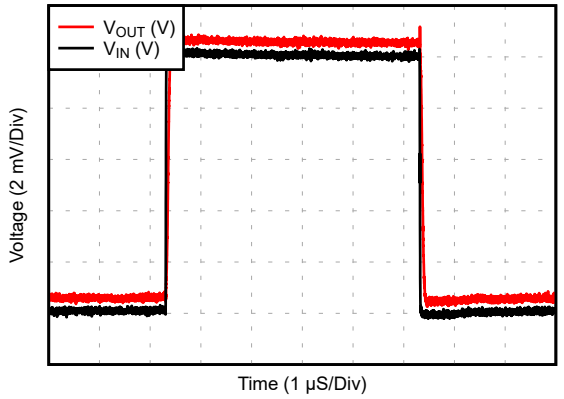


Figure 5-39. Small-Signal Step Response

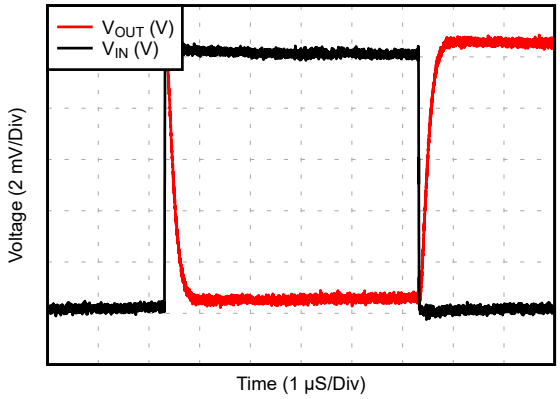


Figure 5-40. Small-Signal Step Response

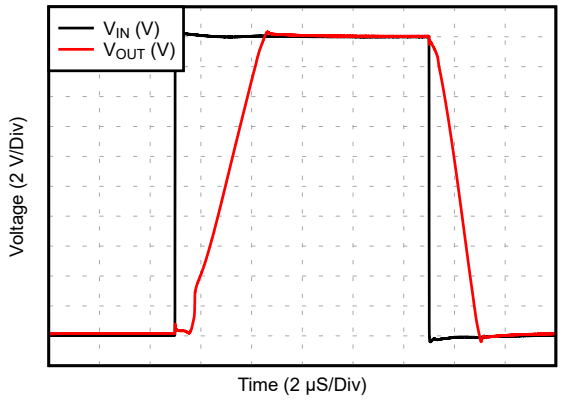


Figure 5-41. Large-Signal Step Response

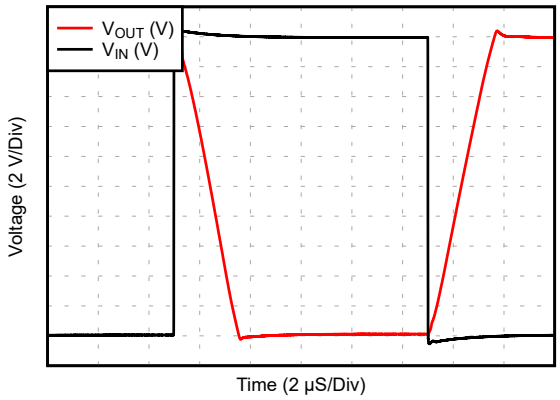


Figure 5-42. Large-Signal Step Response

5.9 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, V_{CM} = V_{OUT} = mid-supply, and R_L = 10 kΩ (unless otherwise noted)

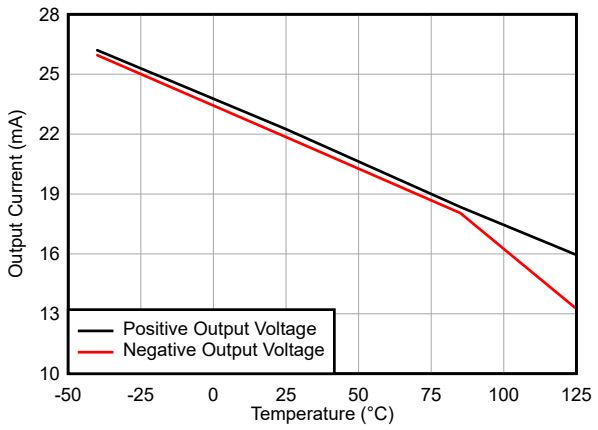


Figure 5-43. Short-Circuit Current vs Temperature

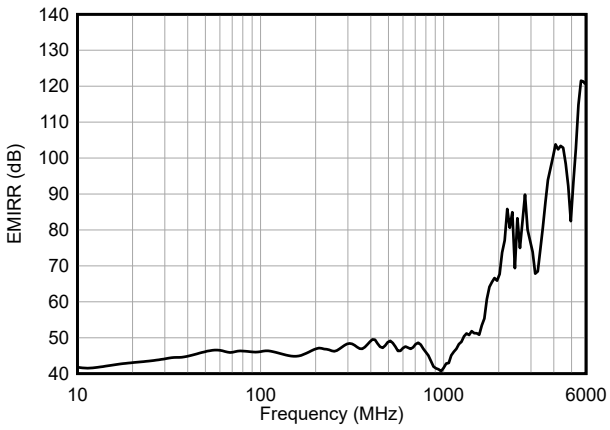


Figure 5-44. Electromagnetic Interference Rejection (EMIRR)

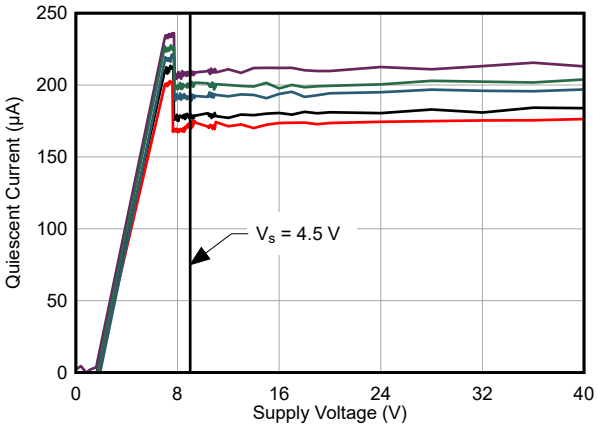


Figure 5-45. Quiescent Current vs Supply Voltage

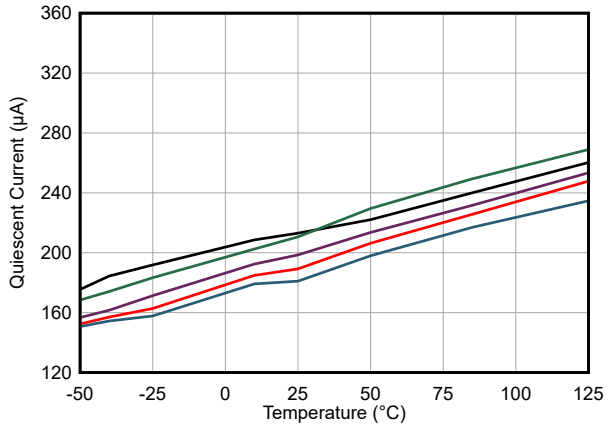


Figure 5-46. Quiescent Current vs Temperature

6 Parameter Measurement Information

6.1 Typical Specifications and Distributions

Designers often have questions about a typical specification of an amplifier to design a more robust circuit. As a result of natural variations in process technology and manufacturing procedures, every specification of an amplifier exhibits some amount of deviation from the ideal value, such as the input bias current of an amplifier. These deviations often follow *Gaussian* (bell curve), or *normal* distributions. Circuit designers can leverage this information to guard band their system, even when there is no minimum or maximum specification in the *Electrical Characteristics*.

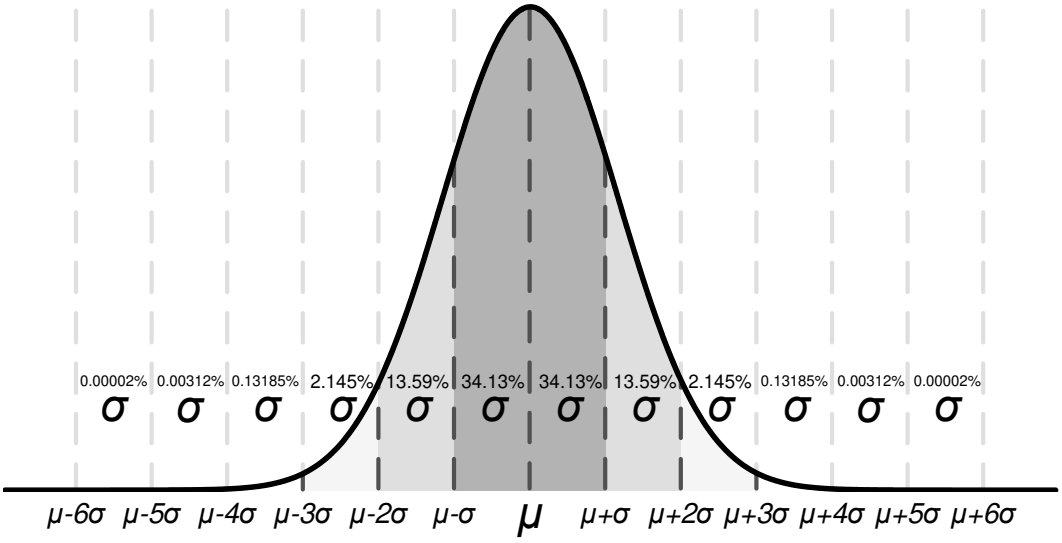


Figure 6-1. Ideal Gaussian Distribution

Figure 6-1 shows an example distribution, where μ, is the mean of the distribution, and where σ, or *sigma*, is the standard deviation of a system. For a specification that exhibits this kind of distribution, approximately two-thirds (68.26%) of all units can be expected to have a value within one standard deviation, or one sigma, of the mean (from $\mu - \sigma$ to $\mu + \sigma$).

Depending on the specification, values listed in the *typical* column of *Electrical Characteristics* are represented in different ways. As a general guideline, if a specification naturally has a nonzero mean (for example, gain bandwidth), then the typical value is equal to the mean (μ). However, if a specification naturally has a mean near zero (for example, input bias current), then the typical value is equal to the mean plus one standard deviation (μ + σ) to most accurately represent the typical value.

Use this chart to calculate the approximate probability of a specification in a unit. For example, the OPAx206 typical input bias current is ±0.1 nA; therefore, 68.2% of all devices are expected to have an input bias from ±0.1 nA. At 4σ, 99.9937% of the distribution has an input bias less than ±0.28 nA, which means that 0.0063% of the population is outside of these limits, and corresponds to approximately 1 in 15,873 units.

Units that are found to exceed any tested minimum or maximum specifications are removed from production material. For example, the OPAx206 have a maximum input bias of ±0.4 nA at 25°C. Although this value corresponds to approximately 6σ (approximately 1 in 500 million units), TI removes any unit with a larger input bias from production material.

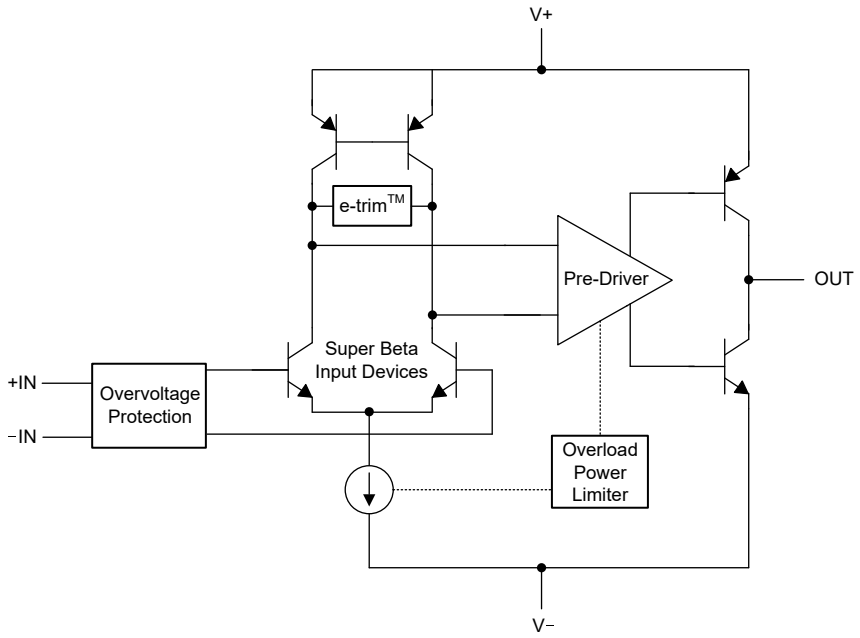
For specifications with no value in the minimum or maximum column, consider selecting a sigma value of sufficient guard band for your application, and design worst-case conditions using this value. Only use this information to estimate the performance of a device.

7 Detailed Description

7.1 Overview

The OPAx206 are the first 36-V, bipolar, e-trim operational amplifiers. These devices use a package-level offset trim to minimize the offset voltage and offset voltage drift introduced during the manufacturing process. This trim is performed after the device is assembled to remove any offset errors introduced throughout the manufacturing process, and trim communication is disabled afterward. The devices feature super-beta inputs that decrease the input bias current and input current noise. The devices also feature input overvoltage protection that protects the device for input voltages up to ±40 V beyond either supply rail.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Overvoltage Protection

The inputs of the OPAx206 are individually protected for voltages up to ±40 V beyond either supply. For example, a common-mode voltage anywhere between –55 V and +55 V does not cause damage when powered from ±15-V supplies. Internal circuitry on each input provides low series impedance under normal signal conditions thus maintaining high performance under normal operating conditions. If the input is overloaded, the protection circuitry limits the input current to a value of approximately 4.8 mA.

During an input overvoltage condition, current flows through the input protection diodes into the power supplies, as shown in Figure 7-1. If the power supplies are unable to sink current, then Zener diode clamps (ZD1 and ZD2) must be placed on the power supplies to provide a current pathway to ground. Figure 7-2 shows that during an overvoltage condition, the input bias current of the inputs increase.

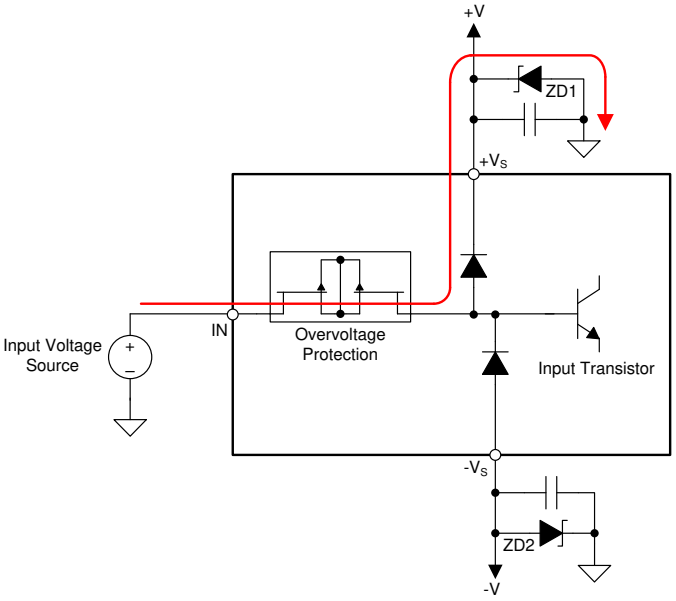
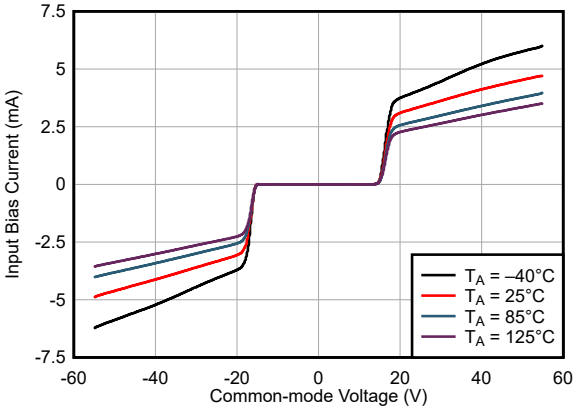


Figure 7-1. OPAx206 Input Overvoltage Current Path

Figure 7-2 shows the input current for input voltages from –55 V to +55 V when the OPAx206 are powered by ±15-V supplies.



V_S = ±15 V

Figure 7-2. OPAx206 Input Current vs Input Voltage (V_S = ±15 V)

7.3.2 Input Offset Trimming

The OPAx206 are the industry's first e-trim operational amplifiers built on a bipolar process. The input offset voltage of an amplifier is determined by the inherent mismatch between the input transistors. The offset can be minimized using laser-trimming performed during the manufacturing process while the device is still in the bare silicon form. However, when the silicon is packaged, the packaging process introduces additional offset due to mechanic stresses. TI's new trimming processes are used to trim the offset after the packaging process is complete to minimize both inherent and package-induced offsets. After trimming, communication is disabled to make sure the amplifier operates properly in the final system.

A comparison between production offset values for a the industry popular, laser-trimmed OPA2277 amplifier and the OPAx206 proprietary trim can be seen in Figure 7-3 and Figure 7-4.

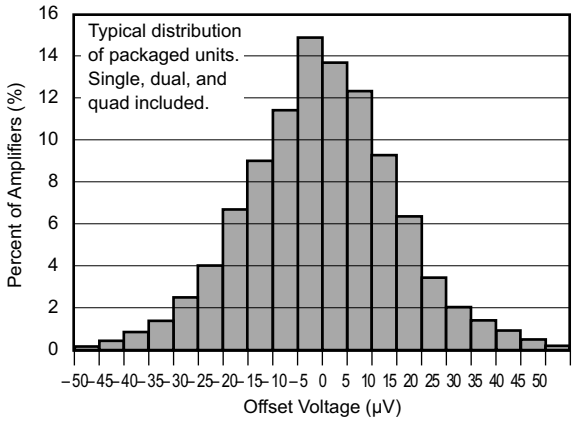


Figure 7-3. OPA2277 Laser-Trimmed Operational Amplifier Offset

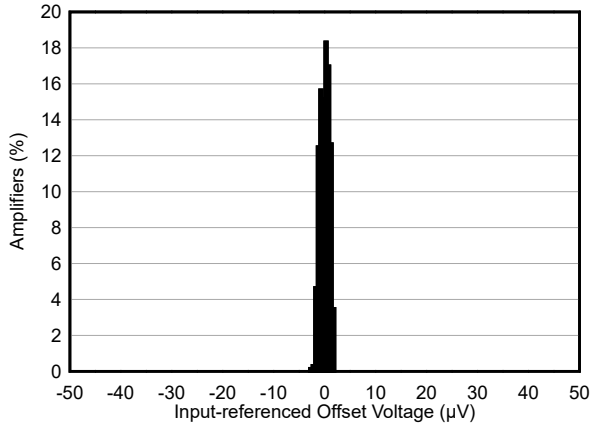


Figure 7-4. OPAx206 e-trim™ Operational Amplifier Offset

The OPAx206 also features exceptional input offset voltage drift over temperature. Figure 7-5 shows the final performance of the offset drift.

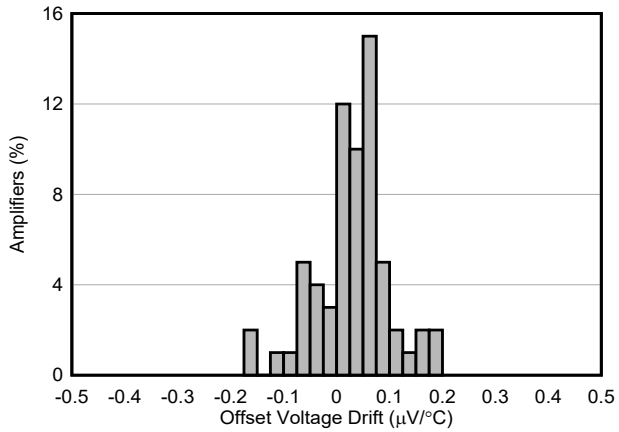


Figure 7-5. OPAx206 e-trim™ Operational Amplifier Drift

7.3.3 Lower Input Bias With Super-Beta Inputs

The OPAx206 have a super-beta input transistor architecture. In a transistor, the beta value is the ratio between the current flowing into the base and the current flowing from the collector to the emitter. A super-beta transistor is one where the beta value has been increased from several hundred to thousands. In a bipolar amplifier, the input bias current is the current flowing into the base of the input transistor pair, as well as a small leakage current that flows through the ESD diodes. A super-beta input reduces the input bias current of the amplifier. In addition, the super-beta inputs lower the input current noise that is directly related to the input bias current of the device. A comparison between the input bias current of the OPA2277 and the OPAx206 super-beta input bias currents can be seen in Figure 7-6 and Figure 7-7.

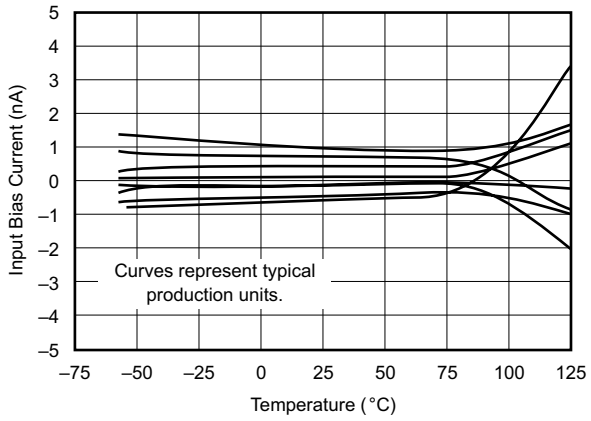


Figure 7-6. OPA2277 Input Bias Current

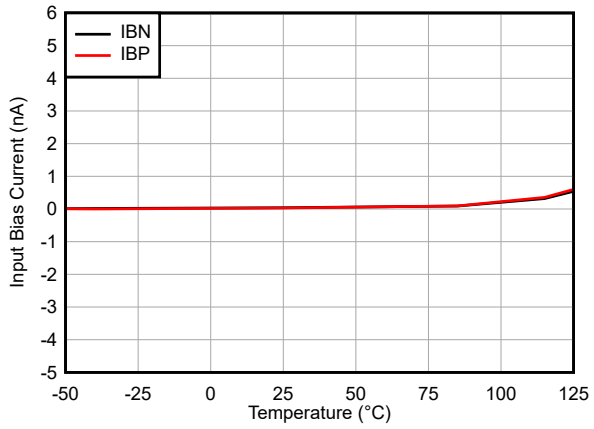


Figure 7-7. OPAx206 Super-Beta Input Bias Current

7.3.4 Overload Power Limiter

In many bipolar-based amplifiers, the output stage of the amplifier can draw significant (several milliamperes) of quiescent current if the output voltage becomes clipped (meaning the output voltage becomes limited by the negative or positive supply voltage). This condition can cause the system to enter a high-power consumption state, and potentially cause oscillations between the power supply and signal chain. The OPAx206 have an advanced output stage design that eliminates this problem. When the output voltage reaches the either supply (V+ or V–), there is virtually no additional current consumption from the nominal quiescent current. This feature helps eliminate any potential system problems when the signal chain is disrupted by a large external transient voltage.

7.3.5 EMI Rejection

The OPAx206 use integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources, such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved through circuit design techniques that improve the system performance. Additional information can be found in the *EMI Rejection Ratio of Operation Amplifiers* application report.

7.4 Device Functional Modes

The OPAx206 have two functional modes. The devices enter normal operation with any supply between 4.5 V (±2.25 V) and 36 V (±18 V), and an input voltage that meets the input common-mode voltage range shown in *Section 5*.

If the input voltage exceeds device specifications, the devices enter an overvoltage protection mode. In this mode, the input overvoltage protection subcircuit limits the voltage and current seen by the amplifier core by adding additional impedance between the input pins and the amplifier core. Figure 7-1 shows how additional current that is generated from the voltage drop across this input impedance is routed through the ESD structure of the OPAx206.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The OPAx206 are unity-gain stable operational amplifiers with very low offset voltage, offset voltage drift, voltage noise, current noise, and power consumption. The built-in overvoltage protection allows this device family to protect against signals outside of the expected range, a reverse connection, or in cases where the inputs are shorted to a system supply. These features make these devices a great choice for a variety of space-constrained and power-constrained systems by removing the need for discrete protection such as clamping diodes.

8.2 Typical Applications

8.2.1 Voltage Attenuator

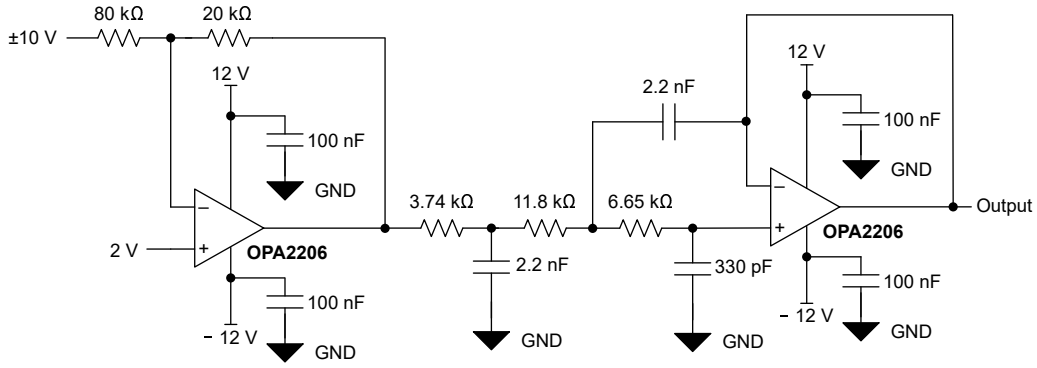


Figure 8-1. OPA2206 Configured as a Voltage Attenuator

8.2.1.1 Design Requirements

The design requirements for this system are:

- Input signal range: ±10 V
- Input signal frequency: up to 10 kHz
- 3rd-order Butterworth filter -3-dB frequency: 20 kHz
- Output voltage: 0 V to 5 V
- Input protection: up to ±52 V

8.2.1.2 Detailed Design Procedure

In this design, a ±10-V, 10-kHz bandwidth, bipolar signal is attenuated and converted to a single-ended signal and filtered by a 3rd-order Butterworth filter to drive a single-ended analog-to-digital converter (ADC). By using the OPA2206, the input of the signal chain is protected from overvoltages up to 40 V beyond either supply. This signal-chain design is common for programmable logic controllers (PLCs), low-power data acquisition systems (DAQs) and field instruments where high precision, low power and signal fault protection are needed.

The OPA2206 was selected for this application because of the high supply range, high dc precision (4-µV offset and 0.08-µV/°C offset drift), and low power consumption (220-µA quiescent current) that minimizes thermal dissipation requirements. Because of the internal OVP topology, the device provides better dc and ac accuracy under normal operating conditions compared to passive external protection and results in a smaller system solution. Be sure to connect a zener diode between each supply to ground to provide a return path for the current that is generated during a fault condition.

The first stage of the signal chain is an attenuator and level-shifter. The input signal to this stage is bipolar ±10 V that is attenuated to ±2.5 V, and then level-shifted so that the output is a single-ended, 0-V to 5-V signal. The feedback and gain resistors were selected as 20 kΩ and 80 kΩ, respectively. Thus, the combined impedance is 100 kΩ, which lowers the input current to the signal chain, and minimizes errors resulting from higher output impedance sensors.

The second stage of the signal chain uses the second channel of the OPA2206 to create a 3rd-order Butterworth filter with a –3-dB response of 20 kHz. For more information on filter design, refer to Texas Instrument's filter design tool.

The output of this signal chain is shown in Figure 8-2 and the filter response is shown in Figure 8-3.

8.2.1.3 Application Curves

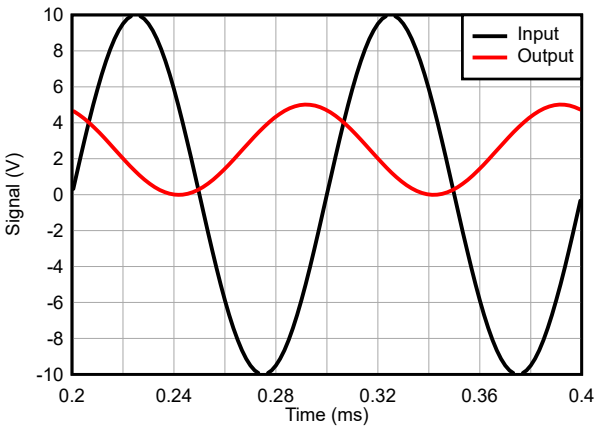


Figure 8-2. Input and Output Signal

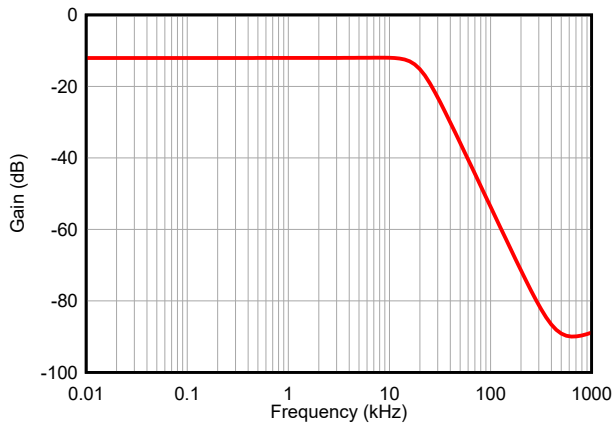


Figure 8-3. Attenuator + Filter Response

8.2.2 Discrete, Two-Op-Amp Instrumentation Amplifier

Figure 8-4 shows the OPA2206 configured as a two op amp, discrete instrumentation amplifier. This configuration allows for a differential signal measurement, such as the signal from a load cell, with higher input impedance to the signal chain than most monolithic instrumentation amplifiers. Additionally, the input overvoltage protection of the OPA2206 protects the signal chain from being damaged by fault conditions where the input signal exceeds the supply voltage of the amplifier.

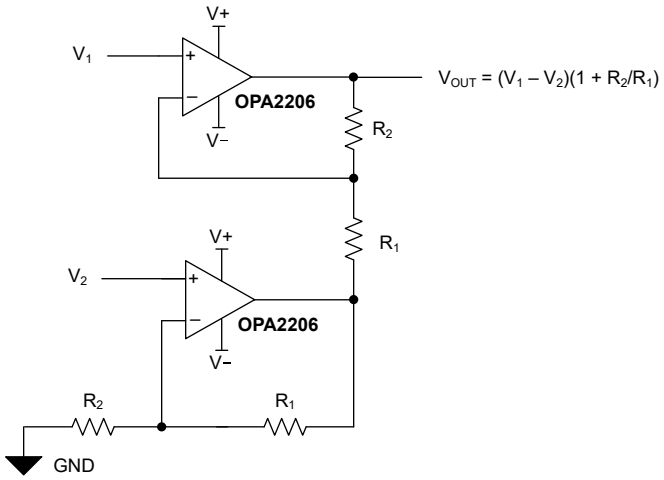


Figure 8-4. OPA2206 Configured as a Two Op Amp, Discrete Instrumentation Amplifier

8.2.3 Input Buffer and Protection for ADC Driver

Section 8.2.1.1 shows the OPA2206 configured as an input buffer for an ADC driver using the THP210. The high dc precision and low noise of the OPA2206 make this device an excellent choice for precision signal chain conditioning. The low input bias of the amplifier minimizes dc errors created for higher output impedance sensors. The integrated input overvoltage protection prevents damage to the signal chain due to an input fault condition where the signal exceeds the supply range of the OPA2206, or if the inputs are shorted to a higher supply rail. For more information on designing a precision ADC driver, see the THP210.

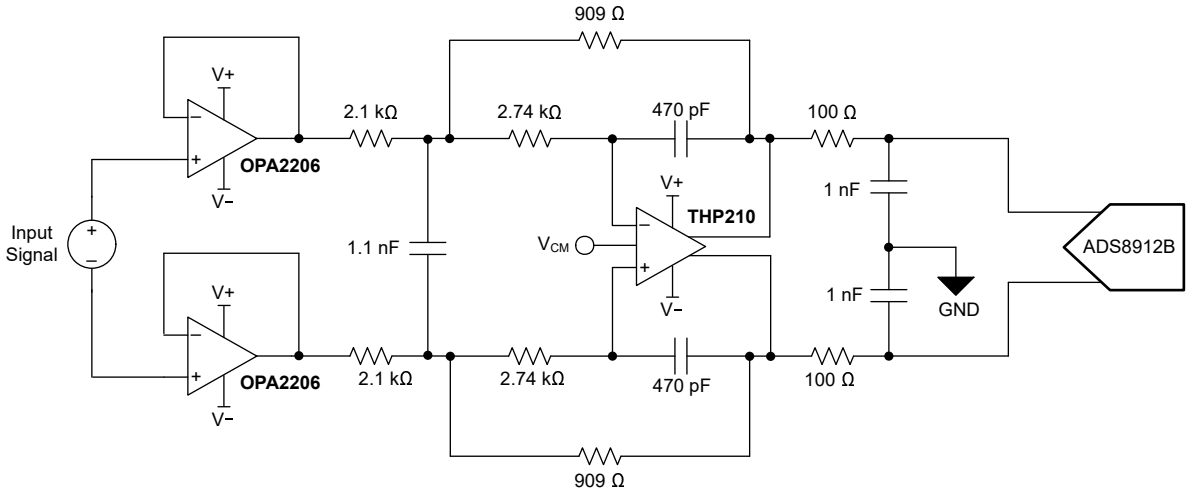


Figure 8-5. OPA2206 Configured as an Input-Signal-Chain Buffer

8.3 Power Supply Recommendations

The OPAx206 operate with a supply between 4.5 V (±2.25 V) and 36 V (±18 V). Parameters that can exhibit significant variance with regard to operating voltages are presented in *Section 5.9*.

8.4 Layout

8.4.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications. Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as through the individual op amp. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
- Make sure to physically separate digital and analog grounds and pay attention to the flow of the ground current. Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better, as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in Figure 8-6, keep RF and RG close to the inverting input to minimize parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Clean the PCB following board assembly for best performance.
- Any precision integrated circuit can experience performance shifts due to moisture ingress into the plastic package. After any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

8.4.2 Layout Example

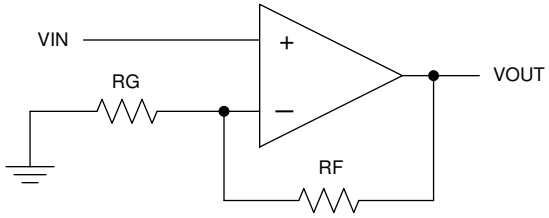


Figure 8-6. Schematic Representation

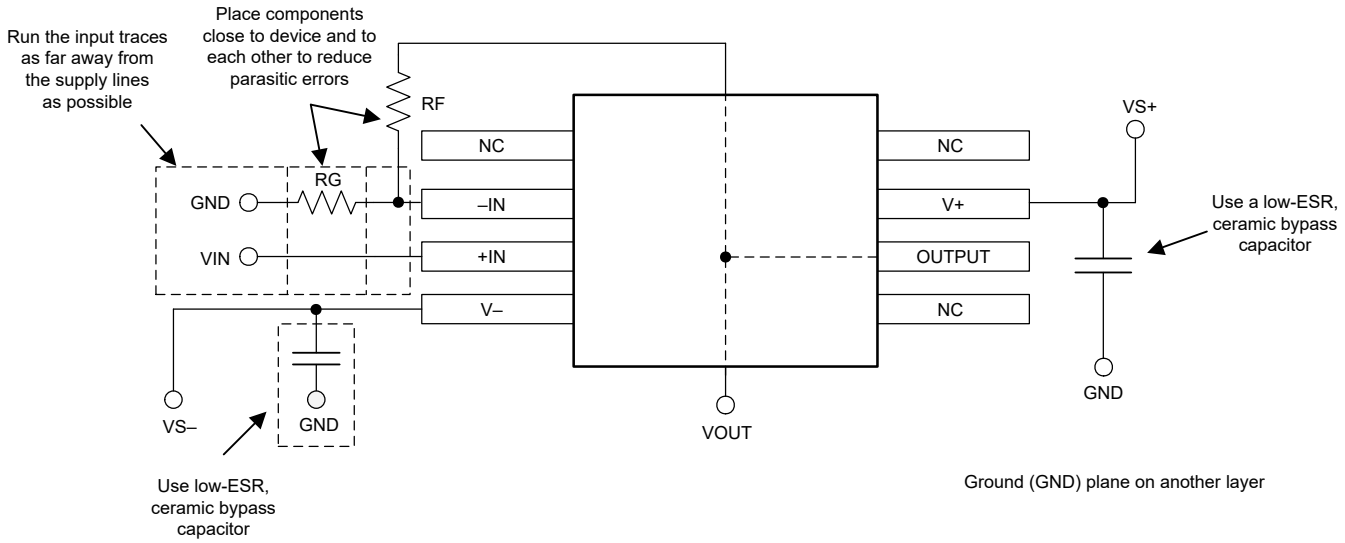


Figure 8-7. Operational Amplifier Board Layout for Noninverting Configuration

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

The following evaluation modules are available:

- DIP-ADAPTER-EVM
- DIYAMP-EVM

9.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *DIP-ADAPTER-EVM* user's guide
- Texas Instruments, *DIYAMP-SOIC-EVM* user's guide

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.5 Trademarks

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PSpice® is a registered trademark of Cadence Design Systems, Inc.
All trademarks are the property of their respective owners.

9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (January 2023) to Revision E (December 2023)	Page
• Added OPA4206 device and associated content	1
• Updated Figure 5-24, *0.1 Hz to 10 Hz Noise*, to more accurately reflect device performance	11

Changes from Revision C (July 2022) to Revision D (January 2023)	Page
• Changed OPA206 in D (SOIC) package from advanced information (preview) to production data (active)	1
• Added OPA2206 in D (SOIC) package and associated content as production data (active)	1
• Changed title to align with updated specifications	1
• Changed offset voltage from 50 µV to 25 µV in *Features*	1
• Changed offset voltage from ±8 µV to ±4 µV in *Description*	1
• Changed input offset voltage maximum value from ±50 µV to ±25 µV in *Electrical Characteristics*	7
• Changed input offset voltage typical value from ±8 µV to ±4 µV in *Electrical Characteristics*	7
• Changed input offset voltage over temperature from ±80 µV to ±55 µV in *Electrical Characteristics*	7
• Changed input offset voltage maximum value from ±50 µV to ±25 µV in *Electrical Characteristics*	9
• Changed input offset voltage typical value from ±8 µV to ±4 µV in *Electrical Characteristics*	9
• Changed input offset voltage over temperature from ±80 µV to ±55 µV in *Electrical Characteristics*	9
• Changed Figures 6-1, 6-2, 6-3, and 6-5 to more accurately show the device performance distributions	11
• Changed input offset drift trimming description text in *Input Offset Trimming*	23
• Changed Figure 8-5 to show the correct input offset drift distribution	23
• Changed offset, offset drift to match standard-grade device specifications in *Detailed Design Description*	25
• Changed Figure 9-7 to show correct VS+ connection	29

Changes from Revision B (August 2021) to Revision C (July 2022)	Page
• Added OPA206 in D (SOIC) package as advanced information (preview)	1

Changes from Revision A (March 2021) to Revision B (August 2021)	Page
• Deleted OPA2206 high-grade version and associated content	1
• Changed quiescent current feature bullet from 220 µA to 240 µA	1
• Changed Figure 6-27, *Current Noise vs Frequency*, to more accurately show the device performance	11

Changes from Revision * (April 2020) to Revision A (March 2021)	Page
• Changed OPA2206 from advanced information (preview) to production data (active)	1
• Changed both *Electrical Characteristics* tables to show differentiated performance between OPA2206 (high grade) and OPA2206A (standard grade)	7

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA206ADR	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP206A
OPA206ADR.Z	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP206A
OPA206ADT	Active	Production	SOIC (D) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP206A
OPA206ADT.Z	Active	Production	SOIC (D) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP206A
OPA2206ADGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	22A6
OPA2206ADGKR.Z	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	22A6
OPA2206ADGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	22A6
OPA2206ADGKT.Z	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	22A6
OPA2206ADR	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2206A
OPA2206ADR.Z	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2206A
OPA2206ADT	Active	Production	SOIC (D) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2206A
OPA2206ADT.Z	Active	Production	SOIC (D) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2206A
OPA4206ADR	Active	Production	SOIC (D) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4206A
OPA4206ADR.Z	Active	Production	SOIC (D) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4206A
OPA4206APWR	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP4206A
OPA4206APWR.Z	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP4206A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

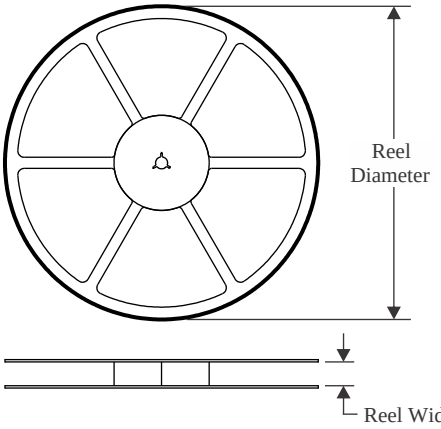
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

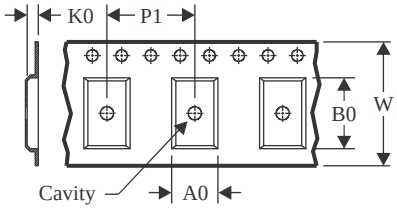
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

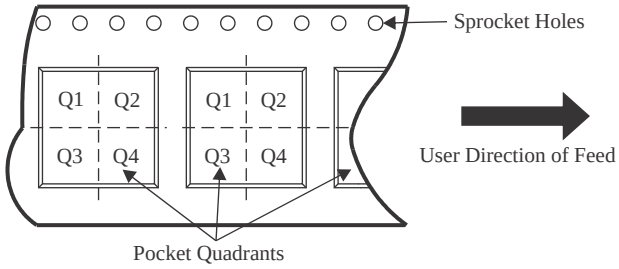


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

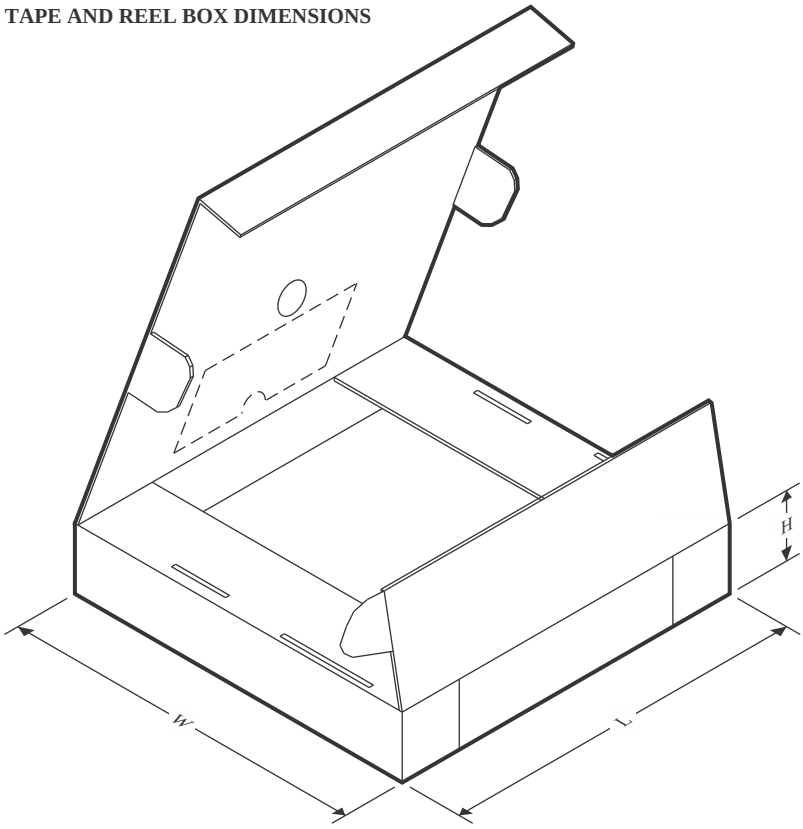
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

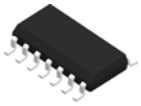
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA206ADR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA206ADT	SOIC	D	8	250	180.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2206ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2206ADGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2206ADR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2206ADT	SOIC	D	8	250	180.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4206ADR	SOIC	D	14	3000	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA206ADR	SOIC	D	8	3000	356.0	356.0	35.0
OPA206ADT	SOIC	D	8	250	210.0	185.0	35.0
OPA2206ADGKR	VSSOP	DGK	8	2500	356.0	356.0	35.0
OPA2206ADGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA2206ADR	SOIC	D	8	3000	356.0	356.0	35.0
OPA2206ADT	SOIC	D	8	250	210.0	185.0	35.0
OPA4206ADR	SOIC	D	14	3000	356.0	356.0	35.0

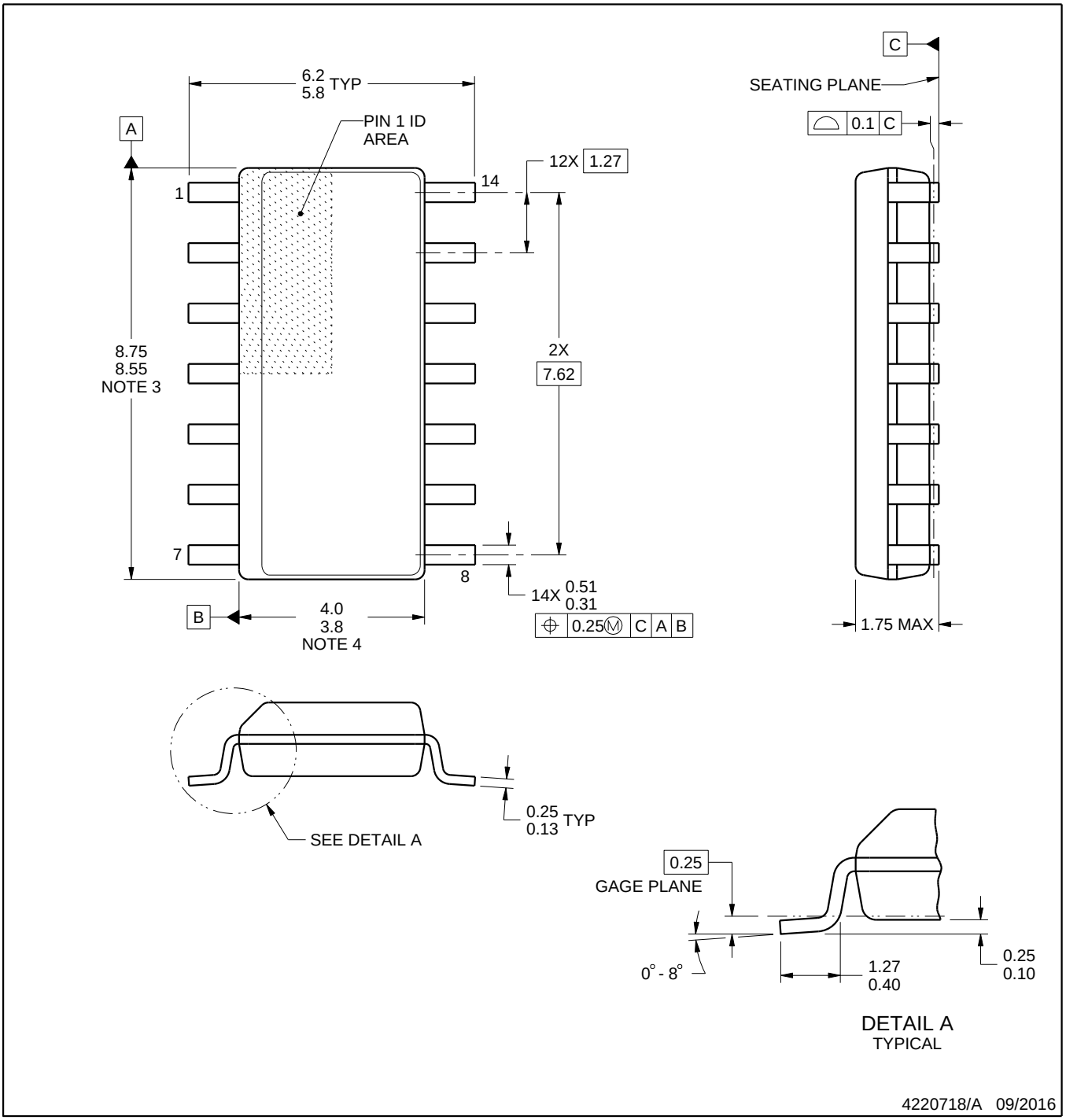


PACKAGE OUTLINE

D0014A

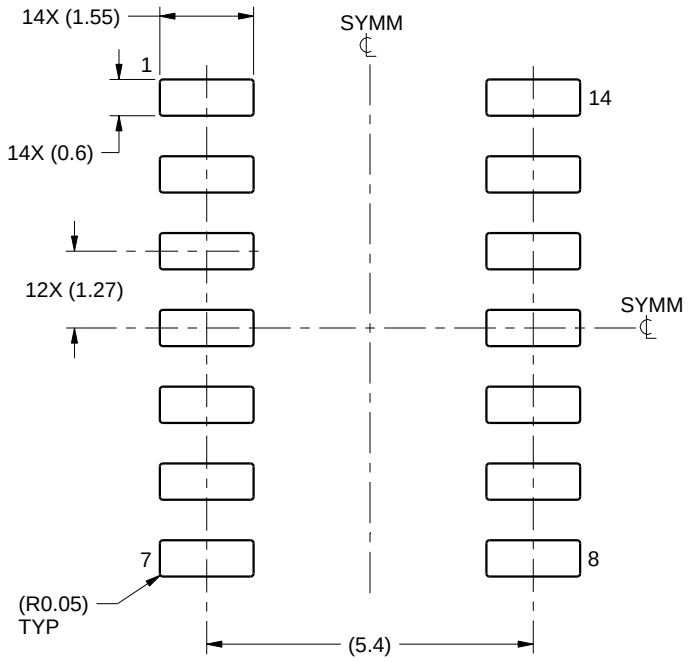
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

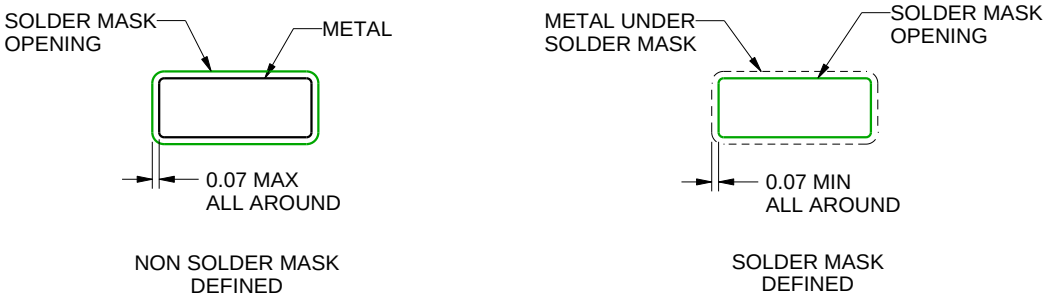


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

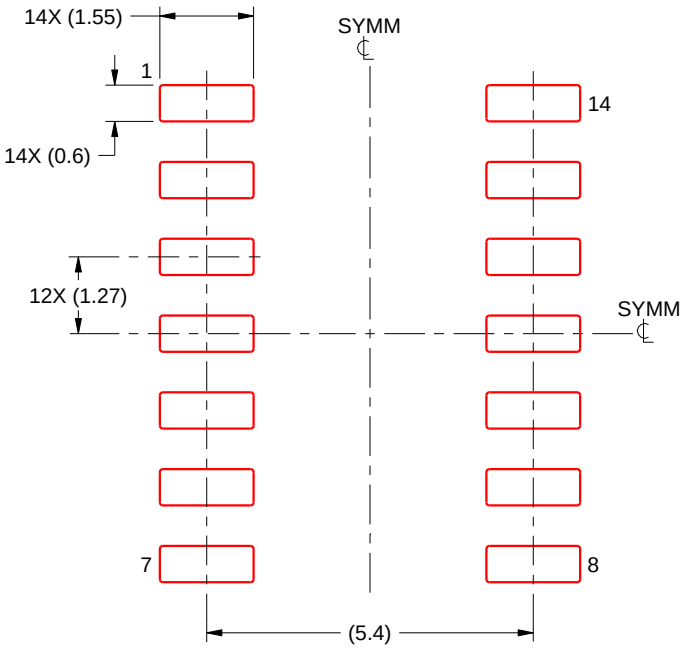
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

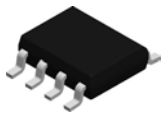


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

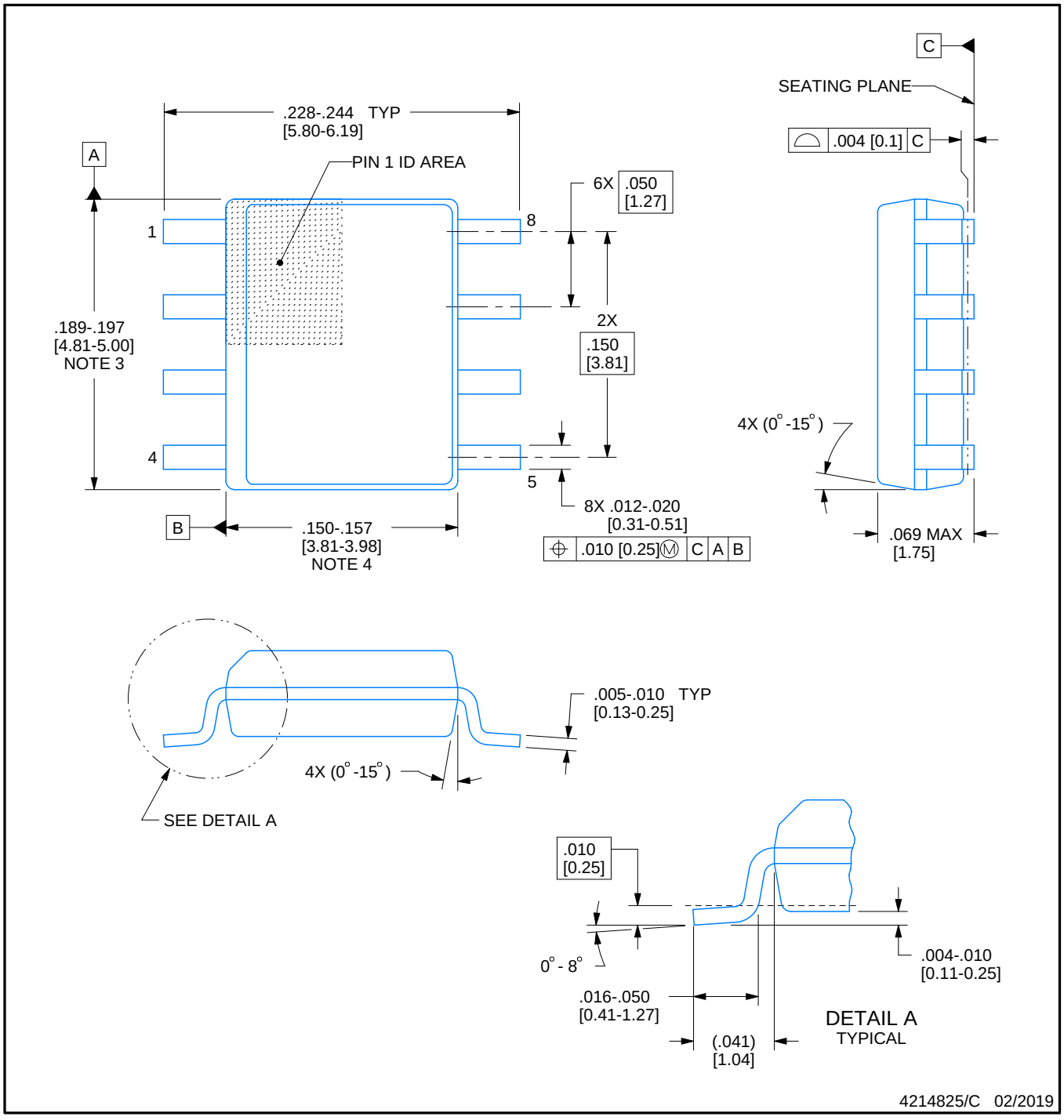


PACKAGE OUTLINE

D0008A

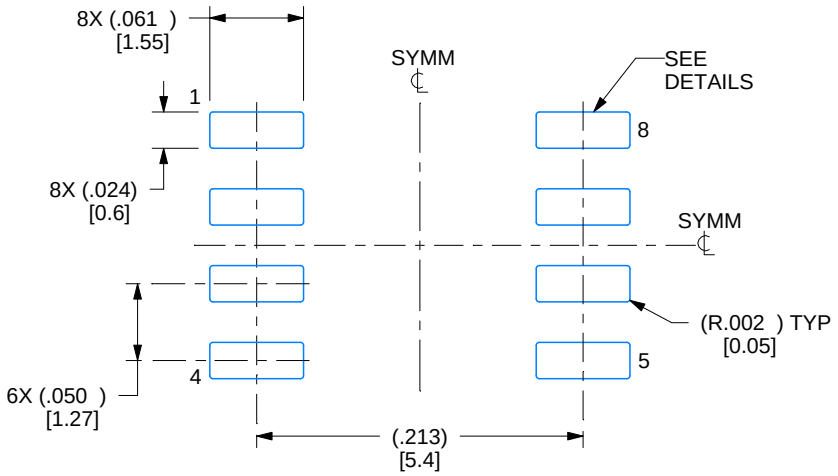
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

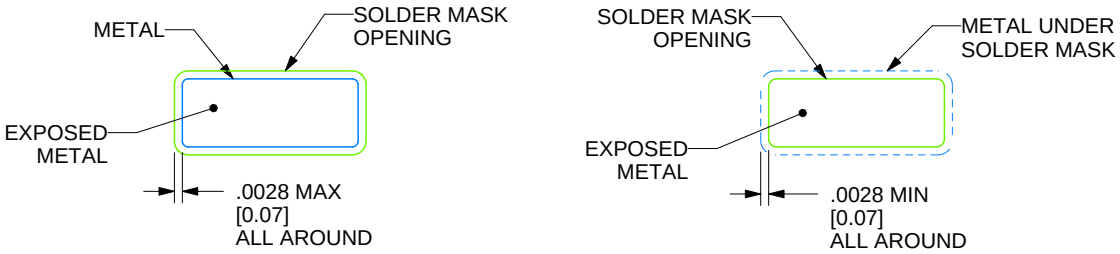


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

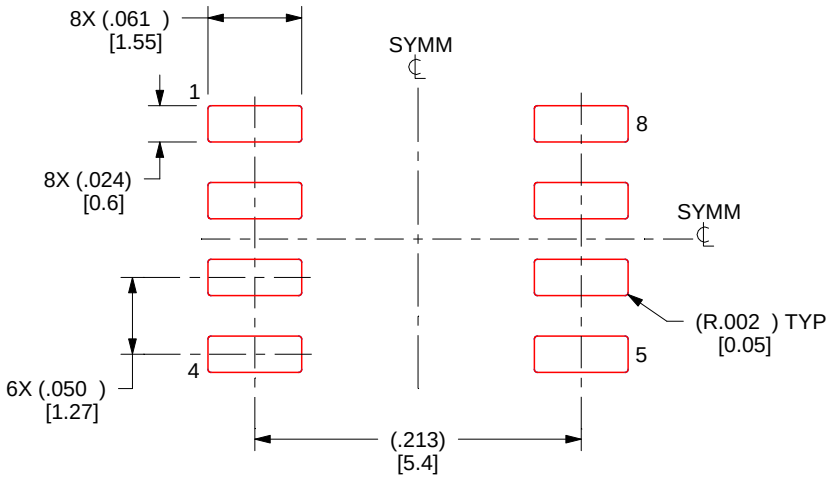
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

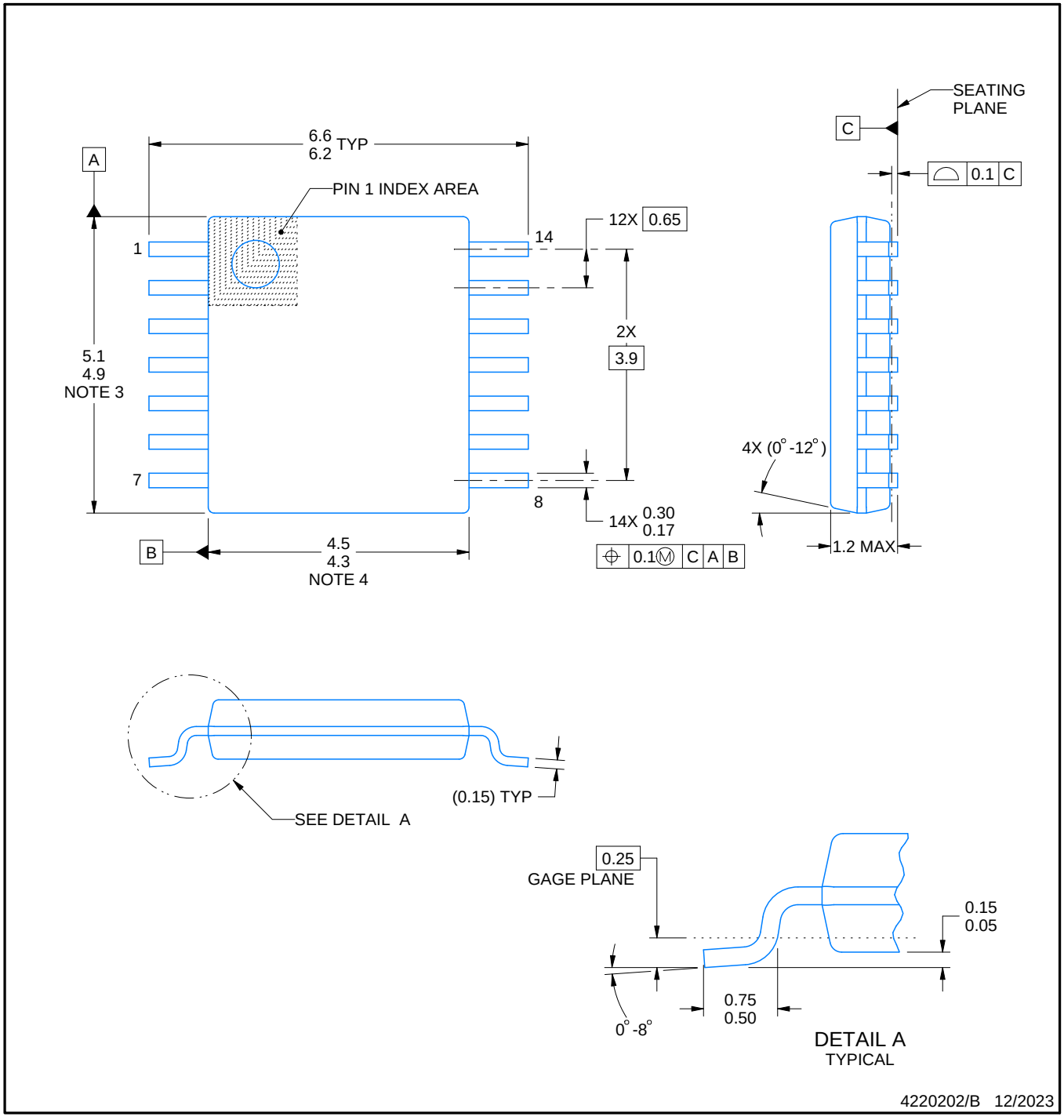
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

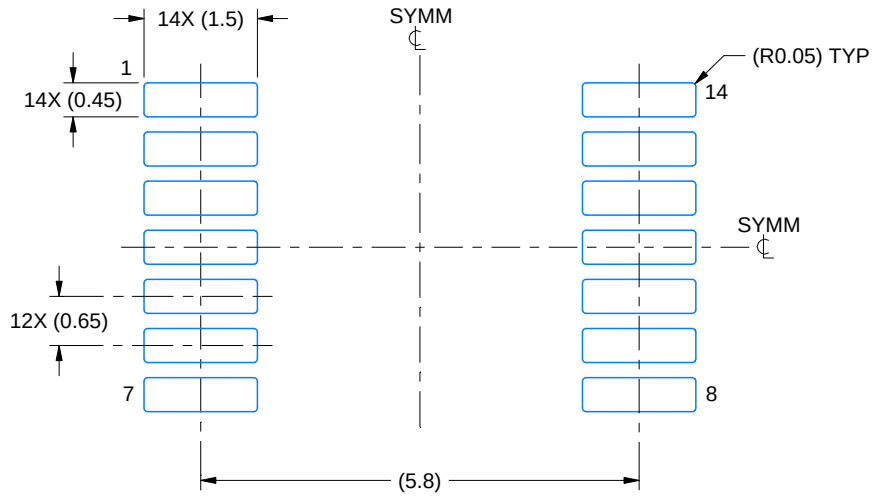
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

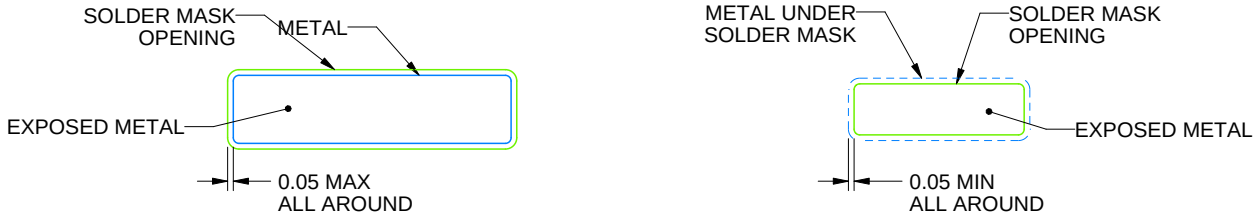


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

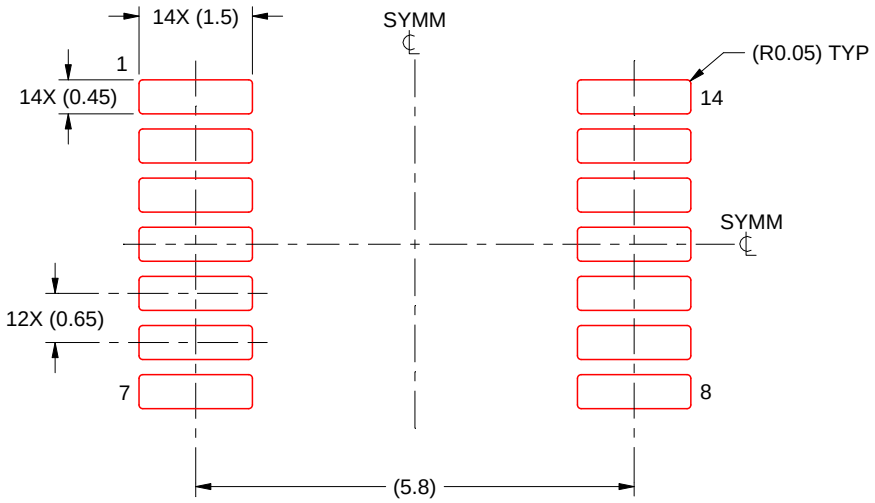


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

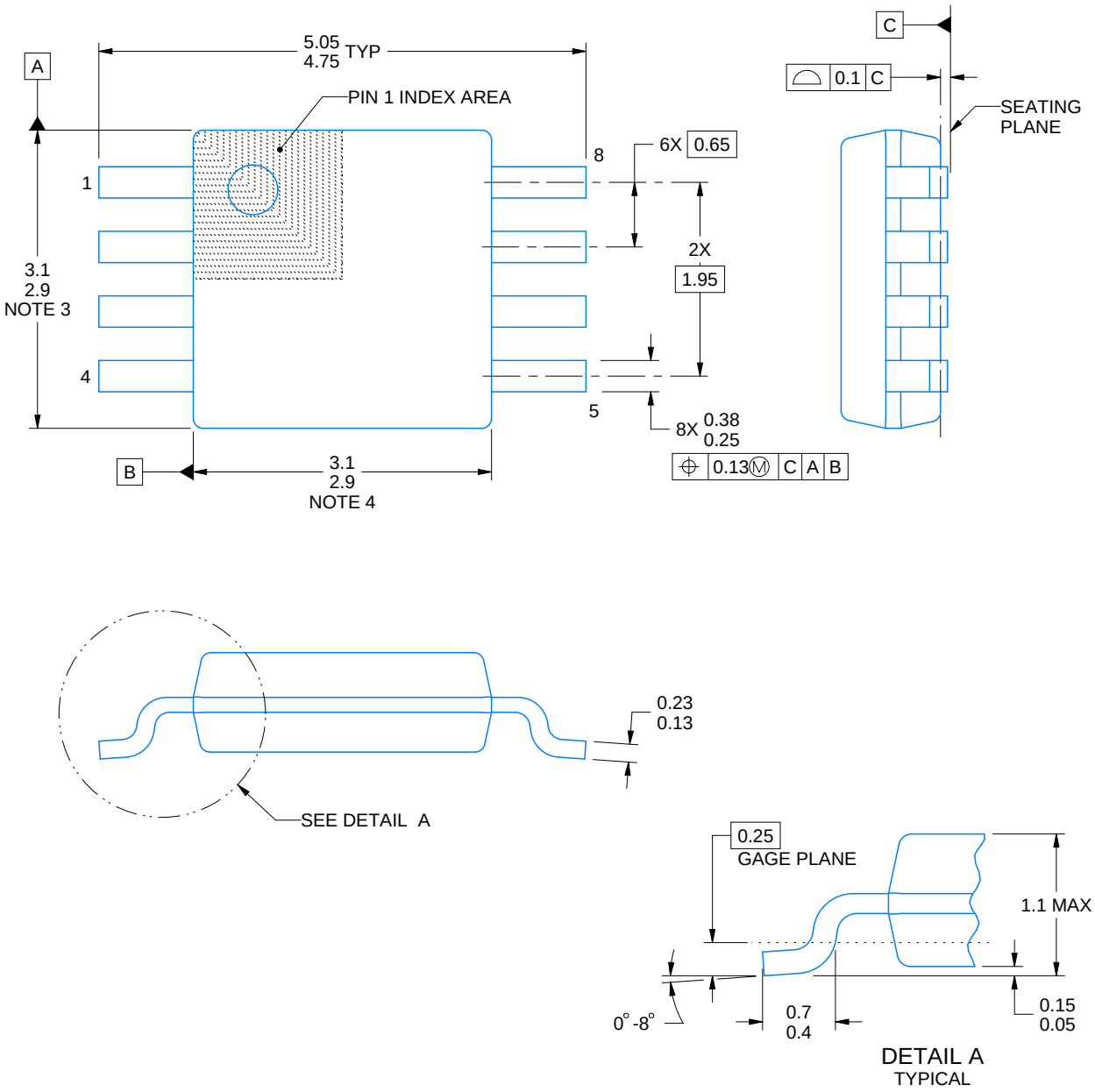
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

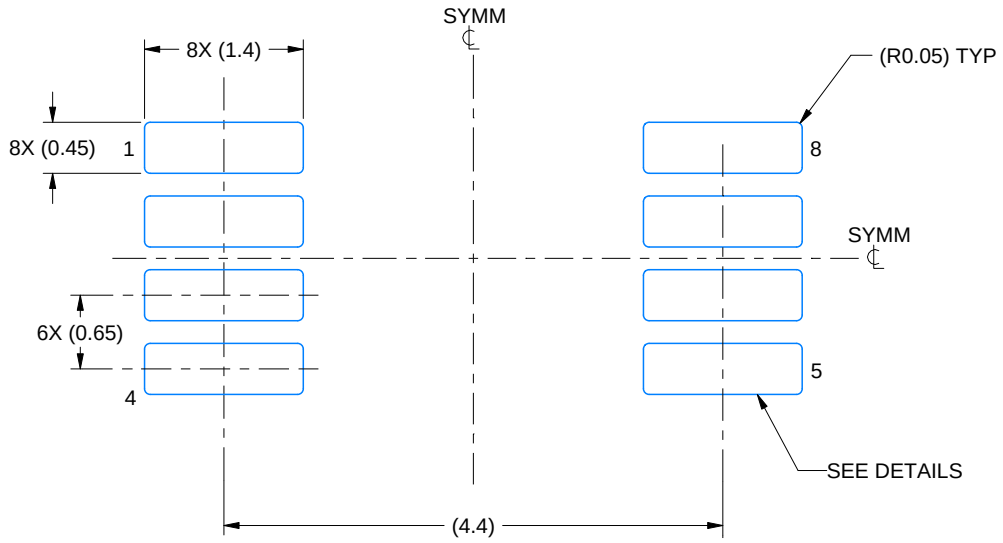
SMALL OUTLINE PACKAGE



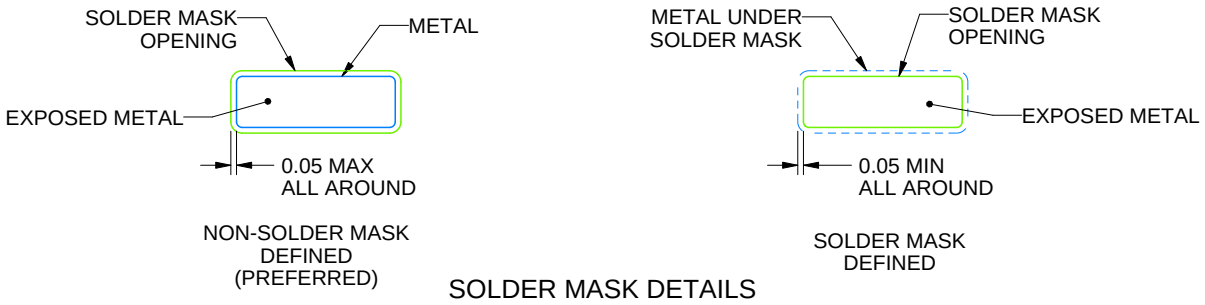
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

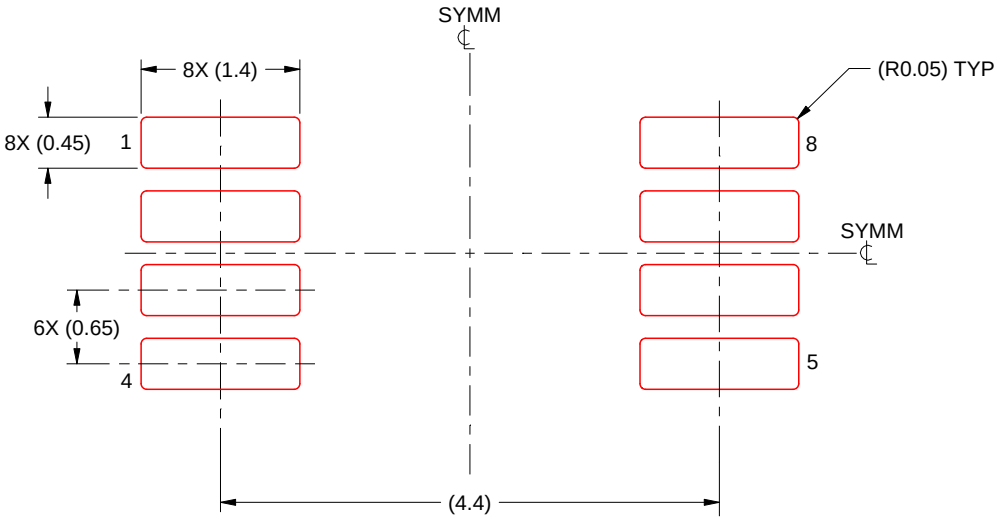


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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