OPAx131 General-Purpose, FET-Input Operational Amplifiers

1 Features

- FET input: I_B = 50pA max
- Low offset voltage: 750μV max
- Wide supply range: ±4.5V to ±18V
- Slew rate: 10V/μs
- Wide bandwidth: 4MHz
- Excellent capacitive load drive
- Single, dual, quad versions

2 Applications

- Data acquisition (DAQ)
- Flow transmitter
- Lab and field instrumentation
- Electrocardiogram (ECG)

3 Description

The OPAx131 series of FET-input op amps provides high performance at low cost. The OPA131 single, OPA2131 dual, and OPA4131 quad versions in industry-standard pinouts allow cost-effective design options.

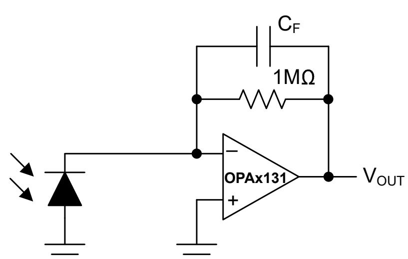
The OPAx131 series offers excellent general-purpose performance, including low offset voltage, drift, and good dynamic characteristics.

Single and dual versions are available in an 8-pin, SOIC, surface-mount package. The quad version is available in 14-pin and 16-pin, SOIC, surface-mount packages, and a 14-pin PDIP package.

Device Information

PART NUMBER	CHANNEL COUNT	PACKAGE[1]
OPA131	Single	D (SOIC, 8)
OPA2131	Dual	D (SOIC, 8)
OPA4131	Quad	D (SOIC, 14)
		DW (SOIC, 16)
		N (PDIP, 14)

(1) For more information, see Section 9.



Simplified Transimpedance Amplifier

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4 Pin Configuration and Functions

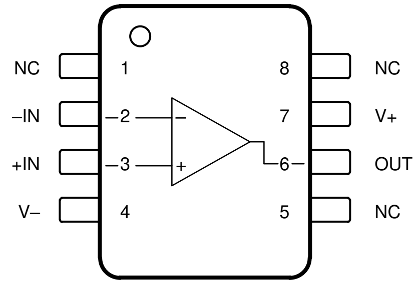


Figure 4-1. OPA131 D Package, 8-Pin SOIC (Top View)

Table 4-1. Pin Functions: OPA131

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN	3	Input	Noninverting input, channel A
–IN	2	Input	Inverting input, channel A
NC	1, 5	—	Do not connect these pins(1)
NC	8	—	No internal connection. Float this pin.
OUT	6	Output	Output
V+	7	Power	Positive (highest) power supply
V–	4	Power	Negative (lowest) power supply

(1) Existing layouts for the OPA131 D package before revision B of this data sheet do not need to be redesigned.

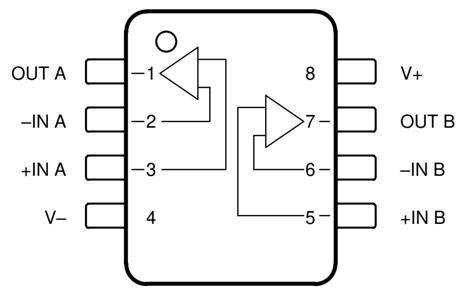


Figure 4-2. OPA2131 D Package, 8-Pin SOIC (Top View)

Table 4-2. Pin Functions: OPA2131

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN A	3	Input	Noninverting input, channel A
+IN B	5	Input	Noninverting input, channel B
–IN A	2	Input	Inverting input, channel A
–IN B	6	Input	Inverting input, channel B
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
V+	8	Power	Positive (highest) power supply
V–	4	Power	Negative (lowest) power supply

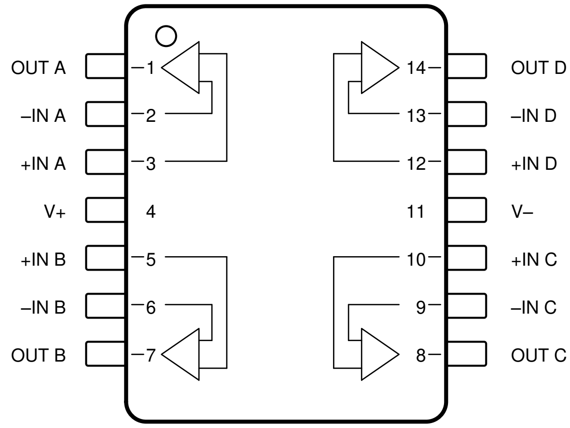


Figure 4-3. OPA4131 D Package, 14-Pin SOIC, and N Package, 14-Pin PDIP (Top View)

Table 4-3. Pin Functions: OPA4131 D and N packages

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN A	3	Input	Noninverting input, channel A
+IN B	5	Input	Noninverting input, channel B
+IN C	10	Input	Noninverting input, channel C
+IN D	12	Input	Noninverting input, channel D
–IN A	2	Input	Inverting input, channel A
–IN B	6	Input	Inverting input, channel B
–IN C	9	Input	Inverting input, channel C
–IN D	13	Input	Inverting input, channel D
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
OUT C	8	Output	Output, channel C
OUT D	14	Output	Output, channel D
V+	4	Power	Positive (highest) power supply
V–	11	Power	Negative (lowest) power supply

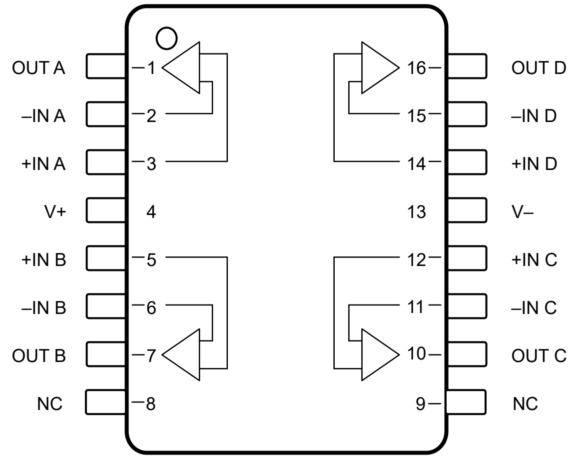


Figure 4-4. OPA4131 DW Package, 16-Pin SOIC (Top View)

Table 4-4. Pin Functions: OPA4131 DW Package

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN A	3	Input	Noninverting input, channel A
+IN B	5	Input	Noninverting input, channel B
+IN C	12	Input	Noninverting input, channel C
+IN D	14	Input	Noninverting input, channel D
–IN A	2	Input	Inverting input, channel A
–IN B	6	Input	Inverting input, channel B
–IN C	11	Input	Inverting input, channel C
–IN D	15	Input	Inverting input, channel D
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
OUT C	10	Output	Output, channel C
OUT D	16	Output	Output, channel D
V+	4	Power	Positive (highest) power supply
V–	13	Power	Negative (lowest) power supply
NC	8, 9	—	No internal connection. Float this pin.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

			MIN	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	Dual supply		±18	V
		Single supply		36	
	Input voltage[(2)]		(V–) – 0.5	(V+) + 0.5	V
	Input current[(2)]			±10	mA
I_{SC}	Output short-circuit[(3)]		Continuous		
T_A	Operating temperature		–55	125	°C
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–55	125	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails must be current limited to 10mA or less.
(3) Short-circuit to ground, one amplifier per package.

5.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	Dual supply	±4.5	±15	±18	V
		Single supply	9	30	36	
T_A	Ambient temperature		–40		+85	°C

5.3 Thermal Information - OPA131

THERMAL METRIC[(1)]		OPA131 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	150	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	74	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	19.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	54.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.4 Thermal Information - OPA2131

THERMAL METRIC[(1)]		OPA2131 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	150	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	10.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	62.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Thermal Information - OPA4131

THERMAL METRIC[(1)]		OPA4131			UNIT
		D (SOIC)	DW (SOIC)	N (PDIP)	
		14 PINS	16 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110	110	80	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56	N/A	N/A	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	53	N/A	N/A	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	19	N/A	N/A	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	46	N/A	N/A	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.6 Electrical Characteristics

at T_A = 25°C, V_S = ±15V, R_L = 10kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	OPAx131UA			±0.2	±1	mV
		OPA2131U, OPA4131U			±0.2	±1.5	
		OPA131U			±0.2	±0.75	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +85°C			±2	±10	µV/°C
PSRR	Power-supply rejection ratio	9V ≤ V_S ≤ 36V	OPAx131UA, OPA2131U, OPA4131U		±50	±200	µV/V
			OPA131U		±50	±100	
INPUT BIAS CURRENT							
I_B	Input bias current(1)				±5	±50	pA
		T_A = –40°C to +85°C		See *Typical Characteristics*			
I_{OS}	Input offset current(1)				±1	±50	pA
NOISE							
e_n	Input voltage noise density	f = 10Hz			21		nV/√Hz
		f = 100Hz			16		
		f = 1kHz			15		
		f = 10kHz			15		
I_n	Input current noise density	f = 1kHz			3		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage			(V–) + 3		(V+) – 3.5	V
CMRR	Common-mode rejection ratio	–12V ≤ V_{CM} ≤ 11.5V	OPAx131UA, OPA2131U, OPA4131U	70	80		dB
			OPA131U	80	86		
INPUT IMPEDANCE							
	Differential				10^{10} || 5		Ω || pF
	Common-mode	–13V ≤ V_{CM} ≤ 11.5V			10^{12} || 4.3		
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	–12V ≤ V_O ≤ 12V	OPAx131UA, OPA2131U, OPA4131U	94	110		dB
			OPA131U	100	110		
FREQUENCY RESPONSE							
GBW	Gain bandwidth product				4		MHz
SR	Slew rate				10		V/µs
	Settling time	10V step, G = 1	0.1%		1.5		µs
			0.01%		2		
THD+N	Total harmonic distortion plus noise	f = 1kHz, G = 1, V_O = 3.5V_{rms}			0.0008%		
OUTPUT							
V_O	Voltage output	R_L = 2kΩ	Positive	(V+) – 3	(V+) – 2.5		V
			Negative		(V–) + 2.5	(V–) + 3	
I_{SC}	Short-circuit current				±20		mA
POWER SUPPLY							
I_Q	Quiescent current (per amplifier)	I_O = 0mA	OPAx131UA		±1.5	±1.75	mA
			OPAx131U		±1.5	±2	

(1) High-speed test at T_J = 25°C.

5.7 Typical Characteristics

at T_A = 25°C, V_S = ±15V, R_L = 10kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

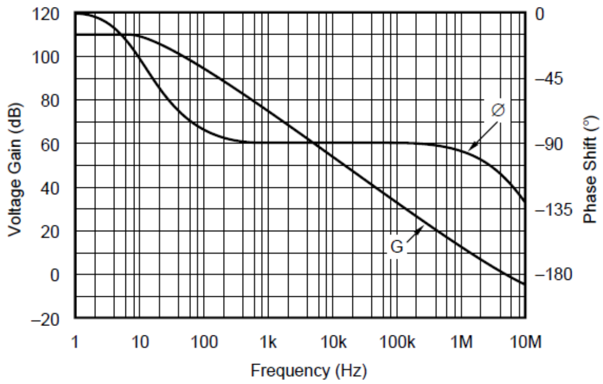


Figure 5-1. Open-Loop Gain and Phase vs Frequency

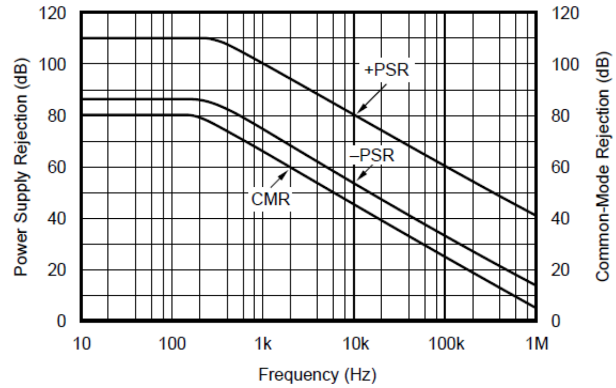


Figure 5-2. Power Supply and Common-Mode Rejection vs Frequency

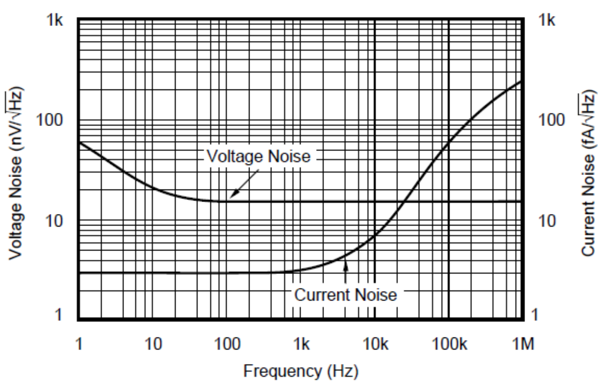


Figure 5-3. Input Voltage and Current Noise Spectral Density vs Frequency

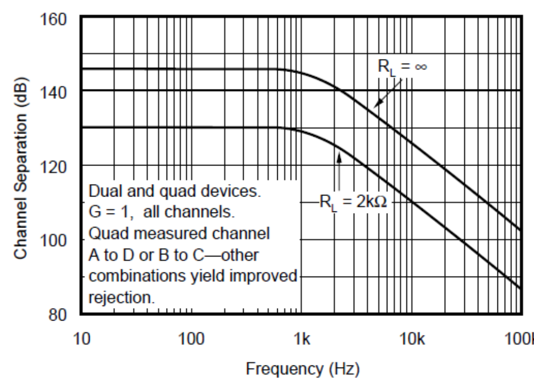


Figure 5-4. Channel Separation vs Frequency

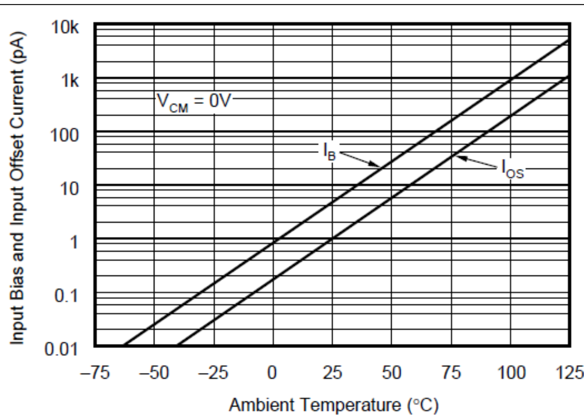


Figure 5-5. Input Bias and Input Offset Current vs Temperature

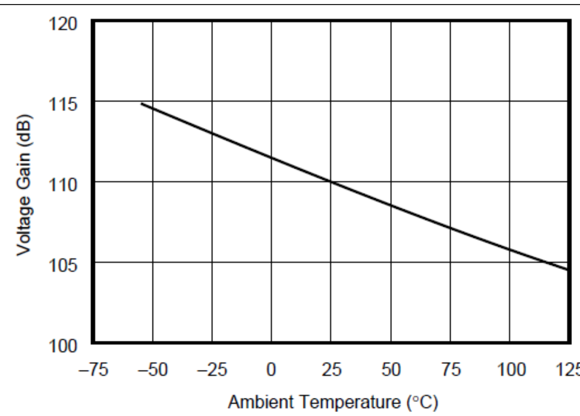


Figure 5-6. Open-Loop Gain vs Temperature

5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15V, R_L = 10kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

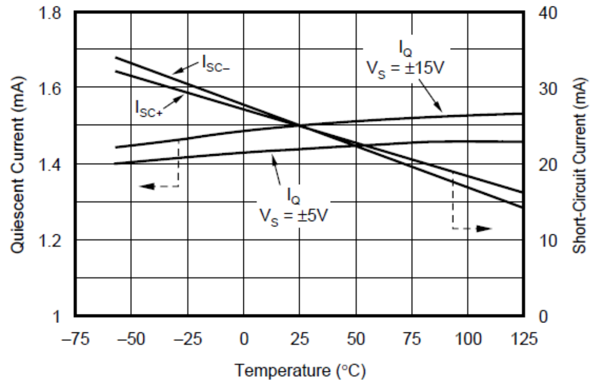


Figure 5-7. Quiescent Current and Short-Circuit Current vs Temperature

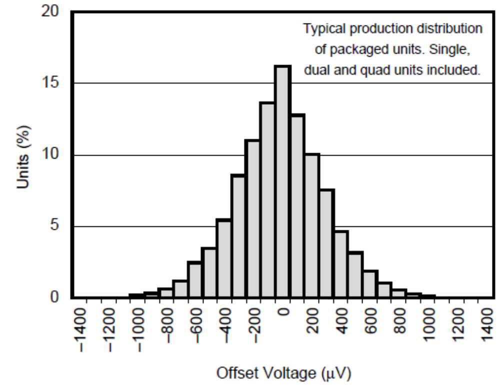


Figure 5-8. Offset Voltage Production Distribution

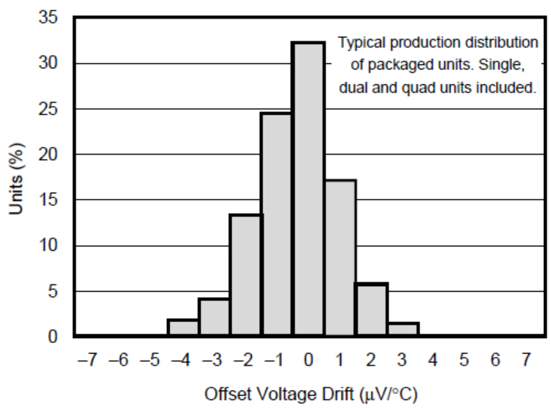


Figure 5-9. Offset Voltage Drift Production Distribution

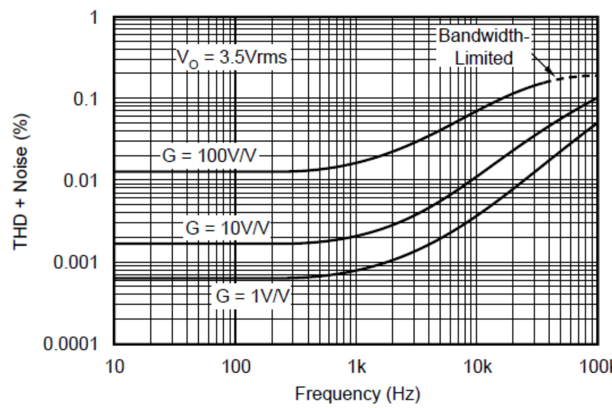


Figure 5-10. Total Harmonic Distortion + Noise vs Frequency

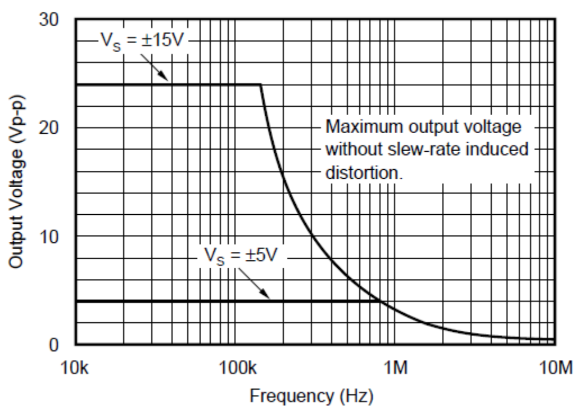


Figure 5-11. Maximum Output Voltage vs Frequency

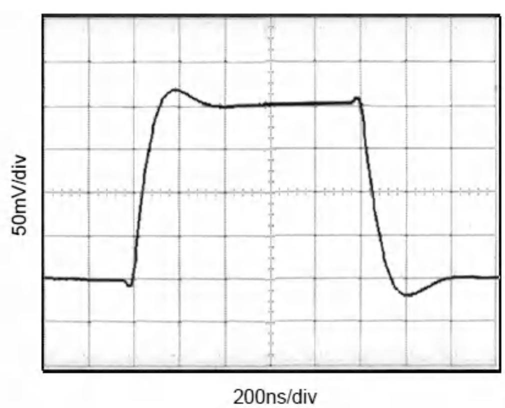


Figure 5-12. Small-Signal Step Response G = 1, C_L = 300pF

5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15V, R_L = 10kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

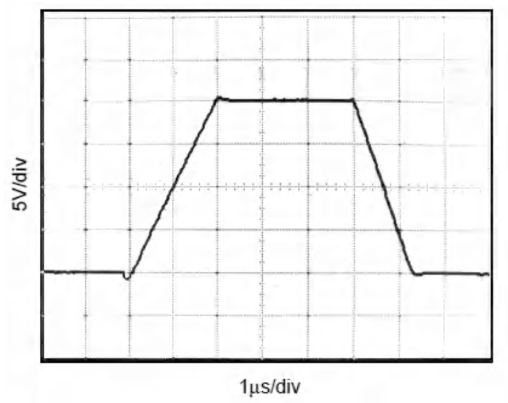


Figure 5-13. Large-Signal Step Response G = 1, C_L = 300pF

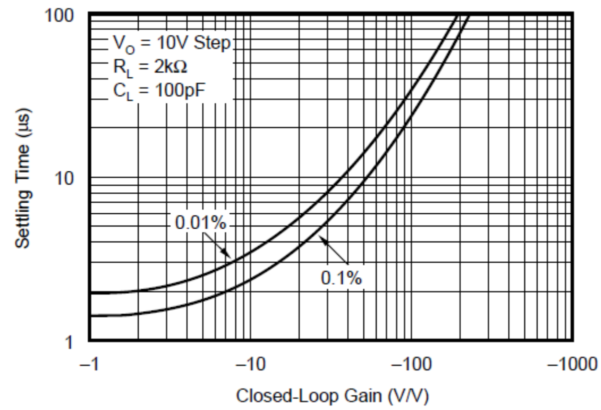


Figure 5-14. Settling Time vs Closed-Loop Gain

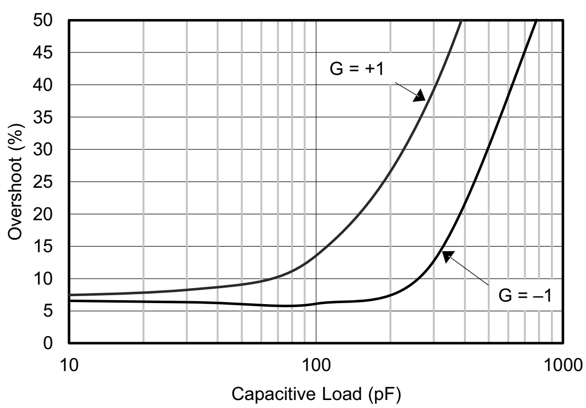


Figure 5-15. Small-Signal Overshoot vs Load Capacitance

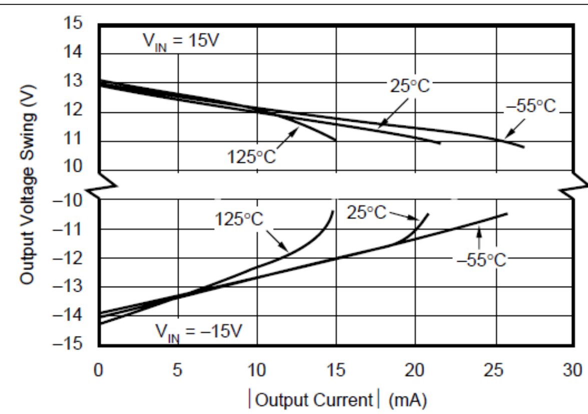


Figure 5-16. Output Voltage Swing vs Output Current

6 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

6.1 Application Information

The OPAx131 series op amps are unity-gain stable and an excellent choice for a wide range of general-purpose applications. Bypass power-supply pins with 10nF ceramic capacitors or larger.

The OPAx131 series op amps are free from unexpected output phase-reversal common with FET op amps. Many FET-input op amps exhibit phase-reversal of the output when the input common-mode voltage range is exceeded. This can occur in voltage-follower circuits, causing serious problems in control-loop applications. All circuitry is completely independent in dual and quad versions, and normal behavior can be expected when one amplifier in a package is overdriven or short-circuited.

6.1.1 Offset Voltage Trim

The offset voltage of the OPAx131 amplifiers is laser trimmed and usually requires no user adjustment. The OPAx131 provide less than ±1mV of input offset voltage and less than 10µV/°C of input offset voltage drift over the operating temperature range.

6.2 Typical Application

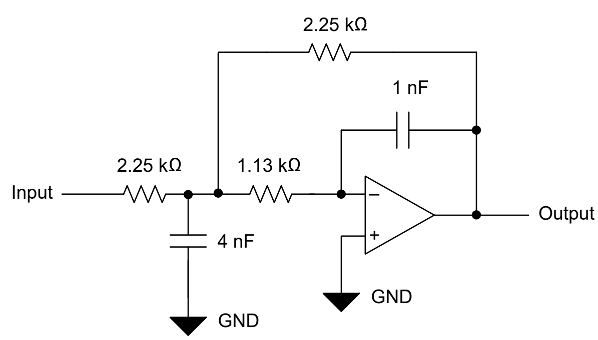


Figure 6-1. Second-Order Low-Pass Filter

6.2.1 Input Bias Current

The input bias current is approximately 5pA at room temperature and increases with temperature (see also Figure 5-5). Input bias current also varies with common-mode voltage and power-supply voltage. This variation depends on the voltage between the negative power supply and the common-mode input voltage.

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

7.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

7.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.5 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (December 2002) to Revision B (July 2024) — **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document ... 1
- Added the *Device Information* table, and the *Applications*, *Pin Configuration and Functions*, *Specifications*, *Recommended Operating Conditions*, *Thermal Information*, *Application and Implementation*, *Typical Application*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections ... 1
- Updated *Description* ... 1
- Deleted obsolete PDIP packages for OPA131 and OPA2131 ... 3
- Updated input voltage in *Absolute Maximum Ratings* ... 6
- Added input current and related footnote to *Absolute Maximum Ratings* ... 6
- Changed format of *Electrical Characteristics* to latest standard ... 8
- Updated nominal conditions in the header of *Electrical Characteristics* ... 8
- Deleted channel separation specification ... 8
- Updated common-mode voltage MAX value ... 8
- Updated common-mode rejection ratio and common-mode input impedance test conditions ... 8
- Changed differential input impedance from $10^{10}\Omega$ || 1pF to $10^{10}\Omega$ || 5pF ... 8
- Changed common-mode input impedance from $10^{10}\Omega$ || 3pF to $10^{10}\Omega$ || 4.3pF ... 8
- Updated open loop voltage gain MIN and TYP values for R_L = 10kΩ and R_L = 2kΩ ... 8
- Updated settling time test condition ... 8
- Moved voltage output negative MIN values to MAX values ... 8

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA131U	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI | Nipdau	Level-3-260C-168 HR	-55 to 125	(O131U, OPA) 131U
OPA131U.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	(O131U, OPA) 131U
OPA131UA	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI | Nipdau	Level-3-260C-168 HR	-55 to 125	(O131U, OPA) 131U A
OPA131UA.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	(O131U, OPA) 131U A
OPA131UA/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI | Nipdau	Level-3-260C-168 HR	-55 to 125	(O131U, OPA) 131U A
OPA131UA/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	(O131U, OPA) 131U A
OPA131UJ	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU | NIPDAU	Level-3-260C-168 HR	-55 to 125	(O131UJ, OPA) 131UJ
OPA131UJ.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	(O131UJ, OPA) 131UJ
OPA131UJ/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-3-260C-168 HR	-55 to 125	(O131UJ, OPA) 131UJ
OPA131UJ/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	(O131UJ, OPA) 131UJ
OPA2131UA	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU | NIPDAU	Level-3-260C-168 HR	-55 to 125	(2131UA, OPA)
OPA2131UA.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	(2131UA, OPA)
OPA2131UA/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-3-260C-168 HR	-55 to 125	(2131UA, OPA)
OPA2131UA/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	(2131UA, OPA)
OPA2131UJ	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU | NIPDAU	Level-3-260C-168 HR	-40 to 85	(2131UJ, OPA)
OPA2131UJ.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	(2131UJ, OPA)
OPA2131UJ/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-3-260C-168 HR	-40 to 85	(2131UJ, OPA)
OPA2131UJ/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	(2131UJ, OPA)
OPA4131NA	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4131NA

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA4131NA.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4131NA
OPA4131NA.B	Active	Production	SOIC (D) | 14	50 | TUBE	-	Call TI	Call TI	-40 to 85	
OPA4131NJ	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4131NJ
OPA4131NJ.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4131NJ
OPA4131NJ.B	Active	Production	SOIC (D) | 14	50 | TUBE	-	Call TI	Call TI	-40 to 85	
OPA4131PA	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	OPA4131PA
OPA4131PA.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	OPA4131PA
OPA4131PAG4	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	OPA4131PA
OPA4131PJ	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	OPA4131PJ
OPA4131PJ.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	OPA4131PJ
OPA4131UA	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4131UA
OPA4131UA.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4131UA
OPA4131UA/1K	Active	Production	SOIC (DW) | 16	1000 | LARGE T&R	Yes	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4131UA
OPA4131UA/1K.A	Active	Production	SOIC (DW) | 16	1000 | LARGE T&R	Yes	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4131UA

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

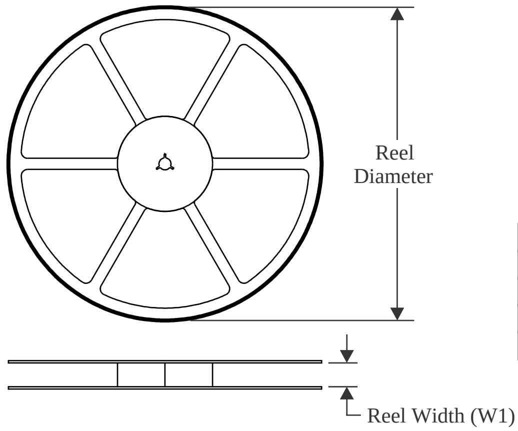
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

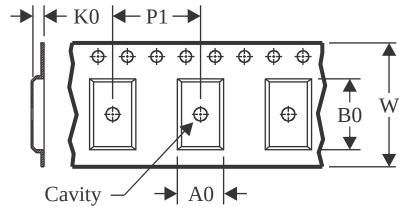
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

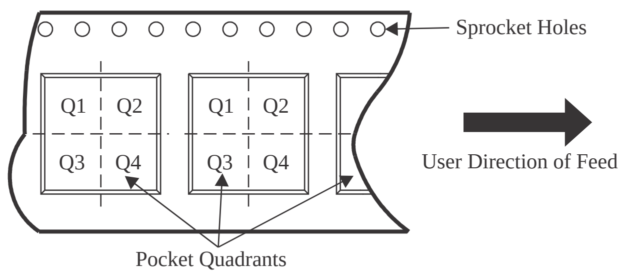


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

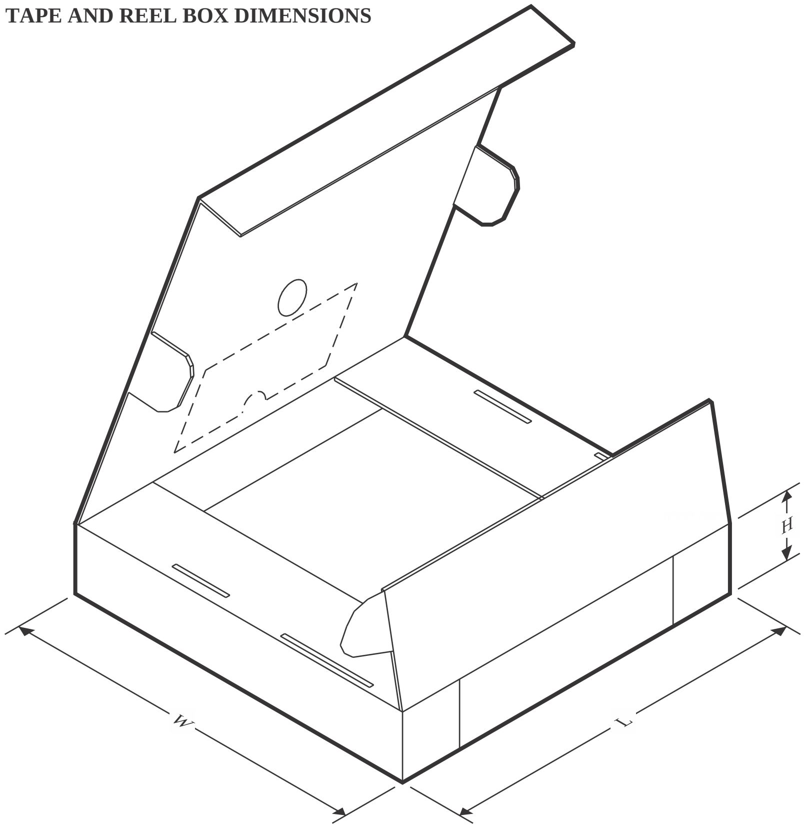
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA131UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA131UJ/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2131UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2131UJ/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4131UA/1K	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

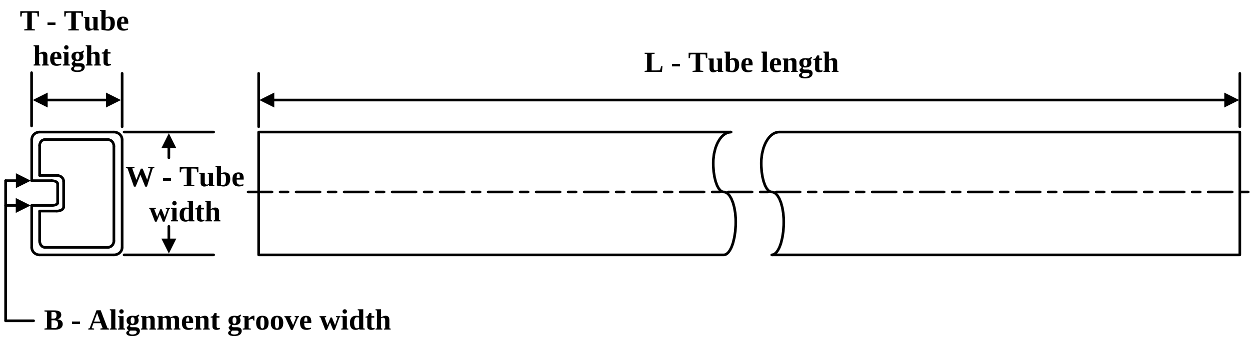
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

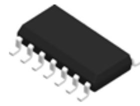
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA131UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0
OPA131UJ/2K5	SOIC	D	8	2500	353.0	353.0	32.0
OPA2131UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0
OPA2131UJ/2K5	SOIC	D	8	2500	353.0	353.0	32.0
OPA4131UA/1K	SOIC	DW	16	1000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA131U	D	SOIC	8	75	506.6	8	3940	4.32
OPA131U.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA131UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA131UA.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA131UJ	D	SOIC	8	75	506.6	8	3940	4.32
OPA131UJ.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA2131UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA2131UA.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA2131UJ	D	SOIC	8	75	506.6	8	3940	4.32
OPA2131UJ.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA4131NA	D	SOIC	14	50	506.6	8	3940	4.32
OPA4131NA.A	D	SOIC	14	50	506.6	8	3940	4.32
OPA4131NJ	D	SOIC	14	50	506.6	8	3940	4.32
OPA4131NJ.A	D	SOIC	14	50	506.6	8	3940	4.32
OPA4131PA	N	PDIP	14	25	506	13.97	11230	4.32
OPA4131PA.A	N	PDIP	14	25	506	13.97	11230	4.32
OPA4131PAG4	N	PDIP	14	25	506	13.97	11230	4.32
OPA4131PJ	N	PDIP	14	25	506	13.97	11230	4.32
OPA4131PJ.A	N	PDIP	14	25	506	13.97	11230	4.32
OPA4131UA	DW	SOIC	16	40	507	12.83	5080	6.6
OPA4131UA.A	DW	SOIC	16	40	507	12.83	5080	6.6

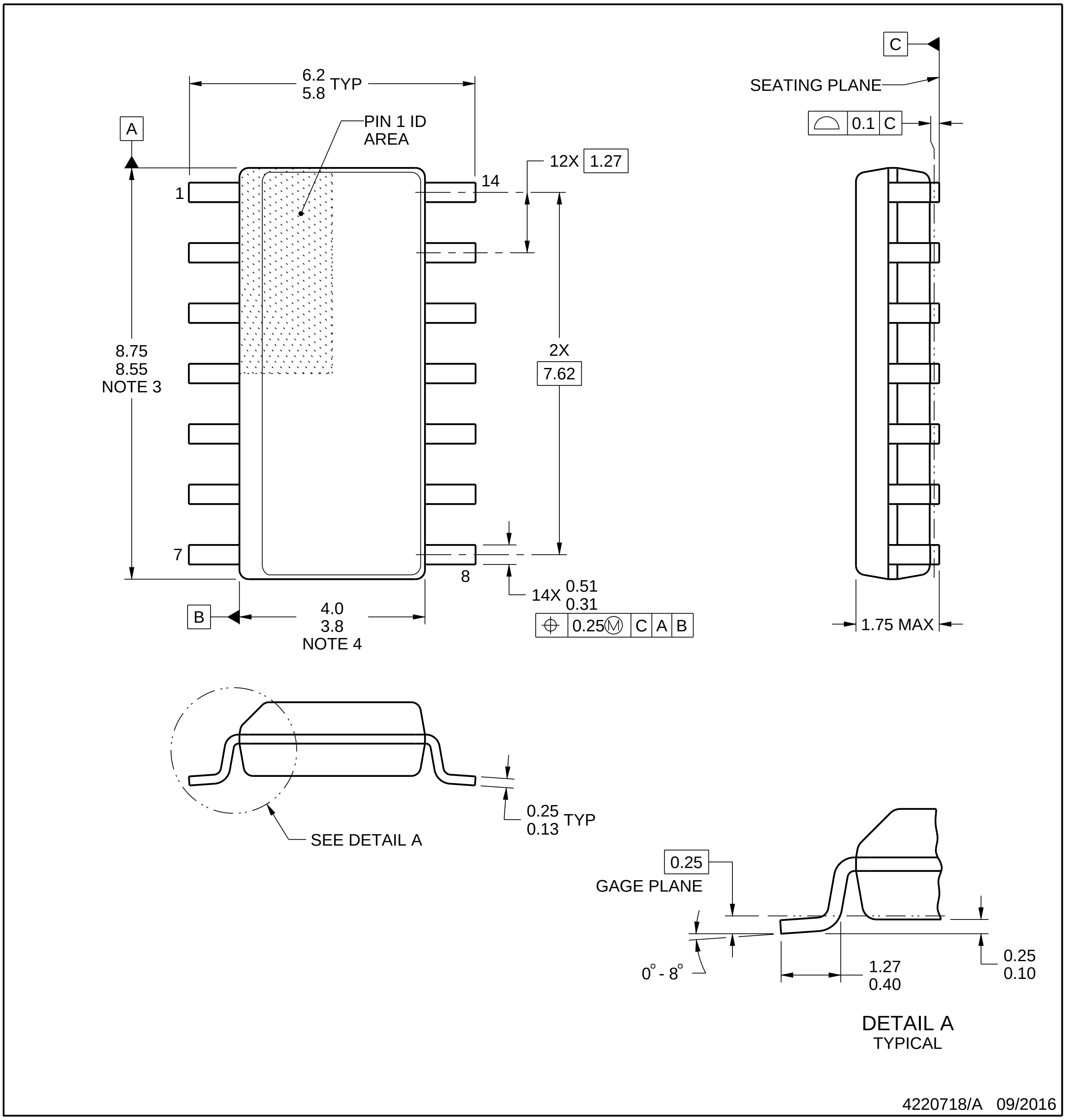


PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

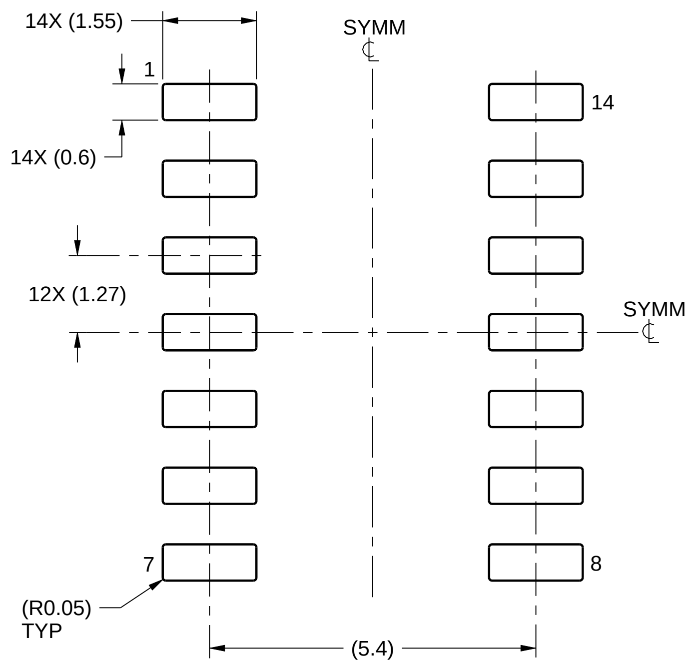
SMALL OUTLINE INTEGRATED CIRCUIT



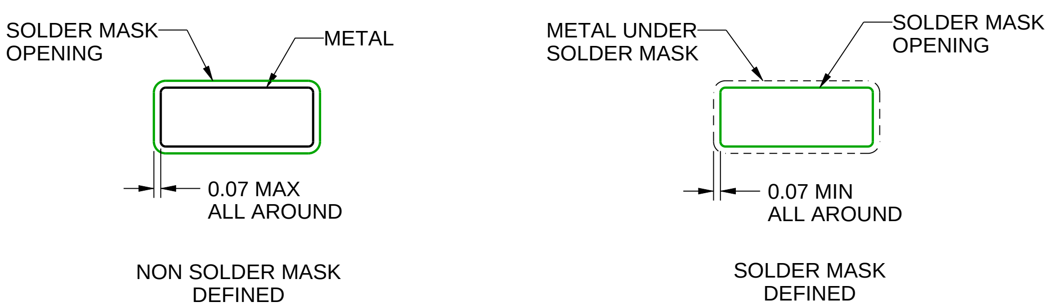
4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X

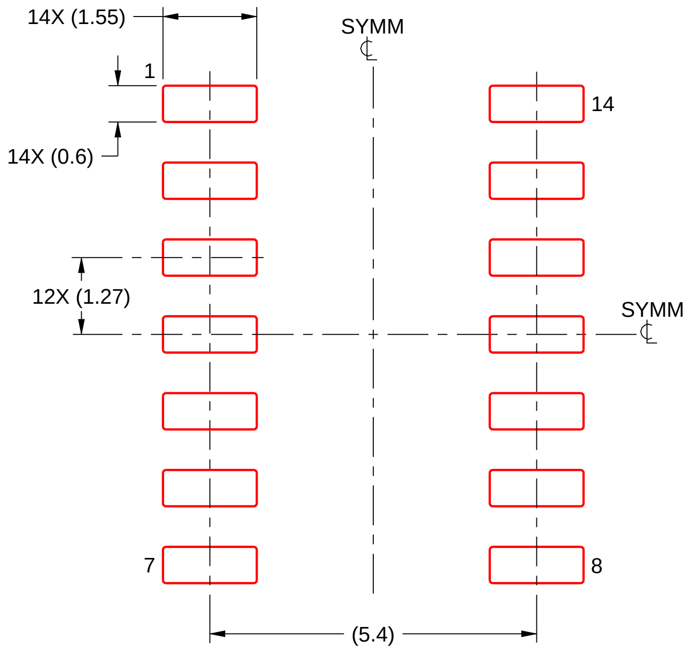


SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



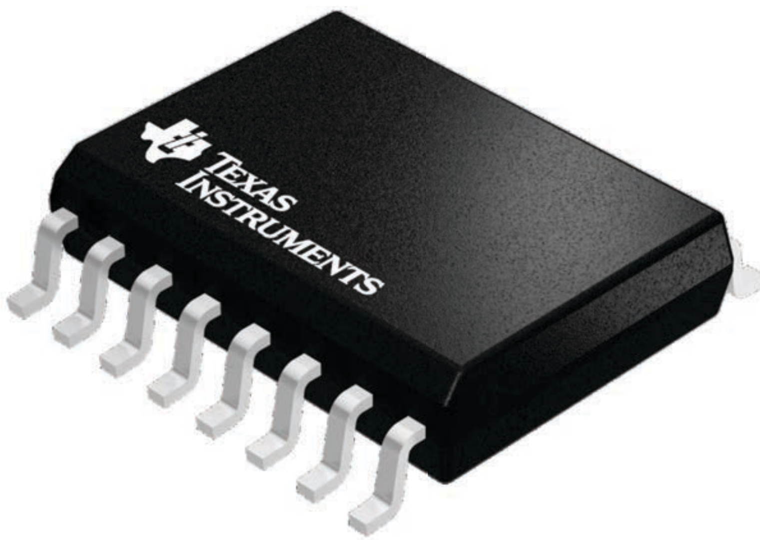
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

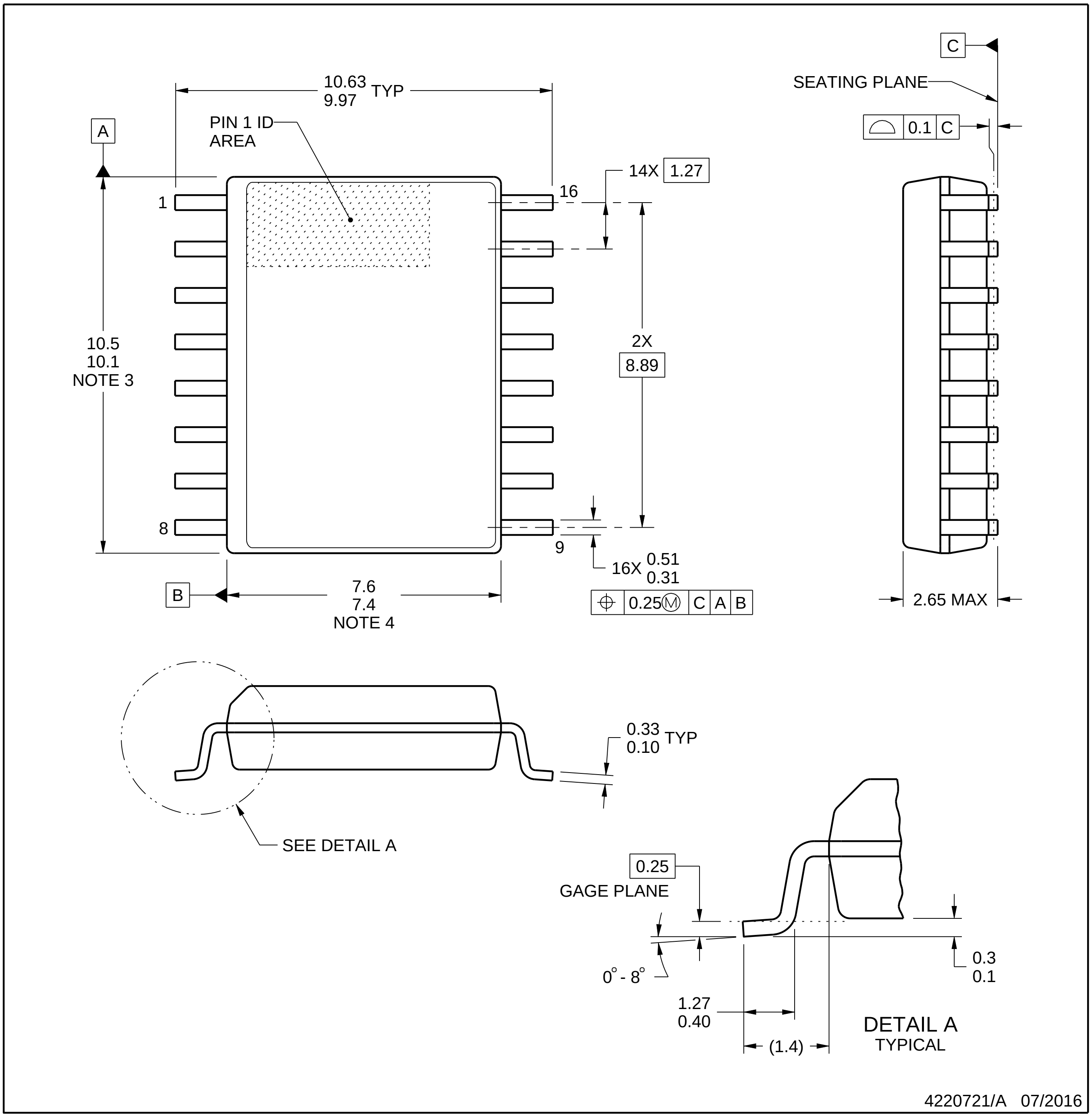
4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

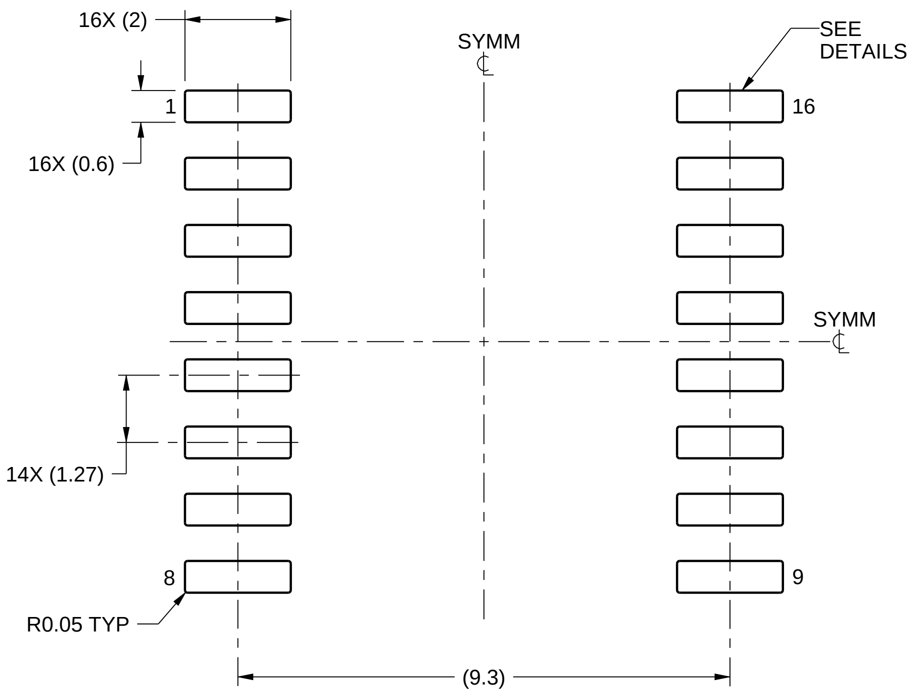
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



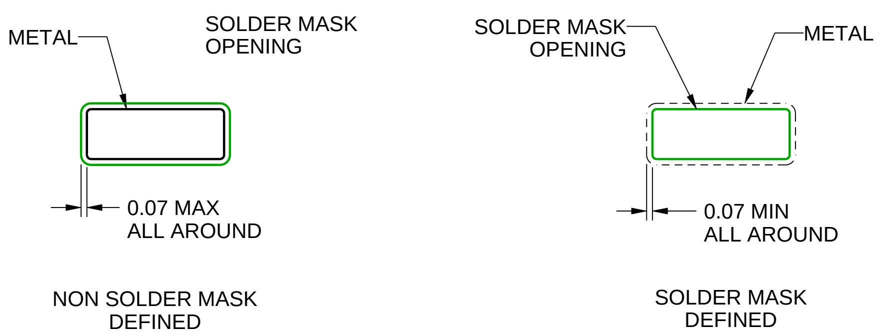


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

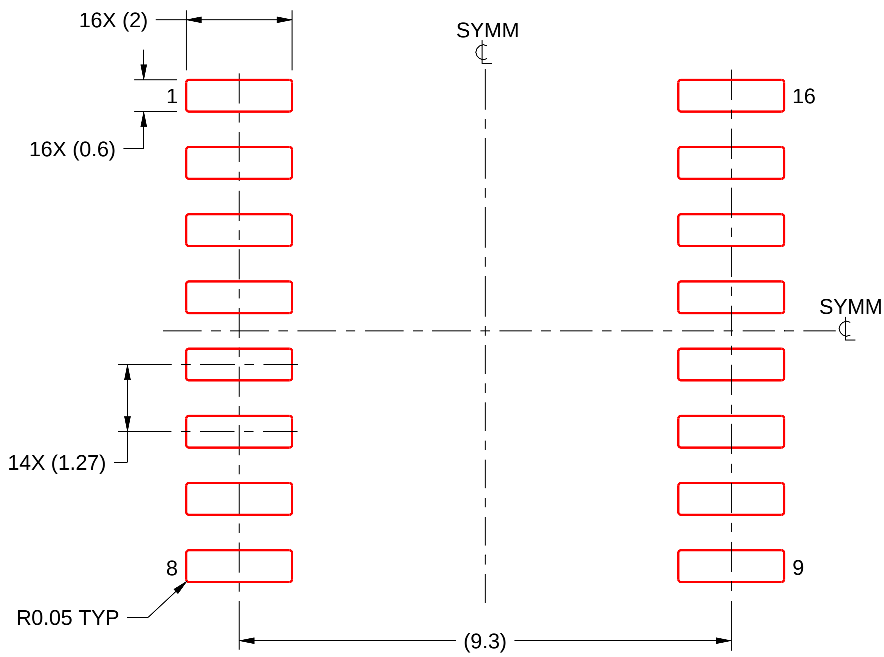


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

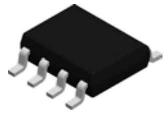


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

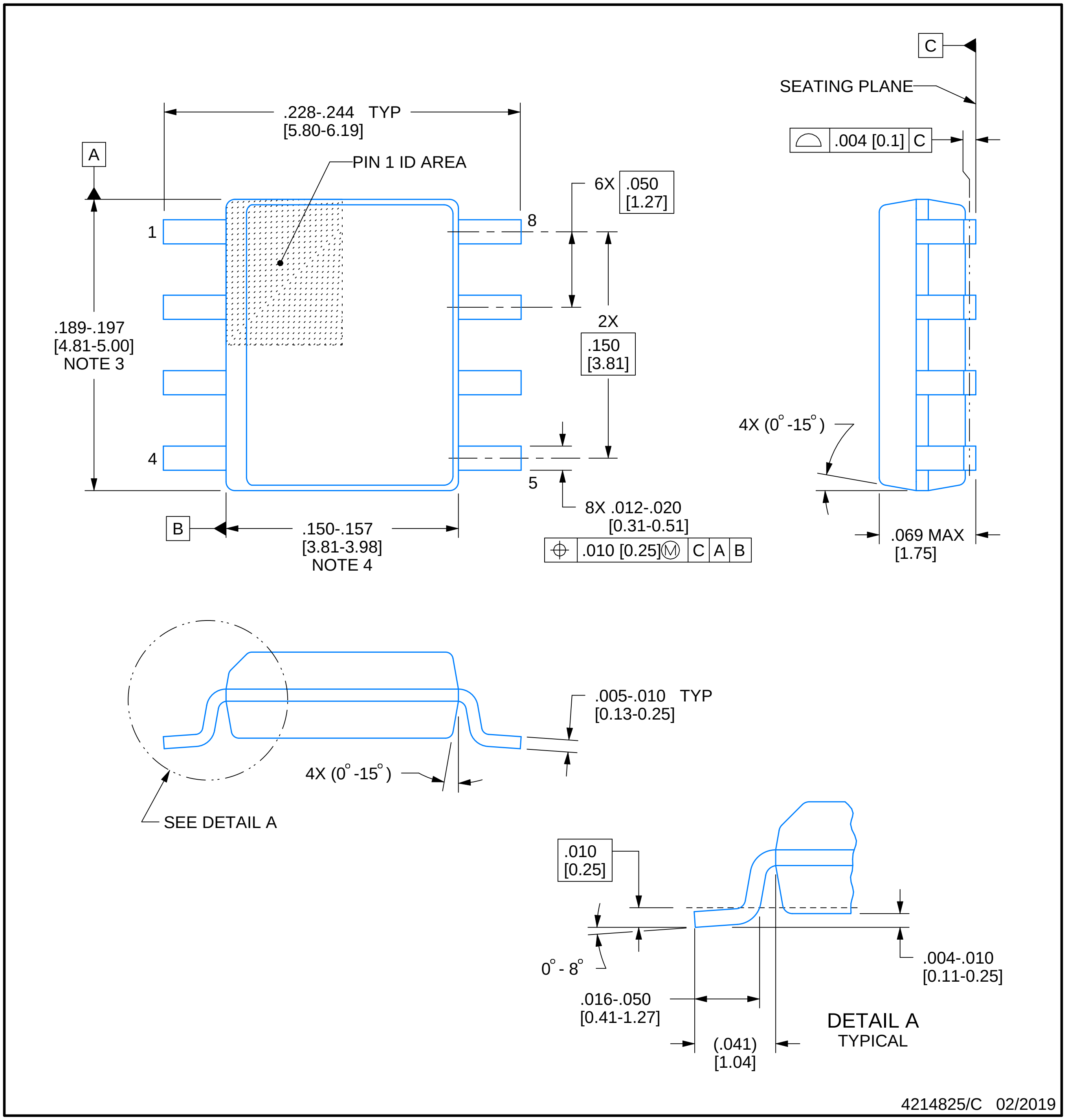


PACKAGE OUTLINE

D0008A

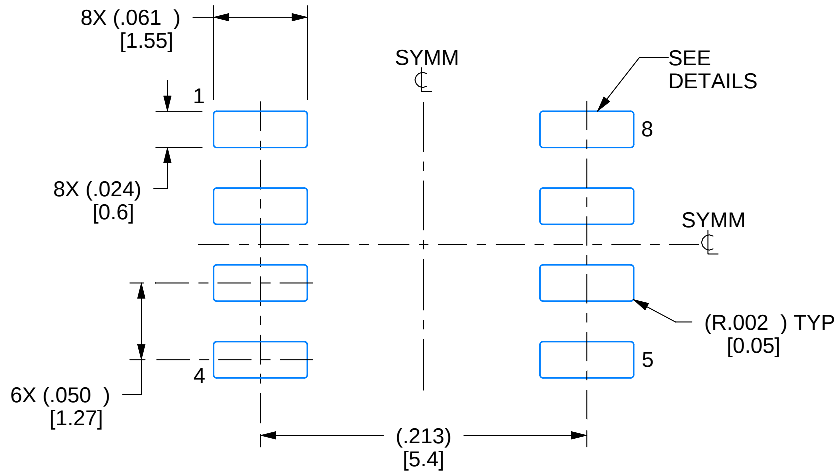
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

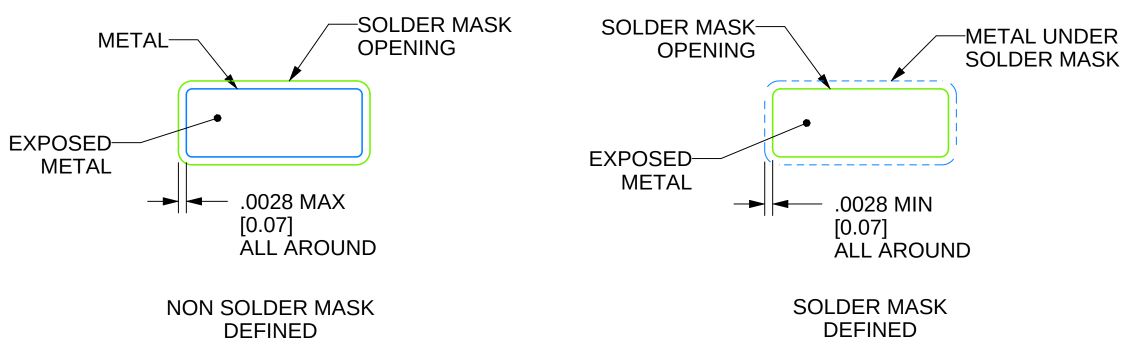


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

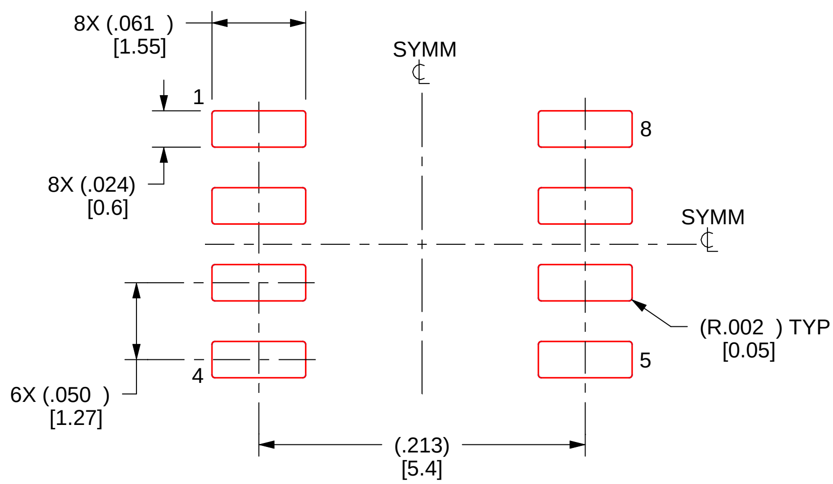


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

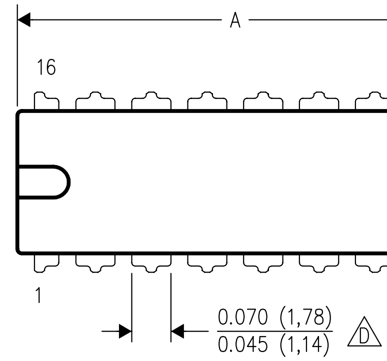
4214825/C 02/2019

NOTES: (continued)

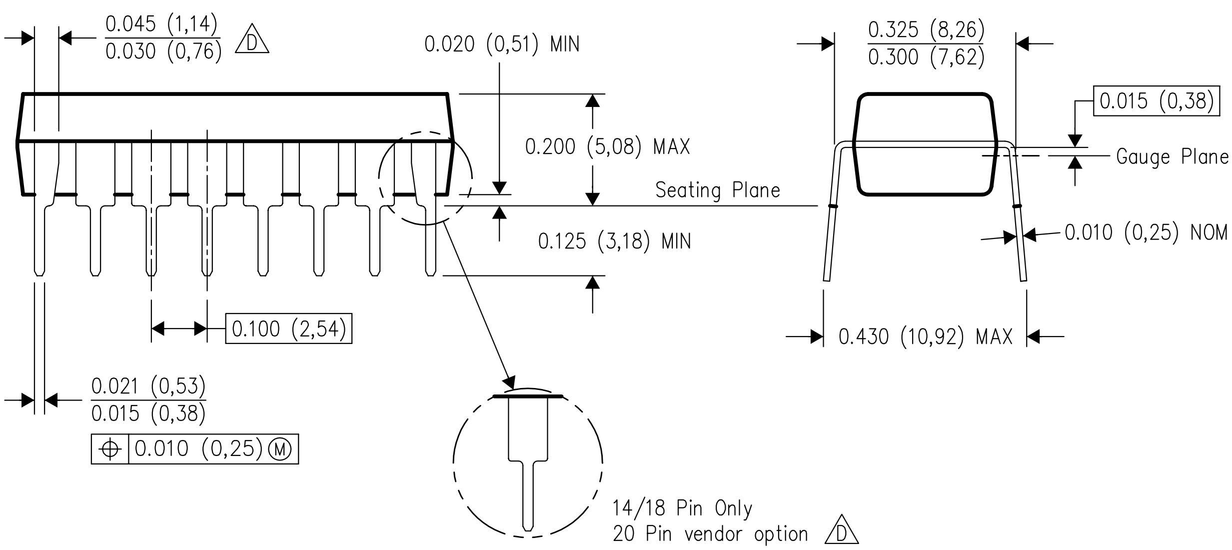
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
C MS–001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
- D. The 20 pin end lead shoulder width is a vendor option, either half or full width.