SBOS638 – JUNE 2012

1.1nV/√Hz NOISE, LOW POWER, PRECISION OPERATIONAL AMPLIFIER

Check for Samples: OPA211-EP

1 FEATURES

- LOW VOLTAGE NOISE: 1.1nV/√Hz at 1kHz
- INPUT VOLTAGE NOISE: $80nV_{PP}$ (0.1Hz to 10Hz)
- THD+N: –136dB (G = 1, f = 1kHz)
- OFFSET VOLTAGE: 180µV (max)
- OFFSET VOLTAGE DRIFT: 0.35µV/°C (typ)
- LOW SUPPLY CURRENT: 3.6mA/Ch (typ)
- UNITY-GAIN STABLE
- GAIN BANDWIDTH PRODUCT:
  80MHz (G = 100)
  45MHz (G = 1)
- SLEW RATE: 27V/µs
- 16-BIT SETTLING: 700ns
- WIDE SUPPLY RANGE:
  ±2.25V to ±18V, +4.5V to +36V
- RAIL-TO-RAIL OUTPUT
- OUTPUT CURRENT: 30mA

2 APPLICATIONS

- PLL LOOP FILTER
- LOW-NOISE, LOW-POWER SIGNAL PROCESSING
- 16-BIT ADC DRIVERS
- DAC OUTPUT AMPLIFIERS
- ACTIVE FILTERS
- LOW-NOISE INSTRUMENTATION AMPS
- ULTRASOUND AMPLIFIERS
- PROFESSIONAL AUDIO PREAMPLIFIERS
- LOW-NOISE FREQUENCY SYNTHESIZERS
- INFRARED DETECTOR AMPLIFIERS
- HYDROPHONE AMPLIFIERS
- GEOPHONE AMPLIFIERS
- MEDICAL

3 SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- CONTROLLED BASELINE
- ONE ASSEMBLY/TEST SITE
- ONE FABRICATION SITE
- AVAILABLE IN MILITARY (–55°C/125°C) TEMPERATURE RANGE (1)
- EXTENDED PRODUCT LIFE CYCLE
- EXTENDED PRODUCT-CHANGE NOTIFICATION
- PRODUCT TRACEABILITY

(1) Additional temperature ranges available - contact factory

4 DESCRIPTION

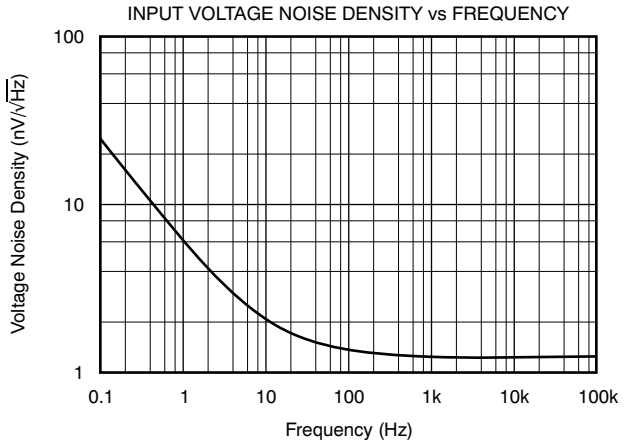
The OPA211 series of precision operational amplifiers achieves very low 1.1nV/√Hz noise density with a supply current of only 3.6mA. This series also offers rail-to-rail output swing, which maximizes dynamic range.

The extremely low voltage and low current noise, high speed, and wide output swing of the OPA211 series make these devices an excellent choice as a loop filter amplifier in PLL applications.

In precision data acquisition applications, the OPA211 series of op amps provides 700ns settling time to 16-bit accuracy throughout 10V output swings. This ac performance, combined with only 125µV of offset and 0.35µV/°C of drift over temperature, makes the OPA211 ideal for driving high-precision 16-bit analog-to-digital converters (ADCs) or buffering the output of high-resolution digital-to-analog converters (DACs).

The OPA211 is specified over a wide dual-power supply range of ±2.25V to ±18V, or for single-supply operation from +4.5V to +36V.

The OPA211 is available in a small MSOP-8 package. This op amp is specified from T_A = –55°C to +125°C.

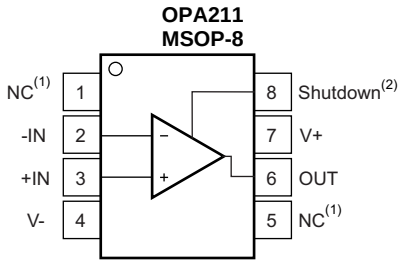


PACKAGE/ORDERING INFORMATION(1)

T_A	PACKAGE	ORDERABLE PART NUMBER	PACKAGE MARKING	VID NUMBER
-55°C to 125°C	MSOP-8 - DGK	OPA211MDGKTEP	OBCM	V62/12619-01XE

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

5 PIN CONFIGURATIONS



(1) NC denotes no internal connection.

(2) Shutdown function:

- Device enabled: (V–) ≤ $V_{SHUTDOWN}$ ≤ (V+) – 3V
- Device disabled: $V_{SHUTDOWN}$ ≥ (V+) – 0.35V

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5.1 ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

		VALUE	UNIT
Supply Voltage	V_S = (V+) – (V–)	40	V
Input Voltage		(V–) – 0.5 to (V+) + 0.5	V
Input Current (Any pin except power-supply pins)		±10	mA
Output Short-Circuit(2)		Continuous	
Operating Temperature	(T_A)	–55 to +125	°C
Storage Temperature	(T_A)	–65 to +150	°C
Junction Temperature	(T_J)	200	°C
ESD Ratings	Human Body Model (HBM)	3000	V
	Charged Device Model (CDM)	1000	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

(2) Short-circuit to V_S/2 (ground in symmetrical dual supply setups), one amplifier per package.

6 THERMAL INFORMATION

THERMAL METRIC(1)		OPA211 DGK 8 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	184.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	71.2	
θ_{JB}	Junction-to-board thermal resistance(4)	104.9	
ψ_{JT}	Junction-to-top characterization parameter(5)	11.5	
ψ_{JB}	Junction-to-board characterization parameter(6)	103.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

6.1 ELECTRICAL CHARACTERISTICS: V_S = ±2.25V to ±18V

BOLDFACE limits apply over the specified temperature range, T_A = –55°C to +125°C.
At T_A = +25°C, R_L = 10kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

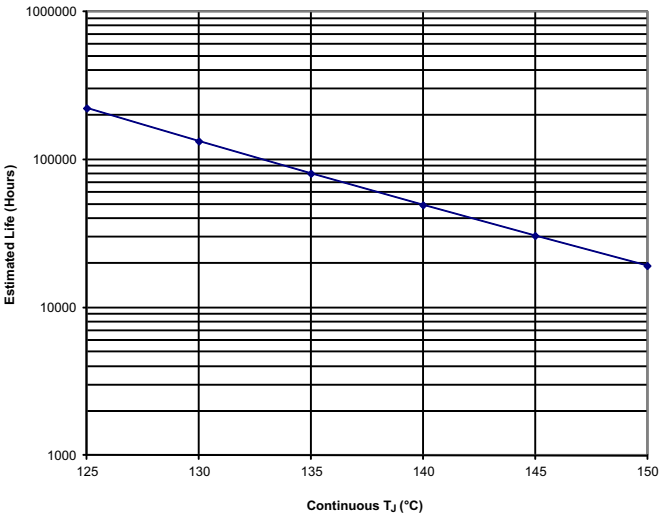
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	V_S = ±15V		±20	±100	µV
Over Temperature					**±180**	**µV**
Drift	**dV_{OS}/dT**			**0.35**		**µV/°C**
vs Power Supply	PSRR	V_S = ±2.25V to ±18V		0.1	0.5	µV/V
Over Temperature					**3**	**µV/V**
INPUT BIAS CURRENT						
Input Bias Current	**I_B**	**V_{CM} = 0V**		**±50**	**±200**	**nA**
Offset Current	**I_{OS}**	**V_{CM} = 0V**		**±20**	**±150**	**nA**
NOISE						
Input Voltage Noise	e_n	f = 0.1Hz to 10Hz		80		nV_{PP}
Input Voltage Noise Density		f = 10Hz		2		$nV/\sqrt{Hz}$
		f = 100Hz		1.4		$nV/\sqrt{Hz}$
		f = 1kHz		1.1		$nV/\sqrt{Hz}$
Input Current Noise Density	I_n	f = 10Hz		3.2		$pA/\sqrt{Hz}$
		f = 1kHz		1.7		$pA/\sqrt{Hz}$
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}	V_S ≥ ±5V	(V–) + 1.8		(V+) – 1.4	V
		V_S < ±5V	(V–) + 2		(V+) – 1.4	V
Common-Mode Rejection Ratio	**CMRR**	**V_S ≥ ±5V, (V–) + 2V ≤ V_{CM} ≤ (V+) – 2V**	**114**	**120**		**dB**
		V_S < ±5V, (V–) + 2V ≤ V_{CM} ≤ (V+) – 2V	**108**	**120**		**dB**
INPUT IMPEDANCE						
Differential				20k || 8		Ω || pF
Common-Mode				10^9 || 2		Ω || pF
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	**A_{OL}**	**(V–) + 0.2V ≤ V_O ≤ (V+) – 0.2V, R_L = 10kΩ**	**114**	**130**		**dB**
	A_{OL}	(V–) + 0.6V ≤ V_O ≤ (V+) – 0.6V, R_L = 600Ω	110	114		dB
Over Temperature	**A_{OL}**	**(V–) + 0.6V ≤ V_O ≤ (V+) – 0.6V, I_O ≤ 15mA**	**110**			**dB**
	A_{OL}	**(V–) + 0.6V ≤ V_O ≤ (V+)–0.6V, 15mA < I_O ≤ 30mA**	**103**			**dB**
FREQUENCY RESPONSE						
Gain-Bandwidth Product	GBW	G = 100		80		MHz
		G = 1		45		MHz
Slew Rate	SR			27		V/µs
Settling Time, 0.01%	t_S	V_S = ±15V, G = –1, 10V Step, C_L = 100pF		400		ns
0.0015% (16-bit)		V_S = ±15V, G = –1, 10V Step, C_L = 100pF		700		ns
Overload Recovery Time		G = –10		500		ns
Total Harmonic Distortion + Noise	THD+N	G = +1, f = 1kHz, V_O = $3V_{RMS}$, R_L = 600Ω		0.000015		%
				–136		dB

ELECTRICAL CHARACTERISTICS: V_S = ±2.25V to ±18V (continued)

BOLDFACE limits apply over the specified temperature range, T_A = –55°C to +125°C.
At T_A = +25°C, R_L = 10kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
Voltage Output	**V_{OUT}**	**R_L = 10kΩ, A_{OL} ≥ 114dB**	**(V–) + 0.2**		**(V+) – 0.2**	**V**
		R_L = 600Ω, A_{OL} ≥ 110dB	(V–) + 0.6		(V+) – 0.6	V
		I_O < 15mA, A_{OL} ≥ 110dB	**(V–) + 0.6**		**(V+) – 0.6**	**V**
Short-Circuit Current	I_{SC}			+30/–45		mA
Capacitive Load Drive	C_{LOAD}			See Typical Characteristics		pF
Open-Loop Output Impedance	Z_O	f = 1MHz		5		Ω
SHUTDOWN						
Shutdown Pin Input Voltage(1)		Device disabled (shutdown)	(V+) – 0.35			V
		Device enabled			(V+) – 3	V
Shutdown Pin Leakage Current				1		µA
Turn-On Time(2)				2		µs
Turn-Off Time(2)				3		µs
Shutdown Current		Shutdown (disabled)		1	20	µA
POWER SUPPLY						
Specified Voltage	V_S		±2.25		±18	V
Quiescent Current (per channel)	I_Q	I_{OUT} = 0A		3.6	4.5	mA
Over Temperature					**6**	**mA**
TEMPERATURE RANGE						
Operating Range		T_A	–55		+125	°C
Thermal Resistance						
	θ_{JA}			200		°C/W

(1) When disabled, the output assumes a high-impedance state.
(2) See Typical Characteristic curves, Figure 42 through Figure 44.



A. See datasheet for absolute maximum and minimum recommended operating conditions.
B. Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

Figure 1. OPA211-EP Wirebond Life Derating Chart

7 TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = ±18V, and R_L = 10kΩ, unless otherwise noted.

INPUT VOLTAGE NOISE DENSITY vs FREQUENCY

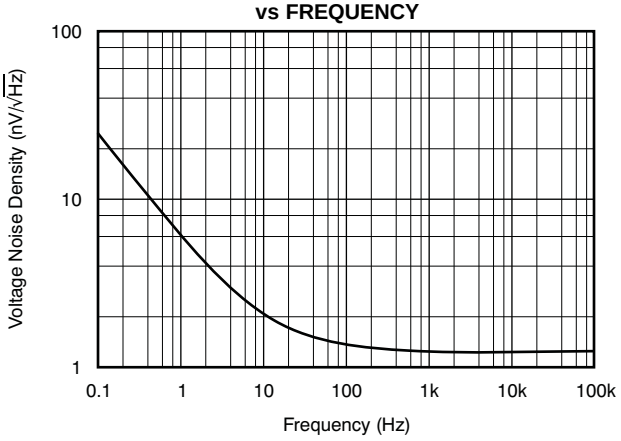


Figure 2.

INPUT CURRENT NOISE DENSITY vs FREQUENCY

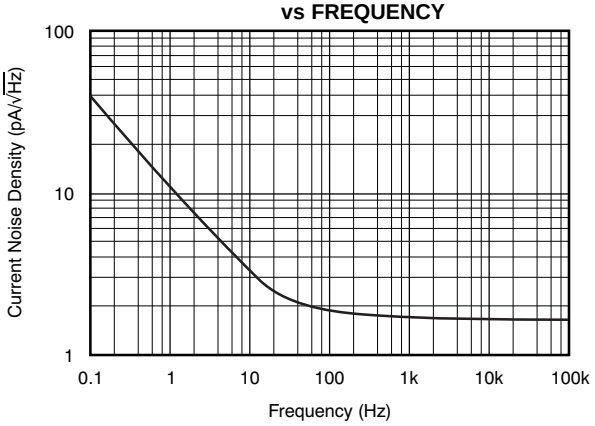


Figure 3.

THD+N RATIO vs FREQUENCY

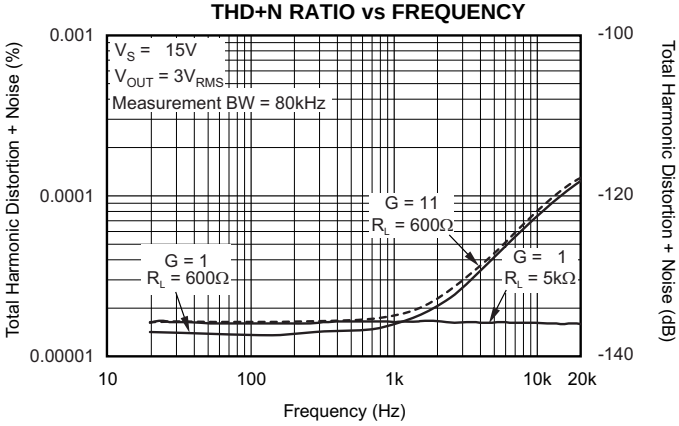


Figure 4.

THD+N RATIO vs OUTPUT VOLTAGE AMPLITUDE

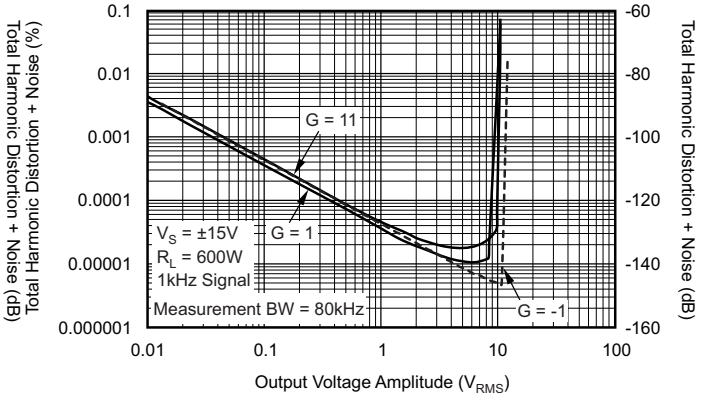


Figure 5.

THD+N RATIO vs FREQUENCY

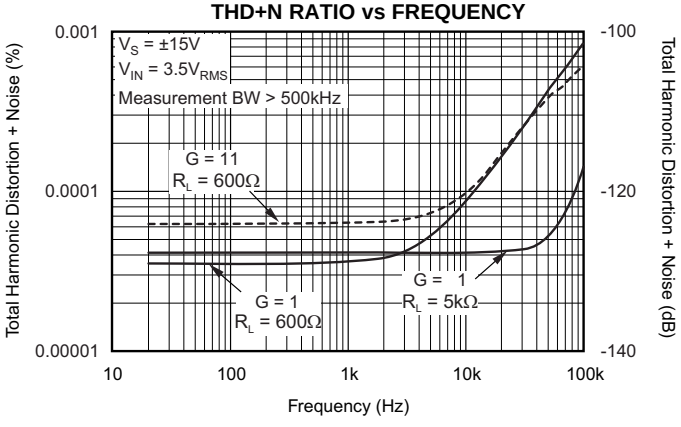


Figure 6.

CHANNEL SEPARATION vs FREQUENCY

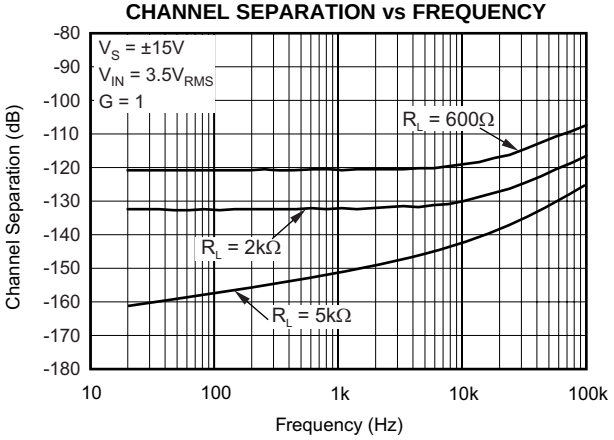


Figure 7.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±18V, and R_L = 10kΩ, unless otherwise noted.

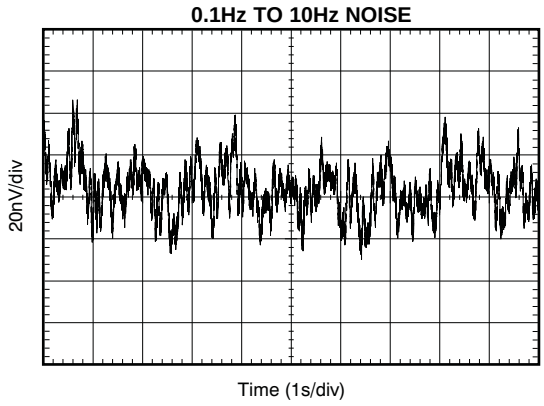


Figure 8.

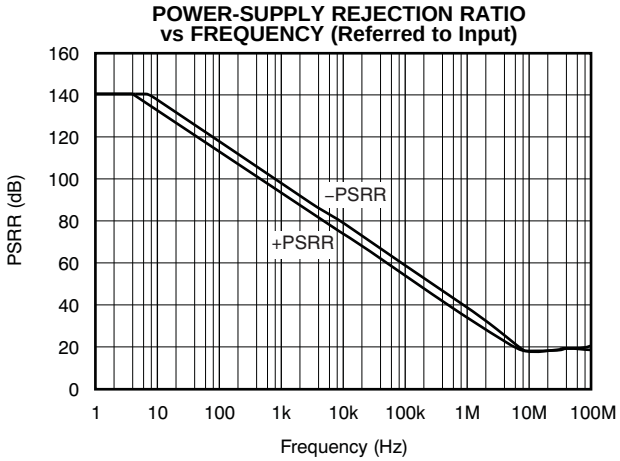


Figure 9.

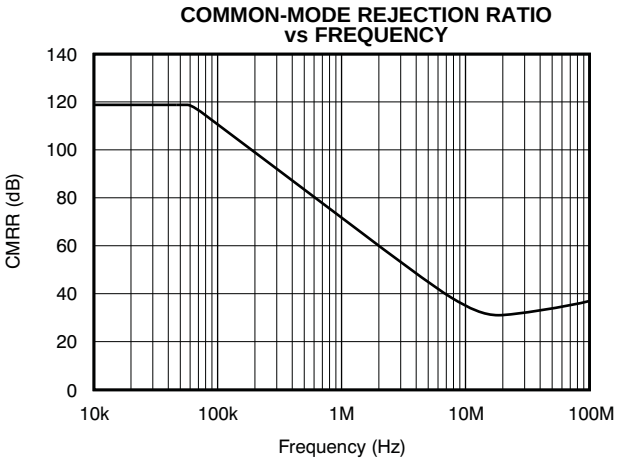


Figure 10.

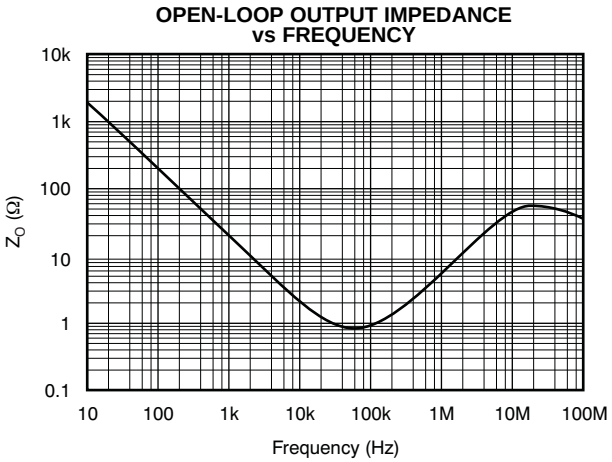


Figure 11.

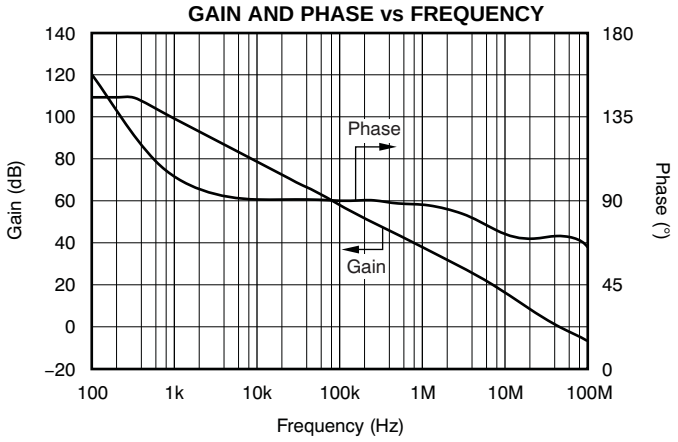


Figure 12.

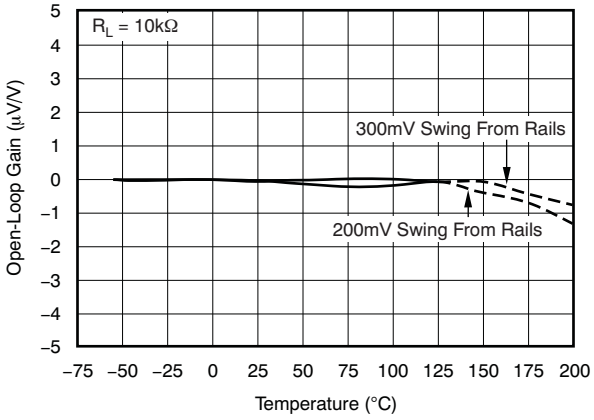


Figure 13.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±18V, and R_L = 10kΩ, unless otherwise noted.

OFFSET VOLTAGE PRODUCTION DISTRIBUTION

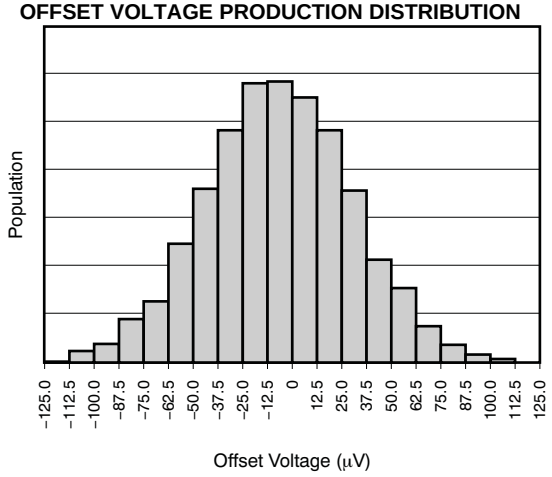


Figure 14.

OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION

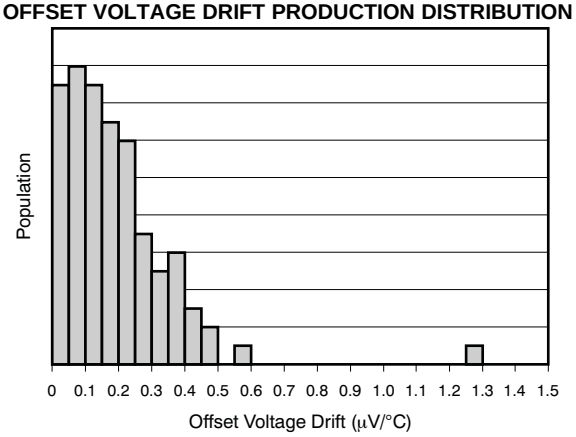


Figure 15.

I_B AND I_{OS} CURRENT vs TEMPERATURE

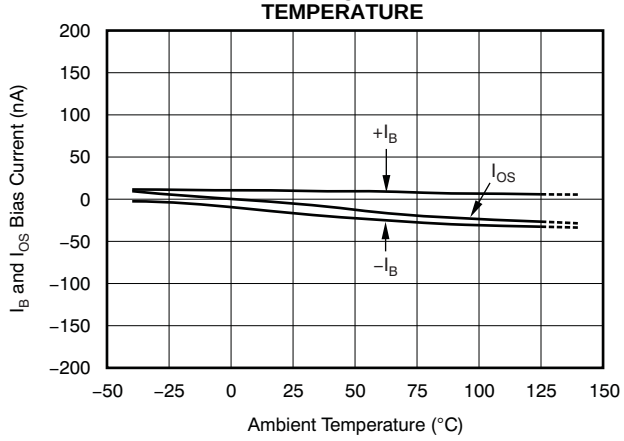


Figure 16.

OFFSET VOLTAGE vs COMMON-MODE VOLTAGE

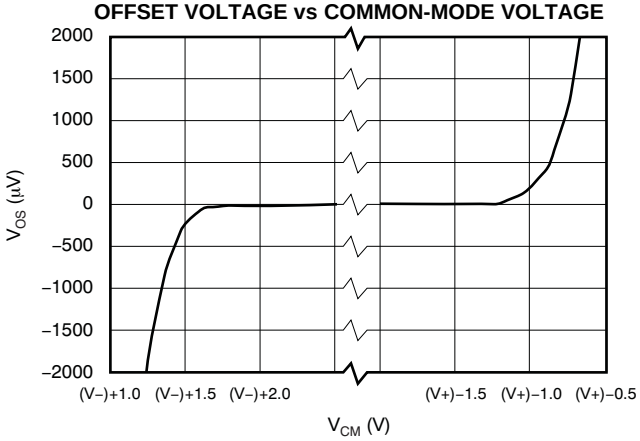


Figure 17.

V_{OS} WARMUP

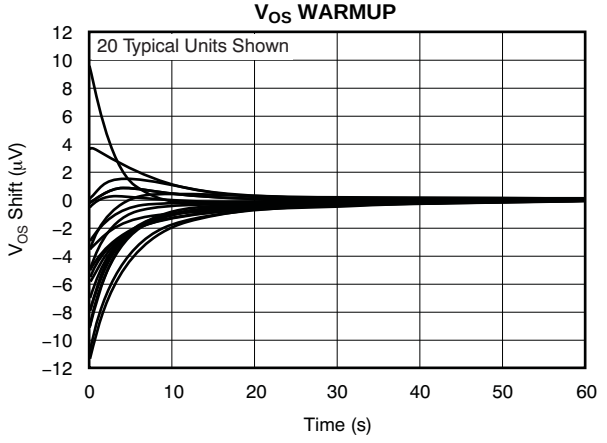


Figure 18.

INPUT OFFSET CURRENT vs SUPPLY VOLTAGE

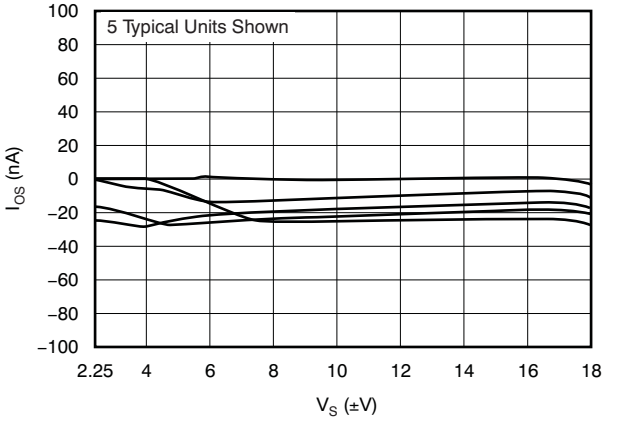


Figure 19.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±18V, and R_L = 10kΩ, unless otherwise noted.

INPUT OFFSET CURRENT vs COMMON-MODE VOLTAGE

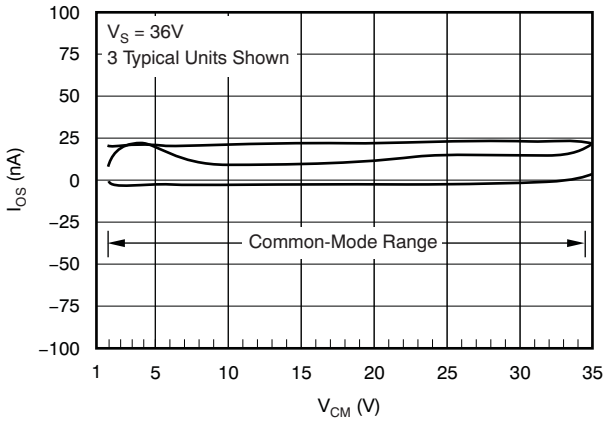


Figure 20.

INPUT BIAS CURRENT vs SUPPLY VOLTAGE

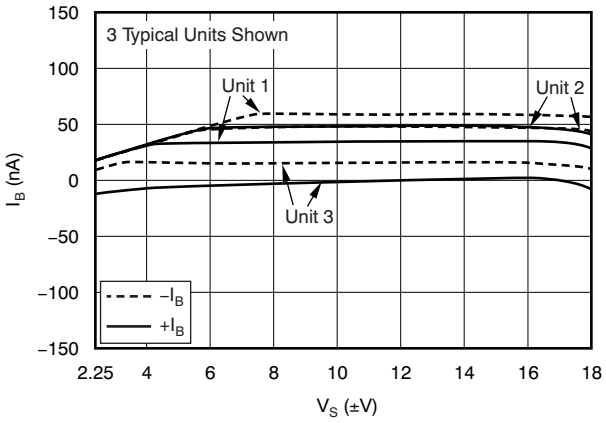


Figure 21.

INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE

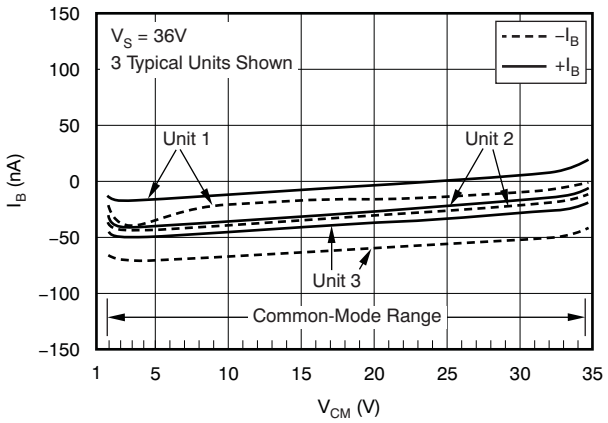


Figure 22.

QUIESCENT CURRENT vs TEMPERATURE

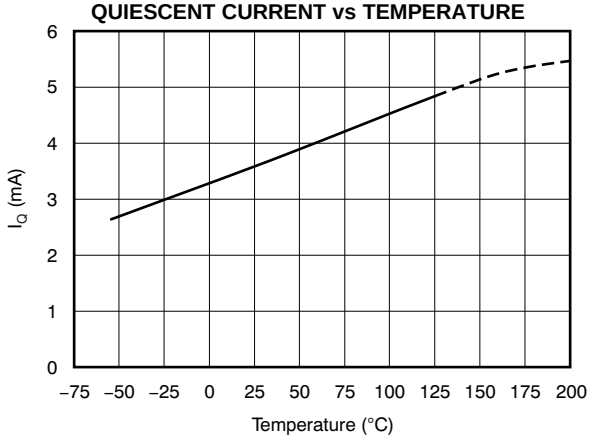


Figure 23.

QUIESCENT CURRENT vs SUPPLY VOLTAGE

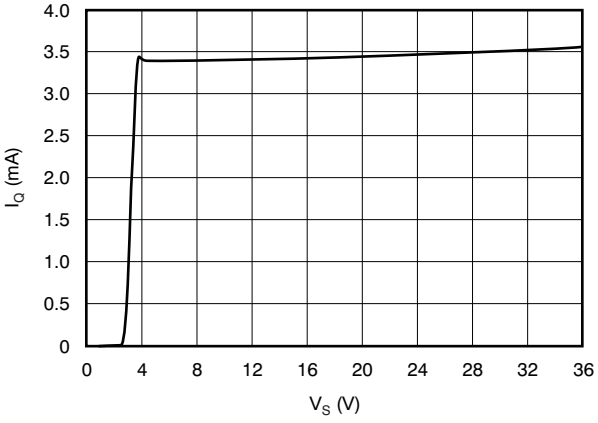


Figure 24.

NORMALIZED QUIESCENT CURRENT vs TIME

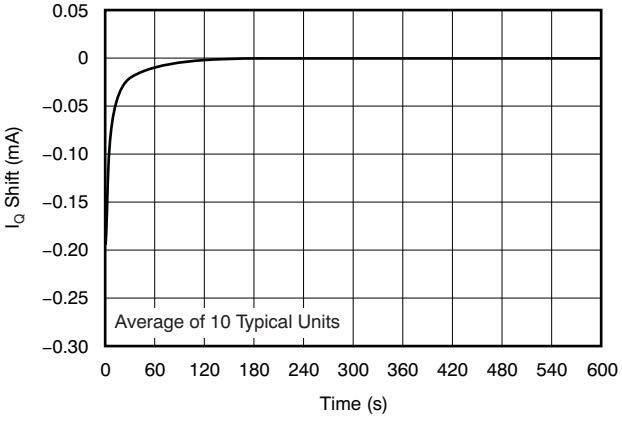


Figure 25.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±18V, and R_L = 10kΩ, unless otherwise noted.

SHORT-CIRCUIT CURRENT vs TEMPERATURE

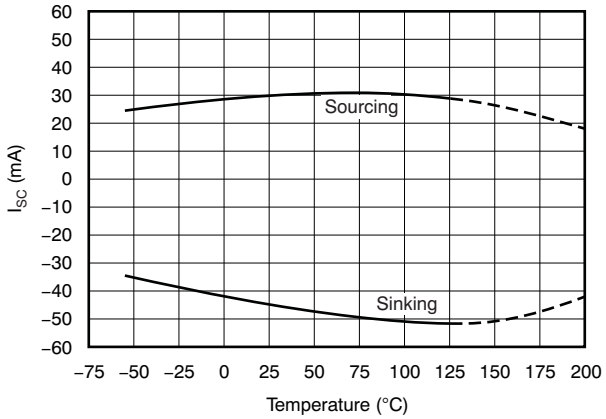


Figure 26.

SMALL-SIGNAL STEP RESPONSE (100mV)

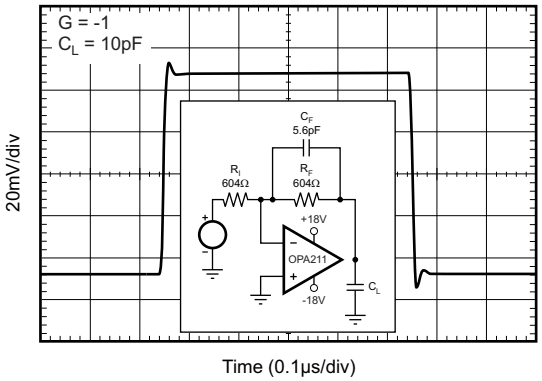


Figure 27.

SMALL-SIGNAL STEP RESPONSE (100mV)

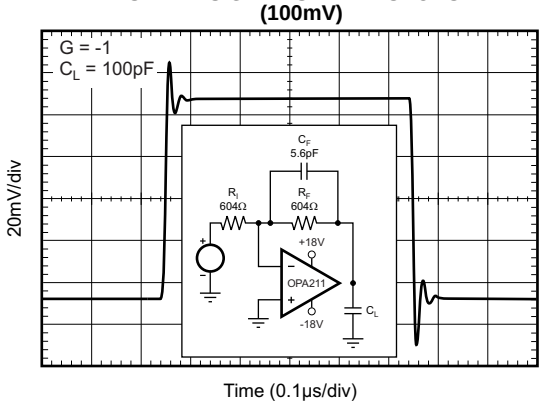


Figure 28.

SMALL-SIGNAL STEP RESPONSE (100mV)

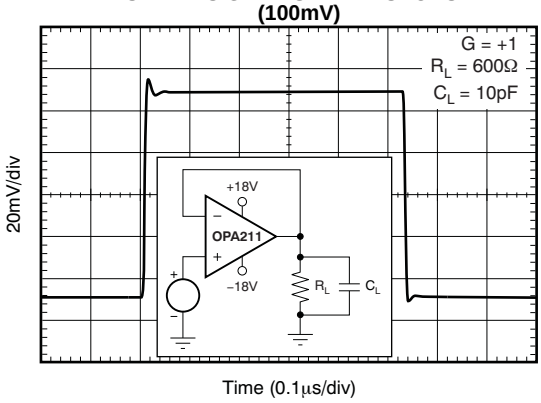


Figure 29.

SMALL-SIGNAL STEP RESPONSE (100mV)

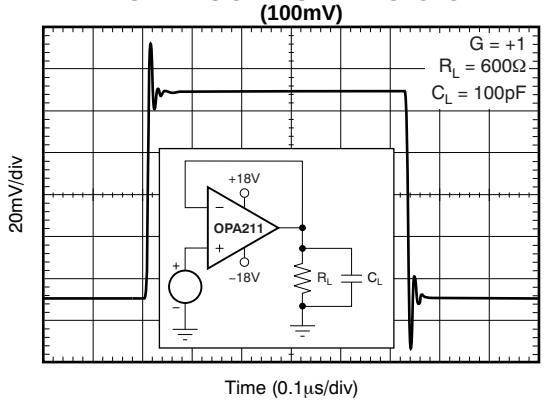


Figure 30.

SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD (100mV Output Step)

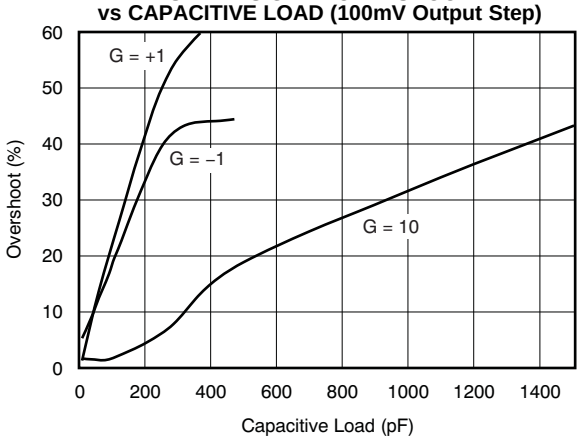


Figure 31.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±18V, and R_L = 10kΩ, unless otherwise noted.

LARGE-SIGNAL STEP RESPONSE

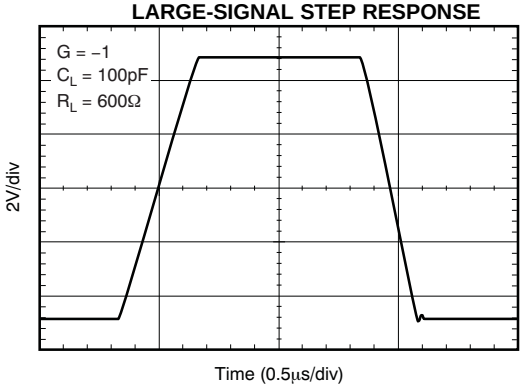


Figure 32.

LARGE-SIGNAL STEP RESPONSE

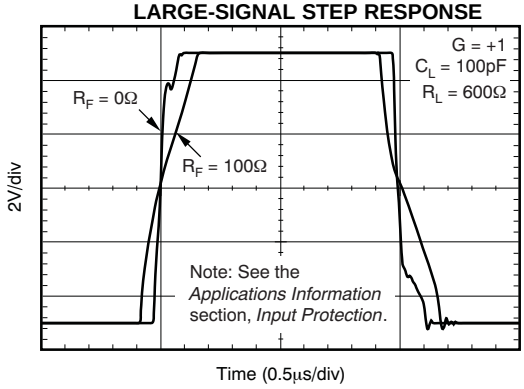


Figure 33.

LARGE-SIGNAL POSITIVE SETTLING TIME ($10V_{PP}$, C_L = 100pF)

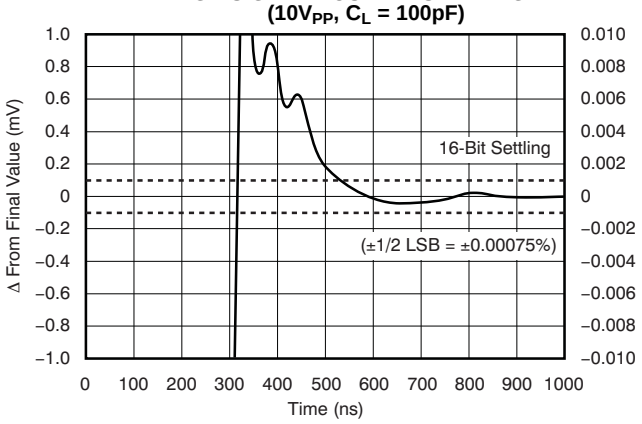


Figure 34.

LARGE-SIGNAL POSITIVE SETTLING TIME ($10V_{PP}$, C_L = 10pF)

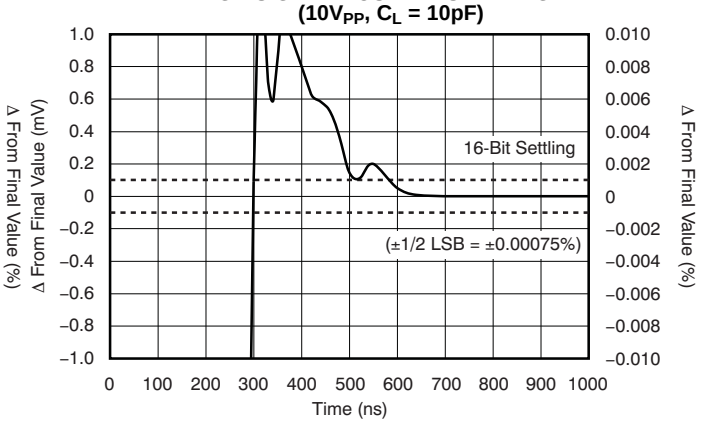


Figure 35.

LARGE-SIGNAL NEGATIVE SETTLING TIME ($10V_{PP}$, C_L = 100pF)

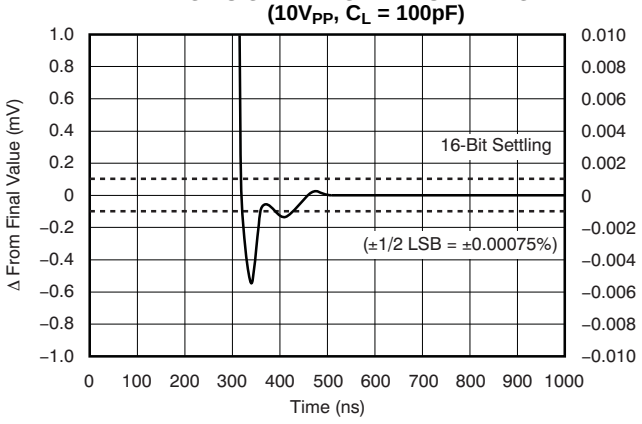


Figure 36.

LARGE-SIGNAL NEGATIVE SETTLING TIME ($10V_{PP}$, C_L = 10pF)

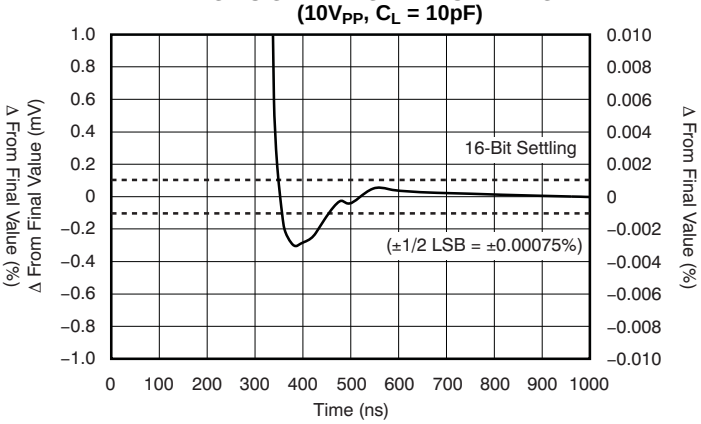


Figure 37.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±18V, and R_L = 10kΩ, unless otherwise noted.

NEGATIVE OVERLOAD RECOVERY

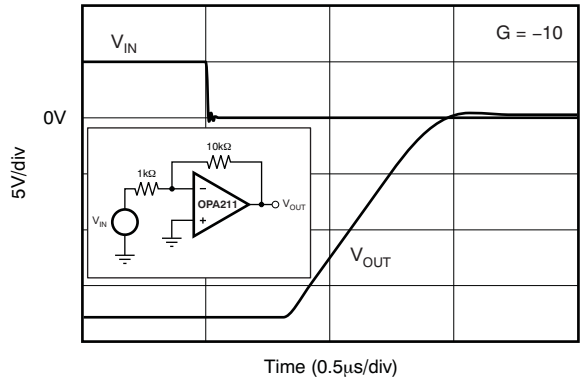


Figure 38.

POSITIVE OVERLOAD RECOVERY

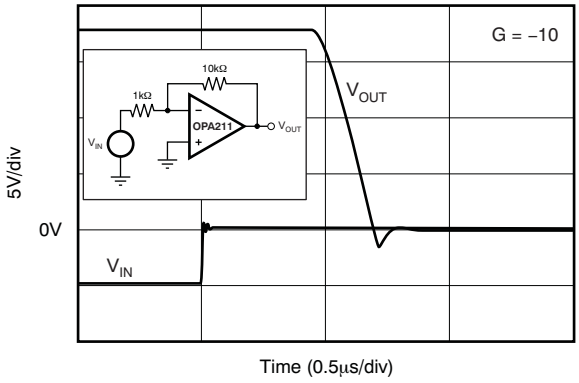


Figure 39.

OUTPUT VOLTAGE vs OUTPUT CURRENT

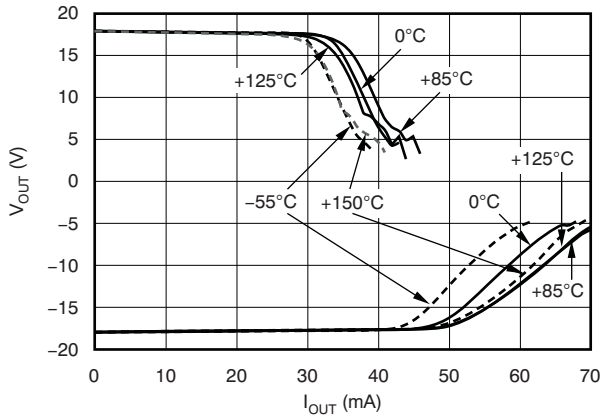


Figure 40.

NO PHASE REVERSAL

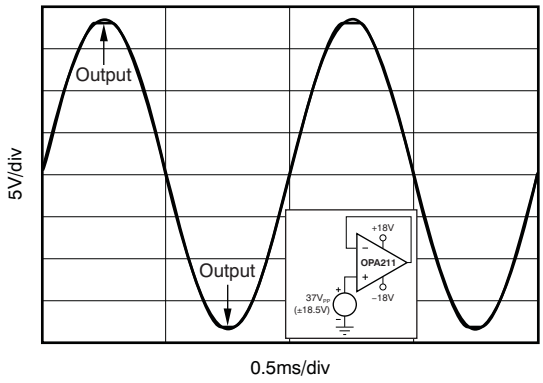


Figure 41.

TURN-OFF TRANSIENT

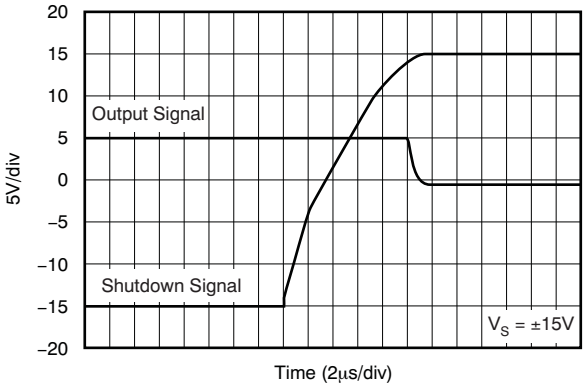


Figure 42.

TURN-ON TRANSIENT

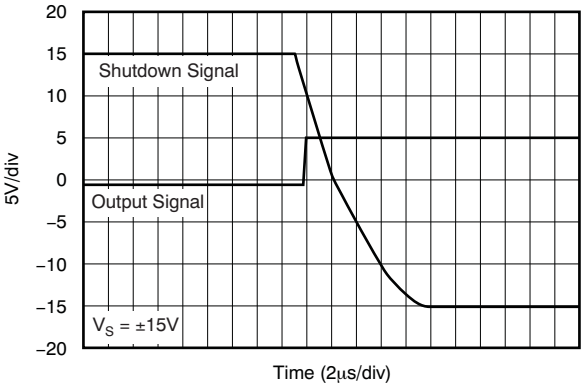


Figure 43.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±18V, and R_L = 10kΩ, unless otherwise noted.

TURN-ON/TURN-OFF TRANSIENT

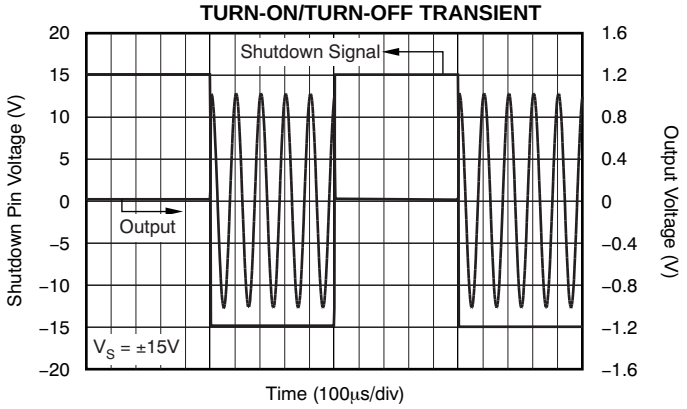


Figure 44.

8 APPLICATION INFORMATION

The OPA211 is a unity-gain stable, precision op amp with very low noise. Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1µF capacitors are adequate. Figure 45 shows a simplified schematic of the OPA211. This die uses a SiGe bipolar process and contains 180 transistors.

8.1 OPERATING VOLTAGE

OPA211 series op amps operate from ±2.25V to ±18V supplies while maintaining excellent performance. The OPA211 series can operate with as little as +4.5V between the supplies and with up to +36V between the supplies. However, some applications do not require equal positive and negative output voltage swing. With the OPA211 series, power-supply voltages do not need to be equal. For example, the positive supply could be set to +25V with the negative supply at –5V or vice-versa.

OPERATING VOLTAGE (continued)

The common-mode voltage must be maintained within the specified range. In addition, key parameters are assured over the specified temperature range, T_A = –55°C to +125°C. Parameters that vary significantly with operating voltage or temperature are shown in the Typical Characteristics.

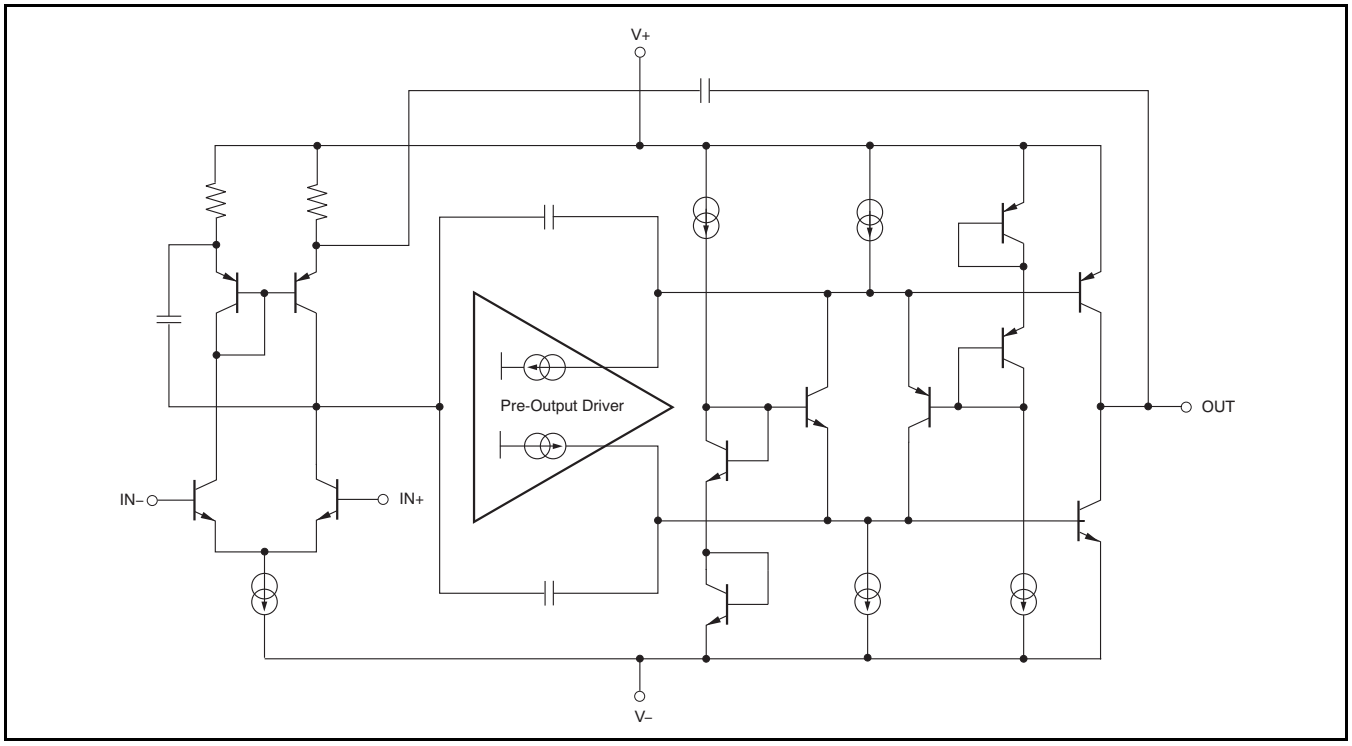


Figure 45. OPA211 Simplified Schematic

8.2 INPUT PROTECTION

The input terminals of the OPA211 are protected from excessive differential voltage with back-to-back diodes, as shown in Figure 46. In most circuit applications, the input protection circuitry has no consequence. However, in low-gain or G = 1 circuits, fast ramping input signals can forward bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. This effect is illustrated in Figure 33 of the Typical Characteristics. If the input signal is fast enough to create this forward bias condition, the input signal current must be limited to 10mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the signal input current. This input series resistor degrades the low-noise performance of the OPA211, and is discussed in the *Noise Performance* section of this data sheet. Figure 46 shows an example implementing a current-limiting feedback resistor.

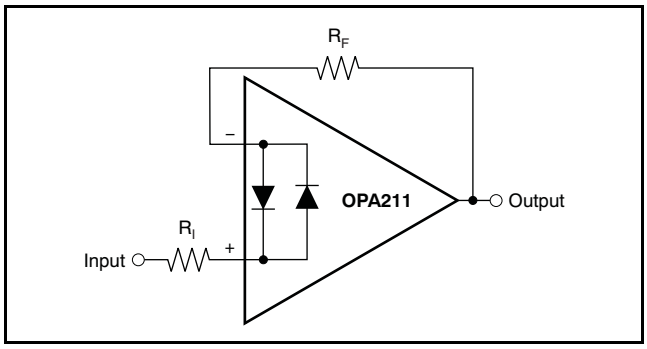


Figure 46. Pulsed Operation

8.3 NOISE PERFORMANCE

Figure 47 shows total circuit noise for varying source impedances with the op amp in a unity-gain configuration (no feedback resistor network, and therefore no additional noise contributions). Two different op amps are shown with total circuit noise calculated. The OPA211 has very low voltage noise, making it ideal for low source impedances (less than 2kΩ). A similar precision op amp, the OPA227, has somewhat higher voltage noise but lower current noise. It provides excellent noise performance at moderate source impedance (10kΩ to 100kΩ). Above 100kΩ, a FET-input op amp such as the OPA132 (very low current noise) may provide improved performance. The equation in Figure 47 is shown for the calculation of the total circuit noise. Note that e_n = voltage noise, I_n = current noise, R_S = source impedance, k = Boltzmann's constant = 1.38×10^{-23} J/K, and T is temperature in K.

NOISE PERFORMANCE (continued)

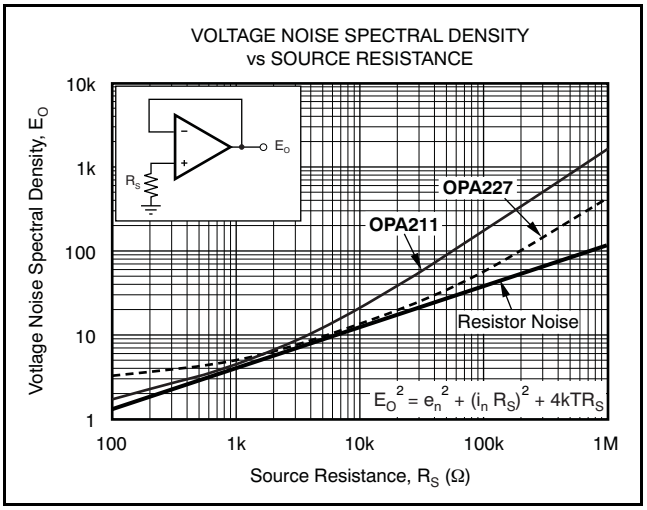


Figure 47. Noise Performance of the OPA211 and OPA227 in Unity-Gain Buffer Configuration

8.4 BASIC NOISE CALCULATIONS

Design of low-noise op amp circuits requires careful consideration of a variety of possible noise contributors: noise from the signal source, noise generated in the op amp, and noise from the feedback network resistors. The total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. This function is plotted in Figure 47. The source impedance is usually fixed; consequently, select the op amp and the feedback resistors to minimize the respective contributions to the total noise.

Figure 47 depicts total noise for varying source impedances with the op amp in a unity-gain configuration (no feedback resistor network, and therefore no additional noise contributions). The operational amplifier itself contributes both a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. Therefore, the lowest noise op amp for a given application depends on the source impedance. For low source impedance, current noise is negligible and voltage noise generally dominates. For high source impedance, current noise may dominate.

BASIC NOISE CALCULATIONS (continued)

Figure 48 illustrates both inverting and noninverting op amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. The current noise of the op amp reacts with the feedback resistors to create additional noise components. The feedback resistor values can generally be chosen to make these noise sources negligible. The equations for total noise are shown for both configurations.

8.5 TOTAL HARMONIC DISTORTION MEASUREMENTS

OPA211 series op amps have excellent distortion characteristics. THD + Noise is below 0.0002% (G = +1, V_{OUT} = $3V_{RMS}$) throughout the audio frequency range, 20Hz to 20kHz, with a 600Ω load.

The distortion produced by OPA211 series op amps is below the measurement limit of many commercially available distortion analyzers. However, a special test circuit illustrated in Figure 49 can be used to extend the measurement capabilities.

Op amp distortion can be considered an internal error source that can be referred to the input. Figure 49 shows a circuit that causes the op amp distortion to be 101 times greater than that normally produced by the op amp. The addition of R_3 to the otherwise standard noninverting amplifier configuration alters the feedback factor or noise gain of the circuit. The closed-loop gain is unchanged, but the feedback available for error correction is reduced by a factor of

TOTAL HARMONIC DISTORTION MEASUREMENTS (continued)

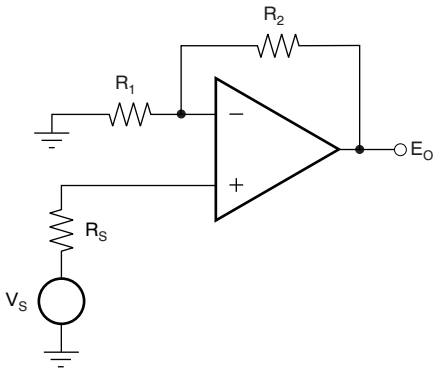
101, thus extending the resolution by 101. Note that the input signal and load applied to the op amp are the same as with conventional feedback without R_3. The value of R_3 should be kept small to minimize its effect on the distortion measurements.

Validity of this technique can be verified by duplicating measurements at high gain and/or high frequency where the distortion is within the measurement capability of the test equipment. Measurements for this data sheet were made with an Audio Precision System Two distortion/noise analyzer, which greatly simplifies such repetitive measurements. The measurement technique can, however, be performed with manual distortion measurement instruments.

8.6 SHUTDOWN

The shutdown (enable) function of the OPA211 is referenced to the positive supply voltage of the operational amplifier. A valid high disables the op amp. A valid high is defined as (V+) – 0.35V of the positive supply applied to the shutdown pin. A valid low is defined as (V+) – 3V below the positive supply pin. For example, with V_{CC} at ±15V, the device is enabled at or below 12V. The device is disabled at or above 14.65V. If dual or split power supplies are used, care should be taken to ensure the valid high or valid low input signals are properly referred to the positive supply voltage. This pin must be connected to a valid high or low voltage or driven, and not left open-circuit. The enable and disable times are provided in the Typical Characteristics section (see Figure 42 through Figure 44). When disabled, the output assumes a high-impedance state.

Noise in Noninverting Gain Configuration



Noise at the output:

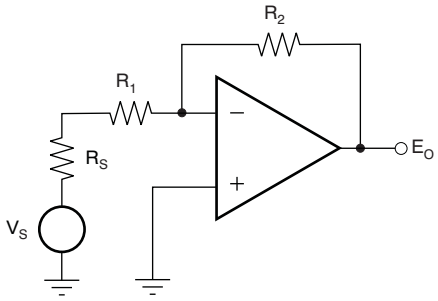
$$E_O^2 = \left(1 + \frac{R_2}{R_1}\right)^2 e_n^2 + e_1^2 + e_2^2 + (i_n R_2)^2 + e_S^2 + (i_n R_S)^2 \left(1 + \frac{R_2}{R_1}\right)^2$$

Where $e_S = \sqrt{4kTR_S} \times \left(1 + \frac{R_2}{R_1}\right)$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1} \times \left(\frac{R_2}{R_1}\right)$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

Noise in Inverting Gain Configuration



Noise at the output:

$$E_O^2 = \left(1 + \frac{R_2}{R_1 + R_S}\right)^2 e_n^2 + e_1^2 + e_2^2 + (i_n R_2)^2 + e_S^2$$

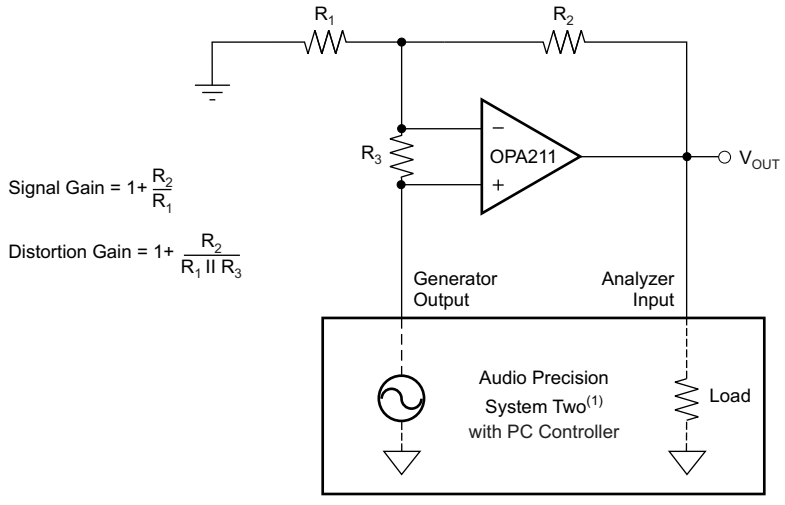
Where $e_S = \sqrt{4kTR_S} \times \left(\frac{R_2}{R_1 + R_S}\right)$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1} \times \left(\frac{R_2}{R_1 + R_S}\right)$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

For the OPA211 series op amps at 1kHz, $e_n = 1.1nV/\sqrt{Hz}$ and $i_n = 1.7pA/\sqrt{Hz}$.

Figure 48. Noise Calculation in Gain Configurations



SIG. GAIN	DIST. GAIN	R_1	R_2	R_3
1	101	∞	1kΩ	10Ω
11	101	100Ω	1kΩ	11Ω

(1) For measurement bandwidth, see Figure 4, Figure 5, and Figure 6.

Figure 49. Distortion Test Circuit

8.7 ELECTRICAL OVERSTRESS

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

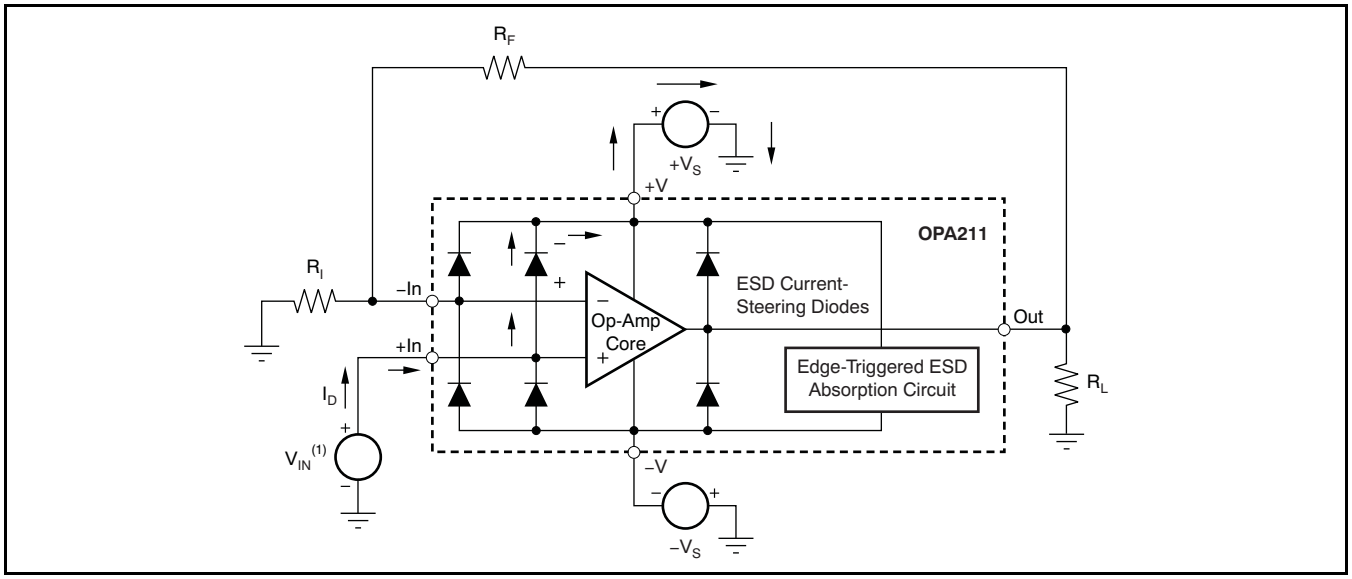
It is helpful to have a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event. Figure 50 illustrates the ESD circuits contained in the OPA211 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where they meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

ELECTRICAL OVERSTRESS (continued)

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more of the amplifier device pins, current flows through one or more of the steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPA211 but below the device breakdown voltage level. Once this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit such as that illustrated in Figure 50, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. Should this condition occur, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through steering diode paths and rarely involves the absorption device.



(1) $V_{IN} = +V_S + 500mV$.

Figure 50. Equivalent Internal ESD Circuitry and Its Relation to a Typical Circuit Application

Figure 50 depicts a specific example where the input voltage, V_{IN}, exceeds the positive supply voltage ($+V_S$) by 500mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the datasheet specifications recommend that applications limit the input current to 10mA.

If the supply is not capable of sinking the current, V_{IN} may begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings. In extreme but rare cases, the absorption device triggers on while $+V_S$ and $–V_S$ are applied. If this event happens, a direct current path is established between the $+V_S$ and $–V_S$ supplies. The power dissipation of the absorption device is quickly exceeded, and the extreme internal heating destroys the operational amplifier.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies $+V_S$ and/or $–V_S$ are at 0V. Again, it depends on the supply characteristic while at 0V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current may be supplied by the input source via the current steering diodes. This state is not a normal bias condition; the amplifier most likely will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

8.8 THERMAL CONSIDERATIONS

The primary issue with all semiconductor devices is junction temperature (T_J). The most obvious consideration is assuring that T_J never exceeds the absolute maximum rating specified for the device. However, addressing device thermal dissipation has benefits beyond protecting the device from damage. Even modest increases in junction temperature can decrease op amp performance, and temperature-related errors can accumulate. Understanding the power generated by the device within the specific application and assessing the thermal effects on the error tolerance lead to a better understanding of system performance and thermal dissipation needs.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA211MDGKTEP	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	OBCM
V62/12619-01XE	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	OBCM

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF OPA211-EP :

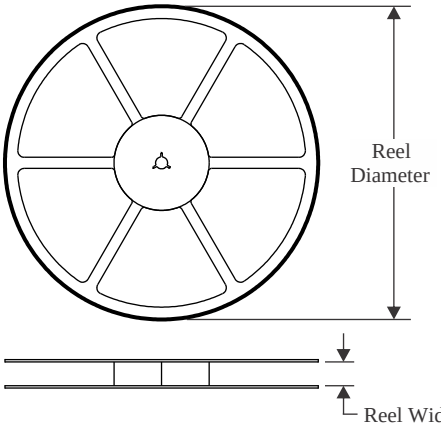
- Catalog : OPA211

NOTE: Qualified Version Definitions:

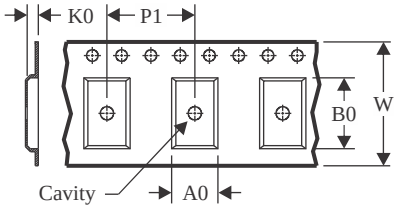
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

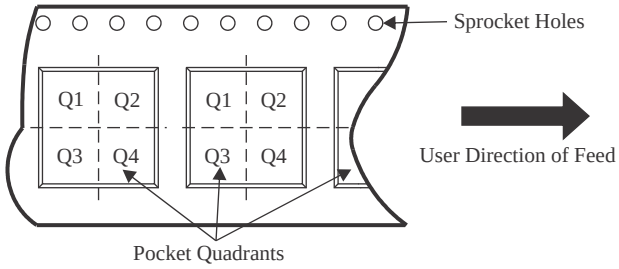


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

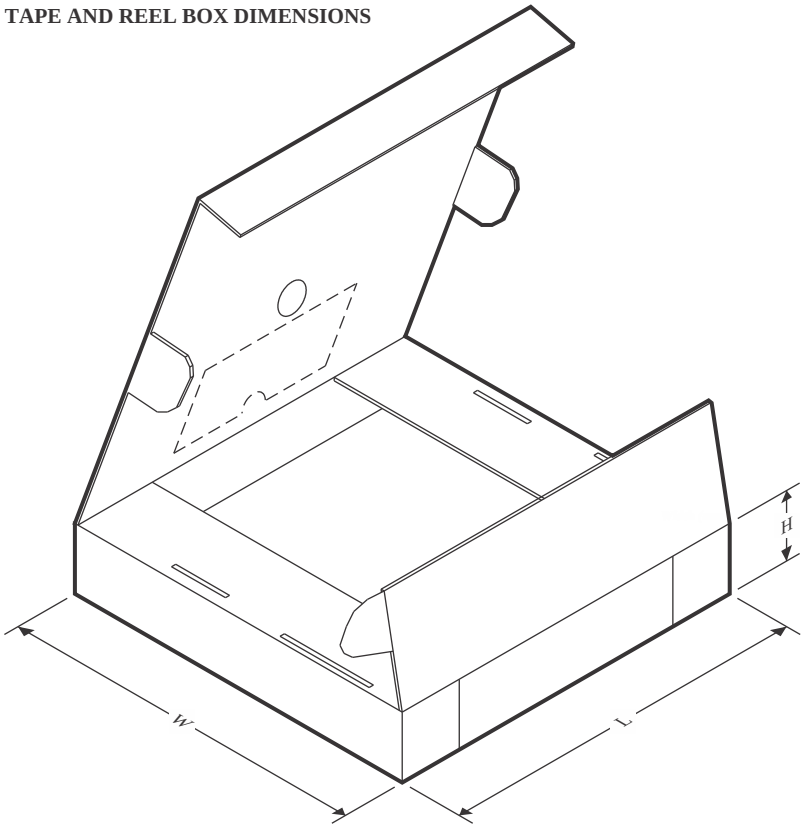
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA211MDGKTEP	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

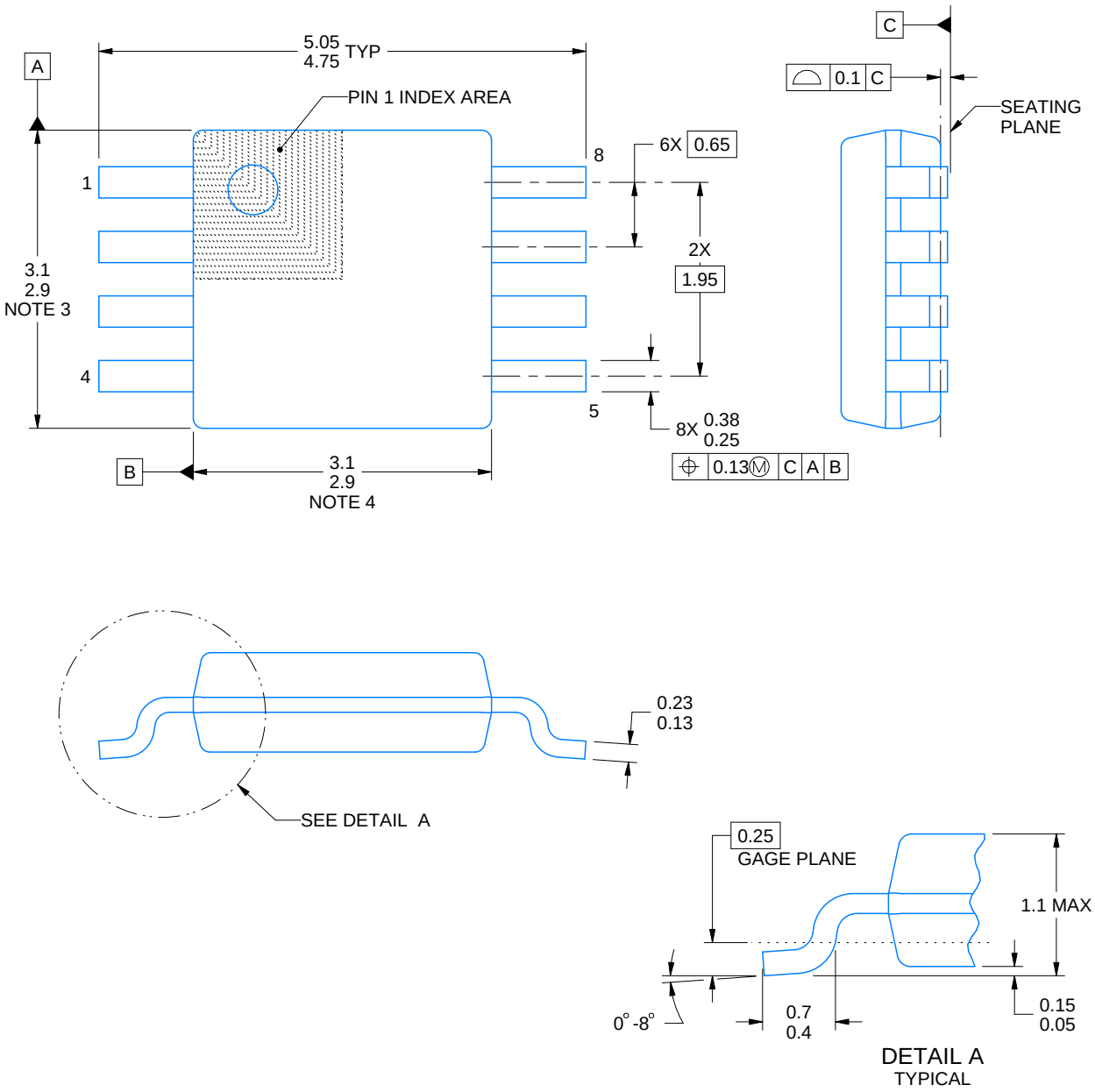
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA211MDGKTEP	VSSOP	DGK	8	250	353.0	353.0	32.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

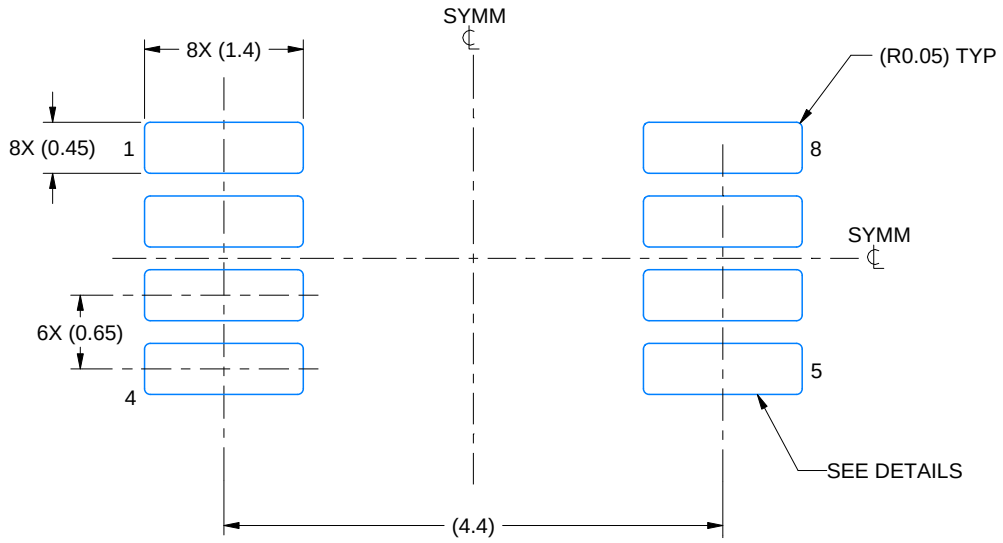
SMALL OUTLINE PACKAGE



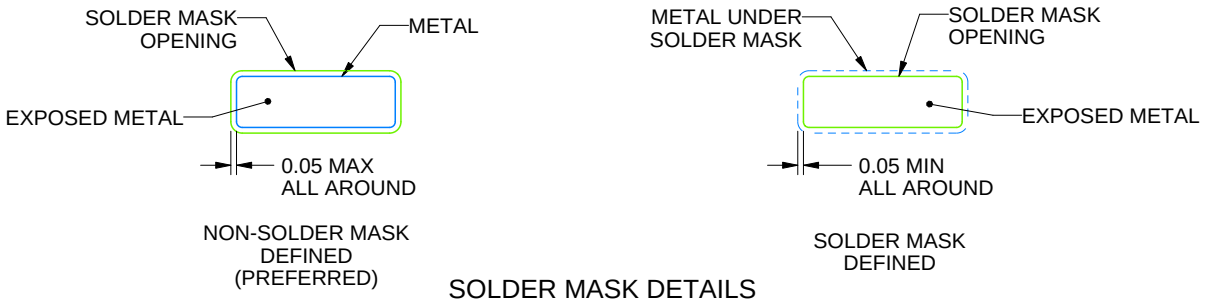
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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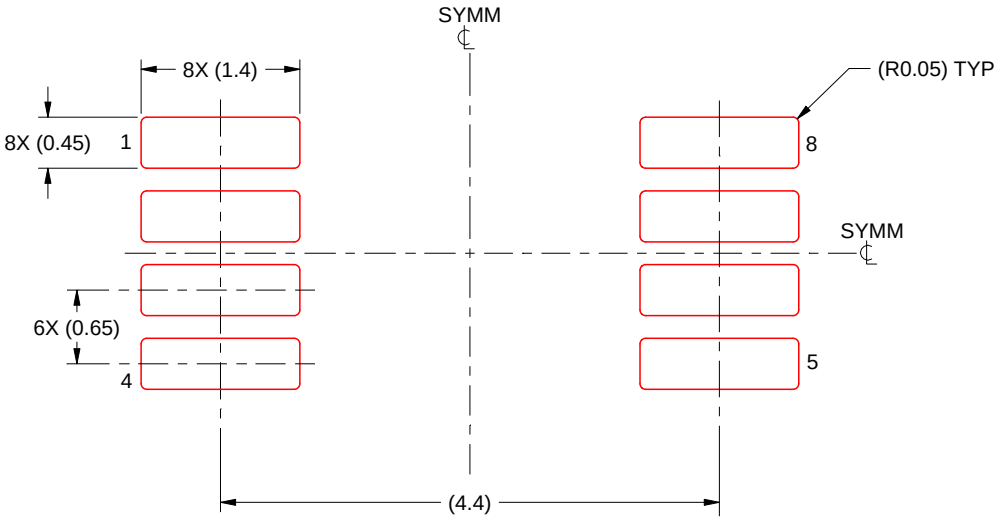
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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