MSPM0G350x-Q1 Automotive Mixed-Signal MicrocontrollersWith CAN-FD Interface

1 Features

- **Core**
  - Arm® 32-bit Cortex®-M0+ CPU with memory protection unit, frequency up to 80MHz
- Functional Safety-Compliant
  - Developed for functional safety applications
  - Documentation available to aid ISO 26262 system design
  - Systematic capability up to ASIL B
  - Hardware integrity up to ASIL B
- Safety-related certification
  - ISO 26262 certified up to ASIL B by TÜV
- **Operating characteristics**
  - Extended temperature: –40°C up to 125°C
  - Wide supply voltage range: 1.62V to 3.6V
- **Memories**
  - Up to 128KB of flash memory with error correction code (ECC)
  - Up to 32KB of SRAM with hardware parity
- **High-performance analog peripherals**
  - Two simultaneous sampling 12-bit 4Msps analog-to-digital converters (ADCs) with up to 17 external channels
    - 14-bit effective resolution at 250ksps with hardware averaging
  - One 12-bit 1Msps digital-to-analog converter with integrated output buffer (DAC)
  - Two zero-drift zero-crossover chopper op-amps (OPA)
    - 0.5µV/°C drift with chopping
    - Integrated programmable gain stage, up to 32x
  - One general-purpose amplifier (GPAMP)
  - Three high-speed comparators (COMP) with 8-bit reference DACs
    - 32ns propagation delay in high-speed mode
    - Support low-power mode operation down to 1µA
  - Programmable analog connections between ADC, OPAs, GPAMP, COMP and DAC
  - Configurable 1.4V or 2.5V internal shared voltage reference (VREF)
  - Integrated temperature sensor
- **Optimized low-power modes**
  - RUN: 101µA/MHz (CoreMark)
  - SLEEP: 40µA/MHz
  - STOP: 190µA at 4MHz
  - STANDBY: 1.5µA with 32KHz LFXT, RTC with SRAM, CPU state, and registers retained
  - SHUTDOWN: 80nA with IO retained and IO wake-up capability
- **Intelligent digital peripherals**
  - 7-channel DMA controller
  - Math accelerator supports DIV, SQRT, MAC and TRIG computations
  - Seven timers supporting up to 22 PWM channels
    - One 16-bit general-purpose timer supports QEI
    - Two 16-bit general-purpose timers support low-power operation in STANDBY mode
    - One 32-bit general-purpose timer
    - Two 16-bit advanced timers with deadband support and complementary outputs up to 12 PWM channels
  - Two window-watchdog timers (WWDT)
  - RTC with alarm and calendar mode
- **Enhanced communication interfaces**
  - Four UART interfaces
    - One supports LIN, IrDA, DALI, Smart Card, Manchester
    - Three support low-power operation in STANDBY mode
  - Two I^2C interfaces supporting FM+ (1Mbit/s), SMBus/PMBus, and wakeup from STOP mode
  - Two SPIs, one SPI supports up to 32Mbits/s
  - One Controller Area Network (CAN) interface supports CAN 2.0 A or B and CAN-FD
- **Clock system**
  - Internal 4MHz to 32MHz oscillator (SYSOSC) with up to ±1.2% accuracy (SYSOSC)
  - Phase-locked loop (PLL) up to 80MHz
  - Internal 32kHz low-frequency oscillator (LFOSC) with ±3% accuracy
  - External 4MHz to 48MHz crystal oscillator (HFXT)
  - External 32kHz crystal oscillator(LFXT)
  - External clock input
- **Data integrity and encryption**
  - Cyclic redundancy checker (CRC-16, CRC-32)
  - True random number generator (TRNG)
  - AES encryption with 128-bit or 256-bit key
- **Flexible I/O features**
  - Up to 60 GPIOs
    - Two 5V-tolerant open drain IOs
    - Two high-drive IOs with 20mA drive strength
    - Up to 5 high speed IOs
- **Development support**
  - 2-pin serial wire debug (SWD)
- **Package options**

- 64-pin LQFP (PM) (0.5mm pitch)
- 48-pin LQFP (PT) (0.5mm pitch)
- 48-pin VQFN (RGZ) (0.5mm pitch)
- 32-pin VQFN (RHB) (0.5mm pitch)
- 32-pin VSSOP (32DGS) (0.5mm pitch)
- 28-pin VSSOP (28DGS) (0.5mm pitch)

- **Family members** (also see *Device Comparison*)
  - MSPM0G3505: 32KB flash, 16KB RAM
  - MSPM0G3506: 64KB flash, 32KB RAM
  - MSPM0G3507: 128KB flash, 32KB RAM
- **Development kits and software** (also see *Tools and Software*)
  - LP-MSPM0G3507 LaunchPad™ development kit
  - MSPM0 Software Development Kit (SDK)
- **Automotive qualification**
  - AEC-Q100 Grade 1
  - 32- and 48-pin QFN with wettable flanks option

2 Applications

- Automotive body electronics and Lighting
- Automotive Gateway
- Steering Wheel Systems
- Automotive Motor Control
- DC to AC Inverters
- Automotive Interior Lighting
- Door handle modules
- Kick to open modules
- Vehicle Occupancy Detection
- Seat Comfort Module

3 Description

MSPM0G350x microcontrollers (MCUs) are part of the MSP highly integrated, ultra-low-power 32-bit MCU family based on the enhanced Arm® Cortex®-M0+ 32-bit core platform operating at up to 80MHz frequency. These cost-optimized MCUs offer high-performance analog peripheral integration, support extended temperature ranges from -40°C to 125°C, and operate with supply voltages ranging from 1.62V to 3.6V.

The MSPM0G350x devices provide up to 128KB embedded flash program memory with built-in error correction code (ECC) and up to 32KB SRAM with hardware parity option. These MCUs also incorporate a memory protection unit, 7-channel DMA, math accelerator, and a variety of high-performance analog peripherals such as two 12-bit 4-Msps ADCs, configurable internal shared voltage reference, one 12-bit 1-Msps DAC, three high speed comparators with built-in reference DACs, two zero-drift zero-crossover op-amps with programmable gain, and one general-purpose amplifier. These devices also offer intelligent digital peripherals such as two 16-bit advanced control timers, five general-purpose timers (with one 16-bit general-purpose timer for QEI interface, two 16-bit general-purpose timers for STANDBY mode, and one 32-bit general-purpose timer), two windowed-watchdog timers, and one RTC with alarm and calendar modes. These devices provide data integrity and encryption peripherals (AES, CRC, TRNG) and enhanced communication interfaces (four UART, two I2C, two SPI, and CAN 2.0/FD).

The TI MSPM0 family of low-power MCUs consists of devices with varying degrees of analog and digital integration that allow customers to find the MCU that meets project needs. The MSPM0 MCU platform combines the Arm Cortex-M0+ platform with a holistic ultra-low-power system architecture, allowing system designers to increase performance while reducing energy consumption.

MSPM0G350x MCUs are supported by an extensive hardware and software ecosystem with reference designs and code examples to get the design started quickly. Development kits available for purchase include a LaunchPad™ development kit. TI also provides a free MSP Software Development Kit (SDK), which is available as a component of Code Composer Studio™ IDE desktop and cloud version within the TI Resource Explorer. MSPM0 MCUs are also supported by extensive online collateral, training with MSP Academy, and online support through the TI E2E™ support forums.

For complete module descriptions, see the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

Table 3-1. Device Comparison

DEVICE NAME	PACKAGE	PACKAGE SIZE
M0G3505QPMRQ1	64 LQFP	12mm × 12mm
M0G3506QPMRQ1		
M0G3507QPMRQ1		
M0G3505QPTRQ1	48 LQFP	9mm × 9mm
M0G3506QPTRQ1		
M0G3507QPTRQ1		
M0G3505QRGZRQ1	48 VQFN	7mm × 7mm
M0G3506QRGZRQ1		
M0G3507QRGZRQ1		
M0G3505QRHBRQ1	32 VQFN	5mm × 5mm
M0G3506QRHBRQ1		
M0G3507QRHBRQ1		

Table 3-1. Device Comparison (continued)

DEVICE NAME	PACKAGE	PACKAGE SIZE
M0G3505QDGS32RQ1	32 VSSOP	8.1mm × 4.9mm
M0G3506QDGS32RQ1		
M0G3507QDGS32RQ1		
M0G3505QDGS28RQ1	28 VSSOP	7.1mm × 3mm
M0G3506QDGS28RQ1		
M0G3507QDGS28RQ1		

CAUTION

System-level ESD protection must be applied in compliance with the device-level ESD specification to prevent electrical overstress or disturbing of data or code memory. See *MSP430™ System-Level ESD Considerations* for more information. The principles in this application note are applicable to MSPM0 MCUs.

4 Functional Block Diagram

Figure 4-1 shows the MSPM0G350x functional block diagram.

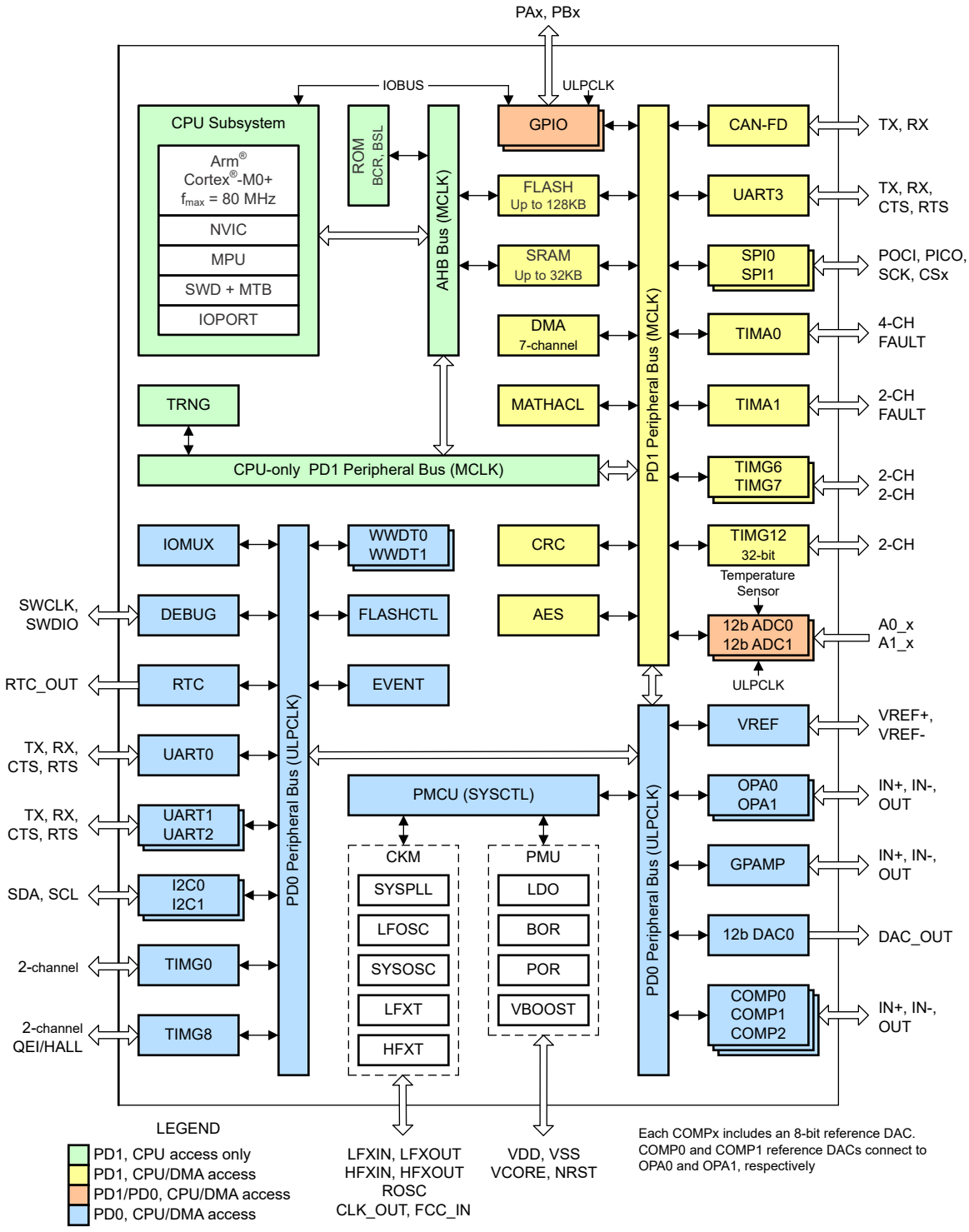

Figure 4-1. MSPM0G350x Functional Block Diagram

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5 Device Comparison

The following table summarizes the features of each device that is described in this data sheet.

Table 5-1. Device Comparison

DEVICE NAME (1) (4)	FLASH /SRAM (KB)	QUAL(2)	MATH ACCEL	ADC / CHAN	COMP	DAC	OPA	GPAMP	UART/I2C/SPI	CAN	TIMA	TIMG	GPIO	PACKAGE [PACKAGE SIZE] (3)
M0G3505QPMRQ1	32 / 16	Q	Y	2 / 17	3	1	2	1	4 / 2 / 2	1	2	5	60	64 LQFP [12mm × 12mm]
M0G3506QPMRQ1	64 / 32													
M0G3507QPMRQ1	128 / 32													
M0G3505QPTRQ1	32 / 16	Q	Y	2 / 16	3	1	2	1	4 / 2 / 2	1	2	5	44	48 LQFP [9mm × 9mm]
M0G3506QPTRQ1	64 / 32													
M0G3507QPTRQ1	128 / 32													
M0G3505QRGZRQ1	32 / 16	Q	Y	2 / 16	3	1	2	1	4 / 2 / 2	1	2	5	44	48 VQFN [7mm × 7mm](5)
M0G3506QRGZRQ1	64 / 32													
M0G3507QRGZRQ1	128 / 32													
M0G3505QRHBRQ1	32 / 16	Q	Y	2 / 11	3 (6)	1	2	1	4 / 2 / 2	1	2	5	28	32 VQFN [5mm × 5mm](5)
M0G3506QRHBRQ1	64 / 32													
M0G3507QRHBRQ1	128 / 32													
M0G3505QDGS32RQ1	32 / 16	Q	Y	2 / 11	3	1	2	1	4 / 2 / 2	1	2	5	28	32 VSSOP [8.1mm × 4.9mm]
M0G3506QDGS32RQ1	64 / 32													
M0G3507QDGS32RQ1	128 / 32													
M0G3505QDGS28RQ1	32 / 16	Q	Y	2 / 11	3 (6)	1	2	1	4 / 2 / 2	1	2	5	24	28 VSSOP [7.1mm × 3mm]
M0G3506QDGS28RQ1	64 / 32													
M0G3507QDGS28RQ1	128 / 32													

(1) For the most current part, package, and ordering information for all available devices, see the *Package Option Addendum* in Section 12, or see the TI website.
(2) Device Qualifications:
- Q = –40°C to 125°C, AEC-Q100 qualified

(3) The package size (length × width) is a nominal value and includes pins, where applicable. For the package dimensions with tolerances, see Section 12.
(4) For more information about the device name, see Section 10.2
(5) 32-pin and 48-pin VQFN packages are available with wettable flanks.
(6) Utilize the internal 8-bit DAC on COMP2 to make use of both IN channels

6 Pin Configuration and Functions

The System Configuration tool provides a graphical interface to enable, configurable, and generate initialization code for pin multiplexing and simplifying pin settings. The following pin diagrams show the primary peripheral functions, some of the integrated device features, and available clock signals to simplify the device pinout. For full descriptions of the pin functions, see the *Pin Attributes* and *Signal Descriptions* sections.

6.1 Pin Diagrams

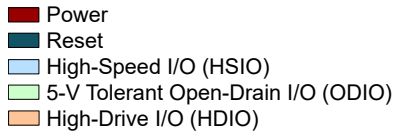


Figure 6-1. Pin Diagram Color Coding

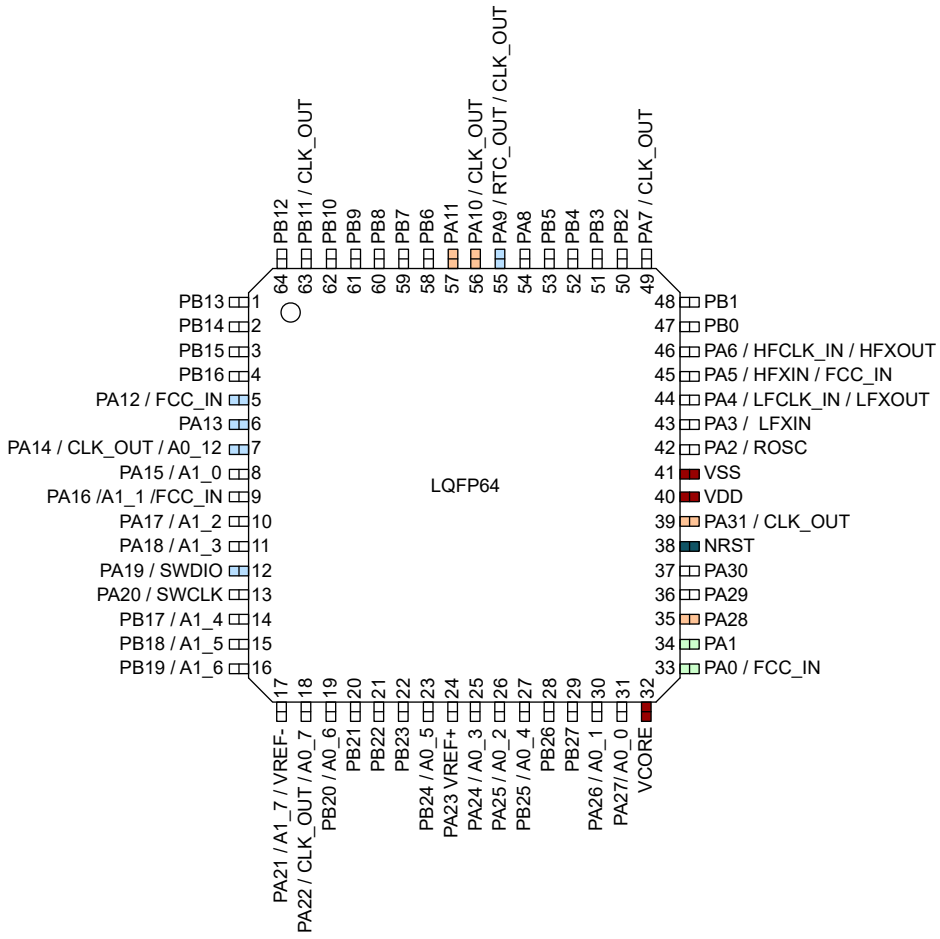


Figure 6-2. 64-Pin PM (LQFP) (Top View)

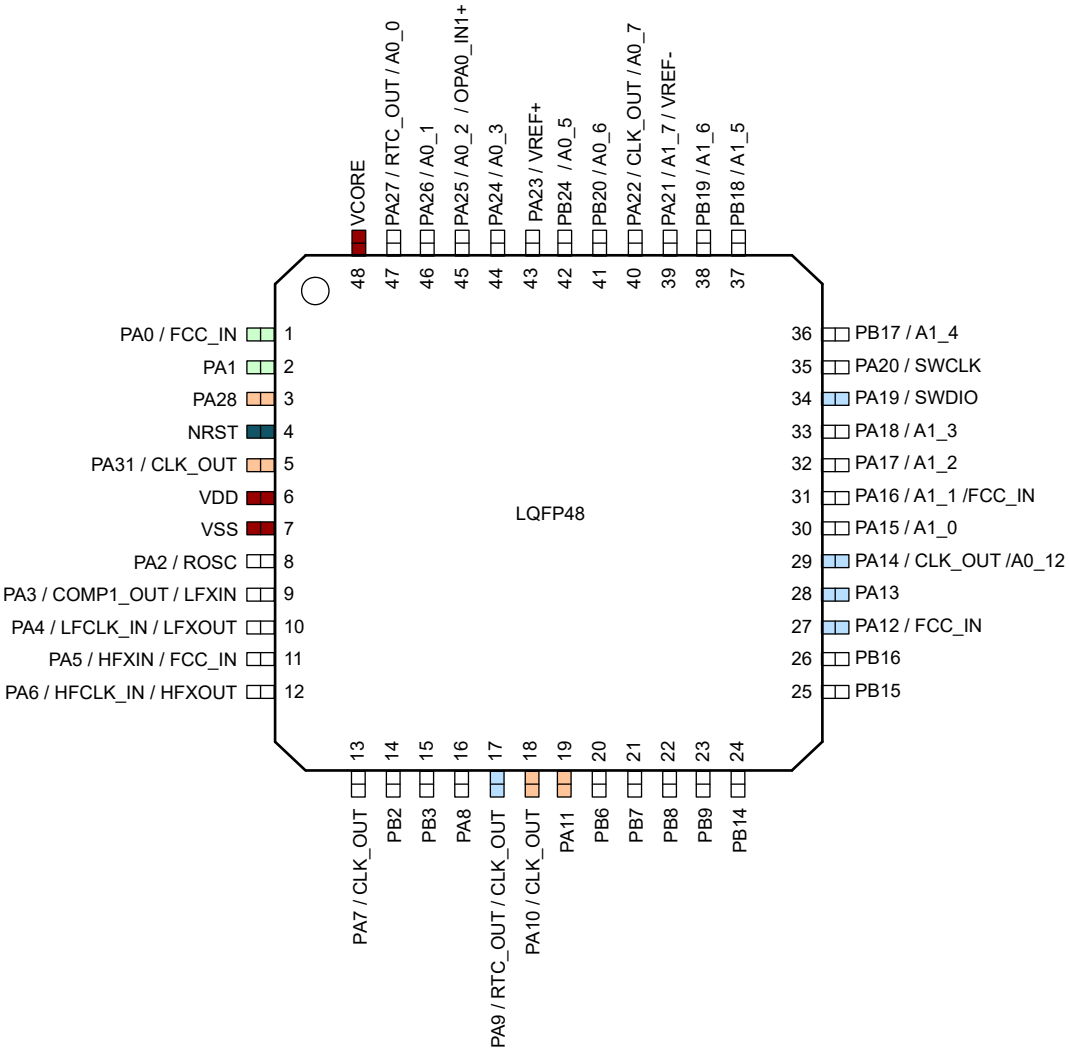


Figure 6-3. 48-Pin PT (LQFP) (Top View)

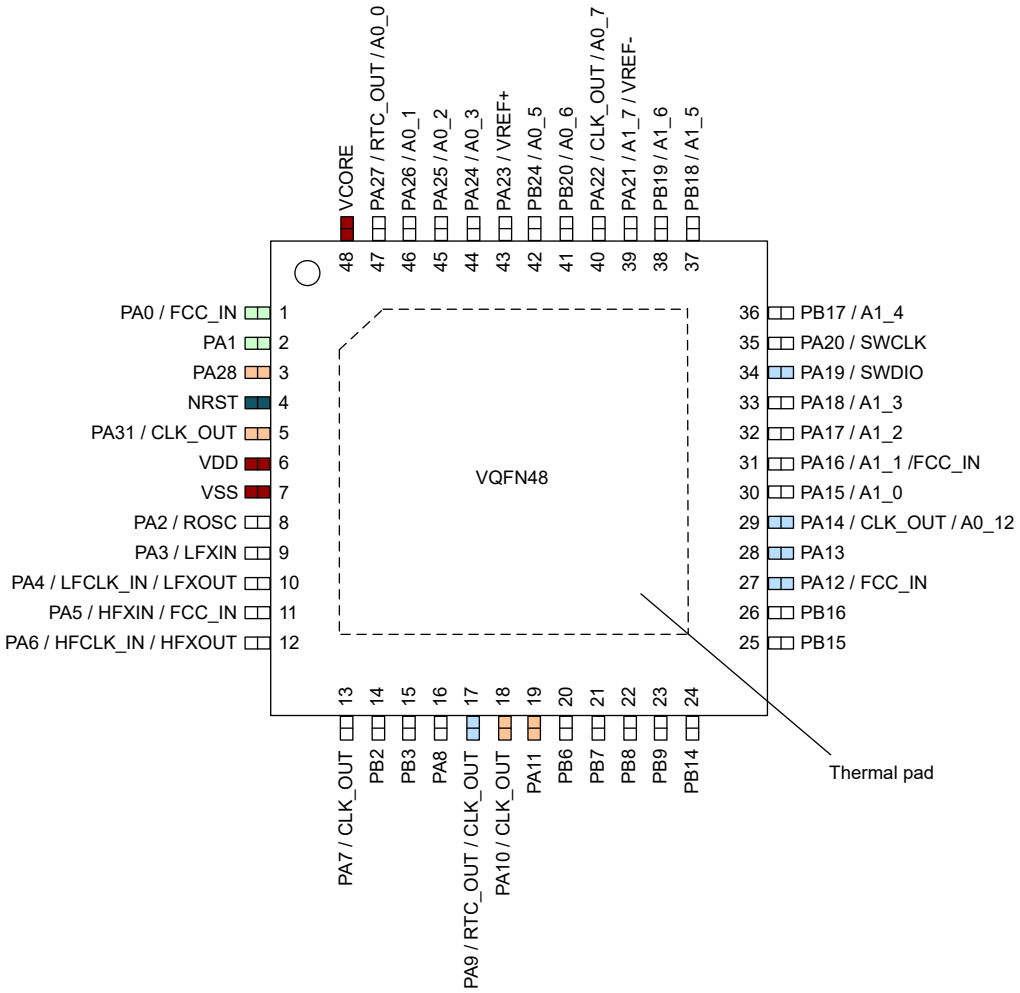


Figure 6-4. 48-Pin RGZ (VQFN) (Top View)

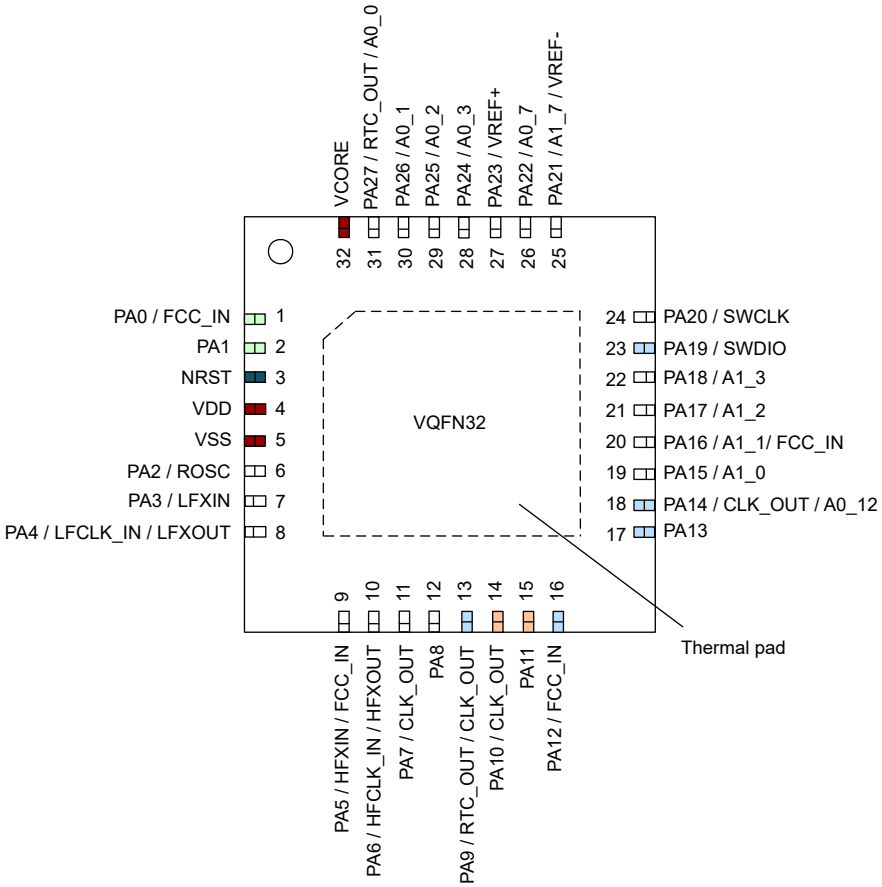


Figure 6-5. 32-Pin RHB (VQFN) (Top View)

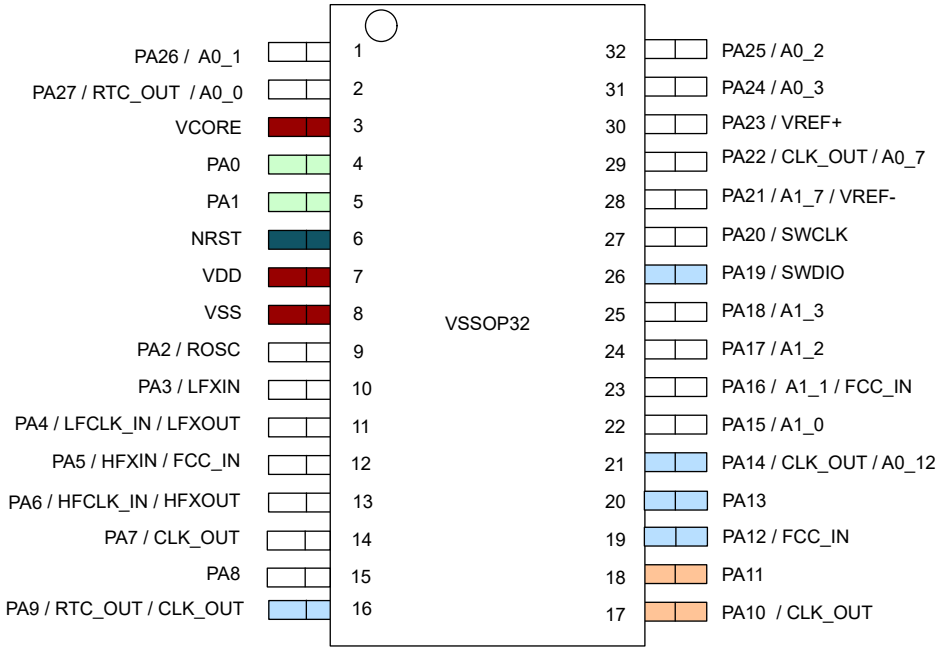


Figure 6-6. 32-Pin DGS32(VSSOP) (Top View)

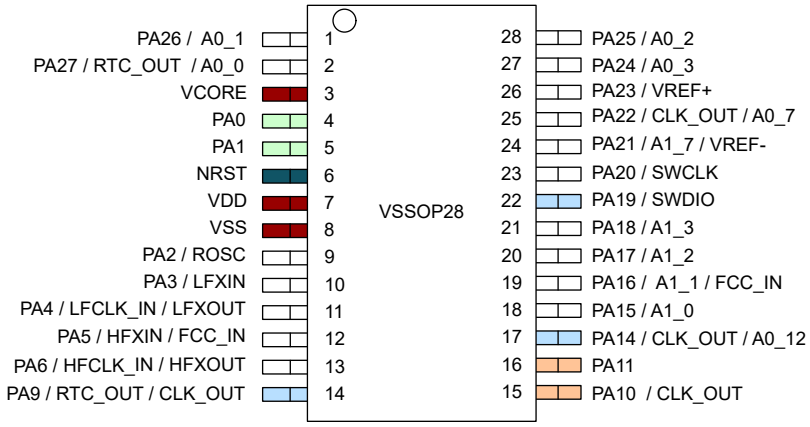


Figure 6-7. 28-Pin DGS28 (VSSOP) (Top View)

Note

For the full pin configuration and description of the functions for each package option, see Pin Attributes and Signal Descriptions.

6.2 Pin Attributes

The following table describes the functions available on every pin for each device package.

Note

Each digital I/O on a device is mapped to a specific Pin Control Management Register (PINCMx) that lets users configure the desired *Pin Function* using the PINCM.PF control bits.

Table 6-1. Digital IO Features by IO Type

IO STRUCTURE	INVERSION CONTROL	DRIVE STRENGTH CONTROL	HYSTERESIS CONTROL	PULLUP RESISTOR	PULLDOWN RESISTOR	WAKEUP LOGIC
Standard drive	Y			Y	Y	
Standard drive with wake(2)	Y			Y	Y	Y
High drive	Y	Y		Y	Y	Y
High speed	Y	Y		Y	Y	
5V-tolerant open drain	Y		Y		Y	Y

Table 6-2. Pin Attributes

PINCMx	PIN NAME	SIGNAL NAMES		PIN NUMBER					IO STRUCTURE
		ANALOG	DIGITAL *[PIN FUNCTION]* (1)	64 LQFP	48 LQFP, VQFN	32 VQFN	32 VSSOP	28 VSSOP	
N/A		VDD		40	6	4	7	7	Power
N/A		VSS		41	7	5	8	8	Power
N/A		VCORE		32	48	32	3	3	Power
N/A		NRST		38	4	3	6	6	Reset
1	PA0		UART0_TX *[2]* / I2C0_SDA *[3]* / TIMA0_C0 *[4]* / TIMA_FAL1 *[5]* / TIMG8_C1 *[6]* / FCC_IN *[7]*/(Default BSL I2C_SDA)	33	1	1	4	4	5V Tol. Open-Drain
2	PA1		UART0_RX *[2]* / I2C0_SCL *[3]* / TIMA0_C1 *[4]* / TIMA_FAL2 *[5]* / TIMG8_IDX *[6]* / TIMG8_C0 *[7]*/ (Default BSL I2C_SCL)	34	2	2	5	5	5V Tol. Open-Drain
7	PA2	ROSC	TIMG8_C1 *[2]* / SPI0_CS0 *[3]* / TIMG7_C1 *[4]* / SPI1_CS0 *[5]*	42	8	6	9	9	Standard
8	PA3	LFXIN	TIMG8_C0 *[2]* / SPI0_CS1 [3] / UART2_CTS [4] / TIMA0_C2 [5] / COMP1_OUT [6] / TIMG7_C0 [7] / TIMA0_C1 [8] / I2C1_SDA [9]	43	9	7	10	10	Standard
9	PA4	LFXOUT	TIMG8_C1 *[2]* / SPI0_POCI *[3]* / UART2_RTS *[4]* / TIMA0_C3 *[5]* / LFCLK_IN *[6]* / TIMG7_C1 *[7]* / TIMA0_C1N *[8]* / I2C1_SCL *[9]*	44	10	8	11	11	Standard
10	PA5	HFXIN	TIMG8_C0 *[2]* / SPI0_PICO *[3]* / TIMA_FAL1 *[4]* / TIMG0_C0 *[5]* / TIMG6_C0 *[6]* / FCC_IN *[7]*	45	11	9	12	12	Standard
11	PA6	HFXOUT	TIMG8_C1 *[2]* / SPI0_SCK *[3]* / TIMA_FAL0 *[4]* / TIMG0_C1 *[5]* / HFCLK_IN *[6]* / TIMG6_C1 *[7]* / TIMA0_C2N *[8]*	46	12	10	13	13	Standard
14	PA7		COMP0_OUT *[2]* / CLK_OUT *[3]* / TIMG8_C0 *[4]* / TIMA0_C2 *[5]* / TIMG8_IDX *[6]* / TIMG7_C1 *[7]* / TIMA0_C1 *[8]*	49	13	11	14	–	Standard
19	PA8		UART1_TX *[2]* / SPI0_CS0 *[3]* / UART0_RTS *[4]* / TIMA0_C0 *[5]* / TIMA1_C0N *[6]*	54	16	12	15	–	Standard
20	PA9		UART1_RX *[2]* / SPI0_PICO *[3]* / UART0_CTS *[4]* / TIMA0_C1 *[5]* / RTC_OUT *[6]* / TIMA0_C0N *[7]* / TIMA1_C1N *[8]* / CLK_OUT *[9]*	55	17	13	16	14	High-Speed

Table 6-2. Pin Attributes (continued)

PINCMx	PIN NAME	SIGNAL NAMES		PIN NUMBER					IO STRUCTURE
		ANALOG	DIGITAL *[PIN FUNCTION]* (1)	64 LQFP	48 LQFP, VQFN	32 VQFN	32 VSSOP	28 VSSOP	
21	PA10		UART0_TX *[2]* / SPI0_POCI *[3]* / I2C0_SDA *[4]* / TIMA1_C0 *[5]* / TIMG12_C0 *[6]* / TIMA0_C2 *[7]* / I2C1_SDA *[8]* / CLK_OUT *[9]*/(Default BSL UART_TX)	56	18	14	17	15	High-Drive
22	PA11		UART0_RX *[2]* / SPI0_SCK *[3]* / I2C0_SCL *[4]* / TIMA1_C1 *[5]* / COMP0_OUT *[6]*/ TIMA0_C2N *[7]* / I2C1_SCL *[8]*/(Default BSL UART_RX)	57	19	15	18	16	High-Drive
34	PA12		UART3_CTS *[2]* / SPI0_SCK *[3]* / TIMG0_C0 *[4]* / CAN_TX *[5]* / TIMA0_C3 *[6]* / FCC_IN *[7]*	5	27	16	19	–	High-Speed
35	PA13	COMP0_IN2-	UART3_RTS *[2]* / SPI0_POCI *[3]* / UART3_RX *[4]* / TIMG0_C1 *[5]* / CAN_RX *[6]* / TIMA0_C3N *[7]*	6	28	17	20	–	High-Speed
36	PA14	COMP0_IN2+ / A0_12	UART0_CTS *[2]* / SPI0_PICO *[3]* / UART3_TX *[4]* / TIMG12_C0 *[5]* / CLK_OUT *[6]*	7	29	18	21	17	High-Speed
37	PA15	A1_0 / DAC_OUT / OPA0_IN2+ / OPA1_IN2+/ COMP0_IN3+ / COMP1_IN3+	UART0_RTS *[2]* / SPI1_CS2 *[3]* / I2C1_SCL *[4]* / TIMA1_C0 *[5]* / TIMG8_IDX *[6]* / TIMA1_C0N *[7]* / TIMA0_C2 *[8]*	8	30	19	22	18	Standard
38	PA16	A1_1 / OPA1_OUT	COMP2_OUT *[2]* / SPI1_POCI *[3]* / I2C1_SDA *[4]* / TIMA1_C1 *[5]* / TIMA1_C1N *[6]* / TIMA0_C2N *[7]* / FCC_IN *[8]*	9	31	20	23	19	Standard
39	PA17	A1_2 / OPA1_IN1- / COMP0_IN1-	UART1_TX *[2]* / SPI1_SCK *[3]* / I2C1_SCL *[4]* / TIMA0_C3 *[5]* / TIMG7_C0 *[6]* / TIMA1_C0 *[7]*	10	32	21	24	20	Standard with wake(2)
40	PA18	A1_3 / OPA1_IN1+ / COMP0_IN1+ / GPAMP_IN-	UART1_RX *[2]* / SPI1_PICO *[3]* / I2C1_SDA *[4]* / TIMA0_C3N *[5]* / TIMG7_C1 *[6]* / TIMA1_C1 *[7]*/ Default BSL_Invoke	11	33	22	25	21	Standard with wake(2)
41	PA19		SWDIO *[2]*	12	34	23	26	22	High-Speed
42	PA20		SWCLK *[2]*	13	35	24	27	23	Standard
46	PA21	A1_7 / COMP2_IN1- / VREF-	UART2_TX *[2]* / TIMG8_C0 *[3]* / UART1_CTS *[4]* / TIMA0_C0 *[5]* / TIMG6_C0 *[6]*	17	39	25	28	24	Standard
47	PA22	A0_7 / GPAMP_OUT / OPA0_OUT	UART2_RX *[2]* / TIMG8_C1 *[3]* / UART1_RTS *[4]* / TIMA0_C1 *[5]* / CLK_OUT *[6]* / TIMA0_C0N *[7]* / TIMG6_C1 *[8]*	18	40	26	29	25	Standard
53	PA23	COMP1_IN1- / VREF+	UART2_TX *[2]* / SPI0_CS3 *[3]* / TIMA0_C3 *[4]* / TIMG0_C0 *[5]* / UART3_CTS *[6]* / TIMG7_C0 *[7]*/ TIMG8_C0 *[8]*	24	43	27	30	26	Standard
54	PA24	A0_3 / OPA0_IN1-	UART2_RX *[2]* / SPI0_CS2 *[3]* / TIMA0_C3N *[4]* / TIMG0_C1 *[5]* / UART3_RTS *[6]* / TIMG7_C1 *[7]* / TIMA1_C1 *[8]*	25	44	28	31	27	Standard
55	PA25	A0_2 / OPA0_IN1+	UART3_RX *[2]* / SPI1_CS3 *[3]* / TIMG12_C1 *[4]* / TIMA0_C3 *[5]* / TIMA0_C1N *[6]*	26	45	29	32	28	Standard
59	PA26	A0_1 / COMP0_IN0+ / OPA0_IN0+ / GPAMP_IN+	UART3_TX *[2]* / SPI1_CS0 *[3]* / TIMG8_C0 *[4]* / TIMA_FAL0 *[5]* / CAN_TX *[6]* / TIMG7_C0 *[7]*	30	46	30	1	1	Standard
60	PA27	A0_0 / COMP0_IN0- / OPA0_IN0-	RTC_OUT *[2]* / SPI1_CS1 *[3]* / TIMG8_C1 *[4]* / TIMA_FAL2 *[5]* / CAN_RX *[6]* / TIMG7_C1 *[7]*	31	47	31	2	2	Standard
3	PA28		UART0_TX *[2]* / I2C0_SDA *[3]* / TIMA0_C3 *[4]* / TIMA_FAL0 *[5]* / TIMG7_C0 *[6]* / TIMA1_C0 *[7]*	35	3	–	–	–	High-Drive

Table 6-2. Pin Attributes (continued)

PINCMx	PIN NAME	SIGNAL NAMES		PIN NUMBER					IO STRUCTURE
		ANALOG	DIGITAL *[PIN FUNCTION]* (1)	64 LQFP	48 LQFP, VQFN	32 VQFN	32 VSSOP	28 VSSOP	
4	PA29		I2C1_SCL *[2]* / UART2_RTS *[3]* / TIMG8_C0 *[4]* / TIMG6_C0 *[5]*	36	–	–	–	–	Standard
5	PA30		I2C1_SDA *[2]* / UART2_CTS *[3]* / TIMG8_C1 *[4]* / TIMG6_C1 *[5]*	37	–	–	–	–	Standard
6	PA31		UART0_RX *[2]* / I2C0_SCL *[3]* / TIMA0_C3N *[4]* / TIMG12_C1 *[5]* / CLK_OUT *[6]*/ TIMG7_C1 *[7]* / TIMA1_C1 *[8]*	39	5	–	–	–	High-Drive
12	PB0		UART0_TX *[2]* / SPI1_CS2 *[3]* / TIMA1_C0 *[4]* / TIMA0_C2 *[5]*	47	–	–	–	–	Standard
13	PB1		UART0_RX *[2]* / SPI1_CS3 *[3]* / TIMA1_C1 *[4]* / TIMA0_C2N *[5]*	48	–	–	–	–	Standard
15	PB2		UART3_TX *[2]* / UART2_CTS *[3]* / I2C1_SCL *[4]* / TIMA0_C3 *[5]* / UART1_CTS *[6]* / TIMG6_C0 *[7]* / TIMA1_C0 *[8]*	50	14	–	–	–	Standard
16	PB3		UART3_RX *[2]* / UART2_RTS *[3]* / I2C1_SDA *[4]* / TIMA0_C3N*[5]* / UART1_RTS *[6]* / TIMG6_C1 *[7]* / TIMA1_C1 *[8]*	51	15	–	–	–	Standard
17	PB4		UART1_TX *[2]* / UART3_CTS *[3]* / TIMA1_C0 *[4]* / TIMA0_C2 *[5]* / TIMA1_C0N *[6]*	52	–	–	–	–	Standard
18	PB5		UART1_RX *[2]* / UART3_RTS *[3]* / TIMA1_C1 *[4]* / TIMA0_C2N *[5]* / TIMA1_C1N *[6]*	53	–	–	–	–	Standard
23	PB6		UART1_TX *[2]* / SPI1_CS0 *[3]* / SPI0_CS1 *[4]* / TIMG8_C0 *[5]* / UART2_CTS *[6]* / TIMG6_C0 *[7]* / TIMA1_C0N *[8]*	58	20	–	–	–	Standard
24	PB7		UART1_RX *[2]* / SPI1_POCI *[3]* / SPI0_CS2 *[4]* / TIMG8_C1 *[5]* / UART2_RTS *[6]* / TIMG6_C1 *[7]* / TIMA1_C1N *[8]*	59	21	–	–	–	Standard
25	PB8		UART1_CTS *[2]* / SPI1_PICO *[3]* / TIMA0_C0 *[4]* / COMP1_OUT *[5]*	60	22	–	–	–	Standard
26	PB9		UART1_RTS *[2]* / SPI1_SCK *[3]* / TIMA0_C1 *[4]* / TIMA0_C0N *[5]*	61	23	–	–	–	Standard
27	PB10		TIMG0_C0 *[2]* / TIMG8_C0 *[3]* / COMP1_OUT *[4]* / TIMG6_C0 *[5]*	62	–	–	–	–	Standard
28	PB11		TIMG0_C1 *[2]* / TIMG8_C1 *[3]* / CLK_OUT *[4]* / TIMG6_C1 *[5]*	63	–	–	–	–	Standard
29	PB12		UART3_TX *[2]* / TIMA0_C2 *[3]* / TIMA_FAL1 *[4]* / TIMA0_C1 *[5]*	64	–	–	–	–	Standard
30	PB13		UART3_RX *[2]* / TIMA0_C3 *[3]* / TIMG12_C0 *[4]* / TIMA0_C1N *[5]*	1	–	–	–	–	Standard
31	PB14		SPI1_CS3 *[2]* / SPI1_POCI *[3]* / SPI0_CS3 *[4]* / TIMG12_C1 *[5]* / TIMG8_IDX *[6]* / TIMA0_C0 *[7]*	2	24	–	–	–	Standard
32	PB15		UART2_TX *[2]* / SPI1_PICO *[3]* / UART3_CTS *[4]* / TIMG8_C0 *[5]* / TIMG7_C0 *[6]*	3	25	–	–	–	Standard
33	PB16		UART2_RX *[2]* / SPI1_SCK *[3]* / UART3_RTS *[4]* / TIMG8_C1 [5] / TIMG7_C1 [6]	4	26	–	–	–	Standard
43	PB17	A1_4 / COMP1_IN2-	UART2_TX *[2]* / SPI0_PICO *[3]* / SPI1_CS1 *[4]* / TIMA1_C0 *[5]* / TIMA0_C2 *[6]*	14	36	–	–	–	Standard
44	PB18	A1_5 / COMP1_IN2+	UART2_RX *[2]* / SPI0_SCK *[3]* / SPI1_CS2 *[4]* / TIMA1_C1 *[5]* / TIMA0_C2N *[6]*	15	37	–	–	–	Standard

Table 6-2. Pin Attributes (continued)

PINCMx	PIN NAME	SIGNAL NAMES		PIN NUMBER					IO STRUCTURE
		ANALOG	DIGITAL *[PIN FUNCTION]* (1)	64 LQFP	48 LQFP, VQFN	32 VQFN	32 VSSOP	28 VSSOP	
45	PB19	A1_6 / COMP2_IN1+ / OPA1_IN0+	COMP2_OUT *[2]* / SPI0_POCI *[3]* / TIMG8_C1 *[4]* / UART0_CTS *[5]* / TIMG7_C1 *[6]*	16	38	–	–	–	Standard
48	PB20	A0_6 / OPA1_IN0-	SPI0_CS2 *[2]* / SPI1_CS0 *[3]* / TIMA0_C2 *[4]* / TIMG12_C0 *[5]* / TIMA_FAL1 *[6]* / TIMA0_C1 *[7]* / TIMA1_C1N *[8]*	19	41	–	–	–	Standard
49	PB21	COMP2_IN0+	SPI1_POCI *[2]* / TIMG8_C0 *[3]*	20	–	–	–	–	Standard
50	PB22	COMP2_IN0-	SPI1_PICO *[2]* / TIMG8_C1 *[3]*	21	–	–	–	–	Standard
51	PB23		SPI1_SCK *[2]* / COMP0_OUT *[3]* / TIMA_FAL0 *[4]*	22	–	–	–	–	Standard
52	PB24	A0_5 / COMP1_IN1+	SPI0_CS3 *[2]* / SPI0_CS1 *[3]* / TIMA0_C3 *[4]* / TIMG12_C1 *[5]* / TIMA0_C1N *[6]* / TIMA1_C0N *[7]*	23	42	–	–	–	Standard
56	PB25	A0_4	UART0_CTS *[2]* / SPI0_CS0 *[3]* / TIMA_FAL2 *[4]*	27	–	–	–	–	Standard
57	PB26	COMP1_IN0+	UART0_RTS *[2]* / SPI0_CS1 *[3]* / TIMA0_C3 *[4]* / TIMG6_C0 [5] / *[6]*	28	–	–	–	–	Standard
58	PB27	COMP1_IN0-	COMP2_OUT *[2]* / SPI1_CS1 *[3]* / TIMA0_C3N *[4]* / TIMG6_C1 *[5]* / TIMA1_C1 *[6]*	29	–	–	–	–	Standard

(1) Set PINCM.PF and PINCM.PC in IOMUX to 0 for analog functions (for example, OPA inputs or outputs, and COMP inputs). Each digital I/O on a device is mapped to a specific Pin Control Management Register (PINCMx) which allows users to configure the desired Pin Function using the PINCM.PF control bits.

(2) Standard with Wake allows the I/O to wake up the device from the lowest low-power mode of SHUTDOWN. All I/O can be configured to wakeup the MCU from higher low-power modes. See section *GPIO FastWake* in the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual* for details.

6.3 Signal Descriptions

Many MSPM0 signals are made available on multiple device pins. The following list describes the column headers:

1. **SIGNAL NAME**: The name of the signal which can be connected to one of the specified pins.
2. **PIN TYPE**: The signal direction and signal type:
   - I = Input
   - O = Output
   - IO = Input, output, or simultaneous input and output
   - ID = Input with open-drain behavior
   - OD = Output with open-drain behavior
   - IOD = Input, output, or simultaneous input and output with open-drain behavior
   - A = Analog
   - PWR = Power function
3. **DESCRIPTION**: A description of the signal.
4. **PIN**: Associated pin number.

For additional information on the pin multiplexing scheme, refer to the IOMUX chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

Note

The IOMUX only supports connecting one IOMUX-managed digital function to the pin at the same time. However, non-IOMUX managed signals (such as analog inputs and WAKE inputs) can be enabled on a pin at the same time that an IOMUX managed digital function is enabled on the pin. In this case, the designer must verify that no contention exists between the functions enabled on each pin.

Table 6-3. Signal Descriptions

FUNCTION	SIGNAL NAME	PIN NO. (1)					PIN TYPE (2)	DESCRIPTION
		64 PM	48 PT, RGZ	32 RHB	32 DGS32	28 DGS28		
ADC	A0_0	31	47	31	2	2	I	ADC0 analog input 0
	A0_1	30	46	30	1	1	I	ADC0 analog input 1
	A0_2	26	45	29	32	28	I	ADC0 analog input 2
	A0_3	25	44	28	31	27	I	ADC0 analog input 3
	A0_4	27	–	–	–	–	I	ADC0 analog input 4
	A0_5	23	42	–	–	–	I	ADC0 analog input 5
	A0_6	19	41	–	–	–	I	ADC0 analog input 6
	A0_7	18	40	26	29	25	I	ADC0 analog input 7
	A0_12	7	29	18	21	17	I	ADC0 analog input 12
	A1_0	8	30	19	22	18	I	ADC1 analog input 0
	A1_1	9	31	20	23	19	I	ADC1 analog input 1
	A1_2	10	32	21	24	20	I	ADC1 analog input 2
	A1_3	11	33	22	25	21	I	ADC1 analog input 3
	A1_4	14	36	–	–	–	I	ADC1 analog input 4
	A1_5	15	37	–	–	–	I	ADC1 analog input 5
	A1_6	16	38	–	–	–	I	ADC1 analog input 6
	A1_7	17	39	25	28	24	I	ADC1 analog input 7
BSL	BSL_invoke	11	33	22	25	21	I	Input pin used to invoke bootloader
BSL (I^2C)	BSLSCL	34	2	2	5	5	I/O	Default I^2C BSL clock
	BSLSDA	33	1	1	4	4	I/O	Default I^2C BSL data
BSL (UART)	BSLRX	57	19	15	18	16	I	Default UART BSL receive
	BSLTX	56	18	14	17	15	O	Default UART BSL transmit
CAN	CAN_TX	5 30	27 46	16 30	1 19	1	O	CAN-FD transmit data
	CAN_RX	6 31	28 47	17 31	2 20	2	I	CAN-FD receive data
Clock	CLK_OUT	7 18 39 49 55 56 63	5 13 17 18 29 40	11 13 14 18 26	14 16 17 21 29	14 15 17 25	O	Configurable clock output
	HFCLK_IN	46	12	10	13	13	I	Digital high-frequency clock input
	HFXIN	45	11	9	12	12	I	Input for high-frequency crystal oscillator HFXT
	HFXOUT	46	12	10	13	13	O	Output for high-frequency crystal oscillator HFXT
	LFCLK_IN	44	10	8	11	11	I	Digital low-frequency clock input
	LFXIN	43	9	7	10	10	I	Input for low-frequency crystal oscillator LFXT
	LFXOUT	44	10	8	11	11	O	Output of low-frequency crystal oscillator LFXT

Table 6-3. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO. (1)					PIN TYPE (2)	DESCRIPTION
		64 PM	48 PT, RGZ	32 RHB	32 DGS32	28 DGS28		
	ROSC	42	8	6	9	9	I	External resistor used for improving oscillator accuracy
Comparator	COMP0_IN0-	31	47	31	2	2	I	Comparator 0 inverting input 0
	COMP0_IN0+	30	46	30	1	1	I	Comparator 0 noninverting input 0
	COMP0_IN1-	10	32	21	24	20	I	Comparator 0 inverting input 1
	COMP0_IN1+	11	33	22	25	21	I	Comparator 0 noninverting input 1
	COMP0_IN2-	6	28	17	20	–	I	Comparator 0 inverting input 2
	COMP0_IN2+	7	29	18	21	17	I	Comparator 0 noninverting input 2
	COMP0_IN3+	8	30	19	22	18	I	Comparator 0 noninverting input 3
	COMP0_OUT	22 49 57	13 19	11 15	18 14	16	O	Comparator 0 output
	COMP1_IN0-	29	–	–	–	–	I	Comparator 1 inverting input 0
	COMP1_IN0+	28	–	–	–	–	I	Comparator 1 noninverting input 0
	COMP1_IN1-	24	43	27	30	26	I	Comparator 1 inverting input 1
	COMP1_IN1+	23	42	–	–	–	I	Comparator 1 noninverting input 1
	COMP1_IN2-	14	36	–	–	–	I	Comparator 1 inverting input 2
	COMP1_IN2+	15	37	–	–	–	I	Comparator 1 noninverting input 2
	COMP1_IN3+	8	30	19	22	18	I	Comparator 1 noninverting input 3
	COMP1_OUT	43 60 62	9 22	7	10	10	O	Comparator 1 output
	COMP2_IN0-	21	–	–	–	–	I	Comparator 2 inverting input 0
	COMP2_IN0+	20	–	–	–	–	I	Comparator 2 noninverting input 0
	COMP2_IN1-	17	39	25	28	24	I	Comparator 2 inverting input 1
	COMP2_IN1+	16	38	–	–	–	I	Comparator 2 noninverting input 1
	COMP2_OUT	9 16 29	31 38	20	23	19	O	Comparator 2 output
DAC	DAC_OUT	8	30	19	22	18	O	DAC output
Debug	SWCLK	13	35	24	27	23	I	Serial wire debug input clock
	SWDIO	12	34	23	26	22	I/O	Serial wire debug data input/output
FCC	FCC_IN	5 9 33 45	1 11 27 31	1 9 16 20	4 12 19 23	4 12 19	I	Frequency clock counter input
General-Purpose Amplifier	GPAMP_IN+	30	46	30	1	1	I	GPAMP noninverting terminal input
	GPAMP_IN-	11	33	22	25	21	I	GPAMP inverting terminal input
	GPAMP_OUT	18	40	26	29	25	O	GPAMP output
GPIO	PA0	33	1	1	4	4	I/O	General-purpose digital I/O with wake up from SHUTDOWN
	PA1	34	2	2	5	5	I/O	General-purpose digital I/O with wake up from SHUTDOWN
	PA2	42	8	6	9	9	I/O	General-purpose digital I/O
	PA3	43	9	7	10	10	I/O	General-purpose digital I/O
	PA4	44	10	8	11	11	I/O	General-purpose digital I/O
	PA5	45	11	9	12	12	I/O	General-purpose digital I/O

Table 6-3. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO. (1)					PIN TYPE (2)	DESCRIPTION
		64 PM	48 PT, RGZ	32 RHB	32 DGS32	28 DGS28		
	PA6	46	12	10	13	13	I/O	General-purpose digital I/O
	PA7	49	13	11	–	–	I/O	General-purpose digital I/O
	PA8	54	16	12	–	–	I/O	General-purpose digital I/O
	PA9	55	17	13	16	14	I/O	General-purpose digital I/O
	PA10	56	18	14	17	15	I/O	General-purpose digital I/O with wake up from SHUTDOWN
	PA11	57	19	15	18	16	I/O	General-purpose digital I/O with wake up from SHUTDOWN
	PA12	5	27	16	–	–	I/O	General-purpose digital I/O
	PA13	6	28	17	–	–	I/O	General-purpose digital I/O
	PA14	7	29	18	21	17	I/O	General-purpose digital I/O
	PA15	8	30	19	22	18	I/O	General-purpose digital I/O
	PA16	9	31	20	23	19	I/O	General-purpose digital I/O
	PA17	10	32	21	24	20	I/O	General-purpose digital I/O with wake up from SHUTDOWN
	PA18	11	33	22	25	21	I/O	General-purpose digital I/O with wake up from SHUTDOWN
	PA19	12	34	23	26	22	I/O	General-purpose digital I/O
	PA20	13	35	24	27	23	I/O	General-purpose digital I/O
	PA21	17	39	25	28	24	I/O	General-purpose digital I/O
	PA22	18	40	26	29	25	I/O	General-purpose digital I/O
	PA23	24	43	27	30	26	I/O	General-purpose digital I/O
	PA24	25	44	28	31	27	I/O	General-purpose digital I/O
	PA25	26	45	29	32	28	I/O	General-purpose digital I/O
	PA26	30	46	30	1	1	I/O	General-purpose digital I/O
	PA27	31	47	31	2	2	I/O	General-purpose digital I/O
	PA28	35	3	–	–	–	I/O	General-purpose digital I/O with wake up from SHUTDOWN
	PA29	36	–	–	–	–	I/O	General-purpose digital I/O
	PA30	37	–	–	–	–	I/O	General-purpose digital I/O
	PA31	39	5	–	–	–	I/O	General-purpose digital I/O with wake up from SHUTDOWN
	PB0	47	–	–	–	–	I/O	General-purpose digital I/O
	PB1	48	–	–	–	–	I/O	General-purpose digital I/O
	PB2	50	14	–	–	–	I/O	General-purpose digital I/O
	PB3	51	15	–	–	–	I/O	General-purpose digital I/O
	PB4	52	–	–	–	–	I/O	General-purpose digital I/O
	PB5	53	–	–	–	–	I/O	General-purpose digital I/O
	PB6	58	20	–	–	–	I/O	General-purpose digital I/O
	PB7	59	21	–	–	–	I/O	General-purpose digital I/O
	PB8	60	22	–	–	–	I/O	General-purpose digital I/O
	PB9	61	23	–	–	–	I/O	General-purpose digital I/O
	PB10	62	–	–	–	–	I/O	General-purpose digital I/O
	PB11	63	–	–	–	–	I/O	General-purpose digital I/O
	PB12	64	–	–	–	–	I/O	General-purpose digital I/O

Table 6-3. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO. (1)					PIN TYPE (2)	DESCRIPTION
		64 PM	48 PT, RGZ	32 RHB	32 DGS32	28 DGS28		
	PB13	1	–	–	–	–	I/O	General-purpose digital I/O
	PB14	2	24	–	–	–	I/O	General-purpose digital I/O
	PB15	3	25	–	–	–	I/O	General-purpose digital I/O
	PB16	4	26	–	–	–	I/O	General-purpose digital I/O
	PB17	14	36	–	–	–	I/O	General-purpose digital I/O
	PB18	15	37	–	–	–	I/O	General-purpose digital I/O
	PB19	16	38	–	–	–	I/O	General-purpose digital I/O
	PB20	19	41	–	–	–	I/O	General-purpose digital I/O
	PB21	20	–	–	–	–	I/O	General-purpose digital I/O
	PB22	21	–	–	–	–	I/O	General-purpose digital I/O
	PB23	22	–	–	–	–	I/O	General-purpose digital I/O
	PB24	23	42	–	–	–	I/O	General-purpose digital I/O
	PB25	27	–	–	–	–	I/O	General-purpose digital I/O
	PB26	28	–	–	–	–	I/O	General-purpose digital I/O
	PB27	29	–	–	–	–	I/O	General-purpose digital I/O
I^2C	I2C0_SCL	34 39 57	2 5 19	2 15	5 18	5 16	I/O	I2C0 serial clock
	I2C0_SDA	33 35 56	1 3 18	1 14	4 17	4 15	I/O	I2C0 serial data
	I2C1_SCL	8 10 36 44 50 57	10 14 19 30 32	8 15 19 21	11 18 20 24	11 16 18 20	I/O	I2C1 serial clock
	I2C1_SDA	9 11 37 43 51 56	9 15 18 31 33	7 14 20 22	10 17 23 25	10 15 19 21	I/O	I2C1 serial data
Operational Amplifier with Chopping (Zero-Drift Op-Amp)	OPA0_IN0+	30	46	30	1	1	I	OPA0 noninverting terminal input 0
	OPA0_IN1+	26	45	29	32	28	I	OPA0 noninverting terminal input 1
	OPA0_IN2+	8	30	19	22	18	I	OPA0 noninverting terminal input 2
	OPA0_IN0-	31	47	31	2	2	I	OPA0 inverting terminal input 0
	OPA0_IN1-	25	44	28	31	27	I	OPA0 inverting terminal input 1
	OPA0_OUT	18	40	26	29	25	O	OPA0 output
	OPA1_IN0+	16	38	–	–	–	I	OPA1 noninverting terminal input 0
	OPA1_IN1+	11	33	22	25	21	I	OPA1 noninverting terminal input 1
	OPA1_IN2+	8	30	19	22	18	I	OPA1 noninverting terminal input 2
	OPA1_IN0-	19	41	–	–	–	I	OPA1 inverting terminal input 0
	OPA1_IN1-	10	32	21	24	20	I	OPA1 inverting terminal input 1
	OPA1_OUT	9	31	20	23	19	O	OPA1 output

Table 6-3. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO. (1)					PIN TYPE (2)	DESCRIPTION
		64 PM	48 PT, RGZ	32 RHB	32 DGS32	28 DGS28		
Power	VSS	41	7	5	8	8	P	Ground supply
	VDD	40	6	4	7	7	P	Power supply
	VCORE	32	48	32	3	3	P	Regulated core power supply output
	QFN Pad	–	Pad	Pad	–	–	P	QFN package exposed thermal pad. TI recommends connection to V_{SS}.
RTC	RTC_OUT	31 55	17 47	13 31	2 16	2 14	O	RTC clock output
SPI	SPI0_CS0	27 42 54	8 16	6 12	9 15	9	I/O	SPI0 chip-select 0
	SPI0_CS1	23 28 43 58	9 20 42	7	10	10	I/O	SPI0 chip-select 1
	SPI0_CS2	19 25 59	21 41 44	28	31	27	I/O	SPI0 chip-select 2
	SPI0_CS3	2 23 24	24 42 43	27	30	26	I/O	SPI0 chip-select 3
	SPI0_SCK	5 15 46 57	12 19 27 37	10 15 16	13 18 19	13 16	I/O	SPI0 clock signal input – SPI peripheral mode Clock signal output – SPI controller mode
	SPI0_POCI	6 16 44 56	10 18 28 38	8 14 17	11 17 20	11 15	I/O	SPI0 controller in/peripheral out
	SPI0_PICO	7 14 45 55	11 17 29 36	9 13 18	12 16 21	12 14 17	I/O	SPI0 controller out/peripheral in
	SPI1_CS0	19 30 42 58	8 20 41 46	6 30	1 9	1 9	I/O	SPI1 chip-select 0
	SPI1_CS1	14 29 31	36 47	31	2	2	I/O	SPI1 chip-select 1
	SPI1_CS2	8 15 47	30 37	19	22	18	I/O	SPI1 chip-select 2
	SPI1_CS3	2 26 48	24 45	29	32	28	I/O	SPI1 chip-select 3
	SPI1_SCK	4 10 22 61	23 26 32	21	24	20	I/O	SPI1 clock signal input – SPI peripheral mode Clock signal output – SPI controller mode
	SPI1_POCI	2 9 20 59	21 24 31	20	23	19	I/O	SPI1 controller in/peripheral out

Table 6-3. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO. (1)					PIN TYPE (2)	DESCRIPTION
		64 PM	48 PT, RGZ	32 RHB	32 DGS32	28 DGS28		
	SPI1_PICO	3 11 21 60	22 25 33	22	25	21	I/O	SPI1 controller out/peripheral in
System	NRST	38	4	3	6	6	I	Reset input active low
Timer	TIMG0_C0	5 24 45 62	11 27 43	9 16 27	12 19 30	12 26	I/O	General purpose timer 0 CCR0 capture input/ compare output
	TIMG0_C1	6 25 46 63	12 28 44	10 17 28	13 20 31	13 27	I/O	General purpose timer 0 CCR1 capture input/ compare output
	TIMG6_C0	17 28 36 45 50 58 62	11 14 20 39	9 25	12 28	12 24	I/O	General purpose timer 6 CCR0 capture input/ compare output
	TIMG6_C1	18 29 37 46 51 59 63	12 15 21 40	10 26	13 29	13 25	I/O	General purpose timer 6 CCR1 capture input/ compare output
	TIMG7_C0	3 10 24 30 35 43	3 9 25 32 43 46	7 21 27 30	1 10 24 30	1 10 20 26	I/O	General purpose timer 7 CCR1 capture input/ compare output
	TIMG7_C1	4 11 16 25 31 39 42 44 49	5 8 10 13 26 33 38 44 47	6 8 11 22 28 31	2 9 11 14 25 31	2 9 11 21 27	I/O	General purpose timer 7 CCR1 capture input/ compare output
	TIMG8_C0	3 17 20 24 30 34 36 43 45 49 58 62	2 9 11 13 20 25 39 43 46	2 7 9 11 25 27 30	1 5 10 12 14 28 30	1 5 10 12 24 26	I/O	General purpose timer 8 CCR0 capture input/ compare output

Table 6-3. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO. (1)					PIN TYPE (2)	DESCRIPTION
		64 PM	48 PT, RGZ	32 RHB	32 DGS32	28 DGS28		
	TIMG8_C1	4 16 18 21 31 33 37 42 44 46 59 63	1 8 10 12 21 26 38 40 47	1 6 8 10 26 31	2 4 9 11 13 29	2 4 9 11 13 25	I/O	General purpose timer 8 CCR1 capture input/ compare output
	TIMG8_IDX	2 8 34 49	2 13 24 30	2 11 19	5 14 22	5 18	I	General purpose timer 8 quadrature encoder index pulse input
	TIMG12_C0	1 7 19 56	18 29 41	14 18	17 21	15 17	I/O	32-bit general purpose timer 0 CCR0 capture input/ compare output
	TIMG12_C1	2 23 26 39	5 24 42 45	29	32	28	I/O	32-bit general purpose timer 0 CCR1 capture input/ compare output
	TIMA0_C0	2 17 33 54 60	1 16 22 24 39	1 12 25	4 15 28	4 24	I/O	Advanced control timer 0 CCR0 capture input/ compare output
	TIMA0_C0N	18 55 61	17 23 40	13 26	16 29	14 25	I/O	Advanced control timer 0 CCR0 compare output (inverting)
	TIMA0_C1	18 34 43 49 55 61 64	2 9 13 17 23 40	2 7 11 13 26	5 10 14 16 29	5 10 14 25	I/O	Advanced control timer 0 CCR1 capture input/ compare output
	TIMA0_C1N	1 19 23 26 44 55	10 17 41 42 45	8 13 29	11 16 32	11 14 28	I/O	Advanced control timer 0 CCR1 compare output (inverting)
	TIMA0_C2	8 14 19 43 47 49 52 56 64	9 13 18 30 36 41	7 11 14 19	10 14 17 22	10 15 18	I/O	Advanced control timer 0 CCR2 capture input/ compare output

Table 6-3. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO. (1)					PIN TYPE (2)	DESCRIPTION
		64 PM	48 PT, RGZ	32 RHB	32 DGS32	28 DGS28		
	TIMA0_C2N	9 15 46 48 53 57	12 19 31 37	10 15 20	13 18 23	13 16 19	I/O	Advanced control timer 0 CCR2 compare output (inverting)
	TIMA0_C3	1 5 10 23 24 26 28 35 44 50	3 10 14 27 32 42 43 45	8 16 21 27 29	11 19 24 30 32	11 20 26 28	I/O	Advanced control timer 0 CCR3 capture input/ compare output
	TIMA0_C3N	6 11 25 29 39 51	5 15 28 33 44	17 22 28	20 25 31	21 27	I/O	Advanced control timer 0 CCR3 compare output (inverting)
	TIMA1_C0	8 10 14 28 35 47 50 52 56	3 14 18 30 32 36	14 19 21	17 22 24	15 18 20	I/O	Advanced control timer 1 CCR0 capture input/ compare output
	TIMA1_C0N	8 23 52 54 58	16 20 30 42	12 19	15 22	18	I/O	Advanced control timer 0 CCR3 compare output (inverting)
	TIMA1_C1	9 11 15 25 29 39 48 51 53 57	5 15 19 31 33 37 44	15 20 22 28	18 23 25 31	16 19 21 27	I/O	Advanced control timer 1 CCR1 capture input/ compare output
	TIMA1_C1N	9 19 53 55 59	17 21 31 41	13 20	16 23	14 19	I/O	Advanced control timer 1 CCR1 compare output (inverting)
	TIMA_FAL0	22 30 35 46	3 12 46	10 30	1 13	1 13	I	Advanced control timer 0 fault handling input
	TIMA_FAL1	19 33 45 64	1 11 41	1 9	4 12	4 12	I	Advanced control timer 1 fault handling input

Table 6-3. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO. (1)					PIN TYPE (2)	DESCRIPTION
		64 PM	48 PT, RGZ	32 RHB	32 DGS32	28 DGS28		
	TIMA_FAL2	27 31 34	2 47	2 31	2 5	2 5	I	Advanced control timer 2 fault handling input
UART	UART0_TX	33 35 47 56	1 3 18	1 14	4 15	4 15	O	UART0 transmit data
	UART0_RX	34 39 48 57	2 5 19	2 15	5 18	5 16	I	UART0 receive data
	UART0_CTS	7 16 27 55	17 29 38	13 18	16 21	14 17	I	UART0 "clear to send" flow control input
	UART0_RTS	8 28 54	16 30	12 19	15 22	18	O	UART0 "request to send" flow control output
	UART1_TX	10 52 54 58	16 20 32	12 21	15 24	20	O	UART1 transmit data
	UART1_RX	11 53 55 59	17 21 33	13 22	16 25	14 21	I	UART1 receive data
	UART1_CTS	17 50 60	14 22 39	25	28	24	I	UART1 "clear to send" flow control input
	UART1_RTS	18 51 61	15 23 40	26	29	25	O	UART1 "request to send" flow control output
	UART2_TX	3 14 17 24	25 36 39 43	25 27	28 30	24 26	O	UART2 transmit data
	UART2_RX	4 15 18 25	26 37 40 44	26 28	29 31	25 27	I	UART2 receive data
	UART2_CTS	37 43 50 58	9 14 20	7	10	10	I	UART2 "clear to send" flow control input
	UART2_RTS	36 44 51 59	10 15 21	8	11	11	O	UART2 "request to send" flow control output
	UART3_TX	7 30 50 64	14 29 46	18 30	1 21	1 17	O	UART3 transmit data
	UART3_RX	1 6 26 51	15 28 45	17 29	20 32	28	I	UART3 receive data

Table 6-3. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO. (1)					PIN TYPE (2)	DESCRIPTION
		64 PM	48 PT, RGZ	32 RHB	32 DGS32	28 DGS28		
	UART3_CTS	3 5 24 52	25 27 43	16 27	19 30	26	I	UART3 "clear to send" flow control input
	UART3_RTS	4 6 25 53	26 28 44	17 28	20 29	27	O	UART3 "request to send" flow control output
Voltage Reference (3)	VREF+	24	43	27	30	26	I/O	Voltage reference (VREF) power supply - external reference input / internal reference output
	VREF-	17	39	25	24	24	I/O	Voltage reference (VREF) ground supply - external reference input / internal reference output

(1) – = not available
(2) I = input, O = output, I/O = input or output, P = power
(3) When using VREF± to bring in an external voltage reference for analog peripherals such as the ADC, a decoupling capacitor must be placed on VREF+ to VREF-/GND with a capacitance based on the external reference source

6.4 Connections for Unused Pins

Table 6-4 lists the correct termination of unused pins.

Table 6-4. Connection of Unused Pins

PIN (1)	POTENTIAL	COMMENT
PAx and PBx	Open	Set corresponding pin functions to GPIO (PINCMx.PF = 0x1) and configure unused pins to output low or input with the internal pullup or pulldown resistor enabled.
NRST	VCC	NRST is an active-low reset signal. Pull the pin high to VCC, or the device cannot start. For more information, see Section 9.1.

(1) Any unused pin with a function that is shared with general-purpose I/O must follow the "PAx and PBx" unused pin connection guidelines.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
VDD	Supply voltage	At VDD pin	–0.3	4.1	V
V_I	Input voltage	Applied to any 5-V tolerant open-drain pins	–0.3	5.5	V
V_I	Input voltage	Applied to any common tolerance pins	–0.3	V_{DD} + 0.3 (4.1 MAX)	V
I_{VDD}	Current into VDD pin (source) (4)	-40°C ≤ T_j ≤ 130°C		80	mA
		-40°C ≤ T_j≤ 90°C		100	mA
I_{VSS}	Current out of VSS pin (sink) (4)	-40°C ≤ T_j≤ 130°C		80	mA
		-40°C ≤ T_j≤ 90°C		100	mA
I_{IO}	Current of SDIO pin	Current sunk or sourced by SDIO pin		6	mA
	Current of HSIO pin	Current sunk or sourced by HSIO pin		6	mA
	Current of HDIO pin	Current sunk or sourced by HDIO pin		20	mA
	Current of ODIO pin	Current sunk by ODIO pin		20	mA
I_D	Supported diode current(3)	Diode current at any device pin	-2	+2	mA
T_A	Ambient Temperature	Ambient Temperature	-40	125	°C
T_J	Junction temperature	Junction temperature	-40	130	°C
T_{stg}	Storage temperature(2)	Storage temperature(2)	–40	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Higher temperatures may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.
(3) PA21 has an internal connection for testing purposes, there is no injection current allowed on this pin.
(4) For applications running at VDD=1.62V, I_VDD/I_VSS<=20mA is required to ensure device functionality

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC-Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC-Q100-011, All pins	±500	V
		Charged device model (CDM), per AEC-Q100-011, Corner pins	±750	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Supply voltage	1.62		3.6	V
VCORE	Voltage on VCORE pin (2)		1.35		V
C_{VDD}	Capacitor connected between VDD and VSS (1)		10		uF
C_{VCORE}	Capacitor connected between VCORE and VSS (1) (2)		470		nF
T_A	Ambient temperature, Q version	–40		125	°C
T_J	Max junction temperature, Q version			130	°C

7.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$f_{MCLK\ (PD1\ bus\ clock)}$	MCLK, CPUCLK frequency with 2 flash wait states (3)			80	MHz
	MCLK, CPUCLK frequency with 1 flash wait state (3)			48	
	MCLK, CPUCLK frequency with 0 flash wait states (3)			24	
$f_{ULPCLK\ (PD0\ bus\ clock)}$	ULPCLK frequency			40	MHz

(1) Connect C_{VDD} and C_{VCORE} between VDD/VSS and VCORE/VSS, respectively, as close to the device pins as possible. A low-ESR capacitor with at least the specified value and tolerance of ±20% or better is required for C_{VDD} and C_{VCORE}.
(2) The VCORE pin must only be connected to C_{VCORE}. Do not supply any voltage or apply any external load to the VCORE pin.
(3) Wait states are managed automatically by the system controller (SYSCTL) and do not need to be configured by application software unless MCLK is sourced from a high speed clock source (HSCLK sourced from HFCLK or SYSPLL).

7.4 Thermal Information

THERMAL METRIC(1)		PACKAGE	VALUE	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	VQFN-48 (RGZ) (Auto)	29.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		20.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		12.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		0.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		12.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		4.1	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	VSSOP-32(DGS32) (Auto)	69.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		24.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		33.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		0.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		33.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		N/A	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	VSSOP-28 (DGS28) (Auto)	74.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		34.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		36.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		2.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		36.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		N/A	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	VQFN-32 (RHB) (Auto)	33.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		24.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		14.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		0.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		14.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		4.1	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	LQFP-64 (PM) (Auto)	61.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		21.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		32.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		1.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		32.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		N/A	°C/W

7.4 Thermal Information (continued)

THERMAL METRIC(1)		PACKAGE	VALUE	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	LQFP-48 (PT) (Auto)	70.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		27.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		34.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		2.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		34.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Supply Current Characteristics

7.5.1 RUN/SLEEP Modes

VDD=3.3V. All inputs tied to 0V or VDD. Outputs do not source or sink any current. All peripherals are disabled.

PARAMETER		MCLK	-40°C		25°C		85°C		105°C		125°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
RUN Mode													
IDD_{RUN}	MCLK=SYSPLL, SYSPLLREF=SYSOSC, CoreMark, execute from flash	80MHz	8		8.1		8.2		8.4		8.7		mA
		48MHz	5		4.9		5.3		5.2		5.8		
	MCLK=SYSOSC, CoreMark, execute from flash	32MHz	3.5		3.6		3.8		3.9		4.2		
		4MHz	0.7		0.7		0.8		1.0		1.4		
	MCLK=SYSPLL, SYSPLLREF=SYSOSC, CoreMark, execute from SRAM	80MHz	6.2		6.3		6.5		6.6		7		
		48MHz	3.9		4		4.2		4.6		5.0		
	MCLK=SYSOSC, CoreMark, execute from SRAM	32MHz	2.6		2.7		2.8		3.0		3.4		
		4MHz	0.6		0.6		0.8		0.9		1.2		
IDD_{RUN}, per MHz	MCLK=SYSPLL, SYSPLLREF=SYSOSC, CoreMark, execute from flash	80MHz	100		101		103		105		109		uA/MHz
	MCLK=SYSPLL, SYSPLLREF=SYSOSC, While(1), execute from flash	80MHz	54	63	55	66	57	70	58	78	64	85	
SLEEP Mode													
IDD_{SLEEP}	MCLK=SYSPLL, SYSPLLREF=SYSOSC, CPU is halted	80MHz	3127	3280	3189	3400	3334	3893	3474	4402	3800	5509	uA
		48MHz	2134	2416	2183	2500	2325	2885	2465	3404	2785	4400	uA
	MCLK=SYSOSC, CPU is halted	32MHz	1436	1525	1473	1593	1608	2113	1745	2626	2094	3731	uA
	MCLK=SYSOSC, CPU is halted	4MHz	463	530	487	620	662	1220	738	1640	1640	2834	uA
IDD_{SLEEP} per MHz	MCLK=SYSPLL, SYSPLLREF=SYSOSC, CPU is halted	80MHz	39		40		42		43		48		uA/MHz

7.5.2 STOP/STANDBY Modes

VDD=3.3V. All inputs tied to 0V or VDD. Outputs do not source or sink any current. All peripherals not noted are disabled.

PARAMETER		ULPCLK	-40°C		25°C		85°C		105°C		125°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
STOP Mode													
IDD_{STOP0}	SYSOSC=32MHz, USE4MHZSTOP=0, DISABLESTOP=0	4MHz	352	444	360	450	364	474	370	504	381	577	uA
IDD_{STOP1}	SYSOSC=4MHz, USE4MHZSTOP=1, DISABLESTOP=0		184	205	190	210	195	250	200	260	213	300	
IDD_{STOP2}	SYSOSC off, DISABLESTOP=1, ULPCLK=LFCLK	32kHz	45	64	47	67	54	90	59	130	71	170	
STANDBY Mode													

7.5.2 STOP/STANDBY Modes (continued)

VDD=3.3V. All inputs tied to 0V or VDD. Outputs do not source or sink any current. All peripherals not noted are disabled.

PARAMETER		ULPCLK	-40°C		25°C		85°C		105°C		125°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
IDD_{STBY0}	LFCLK=LFXT, STOPCLKSTBY=0, RTC enabled	32kHz	2	7	2	7	5	40	9	75	20	105	uA
IDD_{STBY1}	LFCLK=LFOSC, STOPCLKSTBY=1, RTC enabled		1.4	6	1.5	7	4	40	8	70	16	100	
	LFCLK=LFXT, STOPCLKSTBY=1, RTC enabled		1.4	3	1.5	4	4	40	8	70	16	100	
	LFCLK=LFXT, STOPCLKSTBY=1, GPIOA enabled		1.4	3	1.5	4	4	40	8	70	16	100	

7.5.3 SHUTDOWN Mode

All inputs tied to 0V or VDD. Outputs do not source or sink any current. Core regulator is powered down.

PARAMETER		VDD	-40°C		25°C		85°C		105°C		125°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
IDD_{SHDN}	Supply current in SHUTDOWN mode	3.3V	40		80		730		1730		4800		nA

7.6 Power Supply Sequencing

7.6.1 Power Supply Ramp

Figure 7-1 shows the relationships of POR-, POR+, BOR0-, and BOR0+ during powerup and powerdown.

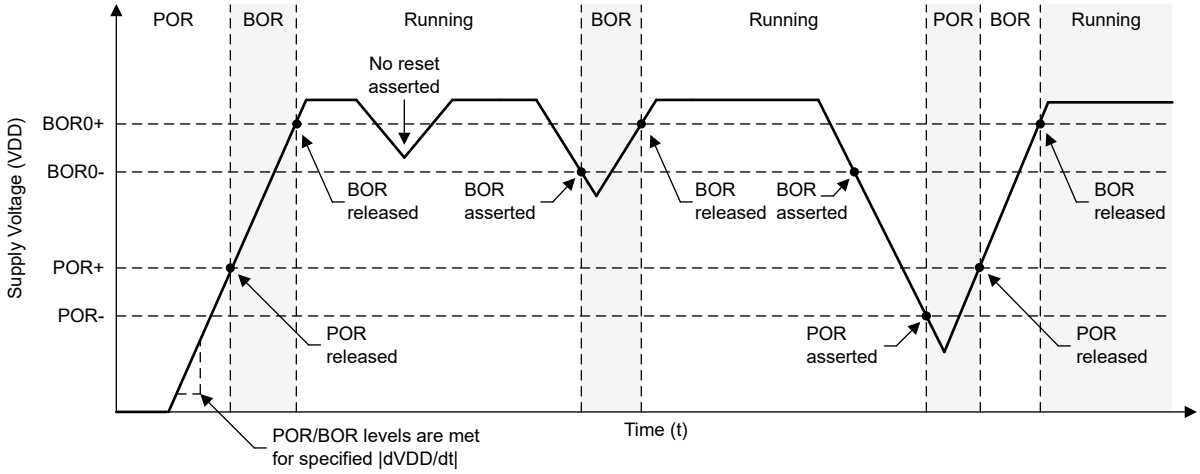


Figure 7-1. Power Cycle POR and BOR Conditions

7.6.1.1 POR and BOR

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
dVDD/dt	VDD (supply voltage) slew rate	Rising			0.1	V/us
		Falling (1)			0.01	
		Falling, STANDBY			0.1	V/ms
V_{POR+}	Power-on reset voltage level	Rising	0.95	1.30	1.59	V
V_{POR-}		Falling	0.9	1.25	1.54	V
$V_{HYS, POR}$	POR hysteresis		30	58	74	mV

7.6.1.1 POR and BOR (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{BOR0+, COLD}$	Brown-out reset voltage level 0 (default level)	-40°C ≤ T_a ≤ 25°C Cold start, rising	1.50	1.56	1.63	V
		25°C ≤ T_a ≤ 125°C Cold start, rising	1.51	1.58	1.65	
V_{BOR0+}		Rising (1)	1.56	1.59	1.62	
V_{BOR0-}		Falling (1)	1.55	1.58	1.61	
$V_{BOR0, STBY}$		STANDBY mode	1.51	1.56	1.61	
V_{BOR1+}	Brown-out-reset voltage level 1	Rising (1)	2.13	2.17	2.21	V
V_{BOR1-}		Falling (1)	2.10	2.14	2.18	
$V_{BOR1, STBY}$		STANDBY mode	2.06	2.13	2.20	
V_{BOR2+}	Brown-out-reset voltage level 2	Rising (1)	2.73	2.77	2.82	V
V_{BOR2-}		Falling (1)	2.7	2.74	2.79	
$V_{BOR2, STBY}$		STANDBY mode	2.62	2.71	2.8	
V_{BOR3+}	Brown-out-reset voltage level 3	Rising (1)	2.88	2.96	3.04	V
V_{BOR3-}		Falling (1)	2.85	2.93	3.01	
$V_{BOR3, STBY}$		STANDBY mode	2.82	2.92	3.02	
$V_{HYS,BOR}$	Brown-out reset hysteresis	Level 0		15	21	mV
		Levels 1-3		34	40	
$T_{PD, BOR}$	BOR propagation delay	RUN/SLEEP/STOP mode			5	us
		STANDBY mode			100	us

(1) Device operating in RUN, SLEEP, or STOP mode.

7.7 Flash Memory Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply						
$VDD_{PGM/ERASE}$	Program and erase supply voltage		1.62		3.6	V
IDD_{ERASE}	Supply current from VDD during erase operation	Supply current delta			10	mA
IDD_{PGM}	Supply current from VDD during program operation	Supply current delta			10	mA
Endurance						
NWEC(HI_ENDURANCE)	Erase/program cycle endurance for chosen 32 sectors of flash (1)		100			k cycles
NWEC (NORMAL_ENDURANCE)	Erase/program cycle endurance (Flash not used for HI_ENDURANCE) (1)		10			k cycles
$NE_{(MAX)}$	Total erase operations before failure (2)		802			k erase operations
$NW_{(MAX)}$	Write operations per word line before sector erase (3)				83	write operations
Retention						
t_{RET_85}	Flash memory data retention	-40°C <= T_j <= 85°C	60			years
t_{RET_105}	Flash memory data retention	-40°C <= T_j <= 105°C	11.4			years
Program and Erase Timing						
$t_{PROG (WORD, 64)}$	Program time for flash word (4) (6)			50	275	µs

7.7 Flash Memory Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PROG (SEC, 64)}$	Program time for 1kB sector (5) (6)			6.4		ms
$t_{ERASE (SEC)}$	Sector erase time	≤2k erase/program cycles, T_j≥25°C		4	20	ms
$t_{ERASE (SEC)}$	Sector erase time	≤10k erase/program cycles, T_j≥25°C		20	150	ms
$t_{ERASE (SEC)}$	Sector erase time	<10k erase/program cycles		20	200	ms
$t_{ERASE (BANK)}$	Bank erase time	<10k erase/program cycles		22	220	ms

(1) Up to 32 application-chosen sectors from the main flash bank(s) or data bank can be used as high endurance sectors. This enables applications that frequently update flash data such as EEPROM emulation.
(2) Total number of cumulative erase operations supported by the flash before failure. A sector erase or bank erase operation is considered to be one erase operation.
(3) Maximum number of write operations allowed per word line before the word line must be erased. If additional writes to the same word line are required, a sector erase is required once the maximum number of write operations per word line is reached.
(4) Program time is defined as the time from when the program command is triggered until the command completion interrupt flag is set in the flash controller.
(5) Sector program time is defined as the time from when the first word program command is triggered until the final word program command completes and the interrupt flag is set in the flash controller. This time includes the time needed for software to load each flash word (after the first flash word) into the flash controller during programming of the sector.
(6) Flash word size is 64 data bits (8 bytes). On devices with ECC, the total flash word size is 72 bits (64 data bits plus 8 ECC bits).

7.8 Timing Characteristics

VDD=3.3V, T_a=25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Wakeup Timing						
$t_{WAKE, SLEEP0}$	Wakeup time from SLEEP0 to RUN (1)			1.3		us
$t_{WAKE, SLEEP1}$	Wakeup time from SLEEP1 to RUN (1)			1.5		us
$t_{WAKE, SLEEP2}$	Wakeup time from SLEEP2 to RUN (1)			2.1		us
$t_{WAKE, STANDBY0}$	Wakeup time from STANDBY0 to RUN (1)			15.2		us
$t_{WAKE, STANDBY1}$	Wakeup time from STANDBY1 to RUN (1)			15.2		us
$t_{WAKE, STOP0}$	Wakeup time from STOP0 to RUN (SYSOSC enabled) (1)			12.1		us
$t_{WAKE, STOP1}$	Wakeup time from STOP1 to RUN (SYSOSC enabled) (1)			13.5		us
$t_{WAKE, STOP2}$	Wakeup time from STOP2 to RUN (SYSOSC disabled) (1)			12.9		
$t_{WAKEUP, SHDN}$	Wakeup time from SHUTDOWN to RUN (2)	Fast boot enabled		240		us
		Fast boot disabled		252		
Asynchronous Fast Clock Request Timing						
$t_{DELAY, SLEEP1}$	Delay time from edge of asynchronous request to first 32MHz MCLK edge	Mode is SLEEP1		0.33		us
$t_{DELAY, SLEEP2}$	Delay time from edge of asynchronous request to first 32MHz MCLK edge	Mode is SLEEP2		0.93		us
$t_{DELAY, STANDBY0}$	Delay time from edge of asynchronous request to first 32MHz MCLK edge	Mode is STANDBY0		3.2		us
$t_{DELAY, STANDBY1}$	Delay time from edge of asynchronous request to first 32MHz MCLK edge	Mode is STANDBY1		3.2		us

7.8 Timing Characteristics (continued)

VDD=3.3V, T_a=25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{DELAY, STOP0}$	Delay time from edge of asynchronous request to first 32MHz MCLK edge	Mode is STOP0		0.1		us
$t_{DELAY, STOP1}$	Delay time from edge of asynchronous request to first 32MHz MCLK edge	Mode is STOP1		2.4		us
$t_{DELAY, STOP2}$	Delay time from edge of asynchronous request to first 32MHz MCLK edge	Mode is STOP2		0.9		us
Startup Timing						
$t_{START, RESET}$	Device cold startup time from reset/ power-up (3)	Fast boot enabled		260		us
		Fast boot disabled		308		
NRST Timing						
$t_{RST, BOOTRST}$	Pulse length on NRST pin to generate BOOTRST	ULPCLK≥4MHz		1.5		us
		ULPCLK=32kHz		80		
$t_{RST, POR}$	Pulse length on NRST pin to generate POR			1		s

(1) The wake-up time is measured from the edge of an external wake-up signal (GPIO wake-up event) to the time that the first instruction of the user program is executed, with glitch filter disabled (FILTEREN=0x0) and fast wake enabled (FASTWAKEONLY=1) .
(2) The wake-up time is measured from the edge of an external wake-up signal (IOMUX wake-up event) to the time that first instruction of the user program is executed.
(3) The start-up time is measured from the time that VDD crosses VBOR0- (cold start-up) to the time that the first instruction of the user program is executed.

7.9 Clock Specifications

7.9.1 System Oscillator (SYSOSC)

Over operating free-air temperature range (unless otherwise noted)). Test conditions indicate lifetime operation under the listed conditions.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SYSOSC}	Factory trimmed SYSOSC frequency	SYSOSCCFG.FREQ=00 (BASE)		32		MHz
		SYSOSCCFG.FREQ=01		4		
	User trimmed SYSOSC frequency	SYSOSCCFG.FREQ=10, SYSOSCTRIMUSER.FREQ=10		24		
		SYSOSCCFG.FREQ=10, SYSOSCTRIMUSER.FREQ=01		16		
f_{SYSOSC}	SYSOSC frequency accuracy when frequency correction loop (FCL) is enabled and an ideal ROSC resistor is assumed (1) (2)	SETUSEFCL=1, T_a = 25 ℃	-0.60		0.68	%
		SETUSEFCL=1, -40 ℃ ≤ T_a ≤ 85 ℃	-0.80		0.93	
		SETUSEFCL=1, -40 ℃ ≤ T_a ≤ 105 ℃	-0.80		1.1	
		SETUSEFCL=1, -40 ℃ ≤ T_a ≤ 125 ℃	-0.80		1.3	
f_{SYSOSC}	SYSOSC accuracy when frequency correction loop (FCL) is enabled with R_{OSC} resistor put at R_{OSC} pin, for factory trimmed frequencies (1) (5) (6)	SETUSEFCL=1, T_a = 25 ℃, ±0.1% ±25ppm R_{OSC}	-0.7		0.78	%
		SETUSEFCL=1, -40 ℃ ≤ T_a ≤ 85 ℃, ±0.1% ±25ppm R_{OSC}	-1.1		1.2	
		SETUSEFCL=1, -40 ℃ ≤ T_a ≤ 105 ℃, ±0.1% ±25ppm R_{OSC}	-1.1		1.4	
		SETUSEFCL=1, -40 ℃ ≤ T_a ≤ 125 ℃, ±0.1% ±25ppm R_{OSC}	-1.1		1.7	
f_{SYSOSC}	SYSOSC frequency accuracy when frequency correction loop (FCL) is enabled when the internal ROSC resistor is used 32MHz (4) (5) (6)	SETUSEFCL=1, T_a = 25 ℃	0		1.0	
		SETUSEFCL=1 -40 ℃ ≤ T_a ≤ 125 ℃	-2.1		1.6	%

7.9.1 System Oscillator (SYSOSC) (continued)

Over operating free-air temperature range (unless otherwise noted)). Test conditions indicate lifetime operation under the listed conditions.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SYSOSC}	SYSOSC frequency accuracy when frequency correction loop (FCL) is enabled when the internal ROSC resistor is used 4MHz (4) (5) (6)	SETUSEFCL=1, T_a = 25 ℃	-1.2		1.7	
		SETUSEFCL=1 -40 ℃ ≤ T_a ≤ 125 ℃	-2.3		1.8	%
f_{SYSOSC}	SYSOSC accuracy when frequency correction loop (FCL) is disabled, 32MHz (5) (6)	SETUSEFCL=0, SYSOSCCFG.FREQ=00, -40 ℃ ≤ T_a ≤ 125 ℃	-2.6		1.8	%
f_{SYSOSC}	SYSOSC accuracy when frequency correction loop (FCL) is disabled, for factory trimmed frequencies, 4MHz (5) (6)	SETUSEFCL=0, SYSOSCCFG.FREQ=01, -40 ℃ ≤ T_a ≤ 125 ℃	-2.8		2.1	
f_{SYSOSC}	External resistor put between ROSC pin and VSS (1)	SETUSEFCL=1		100		kΩ
f_{SYSOSC}	Settling time to target accuracy (3)	VDD>=1.8V, SETUSEFCL=1, ±0.1% 25ppm R_{OSC} (1)			30	us

(1) The SYSOSC frequency correction loop (FCL) enables high SYSOSC accuracy via an external reference resistor (R_{OSC}) which must be connected between the device ROSC pin and VSS when using the FCL. Accuracies are shown for a ±0.1% ±25ppm R_{OSC}; relaxed tolerance resistors may also be used (with reduced SYSOSC accuracy). See the SYSOSC section of the technical reference manual for details on computing SYSOSC accuracy for various R_{OSC} accuracies. R_{OSC} does not need to be populated if the FCL is not enabled.
(2) Represents the device accuracy only. The tolerance and temperature drift of the ROSC resistor used must be combined with this spec to determine final accuracy. Performance for a ±0.1% ±25ppm R_{OSC} is given as a reference point.
(3) When SYSOSC is waking up (for example, when exiting a low power mode) and FCL is enabled, the SYSOSC will initially undershoot the target frequency f_{SYSOSC} by an additional error of up to $f_{settle,SYSOSC}$ for the time $t_{settle,SYSOSC}$, after which the target accuracy is achieved.
(4) The SYSOSC frequency correction loop (FCL) enables high SYSOSC accuracy via an internal reference resistor when using the FCL. See the SYSOSC section of the technical reference manual for details on computing SYSOSC accuracy.
(5) SYSOSC Accuracy is measured in the default power-up state, with MCLK = SYSOSC, the CPU is running a while(1) loop, and the SYSPLL is disabled.
(6) SYSOSC is measured with the internal FCC counter using an external 1ms pulse as the measurement trigger.

7.9.2 SYSOSC Typical Frequency Accuracy

7.9.2.1 Low Frequency Oscillator (LFOSC)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{LFOSC}	LFOSC frequency			32768		Hz
	LFOSC accuracy	-40 ℃ ≤ T_a ≤ 125 ℃	–5		5	%
		-40 ℃ ≤ T_a ≤ 85 ℃	–3		3	%
I_{LFOSC}	LFOSC current consumption			300		nA
$t_{start, LFOSC}$	LFOSC start-up time			1		ms

7.9.3 System Phase Lock Loop (SYSPLL)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{SYSPLLREF}$	SYSPLL reference frequency range(2)		4		48	MHz
f_{VCO}	VCO output frequency		80		400	MHz
f_{SYSPLL}	SYSPLL output frequency range (1)	SYSPLLCLK0, SYSPLLCLK1	2.5		200	MHz
		SYSPLLCLK2X	10		400	
DC_{PLL}	SYSPLL output duty cycle	$f_{SYSPLLREF}$=32MHz, f_{VCO}=160MHz	45		55	%

7.9.3 System Phase Lock Loop (SYSPLL) (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$Jitter_{SYSPLL}$	SYSPLL RMS cycle-to-cycle jitter	$f_{SYSPLLREF}$=32MHz, f_{VCO}=80MHz		60		ps
	SYSPLL RMS period jitter			45		
I_{SYSPLL}	SYSPLL current consumption	$f_{SYSPLLREF}$=32MHz, f_{VCO}=160MHz		316		uA
$t_{start,\ SYSPLL}$	SYSPLL start-up time	$f_{SYSPLLREF}$=32MHz, PDIV=3, QDIV=39, f_{VCO}=160MHz, ±0.5% accuracy		14	24	us

(1) The SYSPLL may support higher output frequencies than the device clock system supports. Ensure that the device maximum frequency specifications are not violated when configuring the SYSPLL output frequencies.
(2) Please refer to SYSPLL tuning parameters in Table 2-6 inside the Techical Reference manual.

7.9.4 Low Frequency Crystal/Clock

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Low frequency crystal oscillator (LFXT)						
f_{LFXT}	LFXT frequency			32768		Hz
DC_{LFXT}	LFXT duty cycle		30		70	%
OA_{LFXT}	LFXT crystal oscillation allowance			419		kΩ
$C_{L,\ eff}$	Integrated effective load capacitance(1)			1		pF
$t_{start,\ LFXT}$	LFXT start-up time			1000		ms
I_{LFXT}	LFXT current consumption	XT1DRIVE=0, LOWCAP=1		200		nA
Low frequency digital clock input (LFCLK_IN)						
f_{LFIN}	LFCLK_IN frequency (2)	SETUSEEXLF=1	29491	32768	36045	Hz
DC_{LFIN}	LFCLK_IN duty cycle (2)	SETUSEEXLF=1	40		60	%
LFCLK Monitor						
$f_{FAULTLF}$	LFCLK monitor fault frequency (3)	MONITOR=1	2800	4200	8400	Hz

(1) This includes parasitic bond and package capacitance (≈2pF per pin), calculated as $C_{LFXIN} \times C_{LFXOUT}/(C_{LFXIN}+C_{LFXOUT})$, where C_{LFXIN} and C_{LFXOUT} are the total capacitance at LFXIN and LFXOUT, respectively.
(2) The digital clock input (LFCLK_IN) accepts a logic level square wave clock.
(3) The LFCLK monitor may be used to monitor the LFXT or LFCLK_IN. It will always fault below the MIN fault frequency, and will never fault above the MAX fault frequency.

7.9.5 High Frequency Crystal/Clock

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
High frequency crystal oscillator (HFXT)						
f_{HFXT}	HFXT frequency	HFXTRSEL=00	4		8	MHz
		HFXTRSEL=01	8.01		16	
		HFXTRSEL=10	16.01		32	
		HFXTRSEL=11	32.01		48	
DC_{HFXT}	HFXT duty cycle	HFXTRSEL=00	40		65	%
		HFXTRSEL=01	40		60	
		HFXTRSEL=10	40		60	
		HFXTRSEL=11	40		60	
OA_{HFXT}	HFXT crystal oscillation allowance	HFXTRSEL=00 (4 to 8MHz range)		2		kΩ
$C_{L,\ eff}$	Integrated effective load capacitance(1)			1		pF
$t_{start,\ HFXT}$	HFXT start-up time (2)	HFXTRSEL=11, 32MHz crystal		0.5		ms

7.9.5 High Frequency Crystal/Clock (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{HFXT}	HFXT current consumption(2)	f_{HFXT}=4MHz, R_m=300Ω, C_L=12pF		75		uA
		f_{HFXT}=48MHz, R_m=30Ω, C_L=12pF, C_m=6.26fF, L_m=1.76mH		600		
High frequency digital clock input (HFCLK_IN)						
f_{HFIN}	HFCLK_IN frequency (3)	USEEXTHFCLK=1	4		48	MHz
DC_{HFIN}	HFCLK_IN duty cycle (3)	USEEXTHFCLK=1	40		60	%

(1) This includes parasitic bond and package capacitance (≈2pF per pin), calculated as $C_{HFXIN} \times C_{HFXOUT}/(C_{HFXIN}+C_{HFXOUT})$, where C_{HFXIN} and C_{HFXOUT} are the total capacitance at HFXIN and HFXOUT, respectively.
(2) The HFXT startup time ($t_{start, HFXT}$) is measured from the time the HFXT is enabled until stable oscillation for a typical crystal. Start-up time is dependent upon crystal frequency and crystal specifications. Refer to the HFXT section of the MSPM0 G-Series 80-MHz Microcontrollers Technical Reference Manual.Current consumption increases with higher RSEL and start up time is decreases with higher RSEL.
(3) The digital clock input (HFCLK_IN) accepts a logic level square wave clock.

7.10 Digital IO

7.10.1 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IH}	High level input voltage	ODIO (1)	VDD≥1.62V	0.7*VDD		5.5	V
			VDD≥2.7V	2		5.5	V
		All I/O except ODIO & Reset	VDD≥1.62V	0.7*VDD		VDD+0.3	V
V_{IL}	Low level input voltage	ODIO	VDD≥1.62V	-0.3		0.3*VDD	V
			VDD≥2.7V	-0.3		0.8	V
		All I/O except ODIO & Reset	VDD≥1.62V	-0.3		0.3*VDD	V
V_{HYS}	Hysteresis	ODIO		0.05*VDD			V
		All I/O except ODIO		0.1*VDD			V
I_{lkg}	High-Z leakage current (All packages except PM)	SDIO(2) (3)	1.62V ≤ VDD ≤ 3.6V, -40 °C ≤ T_a ≤ 125 °C			50(4)	nA
I_{lkg}	High-Z leakage current (PM Package)	SDIO(2) (3)	1.62V ≤ VDD ≤ 3.6V, -40 °C ≤ T_a ≤ 85 °C			50(4)	nA
			1.62V ≤ VDD ≤ 3.6V, -40 °C ≤ T_a ≤ 105 °C			200(4)	nA
			1.62V ≤ VDD ≤ 3.6V, -40 °C ≤ T_a ≤ 125 °C			400(4)	nA
R_{PU}	Pull up resistance	All I/O except ODIO			40		kΩ
R_{PD}	Pull down resistance				40		kΩ
C_I	Input capacitance				5		pF

7.10.1 Electrical Characteristics (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High level output voltage	SDIO	VDD≥2.7V, $\|I_{IO}\|_{,max}$=6mA VDD≥1.71V, $\|I_{IO}\|_{,max}$=2mA VDD≥1.62V, $\|I_{IO}\|_{,max}$=1.5mA -40 °C ≤T_a≤25 °C	VDD-0.4			V
			VDD≥2.7V, $\|I_{IO}\|_{,max}$=6mA VDD≥1.71V, $\|I_{IO}\|_{,max}$=2mA VDD≥1.62V, $\|I_{IO}\|_{,max}$=1.5mA -40 °C ≤T_a≤125 °C	VDD-0.45			
		HSIO	VDD≥2.7V, DRV=1, $\|I_{IO}\|_{,max}$=6mA VDD≥1.71V, DRV=1, $\|I_{IO}\|_{,max}$=3mA VDD≥1.62V, DRV=1, $\|I_{IO}\|_{,max}$=2mA -40 °C ≤T_a≤25 °C	VDD-0.4			
			VDD≥2.7V, DRV=1, $\|I_{IO}\|_{,max}$=6mA VDD≥1.71V, DRV=1, $\|I_{IO}\|_{,max}$=3mA VDD≥1.62V, DRV=1, $\|I_{IO}\|_{,max}$=2mA -40 °C ≤T_a≤125 °C	VDD-0.45			
			VDD≥2.7V, DRV=0, $\|I_{IO}\|_{,max}$=4mA VDD≥1.71V, DRV=0, $\|I_{IO}\|_{,max}$=2mA VDD≥1.62V, DRV=0, $\|I_{IO}\|_{,max}$=1.5mA -40 °C ≤T_a≤25 °C	VDD-0.4			
			VDD≥2.7V, DRV=0, $\|I_{IO}\|_{,max}$=4mA VDD≥1.71V, DRV=0, $\|I_{IO}\|_{,max}$=2mA VDD≥1.62V, $\|I_{IO}\|_{,max}$=1.5mA -40 °C ≤T_a≤125 °C	VDD-0.45			
		HDIO	VDD≥2.7V, DRV=1[(5)], $\|I_{IO}\|_{,max}$=20mA VDD≥1.71V, DRV=1[(5)], $\|I_{IO}\|_{,max}$=10mA	VDD-0.4			
			VDD≥2.7V, DRV=0, $\|I_{IO}\|_{,max}$=6mA VDD≥1.71V, DRV=0, $\|I_{IO}\|_{,max}$=2mA	VDD-0.4			

7.10.1 Electrical Characteristics (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OL}	Low level output voltage	SDIO	VDD≥2.7V, $\|I_{IO}\|_{,max}$=6mA VDD≥1.71V, $\|I_{IO}\|_{,max}$=2mA VDD≥1.62V, $\|I_{IO}\|_{,max}$=1.5mA -40 °C ≤T_a≤25 °C			0.4	V
			VDD≥2.7V, $\|I_{IO}\|_{,max}$=6mA VDD≥1.71V, $\|I_{IO}\|_{,max}$=2mA VDD≥1.62V, $\|I_{IO}\|_{,max}$=1.5mA -40 °C ≤T_a≤125 °C			0.45	
		HSIO	VDD≥2.7V, DRV=1, $\|I_{IO}\|_{,max}$=6mA VDD≥1.71V, DRV=1, $\|I_{IO}\|_{,max}$=3mA VDD≥1.62V, DRV=1, $\|I_{IO}\|_{,max}$=2mA -40 °C ≤T_a≤25 °C			0.4	
			VDD≥2.7V, DRV=1, $\|I_{IO}\|_{,max}$=6mA VDD≥1.71V, DRV=1, $\|I_{IO}\|_{,max}$=3mA VDD≥1.62V, DRV=1, $\|I_{IO}\|_{,max}$=2mA -40 °C ≤T_a≤125 °C			0.45	
			VDD≥2.7V, DRV=0, $\|I_{IO}\|_{,max}$=4mA VDD≥1.71V, DRV=0, $\|I_{IO}\|_{,max}$=2mA VDD≥1.62V, DRV=0, $\|I_{IO}\|_{,max}$=1.5mA -40 °C ≤T_a≤25 °C			0.4	
			VDD≥2.7V, DRV=0, $\|I_{IO}\|_{,max}$=4mA VDD≥1.71V, DRV=0, $\|I_{IO}\|_{,max}$=2mA VDD≥1.62V, DRV=0, $\|I_{IO}\|_{,max}$=1.5mA -40 °C ≤T_a≤125 °C			0.45	
		HDIO	VDD≥2.7V, DRV=1(5), $\|I_{IO}\|_{,max}$=20mA VDD≥1.71V, DRV=1(5), $\|I_{IO}\|_{,max}$=10mA			0.4	
			VDD≥2.7V, DRV=0, $\|I_{IO}\|_{,max}$=6mA VDD≥1.71V, DRV=0, $\|I_{IO}\|_{,max}$=2mA			0.4	
		ODIO	VDD≥2.7V, $I_{OL,max}$=8mA VDD≥1.71V, $I_{OL,max}$=4mA -40 °C ≤T_a≤25 °C			0.4	
			VDD≥2.7V, $I_{OL,max}$=8mA VDD≥1.71V, $I_{OL,max}$=4mA -40 °C ≤T_a≤125 °C			0.45	

(1) I/O Types: ODIO = 5V Tolerant Open-Drain , SDIO = Standard-Drive , HSIO = High-Speed, HDIO = High-Drive
(2) The leakage current is measured with VSS or VDD applied to the corresponding pin(s), unless otherwise noted.
(3) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.
(4) This value is for SDIO not muxed with any analog inputs. If the SDIO is muxed with analog inputs then the leakage can be higher.
(5) When operating a HDIO in DRV=1 high drive strength configuration, a series resistor is necessary to limit the signal slew rate

7.10.2 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Port output frequency(1)	SDIO	VDD ≥ 1.71V, C_L= 20pF			16	MHz
			VDD ≥ 2.7V, CL= 20pF			32	
		HSIO	VDD ≥ 1.71V, DRV = 0, CL= 20pF			16	
			VDD ≥ 1.71V, DRV = 1, CL= 20pF			24	
			VDD ≥ 2.7V, DRV = 0, CL= 20pF			32	
			VDD ≥ 2.7V, DRV = 1, CL= 20pF			40	
		HDIO	VDD ≥ 2.7V, DRV = 1(2), CL= 20pF			20	
			VDD ≥ 2.7V, DRV = 0, CL= 20pF			20	
			VDD ≥ 1.71V, DRV = 1(2), CL= 20pF			16	
			VDD ≥ 1.71V, DRV = 0, CL= 20pF			16	
		ODIO	VDD ≥ 1.71V, FM+, CL= 20pF - 100pF			1	
t_r,t_f	Output rise/fall time	SDIO	VDD ≥ 2.7V, CL= 20pF			3.5	ns
			VDD ≥ 1.71V, C_L= 20pF			6.6	
		HSIO	VDD ≥ 2.7V, DRV = 1, CL= 20pF			1.8	
			VDD ≥ 2.7V, DRV = 0, CL= 20pF			5.9	
			VDD ≥ 1.71V, DRV = 1, CL= 20pF			3.7	
			VDD ≥ 1.71V, DRV = 0, CL= 20pF			12.6	
		HDIO	VDD ≥ 2.7V, DRV = 1, CL= 20pF			1.7	
			VDD ≥ 2.7V, DRV = 0, CL= 20pF			3.8	
			VDD ≥ 1.71V, DRV = 1, CL= 20pF			3.1	
			VDD ≥ 1.71V, DRV = 0, CL= 20pF			8.2	
t_f	Output fall time	ODIO	VDD ≥ 1.71V, FM+, CL= 20pF-100pF	20*VDD/5.5		120	ns

(1) I/O Types: ODIO = 5V Tolerant Open-Drain , SDIO = Standard-Drive , HSIO = High-Speed , HDIO = High-Drive
(2) When operating a HDIO in DRV=1 high drive strength configuration, a series resistor is necessary to limit the signal slew rate

7.11 Analog Mux VBOOST

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VBST}	VBOOST current adder	MCLK/ULPCLK is LFCLK		0.8		uA
		MCLK/ULPCLK is not LFCLK, SYSOSC frequency is 4MHz		10.6		
$t_{START,VBST}$	VBOOST startup time			12	20	us

7.12 ADC

7.12.1 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), all TYP values are measured at 25℃ and all accuracy parameters are measured using 12-bit resolution mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$Vin_{(ADC)}$	Analog input voltage range(1)	Applies to all ADC analog input pins	0		VDD	V
V_{R+}	Positive ADC reference voltage	V_{R+} sourced from VDD		VDD		V
		V_{R+} sourced from external reference pin (VREF+)	1.4		VDD	V
		V_{R+} sourced from internal reference (VREF)		VREF		V

7.12.1 Electrical Characteristics (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), all TYP values are measured at 25℃ and all accuracy parameters are measured using 12-bit resolution mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{R-}	Negative ADC reference voltage			0		V
F_S	ADC sampling frequency	RES = 0x0 (12-bit mode)			4	Msps
		RES = 0x1 (10-bit mode)			4	
		RES = 0x2 (8-bit mode) , SCOMP = 2			5.3	
$I_{(ADC)}$	Operating supply current into VDD terminal	F_S = 4MSPS, V_{R+} = VDD		1.75[2]		mA
$C_{S/H}$	ADC sample-and-hold capacitance			3.3		pF
Rin	ADC input resistance			0.5		kΩ
ENOB	Effective number of bits	f_in = 10KHz, External reference [3]	10.9	11.1		bit
		f_in = 10KHz, External reference [3], HW Averaging Enabled, 16 Samples and 2bit shift	12.3	12.5		
		f_in = 10KHz, Internal reference, V_{R+} = VREF = 2.5V (VRSEL = 1h)[5]	9.9	10.8		
		f_in = 10KHz, Internal reference, V_{R+} = VREF = 2.5V (VRSEL = 2h)		9.2		
SNR	Signal-to-noise ratio	f_in = 10KHz, External reference [3]		68		dB
		f_in = 10KHz, External reference [3], HW Averaging Enabled, 16 Samples and 2bit shift		78		
		f_in = 10KHz, Internal reference, V_{R+} = VREF = 2.5V (VRSEL = 1h)[5]		66		
		f_in = 10KHz, Internal reference, V_{R+} = VREF = 2.5V (VRSEL = 2h)		57		
$PSRR_{DC}$	Power supply rejection ratio, DC	External reference [3], VDD = $VDD_{(min)}$ to $VDD_{(max)}$		62		dB
		VDD = $VDD_{(min)}$ to $VDD_{(max)}$ Internal reference, V_{R+} = VREF = 2.5V		53		
$PSRR_{AC}$	Power supply rejection ratio, AC	External reference [3], ΔVDD = 0.1 V at 1 kHz		61		dB
		ΔVDD = 0.1 V at 1 kHz Internal reference, V_{R+} = VREF = 2.5V		52		
T_{wakeup}	ADC Wakeup Time	Assumes internal reference is active			5	us
$V_{SupplyMon}$	Supply Monitor voltage divider (VDD/3) accuracy	ADC input channel: Supply Monitor [4] [6]	-1.5		1.5	%
$I_{SupplyMon}$	Supply Monitor voltage divider current consumption	ADC input channel: Supply Monitor		10		uA

(1) The analog input voltage range must be within the selected ADC reference voltage range V_{R+} to $V_{R–}$ for valid conversion results.
(2) The internal reference (VREF) supply current is not included in current consumption parameter $I_{(ADC)}$.
(3) All external reference specifications are measured with V_{R+} = VREF+ = VDD = 3.3V and V_{R-} = VREF- = VSS = 0V and external 1uF cap on VREF+ pin
(4) Analog power supply monitor. Analog input on channel 15 is disconnected and is internally connected to the voltage divider which is VDD/3.
(5) Please note that to achieve this ENOB using internal reference VREF, VRSEL bit in MEMCTL register needs to be set to the external reference mode. This will set the REFN as VREF- and REFP as VREF+. In this configuration ,no external connections can be made on the VREF- and VREF+ pins. The REFN pin should be connected to device ground.
(6) Characterized using external reference (VREFSEL = 1)

7.12.2 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{ADCCLK}	ADC clock frequency		4		48	MHz
$t_{ADC\ trigger}$	Software trigger minimum width		3			ADCCLK cycles
t_{Sample}	Sampling time without OPA [1]	12-bit mode, R_S = 50Ω, C_{pext} = 10pF	62.5			ns

7.12.2 Switching Characteristics (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{Sample_PGA}	Sampling time with OPA (1)	12-bit mode	GBW = 0x1, PGA gain = x1	0.22			µs
			GBW = 0x1, PGA gain = x2	0.48			
			GBW = 0x1, PGA gain = x4	0.55			
			GBW = 0x1, PGA gain = x8	0.85			
			GBW = 0x1, PGA gain = x16	1.6			
			GBW = 0x1, PGA gain = x32	2.6			
t_{Sample_DAC}	Sampling time with DAC as input (2)			0.5			µs
t_{Sample_GPAMP}	Sampling time with GPAMP			3			µs
$t_{Sample\_SupplyMon}$	Sample time with Supply Monitor (VDD/3)			5			µs

(1) Only applies for devices with OPA
(2) Only applies for devices with DAC

7.12.3 Linearity Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), all TYP values are measured at 25°C and all linearity parameters are measured using 12-bit resolution mode (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EI	Integral linearity error (INL)	External reference (2)	-2		2	LSB
E_D	Differential linearity error (DNL) Guaranteed no missing codes	External reference (2)	-1		1	LSB
E_O	Offset error	Internal or External reference (2) (3)	-5		5	mV
E_G	Gain error	External reference (2)	-4		4	LSB

(1) Total Unadjusted Error (TUE) can be calculated from E_I, E_O, and E_G using the following formula: $TUE = \sqrt{(E_I^2 + |E_O|^2 + E_G^2)}$
Note: You must convert all of the errors into the same unit, usually LSB, for the above equation to be accurate
(2) All external reference specifications are measured with V_{R+} = VREF+ = VDD and V_{R-} = VSS = 0V, external 1uF cap on VREF+ pin.
(3) Please note that to achieve this offset error using internal reference VREF, VRSEL bit in MEMCTL register needs to be set to the external reference mode. This will set the REFN as VREF- and REFP as VREF+. In this configuration ,no external connections can be made on the VREF- and VREF+ pins.

7.13 Typical Connection Diagram

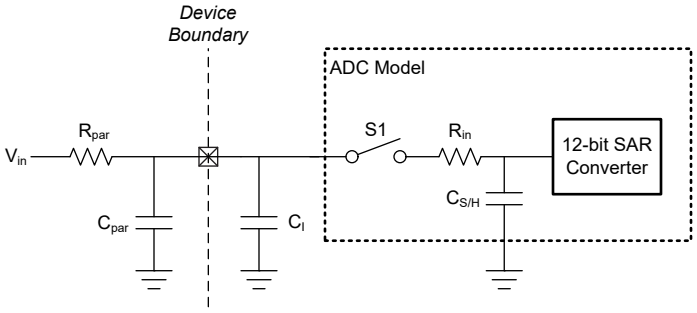


Figure 7-2. ADC Input Network

1. Refer to ADC Electrical Characteristics for the values of R_{in} and $C_{S/H}$
2. Refer to Digital IO Electrical Characteristics for the value of C_I
3. C_{par} and R_{par} represent the parasitic capacitance and resistance of the external ADC input circuitry

Use the following equations to solve for the minimum sampling time (T) required for an ADC conversion:

1. $Tau = (R_{par} + R_{in}) \times C_{S/H} + R_{par} \times (C_{par} + C_I)$
2. $K = \ln(2^n/\text{Settling error}) - \ln((C_{par} + C_I)/C_{S/H})$

3. T (Min sampling time) = K × Tau

7.14 Temperature Sensor

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TS_{TRIM}	Factory trim temperature (2)	ADC and VREF configuration: RES=0 (12-bit mode), VRSEL= 0h (VDD = 3.3V), ADC t_{sample} = 12.5uS	27	30	33	℃
TS_c	Temperature coefficient	-40℃ ≤ T_j ≤ 130℃	-2.1	-1.8	-1.7	mV/℃
$t_{SET, TS}$	Temperature sensor settling time (3)	ADC and VREF configuration: RES=0 (12-bit mode), VRSEL= 0h (VDD = 3.3V), ADC CHANNEL=11			12.5	us

(1) Effective absolute temperature accuracy may be computed by combining the relative temperature accuracy together with the trim accuracy, and accounting for any analog to digital conversion error.
(2) Higher absolute accuracy may be achieved through user calibration. Please refer to temperature sensor chapter in detailed description section.
(3) This is the minimum required ADC sampling time when measuring the temperature sensor.

7.15 VREF

7.15.1 Voltage Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD_{min}	Minimum supply voltage needed for VREF operation	BUFCONFIG = 1	1.62			V
		BUFCONFIG = 0	2.7			
VREF	Voltage reference output voltage	BUFCONFIG = 1	1.38	1.4	1.42	V
		BUFCONFIG = 0	2.46	2.5	2.54	

7.15.2 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VREF}	VREF operating supply current	BUFCONFIG = {0, 1}, No load		189	330	µA
I_{Drive}	VREF output drive strength (1)	Drive strength supported on VREF+ device pin			100	µA
I_{SC}	VREF short circuit current				100	mA
TC_{VREF}	Temperature coefficient of VREF (Bandgap+VRBUF) (2)	BUFCONFIG = {1}			80	ppm/°C
TC_{VREF}	Temperature coefficient of VREF (Bandgap+VRBUF) (2)	BUFCONFIG = {0}			80	ppm/°C
TC_{drift}	Long term VREF drift	Time = 1000 hours, BUFCONFIG = {0, 1}, T = 25℃			300	ppm
$PSRR_{DC}$	VREF Power supply rejection ratio, DC	VDD = 1.7 V to VDDmax, BUFCONFIG = 1	57	63		dB
		VDD = 2.7 V to VDDmax, BUFCONFIG = 0	49	53		
V_{noise}	RMS noise at VREF output (0.1 Hz to 100 MHz)	BUFCONFIG = 1		500		µVrms
		BUFCONFIG = 0		900		
C_{VREF}	Recommended VREF decoupling capacitor on VREF+ pin (3) (4) (5)		0.7	1	1.15	µF
$T_{startup}$	VREF startup time	BUFCONFIG = {0, 1} , VDD = 2.8 V, C_{VREF} = 1µF			200	µS
$T_{refresh}$	VREF External capacitor refresh time		31.25			

(1) The specified MAX output drive strength is supported regardless of which peripherals are being used in the device.
(2) The temperature coefficient of the VREF output is the sum of TC_{VRBUF} and the temperature coefficient of the internal bandgap reference.

(3) Decoupling capacitor (C_{VREF}) is required when using the internal voltage reference VREF and should be connected from the VREF+ pin to VREF-/GND. When using the VREF+/- pins to supply an external reference, a decoupling capacitor value should be selected based on the external reference source.
(4) A ceramic capacitor with package size of 0805 or smaller is preferred. Up to ±20% tolerance is acceptable
(5) The VREF module should only be enabled when C_{VREF} is connected and should not be enabled otherwise.

7.16 Comparator (COMP)

7.16.1 Comparator Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Comparator Electrical Characteristics						
Vcm	Common mode input range		0		VDD	V
V_{offset}	Input offset voltage		-20		20	mV
V_{hys}	DC input hysteresis	HYST=00h		0.4		mV
		HYST=01h		10		
		HYST=02h		20		
		HYST=03h		30		
t_{PD_ls}	Propagation delay, response time	Output Filter off, Overdrive = 100 mV, High Speed Mode		32	50	ns
		Output Filter off, Overdrive = 100 mV, Low Power Mode		1.2	4	µs
t_{en}	Comparator enable time	Startup time to reach propagation delay specification, High Speed Mode (comparator only)			10	µs
		Startup time to reach propagation delay specification, Low Power Mode (comparator only)			10	µs
I_{comp}	Comparator current consumption	Vcm = VDD/2, 100mV overdrive, DAC output as a voltage reference, VDD is reference for DAC, High Speed Mode		130	200	µA
		Vcm = VDD/2, 100mV overdrive, DAC output as a voltage reference, VDD is reference for DAC, Low Power Mode		0.85	2.7	µA
		Vcm = VDD/2, 100mV overdrive, comparator only. High Speed Mode		120	180	µA
		Vcm = VDD/2, 100mV overdrive, comparator only, Low Power Mode		0.7	2.1	µA
	Comparator + VREF current consumption in low power mode	Vcm = VDD/2, 100mV overdrive, DAC output as a voltage reference, internal VREF is reference for DAC, lower power mode. VREF registers SHCYCLE=0xC0, HCYCLE=0xC0, SHMODE=1		3.5		µA
8-bit DAC Electrical Characteristics						
V_{dac}	DAC output range		0		VDD	V
$V_{dac\text{-}code}$	8-bit DAC output voltage for a given code	VIN = reference voltage into 8-bit DAC, code n = 0 to 255		VIN × (n+1) / 256		V
INL	Integral nonlinearity of 8-bit DAC		-1		1	LSB
DNL	Differential nonlinearity of 8-bit DAC		-1		1	LSB
Gain error	Gain error of 8-bit DAC	Reference voltage = VDD	-2		2	% of FSR
Offset error	Offset error of 8-bit DAC		-5		5	mV
t_{dac_settle}	8-bit DAC settling time in static mode	DACCODE0 = 0 → 255, DAC output accurate to 1 LSB		1.5		µs

7.17 DAC

7.17.1 DAC_Supply Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF}	Reference voltage	VDD, External, Internal(1.4V, 2.5V)	1.4		VDD	V

7.17.1 DAC_Supply Specifications (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DAC}	DAC current consumption from VDD	VREF= VDD, No load, DAC code = 0x800		400		µA

7.17.2 DAC Output Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage range	No load, Vref = VDD, DATA = 0x0			20	mV
V_O	Output voltage range	No load, Vref = VDD, DATA = 0xFFF	VDD-0.05	VDD-0.01	VDD	V
V_O	Output voltage range	R_{load} = 3.3kΩ, Vref = VDD, DATA = 0x0			0.13	V
V_O	Output voltage range	R_{load} = 3.3kΩ, Vref = VDD, DATA = 0xFFF	VDD-0.13	VDD-0.1	VDD	V
$C_{L(DAC)}$	Load capacitance				100	pF
$I_{L(DAC)}$	Load current		-1		1	mA
$R_{OUT(DAC)}$	Output resistance	R_{load} = 3.3kΩ, Vref = VDD, V_o = 0.3V to VDD-0.3V		1.2	10	Ω

7.17.3 DAC Dynamic Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate	DATA = 0x80 → 0xF7F → 0x80, Vref = external reference		5.5		V/µs
GE	Glitch energy	DATA = 0x800 → 0x7FF → 0x800, Vref = external reference		1.2		nV-s
PSRR_DC	Power supply rejection ratio, DC	ΔVDD = 100 mV, DATA = 0xFFF, Vref = external reference		79.5		dB
PSRR_AC	Power supply rejection ratio, AC	ΔVDD = 100mV at 100kHz, DATA = 0xFFF, Vref = external reference		25.7		dB
SNR	Signal-to-noise ratio	Vref = external reference, 4kHz input with 1Msps sampling rate(1)		80.9		dB
THD	Total harmonic distortion	Vref = external reference, 4kHz input with 1Msps sampling rate(1)		71.5		dB
SINAD	Signal-to-noise and distortion	Vref = external reference, 4kHz input with 1Msps sampling rate(1)		71.1		dB
ENOB	Effective number of bits	Vref = external reference, 4kHz input with 1Msps sampling rate(1)		11.5		bits

(1) A low pass filter with 300 Hz to 4 kHz pass band connected at DAC output pin.

7.17.4 DAC Linearity Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution				12		bits
DNL	Differential nonlinearity	Vref = internal or external or VDD reference(1)	-1		1	LSB
INL	Integral nonlinearity		-4		4	LSB
E_G	Gain error		-2	-0.5	2	%FSR
E_O	Offset error	Vref = internal or external reference or vdd, With calibration (1)	-2	0.5	2	mV
E_O	Offset error	Vref = internal or external or VDD reference, without calibration (1)	-20		20	mV
t_{cal}	Time for offset calibration		1.3			ms

(1) DAC valid output range is 0.3 to VDD-0.3

7.17.5 DAC Timing Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{ON,12b}$	Turn on time from off state (VREF ready)	DATA = 0xFFF, Error < ±2 LSB, Vref = internal reference		4.5	6.9	µs

7.17.5 DAC Timing Specifications (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{S(FS)}$	Full scale settling time	DATA = 0x1EC->0xFFF->0x1EC, Error< ±2 LSB, Vref = internal reference		0.8	1	µs

7.18 GPAMP

7.18.1 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{CM}	Common mode voltage range	RRI = 0x0		-0.1		VDD-1	V
		RRI = 0x1		1		VDD-0.2	
		RRI = 0x2		-0.1		VDD-0.2	
I_q	Quiescent current, per op-amp	I_O= 0 mA, RRI = 0x0			97		µA
		I_O= 0 mA, RRI = 0x1 or 0x2			93		
GBW	Gain-bandwidth product	C_L = 200pF			0.32		MHz
V_{OS}	Input offset voltage	Noninverting, unity gain, T_A = 25°C, VDD = 3.3V	CHOP = 0x0		±0.2	±9	mV
			CHOP = 0x1		±0.08	±0.4	
dV_{OS}/dT	Input offset voltage temperature drift	Noninverting, unity gain	CHOP = 0x0		7.7		µV/°C
			CHOP = 0x1		0.34		
I_{bias}	Input bias for muxed I/O pin at SoC	0.1V<V_{in}<VDD-0.3V, VDD=3.3V, CHOP=0x0	T_A = 25°C		±40		pA
			T_A = 125°C		±4000		
		0.1V<V_{in}<VDD-0.3V, VDD=3.3V, CHOP = 0x1	T_A = 25°C		±200		
			T_A = 125°C		±4000		
$CMRR_{DC}$	Common mode rejection ratio, DC	Over common mode voltage range	CHOP = 0x0	48	77		dB
			CHOP = 0x1	56	105		
e_n	Input voltage noise density	Noninverting, unity gain	f = 1 kHz		43		nV/√Hz
e_n			f = 10 kHz		19		
R_{in}	Input resistance (1)				0.65		kΩ
C_{in}	Input capacitance	Common mode			4		pF
		Differential			2		
A_{OL}	Open-loop voltage gain, DC	R_L = 350 kΩ, 0.3 < Vo < VDD-0.3		82	90	107	dB
PM	phase margin	C_L = 200 pF, R_L= 350 kΩ		69	70	72	degree
SR	Slew rate	Noninverting, unity gain, C_L = 40 pF			0.32		V/µs
THDN	Total Harmonic Distortion + Noise				0.012		%
I_{Load}	Output load current				4		mA
C_{Load}	Output load capacitance					200	pF

(1) R_{in} here means the input resistance of mux in GPAMP.

7.18.2 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{EN}	GPAMP enable time	ENABLE = 0x0 to 0x1, Bandgap reference ON, 0.1%	Noninverting, unity gain		12	20	µs
$t_{disable}$	GPAMP disable time				4		ULPCLK Cycles

7.18.2 Switching Characteristics (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{SETTLE}	GPAMP settling time	C_L = 200 pF, Vstep = 0.3V to VDD - 0.3V, 0.1%, ENABLE = 0x1	Noninverting, unity gain		9		µs

7.19 OPA

7.19.1 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{CM}	Common mode voltage range	RRI = 0x0		-0.1		VDD-1.1	V
		RRI = 0x1		-0.1		VDD-0.3	
V_O	Voltage output swing from rail range	R_L = 10kΩ connected to VDD/2			20	68	mV
I_q	Quiescent current, per op-amp	I_O= 0mA, RRI = 0x0	GBW = 0x0		94		µA
			GBW = 0x1		319		
		I_O= 0mA, RRI = 0x1	GBW = 0x0		116	134	
			GBW = 0x1		401	500	
I_{BCS}	Burn-out current source current				2		µA
GBW	Gain-bandwidth product	Noninverting, unity gain,C_L = 40 pF	GBW = 0x0		1.5		MHz
			GBW = 0x1		6		
V_{OS}	Input offset voltage	Noninverting, unity gain, VDD = 3.3V, T_A = 25°C	CHOP = 0x0		±0.4	±2	mV
			CHOP = 0x1 or 0x2			±0.3	
		Noninverting, unity gain, VDD = 3.3V	CHOP = 0x0		±1.5	±3.5	
			CHOP = 0x1 or 0x2		±0.1	±0.5	
dV_{OS}/dT	Input offset voltage temperature drift	Noninverting, unity gain, CHOP = 0x0	GBW = 0x0		8.5		µV/°C
			GBW = 0x1		6		
		CHOP = 0x1 or 0x2			0.5		
$PSRR_{DC}$	Power Supply Rejection Ratio, DC	Noninverting, unity gain	CHOP = 0x0	74	86		dB
			CHOP = 0x1 or 0x2	74	86		
I_{bias}	Input bias current	0.1V<V_{in}<VDD-0.3V, VDD = 3.3V, CHOP=0x0	T_A = 25°C		±50		pA
I_{bias} (PM Package)	Input bias current	0.1V<V_{in}<VDD-0.3V, VDD = 3.3V, CHOP=0x0	T_A = 125°C		±0.35	±400	nA
I_{bias} (All packages except PM)	Input bias current	0.1V<V_{in}<VDD-0.3V, VDD = 3.3V, CHOP=0x0	T_A = 125°C		±0.35	±100	nA
I_{bias}	Input bias current	0.1V<V_{in}<VDD-0.3V, VDD = 3.3V, CHOP=0x1	T_A = 25°C		±0.4		nA
I_{bias} (PM Package)	Input bias current	0.1V<V_{in}<VDD-0.3V, VDD = 3.3V, CHOP=0x1	T_A = 125°C		±0.4	±400	nA
I_{bias} (All packages except PM)	Input bias current	0.1V<V_{in}<VDD-0.3V, VDD = 3.3V, CHOP=0x1	T_A = 125°C		±0.4	±104	nA
$CMRR_{DC}$	Common mode rejection ratio, DC	RRI = 0x0: 0V<V_{CM}<VDD-1.1V RRI = 0x1: 0V<V_{CM}<VDD-0.3V	CHOP = 0x0		89		dB
			CHOP = 0x1 or 0x2	73	102		

7.19.1 Electrical Characteristics (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
e_n	Input voltage noise density	GBW = 0x0, Noninverting, unity gain, CHOP = 0x0	f = 1kHz		240		nV/√Hz
			f = 10kHz		88		
	Integrated voltage noise, input referred	f = 0.1Hz to 10Hz, GBW = 0x0, Noninverting, unity gain	CHOP = 0x0		75		µVpp
			CHOP = 0x1 or 0x2		2		
	Integrated voltage noise, output referred	f = 0.1Hz to 10MHz, GBW = 0x0, CHOP = 0x0, Noninverting, unity gain			1.5		mVpp
R_{in}	Input resistance (1)				2.6		kΩ
C_{in}	Input capacitance	Common mode			3		pF
A_{OL}	Open-loop voltage gain, DC	R_L = 20kΩ to GND, 0.3<Vo<VDD-0.3			105		dB
PM	phase margin	C_L = 40pF	GBW = 0x0		57		degree
			GBW = 0x1		50		
SR	Slew rate	Noninverting, unity gain, C_L = 40 pF	GBW = 0x0		1.3		V/µs
			GBW = 0x1		4.9		
THDN	Total harmonic distortion + noise	Noninverting, unity gain, GBW = 0x0, f = 1.5kHz, Integration BW = 100kHz			0.0034		%
		Noninverting, unity gain, GBW = 0x1, f = 6kHz, Integration BW = 100kHz			0.004		
I_{Load}	Output load current	GBW = 0x0			±9		mA
		GBW = 0x1			±30		
C_{Load}	Output load capacitance					40	pF

(1) R_{in} here means the input resistance of mux in OPA.

7.19.2 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{EN}	OPA enable time	ENABLE = 0x0 to 0x1, Bandgap reference ON, 0.1%, Noninverting, unity gain	GBW = 0x0		7.3	12	µs
			GBW = 0x1		4.4	6	
$t_{disable}$	OPA disable time				4		ULPCLK cycles
f_{CHOP}	OPA Chopping Frequency	CHOP = 0x1	GAIN = 0x0		125		kHz
			GAIN = 0x1		62.5		
			GAIN = 0x2		31.25		
			GAIN = 0x3		15.625		
			GAIN = 0x4		7.8		
			GAIN = 0x5		3.9		
t_{SETTLE}	OPA settling time	C_L = 40 pF, Vstep = 0.3V to VDD-0.3V, 0.1%, ENABLE = 0x1, Noninverting, unity gain, VDD>=1.8V	GBW = 0x0		2.5	9	µs
			GBW = 0x1		1.3	5	

7.19.3 PGA Mode

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
G	non- inverting gain error	Buffer Mode(1)		–0.05		+0.05	%
		GAIN = 0x1 (		–0.6		+0.6	
		GAIN = 0x2 (		–0.8		+0.8	
		GAIN = 0x3 (		–1		+1	
		GAIN = 0x4 (		-1.5		+1.5	
		GAIN = 0x5 (		–3.2		+2	
	inverting gain error	GAIN = 0x1 (		–0.8		+0.8	
		GAIN = 0x2 (		–1.0		+1.0	
		GAIN = 0x3 (		–1.2		1.2	
		GAIN = 0x4 (		–1.5		1.5	
		GAIN = 0x5		–3.3		2.1	
R_{PGA}	Programmable gain stage resistance	GAIN = 0x1	R1		64		kΩ
			R2 (feedback resistor)		64		
		GAIN = 0x2	R1		32		
			R2 (feedback resistor)		96		
		GAIN = 0x3	R1		16		
			R2 (feedback resistor)		112		
		GAIN = 0x4	R1		8		
			R2 (feedback resistor)		120		
		GAIN = 0x5	R1		4		
			R2 (feedback resistor)		124		
G/dV	Gain supply drift				0.02	1	%/V
G/dT	Gain temperature drift				0.002	0.02	%/C
THD	Total harmonic distortion	f = 3kHz, R_L = 1.5kOhm to VDD/2, GBW = 0x1, GAIN = 0x1			75		dB
		f = 188Hz, R_L = 1.5kOhm to VDD/2, GBW = 0x1, GAIN = 0x5			55		

(1) OPA operates with unity gain in buffer mode, providing impedance matching and signal buffering without the amplification.

7.20 I2C

7.20.1 I2C Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	Standard mode		Fast mode		Fast mode plus		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{I2C}	I2C input clock frequency		2	32	8	32	20	32	MHz
f_{SCL}	SCL clock frequency		0.025	0.1		0.4		1	MHz
$t_{HD,STA}$	Hold time (repeated) START		4		0.6		0.26		us
t_{LOW}	LOW period of the SCL clock		4.7		1.3		0.5		us
t_{HIGH}	High period of the SCL clock		4		0.6		0.26		us
$t_{SU,STA}$	Setup time for a repeated START		4.7		0.6		0.26		us
$t_{HD,DAT}$	Data hold time		0		0		0		ns
$t_{SU,DAT}$	Data setup time		250		100		50		ns

7.20.1 I2C Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	Standard mode		Fast mode		Fast mode plus		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{SU,STO}$	Setup time for STOP		4		0.6		0.26		us
t_{BUF}	bus free time between a STOP and START condition		4.7		1.3		0.5		us
$t_{VD;DAT}$	data valid time			3.45		0.9		0.45	us
$t_{VD;ACK}$	data valid acknowledge time			3.45		0.9		0.45	us

7.20.2 I2C Filter

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SP}	Pulse duration of spikes suppressed by input filter	AGFSELx = 0		6		ns
		AGFSELx = 1		14	35	ns
		AGFSELx = 2		22	60	ns
		AGFSELx = 3		35	90	ns

7.20.2.1 I²C Timing Diagram

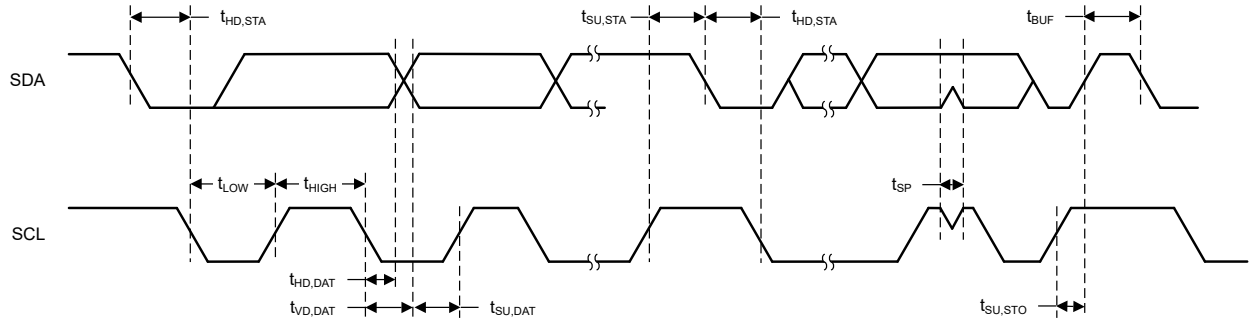


Figure 7-3. I2C Timing Diagram

7.21 SPI

7.21.1 SPI

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SPI						
f_{SPI}	SPI clock frequency	Clock max speed >= 32MHz 1.62 < VDD < 3.6V Controller or peripheral mode			16(4)	MHz
f_{SPI}	SPI clock frequency	Clock max speed >= 48MHz 1.62 < VDD < 2.7V Peripheral or Controller mode with High speed IO			24(4)	MHz
f_{SPI}	SPI clock frequency	Clock max speed >= 64MHz 2.7 < VDD < 3.6V Peripheral or Controller mode with High speed IO			32(4)	MHz
DC_{SCK}	SCK Duty Cycle		40	50	60	%
Controller						

7.21.1 SPI (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{SCLK\_H/L}$	SCLK High or Low time		(tSPI/2) - 1	tSPI / 2	(tSPI/2) + 1	ns
$t_{CS.LEAD}$	CS lead-time, CS active to clock	SPH=0	1 SPI Clock			
$t_{CS.LEAD}$	CS lead-time, CS active to clock	SPH=1	1/2 SPI Clock			
$t_{CS.LEAD}$	CS lag time, Last clock to CS inactive	SPH=0	1/2 SPI Clock			
$t_{CS.LAG}$	CS lag time, Last clock to CS inactive	SPH=1	1 SPI Clock			
$t_{CS.ACC}$	CS access time, CS active to PICO data out				1/2 SPI Clock	
$t_{CS.DIS}$	CS disable time, CS inactive to PICO high inpedance				1 SPI Clock	
$t_{SU.CI}$	POCI input data setup time (1)	2.7 < VDD < 3.6V, delayed sampling enabled	1			ns
$t_{SU.CI}$	POCI input data setup time (1)	1.62 < VDD < 2.7V, delayed sampling enabled	1			ns
$t_{SU.CI}$	POCI input data setup time (1)	2.7 < VDD < 3.6V, no delayed sampling	29			ns
$t_{SU.CI}$	POCI input data setup time (1)	1.62 < VDD < 2.7V, no delayed sampling	37			ns
$t_{HD.CI}$	POCI input data hold time	delayed sampling enabled	24			ns
$t_{HD.CI}$	POCI input data hold time	no delayed sampling	0			ns
$t_{VALID.CO}$	PICO output data valid time (2)				10	ns
$t_{HD.CO}$	PICO output data hold time (3)		6			ns
Peripheral						
$t_{CS.LEAD}$	CS lead-time, CS active to clock		11			ns
$t_{CS.LAG}$	CS lag time, Last clock to CS inactive		1			ns
$t_{CS.ACC}$	CS access time, CS active to POCI data out				26	ns
$t_{CS.DIS}$	CS disable time, CS inactive to POCI high inpedance				26	ns
$t_{SU.PI}$	PICO input data setup time		7			ns
$t_{HD.PI}$	PICO input data hold time		0			ns
$t_{VALID.PO}$	POCI output data valid time(2)	2.7 < VDD < 3.6V			25	ns
$t_{VALID.PO}$	POCI output data valid time(2)	1.62 < VDD < 2.7V			31	ns
$t_{HD.PO}$	POCI output data hold time(3)		5			ns

(1) The POCI input data setup time can be fully compensated when delayed sampling feature is enabled.
(2) Specifies the time to drive the next valid data to the output after the output changing SCLK clock edge
(3) Specifies how long data on the output is valid after the output changing SCLK clock edge
(4) fSPIclk = 1/2tLO/HI with tLO/HI = max(tVALID,CO + tSU,PI, tSU,CI + tVALID,PO).

7.21.2 SPI Timing Diagram

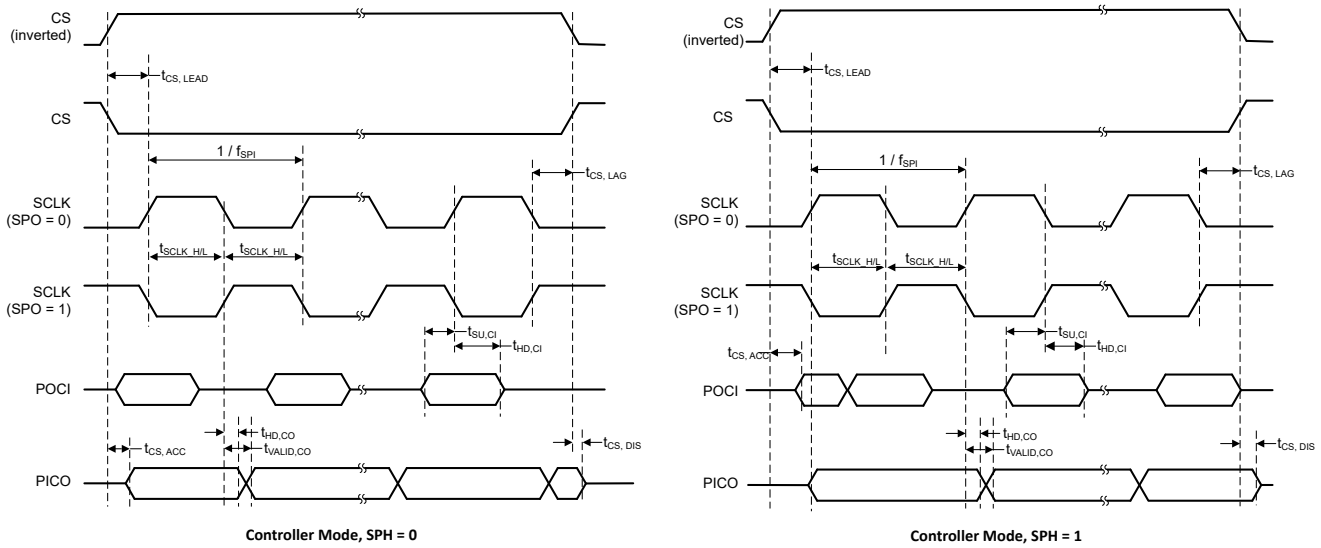


Figure 7-4. SPI Timing Diagram - Controller Mode

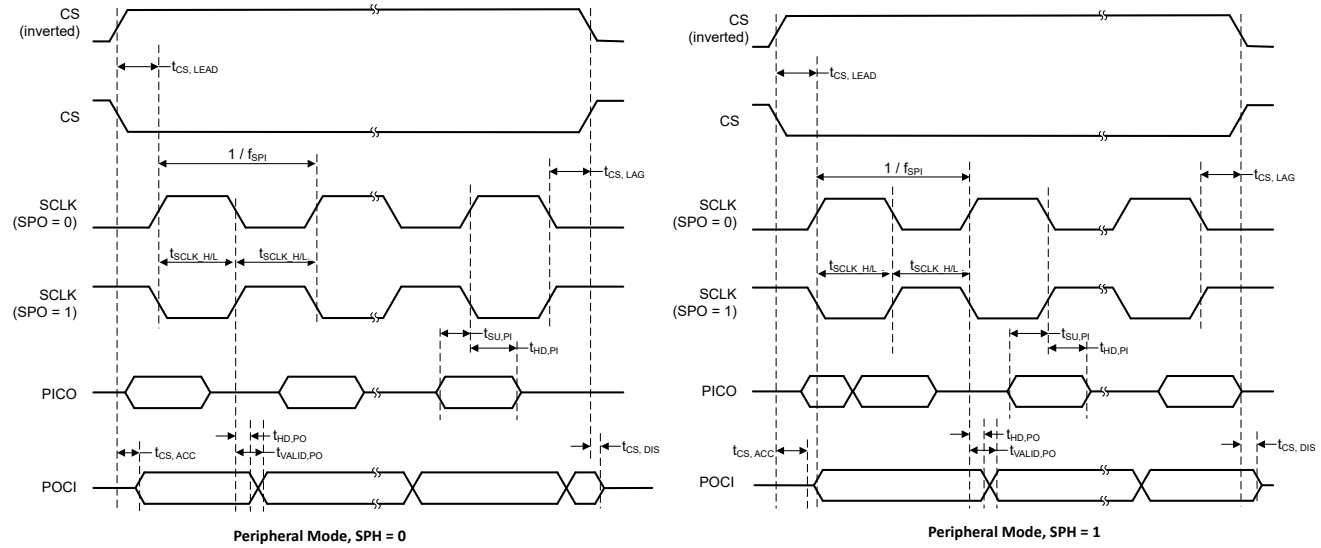


Figure 7-5. SPI Timing Diagram - Peripheral Mode

7.22 UART

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{UART}	UART input clock frequency	UART in Power Domain1			80	MHz
f_{UART}	UART input clock frequency	UART in Power Domain0			40	MHz
f_{BITCLK}	BITCLK clock frequency(equals baud rate in MBaud)	UART in Power Domain1			10	MHz
f_{BITCLK}	BITCLK clock frequency(equals baud rate in MBaud)	UART in Power Domain0			5	MHz

7.22 UART (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SP}	Pulse duration of spikes suppressed by input filter (1)	AGFSELx = 0		6		ns
		AGFSELx = 1		14	35	ns
		AGFSELx = 2		22	60	ns
		AGFSELx = 3		35	90	ns

(1) Pulses on the UART receive input (RX) that are shorter than the UART receive deglitch time are suppressed. Thus the selected deglitch time can limit the maximum useable baud rate. To ensure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.

7.23 TIMx

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{res}	Timer resolution time	TIMx in Power Domain 1, $f_{TIMxCLK}$ = 80MHz	12.5			ns
		TIMx in Power Domain 0, $f_{TIMxCLK}$ = 40MHz	25			ns
			1			$t_{TIMxCLK}$

7.24 TRNG

7.24.1 TRNG Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$TRNG_{IACT}$	TRNG active current	TRNG clock = 20MHz		115		µA

7.24.2 TRNG Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$TRNGCLK_F$	TRNG input clock frequency		9.5	10	25	MHz
$TRNG_{STARTUP}$	TRNG startup time			520		µs
$TRNG_{LAT32}$	Latency to generate 32 random bits	Decimation ratio = 4, TRNG clock = 20MHz		6.4		µs
$TRNG_{LAT256}$	Latency to generate 256 random bits	Decimation ratio = 4, TRNG clock = 20MHz		51.2		µs

7.25 Emulation and Debug

7.25.1 SWD Timing

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SWD}	SWD frequency				10	MHz

8 Detailed Description

The following sections describe all of the components that make up the devices in this data sheet. The peripherals integrated into these devices are configured by software through Memory Mapped Registers (MMRs). For more details, see the corresponding chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.1 CPU

The CPU subsystem (MCPUSS) implements an Arm Cortex-M0+ CPU, an instruction prefetch and cache, a system timer, a memory protection unit, and interrupt management features. The Arm Cortex-M0+ is a cost-optimized 32-bit CPU that delivers high performance and low power to embedded applications. Key features of the CPU subsystem include:

- Arm Cortex-M0+ CPU supporting 32MHz clock frequency
  - Armv6-M Thumb instruction set (little endian) with single-cycle 32×32 multiply instruction
  - Single-cycle access to GPIO registers through Arm single-cycle IO port
- Prefetch logic to improve sequential code execution, and I-cache with four 64-bit cache lines
- System timer (SysTick) with 24-bit down counter and automatic reload
- Memory protection unit (MPU) with eight programmable regions
- Nested vectored interrupt controller (NVIC) with four programmable priority levels and tail chaining
- Interrupt groups for expanding the total interrupt sources, with jump index for low interrupt latency

8.2 Operating Modes

MSPM0G MCUs provide five main operating modes (power modes) to allow for optimization of the device power consumption based on application requirements. In order of decreasing power, the modes are: RUN, SLEEP, STOP, STANDBY, and SHUTDOWN. The CPU is active executing code in RUN mode. Peripheral interrupt events can wake the device from SLEEP, STOP, or STANDBY mode to the RUN mode. SHUTDOWN mode completely disables the internal core regulator to minimize power consumption, and wake is only possible via NRST, SWD, or a logic level match on certain IOs. RUN, SLEEP, STOP, and STANDBY modes also include several configurable policy options (for example, RUN.x) for balancing performance with power consumption.

To further balance performance and power consumption, MSPM0G devices implement two power domains: PD1 (for the CPU, memories, and high performance peripherals), and PD0 (for low speed, low power peripherals). PD1 is always powered in RUN and SLEEP modes, but is disabled in all other modes. PD0 is always powered in RUN, SLEEP, STOP, and STANDBY modes. PD1 and PD0 are both disabled in SHUTDOWN mode.

8.2.1 Functionality by Operating Mode (MSPM0G350x)

Supported functionality in each operating mode is given in Table 8-1.

Functional key:

- **EN**: The function is enabled in the specified mode.
- **DIS**: The function is disabled (either clock or power gated) in the specified mode, but the function's configuration is retained.
- **OPT**: The function is optional in the specified mode, and remains enabled if configured to be enabled.
- **NS**: The function is not automatically disabled in the specified mode, but it is not supported.
- **OFF**: The function is fully powered off in the specified mode, and no configuration information is retained. When waking up from an OFF state, all module registers must be re-configured to the desired settings by application software.

Table 8-1. Supported Functionality by Operating Mode

OPERATING MODE		RUN			SLEEP			STOP			STANDBY		SHUTDOWN
		RUN0	RUN1	RUN2	SLEEP0	SLEEP1	SLEEP2	STOP0	STOP1	STOP2	STANDBY0	STANDBY1	
Oscillators	SYSOSC	EN		DIS	EN		DIS	OPT[1]	EN	DIS	DIS		OFF
	LFOSC or LFXT	EN (LFOSC or LFXT)											OFF
	HFXT	OPT	DIS		OPT	DIS		DIS			DIS		OFF
	SYSPLL	OPT	DIS[4]		OPT	DIS[4]		DIS[4]			DIS[4]		OFF
Clocks	CPUCLK	80MHz	32KHz		DIS								OFF
	MCLK to PD1	80MHz	32KHz		80MHz	32KHz		DIS					OFF
	ULPCLK to PD0	40MHz	32KHz		40MHz	32KHz		4MHz[1]	4MHz	32KHz	32KHz	DIS	OFF
	ULPCLK to TIMG0/8	40MHz	32KHz		40MHz	32KHz		4MHz[1]	4MHz	32KHz	32KHz	32KHz[2]	OFF
	RTCCLK	32KHz											OFF
	MFCLK	OPT	DIS		OPT	DIS		OPT		DIS	DIS		OFF
	MFPCLK	OPT	DIS		OPT	DIS		OPT		DIS	DIS		OFF
	LFCLK to PD0/1	32KHz										DIS	OFF
	LFCLK to TIMG0/8	32KHz										32KHz[2]	OFF
	LFCLK Monitor	OPT											OFF
	MCLK Monitor	OPT										DIS	OFF
PMU	POR monitor	EN											
	BOR monitor	EN											OFF
	Core regulator	FULL DRIVE						REDUCED DRIVE			LOW DRIVE		OFF
Core Functions	CPU	EN			DIS								OFF
	DMA	OPT						DIS (triggers supported)					OFF
	Flash	EN						DIS					OFF
	SRAM	EN						DIS					OFF

Table 8-1. Supported Functionality by Operating Mode (continued)

OPERATING MODE		RUN			SLEEP			STOP			STANDBY		SHUTDOWN
		RUN0	RUN1	RUN2	SLEEP0	SLEEP1	SLEEP2	STOP0	STOP1	STOP2	STANDBY0	STANDBY1	
PD1 Peripherals	MATHACL	OPT						OFF					OFF
	UART3	OPT						DIS					OFF
	SPI0/1	OPT						DIS					OFF
	MCAN0	OPT	OFF		OPT	OFF		OFF					OFF
	TIMA0/1	OPT						OFF					OFF
	TIMG6/7/12	OPT						OFF					OFF
	AES	OPT						OFF					OFF
	CRC	OPT						DIS					OFF
	TRNG	OPT						OFF					OFF
PD0 Peripherals	GPIOA/B[3]	OPT										OPT[2]	OFF
	UART0/1/2	OPT										OPT[2]	OFF
	I2C0/1	OPT										OPT[2]	OFF
	TIMG0/8	OPT										OPT[2]	OFF
	WWDT0/1	OPT										DIS	OFF
	RTC	OPT											OFF
Analog	VREF	OPT											OFF
	ADC0/1[3]	OPT								NS (triggers supported)			OFF
	COMP0/1/2	OPT	OPT (ULP)		OPT	OPT (ULP)		OPT		OPT (ULP)			OFF
	OPA0/1	OPT	NS		OPT	NS		OPT		NS			OFF
	DAC0	OPT								NS			OFF
	GPAMP	OPT								NS			OFF
	TEMP Sensor	OPT									OFF		OFF
IOMUX and IO Wakeup		EN											DIS w/ WAKE
Wake Sources		N/A			ANY IRQ			PD0 IRQ					IOMUX, NRST, SWD

(1) If STOP0 is entered from RUN1 (SYSOSC enabled but MCLK sourced from LFCLK), SYSOSC remains enabled as it was in RUN1, and ULPCLK remains at 32KHz as it was in RUN1. If STOP0 is entered from RUN2 (SYSOSC was disabled and MCLK was sourced from LFCLK), SYSOSC remains disabled as it was in RUN2, and ULPCLK remains at 32KHz as it was in RUN2.
(2) When using the STANDBY1 policy for STANDBY, only specific peripherals (TIMG0, TIMG8, and RTC) are clocked. Other PD0 peripherals can generate an asynchronous fast clock request upon external activity but are not actively clocked.
(3) For ADCx and GPIO Ports A and B, the digital logic is in PD0 and the register interface is in PD1. These peripherals support fast single-cycle register access when PD1 is active and also support basic operation down to STANDBY mode where PD0 is still active.
(4) SYSPLL is not automatically disabled, and needs to be manually disabled through the HSCLKEN.SYSPLLEN field within the SYSCTL registers in order to reduce power consumption.

8.3 Power Management Unit (PMU)

The power management unit (PMU) generates the internally regulated core supplies for the device and provides supervision of the external supply (VDD). The PMU also contains the bandgap voltage reference used by the PMU itself as well as analog peripherals. Key features of the PMU include:

- Power-on reset (POR) supply monitor
- Brownout reset (BOR) supply monitor with early warning capability using three programmable thresholds
- Core regulator with support for RUN, SLEEP, STOP, and STANDBY operating modes to dynamically balance performance with power consumption
- Parity-protected trim to immediately generate a power-on reset (POR) in the event that a power management trim is corrupted

For more details, see the PMU chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.4 Clock Module (CKM)

The clock module provides the following oscillators:

- **LFOSC**: Internal low-frequency oscillator (32kHz)
- **SYSOSC**: Internal high-frequency oscillator (4MHz or 32MHz with factory trim, 16MHz or 24MHz with user trim)
- **LFXT/LFCKIN** : Low-frequency external crystal oscillator or digital clock input (32kHz)
- **HFXT/HFCKIN**: High-frequency external crystal oscillator or digital clock input (4 to 48MHz)
- **SYSPLL**: System phase locked loop with 3 outputs (32 to 80MHz)

The following clocks are distributed by the clock module for use by the processor, bus, and peripherals:

- **MCLK**: Main system clock for PD1 peripherals, derived from SYSOSC, LFCLK, or HSCLK, active in RUN and SLEEP modes
- **CPUCLK**: Clock for the processor (derived from MCLK), active in RUN mode
- **ULPCLK**: Ultra-low power clock for PD0 peripherals, active in RUN, SLEEP, STOP, and STANDBY modes
- **MFCLK**: 4MHz fixed mid-frequency clock for peripherals, available in RUN, SLEEP, and STOP modes
- **MFPCLK**: 4MHz fixed mid-frequency precision clock, available in RUN, SLEEP, and STOP modes
- **LFCLK**: 32kHz fixed low-frequency clock for peripherals or MCLK, active in RUN, SLEEP, STOP, and STANDBY modes
- **ADCCLK**: ADC clock, available in RUN, SLEEP and STOP modes
- **CLK_OUT**: Used to output a clock externally, available in RUN, SLEEP, STOP, and STANDBY modes
- **HFCLK**: High-frequency clock derived from HFXT or HFCLK_IN, available in RUN and SLEEP mode
- **HSCLK**: High-speed clock derived from HFCLK or the SYSPLL, available in RUN and SLEEP mode
- **CANCLK**: CAN functional clock, derived from HFCLK or SYSPLL

For more details, see the CKM chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.5 DMA

The direct memory access (DMA) controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA can be used to move data from ADC conversion memory to SRAM. The DMA reduces system power consumption by allowing the CPU to remain in low power mode, without having to awaken to move data to or from a peripheral.

The DMA in these devices support the following key features:

- 7 independent DMA transfer channels
  - 3 full-feature channel (DMA0, DMA1 and DMA2), supporting repeated transfer modes
  - 4 basic channels (DMA3, DMA4, DMA5 and DMA6) supporting single transfer modes
- Configurable DMA channel priorities

- Byte (8-bit), short word (16-bit), word (32-bit) and long word (64-bit) or mixed byte and word transfer capability
- Transfer counter block size supports up to 64k transfers of any data type
- Configurable DMA transfer trigger selection
- Active channel interruption to service other channels
- Early interrupt generation for ping-pong buffer architecture
- Cascading channels upon completion of activity on another channel
- Stride mode to support data re-organization, such as 3-phase metering applications

Table 8-3 lists the available triggers for the DMA which are configured using the DMATCTL.DMATSEL control bits in the DMA memory mapped registers.

Table 8-2. DMA Features

Feature	FULL	BASIC
Channel#	0,1,2	3,4,5,6
Repeat Mode	Yes	-
Table & Fill Mode	Yes	-
Gather Mode	-	-
Pre-IRQ	-	-
Auto Enable	-	-
Long Long (128-bit) Transfer	-	-
Stride Mode	-	-
Cascading Channel Support	-	-

Table 8-3. DMA Trigger Mapping

Trigger 0:12	Source	Trigger 13:24	Source
0	Software	13	SPI1 Publisher 1
1	Generic Subscriber 0 (FSUB_0)	14	SPI1 Publisher 2
2	Generic Subscriber 1 (FSUB_1)	15	UART3 Publisher 1
3	AES Publisher 1	16	UART3 Publisher 2
4	AES Publisher 2	17	UART0 Publisher 1
5	AES Publisher 3	18	UART0 Publisher 2
6	DAC0 Publisher 2	19	UART1 Publisher 1
7	I2C0 Publisher 1	20	UART1 Publisher 2
8	I2C0 Publisher 2	21	UART2 Publisher 1
9	I2C1 Publisher 1	22	UART2 Publisher 2
10	I2C1 Publisher 2	23	ADC0 Publisher 2
11	SPI0 Publisher 1	24	ADC1 Publisher 2
12	SPI0 Publisher 2		

For more details, see the DMA chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.6 Events

The event manager transfers digital events from one entity (for example, a peripheral) to another (for example, a second peripheral, the DMA, or the CPU). The event manager implements event transfer through a defined set of event publishers (generators) and subscribers (receivers) which are interconnected through an event fabric containing a combination of static and programmable routes.

Events that are transferred by the event manager include:

- Peripheral event transferred to the CPU as an interrupt request (IRQ) (Static Event)
  - Example: RTC interrupt is sent to the CPU
- Peripheral event transferred to the DMA as a DMA trigger (DMA Event)
  - Example: UART data receive trigger to DMA to request a DMA transfer
- Peripheral event transferred to another peripheral to directly trigger an action in hardware (Generic Event)
  - Example: TIMx timer peripheral publishes a periodic event to the ADC subscriber port, and the ADC uses the event to trigger start-of-sampling

Refer to the Event chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual* for more information.

Table 8-4. Generic Event Channels

A generic route is either a point-to-point (1:1) route or a point-to-two (1:2) splitter route in which the peripheral publishing the event is configured to use one of several available generic route channels to publish its event to another entity (or entities, in the case of a splitter route), where an entity may be another peripheral, a generic DMA trigger event, or a generic CPU event.

CHANID	Generic Route Channel Selection	Channel Type
0	No generic event channel selected	N/A
1	Generic event channel 1 selected	1 : 1
2	Generic event channel 2 selected	1 : 1
3	Generic event channel 3 selected	1 : 1
4	Generic event channel 4 selected	1 : 1
5	Generic event channel 5 selected	1 : 1
6	Generic event channel 6 selected	1 : 1
7	Generic event channel 7 selected	1 : 1
8	Generic event channel 8 selected	1 : 1
9	Generic event channel 9 selected	1 : 1
10	Generic event channel 10 selected	1 : 1
11	Generic event channel 11 selected	1 : 1
12	Generic event channel 12 selected	1 : 2 (splitter)
13	Generic event channel 13 selected	1 : 2 (splitter)
14	Generic event channel 14 selected	1 : 2 (splitter)
15	Generic event channel 15 selected	1 : 2 (splitter)

8.7 Memory

8.7.1 Memory Organization

Table 8-5 summarizes the memory map of the devices. For more information about the memory region detail, see the *Platform Memory Map* section in the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual* .

Table 8-5. Memory Organization

MEMORY REGION	SUBREGION	MSPM0G3505	MSPM0G3506	MSPM0G3507
Code (Flash)	ECC Corrected	32KB-8B (1) 0x0000.0000 to 0x0000.7FF8	64KB-8B (1) 0x0000.0000 to 0x0000.FFF8	128KB-8B (1) 0x0000.0000 to 0x0001.FFF8
	ECC Uncorrected	0x0040.0000 to 0x0040.7FF8	0x0040.0000 to 0x0040.FFF8	0x0040.0000 to 0x0041.FFF8

Table 8-5. Memory Organization (continued)

MEMORY REGION	SUBREGION	MSPM0G3505	MSPM0G3506	MSPM0G3507
SRAM (SRAM)	Parity checked	0x2010.0000 to 0x2010.3FFF	0x2010.0000 to 0x2010.7FFF	0x2010.0000 to 0x2010.7FFF
	Un-checked	0x2020.0000 to 0x2020.3FFF	0x2020.0000 to 0x2020.7FFF	0x2020.0000 to 0x2020.7FFF
	Parity code	0x2030.0000 to 0x2030.3FFF	0x2030.0000 to 0x2030.7FFF	0x2030.0000 to 0x2030.7FFF
Peripheral	Peripherals	0x4000.0000 to 0x40FF.FFFF	0x4000.0000 to 0x40FF.FFFF	0x4000.0000 to 0x40FF.FFFF
	Flash ECC Corrected	0x4100.0000 to 0x4100.8000	0x4100.0000 to 0x4101.0000	0x4100.0000 to 0x4102.0000
	Flash ECC Uncorrected	0x4140.0000 to 0x4140.8000	0x4140.0000 to 0x4141.0000	0x4140.0000 to 0x4142.0000
	Flash ECC code	0x4180.0000 to 0x4180.8000	0x4180.0000 to 0x4181.0000	0x4180.0000 to 0x4182.0000
	Configuration NVM(NONMAIN) ECC Corrected	512 bytes 0x41C0.0000 to 0x41C0.0200	512 bytes 0x41C0.0000 to 0x41C0.0200	512 bytes 0x41C0.0000 to 0x41C0.0200
	Configuration NVM(NONMAIN) ECC Uncorrected	0x41C1.0000 to 0x41C1.0200	0x41C1.0000 to 0x41C1.0200	0x41C1.0000 to 0x41C1.0200
	Configuration NVM(NONMAIN) ECC code	0x41C2.0000 to 0x41C2.0200	0x41C2.0000 to 0x41C2.0200	0x41C2.0000 to 0x41C2.0200
	FACTORY Corrected	0x41C4.0000 to 0x41C4.0080	0x41C4.0000 to 0x41C4.0080	0x41C4.0000 to 0x41C4.0080
	FACTORY Uncorrected	0x41C5.0000 to 0x41C5.0080	0x41C5.0000 to 0x41C5.0080	0x41C5.0000 to 0x41C5.0080
	FACTORY ECC code	0x41C6.0000 to 0x41C6.0080	0x41C6.0000 to 0x41C6.0080	0x41C6.0000 to 0x41C6.0080
Subsystem		0x6000.0000 to 0x7FFF.FFFF	0x6000.0000 to 0x7FFF.FFFF	0x6000.0000 to 0x7FFF.FFFF
System PPB		0xE000.0000 to 0xE00F.FFFF	0xE000.0000 to 0xE00F.FFFF	0xE000.0000 to 0xE00F.FFFF

(1) First 32KB flash memory (address 0x0000.0000 to 0x0000.8000) has up to 100000 program/erase cycles.

8.7.2 Peripheral File Map

Table 8-6 lists the available peripherals and the register base address for each.

Table 8-6. Peripherals Summary

Peripheral Name	Base Address	Size
COMP0	0x40008000	0x2000
COMP1	0x4000A000	0x2000
COMP2	0x4000C000	0x2000
DAC_OUT	0x40018000	0x2000
OPA0	0x40020000	0x2000
OPA1	0x40022000	0x2000
VREF	0x40030000	0x2000
WWDT0	0x40080000	0x2000
WWDT1	0x40082000	0x2000
TIMG0	0x40084000	0x2000
TIMG8	0x40090000	0x2000

Table 8-6. Peripherals Summary (continued)

Peripheral Name	Base Address	Size
RTC	0x40094000	0x2000
GPIO0	0x400A0000	0x2000
GPIO1	0x400A2000	0x2000
SYSCTL	0x400AF000	0x3000
DEBUGSS	0x400C7000	0x2000
EVENT	0x400C9000	0x3000
NVMNW	0x400CD000	0x2000
I2C0	0x400F0000	0x2000
I2C1	0x400F2000	0x2000
UART1	0x40100000	0x2000
UART2	0x40102000	0x2000
UART0	0x40108000	0x2000
MCPUSS	0x40400000	0x2000
MATHACL	0x40410000	0x2000
WUC	0x40424000	0x1000
IOMUX	0x40428000	0x2000
DMA	0x4042A000	0x2000
CRC	0x40440000	0x2000
AES	0x40442000	0x2000
TRNG	0x40444000	0x2000
SPI0	0x40468000	0x2000
SPI1	0x4046A000	0x2000
UART3	0x40500000	0x2000
CAN-FD	0x40508000	0x8000
ADC0	0x40000000	0x1000
ADC1	0x40002000	0x1000
ADC0(1)	0x40556000	0x1000
ADC1(1)	0x40558000	0x1000
TIMA0	0x40860000	0x2000
TIMA1	0x40862000	0x2000
TIMG6	0x40868000	0x2000
TIMG7	0x4086A000	0x2000
TIMG12	0x40870000	0x2000

(1) Aliased region of ADC0 and ADC1 memory-mapped registers

8.7.3 Peripheral Interrupt Vector

Table 8-7 shows the IRQ number and the interrupt group number for each peripherals in this device.

Table 8-7. Interrupt Vector Number

PERIPHERAL NAME	NVIC IRQ	GROUP IIDX
WWDT0	0	0
WWDT1	0	1
DEBUGSS	0	2
NVMNW	0	3
EVENT SUB PORT0	0	4
EVENT SUB PORT1	0	5
SYSCTL	0	6
GPIO0	1	0
GPIO1	1	1
COMP0	1	2
COMP1	1	3
COMP2	1	4
TRNG	1	5
TIMG8	2	-
UART3	3	-
ADC0	4	-
ADC1	5	-
CAN-FD	6	-
DAC_OUT	7	-
SPI0	9	-
SPI1	10	-
UART1	13	-
UART2	14	-
UART0	15	-
TIMG0	16	-
TIMG6	17	-
TIMA0	18	-
TIMA1	19	-
TIMG7	20	-
TIMG12	21	-
I2C0	24	-
I2C1	25	-
AES	28	-
RTC	30	-
DMA	31	-

8.8 Flash Memory

A single bank of non-volatile flash memory is provided for storing executable program code and application data.

Key features of the flash include:

- Hardware ECC protection (encode and decode) with single bit error correction and double-bit error detection
- In-circuit program and erase operations supported across the entire recommended supply range

- Small 1KB sector sizes (minimum erase resolution of 1KB)
- Up to 32 application-chosen sectors of flash address space can be used as high endurance sectors to enable EEPROM emulation applications.This includes sectors from the main bank(s) and optional data bank. In devices with data bank, it is possible to use some sectors from the data bank and the rest from the main bank(s) as high endurance sectors.On devices with <=32kB flash memory, the entire flash memory supports NWEC(HI_ENDURANCE) erase/program cycles

For a complete description of the flash memory, see the NVM chapter of the technical reference manual.

8.9 SRAM

MSPM0Gxx MCUs include a low power, high performance SRAM memory with zero wait state access across the supported CPU frequency range of the device. MSPM0Gxx MCUs also provides up to 32KB of SRAM with hardware parity. SRAM memory can be used for storing volatile information such as the call stack, heap, global data, and code. The SRAM memory content is fully retained in run, sleep, stop, and standby operating modes and is lost in shutdown mode. A write protection mechanism is provided to allow the application to prevent unintended modifications to the SRAM memory. Write protection is useful when placing executable code into SRAM as it provides a level of protection against unintentional overwrites of code by either the CPU or DMA. Placing code in SRAM can improve performance of critical loops by enabling zero wait state operation and lower power consumption.

A write-execute mutual exclusion mechanism is provided to allow the application to partition the SRAM into two sections: a read-write (RW) partition and a read-execute (RX) partition. The SRAMBOUNDARY register in SYSCTL needs to be configured to set up these partitions. The RX partition occupies the upper portion of the SRAM address space. Write protection is useful when placing executable code into SRAM as it provides a level of protection against unintentional overwrites of code by either the CPU or DMA. Placing code in SRAM can improve performance of critical loops by enabling zero wait state operation and lower power consumption. Preventing code execution from the RW partition improves security by preventing self-modifying code execution ability.

8.10 GPIO

The general purpose input/output (GPIO) peripheral provides the user with a means to write data out and read data in to and from the device pins. Through the use of the Port A and Port B GPIO peripherals, these devices support up to 60 GPIO pins.

The key features of the GPIO module include:

- 0 wait state MMR access from CPU
- Set/Clear/Toggle multiple bits without the need of a read-modify-write construct in software
- GPIOs with "Standard with Wake" drive functionality able to wake the device from SHUTDOWN mode
- "FastWake" feature enables low-power wakeup from STOP and STANDBY modes for any GPIO port
- User controlled input filtering

For more details, see the GPIO chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.11 IOMUX

The IOMUX peripheral enables IO pad configuration and controls digital data flow to and from the device pins. The key features of the IOMUX include:

- IO Pad configuration registers allow for programmable drive strength, speed, pullup-down, and more
- Digital pin muxing allows for multiple peripheral signals to be routed to the same IO pad
- Pin functions and capabilities are user-configured using the PINCM register

For more details, see the IOMUX chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.12 ADC

Both 12-bit analog-to-digital converter (ADC) modules in these devices, ADC0 and ADC1, support fast 12-bit conversions with single-ended inputs and simultaneous sampling operation.

ADC features include:

- 12-bit output resolution at 4Msps with greater than 11.1 ENOB
- HW averaging enables 14-bit effective resolution at 250ksps
- Up to 17 total external input channels with individual result storage registers
- Internal channels for temperature sensing, supply monitoring, and analog signal chain (interconnection with OPA, DAC, etc.)
- Software selectable reference:
  - Configurable internal reference voltage of 1.4V and 2.5V (requires decoupling capacitor on VREF± pins)
  - MCU supply voltage (VDD)
  - External reference supplied to the ADC through the VREF± pins
- Operates in RUN, SLEEP, and STOP modes

Table 8-8. ADC Channel Mapping

CHANNEL[0:7]	SIGNAL NAME(2)		CHANNEL[8:15]	SIGNAL NAME(1) (2)	
	ADC0	ADC1		ADC0	ADC1
0	A0_0	A1_0 / DAC_OUT(4)	8	A1_7(3)	A0_7(3)
1	A0_1	A1_1	9	-	-
2	A0_2	A1_2	10	-	-
3	A0_3	A1_3	11	*Temperature Sensor*	-
4	A0_4	A1_4	12	A0_12	*Temperature Sensor*
5	A0_5	A1_5	13	*OPA0 output*	*OPA1 output*
6	A0_6	A1_6	14	*GPAMP output*	*GPAMP output*
7	A0_7	A1_7	15	*Supply/Battery Monitor*	*Supply/Battery Monitor*

(1) *Italicized* signal names are purely internal to the SoC. These signals are used for internal peripheral interconnections.
(2) For more information about device analog connections please refer to Section 8.30
(3) Note that each channel 8 of each ADC can be sampled by the opposite ADC.
(4) When DAC_OUT is used, A1_0 cannot be used to sample external signals. Avoid using external circuitry on the PA15 pin when using DAC_OUT.

For more details, see the ADC chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.13 Temperature Sensor

The temperature sensor provides a voltage output that changes linearly with device temperature. The temperature sensor output is internally connected to one of ADC input channels to enable a temperature-to-digital conversion.

A unit-specific single-point calibration value for the temperature sensor is provided in the factory constants memory region. This calibration value represents the ADC conversion result (in ADC code format) corresponding to the temperature sensor being measured in 12-bit mode with the 3.3V VDD reference at the factory trim temperature (TS_{TRIM}). The ADC and VREF configuration for the above measurement is as the following: RES=0 (12-bit mode), VRSEL=0h (VDD), ADC t_{Sample}=12.5µs. This calibration value can be used with the temperature sensor temperature coefficient (TS_c) to estimate the device temperature. See the temperature sensor section of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual* for guidance on estimating the device temperature with the factory trim value.

8.14 VREF

The shared voltage reference module (VREF) in these devices contain a configurable voltage reference buffer which allows users to supply a stable reference to on-board analog peripherals. It also supports bringing in an external reference for applications where higher accuracy is required.

VREF features include:

- 1.4V and 2.5V user-selectable internal references
- Internal reference supports full speed ADC operation
- Support for bringing in an external reference on VREF± device pins
- Requires a decoupling capacitor placed on VREF± pins for proper operation. See VREF specification section for more details

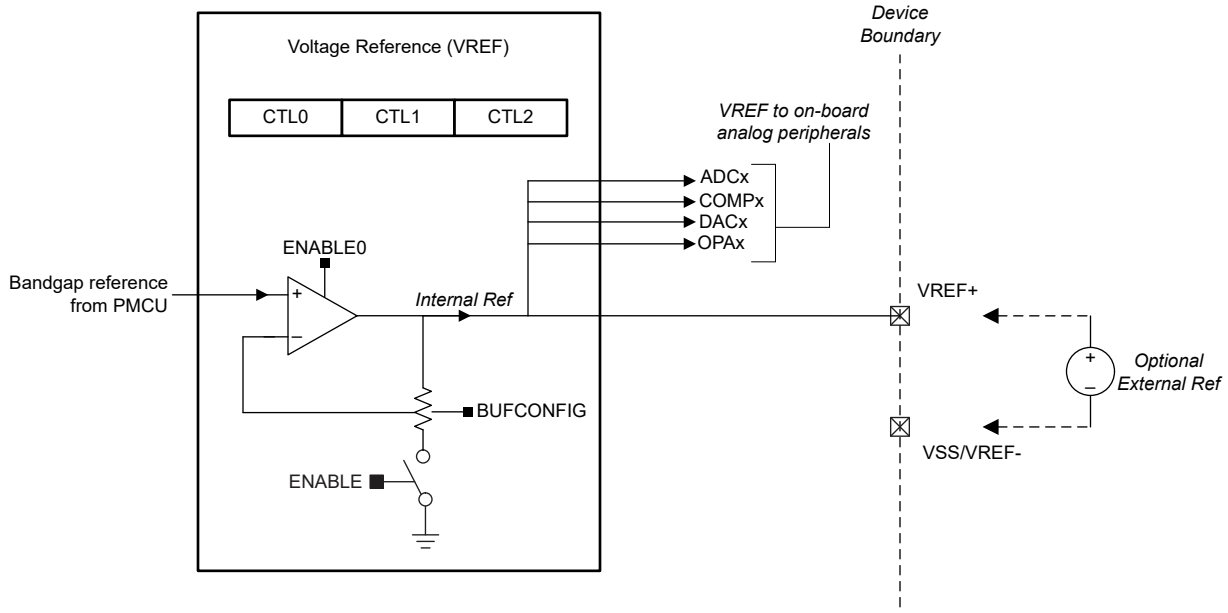


Figure 8-1. VREF Module

For more details, see the VREF chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.15 COMP

The comparator peripheral in the device compares the voltage levels on two inputs terminals and provides a digital output based on this comparison. It supports the following key features:

- Programmable hysteresis
- Programmable reference voltage:
  - External reference voltage (VREF IO)
  - Internal reference voltage (1.4V, 2.5V)
  - Integrated 8-bit reference DAC, the output can also connect to OPA input terminal internally as an output buffer.
- Configurable operation modes:
  - High speed mode
  - Lower power mode
- Programmable output glitch filter delay
- Supports 6 blanking sources (refer to the CTL2 register of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*)
- Support output wake up device from most low-power modes except the shutdown mode.
- Output connected to advanced timer fault handling mechanism

- The IPSEL and IMSEL bits in comparator registers can be used to select the comparator channel inputs from device pins or from internal analog modules.

Table 8-9. COMP Blanking Source Table

CTL2.BLANKSRC VALUE	BLANKING SOURCE
1	TIMA0.CC2
2	TIMA0.CC3
3	TIMA1.CC1
4	TIMG12.CC1
5	TIMG6.CC1
6	TIMG7.CC1

Table 8-10. COMP0 Input Channel Selection

IPSEL / IMSEL BITS	POSITIVE TERMINAL INPUT	NEGATIVE TERMINAL INPUT
0x0	COMP0_IN0+	COMP0_IN0-
0x1	COMP0_IN1+	COMP0_IN1-
0x2	COMP0_IN2+	COMP0_IN2-
0x5	DAC_OUT / COMP0_IN3+(1)	Temp Sense Output
0x6	OPA1 output	OPA0 output
0x7	COMP1 positive terminal signal	GPAMP Output

Table 8-11. COMP1 Input Channel Selection

IPSEL / IMSEL BITS	POSITIVE TERMINAL INPUT	NEGATIVE TERMINAL INPUT
0x0	COMP1_IN0+	COMP1_IN0-
0x1	COMP1_IN1+	COMP1_IN1-
0x2	COMP1_IN2+	COMP1_IN2-
0x5	DAC_OUT / COMP1_IN3+(1)	-
0x7	COMP0 positive terminal signal	GPAMP Output

Table 8-12. COMP2 Input Channel Selection

IPSEL / IMSEL BITS	POSITIVE TERMINAL INPUT	NEGATIVE TERMINAL INPUT
0x0	COMP2_IN0+	COMP2_IN0-
0x1	COMP2_IN1+	COMP2_IN1-
0x5	DAC_OUT(1)	-
0x7	-	GPAMP Output

(1) The connection to COMP0/1_IN3+ and DAC_OUT connects using the PA15 pin. When connecting DAC_OUT to COMP0/1_IN3+, avoid using external circuitry on the PA15 pin.

For more information about device analog connections, see Section 8.30.

For more details, see the COMP chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.16 DAC

The 12-bit buffered digital-to-analog converter (DAC) in these devices converts a digital input value into an analog voltage to a buffered output channel and it supports the following key features:

- Up to 1-Msps output sampling rate
- 8-bit or 12-bit voltage-output resolution
- Self-calibration option for offset error correction
- Straight binary or twos-complement data format
- Integrated sample time generator for generation of predefined sampling rates
- Integrated FIFO and support DMA operation

- One hardware trigger from event fabric for conversion
- Programmable voltage reference options:
  - Supply voltage (VDD)
  - External reference voltage (VREF IO)
  - Internal reference voltage (1.4V, 2.5V)

For more information about device analog connections, see Section 8.30.

For more details, see the DAC chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.17 OPA

The zero-drift op amps (OPAs) in these devices, OPA0 and OPA1, are chopper stabilized operational amplifiers with rail-to-rail input/output and a programmable gain stage feedback loop.

The OPA peripherals support the following key features:

- Software-selectable zero-drift chopper stabilization for improved accuracy and drift performance
- Factory trimming to remove offset error
- Burnout current source (BCS) integrated to monitor sensor health
- Programmable gain amplifier (PGA) up to 32x

The OPA features configurable input muxes P-MUX, N-MUX, and M-MUX to support various analog signal chain amplifier configurations that include general purpose, inverting, noninverting, unity gain, cascade, noninverting cascade, difference, and more. The following tables list the input channel mapping for each OPA.

Table 8-13. OPA0 Input Channel Mapping

PSEL	P-MUX INPUTS	NSEL	N-MUX INPUTS	MSEL	M-MUX INPUTS
0x0	Open	0x0	Open	0x0	Open
0x1	OPA0_IN0+	0x1	OPA0_IN0-	0x1	OPA0_IN1-
0x2	OPA0_IN1+	0x2	OPA0_IN1-	0x2	GND
0x3	DAC_OUT / OPA0_IN2+(1)	0x3	OPA1_RBOT	0x3	DAC_OUT / OPA0_IN2+(1)
0x4	DAC8.0_OUT	0x4	RTAP	0x4	OPA1_RTOP
0x5	VREF	0x5	RTOP		
0x6	OPA1_RTOP				
0x7	GPAMP Output				
0x8	GROUND				

Table 8-14. OPA1 Input Channel Mapping

PSEL	P-MUX INPUTS	NSEL	N-MUX INPUTS	MSEL	M-MUX INPUTS
0x0	Open	0x0	Open	0x0	Open
0x1	OPA1_IN0+	0x1	OPA1_IN0-	0x1	OPA1_IN1-
0x2	OPA1_IN1+	0x2	OPA1_IN1-	0x2	GND
0x3	DAC_OUT / OPA1_IN2+(1)	0x3	OPA0_RBOT	0x3	DAC_OUT / OPA1_IN2+(1)
0x4	DAC8.1_OUT	0x4	RTAP	0x4	OPA0_RTOP
0x5	VREF	0x5	RTOP		
0x6	OPA0_RTOP				
0x7	GPAMP Output				
0x8	GROUND				

(1) The connection to OPA and DAC_OUT connects using the PA15 pin. When connecting DAC_OUT to OPA, avoid using external circuitry on the PA15 pin.

For more information about device analog connections, see Section 8.30

For more details, see the OPA chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.18 GPAMP

The general-purpose amplifier (GPAMP) peripheral is a chopper-stabilized general-purpose operational amplifier with rail-to-rail input and output.

The GPAMP supports the following features:

- Software selectable chopper stabilization
- Rail-to-rail input and output
- Programmable internal unity gain feedback loop

For more details, see the ADC chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.19 TRNG

The true random number generator (TRNG) utilizes an internal circuit to generate 32-bit random numbers. The TRNG is intended to be used as a source to a deterministic random number generator (DRNG) to build a FIPS-140-2 compliant system. Key features of the TRNG include:

- Generation of 32-bit random numbers
- A new 32-bit number may be generated every 32 × 4 = 128 TRNG clock cycles
- Built-in health tests
- Available in RUN and SLEEP modes

For more details, see the TRNG chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.20 AES

The advanced encryption standard (AES) accelerator offloads AES (FIPS PUB 197) encryption and decryption operations from the CPU. Key features include:

- Support for 128-bit and 256-bit encryption keys
- On-the-fly key expansion
- Offline key generation for decryption
- Shadow register for storing the initial key for all key lengths
- DMA support for ECB, CBC, OFB, and CFB cipher modes
- AES ready interrupt generation
- Available in RUN and SLEEP modes

For more details, see the AES chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.21 CRC

The cyclical redundancy check (CRC) module provides a signature for an input data sequence. Key features of the CRC module include:

- Support for 16-bit CRC based on CRC16-CCITT
- Support for 32-bit CRC based on CRC32-ISO3309
- Support for bit reversal

For more details, see the CRC chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.22 MATHACL

The math accelerator (MATHACL) is a collection of hardware accelerated 32-bit math functions to improve system computational throughput. The MATHACL offloads mathematical calculations performed by the CPU to improve efficiency and CoreMark performance.

The following hardware functions are available in the MATHACL:

- Sine/Cosine (SINCOS)
- Arc tangent (ATAN2)
- Square root (SQRT)
- Division (DIV)
- Multiply with 32-bit result (MPY32)
- Square with 32-bit result (SQUARE32)
- Multiply with 64-bit result (MPY64)
- Square with 64-bit result (SQUARE64)
- Multiply-accumulate (MAC)
- Square-accumulate (SAC)

For more details, see the MATHACL chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.23 UART

The UART peripherals (UART0, UART1, UART2, and UART3) provide the following key features:

- Standard asynchronous communication bits for start, stop, and parity
- Fully programmable serial interface
  - 5, 6, 7 or 8 data bits
  - Even, odd, stick, or no-parity bit generation and detection
  - 1 or 2 stop bit generation
  - Line-break detection
  - Glitch filter on the input signals
  - Programmable baud rate generation with oversampling by 16, 8 or 3
  - Local Interconnect Network (LIN) mode support
- Separated transmit and receive FIFOs support DAM data transfer
- Support transmit and receive loopback mode operation
- See Table 8-15 for detail information on supported protocols

Table 8-15. UART Features

UART Features	UART0 (Extend)	UART1 and 2 (Main)	UART3 (Main)
Active in Stop and Standby Mode	Yes	Yes	-
Separate transmit and receive FIFOs	Yes	Yes	Yes
Support hardware flow control	Yes	Yes	Yes
Support 9-bit configuration	Yes	Yes	Yes
Support LIN mode	Yes	-	-
Support DALI	Yes	-	-
Support IrDA	Yes	-	-
Support ISO7816 Smart Card	Yes	-	-
Support Manchester coding	Yes	-	-

For more details, see the UART chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.24 I2C

The inter-integrated circuit interface (I^2C) peripherals in these devices provide bidirectional data transfer with other I2C devices on the bus and support the following key features:

- 7-bit and 10-bit addressing mode with multiple 7-bit target addresses
- Multiple-controller transmitter or receiver mode
- Target receiver or transmitter mode with configurable clock stretching
- Support Standard-mode (Sm), with a bit rate up to 100 kbit/s

- Support Fast-mode (Fm), with a bit rate up to 400 kbit/s
- Support Fast-mode Plus (Fm+), with a bit rate up to 1 Mbit/s
  - Supported on open drain IOs (ODIO) and high-drive (HDIO) IOs only
- Separated transmit and receive FIFOs support DMA data transfer
- Support SMBus 3.0 with PEC, ARP, timeout detection and host support
- Wakeup from low power mode on address match
- Support analog and digital glitch filter for input signal glitch suppression
- 8-entry transmit and receive FIFOs

For more details, see the I2C chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.25 SPI

The serial peripheral interface (SPI) peripherals in these devices support the following key features:

- Support MCLK/2 bit rate and up to 32Mbps in both controller and peripheral mode [1]
- Configurable as a controller or a peripheral
- Configurable chip select for both controller and peripheral
- Programmable clock prescaler and bit rate
- Programmable data frame size from 4 bits to 16 bits (controller mode) and 7 bits to 16 bit (peripheral mode)
- Supports PACKEN feature that allows the packing of two 16 bit FIFO entries into a 32-bit value to improve CPU performance
- Transmit and receive FIFOs (four entries each with 16 bits per entry) supporting DMA data transfer
- Supports TI mode, Motorola mode and National Microwire format

For more details, see the SPI chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.26 CAN-FD

The controller area network (CAN) controller enables communication with a CAN2.0A, CAN2.0B, or CAN-FD bus and is compliant to ISO 11898-1:2015 standard supporting up to 5Mbit/s bit rate. Key features of the CAN-FD peripheral include:

- Full support for 64-byte CAN-FD frames
- Dedicated 1KB message SRAM with ECC
- Configurable transmit FIFO, transmit queue and event FIFO (up to 32 elements)
- Up to 32 dedicated transmit buffers and 64 dedicated receive buffers
- Two configurable receive FIFOs (up to 64 elements each)
- Up to 128 filter elements
- Two interrupt lines
- Power-down and wake-up support
- Timestamp counter

For more details, see the CAN-FD chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.27 WWDT

The windowed watchdog timer (WWDT) can be used to supervise the operation of the device, specifically code execution. The WWDT can be used to generate a reset or an interrupt if the application software does not successfully reset the watchdog within a specified window of time. Key features of the WWDT include:

- 25-bit counter
- Programmable clock divider
- Eight software selectable watchdog timer periods
- Eight software selectable window sizes
- Support for stopping the WWDT automatically when entering a sleep mode

[1] Only SPI signals on HSIO pins support data rate > 16Mbps; see the *Pin Diagrams* section for HSIO pins.

- Interval timer mode for applications which do not require watchdog functionality

For more details, see the WWDT chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.28 RTC

The real-time clock (RTC) operates off of a 32kHz input clock source (typically a low frequency crystal) and provides a time base to the application with multiple options for interrupts to the CPU. Key features of the RTC include:

- Counters for seconds, minutes, hours, day of the week, day of the month, month, and year
- Binary or BCD format
- Leap-year handling
- One customizable alarm interrupt based on minute, hour, day of the week, and day of the month
- Interval alarm interrupt to wake every minute, every hour, at midnight, or at noon
- Interval alarm interrupt providing periodic wake-up at 4096, 2048, 1024, 512, 256, or 128Hz
- Interval alarm interrupt providing periodic wake-up at 64, 32, 16, 8, 4, 2, 1, and 0.5Hz
- Calibration for crystal offset error (up to ± 240ppm)
- Compensation for temperature drift (up to ± 240ppm)
- RTC clock output to pin for calibration

For more details, see the RTC chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.29 Timers (TIMx)

The timer peripherals in these devices support the following key features, for specific configuration see Table 8-16:

Specific features for the general-purpose timer (TIMGx) include:

- 16-bit and 32-bit timers with up, down or up-down counting modes, with repeat-reload mode
- Selectable and configurable clock source
- 8-bit programmable prescaler to divide the counter clock frequency
- Two independent CC channels for
  - Output compare
  - Input capture
  - PWM output
  - One-shot mode
- Shadow CC register available in TIMG6, TIMG7 and TIMG12
- Shadow load register available in TIMG6, TIMG7
- Support quadrature encoder interface (QEI) for positioning and movement sensing available in TIMG8
- Support synchronization and cross trigger among different TIMx instances in the same power domain
- Support interrupt/DMA trigger generation and cross peripherals (such as ADC) trigger capability
- Cross trigger event logic for Hall sensor inputs (TIMG8)

Specific features for the advanced timer (TIMAx) include:

- 16-bit timer with up, down or up-down counting modes, with repeat-reload mode
- Selectable and configurable clock source
- 8-bit programmable prescaler to divide the counter clock frequency
- Repeat counter to generate an interrupt or event only after a given number of cycles of the counter
- Up to four independent CC channels for
  - Output compare
  - Input capture
  - PWM output
  - One-shot mode
- Internal fifth and sixth internal CC channel for capture/compare events
- Shadow register for load and CC register available in both TIMA0 and TIMA1

- Complementary output PWM
- Asymmetric PWM with programmable dead band insertion
- Fault handling mechanism to ensure the output signals in a safe user-defined state when a fault condition is encountered
- Support synchronization and cross trigger among different TIMx instances in the same power domain
- Support interrupt and DMA trigger generation and cross peripherals (such as ADC) trigger capability
- Two additional capture/compare channels for internal events

Table 8-16. TIMx Configurations

TIMER NAME	POWER DOMAIN	RESOLUTION	PRESCALER	REPEAT COUNTER	CAPTURE / COMPARE CHANNELS	PHASE LOAD	SHADOW LOAD	SHADOW CC	DEADBAND	FAULT	QEI
TIMG0	PD0	16-bit	8-bit	–	2	–	–	–	–	–	–
TIMG6	PD1	16-bit	8-bit	–	2	–	Yes	Yes	–	–	–
TIMG7	PD1	16-bit	8-bit	–	2	–	Yes	Yes	–	–	–
TIMG8	PD0	16-bit	8-bit	–	2	–	–	–	–	–	Yes
TIMG12	PD1	32-bit	–	–	2	–	–	Yes	–	–	–
TIMA0	PD1	16-bit	8-bit	8-bit	4	Yes	Yes	Yes	Yes	Yes	–
TIMA1	PD1	16-bit	8-bit	8-bit	2	Yes	Yes	Yes	Yes	Yes	–

Table 8-17. TIMx Cross Trigger Map (PD1)

TSEL.ETSEL Selection	TIMA0	TIMA1	TIMG6	TIMG7	TIMG12
0	TIMA0.TRIG0	TIMA0.TRIG0	TIMA0.TRIG0	TIMA0.TRIG0	TIMA0.TRIG0
1	TIMA1.TRIG0	TIMA1.TRIG0	TIMA1.TRIG0	TIMA1.TRIG0	TIMA1.TRIG0
2	TIMG6.TRIG0	TIMG6.TRIG0	TIMG6.TRIG0	TIMG6.TRIG0	TIMG6.TRIG0
3	TIMG7.TRIG0	TIMG7.TRIG0	TIMG7.TRIG0	TIMG7.TRIG0	TIMG7.TRIG0
4	TIMG12.TRIG0	TIMG12.TRIG0	TIMG12.TRIG0	TIMG12.TRIG0	TIMG12.TRIG0
5	TIMG8.TRIG0	TIMG8.TRIG0	TIMG8.TRIG0	TIMG8.TRIG0	TIMG8.TRIG0
6 to 15	Reserved				
16	Event Subscriber Port 0 (FSUB0)				
17	Event Subscriber Port 1 (FSUB1)				
18-31	Reserved				

Table 8-18. TIMx Cross Trigger Map (PD0)

TSEL.ETSEL SELECTION	TIMG0	TIMG8
0	TIMG0.TRIG0	TIMG0.TRIG0
1	TIMG8.TRIG0	TIMG8.TRIG0
2 to 15	Reserved	
16	Event Subscriber Port 0 (FSUB0)	
17	Event Subscriber Port 1 (FSUB1)	
18-31	Reserved	

For more details, see the TIMx chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.30 Device Analog Connections

Figure 8-2 shows the internal analog connection of the device.

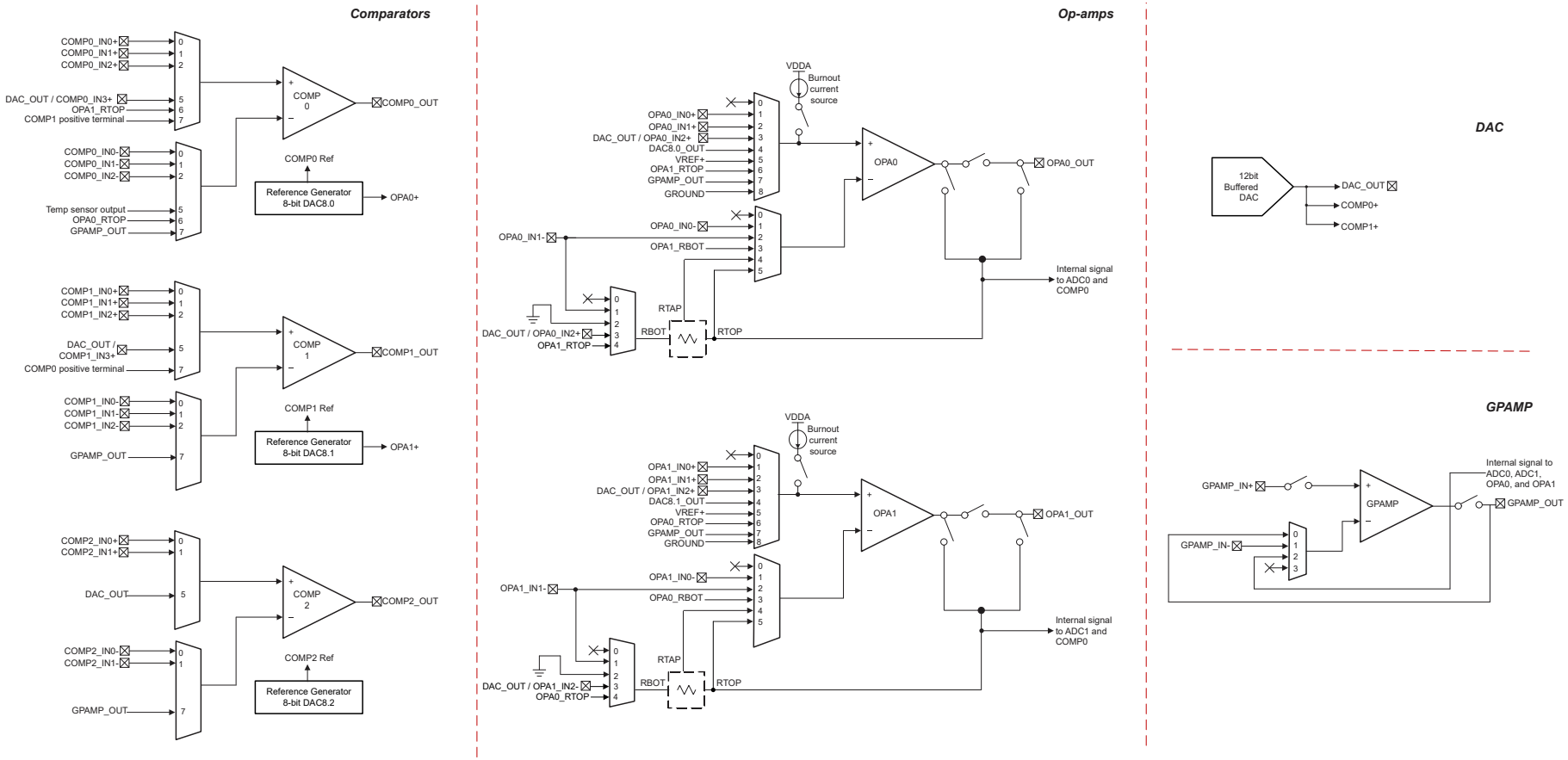


Figure 8-2. Device Analog Connections

Note

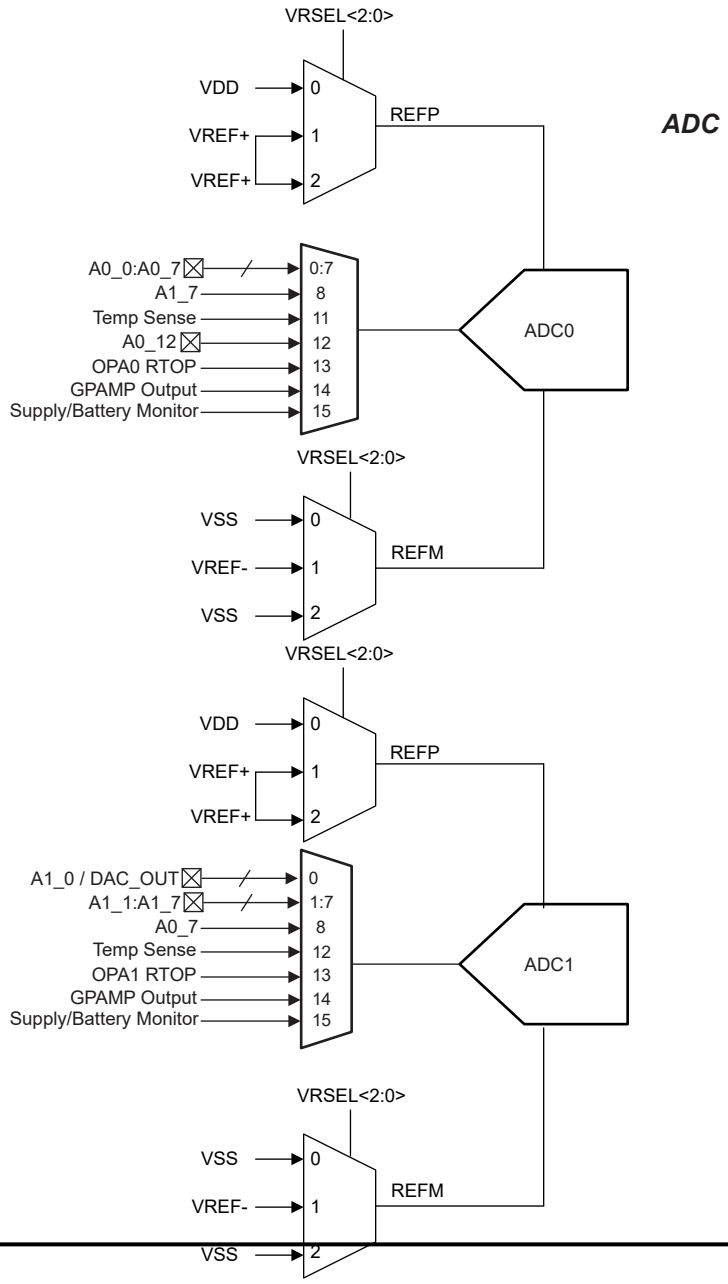


Figure 8-3. Device Analog Connections (ADC0 and ADC1)

Enabling DAC_OUT connects to PA15 therefore it is not recommended to have any external signal on PA15 when using DAC_OUT.

8.31 Input/Output Diagrams

The IOMUX manages the selection of which peripheral function is to be used on a digital IO. It also provides the controls for the output driver, input path, and the wake-up logic for wakeup from SHUTDOWN mode. For more information, refer to the IOMUX section of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

The mixed-signal IO pin slice diagram for a full featured IO pin is shown in Figure 8-4. Not all pins will have analog functions, wake-up logic, drive strength control, and pullup or pulldown resistors available. See the device-specific data sheet for detailed information on what features are supported for a specific pin.

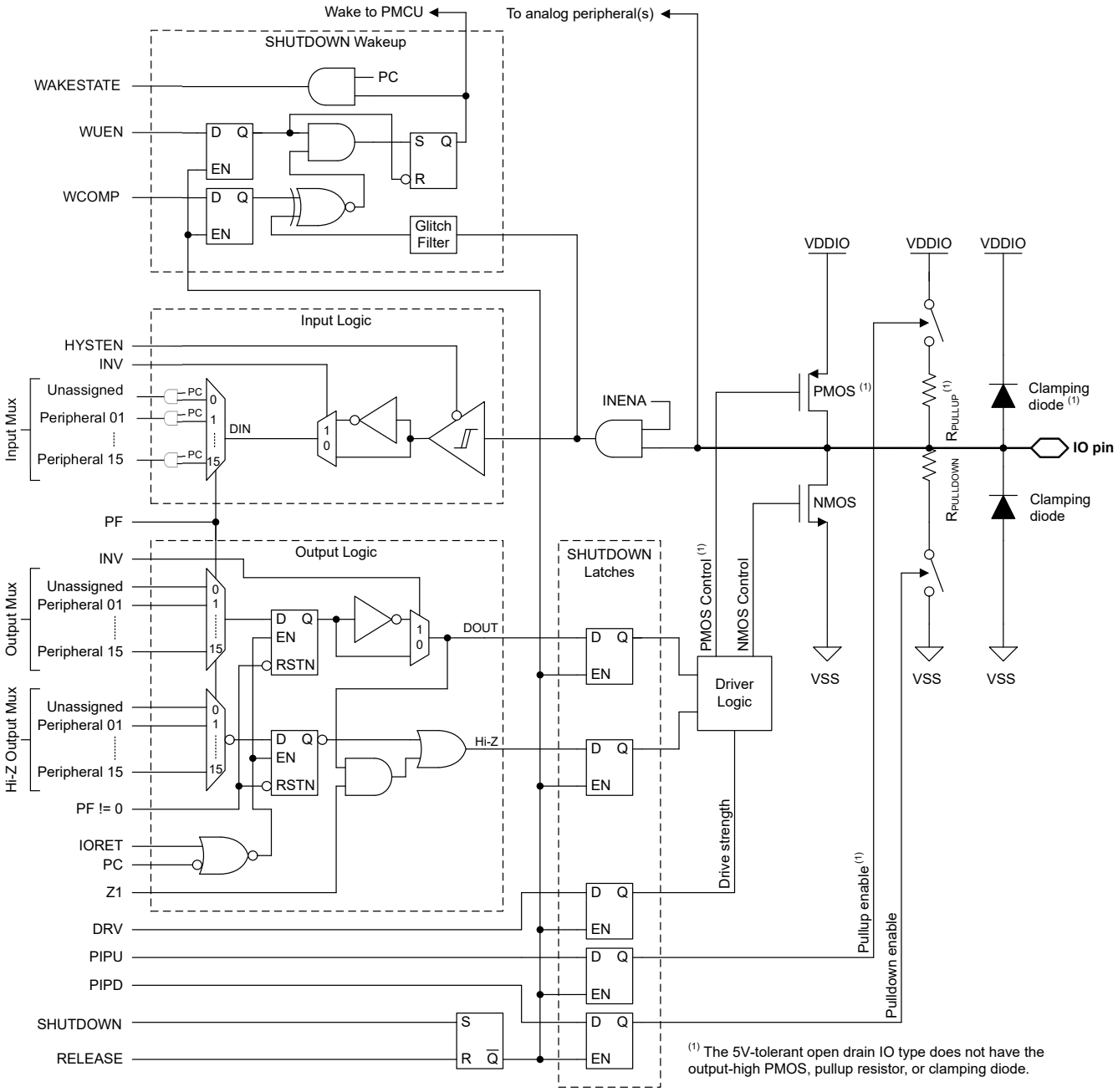


Figure 8-4. Superset Input/Output Diagram

8.32 Serial Wire Debug Interface

A serial wire debug (SWD) two-wire interface is provided via an Arm compatible serial wire debug port (SW-DP) to enable access to multiple debug functions within the device. For a complete description of the debug functionality offered on MSPM0 devices, see the debug chapter of the technical reference manual.

Table 8-19. Serial Wire Debug Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	SWD FUNCTION
SWCLK	Input	Serial wire clock from debug probe
SWDIO	Input/Output	Bi-directional (shared) serial wire data

8.33 Bootstrap Loader (BSL)

The bootstrap loader (BSL) enables configuration of the device as well as programming of the device memory through a UART or I2C serial interface. Access to the device memory and configuration through the BSL is protected by a 256-bit user-defined password, and it is possible to completely disable the BSL in the device configuration, if desired. The BSL is enabled by default from TI to support use of the BSL for production programming.

A minimum of two pins are required to use the BSL: the BSLRX and BSLTX signals (for UART), or the BSLSCL and BSLSDA signals (for I^2C). Additionally, one or two additional pins (BSL_invoke and NRST) may be used for controlled invocation of the bootloader by an external host.

If enabled, the BSL may be invoked (started) in the following ways:

- The BSL is invoked during the boot process if the BSL_invoke pin state matches the defined BSL_invoke logic level. If the device fast boot mode is enabled, this invocation check is skipped. An external host can force the device into the BSL by asserting the invoke condition and applying a reset pulse to the NRST pin to trigger a BOOTRST, after which the device will verify the invoke condition during the reboot process and start the BSL if the invoke condition matches the expected logic level.
- The BSL is automatically invoked during the boot process if the reset vector and stack pointer are left unprogrammed. As a result, a blank device from TI will invoke the BSL during the boot process without any need to provide a hardware invoke condition on the BSL_invoke pin. This enables production programming using just the serial interface signals.
- The BSL may be invoked at runtime from application software by issuing a SYSRST with BSL entry command.

Table 8-20. BSL Pin Requirements and Functions

DEVICE SIGNAL	CONNECTION	BSL FUNCTION
BSLRX	Required for UART	UART receive signal (RXD), an input
BSLTX	Required for UART	UART transmit signal (TXD) an output
BSLSCL	Required for I2C	I^2C BSL clock signal (SCL)
BSLSDA	Required for I2C	I^2C BSL data signal (SDA)
BSL_invoke	Optional	Active-high digital input used to start the BSL during boot
NRST	Optional	Active-low reset pin used to trigger a reset and subsequent check of the invoke signal (BSL_invoke)

For a complete description of the BSL functionality and command set, see the *MSPM0 Bootloader User's Guide*.

8.34 Device Factory Constants

All devices include a memory-mapped FACTORY region which provides read-only data describing the capabilities of a device as well as any factory-provided trim information for use by application software. Please refer to Factory Constants chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual* for more information.

Table 8-21. DEVICEID

DEVICEID address is 0x41C4.0004, PARTNUM is bit 12 to 27, MANUFACTURER is bit 1 to 11.

Device	PARTNUM	MANUFACTURER
MSPM0G3505	0xBB88	0x17
MSPM0G3506	0xBB88	0x17
MSPM0G3507	0xBB88	0x17

Table 8-22. USERID

USERID address is 0x41C4.0008, PART is bit 0 to 15, VARIANT is bit 16 to 23

Device	PART	VARIANT	Device	PART	VARIANT
M0G3507QPMRQ1	0x34E0	0x26	M0G3506QRHBRQ1	0xEE12	0xFC
M0G3507QRGZRQ1	0x34E0	0xC5	M0G3506QDGS32RQ1	0xEE12	0x6C
M0G3507QSPTRQ1	0x34E0	0xE3	M0G3506QDGS28RQ1	0xEE12	0x71
M0G3507QRHBRQ1	0x34E0	0xAC	M0G3505QPMRQ1	0x704E	0x7B
M0G3507QDGS32RQ1	0x34E0	0xF6	M0G3505QRGZRQ1	0x704E	0xC9
M0G3507QDGS28RQ1	0x34E0	0xEA	M0G3505QPTRQ1	0x704E	0x9C
M0G3506QPMRQ1	0xEE12	0x7B	M0G3505QRHBRQ1	0x704E	0x26
M0G3506QRGZRQ1	0xEE12	0xD2	M0G3505QDGS32RQ1	0x704E	0x7F
M0G3506QPTRQ1	0xEE12	0x5A	M0G3505QDGS28RQ1	0x704E	0x4C

8.35 Identification

Revision and Device Identification

The hardware revision and device identification values are stored in the memory-mapped FACTORY region, refer to Device Factory Constants section, which provides read-only data describing the capabilities of a device as well as any factory-provided trim information for use by application software. Refer to Factory Constants chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual* for more information. To identify the ROM (firmware) version the address 32'h01000048 can be accessed.

The device revision and identification information are also included as part of the top-side marking on the device package. The device-specific errata sheet describes these markings (see Section 10.4).

9 Applications, Implementation, and Layout

9.1 Typical Application

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1.1 Schematic

TI recommends connecting a combination of a 10µF and a 0.1µF low-ESR ceramic decoupling capacitor across the VDD and VSS pins, as well as placing these capacitors as close as possible to the supply pins that they decouple (within a few millimeters) to achieve a minimal loop area. The 10µF bulk decoupling capacitor is a recommended value for most applications, but this capacitance can be adjusted if needed based upon the PCB design and application requirements. For example, larger bulk capacitors can be used, but this can affect the supply rail ramp-up time.

The NRST reset pin must be pulled up to VDD (supply level) for the device to release from RESET state and start the boot process. TI recommends connecting an external 47kΩ pullup resistor with a 10nF pulldown capacitor for most applications, enabling the NRST pin to be controlled by another device or a debug probe.

The SYSOSC frequency correction loop (FCL) circuit utilizes an external 100kΩ with 0.1% tolerance resistor with a temperature coefficient (TCR) of 25ppm/C or better populated between the ROSC pin and VSS. This resistor establishes a reference current to stabilize the SYSOSC frequency through a correction loop. This resistor is required if the FCL feature is used for higher accuracy, and it is not required if the SYSOSC FCL is not enabled. When the FCL mode is not used, the PA2 pin can be used as a digital input/output pin.

A 0.47µF tank capacitor is required for the VCORE pin and must be placed close to the device with minimum distance to the device ground. Do not connect other circuits to the VCORE pin.

For the 5V-tolerant open drain (ODIO), a pullup resistor is required to output high for I2C and UART functions, as the open drain IO only implement a low-side NMOS driver and no high-side PMOS driver. The 5V-tolerant open drain IOs are fail-safe and can have a voltage present even if VDD is not supplied.

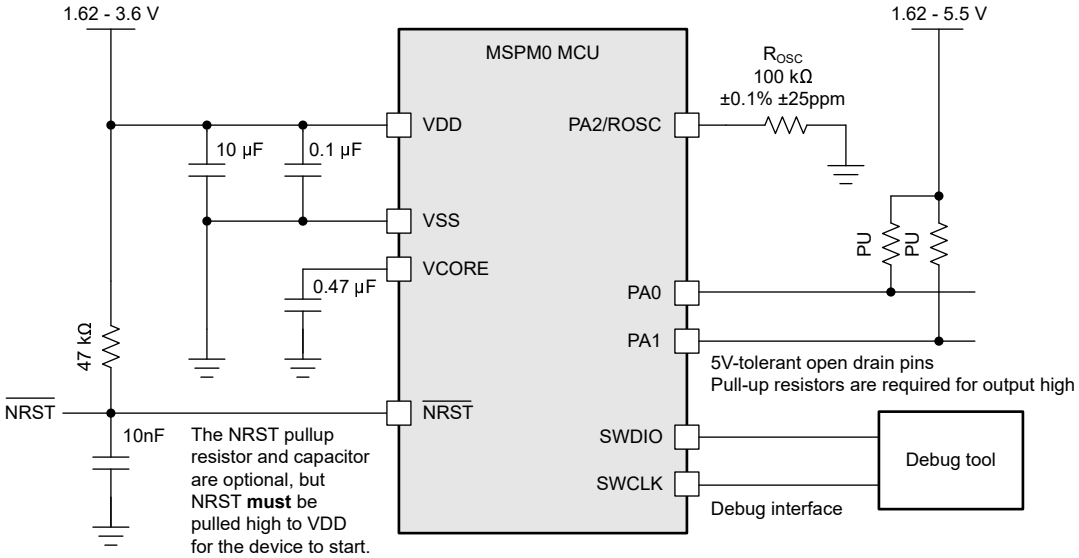


Figure 9-1. Basic Application Schematic

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Getting Started and Next Steps

For more information on the MSP low-power microcontrollers and the tools and libraries that are available to help with development, visit the Texas Instruments *Arm Cortex-M0+ MCUs* page.

10.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP MCU devices and support tools. . Each MSP MCU commercial family member has one of two prefixes: M0 or X. These prefixes represent evolutionary stages of product development from engineering prototypes (X) through fully qualified production devices (M0).

X or XMS – Experimental device that is not necessarily representative of the final device's electrical specifications

M0 – Fully qualified production device

X and XMS – Devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes." MSP devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies. Predictions show that prototype devices (X) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the temperature range, package type, and distribution format. Figure 10-1 provides a legend for reading the complete device name.

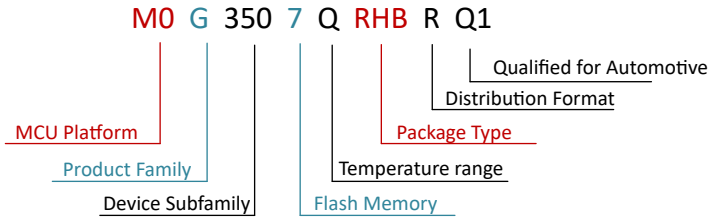


Figure 10-1. Device Nomenclature

Table 10-1. Device Nomenclature

MCU Platform	M0M0 = Arm based 32-bit M0+ XM0 = Experimental silicon Arm-based 32-bit M0+
Product Family	G = 80MHz frequency
Device Subfamily	350 = CAN-FD, 2x ADC, 2x OPA, 3x COMP
Flash Memory	5 = 32KB 6 = 64KB 7 = 128KB
Temperature Range	Q = –40°C to 125°C, AEC-Q100 qualified
Package Type	See the Device Comparison section and https://www.ti.com/packaging
Distribution Format	R = Large reel

Table 10-1. Device Nomenclature (continued)

Qualification	Q1 = Qualified for automotive applications

For orderable part numbers of MSP devices in different package types, see the Package Option Addendum of this document, ti.com, or contact your TI sales representative.

10.3 Tools and Software

Design Kits and Evaluation Modules

MSPM0 LaunchPad (LP) Boards: LP-MSPM0G3507	Empowers you to immediately start developing on the industry's best integrated analog and most cost-optimized general purpose MSPM0 MCU family. Exposes all device pins and functionality; includes some built-in circuitry, out-of-box software demos, and on-board XDS110 debug probe for programming/debugging/ EnergyTrace. The LP ecosystem includes dozens of BoosterPack stackable plug-in modules to extend functionality.
Embedded Software	
MSPM0 Software Development Kit (SDK)	Contains software drivers, middleware libraries, documentation, tools, and code examples that create a familiar and easy user experience for all MSPM0 devices.
MSP Software Diagnostics Library	Collection of functional safety software to assist customers to meet their functional safety requirements .
Software Development Tools	
TI Developer Zone	Start your evaluation and development on a web browser without any installation. Cloud tools also have a downloadable, offline version.
TI Resource Explorer	Online portal to TI SDKs. Accessible in CCS IDE or in TI Cloud Tools.
SysConfig	Intuitive GUI to configure device and peripherals, resolve system conflicts, generate configuration code, and automate pin mux settings. Accessible in CCS IDE ,in TI Cloud Tools or a standalone version. (offline version)
MSP Academy	Great starting point for all developers to learn about the MSPM0 MCU Platform with training modules that span a wide range of topics. Part of TIRex.
GUI Composer	GUIs that simplify evaluation of certain MSPM0 features, such as configuring and monitoring a fully integrated analog signal chain without any code needed.
IDE & compiler toolchains	
Code Composer Studio™ (CCS)	Code Composer Studio is an integrated development environment (IDE) for TI's microcontrollers and processors. It comprises a suite of tools used to develop and debug embedded applications. CCS is completely free to use and is available on Eclipse and Theia frameworks.
IAR Embedded Workbench® IDE	IAR Embedded Workbench for Arm delivers a complete development toolchain for building and debugging embedded applications for MSPM0.The included IAR C/C++ Compiler generates highly optimized code for your application, and the C-SPY Debugger is a fully integrated debugger for source and disassembly level debugging with support for complex code and data breakpoint.
Keil® MDK IDE	Arm Keil MDK is a complete debugger and C/C++ compiler toolchain for building and debugging embedded applications for MSPM0.Keil MDK includes a fully integrated debugger for source and disassembly level debugging. MDK provides full CMSIS compliance.
TI Arm-Clang	TI Arm Clang is included in the Code Composer Studio IDE.

GNU Arm Embedded Toolchain	The MSPM0 SDK supports development using the open-source Arm GNU Toolchain. Arm GCC is supported by Code Composer Studio IDE (CCS).

10.4 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The following documents describe the MSPM0 MCUs. Copies of these documents are available on the Internet at www.ti.com.

Technical Reference Manual

MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual	This manual describes the modules and peripherals of the MSPM0G family of devices. Each description presents the module or peripheral in a general sense. Not all features and functions of all modules or peripherals are present on all devices. In addition, modules or peripherals can differ in their exact implementation on different devices. Pin functions, internal signal connections, and operational parameters differ from device to device. See the device-specific data sheet for these details.

10.5 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.6 Trademarks

LaunchPad™, Code Composer Studio™, and TI E2E™ are trademarks of Texas Instruments.
Arm® and Cortex® are registered trademarks of Arm Limited.
All trademarks are the property of their respective owners.

10.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.8 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

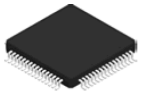
Changes from May 31, 2024 to September 30, 2025 (from Revision (May 2024) to Revision (September 2025)) **Page**

- Added comlementary output to the advanced timer feature description ... 1
- Added WWDT acronym to the windowed watch dog timer feature description ... 1
- Added pitch and package identifier details to package options list ... 1
- Changed communications feature section formatting for clarity ... 1
- Added "open drain" to 5V IO description ... 1
- Added "GPAMP" to list of analog peripherals with internal connections ... 1
- Added number of high speed IOs to Flexible I/O Features section ... 1

- Updated Optimized Low-Power Mode section ... 1
- Updated functional safety branding to indicate ASIL B compliance ... 1
- Updated Features page to match supply current characteristics electrical specifications ... 1
- Changed VSSOP width from 3mm to 4.9mm to account for leads ... 7
- Added package pitch information ... 7
- Removed wildcard from part number ... 7
- Updated comparison table values ... 7
- Added "R" to OPNs to designate distribution format ... 7
- Moved Digital Features by IO Type table to beginning of Pin Attributes section ... 13
- Added pin type information to the beginning of the Signal Description section ... 16
- Added footnote to absolute maximum ratings section for diode current injection limitation on PA21 GPIO pin ... 27
- Added I_VDD/I_VSS missing footnote to absolute maximum ratings for lower current at VDD=1.62V ... 27
- Updated LFOSC start-up time specification from 1.7ms to 1ms ... 27
- Updated Digital IO VOL specification for HSIO to correctly reference temperature condition to match with other IO types for this spec ... 27
- Updated Digital IO Electrical specifications and Switching specifications sections with added footnote for series current limiting resistor when using HDIO in DRV=1 drive strength setting ... 27
- Added Digital IO switching specifications line item for port output frequency for HDIO operation with DRV=1 drive strength setting ... 27
- Added condition for comparator electrical specifications section on I_comp specification HCYCLE register setting ... 27
- Updated power-on reset voltage level specifications ... 31
- Updated BOR COLD specification section ... 31
- Changed the VBOR0- falling from 1.56 to 1.55 ... 31
- Added SLEEP0 wakeup time ... 33
- Changed "fSYSOSC additional undershoot accuracy during tsettle" min from -11 to -16 ... 34
- Changed SYSPLLCLK0/1from 1MHz to 2.5MHz ... 35
- Changed SYSPLL RMS cycle-to-cycle jitter from 24ps to 60ps ... 35
- Changed the SYSPLL typical start up time from 14us to 7us, and the maximum start up time from 24us to 18us ... 35
- Changed VDD ≥ 2.7V, DRV = 1, CL= 20pF specification from 40MHz to 32MHz ... 40
- 32Changed VDD ≥ 2.7V, DRV = 1, CL= 20pF specification from 40MHz to 32MHz ... 40
- Changed I_VBST from 0.7uA to 0.8uA ... 40
- Added "f_in = 10KHz" test condition ... 40
- Changed V_SupplyMon max from 1% to 1.5% ... 40
- Changed offset error from +/-2mV to +/-3.5mV ... 42
- Changed gain error from +/-3LSB to +/-4LSB ... 42
- Changed temperature sensor settling time from 10us to 12.5us ... 43
- Added COMP + VREF current consumption in low power mode ... 44
- Changed COMP low power mode current consumption from 0.84uA to 0.85uA ... 44
- Changed COMP IDD from 102uA to 120uA ... 44
- Split parameter section of comparator current consumption section ... 44
- Changed COMP+VREF low power mode IDD spec from 2.5uA to 3.5uA ... 44
- Added DAC code test condition ... 44
- Changed DAC IDD from 300uA to 400uA ... 44
- Added V_o = 0.3V to VDD-0.3V test condition ... 45
- Removed +/- from output load current and only made it +4mA ... 46
- Changed non- inverting gain error (Gain=32) from (-2.6% to +2.6%) to (-3.2% to +2%) ... 49
- Changed inverting gain error (Gain=-31) from (-2.7% to +2.7%) to (-3.3% to +2.1%) ... 49
- Updated table with accurate details ... 54
- Changed the temperature sensor calibration condition from 1.4V to 3.3V with the correct register configuration setting ... 64

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

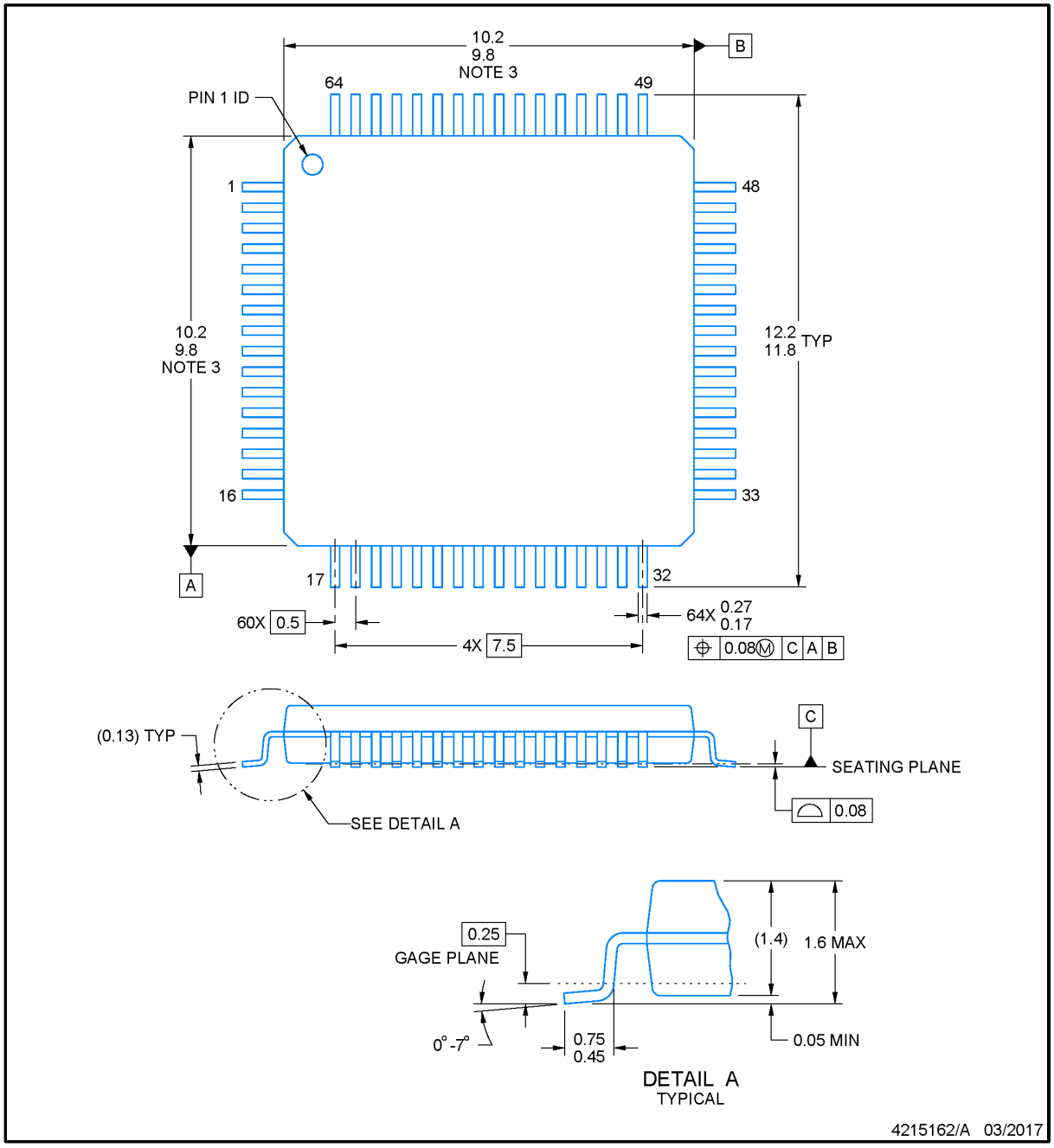


PACKAGE OUTLINE

PM0064A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



NOTES:

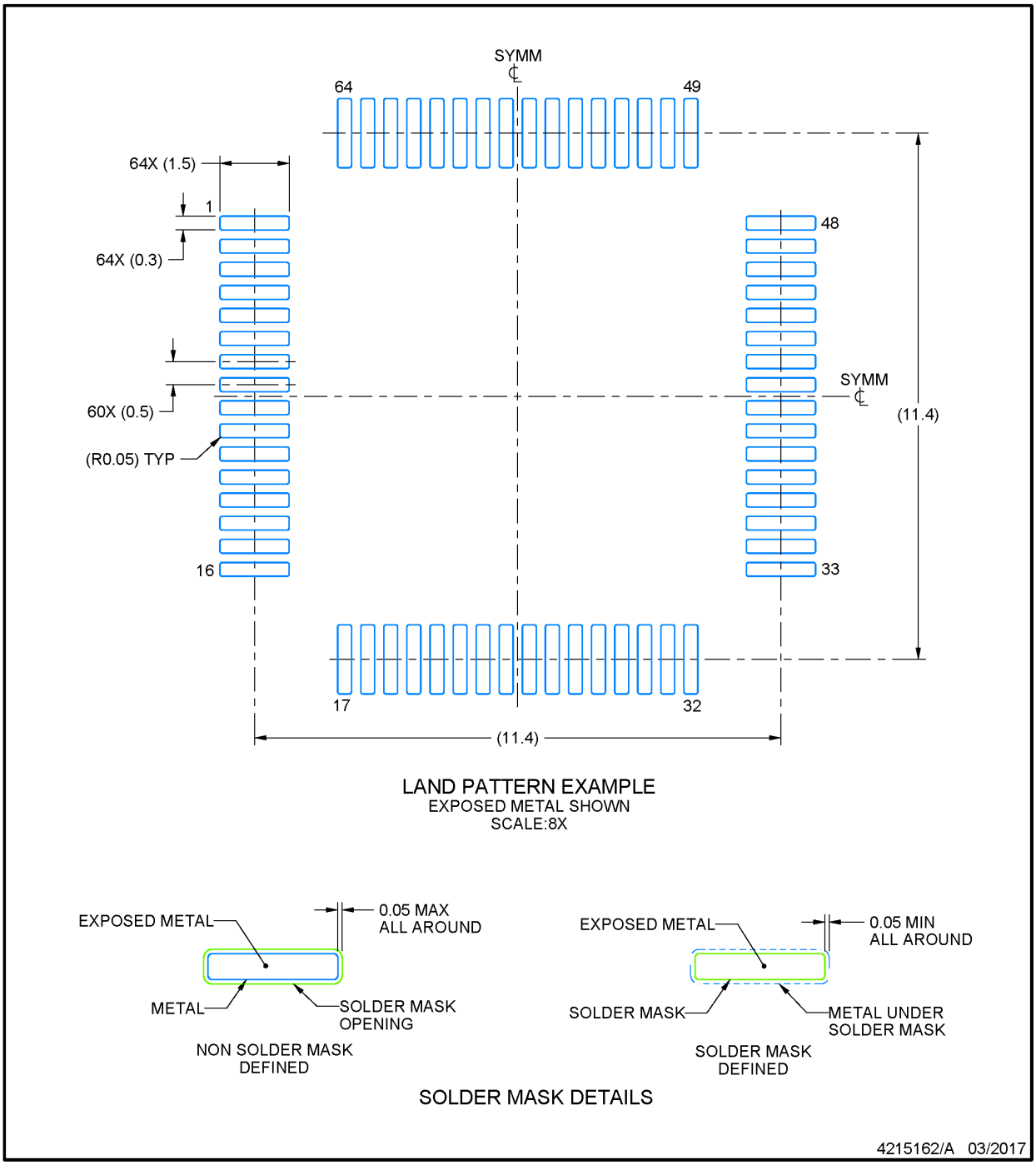
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.

EXAMPLE BOARD LAYOUT

PM0064A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



NOTES: (continued)

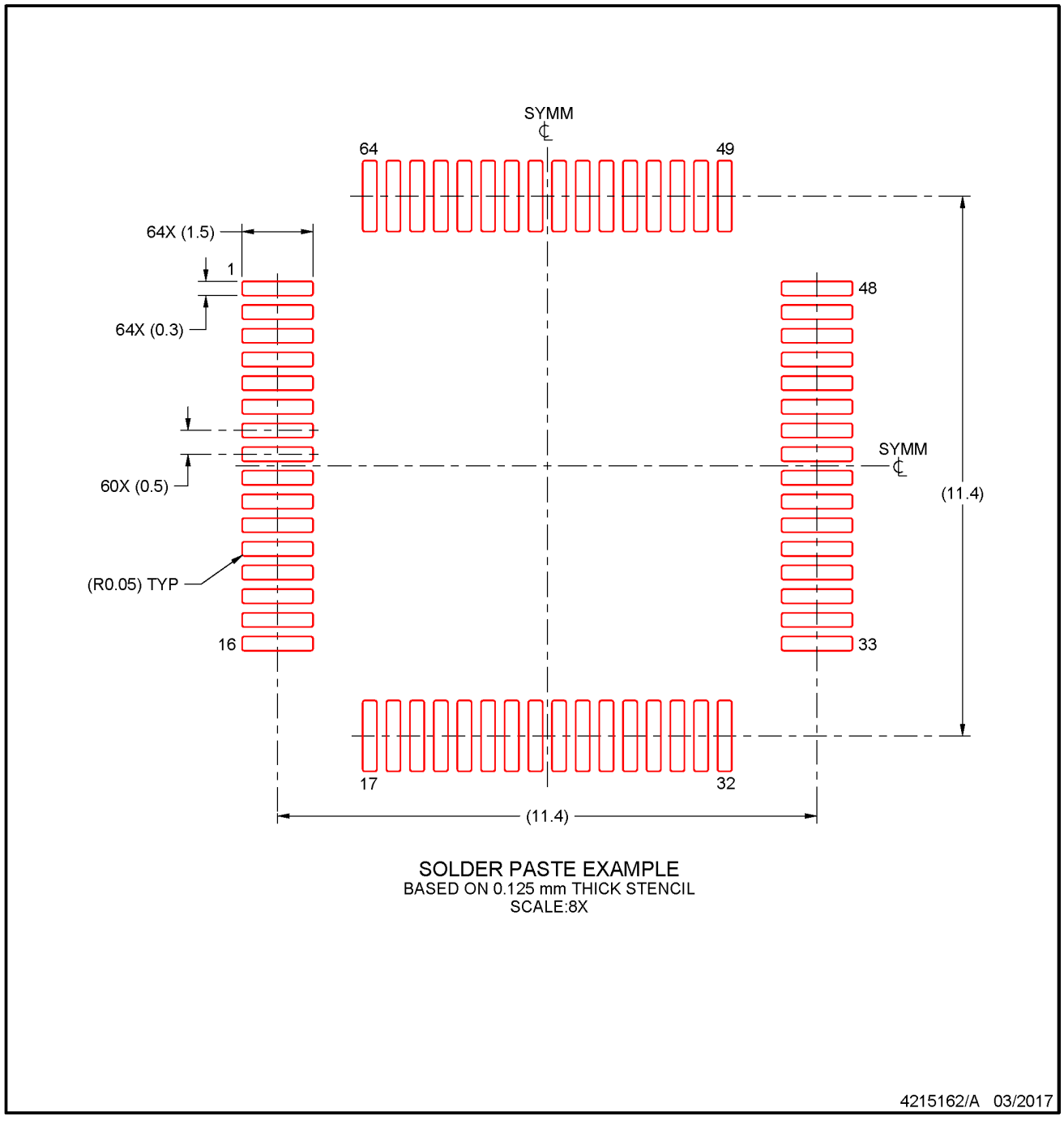
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).

EXAMPLE STENCIL DESIGN

PM0064A

LQFP - 1.6 mm max height

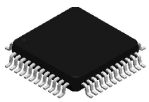
PLASTIC QUAD FLATPACK



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

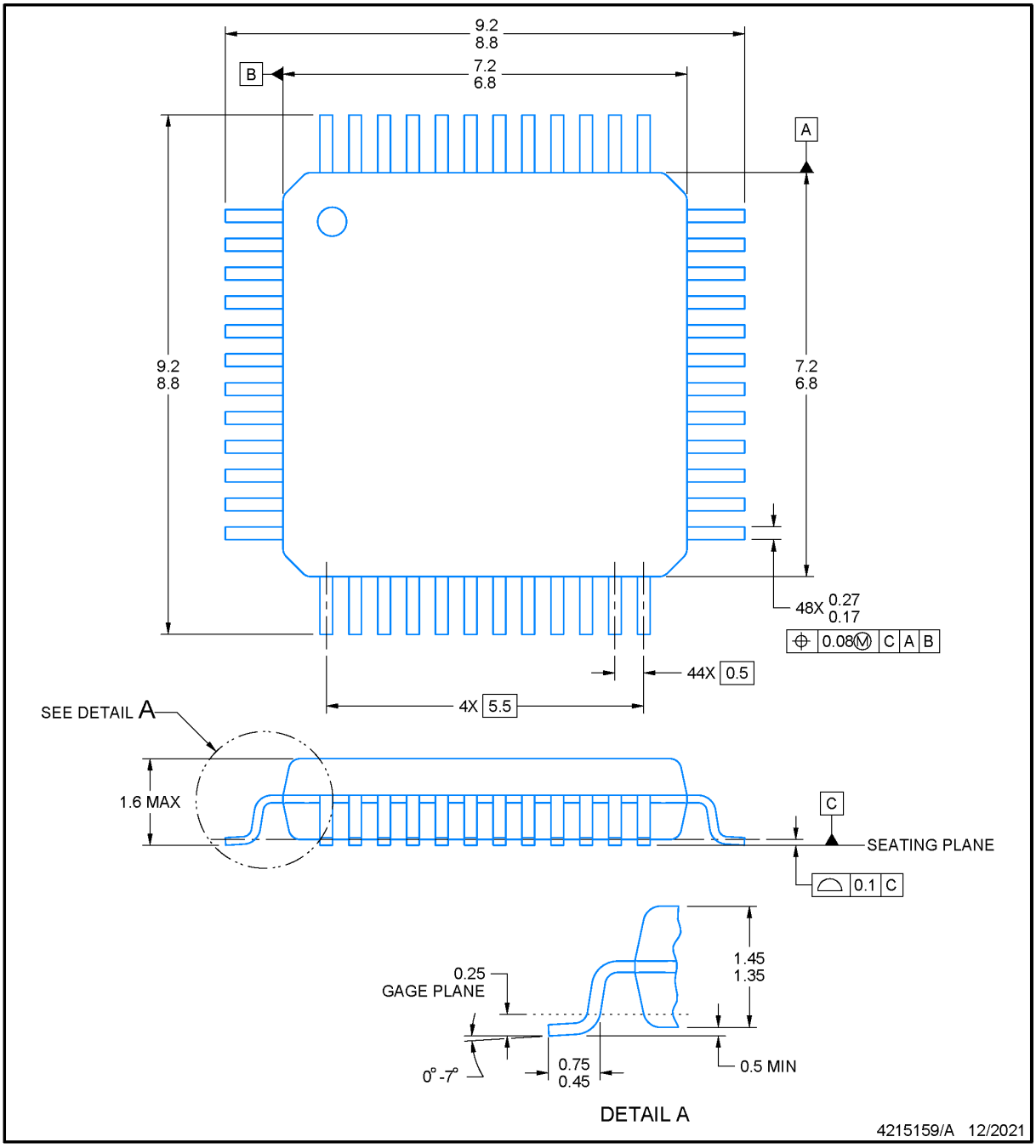
PACKAGE OUTLINE



PT0048A

LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK



NOTES:

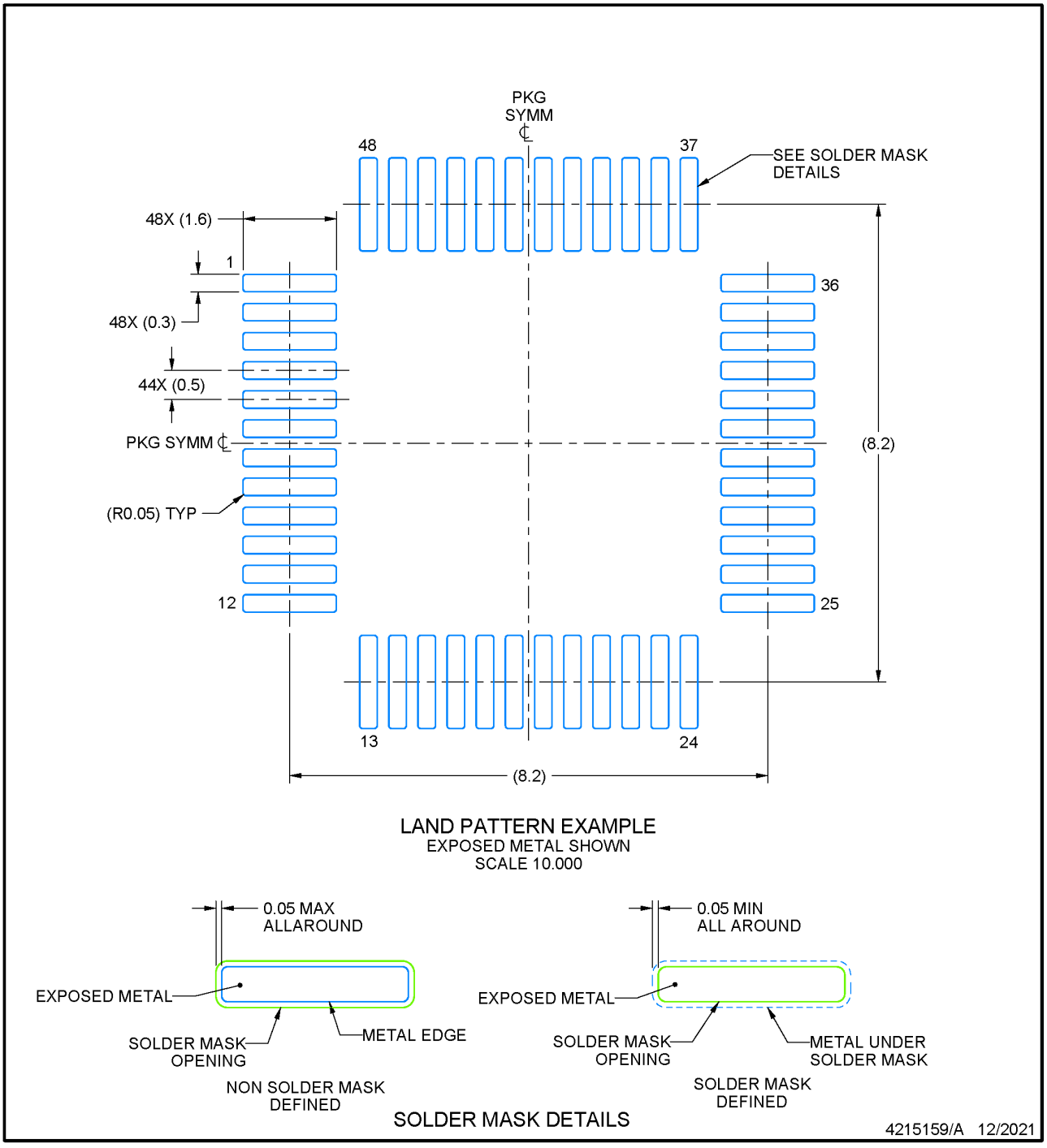
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.
4. This may also be a thermally enhanced plastic package with leads conected to the die pads.

EXAMPLE BOARD LAYOUT

PT0048A

LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK



NOTES: (continued)

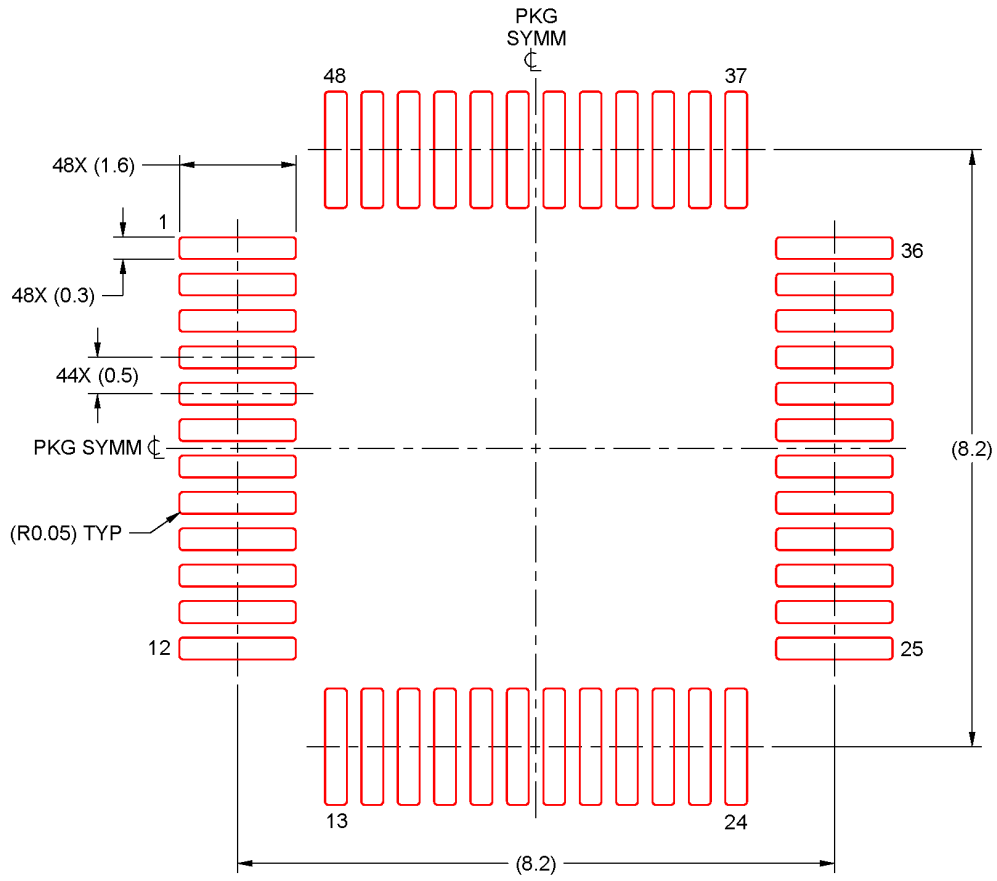
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PT0048A

LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 10X

4215159/A 12/2021

NOTES: (continued)

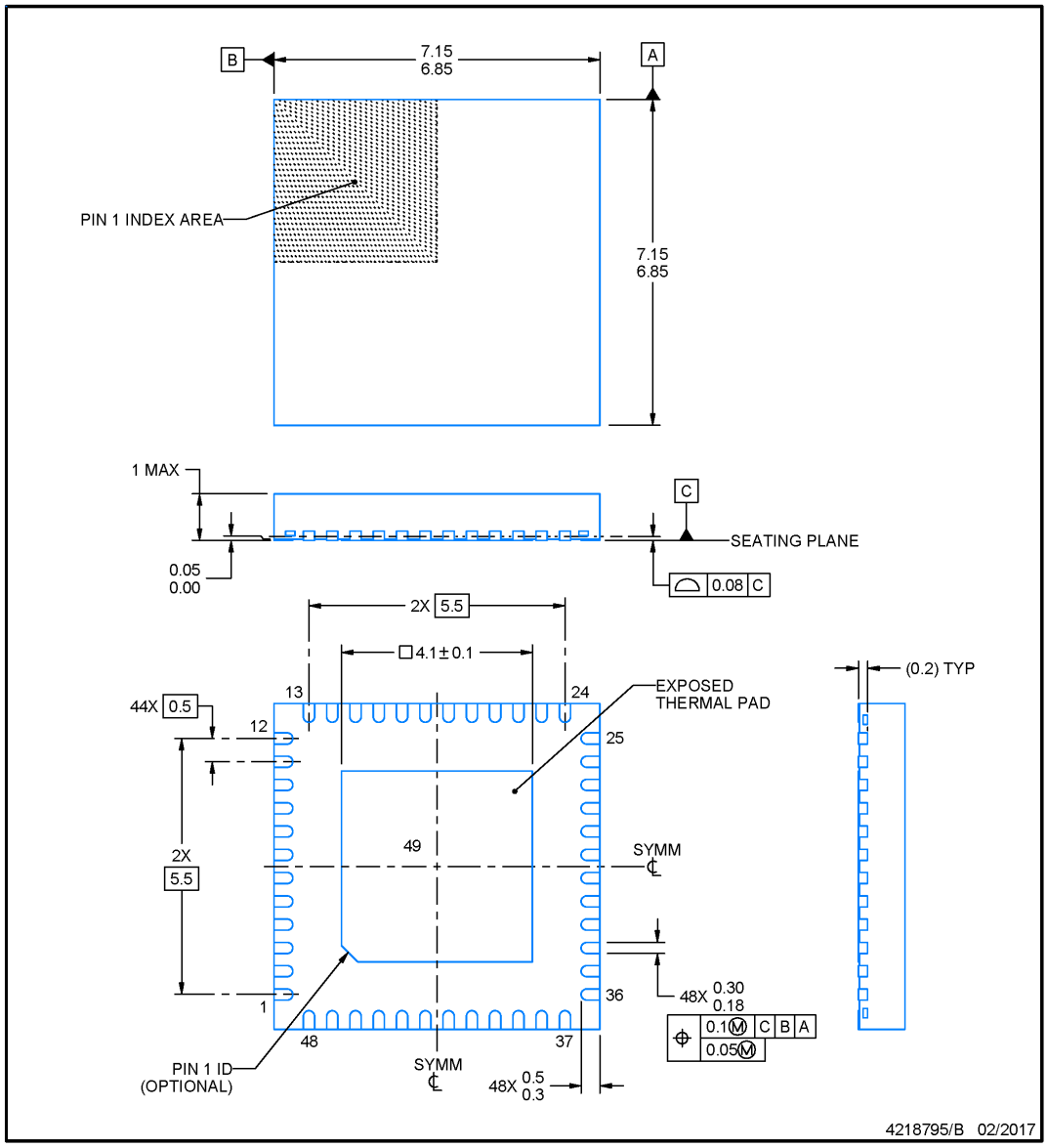
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

RGZ0048B

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



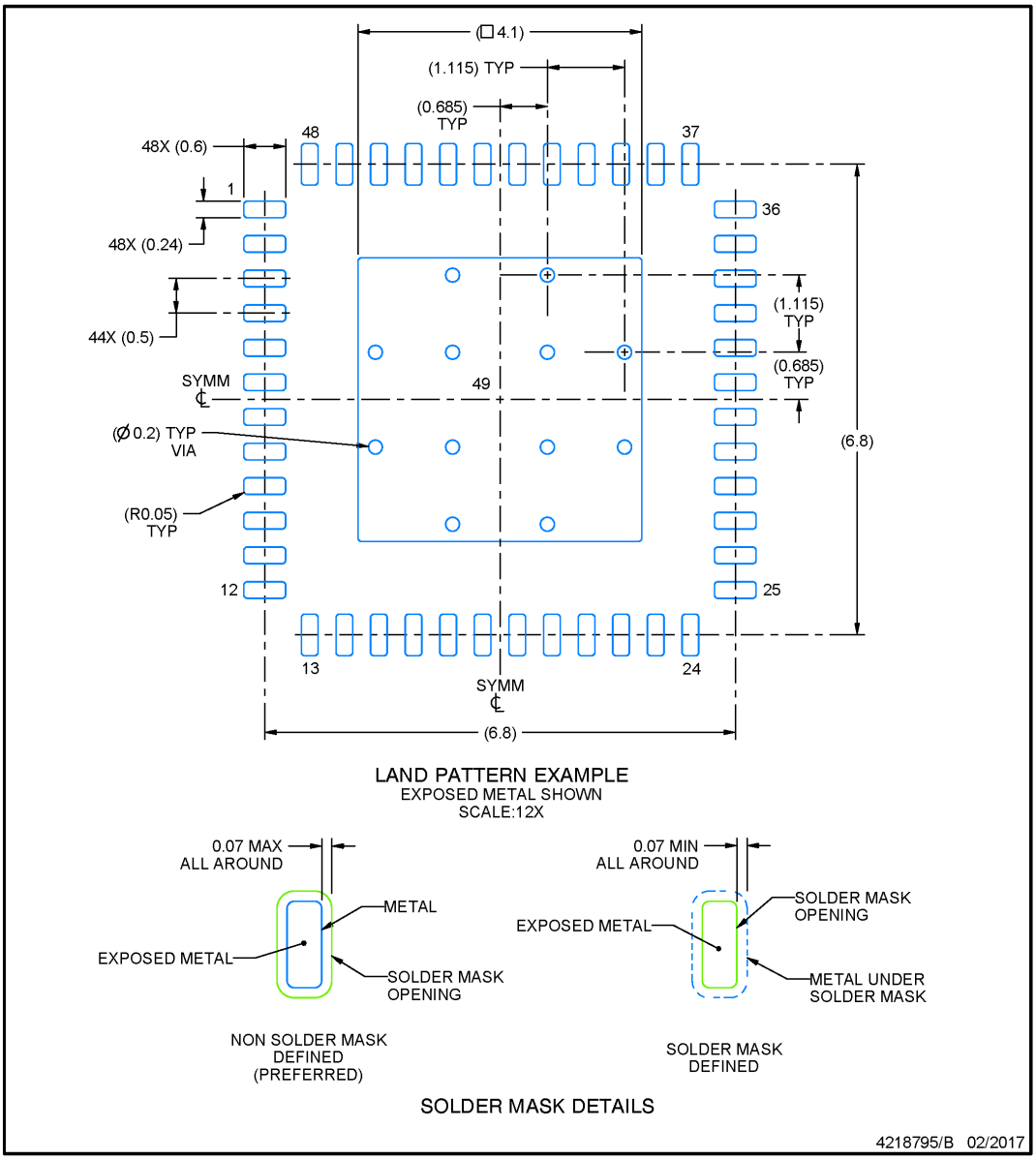
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RGZ0048B — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



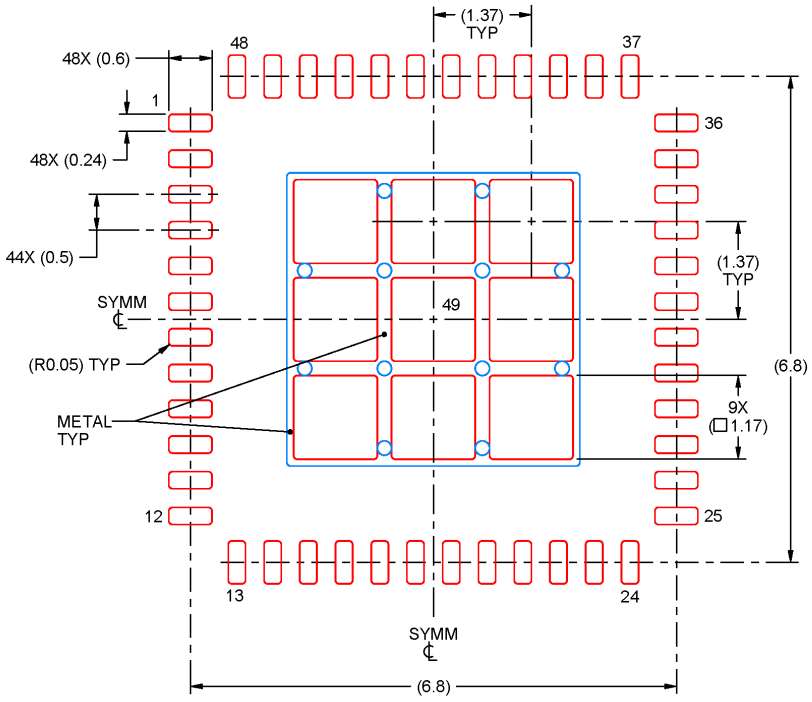
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGZ0048B — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
73% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

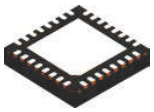
4218795/B 02/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

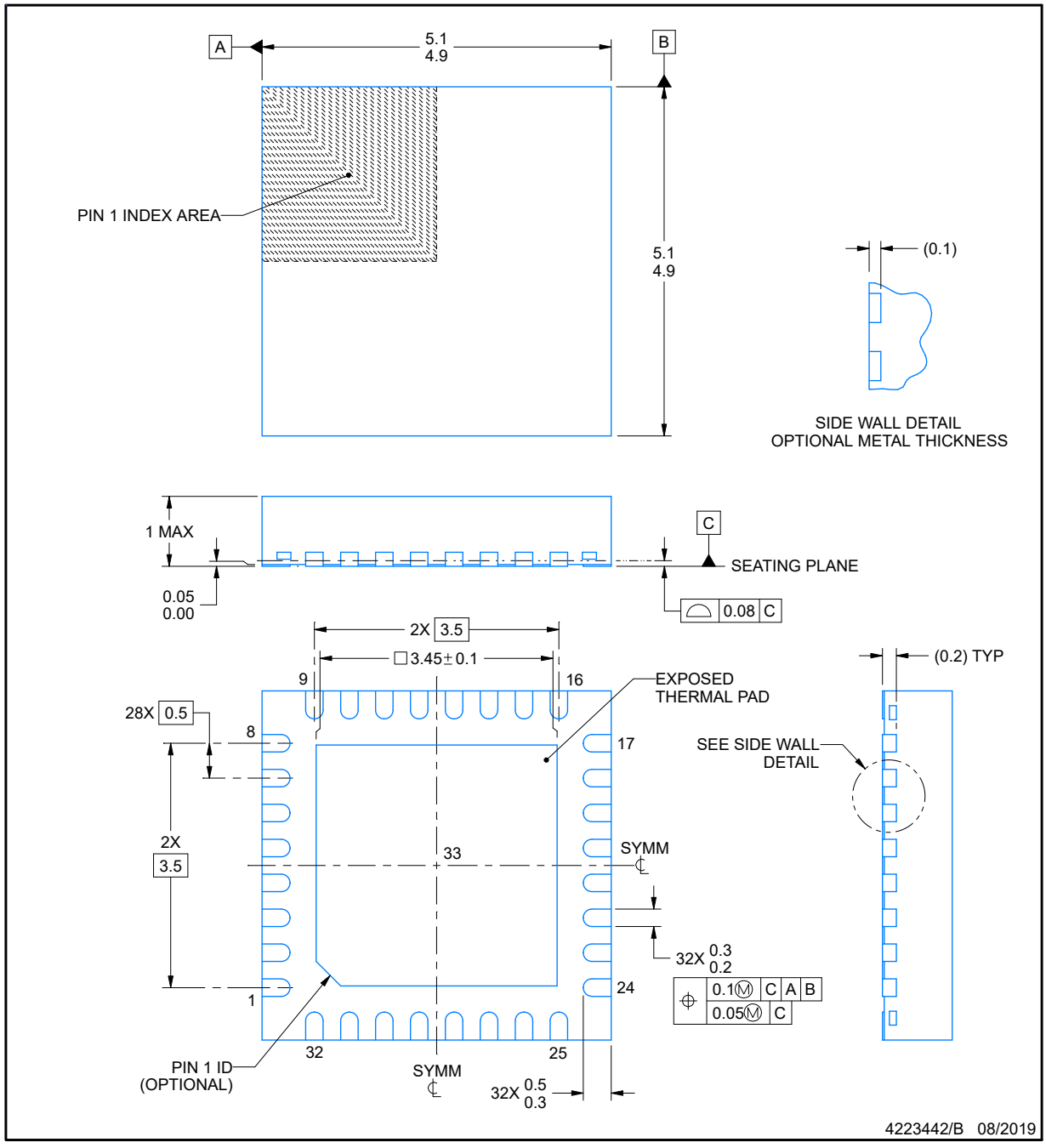
PACKAGE OUTLINE

RHB0032E



VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

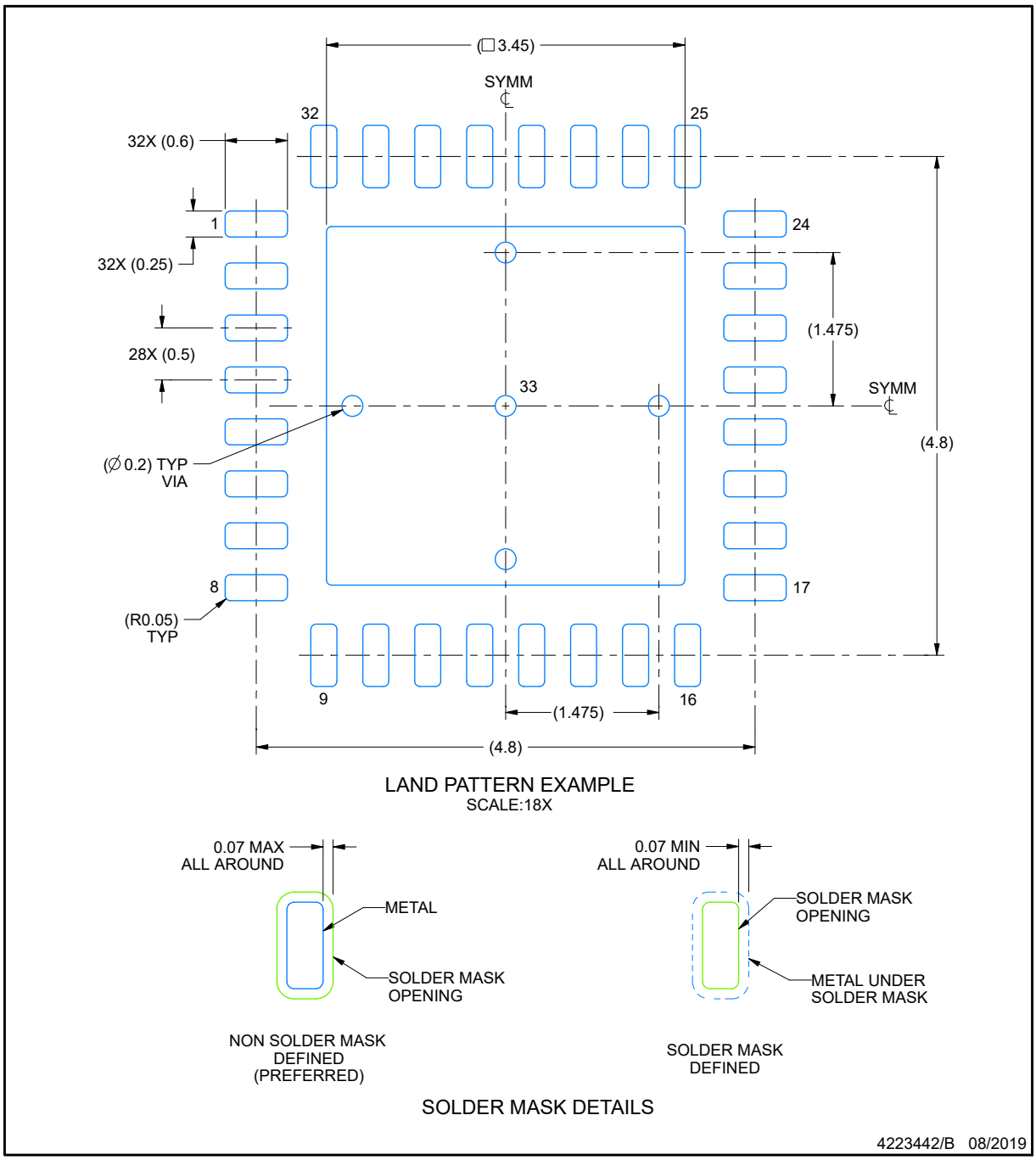
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

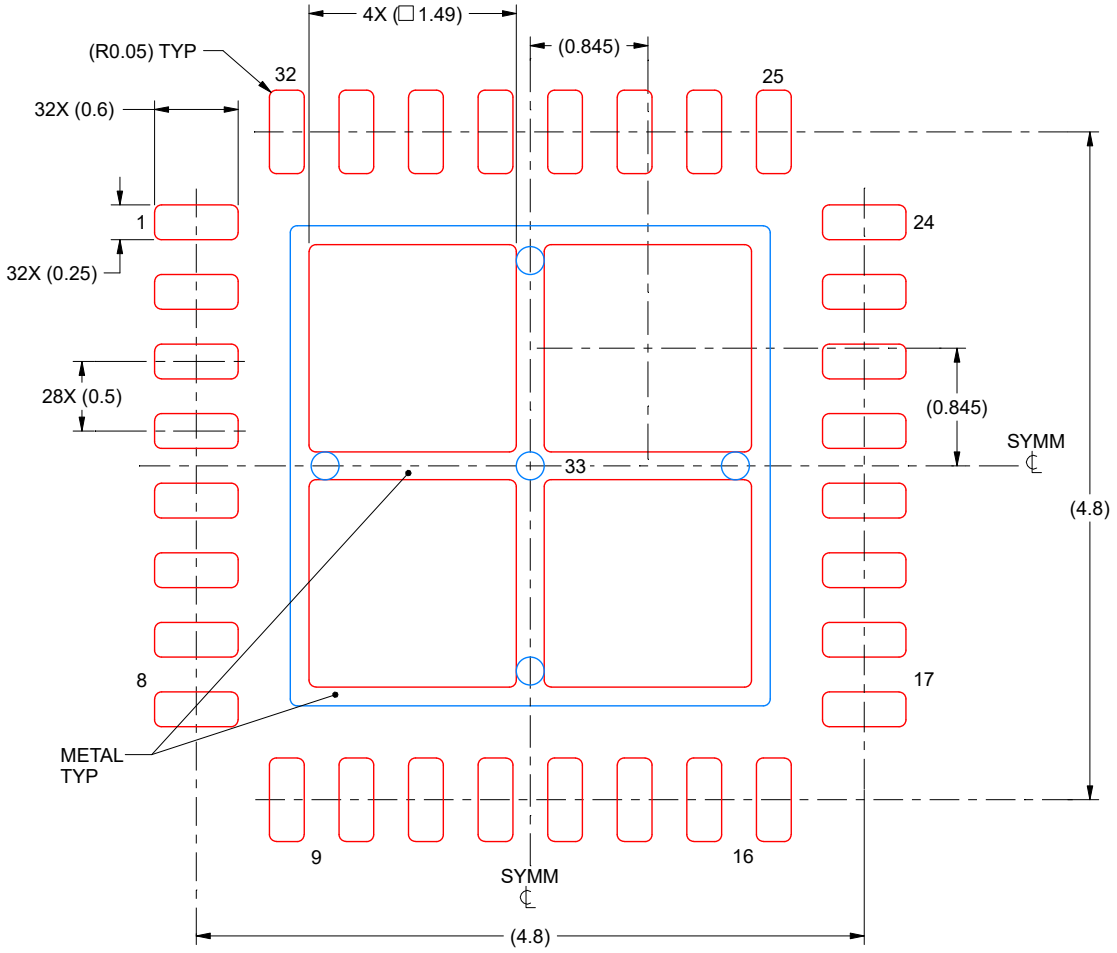
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

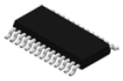
4223442/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

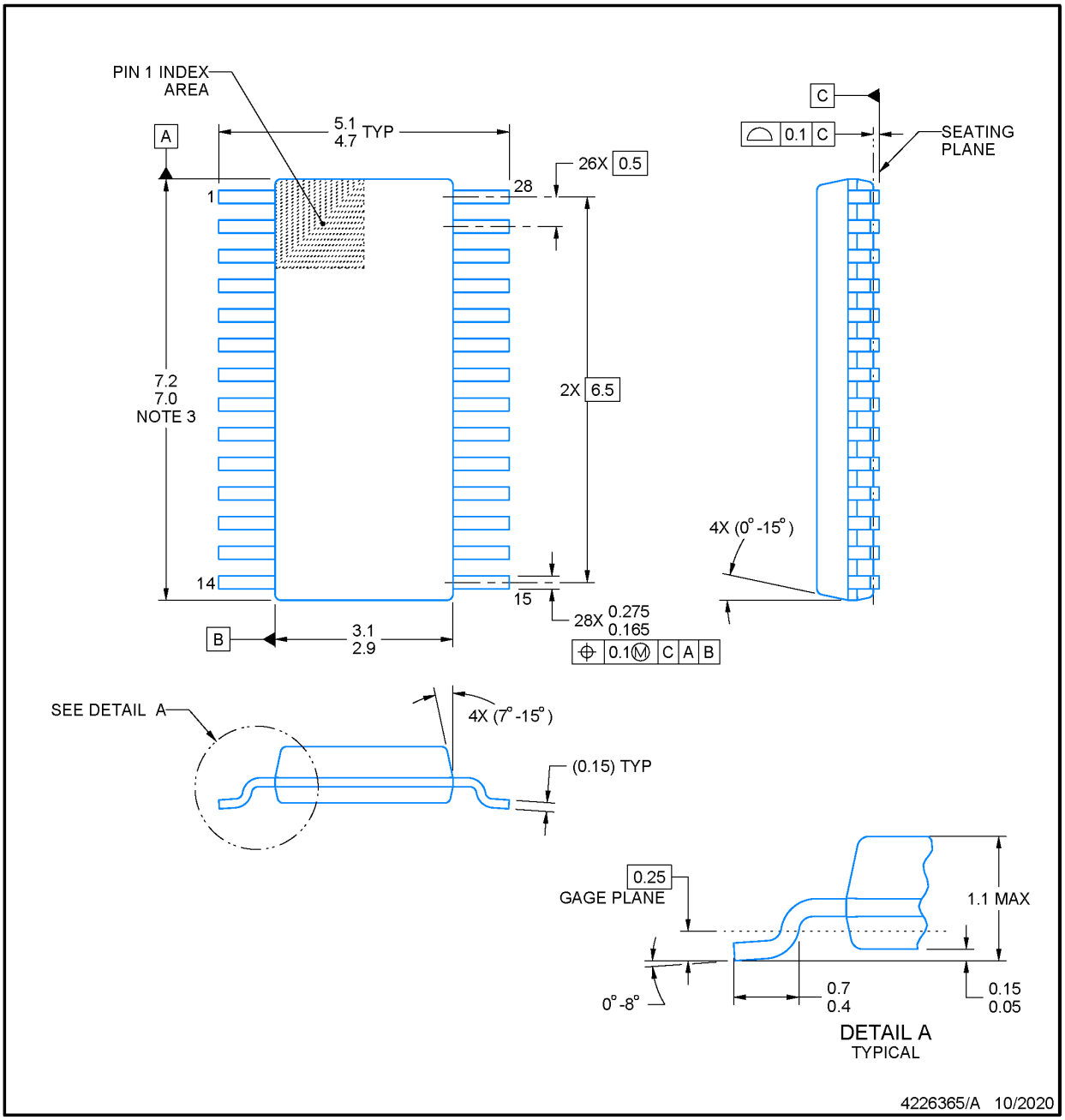
PACKAGE OUTLINE

DGS0028A



VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



PowerPAD is a trademark of Texas Instruments.

NOTES:

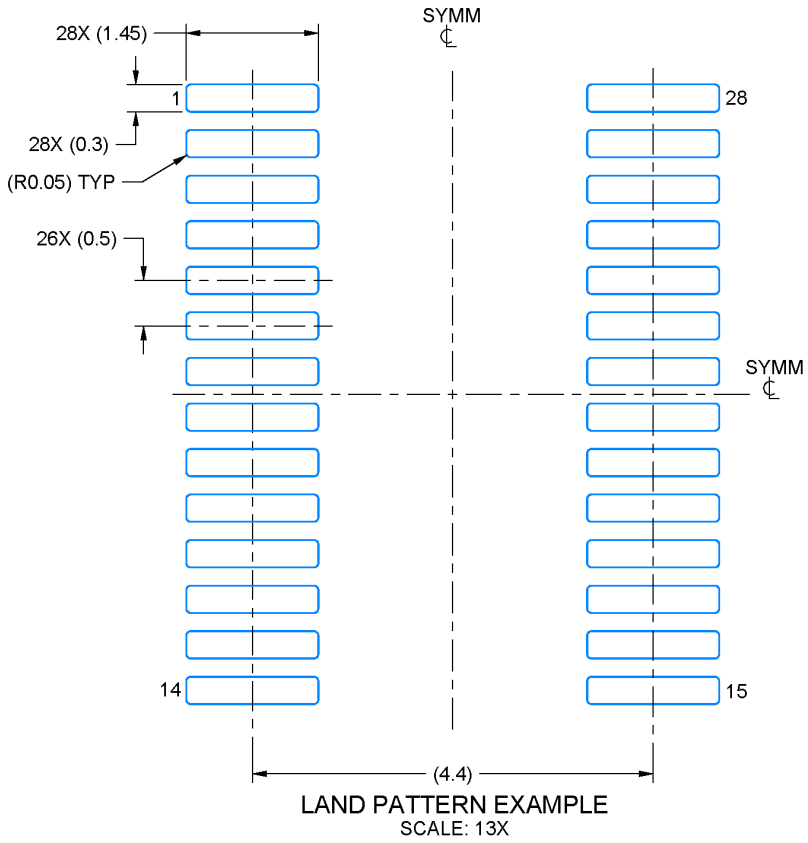
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

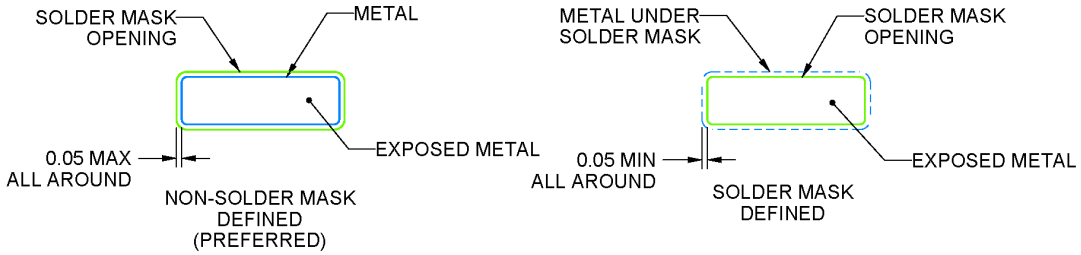
DGS0028A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE: 13X



SOLDER MASK DETAILS

4226365/A 10/2020

NOTES: (continued)

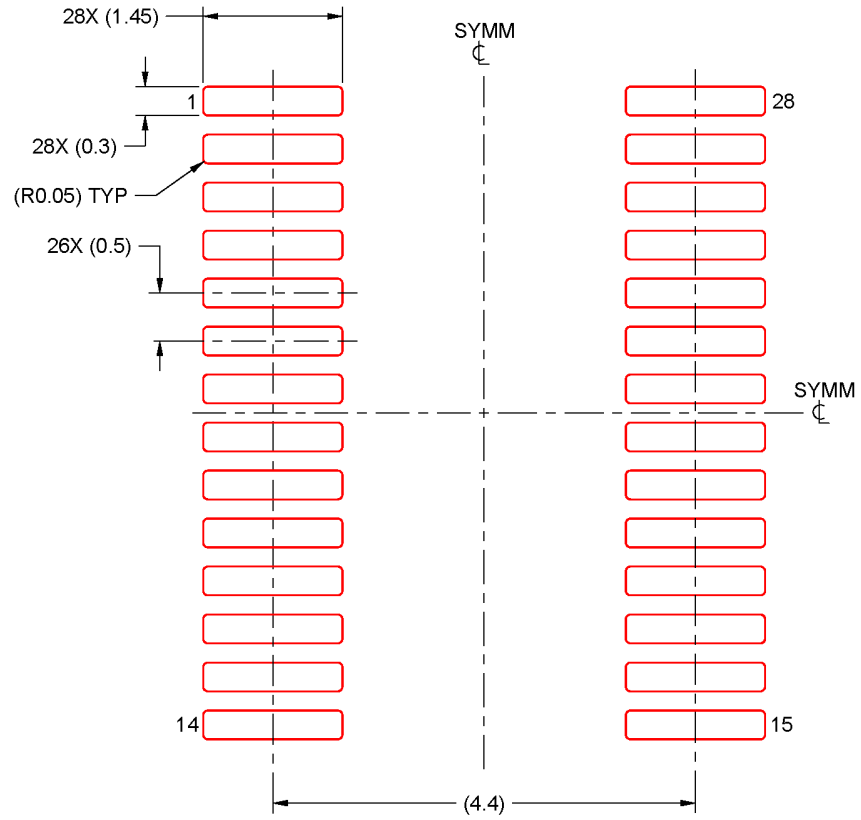
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DGS0028A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 13X

4226365/A 10/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
M0G3505QDGS28RQ1	Active	Production	VSSOP (DGS) | 28	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	G3505Q
M0G3505QDGS28RQ1.A	Active	Production	VSSOP (DGS) | 28	5000 | LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	G3505Q
M0G3505QDGS28RQ1.B	Active	Production	VSSOP (DGS) | 28	5000 | LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	G3505Q
M0G3505QDGS32RQ1	Active	Production	VSSOP (DGS) | 32	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	G3505Q
M0G3505QDGS32RQ1.A	Active	Production	VSSOP (DGS) | 32	5000 | LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	G3505Q
M0G3505QDGS32RQ1.B	Active	Production	VSSOP (DGS) | 32	5000 | LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	G3505Q
M0G3505QPMRQ1	Active	Production	LQFP (PM) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0G3505Q
M0G3505QPMRQ1.A	Active	Production	LQFP (PM) | 64	1000 | LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0G3505Q
M0G3505QPMRQ1.B	Active	Production	LQFP (PM) | 64	1000 | LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0G3505Q
M0G3505QPTRQ1	Active	Production	LQFP (PT) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0G3505Q
M0G3505QPTRQ1.A	Active	Production	LQFP (PT) | 48	1000 | LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0G3505Q
M0G3505QPTRQ1.B	Active	Production	LQFP (PT) | 48	1000 | LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0G3505Q
M0G3505QRGZRQ1	Active	Production	VQFN (RGZ) | 48	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 G3505Q
M0G3505QRGZRQ1.A	Active	Production	VQFN (RGZ) | 48	3000 | LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 G3505Q
M0G3505QRGZRQ1.B	Active	Production	VQFN (RGZ) | 48	3000 | LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 G3505Q
M0G3505QRHBRQ1	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 G3505Q
M0G3505QRHBRQ1.A	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 G3505Q
M0G3505QRHBRQ1.B	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 G3505Q
M0G3506QDGS28RQ1	Active	Production	VSSOP (DGS) | 28	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	G3506Q
M0G3506QDGS28RQ1.A	Active	Production	VSSOP (DGS) | 28	5000 | LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	G3506Q
M0G3506QDGS28RQ1.B	Active	Production	VSSOP (DGS) | 28	5000 | LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	G3506Q
M0G3506QDGS32RQ1	Active	Production	VSSOP (DGS) | 32	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	G3506Q
M0G3506QDGS32RQ1.A	Active	Production	VSSOP (DGS) | 32	5000 | LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	G3506Q
M0G3506QDGS32RQ1.B	Active	Production	VSSOP (DGS) | 32	5000 | LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	G3506Q
M0G3506QPMRQ1	Active	Production	LQFP (PM) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0G3506Q

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
M0G3506QPMRQ1.A	Active	Production	LQFP (PM) | 64	1000 | LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0G3506Q
M0G3506QPMRQ1.B	Active	Production	LQFP (PM) | 64	1000 | LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0G3506Q
M0G3506QPTRQ1	Active	Production	LQFP (PT) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0G3506Q
M0G3506QPTRQ1.A	Active	Production	LQFP (PT) | 48	1000 | LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0G3506Q
M0G3506QPTRQ1.B	Active	Production	LQFP (PT) | 48	1000 | LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0G3506Q
M0G3506QRGZRQ1	Active	Production	VQFN (RGZ) | 48	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 G3506Q
M0G3506QRGZRQ1.A	Active	Production	VQFN (RGZ) | 48	3000 | LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 G3506Q
M0G3506QRGZRQ1.B	Active	Production	VQFN (RGZ) | 48	3000 | LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 G3506Q
M0G3506QRHBRQ1	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 G3506Q
M0G3506QRHBRQ1.A	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 G3506Q
M0G3506QRHBRQ1.B	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 G3506Q
M0G3507QDGS28RQ1	Active	Production	VSSOP (DGS) | 28	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	G3507Q
M0G3507QDGS28RQ1.A	Active	Production	VSSOP (DGS) | 28	5000 | LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	G3507Q
M0G3507QDGS28RQ1.B	Active	Production	VSSOP (DGS) | 28	5000 | LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	G3507Q
M0G3507QDGS32RQ1	Active	Production	VSSOP (DGS) | 32	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	G3507Q
M0G3507QDGS32RQ1.A	Active	Production	VSSOP (DGS) | 32	5000 | LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	G3507Q
M0G3507QDGS32RQ1.B	Active	Production	VSSOP (DGS) | 32	5000 | LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	G3507Q
M0G3507QPMRQ1	Active	Production	LQFP (PM) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0G3507Q
M0G3507QPMRQ1.A	Active	Production	LQFP (PM) | 64	1000 | LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0G3507Q
M0G3507QPMRQ1.B	Active	Production	LQFP (PM) | 64	1000 | LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0G3507Q
M0G3507QPTRQ1	Active	Production	LQFP (PT) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0G3507Q
M0G3507QPTRQ1.A	Active	Production	LQFP (PT) | 48	1000 | LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0G3507Q
M0G3507QPTRQ1.B	Active	Production	LQFP (PT) | 48	1000 | LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0G3507Q
M0G3507QRGZRQ1	Active	Production	VQFN (RGZ) | 48	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 G3507Q
M0G3507QRGZRQ1.A	Active	Production	VQFN (RGZ) | 48	3000 | LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 G3507Q

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
M0G3507QRGZRQ1.B	Active	Production	VQFN (RGZ) | 48	3000 | LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 G3507Q
M0G3507QRHBRQ1	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 G3507Q
M0G3507QRHBRQ1.A	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 G3507Q
M0G3507QRHBRQ1.B	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 G3507Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF MSPM0G3505-Q1, MSPM0G3506-Q1, MSPM0G3507-Q1 :

- Catalog : MSPM0G3505, MSPM0G3506, MSPM0G3507

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

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