Mixed-Signal Microcontrollers With CAN-FD Interface

1 Features

- **Core**
  - Arm® 32-bit Cortex® M0+ CPU with memory protection unit, frequency up to 80MHz
- PSA-L1 Certification planned
- **Operating characteristics**
  - Extended temperature: –40°C up to 125°C
  - Wide supply voltage range: 1.62V to 3.6V
- **Memories**
  - Up to 256KB of flash memory with error correction code (ECC)
    - Dual-bank with address swap for OTA updates
  - 8KB data flash bank with ECC protection
  - 32KB total SRAM with ECC protection or hardware parity
- **High-performance analog peripherals**
  - Up to two simultaneous sampling 12-bit 1.6Msps analog-to-digital converters (ADC) with up to 27 external channels
    - 14-bit effective resolution at 100ksps with hardware averaging
  - Up to two high-speed comparators (COMP) with integrated 8-bit reference DACs
    - 32ns propagation delay in high-speed mode
    - Support low-power mode operation down to <1µA
  - Programmable analog connections between ADC and COMP
  - Two voltage references (VREF)
    - Configurable 1.4V or 2.5V internal shared voltage reference with external VREF capacitor
    - Configurable 1.4V or 2.5V internal only voltage reference without external VREF capacitor
  - Integrated temperature sensor
- **Optimized low-power modes (estimates for early samples)**
  - RUN: 104µA/MHz (CoreMark)
  - SLEEP: 614uA at 4MHz
  - STOP: 56µA at 32kHz
  - STANDBY: 1.4µA at 32kHz with RTC and SRAM state retention
  - SHUTDOWN: 69nA with IO wake-up capability
- **Intelligent digital peripherals**
  - 9-channel DMA controller
  - Math accelerator supports DIV, SQRT, MAC and TRIG computations
  - Five timers support up to 18 PWM channels
    - One 16-bit general-purpose timers support QEI
    - Two 16-bit general-purpose timers support low-power operation in STANDBY mode
    - Two 16-bit advanced timers with deadband support and complimentary outputs up to 12 PWM channels
  - Two basic software timers including 4 independent configurable 16-bit counters each
    - Ability to daisy-chain 2 of the 16-bit counters to form a 32-bit counter
    - Ability to generate 2x interrupt driven PWMs per basic software timer
  - Two windowed watchdog timers (WWDT), one independent watchdog timer (IWDT)
  - RTC with alarm and calendar mode
- **Enhanced communication interfaces**
  - Five configurable serial interfaces (UNICOMM)
    - One configurable serial interface supporting UART or SPI
    - One configurable serial interfaces supporting UART (with LIN) or I2C (controller or target mode)
    - One configurable serial interfaces supporting UART or I2C (controller or target mode)
    - One dedicated UART + LIN interface
    - One dedicated SPI interface up to 32Mbits/s
    - One Controller Area Network (CAN) interface supporting CAN 2.0 A or B and CAN-FD
- **Clock system**
  - Internal 4 to 32MHz oscillator (SYSOSC) with up to ±1.2% accuracy
  - Phase-locked loop (PLL) up to 80MHz
  - Internal 32kHz low-frequency oscillator (LFOSC) with ±3% accuracy
  - External 4 to 48MHz crystal oscillator (HFXT)
  - External 32kHz crystal oscillator (LFXT)
  - External clock input
- **Data integrity and encryption**
  - AES-128/256 accelerator with support for GCM/GMAC, CCM/CBC-MAC, CBC, CTR
  - Secure key storage for up to four AES keys
  - Flexible firewalls for protecting code and data
  - Cyclic redundancy checker (CRC-16, CRC-32)
- **Flexible I/O features**
  - Up to 60 GPIOs
    - Two 5V-tolerant open-drain IOs
    - Three high-drive IOs with 20mA drive strength

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- Four high-speed IOs
- **Development support**
  - 2-pin serial wire debug (SWD)
- **Package options**
  - 64-pin LQFP (PM) (0.5mm pitch)
  - 48-pin LQFP (PT) (0.5mm pitch)
  - 48-pin VQFN (RGZ) (0.5mm pitch)
  - 32-pin VQFN (RHB) (0.5mm pitch)
  - 28-pin WQFN (RUY) (0.4mm pitch)
  - 28-pin VSSOP (28DGS) (0.5mm pitch)
  - 24-pin VQFN (RGE) (0.4mm pitch)
- **Family members** (also see *Device Comparison*)
  - MSPM0G1218: 256KB flash, 32KB RAM, 8KB Databank, 2x ADC, 2x COMP
  - MSPM0G1207: 128KB flash, 32KB RAM, 8KB Databank, 1xADC, 1x COMP
  - MSPM0G3218: 256KB flash, 32KB RAM, 8KB Databank, 2x ADC, 2x COMP, 1x CAN-FD
  - MSPM0G3207: 128KB flash, 32KB RAM, 8KB Databank, 1x ADC, 1x COMP, 1x CAN-FD
- **Development kits and software** (also see *Tools and Software*)
  - LP-MSPM0G3218 Launchpad Development Kit
  - MSPM0 Software Development Kit (SDK)

2 Applications

- Motor control
- Home appliances
- Uninterruptible power supplies and inverters
- Electronic point of sale systems
- Medical and healthcare
- Test and measurement
- Factory automation and control
- Industrial transport
- Grid infrastructure
- Smart metering
- Communication modules
- Lighting

3 Description

MSPM0Gx218 and MSPM0Gx207 microcontrollers (MCUs) are part of the MSP highly integrated, ultra-low-power 32-bit MCU family based on the enhanced Arm® Cortex®-M0+ 32-bit core platform, operating at up to 80MHz frequency. These MCUs offer a blend of cost optimization and design flexibility for applications requiring 128KB to 256KB of flash memory in packages ranging from 24 to 64 pins. These devices include CAN-FD controllers, cybersecurity enablers, high performance integrated analog, and provide excellent low power performance across the operating temperature range.

The device has up to 256KB of embedded flash program memory with built-in error correction code (ECC) and up to 32KB SRAM (with ECC and parity protection). The flash memory is organized into two main banks to support field firmware updates, with address swap support provided between the two main banks.

Flexible cybersecurity enablers can be used to support secure boot, secure in-field firmware updates, IP protection (execute-only memory), key storage, and more. Hardware acceleration is provided for a variety of AES symmetric cipher modes. The cybersecurity architecture is pending Arm® PSA Level 1 certification.

A set of high performance analog modules is provided, such as two simultaneously sampling 12-bit, 1.6Msps ADCs supporting up to 27 external channels, on-chip voltage reference (1.4V or 2.5V), and two comparators operable in low-power and high-speed modes with additional built-in 8-bit reference DACs.

The TI MSPM0 family of low-power MCUs consists of devices with varying degrees of analog and digital integration. The MSPM0 MCU platform combines the Arm Cortex-M0+ platform with a holistic ultra-low-power system architecture, allowing system designers to increase performance while reducing energy consumption.

MSPM0Gx218 and MSPM0Gx207 MCUs are supported by an extensive hardware and software ecosystem with reference designs and code examples to get the design started quickly. Development kits include a LaunchPad available for purchase. TI also provides a free MSPM0 Software Development Kit (SDK), which is available as a component of Code Composer Studio™ IDE desktop and cloud version within the TI Resource Explorer. MSPM0 MCUs are also supported by extensive online collateral, training with MSP Academy, and online support through the TI E2E™ support forums.

For complete module descriptions, see the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

CAUTION

System-level ESD protection must be applied in compliance with the device-level ESD specification to prevent electrical overstress or disturbing of data or code memory. See *MSP430™ System-Level ESD Considerations* for more information. The principles in this application note are applicable to MSPM0 MCUs.

Device Information

PART NUMBER	PACKAGE (1)	PACKAGE SIZE (2)
MSPM0G3218SPMR	PM (LQFP, 64)	12mm x 12mm
MSPM0G3207SPMR		
MSPM0G1218SPMR		
MSPM0G1207SPMR		
MSPM0G3218SPTR	PT (LQFP, 48)	9mm x 9mm
MSPM0G3207SPTR		
MSPM0G1218SPTR		
MSPM0G1207SPTR		
MSPM0G3218SRGZR	RGZ (VQFN, 48)	7mm x 7mm
MSPM0G3207SRGZR		
MSPM0G1218SRGZR		
MSPM0G1207SRGZR		
MSPM0G3218SRHBR	RHB (VQFN, 32)	5mm x 5mm
MSPM0G3207SRHBR		
MSPM0G1218SRHBR		
MSPM0G1207SRHBR		
MSPM0G1218SRUYR	RUY (WQFN, 28)	4mm x 4mm
MSPM0G1207SRUYR		
MSPM0G1218S28DGSR	DGS28 (VSSOP, 28)	7.1mm x 4.9mm
MSPM0G1207S28DGSR		
MSPM0G3218SRGER	VQFN (RGE, 24)	4mm x 4mm
MSPM0G3207SRGER		
MSPM0G1218SRGER		

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4 Functional Block Diagram

Figure 4-1 shows the devices' detailed functional block diagram.

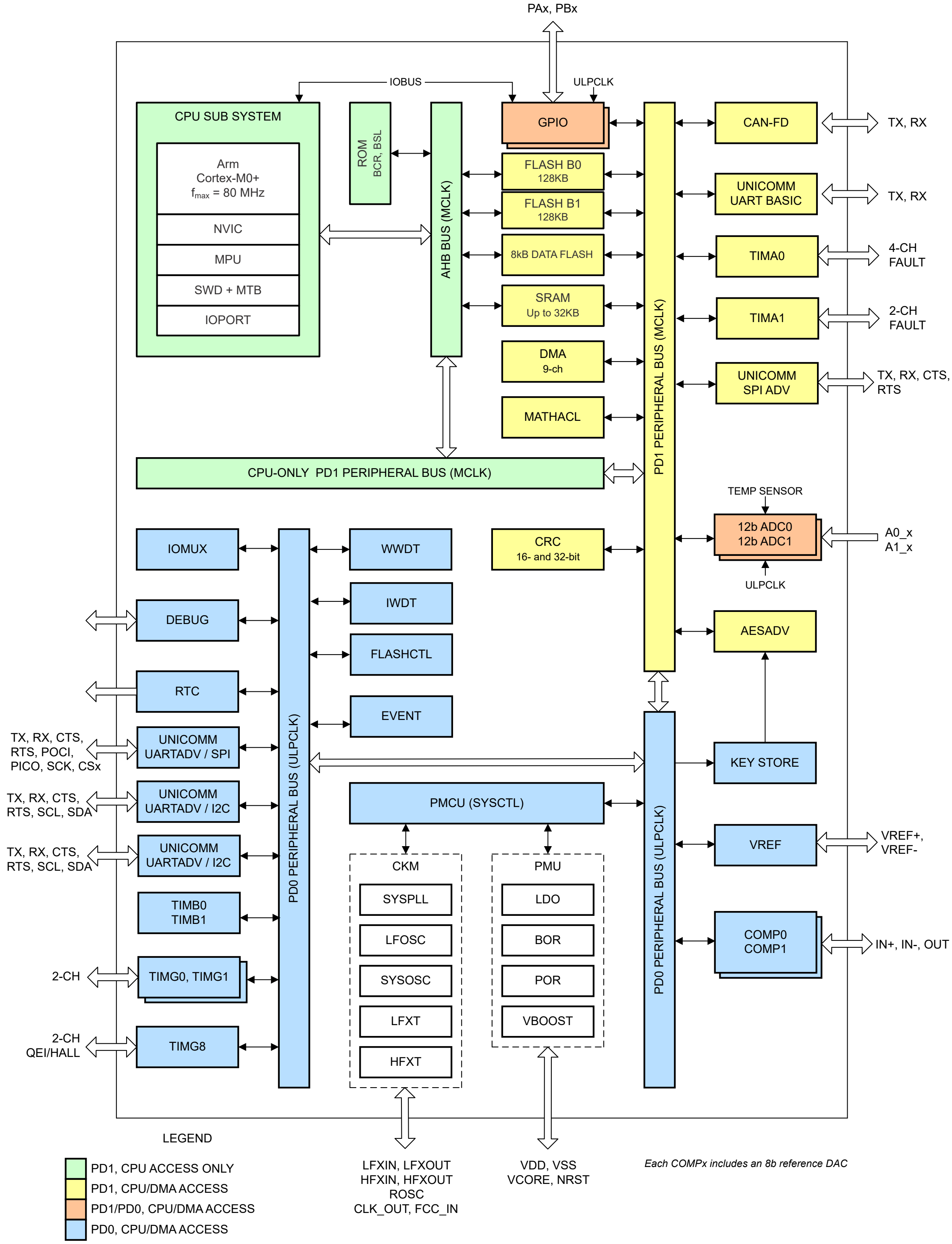

Figure 4-1. MSPM0G3218 Functional Block Diagram

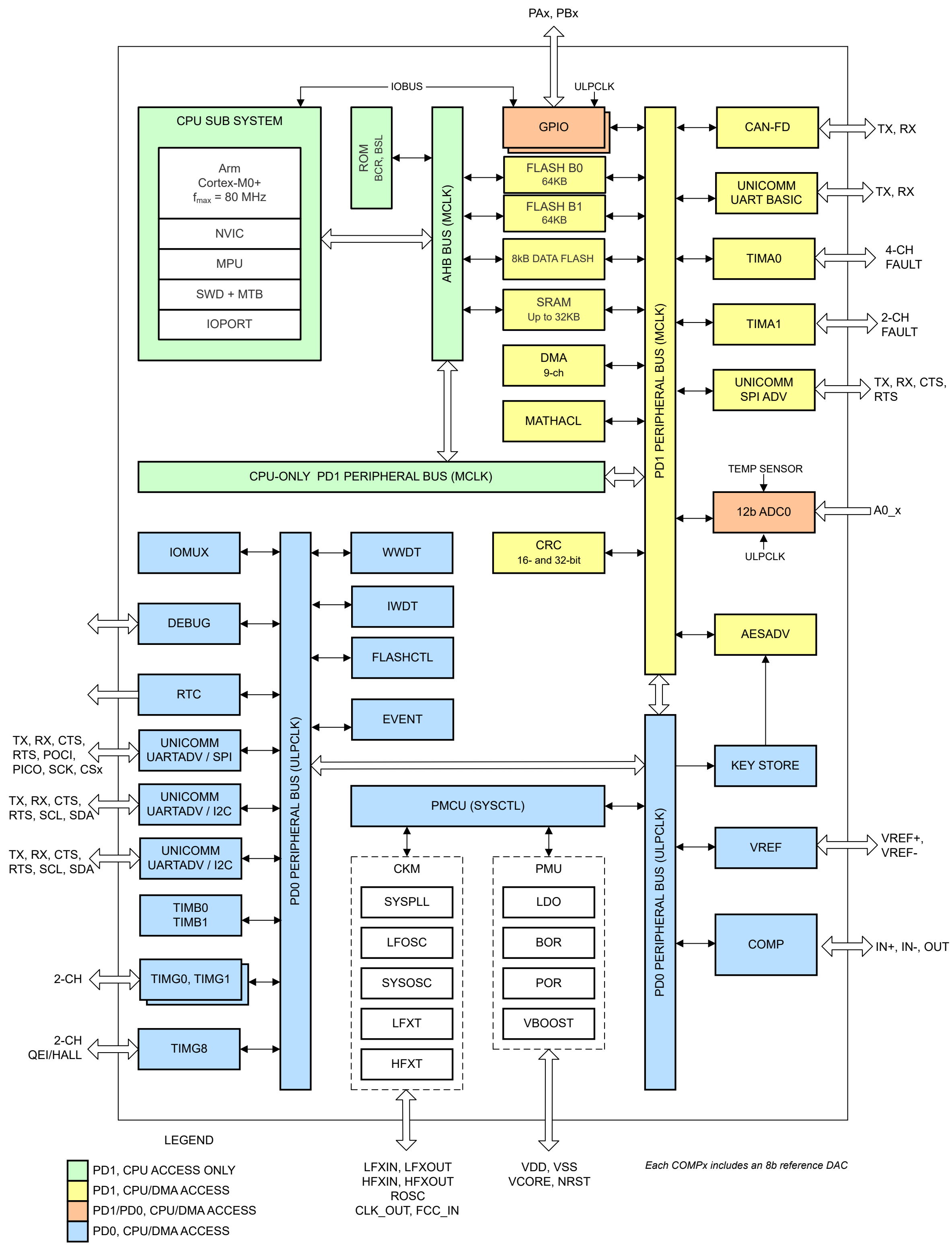

Figure 4-2. MSPM0G3207 Functional Block Diagram

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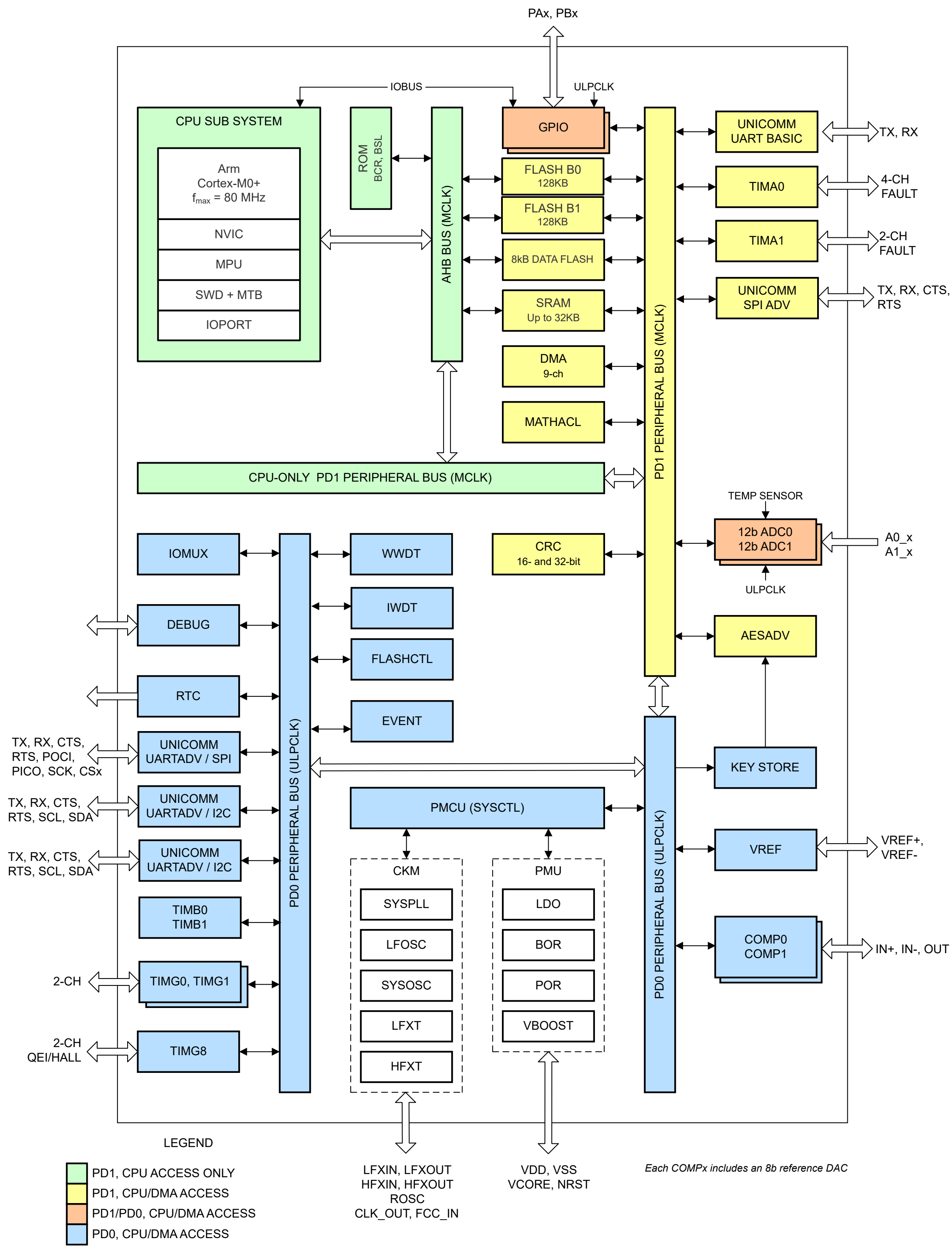

Figure 4-3. MSPM0G1218 Functional Block Diagram

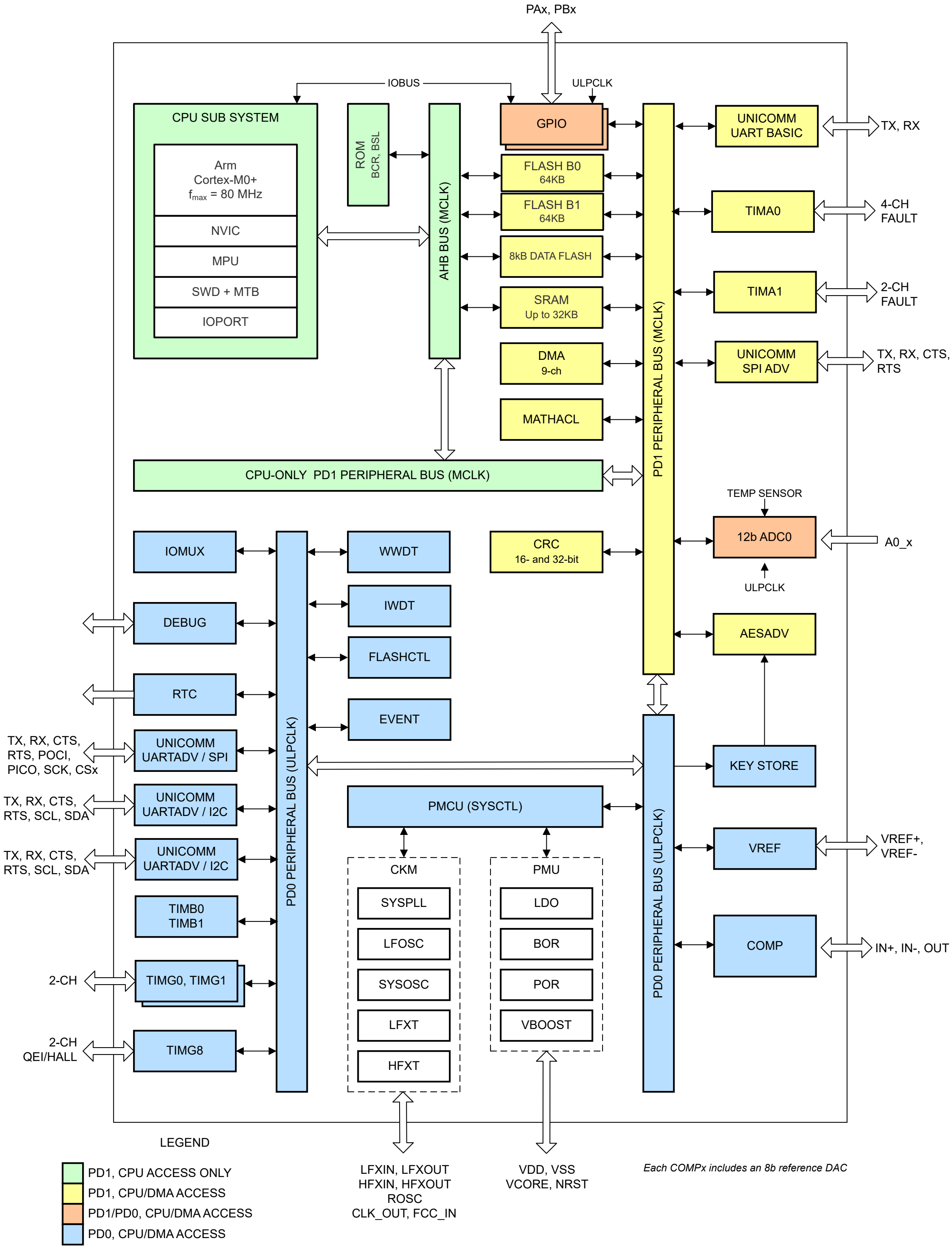

Figure 4-4. MSPM0G1207 Functional Block Diagram

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5 Device Comparison

The following table summarizes the features of each device that is described in this data sheet.

Table 5-1. Device Comparison Table

DEVICE NAME[(1) (4)]	FLASH / SRAM (KB)	QUAL[(2)]	CAN	UART/I2C/SPI	ADC / CHAN	COMP	GPIO	PACKAGE[(3)]
MSPM0G3218SPMR	256 / 32	S	1	4 / 2 / 2	2 / 27	2	60	64 LQFP (0.5mm pitch) [12mm x 12mm]
MSPM0G3207SPMR	128 / 32	S	1	4 / 2 / 2	1 / 13	1	60	
MSPM0G1218SPMR	256 / 32	S	0	4 / 2 / 2	2 / 27	2	60	
MSPM0G1207SPMR	128 / 32	S	0	4 / 2 / 2	1 / 13	1	60	
MSPM0G3218SPTR	256 / 128	S	1	4 / 2 / 2	2 / 21	2	44	48 LQFP (0.5mm pitch) [9mm x 9mm]
MSPM0G3207SPTR	128 / 32	S	1	4 / 2 / 2	1 / 12	1	44	
MSPM0G1218SPTR	256 / 32	S	0	4 / 2 / 2	2 / 21	2	44	
MSPM0G1207SPTR	128 / 32	S	0	4 / 2 / 2	1 / 12	1	44	
MSPM0G3218SRGZR	256 / 32	S	1	4 / 2 / 2	2 / 21	2	44	48 VQFN (0.5mm pitch) [7mm x 7mm]
MSPM0G3207SRGZR	128 / 32	S	1	4 / 2 / 2	1 / 12	1	44	
MSPM0G1218SRGZR	256 / 32	S	0	4 / 2 / 2	2 / 21	2	44	
MSPM0G1207SRGZR	128 / 32	S	0	4 / 2 / 2	1 / 12	1	44	
MSPM0G3218SRHBR	256 / 32	S	1	4 / 2 / 2	2 / 16	2	28	32 VQFN (0.5mm pitch) [5mm x 5mm]
MSPM0G3207SRHBR	128 / 32	S	1	4 / 2 / 2	1 / 10	1	28	
MSPM0G1218SRHBR	256 / 32	S	0	4 / 2 / 2	2 / 16	2	28	
MSPM0G1207SRHBR	128 / 32	S	0	4 / 2 / 2	1 / 10	1	28	
MSPM0G1218SRUYR	256 / 32	S	0	4 / 2 / 2	2 / 14	2	24	28 WQFN (0.4mm pitch) [4mm x 4mm]
MSPM0G1207SRUYR	128 / 32	S	0	4 / 2 / 2	1 / 8	1	24	
MSPM0G1218S28DGSR	256 / 32	S	0	4 / 2 / 2	2 / 10	2	24	28 VSSOP (0.5mm pitch) [7.1mm x 3.0mm]
MSPM0G1207S28DGSR	128 / 32	S	0	4 / 2 / 2	1 / 7	1	24	
MSPM0G3218SRGER	256 / 32	S	1	4 / 2 / 2	2 / 11	2	20	24 VQFN (0.5mm pitch) [4mm x 4mm]
MSPM0G3207SRGER	128 / 32	S	1	4 / 2 / 2	1 / 6	1	20	
MSPM0G1218SRGER	256 / 32	S	0	4 / 2 / 2	2 / 11	2	20	

(1) For the most current part, package, and ordering information for all available devices, see the *Package Option Addendum* in Section 12, or see the TI website.

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(2) Device Qualifications:
- S = –40°C to 125°C

(3) The package size (length × width) is a nominal value and includes pins, where applicable. For the package dimensions with tolerances, see Section 12.

(4) For more information about the device name, see Section 10.2

6 Pin Configuration and Functions

The System Configuration tool provides a graphical interface to enable, configurable, and generate initialization code for pin multiplexing and simplifying pin settings. The pin diagrams shown in the data sheet show the primary peripheral functions, some of the integrated device features, and available clock signals to simplify the device pinout.

For full descriptions of the pin functions, see the *Pin Attributes* and *Signal Descriptions* sections.

6.1 Pin Diagrams

For full pin configuration and functions for each package option, refer to *Pin Attributes* and *Signal Descriptions*.

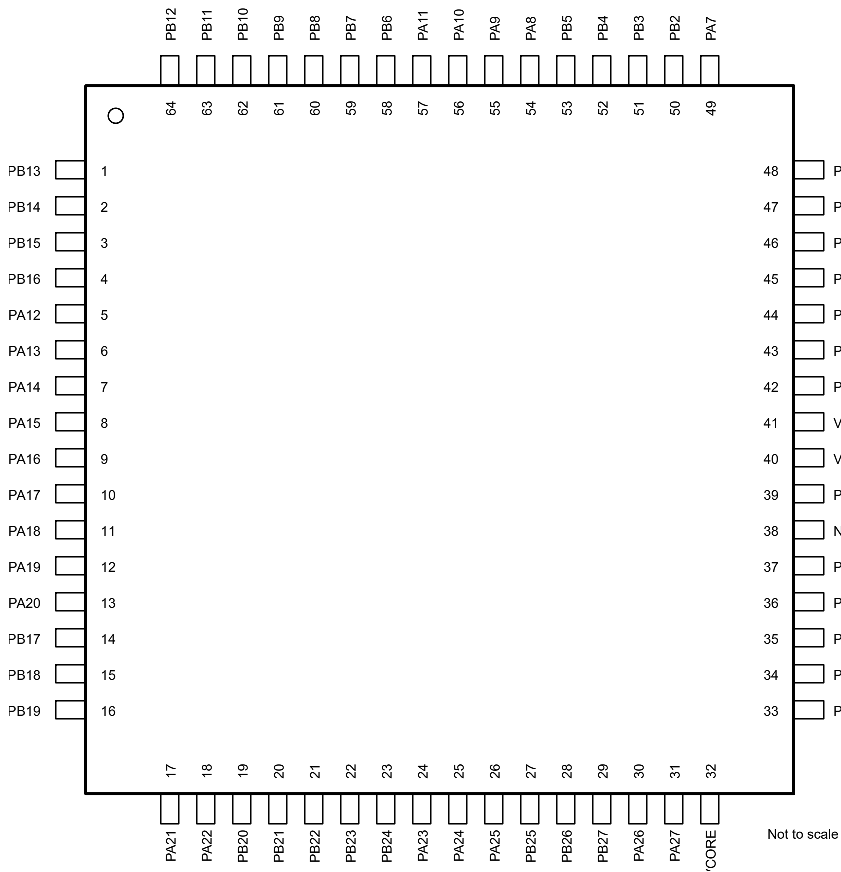

Figure 6-1. 64-pin PM (0.5mm) (LQFP) Package Diagram

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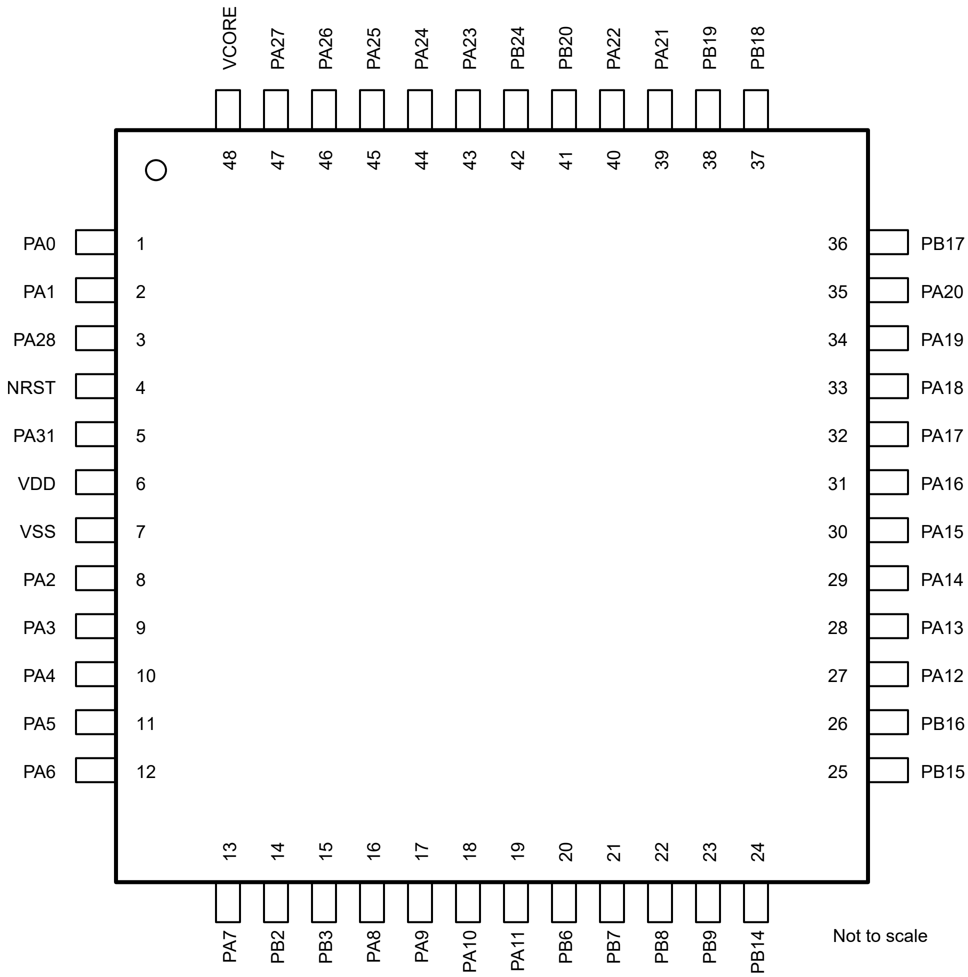

Figure 6-2. 48-pin PT (0.5mm) (LQFP) Package Diagram

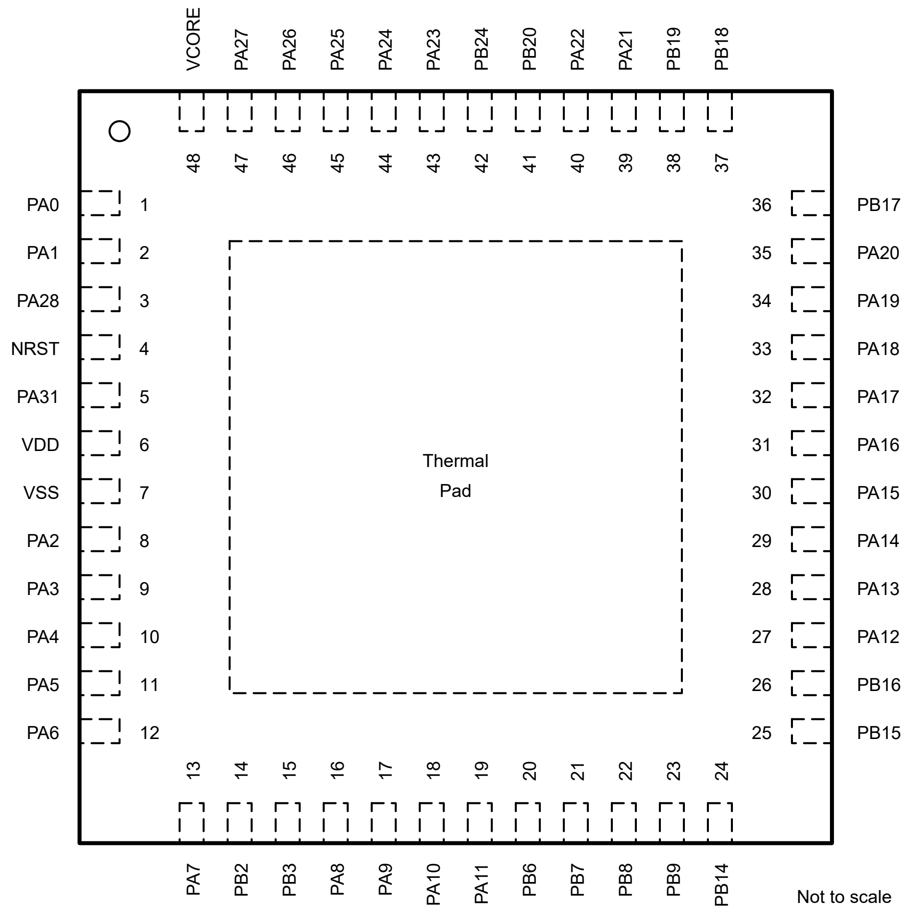

Figure 6-3. 48-pin RGZ (0.5mm) (VQFN) Package Diagram

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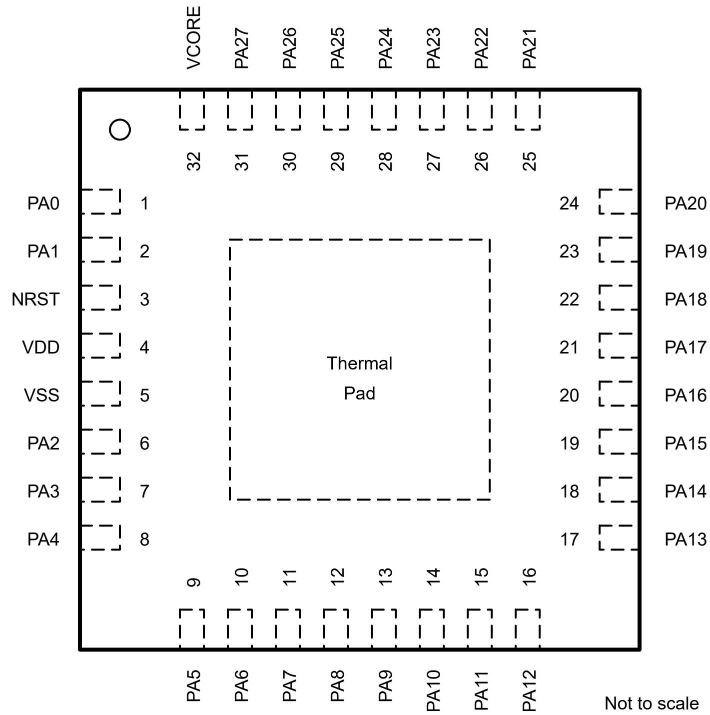

Figure 6-4. 32-pin RHB (0.5mm) (VQFN) Package Diagram

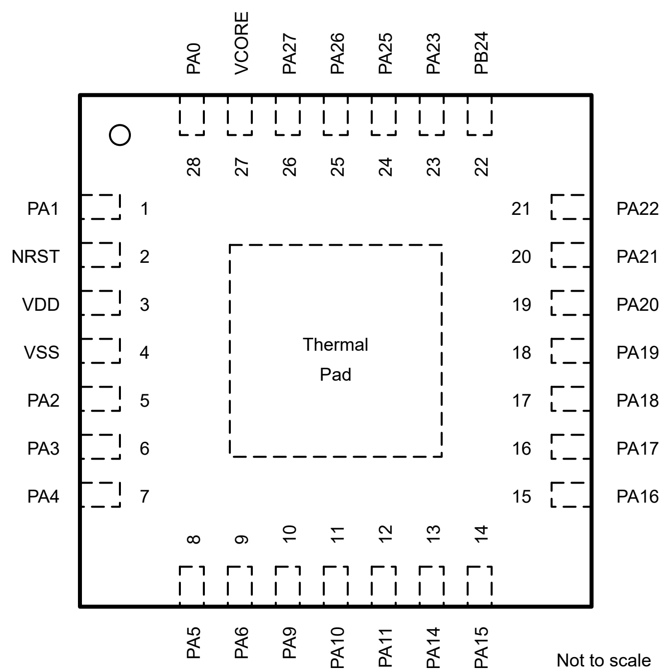

Figure 6-5. 28-pin RUY (0.5mm) (VQFN) Package Diagram

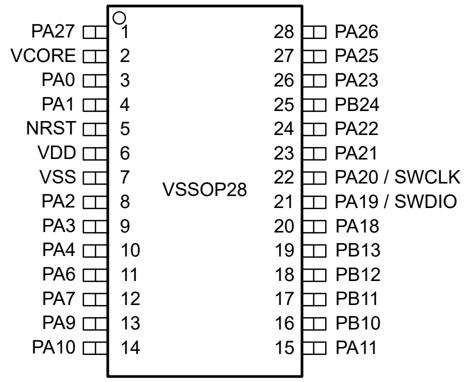

Figure 6-6. 28-pin 28DGS (0.5mm)(VSSOP) Package Diagram

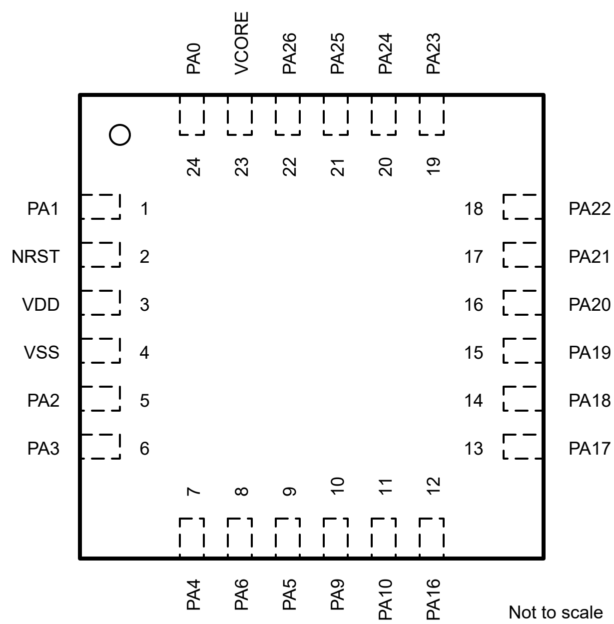

Figure 6-7. 24-pin RGE (0.5mm)(VQFN) Package Diagram

6.2 Pin Attributes

The following table describes the functions available on every pin for each device package.

Note

Each digital I/O on a device is mapped to a specific Pin Control Management Register (PINCMx) that lets users configure the desired *Pin Function* using the PINCM.PF control bits.

Each digital I/O on a device is mapped to a specific Pin Control Management Register (PINCMx) which allows users to configure the desired Pin Function using the PINCM.PF control bits. The IOMUX only supports connecting one IOMUX-managed digital function to the pin at the same time. The PINCM.PF and PINCM.PC in IOMUX are recommended to be set to 0 when non-IOMUX managed functions (such as analog connections) are intended to be used on a pin. However, non-IOMUX managed signals (such as analog inputs and WAKE inputs) can be enabled on a pin at the same time that an IOMUX managed digital function is enabled on the pin,

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provided there is no contention between the functions. In this case, the designer must verify that no contention exists between the functions enabled on each pin.

Table 6-1. Digital IO Features by IO Type

BUFFER TYPE	INVERSION CONTROL	DRIVE STRENGTH CONTROL	HYSTERESIS CONTROL	PULLUP RESISTOR	PULLDOWN RESISTOR	WAKEUP LOGIC
SDIO (standard drive)	Y			Y	Y	
SDIO (standard drive) with wake[(1)]	Y			Y	Y	Y
HDIO (High drive)	Y	Y		Y	Y	Y
HSIO (High speed)	Y	Y		Y	Y	
ODIO (5V-tolerant open drain)	Y		Y		Y	Y

1. Standard with Wake allows the I/O to wake up the device from the lowest low-power mode of SHUTDOWN. All I/O can be configured to wakeup the MCU from higher low-power modes. See section *GPIO FastWake* in the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*. for details.

Table 6-2. Pin Attributes (PM, PT, RGZ, RHB, DGS28, RGE, RUY Packages)

PM PIN	PT PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	RUY PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
38	4	4	3	5	2	2	NRST	NRST	(Non-IOMUX 1) 0	RESET	RESET
33	1	1	1	3	24	28	PA0 PINCM1 0x40428000	PA0	1	IO	ODIO (5V-tol)with wake
								UC4_PICO_TX	2	IO	
								UC0_SDA_TX	3	IOD	
								TIMA0_C0	4	IO	
								TIMA_FAL1	5	I	
								FCC_IN	6	I	
								TIMG8_C1	7	IO	
								TIMG0_C0	9	IO	
								BSL_I2C_SDA	(Non-IOMUX 1) 0	IOD	
34	2	2	2	4	1	1	PA1 PINCM2 0x40428004	PA1	1	IO	ODIO (5V-tol)with wake
								UC4_SCLK_RX	2	IOD	
								UC0_SCL_RX	3	IOD	
								TIMA0_C1	4	IO	
								TIMA_FAL2	5	I	
								TIMG8_IDX	6	I	
								TIMG8_C0	7	IO	
								TIMG0_C1	9	IO	
								UC2_CS3	10	IO	
								BSL_I2C_SCL	(Non-IOMUX 1) 0	IOD	
42	8	8	6	8	5	5	PA2 PINCM7 0x40428018	PA2	1	IO	SDIO (standard)
								TIMG8_C1	2	IO	
								UC2_CS0	3	IO	
								UC4_CS0_CTS	5	IO	
								TIMA0_C3N	6	O	
								TIMA0_C2N	7	O	
								TIMA_FAL0	8	I	
								TIMA_FAL1	9	I	
								TIMA0_C0	11	IO	
								ROSC	(Non-IOMUX 1) 0	A	

Table 6-2. Pin Attributes (PM, PT, RGZ, RHB, DGS28, RGE, RUY Packages) (continued)

PM PIN	PT PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	RUY PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
43	9	9	7	9	6	6	PA3 PINCM8 0x4042801c	PA3	1	IO	SDIO (standard)
								TIMG8_C0	2	IO	
								UC2_CS1	3	IO	
								UC5_SDA_TX	4	IOD	
								TIMA0_C1	5	IO	
								COMP0_OUT	6	O	
								TIMA0_C2	8	IO	
								UC0_CTS	9	IO	
								UC2_CS3	11	IO	
								COMP1_OUT	12	O	
								LFXIN	(Non-IOMUX 1) 0	A	
44	10	10	8	10	7	7	PA4 PINCM9 0x40428020	PA4	1	IO	SDIO (standard)
								TIMG8_C1	2	IO	
								UC2_POCI	3	IO	
								UC5_SCL_RX	4	IOD	
								TIMA0_C1N	5	O	
								LFCLKIN	6	I	
								TIMA0_C3	8	IO	
								UC0_RTS	9	IO	
								UC2_CS0	11	IO	
								LFXOUT	(Non-IOMUX 1) 0	A	
45	11	11	9		9	8	PA5 PINCM10 0x40428024	PA5	1	IO	SDIO (standard)
								TIMG8_C0	2	IO	
								UC2_PICO	3	IO	
								UC5_SDA_TX	4	IOD	
								TIMG0_C0	5	IO	
								FCC_IN	6	I	
								TIMA_FAL1	8	I	
								UC4_CS0_CTS	9	IO	
								HFXIN	(Non-IOMUX 1) 0	A	
46	12	12	10	11	8	9	PA6 PINCM11 0x40428028	PA6	1	IO	SDIO (standard)
								TIMG8_C1	2	IO	
								UC2_SCLK	3	IOD	
								UC5_SCL_RX	4	IOD	
								TIMG0_C1	5	IO	
								HFCLKIN	6	I	
								TIMA_FAL0	8	I	
								UC4_POCI_RTS	9	IO	
								TIMA0_C2N	10	O	
								HFXOUT	(Non-IOMUX 1) 0	A	

Table 6-2. Pin Attributes (PM, PT, RGZ, RHB, DGS28, RGE, RUY Packages) (continued)

PM PIN	PT PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	RUY PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
49	13	13	11	12			PA7 PINCM14 0x40428034	PA7	1	IO	SDIO (standard)
								COMP0_OUT	2	O	
								CLK_OUT	3	O	
								TIMG8_C0	4	IO	
								TIMA0_C2	5	IO	
								TIMG8_IDX	6	I	
								TIMA0_C1	8	IO	
								UC2_CS2	9	IO	
								FCC_IN	10	I	
								UC2_POCI	11	IO	
54	16	16	12				PA8 PINCM19 0x40428048	PA8	1	IO	SDIO (standard)
								UC5_SDA_TX	2	IOD	
								UC2_CS0	3	IO	
								UC0_SDA_TX	4	IOD	
								TIMA0_C0	5	IO	
								TIMA_FAL2	6	I	
								TIMA_FAL0	7	I	
								UC2_CS3	8	IO	
								HFCLKIN	10	I	
								UC4_POCI_RTS	11	IO	
								TIMA1_C0N	12	O	
55	17	17	13	13	10	10	PA9 PINCM20 0x4042804c	PA9	1	IO	HSIO (high-speed)
								UC5_SCL_RX	2	IOD	
								UC2_PICO	3	IO	
								UC0_SCL_RX	4	IOD	
								TIMA0_C0N	5	O	
								CLK_OUT	6	O	
								TIMA0_C1	7	IO	
								RTC_OUT	8	O	
								UC4_CS0_CTS	11	IO	
								TIMA1_C1N	12	O	
56	18	18	14	14	11	11	PA10 PINCM21 0x40428050	PA10	1	IO	HDIO (high-drive)with wake
								UC4_PICO_TX	2	IO	
								UC2_POCI	3	IO	
								UC0_SDA_TX	4	IOD	
								TIMA0_C2	5	IO	
								CLK_OUT	6	O	
								TIMG0_C0	7	IO	
								UC5_SDA_TX	8	IOD	
								TIMA_FAL1	10	I	
								TIMA1_C0	11	IO	
								COMP1_DAC_OUT	(Non-IOMUX 1) 0	A	
								BSL_UART_RX	(Non-IOMUX 2) 0	IO	

Table 6-2. Pin Attributes (PM, PT, RGZ, RHB, DGS28, RGE, RUY Packages) (continued)

PM PIN	PT PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	RUY PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
57	19	19	15	15		12	PA11 PINCM22 0x40428054	PA11	1	IO	HDIO (high-drive)with wake
								UC4_SCLK_RX	2	IOD	
								UC2_SCLK	3	IOD	
								UC0_SCL_RX	4	IOD	
								TIMA0_C2N	5	O	
								COMP0_OUT	6	O	
								TIMG0_C1	7	IO	
								UC5_SCL_RX	8	IOD	
								TIMA_FAL0	10	I	
								TIMA1_C1	11	IO	
								COMP0_DAC_OUT	(Non-IOMUX 1) 0	A	
								BSL_UART_TX	(Non-IOMUX 2) 0	IO	
5	27	27	16				PA12 PINCM34 0x40428084	PA12	1	IO	HSIO (high-speed)
								UC2_SCLK	3	IOD	
								COMP0_OUT	4	O	
								TIMA0_C3	5	IO	
								FCC_IN	6	I	
								TIMG0_C0	7	IO	
								UC2_CS1	9	IO	
								UC0_CTS	10	IO	
								CANFD0_CANTX	12	O	
								ADC0_8	(Non-IOMUX 1) 0	A	
6	28	28	17				PA13 PINCM35 0x40428088	PA13	1	IO	HSIO (high-speed)
								UC2_POCI	3	IO	
								UC9_RX	4	IO	
								TIMA0_C3N	5	O	
								RTC_OUT	6	O	
								TIMG0_C1	7	IO	
								UC4_CS0_CTS	8	IO	
								UC2_CS3	9	IO	
								UC0_SDA_TX	10	IOD	
								CANFD0_CANRX	12	I	
								ADC0_9	(Non-IOMUX 1) 0	A	
								COMP0_IN2-	(Non-IOMUX 2) 0	A	
7	29	29	18			13	PA14 PINCM36 0x4042808c	PA14	1	IO	HSIO (high-speed)
								UC4_CS0_CTS	2	IO	
								UC2_PICO	3	IO	
								UC9_TX	4	IO	
								CLK_OUT	6	O	
								UC2_CS2	9	IO	
								UC0_SCL_RX	10	IOD	
								ADC0_12	(Non-IOMUX 1) 0	A	
								COMP0_IN2+	(Non-IOMUX 2) 0	A	

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Table 6-2. Pin Attributes (PM, PT, RGZ, RHB, DGS28, RGE, RUY Packages) (continued)

PM PIN	PT PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	RUY PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
8	30	30	19			14	PA15 PINCM37 0x40428090	PA15	1	IO	SDIO (standard)
								UC4_POCI_RTS	2	IO	
								UC5_SCL_RX	4	IOD	
								TIMA0_C2	5	IO	
								TIMG8_IDX	7	I	
								TIMA1_C0N	9	O	
								UC0_RTS	10	IO	
								TIMA1_C0	11	IO	
								ADC1_0	(Non-IOMUX 1) 0	A	
								COMP0_IN3+	(Non-IOMUX 2) 0	A	
								COMP1_IN3+	(Non-IOMUX 3) 0	A	
9	31	31	20		12	15	PA16 PINCM38 0x40428094	PA16	1	IO	SDIO (standard)
								COMP0_OUT	2	O	
								UC4_POCI_RTS	3	IO	
								UC5_SDA_TX	4	IOD	
								TIMA0_C2N	5	O	
								FCC_IN	7	I	
								UC0_CTS	10	IO	
								TIMA1_C1	11	IO	
								TIMA1_C1N	12	O	
								ADC1_1	(Non-IOMUX 1) 0	A	
10	32	32	21		13	16	PA17 PINCM39 0x40428098	PA17	1	IO	SDIO (standard)with wake
								UC5_SDA_TX	2	IOD	
								UC4_SCLK_RX	3	IOD	
								UC5_SCL_RX	4	IOD	
								TIMA0_C3	5	IO	
								TIMG8_C0	7	IO	
								UC2_CS1	9	IO	
								TIMA1_C0	10	IO	
								ADC1_2	(Non-IOMUX 1) 0	A	
								COMP0_IN1-	(Non-IOMUX 2) 0	A	
11	33	33	22	20	14	17	PA18 PINCM40 0x4042809c	PA18	1	IO	SDIO (standard)with wake
								UC5_SCL_RX	2	IOD	
								UC4_PICO_TX	3	IO	
								UC5_SDA_TX	4	IOD	
								TIMA0_C3N	5	O	
								TIMG8_C1	7	IO	
								UC2_CS0	9	IO	
								TIMA1_C1	10	IO	
								ADC1_3	(Non-IOMUX 1) 0	A	
								COMP0_IN1+	(Non-IOMUX 2) 0	A	
								BSL_INVOKE	(Non-IOMUX 3) 0	I	

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Table 6-2. Pin Attributes (PM, PT, RGZ, RHB, DGS28, RGE, RUY Packages) (continued)

PM PIN	PT PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	RUY PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
12	34	34	23	21	15	18	PA19 PINCM41 0x404280a0	PA19	1	IO	SDIO (standard)
								SWDIO	2	IO	
								UC4_POCI_RTS	3	IO	
								UC5_SDA_TX	4	IOD	
								TIMA0_C2	5	IO	
								TIMG0_C0	6	IO	
								ADC0_13	(Non-IOMUX 1) 0	A	
13	35	35	24	22	16	19	PA20 PINCM42 0x404280a4	PA20	1	IO	SDIO (standard)
								SWCLK	2	I	
								UC4_SCLK_RX	3	IOD	
								UC5_SCL_RX	4	IOD	
								TIMA0_C2N	5	O	
								TIMG0_C1	6	IO	
								ADC0_14	(Non-IOMUX 1) 0	A	
17	39	39	25	23	17	20	PA21 PINCM46 0x404280b4	PA21	1	IO	SDIO (standard)
								UC0_SDA_TX	2	IOD	
								UC2_CS3	3	IO	
								TIMA0_C0	5	IO	
								UC0_CTS	8	IO	
								TIMG8_C0	10	IO	
								ADC1_7	(Non-IOMUX 1) 0	A	
								ADC0_VREF-	(Non-IOMUX 2) 0	A	
								ADC1_VREF-	(Non-IOMUX 3) 0	A	
18	40	40	26	24	18	21	PA22 PINCM47 0x404280b8	PA22	1	IO	SDIO (standard)
								UC0_SCL_RX	2	IOD	
								UC2_CS2	3	IO	
								TIMA0_C0N	5	O	
								TIMA0_C1	7	IO	
								CLK_OUT	8	O	
								TIMG8_C1	10	IO	
								ADC0_7	(Non-IOMUX 1) 0	A	
24	43	43	27	26	19	23	PA23 PINCM53 0x404280d0	PA23	1	IO	SDIO (standard)
								UC0_SDA_TX	2	IOD	
								UC2_CS3	3	IO	
								TIMG1_C0	4	IO	
								TIMA0_C3	5	IO	
								TIMG8_C0	6	IO	
								TIMG0_C0	9	IO	
								ADC1_12	(Non-IOMUX 1) 0	A	
								COMP1_IN1-	(Non-IOMUX 2) 0	A	
								ADC0_VREF+	(Non-IOMUX 3) 0	A	

Table 6-2. Pin Attributes (PM, PT, RGZ, RHB, DGS28, RGE, RUY Packages) (continued)

PM PIN	PT PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	RUY PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
25	44	44	28		20		PA24 PINCM54 0x404280d4	PA24	1	IO	SDIO (standard)
								UC0_SCL_RX	2	IOD	
								UC2_CS2	3	IO	
								TIMA0_C3N	5	O	
								TIMG8_C1	6	IO	
								TIMA1_C1	7	IO	
								TIMG0_C1	9	IO	
								ADC0_3	(Non-IOMUX 1) 0	A	
26	45	45	29	27	21	24	PA25 PINCM55 0x404280d8	PA25	1	IO	SDIO (standard)
								UC9_RX	2	IO	
								TIMG1_C1	4	IO	
								TIMA0_C3	5	IO	
								TIMA0_C1N	6	O	
								COMP0_OUT	7	O	
								UC0_CTS	8	IO	
								UC9_TX	9	IO	
								CANFD0_CANRX	10	I	
								ADC0_2	(Non-IOMUX 1) 0	A	
30	46	46	30	28	22	25	PA26 PINCM59 0x404280e8	PA26	1	IO	SDIO (standard)
								UC9_TX	2	IO	
								UC4_CS0_CTS	3	IO	
								TIMG8_C0	4	IO	
								TIMA_FAL0	5	I	
								TIMA0_C3N	6	O	
								UC0_RTS	8	IO	
								UC9_RX	9	IO	
								CANFD0_CANTX	10	O	
								ADC0_1	(Non-IOMUX 1) 0	A	
								COMP0_IN0+	(Non-IOMUX 2) 0	A	
31	47	47	31	1		26	PA27 PINCM60 0x404280ec	PA27	1	IO	SDIO (standard)
								UC9_RX	2	IO	
								TIMG8_C1	4	IO	
								TIMA_FAL2	5	I	
								CLK_OUT	6	O	
								RTC_OUT	8	O	
								COMP0_OUT	9	O	
								CANFD0_CANRX	10	I	
								ADC0_0	(Non-IOMUX 1) 0	A	
								COMP0_IN0-	(Non-IOMUX 2) 0	A	
35	3	3					PA28 PINCM3 0x40428008	PA28	1	IO	HDIO (high-drive)with wake
								UC4_PICO_TX	2	IO	
								UC0_SDA_TX	3	IOD	
								TIMA0_C3	4	IO	
								TIMA_FAL0	5	I	
								TIMA0_C1	7	IO	
								TIMA1_C0	9	IO	

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Table 6-2. Pin Attributes (PM, PT, RGZ, RHB, DGS28, RGE, RUY Packages) (continued)

PM PIN	PT PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	RUY PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
36							PA29 PINCM4 0x4042800c	PA29	1	IO	SDIO (standard)
								UC5_SCL_RX	2	IOD	
								UC0_RTS	3	IO	
								TIMG8_C0	4	IO	
								UC4_CS0_CTS	7	IO	
								UC2_CS3	8	IO	
								TIMG1_C0	11	IO	
37							PA30 PINCM5 0x40428010	PA30	1	IO	SDIO (standard)
								UC5_SDA_TX	2	IOD	
								UC0_CTS	3	IO	
								TIMG8_C1	4	IO	
								UC4_POCI_RTS	7	IO	
								UC2_CS2	8	IO	
								TIMG1_C1	11	IO	
39	5	5					PA31 PINCM6 0x40428014	PA31	1	IO	SDIO (standard)with wake
								UC4_SCLK_RX	2	IOD	
								UC0_SCL_RX	3	IOD	
								TIMA0_C3N	4	O	
								CLK_OUT	6	O	
								UC2_CS3	8	IO	
								TIMA1_C1	11	IO	
47							PB0 PINCM12 0x4042802c	PB0	1	IO	SDIO (standard)
								UC4_PICO_TX	2	IO	
								UC0_SCL_RX	4	IOD	
								TIMA0_C2	5	IO	
								TIMG0_C0	6	IO	
								UC2_CS3	7	IO	
								TIMA1_C0	8	IO	
48							PB1 PINCM13 0x40428030	PB1	1	IO	SDIO (standard)
								UC4_SCLK_RX	2	IOD	
								UC0_SDA_TX	4	IOD	
								TIMA0_C2N	5	O	
								TIMG0_C1	6	IO	
								UC2_CS2	7	IO	
								TIMA1_C1	8	IO	
50	14	14					PB2 PINCM15 0x40428038	PB2	1	IO	SDIO (standard)
								UC9_TX	2	IO	
								UC0_CTS	3	IO	
								UC5_SCL_RX	4	IOD	
								TIMA0_C3	5	IO	
								TIMG1_C0	7	IO	
								UC0_SDA_TX	8	IOD	
								HFCLKIN	10	I	
								UC2_PICO	11	IO	
								TIMA1_C0	12	IO	

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Table 6-2. Pin Attributes (PM, PT, RGZ, RHB, DGS28, RGE, RUY Packages) (continued)

PM PIN	PT PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	RUY PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
51	15	15					PB3 PINCM16 0x4042803c	PB3	1	IO	SDIO (standard)
								UC9_RX	2	IO	
								UC0_RTS	3	IO	
								UC5_SDA_TX	4	IOD	
								TIMA0_C3N	5	O	
								TIMG1_C1	7	IO	
								UC0_SCL_RX	8	IOD	
								TIMA0_C0	10	IO	
								UC2_SCLK	11	IOD	
								TIMA1_C1	12	IO	
52							PB4 PINCM17 0x40428040	PB4	1	IO	SDIO (standard)
								UC5_SDA_TX	2	IOD	
								TIMA0_C1	4	IO	
								TIMA0_C2	5	IO	
								TIMG0_C0	6	IO	
								TIMA1_C0	8	IO	
								TIMA1_C0N	11	O	
53							PB5 PINCM18 0x40428044	PB5	1	IO	SDIO (standard)
								UC5_SCL_RX	2	IOD	
								TIMA0_C1N	4	O	
								TIMA0_C2N	5	O	
								TIMG0_C1	6	IO	
								TIMA1_C1	8	IO	
								TIMA1_C1N	11	O	
58	20	20					PB6 PINCM23 0x40428058	PB6	1	IO	SDIO (standard)
								UC5_SDA_TX	2	IOD	
								UC4_CS0_CTS	3	IO	
								TIMG8_C0	5	IO	
								UC0_CTS	6	IO	
								TIMA_FAL2	8	I	
								UC2_CS1	9	IO	
								TIMA1_C0N	12	O	
59	21	21					PB7 PINCM24 0x4042805c	PB7	1	IO	SDIO (standard)
								UC5_SCL_RX	2	IOD	
								UC4_POCI_RTS	3	IO	
								TIMG8_C1	5	IO	
								UC0_RTS	6	IO	
								UC2_CS2	9	IO	
								TIMA1_C1N	12	O	
60	22	22					PB8 PINCM25 0x40428060	PB8	1	IO	SDIO (standard)
								UC4_PICO_TX	3	IO	
								TIMA0_C0	5	IO	
								COMP0_OUT	6	O	
								COMP1_OUT	8	O	
61	23	23					PB9 PINCM26 0x40428064	PB9	1	IO	SDIO (standard)
								UC4_SCLK_RX	3	IOD	
								TIMA0_C0N	5	O	
								TIMA0_C1	6	IO	

Table 6-2. Pin Attributes (PM, PT, RGZ, RHB, DGS28, RGE, RUY Packages) (continued)

PM PIN	PT PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	RUY PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
62				16			PB10 PINCM27 0x40428068	PB10	1	IO	SDIO (standard)
								TIMG0_C0	2	IO	
								TIMG8_C0	3	IO	
								COMP0_OUT	4	O	
								COMP1_OUT	11	O	
63				17			PB11 PINCM28 0x4042806c	PB11	1	IO	SDIO (standard)
								TIMG0_C1	2	IO	
								TIMG8_C1	3	IO	
								CLK_OUT	4	O	
64				18			PB12 PINCM29 0x40428070	PB12	1	IO	SDIO (standard)
								UC9_TX	2	IO	
								TIMA0_C2	3	IO	
								TIMA_FAL1	4	I	
								TIMA0_C1	5	IO	
								TIMG1_C0	10	IO	
1				19			PB13 PINCM30 0x40428074	PB13	1	IO	SDIO (standard)
								UC9_RX	2	IO	
								TIMA0_C3	3	IO	
								TIMA0_C1N	5	O	
								UC4_CS0_CTS	7	IO	
								TIMG1_C1	10	IO	
2	24	24					PB14 PINCM31 0x40428078	PB14	1	IO	SDIO (standard)
								UC4_POCI_RTS	3	IO	
								TIMA0_C0	5	IO	
								TIMG8_IDX	6	I	
								UC2_CS3	7	IO	
3	25	25					PB15 PINCM32 0x4042807c	PB15	1	IO	SDIO (standard)
								UC0_SDA_TX	2	IOD	
								UC4_PICO_TX	3	IO	
								TIMG8_C0	5	IO	
4	26	26					PB16 PINCM33 0x40428080	PB16	1	IO	SDIO (standard)
								UC0_SCL_RX	2	IOD	
								UC4_SCLK_RX	3	IOD	
								TIMG8_C1	5	IO	
14	36	36					PB17 PINCM43 0x404280a8	PB17	1	IO	SDIO (standard)
								UC0_SDA_TX	2	IOD	
								UC2_PICO	3	IO	
								UC0_SCL_RX	4	IOD	
								TIMA0_C2	5	IO	
								TIMG0_C0	6	IO	
								TIMA1_C0	11	IO	
								ADC1_4	(Non-IOMUX 1) 0	A	
								COMP1_IN2-	(Non-IOMUX 2) 0	A	

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Table 6-2. Pin Attributes (PM, PT, RGZ, RHB, DGS28, RGE, RUY Packages) (continued)

PM PIN	PT PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	RUY PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
15	37	37					PB18 PINCM44 0x404280ac	PB18	1	IO	SDIO (standard)
								UC0_SCL_RX	2	IOD	
								UC2_SCLK	3	IOD	
								UC0_SDA_TX	4	IOD	
								TIMA0_C2N	5	O	
								TIMG0_C1	6	IO	
								TIMA1_C1	11	IO	
								ADC1_5	(Non-IOMUX 1) 0	A	
								COMP1_IN2+	(Non-IOMUX 2) 0	A	
16	38	38					PB19 PINCM45 0x404280b0	PB19	1	IO	SDIO (standard)
								COMP0_OUT	2	O	
								UC2_POCI	3	IO	
								TIMG8_C1	4	IO	
								UC4_CS0_CTS	5	IO	
								TIMG8_IDX	7	I	
								UC0_CTS	8	IO	
								ADC1_6	(Non-IOMUX 1) 0	A	
19	41	41					PB20 PINCM48 0x404280bc	PB20	1	IO	SDIO (standard)
								UC2_CS2	2	IO	
								UC4_CS0_CTS	3	IO	
								TIMA0_C2	5	IO	
								TIMA_FAL1	6	I	
								TIMA0_C1	7	IO	
								UC0_RTS	8	IO	
								UC0_SDA_TX	9	IOD	
								TIMA1_C1N	10	O	
								ADC0_6	(Non-IOMUX 1) 0	A	
20							PB21 PINCM49 0x404280c0	PB21	1	IO	SDIO (standard)
								UC4_POCI_RTS	3	IO	
								UC0_SCL_RX	4	IOD	
								TIMG8_C0	5	IO	
								UC5_SDA_TX	6	IOD	
								ADC1_8	(Non-IOMUX 1) 0	A	
21							PB22 PINCM50 0x404280c4	PB22	1	IO	SDIO (standard)
								UC4_PICO_TX	3	IO	
								UC0_SDA_TX	4	IOD	
								TIMG8_C1	5	IO	
								UC5_SCL_RX	6	IOD	
								ADC1_10	(Non-IOMUX 1) 0	A	
22							PB23 PINCM51 0x404280c8	PB23	1	IO	SDIO (standard)
								UC4_SCLK_RX	3	IOD	
								TIMA_FAL0	4	I	
								COMP0_OUT	5	O	
								ADC1_11	(Non-IOMUX 1) 0	A	

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Table 6-2. Pin Attributes (PM, PT, RGZ, RHB, DGS28, RGE, RUY Packages) (continued)

PM PIN	PT PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	RUY PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
23	42	42		25		22	PB24 PINCM52 0x404280cc	PB24	1	IO	SDIO (standard)
								UC2_CS3	2	IO	
								UC2_CS1	3	IO	
								TIMA0_C3	5	IO	
								TIMA0_C1N	6	O	
								UC0_RTS	8	IO	
								TIMA1_C0N	10	O	
								ADC0_5	(Non-IOMUX 1) 0	A	
								COMP1_IN1+	(Non-IOMUX 2) 0	A	
27							PB25 PINCM56 0x404280dc	PB25	1	IO	SDIO (standard)
								UC4_CS0_CTS	2	IO	
								UC2_CS0	3	IO	
								TIMA_FAL0	4	I	
								TIMA_FAL1	5	I	
								TIMA_FAL2	6	I	
								COMP0_OUT	7	O	
								FCC_IN	8	I	
								ADC0_4	(Non-IOMUX 1) 0	A	
28							PB26 PINCM57 0x404280e0	PB26	1	IO	SDIO (standard)
								UC4_POCI_RTS	2	IO	
								UC2_CS1	3	IO	
								TIMA0_C0	4	IO	
								TIMA0_C3	5	IO	
								COMP0_OUT	7	O	
								FCC_IN	8	I	
								TIMA1_C0	9	IO	
								ADC1_13	(Non-IOMUX 1) 0	A	
								COMP1_IN0+	(Non-IOMUX 2) 0	A	
29							PB27 PINCM58 0x404280e4	PB27	1	IO	SDIO (standard)
								COMP0_OUT	2	O	
								TIMA0_C0N	4	O	
								TIMA0_C3N	5	O	
								TIMA1_C1	9	IO	
								ADC1_14	(Non-IOMUX 1) 0	A	
								COMP1_IN0-	(Non-IOMUX 2) 0	A	
32	48	48	32	2	23	27	VCORE	VCORE	(Non-IOMUX 1) 0	PWR	PWR
40	6	6	4	6	3	3	VDD	VDD	(Non-IOMUX 1) 0	PWR	PWR
41	7	7	5	7	4	4	VSS	VSS	(Non-IOMUX 1) 0	PWR	PWR

6.3 Signal Descriptions

Many MSPM0 signals are made available on multiple device pins. The following list describes the column headers:

1. **SIGNAL NAME**: The name of the signal which can be connected to one of the specified pins.
2. **PIN TYPE**: The signal direction and signal type:
   - I = Input
   - O = Output
   - IO = Input, output, or simultaneous input and output

- ID = Input with open-drain behavior
- OD = Output with open-drain behavior
- IOD = Input, output, or simultaneous input and output with open-drain behavior
- A = Analog
- PWR = Power function

3. **DESCRIPTION**: A description of the signal.
4. **PIN**: Associated pin number.

For additional information on the pin multiplexing scheme, refer to the IOMUX chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

Note

The IOMUX only supports connecting one IOMUX-managed digital function to the pin at the same time. However, non-IOMUX managed signals (such as analog inputs and WAKE inputs) can be enabled on a pin at the same time that an IOMUX managed digital function is enabled on the pin. In this case, the designer must verify that no contention exists between the functions enabled on each pin.

Table 6-3. Analog to Digital Converter (ADC) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PM PIN	PT PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	RUY PIN
ADC0_VREF+	A	ADC0 voltage reference (VREF) power supply	24	43	43	27	26	19	23
ADC0_VREF-	A	ADC0 voltage reference (VREF) ground supply	17	39	39	25	23	17	20
ADC1_VREF-	A	ADC1 voltage reference (VREF) ground supply	17	39	39	25	23	17	20
ADC0_0	A	ADC0 analog input channel 0	31	47	47	31	1		26
ADC0_1	A	ADC0 analog input channel 1	30	46	46	30	28	22	25
ADC0_2	A	ADC0 analog input channel 2	26	45	45	29	27	21	24
ADC0_3	A	ADC0 analog input channel 3	25	44	44	28		20	
ADC0_4	A	ADC0 analog input channel 4	27						
ADC0_5	A	ADC0 analog input channel 5	23	42	42		25		22
ADC0_6	A	ADC0 analog input channel 6	19	41	41				
ADC0_7	A	ADC0 analog input channel 7	18	40	40	26	24	18	21
ADC0_8	A	ADC0 analog input channel 8	5	27	27	16			
ADC0_9	A	ADC0 analog input channel 9	6	28	28	17			
ADC0_12	A	ADC0 analog input channel 12	7	29	29	18			13
ADC0_13	A	ADC0 analog input channel 13	12	34	34	23	21	15	18
ADC0_14	A	ADC0 analog input channel 14	13	35	35	24	22	16	19
ADC1_0	A	ADC1 analog input channel 0	8	30	30	19			14
ADC1_1	A	ADC1 analog input channel 1	9	31	31	20		12	15
ADC1_2	A	ADC1 analog input channel 2	10	32	32	21		13	16
ADC1_3	A	ADC1 analog input channel 3	11	33	33	22	20	14	17
ADC1_4	A	ADC1 analog input channel 4	14	36	36				
ADC1_5	A	ADC1 analog input channel 5	15	37	37				
ADC1_6	A	ADC1 analog input channel 6	16	38	38				
ADC1_7	A	ADC1 analog input channel 7	17	39	39	25	23	17	20
ADC1_8	A	ADC1 analog input channel 8	20						
ADC1_10	A	ADC1 analog input channel 10	21						
ADC1_11	A	ADC1 analog input channel 11	22						

Table 6-3. Analog to Digital Converter (ADC) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	PM PIN	PT PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	RUY PIN
ADC1_12	A	ADC1 analog input channel 12	24	43	43	27	26	19	23
ADC1_13	A	ADC1 analog input channel 13	28						
ADC1_14	A	ADC1 analog input channel 14	29						

Table 6-4. Bootstrap Loader (BSL) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PM PIN	PT PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	RUY PIN
BSL_I2C_SCL	IOD	BSL I2C data signal (SCL)	34	2	2	2	4	1	1
BSL_I2C_SDA	IOD	BSL I2C data signal (SDA)	33	1	1	1	3	24	28
BSL_INVOKE	I	BSL invoke signal (if BSL is enabled, must be HIGH during BOOTRST for a BSL entry, and LOW during BOOTRST to prevent BSL entry)	11	33	33	22	20	14	17
BSL_UART_RX	IO	BSL UART receive signal (RX)	56	18	18	14	14	11	11
BSL_UART_TX	IO	BSL UART transmit signal (TX)	57	19	19	15	15		12

Table 6-5. Clock Module (CKM) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PM PIN	PT PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	RUY PIN
CLK_OUT	O	CLK_OUT digital clock output from the PMCU	18, 31, 39, 49, 55, 56, 63, 7	13, 17, 18, 29, 40, 47, 5	13, 17, 18, 29, 40, 47, 5	11, 13, 14, 18, 26, 31	1, 12, 13, 14, 17, 24	10, 11, 18	10, 11, 13, 21, 26
FCC_IN	I	Frequency clock counter (FCC) input signal	27, 28, 33, 45, 49, 5, 9	1, 11, 13, 27, 31	1, 11, 13, 27, 31	1, 11, 16, 20, 9	12, 3	12, 24, 9	15, 28, 8
HFCLKIN	I	High frequency clock digital clock input signal	46, 50, 54	12, 14, 16	12, 14, 16	10, 12	11	8	9
HFXIN	A	High frequency crystal oscillator (HFXT) signal	45	11	11	9		9	8
HFXOUT	A	High frequency crystal oscillator (HFXT) signal	46	12	12	10	11	8	9
LFCLKIN	I	Low frequency clock digital clock input signal	44	10	10	8	10	7	7
LFXIN	A	Low frequency crystal oscillator (LFXT) signal	43	9	9	7	9	6	6
LFXOUT	A	Low frequency crystal oscillator (LFXT) signal	44	10	10	8	10	7	7
ROSC	A	SYSOSC frequency correction loop (FCL) external resistor signal	42	8	8	6	8	5	5

Table 6-6. Comparator (COMP) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PM PIN	PT PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	RUY PIN
COMP0_DAC_OUT	A	COMP0 DAC output	57	19	19	15	15		12
COMP0_OUT	O	COMP0 output	16, 22, 26, 27, 28, 29, 31, 43, 49, 5, 57, 60, 62, 9	13, 19, 22, 27, 31, 38, 45, 47, 9	13, 19, 22, 27, 31, 38, 45, 47, 9	11, 15, 16, 20, 29, 31, 7	1, 12, 15, 16, 27, 9	12, 21, 6	12, 15, 24, 26, 6

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Table 6-6. Comparator (COMP) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	PM PIN	PT PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	RUY PIN
COMP1_DAC_OUT	A	COMP1 DAC output	56	18	18	14	14	11	11
COMP1_OUT	O	COMP1 output	43, 60, 62	22, 9	22, 9	7	16, 9	6	6
COMP0_IN0+	A	COMP0 non-inverting input 0	30	46	46	30	28	22	25
COMP0_IN0-	A	COMP0 inverting input 0	31	47	47	31	1		26
COMP0_IN1+	A	COMP0 non-inverting input 1	11	33	33	22	20	14	17
COMP0_IN1-	A	COMP0 inverting input 1	10	32	32	21		13	16
COMP0_IN2+	A	COMP0 non-inverting input 2	7	29	29	18			13
COMP0_IN2-	A	COMP0 inverting input 2	6	28	28	17			
COMP0_IN3+	A	COMP0 non-inverting input 3	8	30	30	19			14
COMP1_IN0+	A	COMP1 non-inverting input 0	28						
COMP1_IN0-	A	COMP1 inverting input 0	29						
COMP1_IN1+	A	COMP1 non-inverting input 1	23	42	42		25		22
COMP1_IN1-	A	COMP1 inverting input 1	24	43	43	27	26	19	23
COMP1_IN2+	A	COMP1 non-inverting input 2	15	37	37				
COMP1_IN2-	A	COMP1 inverting input 2	14	36	36				
COMP1_IN3+	A	COMP1 non-inverting input 3	8	30	30	19			14

Table 6-7. General Purpose Input Output Module Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PM PIN	PT PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	RUY PIN
PA0	IO	GPIO port A input/output 0	33	1	1	1	3	24	28
PA1	IO	GPIO port A input/output 1	34	2	2	2	4	1	1
PA2	IO	GPIO port A input/output 2	42	8	8	6	8	5	5
PA3	IO	GPIO port A input/output 3	43	9	9	7	9	6	6
PA4	IO	GPIO port A input/output 4	44	10	10	8	10	7	7
PA5	IO	GPIO port A input/output 5	45	11	11	9		9	8
PA6	IO	GPIO port A input/output 6	46	12	12	10	11	8	9
PA7	IO	GPIO port A input/output 7	49	13	13	11	12		
PA8	IO	GPIO port A input/output 8	54	16	16	12			
PA9	IO	GPIO port A input/output 9	55	17	17	13	13	10	10
PA10	IO	GPIO port A input/output 10	56	18	18	14	14	11	11
PA11	IO	GPIO port A input/output 11	57	19	19	15	15		12
PA12	IO	GPIO port A input/output 12	5	27	27	16			
PA13	IO	GPIO port A input/output 13	6	28	28	17			
PA14	IO	GPIO port A input/output 14	7	29	29	18			13
PA15	IO	GPIO port A input/output 15	8	30	30	19			14
PA16	IO	GPIO port A input/output 16	9	31	31	20		12	15
PA17	IO	GPIO port A input/output 17	10	32	32	21		13	16
PA18	IO	GPIO port A input/output 18	11	33	33	22	20	14	17
PA19	IO	GPIO port A input/output 19	12	34	34	23	21	15	18
PA20	IO	GPIO port A input/output 20	13	35	35	24	22	16	19
PA21	IO	GPIO port A input/output 21	17	39	39	25	23	17	20
PA22	IO	GPIO port A input/output 22	18	40	40	26	24	18	21
PA23	IO	GPIO port A input/output 23	24	43	43	27	26	19	23

Table 6-7. General Purpose Input Output Module Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	PM PIN	PT PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	RUY PIN
PA24	IO	GPIO port A input/output 24	25	44	44	28		20	
PA25	IO	GPIO port A input/output 25	26	45	45	29	27	21	24
PA26	IO	GPIO port A input/output 26	30	46	46	30	28	22	25
PA27	IO	GPIO port A input/output 27	31	47	47	31	1		26
PA28	IO	GPIO port A input/output 28	35	3	3				
PA29	IO	GPIO port A input/output 29	36						
PA30	IO	GPIO port A input/output 30	37						
PA31	IO	GPIO port A input/output 31	39	5	5				
PB0	IO	GPIO port B input/output 0	47						
PB1	IO	GPIO port B input/output 1	48						
PB2	IO	GPIO port B input/output 2	50	14	14				
PB3	IO	GPIO port B input/output 3	51	15	15				
PB4	IO	GPIO port B input/output 4	52						
PB5	IO	GPIO port B input/output 5	53						
PB6	IO	GPIO port B input/output 6	58	20	20				
PB7	IO	GPIO port B input/output 7	59	21	21				
PB8	IO	GPIO port B input/output 8	60	22	22				
PB9	IO	GPIO port B input/output 9	61	23	23				
PB10	IO	GPIO port B input/output 10	62				16		
PB11	IO	GPIO port B input/output 11	63				17		
PB12	IO	GPIO port B input/output 12	64				18		
PB13	IO	GPIO port B input/output 13	1				19		
PB14	IO	GPIO port B input/output 14	2	24	24				
PB15	IO	GPIO port B input/output 15	3	25	25				
PB16	IO	GPIO port B input/output 16	4	26	26				
PB17	IO	GPIO port B input/output 17	14	36	36				
PB18	IO	GPIO port B input/output 18	15	37	37				
PB19	IO	GPIO port B input/output 19	16	38	38				
PB20	IO	GPIO port B input/output 20	19	41	41				
PB21	IO	GPIO port B input/output 21	20						
PB22	IO	GPIO port B input/output 22	21						
PB23	IO	GPIO port B input/output 23	22						
PB24	IO	GPIO port B input/output 24	23	42	42		25		22
PB25	IO	GPIO port B input/output 25	27						
PB26	IO	GPIO port B input/output 26	28						
PB27	IO	GPIO port B input/output 27	29						

Table 6-8. Controller Area Network (CAN) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PM PIN	PT PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	RUY PIN
CANFD0_CANRX	I	CANFD0 receive signal	26, 31, 6	28, 45, 47	28, 45, 47	17, 29, 31	1, 27	21	24, 26
CANFD0_CANTX	O	CANFD0 transmit signal	30, 5	27, 46	27, 46	16, 30	28	22	25

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Table 6-9. Real-time Clock (RTC) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PM PIN	PT PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	RUY PIN
RTC_OUT	O	Real-time clock output signal	31, 55, 6	17, 28, 47	17, 28, 47	13, 17, 31	1, 13	10	10, 26

Table 6-10. Serial Wire Debug (SWD) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PM PIN	PT PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	RUY PIN
SWCLK	I	Serial wire debug interface clock input signal	13	35	35	24	22	16	19
SWDIO	IO	Serial wire debug interface data input/output signal	12	34	34	23	21	15	18

Table 6-11. System Controller (SYSCTL) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PM PIN	PT PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	RUY PIN
NRST	RESET	Active-low reset signal (must be logic high for the device to start)	38	4	4	3	5	2	2
VCORE	PWR	VCORE capacitor connection	32	48	48	32	2	23	27
VDD	PWR	VDD supply	40	6	6	4	6	3	3
VSS	PWR	VSS (ground)	41	7	7	5	7	4	4

Table 6-12. Timer (TIMx) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PM PIN	PT PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	RUY PIN
TIMA0_C0	IO	TIMA0 capture/compare 0 signal	17, 2, 28, 33, 42, 51, 54, 60	1, 15, 16, 22, 24, 39, 8	1, 15, 16, 22, 24, 39, 8	1, 12, 25, 6	23, 3, 8	17, 24, 5	20, 28, 5
TIMA0_C1	IO	TIMA0 capture/compare 1 signal	18, 19, 34, 35, 43, 49, 52, 55, 61, 64	13, 17, 2, 23, 3, 40, 41, 9	13, 17, 2, 23, 3, 40, 41, 9	11, 13, 2, 26, 7	12, 13, 18, 24, 4, 9	1, 10, 18, 6	1, 10, 21, 6
TIMA0_C2	IO	TIMA0 capture/compare 2 signal	12, 14, 19, 43, 47, 49, 52, 56, 64, 8	13, 18, 30, 34, 36, 41, 9	13, 18, 30, 34, 36, 41, 9	11, 14, 19, 23, 7	12, 14, 18, 21, 9	11, 15, 6	11, 14, 18, 6
TIMA0_C3	IO	TIMA0 capture/compare 3 signal	1, 10, 23, 24, 26, 28, 35, 44, 5, 50	10, 14, 27, 3, 32, 42, 43, 45	10, 14, 27, 3, 32, 42, 43, 45	16, 21, 27, 29, 8	10, 19, 25, 26, 27	13, 19, 21, 7	16, 22, 23, 24, 7
TIMA0_C0N	O	TIMA0 capture/compare 0 complementary output	18, 29, 55, 61	17, 23, 40	17, 23, 40	13, 26	13, 24	10, 18	10, 21
TIMA0_C1N	O	TIMA0 capture/compare 1 complementary output	1, 23, 26, 44, 53	10, 42, 45	10, 42, 45	29, 8	10, 19, 25, 27	21, 7	22, 24, 7
TIMA0_C2N	O	TIMA0 capture/compare 2 complementary output	13, 15, 42, 46, 48, 53, 57, 9	12, 19, 31, 35, 37, 8	12, 19, 31, 35, 37, 8	10, 15, 20, 24, 6	11, 15, 22, 8	12, 16, 5, 8	12, 15, 19, 5, 9

Table 6-12. Timer (TIMx) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	PM PIN	PT PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	RUY PIN
TIMA0_C3N	O	TIMA0 capture/compare 3 complementary output	11, 25, 29, 30, 39, 42, 51, 6	15, 28, 33, 44, 46, 5, 8	15, 28, 33, 44, 46, 5, 8	17, 22, 28, 30, 6	20, 28, 8	14, 20, 22, 5	17, 25, 5
TIMA1_C0	IO	TIMA1 capture/compare 0 signal	10, 14, 28, 35, 47, 50, 52, 56, 8	14, 18, 3, 30, 32, 36	14, 18, 3, 30, 32, 36	14, 19, 21	14	11, 13	11, 14, 16
TIMA1_C1	IO	TIMA1 capture/compare 1 signal	11, 15, 25, 29, 39, 48, 51, 53, 57, 9	15, 19, 31, 33, 37, 44, 5	15, 19, 31, 33, 37, 44, 5	15, 20, 22, 28	15, 20	12, 14, 20	12, 15, 17
TIMA1_C0N	O	TIMA1 capture/compare 0 complementary output	23, 52, 54, 58, 8	16, 20, 30, 42	16, 20, 30, 42	12, 19	25		14, 22
TIMA1_C1N	O	TIMA1 capture/compare 1 complementary output	19, 53, 55, 59, 9	17, 21, 31, 41	17, 21, 31, 41	13, 20	13	10, 12	10, 15
TIMA_FAL0	I	TIMA fault input 0	22, 27, 30, 35, 42, 46, 54, 57	12, 16, 19, 3, 46, 8	12, 16, 19, 3, 46, 8	10, 12, 15, 30, 6	11, 15, 28, 8	22, 5, 8	12, 25, 5, 9
TIMA_FAL1	I	TIMA fault input 1	19, 27, 33, 42, 45, 56, 64	1, 11, 18, 41, 8	1, 11, 18, 41, 8	1, 14, 6, 9	14, 18, 3, 8	11, 24, 5, 9	11, 28, 5, 8
TIMA_FAL2	I	TIMA fault input 2	27, 31, 34, 54, 58	16, 2, 20, 47	16, 2, 20, 47	12, 2, 31	1, 4	1	1, 26
TIMG8_IDX	I	TIMG8 quadrature encoder index pulse signal	16, 2, 34, 49, 8	13, 2, 24, 30, 38	13, 2, 24, 30, 38	11, 19, 2	12, 4	1	1, 14
TIMG0_C0	IO	TIMG0 capture/compare 0 signal	12, 14, 24, 33, 45, 47, 5, 52, 56, 62	1, 11, 18, 27, 34, 36, 43	1, 11, 18, 27, 34, 36, 43	1, 14, 16, 23, 27, 9	14, 16, 21, 26, 3	11, 15, 19, 24, 9	11, 18, 23, 28, 8
TIMG0_C1	IO	TIMG0 capture/compare 1 signal	13, 15, 25, 34, 46, 48, 53, 57, 6, 63	12, 19, 2, 28, 35, 37, 44	12, 19, 2, 28, 35, 37, 44	10, 15, 17, 2, 24, 28	11, 15, 17, 22, 4	1, 16, 20, 8	1, 12, 19, 9
TIMG1_C0	IO	TIMG1 capture/compare 0 signal	24, 36, 50, 64	14, 43	14, 43	27	18, 26	19	23
TIMG1_C1	IO	TIMG1 capture/compare 1 signal	1, 26, 37, 51	15, 45	15, 45	29	19, 27	21	24
TIMG8_C0	IO	TIMG8 capture/compare 0 signal	10, 17, 20, 24, 3, 30, 34, 36, 43, 45, 49, 58, 62	11, 13, 2, 20, 25, 32, 39, 43, 46, 9	11, 13, 2, 20, 25, 32, 39, 43, 46, 9	11, 2, 21, 25, 27, 30, 7, 9	12, 16, 23, 26, 28, 4, 9	1, 13, 17, 19, 22, 6, 9	1, 16, 20, 23, 25, 6, 8

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Table 6-12. Timer (TIMx) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	PM PIN	PT PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	RUY PIN
TIMG8_C1	IO	TIMG8 capture/compare 1 signal	11, 16, 18, 21, 25, 31, 33, 37, 4, 42, 44, 46, 59, 63	1, 10, 12, 21, 26, 33, 38, 40, 44, 47, 8	1, 10, 12, 21, 26, 33, 38, 40, 44, 47, 8	1, 10, 22, 26, 28, 31, 6, 8	1, 10, 11, 17, 20, 24, 3, 8	14, 18, 20, 24, 5, 7, 8	17, 21, 26, 28, 5, 7, 9

Table 6-13. Unified Communication Module (UniComm) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PM PIN	PT PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	RUY PIN
UC0_CTS	IO	Unified Communication Module UC0: UART CTS signal	16, 17, 26, 37, 43, 5, 50, 58, 9	14, 20, 27, 31, 38, 39, 45, 9	14, 20, 27, 31, 38, 39, 45, 9	16, 20, 25, 29, 7	23, 27, 9	12, 17, 21, 6	15, 20, 24, 6
UC0_RTS	IO	Unified Communication Module UC0: UART RTS signal	19, 23, 30, 36, 44, 51, 59, 8	10, 15, 21, 30, 41, 42, 46	10, 15, 21, 30, 41, 42, 46	19, 30, 8	10, 25, 28	22, 7	14, 22, 25, 7
UC0_SCL_RX	IOD	Unified Communication Module UC0: I2C SCL or UART RX signal	14, 15, 18, 20, 25, 34, 39, 4, 47, 51, 55, 57, 7	15, 17, 19, 2, 26, 29, 36, 37, 40, 44, 5	15, 17, 19, 2, 26, 29, 36, 37, 40, 44, 5	13, 15, 18, 2, 26, 28	13, 15, 24, 4	1, 10, 18, 20	1, 10, 12, 13, 21
UC0_SDA_TX	IOD	Unified Communication Module UC0: I2C SDA or UART TX signal	14, 15, 17, 19, 21, 24, 3, 33, 35, 48, 50, 54, 56, 6	1, 14, 16, 18, 25, 28, 3, 36, 37, 39, 41, 43	1, 14, 16, 18, 25, 28, 3, 36, 37, 39, 41, 43	1, 12, 14, 17, 25, 27	14, 23, 26, 3	11, 17, 19, 24	11, 20, 23, 28
UC2_PICO	IO	Unified Communication Module UC2: SPI PICO signal	14, 45, 50, 55, 7	11, 14, 17, 29, 36	11, 14, 17, 29, 36	13, 18, 9	13	10, 9	10, 13, 8
UC2_POCI	IO	Unified Communication Module UC2: SPI POCI signal	16, 44, 49, 56, 6	10, 13, 18, 28, 38	10, 13, 18, 28, 38	11, 14, 17, 8	10, 12, 14	11, 7	11, 7
UC2_SCLK	IOD	Unified Communication Module UC2: SPI SCLK signal	15, 46, 5, 51, 57	12, 15, 19, 27, 37	12, 15, 19, 27, 37	10, 15, 16	11, 15	8	12, 9
UC4_PICO_TX	IO	Unified Communication Module UC4: SPI PICO or UART TX signal	11, 21, 3, 33, 35, 47, 56, 60	1, 18, 22, 25, 3, 33	1, 18, 22, 25, 3, 33	1, 14, 22	14, 20, 3	11, 14, 24	11, 17, 28
UC4_POCI_RTS	IO	Unified Communication Module UC4: SPI POCI or UART RTS signal	12, 2, 20, 28, 37, 46, 54, 59, 8, 9	12, 16, 21, 24, 30, 31, 34	12, 16, 21, 24, 30, 31, 34	10, 12, 19, 20, 23	11, 21	12, 15, 8	14, 15, 18, 9
UC4_SCLK_RX	IOD	Unified Communication Module UC4: SPI SCLK or UART RX signal	10, 13, 22, 34, 39, 4, 48, 57, 61	19, 2, 23, 26, 32, 35, 5	19, 2, 23, 26, 32, 35, 5	15, 2, 21, 24	15, 22, 4	1, 13, 16	1, 12, 16, 19

Table 6-13. Unified Communication Module (UniComm) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	PM PIN	PT PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	RUY PIN
UC5_SCL_RX	IOD	Unified Communication Module UC5: I2C SCL or UART RX signal	10, 11, 13, 21, 36, 44, 46, 50, 53, 55, 57, 59, 8	10, 12, 14, 17, 19, 21, 30, 32, 33, 35	10, 12, 14, 17, 19, 21, 30, 32, 33, 35	10, 13, 15, 19, 21, 22, 24, 8	10, 11, 13, 15, 20, 22	10, 13, 14, 16, 7, 8	10, 12, 14, 16, 17, 19, 7, 9
UC5_SDA_TX	IOD	Unified Communication Module UC5: I2C SDA or UART TX signal	10, 11, 12, 20, 37, 43, 45, 51, 52, 54, 56, 58, 9	11, 15, 16, 18, 20, 31, 32, 33, 34, 9	11, 15, 16, 18, 20, 31, 32, 33, 34, 9	12, 14, 20, 21, 22, 23, 7, 9	14, 20, 21, 9	11, 12, 13, 14, 15, 6, 9	11, 15, 16, 17, 18, 6, 8
UC9_RX	IO	Unified Communication Module UC9: UART RX signal	1, 26, 30, 31, 51, 6	15, 28, 45, 46, 47	15, 28, 45, 46, 47	17, 29, 30, 31	1, 19, 27, 28	21, 22	24, 25, 26
UC9_TX	IO	Unified Communication Module UC9: UART TX signal	26, 30, 50, 64, 7	14, 29, 45, 46	14, 29, 45, 46	18, 29, 30	18, 27, 28	21, 22	13, 24, 25
UC2_CS0	IO	Unified Communication Module UC2: SPI CS0 signal	11, 27, 42, 44, 54	10, 16, 33, 8	10, 16, 33, 8	12, 22, 6, 8	10, 20, 8	14, 5, 7	17, 5, 7
UC2_CS1	IO	Unified Communication Module UC2: SPI CS1 signal	10, 23, 28, 43, 5, 58	20, 27, 32, 42, 9	20, 27, 32, 42, 9	16, 21, 7	25, 9	13, 6	16, 22, 6
UC2_CS2	IO	Unified Communication Module UC2: SPI CS2 signal	18, 19, 25, 37, 48, 49, 59, 7	13, 21, 29, 40, 41, 44	13, 21, 29, 40, 41, 44	11, 18, 26, 28	12, 24	18, 20	13, 21
UC2_CS3	IO	Unified Communication Module UC2: SPI CS3 signal	17, 2, 23, 24, 34, 36, 39, 43, 47, 54, 6	16, 2, 24, 28, 39, 42, 43, 5, 9	16, 2, 24, 28, 39, 42, 43, 5, 9	12, 17, 2, 25, 27, 7	23, 25, 26, 4, 9	1, 17, 19, 6	1, 20, 22, 23, 6
UC4_CS0_CTS	IO	Unified Communication Module UC4: SPI CS0 or UART CTS signal	1, 16, 19, 27, 30, 36, 42, 45, 55, 58, 6, 7	11, 17, 20, 28, 29, 38, 41, 46, 8	11, 17, 20, 28, 29, 38, 41, 46, 8	13, 17, 18, 30, 6, 9	13, 19, 28, 8	10, 22, 5, 9	10, 13, 25, 5, 8

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6.4 Connections for Unused Pins

Table 6-14 lists the correct termination of unused pins.

Table 6-14. Connection of Unused Pins

PIN (1)	POTENTIAL	COMMENT
PAx, PBx	Open	Set corresponding pin functions to GPIO (PINCMx.PF = 0x1) and configure unused pins to output low or input with internal pullup/ pulldown resistor.
NRST	VCC	NRST is an active-low reset signal; it must be pulled high to VCC or the device will not start, for more information refer to Section 9.1

(1) Any unused pin with a function that is shared with general-purpose I/O should follow the "PAx and PBx" unused pin connection guidelines.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

			MIN	MAX	UNIT
VDD	Supply voltage	At VDD pin	–0.3	4.1	V
V_I	Input voltage	Applied to any 5-V tolerant open-drain pins	–0.3	5.5	V
V_I	Input voltage	Applied to any common tolerance pins	–0.3	V_{DD} + 0.3 (4.1 MAX)	V
I_{VDD}	Current into VDD pin (source)	-40°C ≤ Tj ≤ 130°C, VDD>=2.7V		80	mA
	Current into VDD pin (source)	-40°C ≤ Tj ≤ 85°C, VDD>=2.7V		100	mA
I_{VSS}	Current out of VSS pin (sink)	-40°C ≤ Tj ≤ 130°C, VDD>=2.7V		80	mA
	Current out of VSS pin (sink)	-40°C ≤ Tj ≤ 85°C, VDD>=2.7V		100	mA
I_{IO}	Current of SDIO pin	Current sunk or sourced by SDIO pin, VDD>=2.7V		6	mA
	Current of HS_IO pin	Current sunk or sourced by HSIO pin, VDD>=2.7V		6	mA
	Current of HDIO pin	Current sunk or sourced by HDIO pin		20	mA
	Current of ODIO pin	Current sunk by ODIO pin		20	mA
I_D	Supported diode current	Diode current at any device pin (excluding Open Drain IO)	-2	2	mA
T_A	Ambient temperature	Ambient temperature	-40	125	°C
T_J	Junction temperature	Junction temperature	-40	130	°C
T_{stg}	Storage temperature	Storage temperature	–40	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins	±500	V

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Supply voltage	1.62		3.6	V
VCORE	Voltage on VCORE pin [(2)]		1.35		V
C_{VDD}	Capacitor connected between VDD and VSS [(1)]		10		uF
C_{VCORE}	Capacitor connected between VCORE and VSS [(1)] [(2)]		470		nF
T_A	Ambient temperature	–40		125	°C
T_J	Max junction temperature			130	°C
f_{MCLK} (PD1 bus clock)	MCLK, CPUCLK frequency with 2 flash wait states [(3)]			80	MHz
	MCLK, CPUCLK frequency with 1 flash wait state [(3)]			48	MHz
	MCLK, CPUCLK frequency with 0 flash wait states [(3)]			24	MHz

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over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$f_{ULPCLK\ (PD0\ bus\ clock)}$	ULPCLK frequency			40	MHz

(1) Connect C_{VDD} and C_{VCORE} between VDD/VSS and VCORE/VSS, respectively, as close to the device pins as possible. A low-ESR capacitor with at least the specified value and tolerance of ±20% or better is required for C_{VDD} and C_{VCORE}.
(2) The VCORE pin must only be connected to C_{VCORE}. Do not supply any voltage or apply any external load to the VCORE pin.
(3) Wait states are managed automatically by the system controller (SYSCTL) and do not need to be configured by application software unless MCLK is sourced from a high speed clock source (HSCLK sourced from HFCLK or SYSPLL).

7.4 Thermal Information

THERMAL METRIC[(1)]		PACKAGE	VALUE	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	LQFP-64 (PM)	62	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		25.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		45.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		1.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		44.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		N/A	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	LQFP-48 (PT)	76.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		31.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		48.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		2.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		48.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		N/A	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	VQFN-48 (RGZ)	29.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		20.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		12.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		0.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		12.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		4.8	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	VQFN-32 (RHB)	34.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		25.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		14.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		0.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		14.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		4.8	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	WQFN-28 (RUY)	42.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		29.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		18.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		0.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		18.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		4.8	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	VSSOP-28 (DGS28)	75.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		34.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		37.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		2.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		36.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		N/A	°C/W

THERMAL METRIC[(1)]		PACKAGE	VALUE	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	VQFN-24 (RGE)	42.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		33.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		19.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		0.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		19.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		5.0	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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7.5 Supply Current Characteristics

7.5.1 RUN/SLEEP Modes

VDD=3.3V. All inputs tied to 0V or VDD. Outputs do not source or sink any current. All peripherals are disabled.

PARAMETER		MCLK	-40°C		25°C		85°C		105°C		125°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
RUN Mode													
IDD_{RUN}	MCLK=SYSPLL, SYSPLLREF=SYSOSC, CoreMark, execute from flash	80MHz	8.3		8.3		8.3		8.4		8.6		mA
		48MHz	5.4		5.4		5.5		5.5		5.7		
	MCLK=SYSOSC, CoreMark, execute from flash	32MHz	4.0		4.0		4.0		4.0		4.3		
		4MHz	0.8		0.8		0.8		0.9		1.1		
	MCLK=SYSPLL, SYSPLLREF=SYSOSC, CoreMark, execute from SRAM	80MHz	7.3		7.3		7.4		7.4		7.6		
		48MHz	4.8		4.8		4.9		4.9		5.1		
	MCLK=SYSOSC, CoreMark, execute from SRAM	32MHz	3.3		3.4		3.4		3.5		3.6		
		4MHz	0.7		0.7		0.8		0.8		1.0		
IDD_{RUN}, per MHz	MCLK=SYSPLL, SYSPLLREF=SYSOSC, CoreMark, execute from flash	80MHz	103		104		104		105		107		uA/MHz
	MCLK=SYSPLL, SYSPLLREF=SYSOSC, While(1), execute from flash	80MHz	54	TBD	54	TBD	55	TBD	55	TBD	58	TBD	
SLEEP Mode													
IDD_{SLEEP}	MCLK=SYSPLL, SYSPLLREF=SYSOSC, CPU is halted	80MHz	2891	TBD	2967	TBD	3256	TBD	3590	TBD	4353	TBD	uA
		48MHz	2160	TBD	2228	TBD	2516	TBD	2854	TBD	3607	TBD	
	MCLK=SYSOSC, CPU is halted	32MHz	1686	TBD	1747	TBD	2029	TBD	2368	TBD	3127	TBD	
		4MHz	562	TBD	614	TBD	893	TBD	1232	TBD	1981	TBD	
IDD_{SLEEP}	MCLK=SYSPLL, SYSPLLREF=SYSOSC, CPU is halted	80MHz	37		38		42		46		56		uA/MHz

7.5.2 STOP/STANDBY Modes

VDD=3.3V. All inputs tied to 0V or VDD. Outputs do not source or sink any current. All peripherals not noted are disabled.

PARAMETER		ULPCLK	-40°C		25°C		85°C		105°C		125°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
STOP Mode													
IDD_{STOP0}	SYSOSC=32MHz, USE4MHZSTOP=0, DISABLESTOP=0	4MHz	400	TBD	404	TBD	406	TBD	409	TBD	416	TBD	uA
IDD_{STOP1}	SYSOSC=4MHz, USE4MHZSTOP=1, DISABLESTOP=0		202	TBD	207	TBD	406	TBD	409	TBD	417	TBD	
IDD_{STOP2}	SYSOSC off, DISABLESTOP=1, ULPCLK=LFCLK	32kHz	53	TBD	56	TBD	58	TBD	60	TBD	69	TBD	
STANDBY Mode													

VDD=3.3V. All inputs tied to 0V or VDD. Outputs do not source or sink any current. All peripherals not noted are disabled.

PARAMETER		ULPCLK	-40°C		25°C		85°C		105°C		125°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
IDD_{STBY0}	LFCLK=LFXT, STOPCLKSTBY=0, RTC enabled	32kHz	1.8	TBD	2.0	TBD	3.6	TBD	6.4	TBD	15	TBD	uA
IDD_{STBY1}	LFCLK=LFOSC, STOPCLKSTBY=1, RTC enabled		1.8	TBD	2.0	TBD	3.6	TBD	6.4	TBD	15	TBD	
	LFCLK=LFXT, STOPCLKSTBY=1, RTC enabled		1.3	TBD	1.4	TBD	3.1	TBD	6.0	TBD	15	TBD	
	LFCLK=LFXT, STOPCLKSTBY=1, GPIOA enabled		1.3	TBD	1.4	TBD	3.1	TBD	6.0	TBD	15	TBD	

7.5.3 SHUTDOWN Mode

All inputs tied to 0V or VDD. Outputs do not source or sink any current. Core regulator is powered down.

PARAMETER		VDD	-40°C		25°C		85°C		105°C		125°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
IDD_{SHDN}	Supply current in SHUTDOWN mode	3.3V	60		69		336		786		2210		nA

7.6 Power Supply Sequencing

7.6.1 Power Supply Ramp

Figure 7-1 gives the relationship of POR- POR+, BOR0-, and BOR0+ during power-up and power-down.

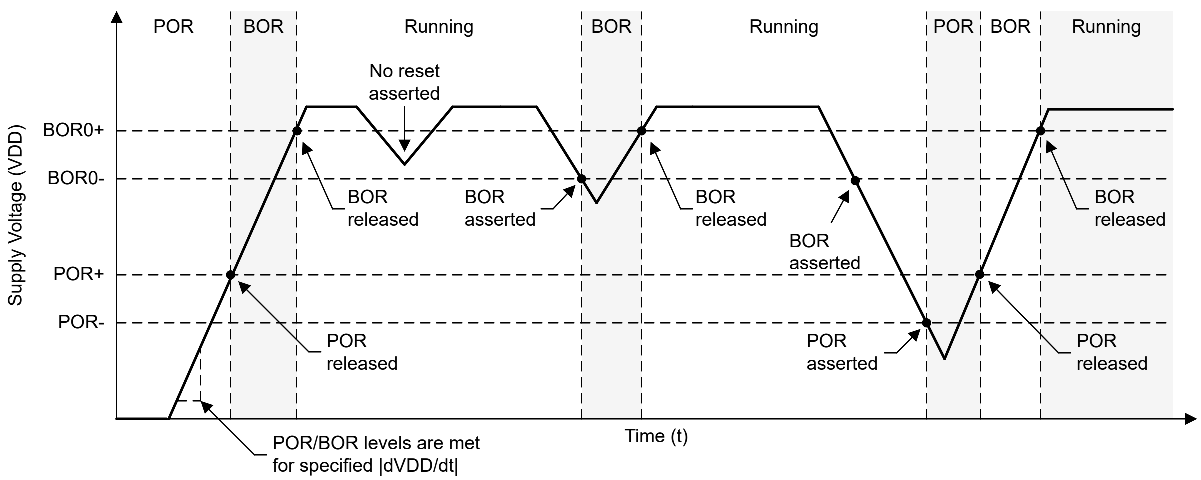

Figure 7-1. Power Cycle POR/BOR Conditions - VDD

7.6.2 POR and BOR

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
dVDD/dt	VDD (supply voltage) slew rate	Rising			0.1	V/us
		Falling [(1)]			0.01	V/us
		Falling, STANDBY			0.1	V/ms
V_{POR+}	Power-on reset voltage level	Rising	0.95	1.30	1.59	V
V_{POR-}		Falling	0.9	1.25	1.54	V
$V_{HYS, POR}$	POR hysteresis		30	58	74	mV

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over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{BOR0+, COLD}$	Brown-out reset voltage level 0 (default level)	Cold start, rising	1.40	1.48	1.61	V
V_{BOR0+}		Rising (1)	1.56	1.59	1.62	
V_{BOR0-}		Falling (1)	1.55	1.58	1.61	
$V_{BOR0, STBY}$		STANDBY mode	1.51	1.56	1.61	
V_{BOR1+}	Brown-out-reset voltage level 1	Rising (1)	2.13	2.17	2.21	V
V_{BOR1-}		Falling (1)	2.10	2.14	2.18	
$V_{BOR1, STBY}$		STANDBY mode	2.06	2.13	2.20	
V_{BOR2+}	Brown-out-reset voltage level 2	Rising (1)	2.73	2.77	2.82	V
V_{BOR2-}		Falling (1)	2.7	2.74	2.79	
$V_{BOR2, STBY}$		STANDBY mode	2.62	2.71	2.8	
V_{BOR3+}	Brown-out-reset voltage level 3	Rising (1)	2.88	2.96	3.04	V
V_{BOR3-}		Falling (1)	2.85	2.93	3.01	
$V_{BOR3, STBY}$		STANDBY mode	2.82	2.92	3.02	
$V_{HYS,BOR}$	Brown-out reset hysteresis	Level 0		15	21	mV
		Levels 1-3		34	40	
$T_{PD, BOR}$	BOR propagation delay	RUN/SLEEP/STOP mode			5	us
		STANDBY mode			100	us

(1) Device operating in RUN, SLEEP, or STOP mode.

7.7 Flash Memory Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply						
$VDD_{PGM/ERASE}$	Program and erase supply voltage		1.62		3.6	V
IDD_{ERASE}	Supply current from VDD during erase operation	Supply current delta			10	mA
IDD_{PGM}	Supply current from VDD during program operation	Supply current delta			10	mA
Endurance						
NWEC(HI_ENDURANCE)	Erase/program cycle endurance for chosen 32 sectors of flash (1)		100			k cycles
NWEC (NORMAL_ENDURANCE)	Erase/program cycle endurance (Flash not used for HI_ENDURANCE) (1)		10			k cycles
$NE_{(MAX)}$	Total erase operations before failure (2)		802			k erase operations
$NW_{(MAX)}$	Write operations per word line before sector erase (3)				83	write operations
Retention						
t_{RET_85}	Flash memory data retention	-40°C <= Tj <= 85°C	60			years
t_{RET_105}	Flash memory data retention	-40°C <= Tj <= 105°C	11.4			years
Program and Erase Timing						
$t_{PROG (WORD, 64)}$	Program time for flash word (4) (6)			50	275	µs
$t_{PROG (SEC, 64)}$	Program time for 1kB sector (5) (6)			6.4		ms
$t_{ERASE (SEC)}$	Sector erase time	≤2k erase/program cycles, T_j≥25°C		4	20	ms

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{ERASE\ (SEC)}$	Sector erase time	≤10k erase/program cycles, T_j≥25°C		20	150	ms
$t_{ERASE\ (SEC)}$	Sector erase time	<10k erase/program cycles		20	200	ms
$t_{ERASE\ (BANK)}$	Bank erase time	<10k erase/program cycles		22	220	ms

(1) Up to 32 application-chosen sectors from the main flash bank(s) or data bank can be used as high endurance sectors. This enables applications that frequently update flash data such as EEPROM emulation.
(2) Total number of cumulative erase operations supported by the flash before failure. A sector erase or bank erase operation is considered to be one erase operation.
(3) Maximum number of write operations allowed per word line before the word line must be erased. If additional writes to the same word line are required, a sector erase is required once the maximum number of write operations per word line is reached.
(4) Program time is defined as the time from when the program command is triggered until the command completion interrupt flag is set in the flash controller.
(5) Sector program time is defined as the time from when the first word program command is triggered until the final word program command completes and the interrupt flag is set in the flash controller. This time includes the time needed for software to load each flash word (after the first flash word) into the flash controller during programming of the sector.
(6) Flash word size is 64 data bits (8 bytes). On devices with ECC, the total flash word size is 72 bits (64 data bits plus 8 ECC bits).

7.8 Timing Characteristics

VDD=3.3V, T_a=25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Wakeup Timing						
$t_{WAKE,\ SLEEP0}$	Wakeup time from SLEEP0 to RUN (1)			1.4		us
$t_{WAKE,\ SLEEP1}$	Wakeup time from SLEEP1 to RUN (1)			1.6		us
$t_{WAKE,\ SLEEP2}$	Wakeup time from SLEEP2 to RUN (1)			2.2		us
$t_{WAKE,\ STANDBY0}$	Wakeup time from STANDBY0 to RUN (1)			11.4		us
$t_{WAKE,\ STANDBY1}$	Wakeup time from STANDBY1 to RUN (1)			11.4		us
$t_{WAKE,\ STOP0}$	Wakeup time from STOP0 to RUN (SYSOSC enabled) (1)			10		us
$t_{WAKE,\ STOP1}$	Wakeup time from STOP1 to RUN (SYSOSC enabled) (1)			10		us
$t_{WAKE,\ STOP2}$	Wakeup time from STOP2 to RUN (SYSOSC disabled) (1)			10		
$t_{WAKEUP,\ SHDN}$	Wakeup time from SHUTDOWN to RUN (2)	Fast boot enabled		306		us
		Fast boot disabled		345		
Asynchronous Fast Clock Request Timing						
$t_{DELAY,\ SLEEP1}$	Delay time from edge of asynchronous request to first 32MHz MCLK edge	Mode is SLEEP1		0.34		us
$t_{DELAY,\ SLEEP2}$	Delay time from edge of asynchronous request to first 32MHz MCLK edge	Mode is SLEEP2		0.94		us
$t_{DELAY,\ STANDBY0}$	Delay time from edge of asynchronous request to first 32MHz MCLK edge	Mode is STANDBY0		3		us
$t_{DELAY,\ STANDBY1}$	Delay time from edge of asynchronous request to first 32MHz MCLK edge	Mode is STANDBY1		3.1		us
$t_{DELAY,\ STOP0}$	Delay time from edge of asynchronous request to first 32MHz MCLK edge	Mode is STOP0		0.1		us
$t_{DELAY,\ STOP1}$	Delay time from edge of asynchronous request to first 32MHz MCLK edge	Mode is STOP1		2.4		us

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VDD=3.3V, T_a=25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{DELAY, STOP2}$	Delay time from edge of asynchronous request to first 32MHz MCLK edge	Mode is STOP2		0.9		us
Startup Timing						
$t_{START, RESET}$	Device cold startup time from reset/ power-up (3)	Fast boot enabled		300		us
		Fast boot disabled		350		
NRST Timing						
$t_{RST, BOOTRST}$	Pulse length on NRST pin to generate BOOTRST	ULPCLK≥4MHz		1.5		us
		ULPCLK=32kHz		29		
$t_{RST, POR}$	Pulse length on NRST pin to generate POR			1		s

(1) The wake-up time is measured from the edge of an external wake-up signal (GPIO wake-up event) to the time that the first instruction of the user program is executed, with glitch filter disabled (FILTEREN=0x0) and fast wake enabled (FASTWAKEONLY=1) .
(2) The wake-up time is measured from the edge of an external wake-up signal (IOMUX wake-up event) to the time that first instruction of the user program is executed.
(3) The start-up time is measured from the time that VDD crosses VBOR0- (cold start-up) to the time that the first instruction of the user program is executed.

7.9 Clock Specifications

7.9.1 System Oscillator (SYSOSC)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SYSOSC}	Factory trimmed SYSOSC frequency	SYSOSCCFG.FREQ=00 (BASE)		32		MHz
		SYSOSCCFG.FREQ=01		4		
	User trimmed SYSOSC frequency	SYSOSCCFG.FREQ=10, SYSOSCTRIMUSER.FREQ=10		24		
		SYSOSCCFG.FREQ=10, SYSOSCTRIMUSER.FREQ=01		16		
f_{SYSOSC}	SYSOSC frequency accuracy when frequency correction loop (FCL) is enabled and an ideal ROSC resistor is assumed (1) (2)	SETUSEFCL=1, T_a = 25 ℃	-0.60		0.68	%
		SETUSEFCL=1, -40 ℃ ≤ T_a ≤ 85 ℃	-0.80		0.93	
		SETUSEFCL=1, -40 ℃ ≤ T_a ≤ 105 ℃	-0.80		1.1	
		SETUSEFCL=1, -40 ℃ ≤ T_a ≤ 125 ℃	-0.80		1.3	
f_{SYSOSC}	SYSOSC accuracy when frequency correction loop (FCL) is enabled with R_{OSC} resistor put at R_{OSC} pin, for factory trimmed frequencies(1) (5) (6)	SETUSEFCL=1, T_a = 25 ℃, ±0.1% ±25ppm R_{OSC}	-0.7		0.78	%
		SETUSEFCL=1, -40 ℃ ≤ T_a ≤ 85 ℃, ±0.1% ±25ppm R_{OSC}	-1.1		1.2	
		SETUSEFCL=1, -40 ℃ ≤ T_a ≤ 105 ℃, ±0.1% ±25ppm R_{OSC}	-1.1		1.4	
		SETUSEFCL=1, -40 ℃ ≤ T_a ≤ 125 ℃, ±0.1% ±25ppm R_{OSC}	-1.1		1.7	
f_{SYSOSC}	SYSOSC frequency accuracy when frequency correction loop (FCL) is enabled when the internal ROSC resistor is used, 32MHz(4) (5) (6)	SETUSEFCL=1, T_a = 25 ℃	0		1	%
		SETUSEFCL=1, -40 ℃ ≤ T_a ≤ 125 ℃	-2.1		1.6	
f_{SYSOSC}	SYSOSC frequency accuracy when frequency correction loop (FCL) is enabled when the internal ROSC resistor is used, 4MHz(4) (5) (6)	SETUSEFCL=1, T_a = 25 ℃	0		1.6	%
		SETUSEFCL=1, -40 ℃ ≤ T_a ≤ 125 ℃	-2.3		1.8	
f_{SYSOSC}	SYSOSC accuracy when frequency correction loop (FCL) is disabled, 32MHz(5) (6)	SETUSEFCL=0, SYSOSCCFG.FREQ=00, -40 ℃ ≤ T_a ≤ 125 ℃	-2.6		1.8	%

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SYSOSC}	SYSOSC accuracy when frequency correction loop (FCL) is disabled, for factory trimmed frequencies, 4MHz[5] [6]	SETUSEFCL=0, SYSOSCCFG.FREQ=01, -40 ℃ ≤ T_a ≤ 125 ℃	-2.8		2.1	%
R_{OSC}	External resistor put between ROSC pin and VSS [1]	SETUSEFCL=1		100		kΩ
$t_{settle, SYSOSC}$	Settling time to target accuracy [3]	SETUSEFCL=1, ±0.1% 25ppm R_{OSC} [1]			40	us

(1) The SYSOSC frequency correction loop (FCL) enables high SYSOSC accuracy via an external reference resistor (R_{OSC}) which must be connected between the device ROSC pin and VSS when using the FCL. Accuracies are shown for a ±0.1% ±25ppm R_{OSC}; relaxed tolerance resistors may also be used (with reduced SYSOSC accuracy). See the SYSOSC section of the technical reference manual for details on computing SYSOSC accuracy for various R_{OSC} accuracies. R_{OSC} does not need to be populated if the FCL is not enabled.
(2) Represents the device accuracy only. The tolerance and temperature drift of the ROSC resistor used must be combined with this spec to determine final accuracy. Performance for a ±0.1% ±25ppm R_{OSC} is given as a reference point.
(3) When SYSOSC is waking up (for example, when exiting a low power mode) and FCL is enabled, the SYSOSC will initially undershoot the target frequency f_{SYSOSC} by an additional error of up to $f_{settle,SYSOSC}$ for the time $t_{settle,SYSOSC}$, after which the target accuracy is achieved.
(4) The SYSOSC frequency correction loop (FCL) enables high SYSOSC accuracy via an internal reference resistor when using the FCL. See the SYSOSC section of the technical reference manual for details on computing SYSOSC accuracy.
(5) SYSOSC Accuracy is measured in the default power-up state, with MCLK = SYSOSC, the CPU is running a while(1) loop, and the SYSPLL is disabled.
(6) SYSOSC is measured with the internal FCC counter using an external 1ms pulse as the measurement trigger.

7.9.2 Low Frequency Oscillator (LFOSC)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{LFOSC}	LFOSC frequency			32768		Hz
	LFOSC accuracy	-40 ℃ ≤ T_a ≤ 125 ℃	–5		5	%
		-40 ℃ ≤ T_a ≤ 85 ℃	–3		3	%
I_{LFOSC}	LFOSC current consumption			300		nA
$t_{start, LFOSC}$	LFOSC start-up time			1		ms

7.9.3 System Phase Lock Loop (SYSPLL)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{SYSPLLREF}$	SYSPLL reference frequency range [2]		4		48	MHz
f_{VCO}	VCO output frequency		100		400	MHz
f_{SYSPLL}	SYSPLL output frequency range [1]	SYSPLLCLK0, SYSPLLCLK1	2.5		200	MHz
		SYSPLLCLK2X [3]	10		400	
DC_{PLL}	SYSPLL output duty cycle	$f_{SYSPLLREF}$=32MHz, f_{VCO}=160MHz	45		55	%
$Jitter_{SYSPLL}$	SYSPLL RMS cycle-to-cycle jitter	$f_{SYSPLLREF}$=32MHz, f_{VCO}=160MHz		60		ps
	SYSPLL RMS period jitter			45		
I_{SYSPLL}	SYSPLL current consumption	$f_{SYSPLLREF}$=32MHz, f_{VCO}=160MHz		322		uA
$t_{start, SYSPLL}$	SYSPLL start-up time	$f_{SYSPLLREF}$=32MHz, PDIV=3, QDIV=39, f_{VCO}=160MHz, ±0.5% accuracy		14	24	us

(1) The SYSPLL may support higher output frequencies than the device clock system supports. Ensure that the device maximum frequency specifications are not violated when configuring the SYSPLL output frequencies.
(2) Please refer to SYSPLL tuning parameters in Table 2-6 inside the _:AMP:_
(3) Limit f_{VCO} to 200MHz maximum when using SYSPLL2X

7.9.4 Low Frequency Crystal/Clock

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Low frequency crystal oscillator (LFXT)						
f_{LFXT}	LFXT frequency			32768		Hz
DC_{LFXT}	LFXT duty cycle		30		70	%
OA_{LFXT}	LFXT crystal oscillation allowance			419		kΩ
$C_{L, eff}$	Integrated effective load capacitance[1]			1		pF
$t_{start, LFXT}$	LFXT start-up time			200		ms
I_{LFXT}	LFXT current consumption	XT1DRIVE=0, LOWCAP=1 [4]		200		nA
Low frequency digital clock input (LFCLK_IN)						
f_{LFIN}	LFCLK_IN frequency [2]	SETUSEEXLF=1	29491	32768	36045	Hz
DC_{LFIN}	LFCLK_IN duty cycle [2]	SETUSEEXLF=1	40		60	%
LFCLK Monitor						
$f_{FAULTLF}$	LFCLK monitor fault frequency [3]	MONITOR=1	2800	4200	8400	Hz

(1) This includes parasitic bond and package capacitance (≈2pF per pin), calculated as $C_{LFXIN} \times C_{LFXOUT} / (C_{LFXIN} + C_{LFXOUT})$, where C_{LFXIN} and C_{LFXOUT} are the total capacitance at LFXIN and LFXOUT, respectively.
(2) The digital clock input (LFCLK_IN) accepts a logic level square wave clock.
(3) The LFCLK monitor may be used to monitor the LFXT or LFCLK_IN. It will always fault below the MIN fault frequency, and will never fault above the MAX fault frequency.
(4) When using LFXT, the user must ensure that the crystal is properly rated to support the start-up drive load (e.g. 0.1uW)

7.9.5 High Frequency Crystal/Clock

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
High frequency crystal oscillator (HFXT)						
f_{HFXT}	HFXT frequency	HFXTRSEL=00	4		8	MHz
		HFXTRSEL=01	8.01		16	
		HFXTRSEL=10	16.01		32	
		HFXTRSEL=11	32.01		48	
DC_{HFXT}	HFXT duty cycle	HFXTRSEL=00	40		65	%
		HFXTRSEL=01	40		60	
		HFXTRSEL=10	40		60	
		HFXTRSEL=11	40		60	
OA_{HFXT}	HFXT crystal oscillation allowance	HFXTRSEL=00 (4 to 8MHz range)		2		kΩ
$C_{L, eff}$	Integrated effective load capacitance[1]			1		pF
$t_{start, HFXT}$	HFXT start-up time [2]	HFXTRSEL=11, 32MHz crystal		0.5		ms
I_{HFXT}	HFXT current consumption[2]	f_{HFXT}=4MHz, R_m=300Ω, C_L=12pF		100		uA
		f_{HFXT}=48MHz, R_m=30Ω, C_L=12pF, C_m=6.26fF, L_m=1.76mH		600		
High frequency digital clock input (HFCLK_IN)						
f_{HFIN}	HFCLK_IN frequency [3]	USEEXTHFCLK=1	4		48	MHz
DC_{HFIN}	HFCLK_IN duty cycle [3]	USEEXTHFCLK=1	40		60	%

(1) This includes parasitic bond and package capacitance (≈2pF per pin), calculated as $C_{HFXIN} \times C_{HFXOUT} / (C_{HFXIN} + C_{HFXOUT})$, where C_{HFXIN} and C_{HFXOUT} are the total capacitance at HFXIN and HFXOUT, respectively.
(2) The HFXT startup time ($t_{start, HFXT}$) is measured from the time the HFXT is enabled until stable oscillation for a typical crystal. Start-up time is dependent upon crystal frequency and crystal specifications. Refer to the HFXT section of the MSPM0 G-Series 80-MHz Microcontrollers Technical Reference Manual.Current consumption increases with higher RSEL and start up time is decreases with higher RSEL.

(3) The digital clock input (HFCLK_IN) accepts a logic level square wave clock.

7.10 Digital IO

7.10.1 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IH}	High level input voltage	ODIO [1]	VDD≥1.62V	0.7*VDD		5.5	V
			VDD≥2.7V	2		5.5	V
		All I/O except ODIO & Reset	VDD≥1.62V	0.7*VDD		VDD+0.3	V
V_{IL}	Low level input voltage	ODIO	VDD≥1.62V	-0.3		0.3*VDD	V
			VDD≥2.7V	-0.3		0.8	V
		All I/O except ODIO & Reset	VDD≥1.62V	-0.3		0.3*VDD	V
V_{HYS}	Hysteresis	ODIO		0.05*VDD			V
		All I/O except ODIO		0.1*VDD			V
I_{lkg}	High-Z leakage current (All packages except PM)	SDIO[2] [3]	1.62V ≤ VDD ≤ 3.6V, -40 ℃ ≤ T_a ≤ 125 ℃			50[4]	nA
	High-Z leakage current (PM package)	SDIO[2] [3]	1.62V ≤ VDD ≤ 3.6V, -40 ℃ ≤ T_a ≤ 85 ℃			70[4]	nA
			1.62V ≤ VDD ≤ 3.6V, -40 ℃ ≤ T_a ≤ 125 ℃			400[4]	nA
R_{PU}	Pull up resistance	All I/O except ODIO	VIN = VSS		40		kΩ
R_{PD}	Pull down resistance		VIN = VDD		40		kΩ
C_I	Input capacitance		VDD = 3.3V		5		pF
V_{OH}	High level output voltage	SDIO	VDD≥2.7V, $\|I_{IO}\|_{,max}$=6mA VDD≥1.71V, $\|I_{IO}\|_{,max}$=2mA VDD≥1.62V, $\|I_{IO}\|_{,max}$=1.5mA -40 °C ≤T_j≤25 °C	VDD-0.4			V
			VDD≥2.7V, $\|I_{IO}\|_{,max}$=6mA VDD≥1.71V, $\|I_{IO}\|_{,max}$=2mA VDD≥1.62V, $\|I_{IO}\|_{,max}$=1.5mA -40 °C ≤T_j≤130 °C	VDD-0.45			
		HSIO	VDD≥2.7V, DRV=1, $\|I_{IO}\|_{,max}$=6mA VDD≥1.71V, DRV=1, $\|I_{IO}\|_{,max}$=3mA VDD≥1.62V, DRV=1, $\|I_{IO}\|_{,max}$=2mA -40 °C ≤T_j≤25 °C	VDD-0.4			
			VDD≥2.7V, DRV=1, $\|I_{IO}\|_{,max}$=6mA VDD≥1.71V, DRV=1, $\|I_{IO}\|_{,max}$=3mA VDD≥1.62V, DRV=1, $\|I_{IO}\|_{,max}$=2mA -40 °C ≤T_j≤130 °C	VDD-0.45			
			VDD≥2.7V, DRV=0, $\|I_{IO}\|_{,max}$=4mA VDD≥1.71V, DRV=0, $\|I_{IO}\|_{,max}$=2mA VDD≥1.62V, DRV=0, $\|I_{IO}\|_{,max}$=1.5mA -40 °C ≤T_j≤25 °C	VDD-0.4			
			VDD≥2.7V, DRV=0, $\|I_{IO}\|_{,max}$=4mA VDD≥1.71V, DRV=0, $\|I_{IO}\|_{,max}$=2mA VDD≥1.62V, $\|I_{IO}\|_{,max}$=1.5mA -40 °C ≤T_j≤130 °C	VDD-0.45			
		HDIO	VDD≥2.7V, DRV=1, $\|I_{IO}\|_{,max}$=20mA VDD≥1.71V, DRV=1, $\|I_{IO}\|_{,max}$=10mA	VDD-0.4			
			VDD≥2.7V, DRV=0, $\|I_{IO}\|_{,max}$=6mA VDD≥1.71V, DRV=0, $\|I_{IO}\|_{,max}$=2mA	VDD-0.4			

ADVANCE INFORMATION

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OL}	Low level output voltage	SDIO	VDD≥2.7V, $\lvert I_{IO}\rvert_{,max}$=6mA VDD≥1.71V, $\lvert I_{IO}\rvert_{,max}$=2mA VDD≥1.62V, $\lvert I_{IO}\rvert_{,max}$=1.5mA -40 °C ≤$T_j$≤25 °C			0.4	V
			VDD≥2.7V, $\lvert I_{IO}\rvert_{,max}$=6mA VDD≥1.71V, $\lvert I_{IO}\rvert_{,max}$=2mA VDD≥1.62V, $\lvert I_{IO}\rvert_{,max}$=1.5mA -40 °C ≤$T_j$≤130 °C			0.45	V
		HSIO	VDD≥2.7V, DRV=1, $\lvert I_{IO}\rvert_{,max}$=6mA VDD≥1.71V, DRV=1, $\lvert I_{IO}\rvert_{,max}$=3mA VDD≥1.62V, DRV=1, $\lvert I_{IO}\rvert_{,max}$=2mA -40 °C ≤$T_j$≤25 °C			0.4	
			VDD≥2.7V, DRV=1, $\lvert I_{IO}\rvert_{,max}$=6mA VDD≥1.71V, DRV=1, $\lvert I_{IO}\rvert_{,max}$=3mA VDD≥1.62V, DRV=1, $\lvert I_{IO}\rvert_{,max}$=2mA -40 °C ≤$T_j$≤130 °C			0.45	
			VDD≥2.7V, DRV=0, $\lvert I_{IO}\rvert_{,max}$=4mA VDD≥1.71V, DRV=0, $\lvert I_{IO}\rvert_{,max}$=2mA VDD≥1.62V, DRV=0, $\lvert I_{IO}\rvert_{,max}$=1.5mA -40 °C ≤$T_j$≤25 °C			0.4	
			VDD≥2.7V, DRV=0, $\lvert I_{IO}\rvert_{,max}$=4mA VDD≥1.71V, DRV=0, $\lvert I_{IO}\rvert_{,max}$=2mA VDD≥1.62V, DRV=0, $\lvert I_{IO}\rvert_{,max}$=1.5mA -40 °C ≤$T_j$≤130 °C			0.45	
		HDIO	VDD≥2.7V, DRV=1, $\lvert I_{IO}\rvert_{,max}$=20mA VDD≥1.71V, DRV=1, $\lvert I_{IO}\rvert_{,max}$=10mA			0.4	
			VDD≥2.7V, DRV=0, $\lvert I_{IO}\rvert_{,max}$=6mA VDD≥1.71V, DRV=0, $\lvert I_{IO}\rvert_{,max}$=2mA			0.4	
		ODIO	VDD≥2.7V, $I_{OL,max}$=8mA VDD≥1.71V, $I_{OL,max}$=4mA -40 °C ≤T_j≤25 °C			0.4	V
			VDD≥2.7V, $I_{OL,max}$=8mA VDD≥1.71V, $I_{OL,max}$=4mA -40 °C ≤T_j≤130 °C			0.45	V

(1) I/O Types: ODIO = 5V Tolerant Open-Drain , SDIO = Standard-Drive , HSIO = High-Speed, HDIO = High-Drive
(2) The leakage current is measured with VSS or VDD applied to the corresponding pin(s), unless otherwise noted.
(3) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.
(4) This value is for SDIO not muxed with any analog inputs. If the SDIO is muxed with analog inputs then the leakage can be higher.

7.10.2 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Port output frequency(1)	SDIO	VDD ≥ 2.7V, CL= 20pF			32	MHz
			VDD ≥ 1.71V, CL= 20pF			16	
		HSIO	VDD ≥ 2.7V, DRV = 1, CL= 20pF			40	
			VDD ≥ 2.7V, DRV = 0, CL= 20pF			32	
			VDD ≥ 1.71V, DRV = 1, CL= 20pF			24	
			VDD ≥ 1.71V, DRV = 0, CL= 20pF			16	
		HDIO	VDD ≥ 2.7V, DRV = 1(2), CL= 20pF			20	
			VDD ≥ 2.7V, DRV = 0, CL= 20pF			20	
			VDD ≥ 1.71V, DRV = 1(2), CL= 20pF			16	
			VDD ≥ 1.71V, DRV = 0, CL= 20pF			16	
		ODIO	VDD ≥ 1.71V, FM^+, CL= 20pF - 100pF			1	

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_r,t_f	Output rise/fall time	SDIO	VDD ≥ 2.7V, CL= 20pF			3.5	ns
			VDD ≥ 1.71V, C_L= 20pF			6.6	
		HSIO	VDD ≥ 2.7V, DRV = 1, CL= 20pF			1.8	
			VDD ≥ 2.7V, DRV = 0, CL= 20pF			5.9	
			VDD ≥ 1.71V, DRV = 1, CL= 20pF			3.7	
			VDD ≥ 1.71V, DRV = 0, CL= 20pF			12.6	
		HDIO	VDD ≥ 2.7V, DRV = 1, CL= 20pF			1.7	
			VDD ≥ 2.7V, DRV = 0, CL= 20pF			3.8	
			VDD ≥ 1.71V, DRV = 1, CL= 20pF			3.1	
			VDD ≥ 1.71V, DRV = 0, CL= 20pF			8.2	
t_f	Output fall time	ODIO	VDD ≥ 1.71V, FM$^+$, CL= 20pF-100pF	20*VDD/5.5		120	ns

(1) I/O Types: ODIO = 5V Tolerant Open-Drain , SDIO = Standard-Drive , HSIO = High-Speed , HDIO = High-Drive, USBIO = USB protocol
(2) When operating a HDIO in DRV=1 high drive strength configuration, a series resistor is necessary to limit the signal slew rate

7.11 Analog Mux VBOOST

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VBST}	VBOOST current adder	MCLK/ULPCLK is LFCLK		0.8		uA
		MCLK/ULPCLK is not LFCLK, SYSOSC frequency is 4MHz		10.6		
$t_{START,VBST}$	VBOOST startup time			12	20	us

7.12 ADC

7.12.1 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), all TYP values are measured at 25℃ and all accuracy parameters are measured using 12-bit resolution mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$Vin_{(ADC)}$	Analog input voltage range[1]	Applies to all ADC analog input pins	0		VDD	V
V_{R+}	Positive ADC reference voltage	V_{R+} sourced from VDD		VDD		V
		V_{R+} sourced from internal reference (VREF)		VREF		V
V_{R-}	Negative ADC reference voltage			0		V
Fs	ADC sampling frequency	RES = 0x0 (12-bit mode), External/Internal Reference(VRSEL=1h)			1.6	Msps
		RES = 0x1 (10-bit mode), External/Internal Reference(VRSEL1h)			1.7	
		RES = 0x2 (8-bit mode), External/Internal Reference(VRSEL=1h)			2	
F_S	ADC sampling frequency	RES = 0x0 (12-bit mode), Internal Reference(VRSEL=2h)			0.9	Msps
		RES = 0x1 (10-bit mode), Internal Reference(VRSEL=2h)			1	
		RES = 0x2 (8-bit mode), Internal Reference(VRSEL=2h)			1.2	
$I_{(ADC)}$	Operating supply current into VDD terminal	F_S = 1.6MSPS, External reference(VRSEL=1h),V_{R+} = VDD		350		µA
$I_{(ADC)}$	Operating supply current into VDD terminal	F_S = 1.6MSPS, Internal reference(VRSEL=1h),VREF = 2.5V (VREF1 power consumption included)		550		µA
		F_S = 0.9MSPS,Internal reference(VRSEL=2h),VREF = 2.5V (VREF2 power consumption included)		400		
$C_{S/H}$	ADC sample-and-hold capacitance			0.22		pF

ADVANCE INFORMATION

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), all TYP values are measured at 25℃ and all accuracy parameters are measured using 12-bit resolution mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Rin	ADC switch resistance			15		kΩ
ENOB	Effective number of bits	Fin=10kHz,External Reference(VRSEL=1h)	10	10.6		bit
		Fin=10kHz,External reference with over sampling		11.8		
		Fin=10kHz,Internal reference(VRSEL=1h or 2h), VREF = 2.5V	9.2	10.2		
SNR	Signal-to-noise ratio	Fin=10kHz,External Reference(VRSEL=1h)		67		dB
		Fin=10kHz,External reference with over sampling		75		
		Fin=10kHz,Internal reference(VRSEL=1h or 2h), V_{R+} = VREF = 2.5V		62		
$PSRR_{DC}$	Power supply rejection ratio, DC	External reference(VRSEL=1h), VDD = $VDD_{(min)}$ to $VDD_{(max)}$		66		dB
$PSRR_{DC}$	Power supply rejection ratio, DC	Internal reference(VRSEL=1h or 2h), V_{R+} = VREF = 2.5V, VDD=2.7 to 3.6		60		dB
T_{wakeup}	ADC Wakeup Time	Assumes internal reference is active			5	us
$V_{SupplyMon}$	Supply Monitor voltage divider (VDD/3) accuracy	ADC input channel: Supply Monitor (2)	-1.5		+1.5	%
$I_{SupplyMon}$	Supply Monitor voltage divider current consumption	ADC input channel: Supply Monitor		10		uA

(1) The analog input voltage range must be within the selected ADC reference voltage range V_{R+} to V_{R-} for valid conversion results.
(2) Analog power supply monitor. Analog input on channel 31 is disconnected and is internally connected to the voltage divider which is VDD/3.

7.12.2 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{ADCCLK}	ADC clock frequency		4		32	MHz
$t_{ADC\ trigger}$	Software trigger minimum width		3			ADCCLK cycles
t_{Sample_step}	Sampling time for step input	12-bit mode, R_S = 50Ω, C_{pext} = 10pF	0.188			µs
t_{Sample_VREF}	Sample time with VREF	ADC CHANNEL=28,12-bit mode, VDD as reference	4			µs
$t_{Sample\_SupplyMon}$	Sample time with Supply Monitor (VDD/3)	ADC CHANNEL=30,12-bit mode,Internal reference(VRSEL=1h or 2h)	5			µs

7.12.3 Linearity Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), all TYP values are measured at 25℃ and all linearity parameters are measured using 12-bit resolution mode (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
E_I	Integral linearity error (INL)	External reference	-2		2	LSB
E_D	Differential linearity error (DNL)	External reference (2)	-1		1	LSB
E_O	Offset error	External reference (2)	-5		5	mV
E_G	Gain error	External reference(VRSEL=1h) (2)	-6		6	LSB

(1) Total Unadjusted Error (TUE) can be calculated from E_I , E_O , and E_G using the following formula: TUE = $\sqrt{(E_I^2 + |E_O|^2 + E_G^2)}$
Note: You must convert all of the errors into the same unit, usually LSB, for the above equation to be accurate
(2) VDD reference specifications are measured with V_{R+} = VDD = 3.3V and V_{R-} = VSS = 0V.

7.12.4 Typical Connection Diagram

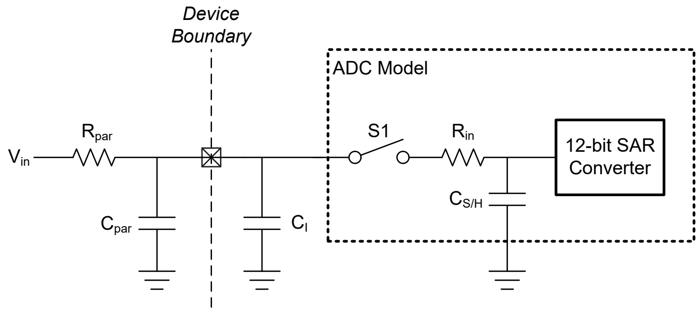

Figure 7-2. ADC Input Network

1. Refer to *ADC ADC Electrical Characteristics* for the values of R_{in} and $C_{S/H}$
2. Refer to *Digital IO Electrical Characteristics* for the value of C_I
3. C_{par} and R_{par} represent the parasitic capacitance and resistance of the external ADC input circuitry

Use the following equations to solve for the minimum sampling time (T) required for an ADC conversion:

1. $Tau = (R_{par} + R_{in})* C_{S/H} + R_{par}*(C_{par} + C_I)$
2. $K= ln(2^n/Settling\ error) – ln((C_{par} + C_I)/C_{S/H})$
3. T (Min sampling time) = K*Tau

7.13 Temperature Sensor

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TS_{TRIM}	Factory trim temperature (1)	ADC and VREF configuration: RES=0 (12-bit mode), VRSEL=2h(Internal reference), V_{R+} = VREF = 1.4V (BUFCONFIG =1), cap=1uF on VREF+, ADC t_{Sample}=10µs	27	30	33	℃
TS_c	Temperature coefficient	-40℃ ≤ T_j ≤ 130℃	-2.05	-1.90	-1.75	mV/℃
$t_{SET, TS}$	Temperature sensor settling time (2)	ADC and VREF configuration: RES=0 (12-bit mode), VRSEL= 2h(internal reference), ADC CHANNEL=11			10	us

(1) Higher absolute accuracy may be achieved through user calibration. Please refer to temperature sensor chapter in detailed description section.
(2) This is the minimum required ADC sampling time when measuring the temperature sensor.

7.14 VREF1

7.14.1 Voltage Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD_{min}	Minimum supply voltage needed for VREF operation	BUFCONFIG = 1	1.62			V
		BUFCONFIG = 0	2.7			
VREF	Voltage reference output voltage	BUFCONFIG = 1	1.38	1.4	1.42	V
		BUFCONFIG = 0	2.46	2.5	2.54	

7.14.2 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VREF}	VREF operating supply current	BUFCONFIG = {0, 1}, No load		189	330	µA

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over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{Drive}	VREF output drive strength (1)	Drive strength supported on VREF+ device pin			100	µA
I_{SC}	VREF short circuit current				100	mA
TC_{VREF}	Temperature coefficient of VREF (Bandgap+VRBUF) (2)	BUFCONFIG = {1}			75	ppm/°C
TC_{VREF}	Temperature coefficient of VREF (Bandgap+VRBUF) (2)	BUFCONFIG = {0}			75	ppm/°C
TC_{drift}	Long term VREF drift	Time = 1000 hours, BUFCONFIG = {0, 1}, T = 25℃			300	ppm
$PSRR_{DC}$	VREF Power supply rejection ratio, DC	VDD = 1.7 V to VDDmax, BUFCONFIG = 1	60	70		dB
		VDD = 2.7 V to VDDmax, BUFCONFIG = 0	50	60		
V_{noise}	RMS noise at VREF output (0.1 Hz to 100 MHz)	BUFCONFIG = 1		350		µVrms
		BUFCONFIG = 0		500		
C_{VREF}	Recommended VREF decoupling capacitor on VREF+ pin (3) (4) (5)		0.7	1	1.15	µF
$T_{startup}$	VREF startup time	BUFCONFIG = {0, 1} , VDD = 2.8 V, C_{VREF} = 1µF			200	µS
$T_{refresh}$	VREF External capacitor refresh time		31.25			

(1) The specified MAX output drive strength is supported regardless of which peripherals are being used in the device.
(2) The temperature coefficient of the VREF output is the sum of TC_{VRBUF} and the temperature coefficient of the internal bandgap reference.
(3) Decoupling capacitor (C_{VREF}) is required when using the internal voltage reference VREF and should be connected from the VREF+ pin to VREF-/GND. When using the VREF+/- pins to supply an external reference, a decoupling capacitor value should be selected based on the external reference source.
(4) A ceramic capacitor with package size of 0805 or smaller is preferred. Up to ±20% tolerance is acceptable
(5) The VREF module should only be enabled when C_{VREF} is connected and should not be enabled otherwise.

7.15 VREF2

7.15.1 Voltage Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD_{min}	Minimum supply voltage needed for VREF operation	BUFCONFIG = 1	1.62			V
		BUFCONFIG = 0	2.7			
VREF	Voltage reference output voltage	BUFCONFIG = 1	1.38	1.4	1.42	V
		BUFCONFIG = 0	2.46	2.5	2.54	

7.15.2 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{VREF}	VREF operating supply current	BUFCONFIG = {0, 1}, No load			130	200	µA
TC_{VREF}	Temperature coefficient of VREF (Bandgap+VRBUF) (1)	BUFCONFIG = {0,1}				80	ppm/°C
TC_{drift}	Long term VREF drift	Time = 1000 hours, BUFCONFIG = {0, 1}, T = 25℃				300	ppm
$PSRR_{DC}$	VREF Power supply rejection ratio, DC	VDD = 1.7 V to VDDmax, BUFCONFIG = 1		60	70		dB
		VDD = 2.7 V to VDDmax, BUFCONFIG = 0		50	60		
V_{noise}	RMS noise at VREF output (0.1 Hz to 100 MHz)	BUFCONFIG = 1			350		µVrms
		BUFCONFIG = 0			500		
ADC F_S	Max supported ADC sampling frequency	Using VREF as ADC reference	Using VREF as ADC reference			900	Ksps

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{startup}$	VREF startup time				30	us

(1) The temperature coefficient of the VREF output is the sum of TC_{VRBUF} and the temperature coefficient of the internal bandgap reference.

7.16 Comparator (COMP)

7.16.1 Comparator Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Comparator Electrical Characteristics						
Vcm	Common mode input range		0		VDD	V
V_{offset}	Input offset voltage		-20		20	mV
V_{hys}	DC input hysteresis	HYST=00h		0.4		mV
		HYST=01h		10		
		HYST=02h		20		
		HYST=03h		30		
t_{PD_ls}	Propagation delay, response time	Output Filter off, Overdrive = 100 mV, High Speed Mode		32	50	ns
		Output Filter off, Overdrive = 100 mV, Low Power Mode		1.2	4	µs
t_{en}	Comparator enable time	Startup time to reach propagation delay specification, High Speed Mode (comparator only)			5	µs
		Startup time to reach propagation delay specification, Low Power Mode (comparator only)			10	µs
I_{comp}	Comparator current consumption.	Vcm = VDD/2, 100mV overdrive, DAC output as a voltage reference, VDD is reference for DAC, High Speed Mode		130	200	µA
		Vcm = VDD/2, 100mV overdrive, DAC output as a voltage reference, VDD is reference for DAC, Low Power Mode		0.85	2.7	µA
		Vcm = VDD/2, 100mV overdrive, comparator only. High Speed Mode		120	180	µA
		Vcm = VDD/2, 100mV overdrive, comparator only, Low Power Mode		0.7	2.1	µA
I_{comp}	Comparator +VREF current consumption in low power	Vcm = VDD/2, 100mV overdrive, DAC output as a voltage reference, Internal VREF is reference for DAC, Low Power Mode. VREF registers SHCYCLE=0xC0, HCYCLE=0xC0, SHMODE=1		3		uA
8-bit DAC Electrical Characteristics						
V_{dac}	DAC output range		0		VDD	V
$V_{dac\text{-}code}$	8-bit DAC output voltage for a given code	VIN = reference voltage into 8-bit DAC, code n = 0 to 255		VIN × (n+1) / 256		V
INL	Integral nonlinearity of 8-bit DAC		-1		1	LSB
DNL	Differential nonlinearity of 8-bit DAC		-1		1	LSB
Gain error	Gain error of 8-bit DAC	Reference voltage = VDD	-2		2	% of FSR
Offset error	Offset error of 8-bit DAC		-5		5	mV
Output Impedance	8-bit DAC output impedance			50		kΩ
t_{dac_settle}	8-bit DAC settling time in static mode	DACCODE0 = 0 → 255, DAC output accurate to 1 LSB, DAC out-put on pin PA3, PA11, Cload = 15pF		6		µs
t_{dac_settle}	8-bit DAC settling time in static mode	DACCODE0 = 0 → 255, DAC output accurate to 1 LSB		1.5		µs

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7.17 I2C

7.17.1 I2C Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	Standard mode		Fast mode		Fast mode plus		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{I2C}	I2C input clock frequency	I2C in Power Domain0	2	32	8	32	20	32	MHz
f_{SCL}	SCL clock frequency		0.025	0.1		0.4		1	MHz
$t_{HD,STA}$	Hold time (repeated) START		4		0.6		0.26		us
t_{LOW}	LOW period of the SCL clock		4.7		1.3		0.5		us
t_{HIGH}	High period of the SCL clock		4		0.6		0.26		us
$t_{SU,STA}$	Setup time for a repeated START		4.7		0.6		0.26		us
$t_{HD,DAT}$	Data hold time		0		0		0		ns
$t_{SU,DAT}$	Data setup time		250		100		50		ns
$t_{SU,STO}$	Setup time for STOP		4		0.6		0.26		us
t_{BUF}	bus free time between a STOP and START condition		4.7		1.3		0.5		us
$t_{VD;DAT}$	data valid time			3.45		0.9		0.45	us
$t_{VD;ACK}$	data valid acknowledge time			3.45		0.9		0.45	us

7.17.2 I2C Filter

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SP}	Pulse duration of spikes suppressed by input filter	AGFSELx = 0		6		ns
		AGFSELx = 1		14	35	ns
		AGFSELx = 2		22	60	ns
		AGFSELx = 3		35	90	ns

7.17.3 I²C Timing Diagram

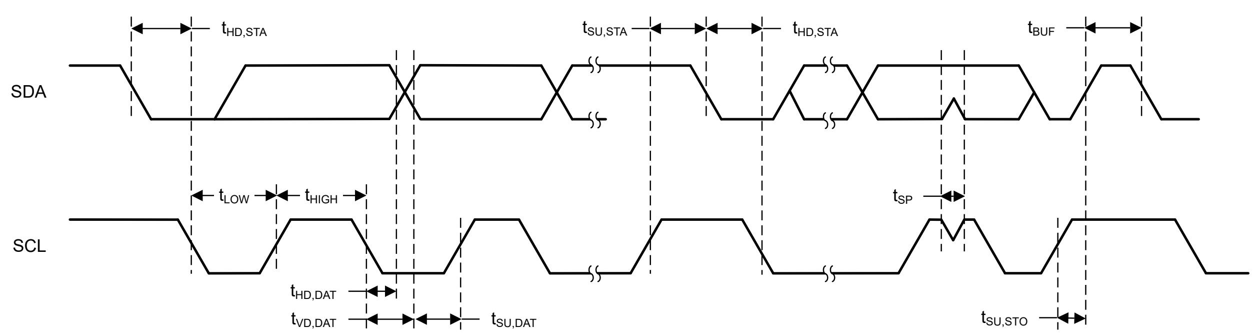

Figure 7-3. I2C Timing Diagram

7.18 SPI

7.18.1 SPI

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SPI						
f_{SPI}	SPI clock frequency	Clock max speed >= 32MHz 1.62 < VDD < 3.6V Peripheral or Controller mode			16	MHz

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SPI}	SPI clock frequency	Clock max speed >= 48MHz 1.62 < VDD < 2.7V Peripheral or Controller mode with High speed IO			24	MHz
f_{SPI}	SPI clock frequency	Clock max speed >= 64MHz 2.7 < VDD < 3.6V Peripheral or Controller mode with High speed IO			32	MHz
DC_{SCK}	SCK Duty Cycle		40	50	60	%
Controller						
$t_{SCLK\_H/L}$	SCLK High or Low time		(tSPI/2) - 1	tSPI / 2	(tSPI/2) + 1	ns
$t_{CS.LEAD}$	CS lead-time, CS active to clock	SPH=0	1 SPI Clock			
$t_{CS.LEAD}$	CS lead-time, CS active to clock	SPH=1	1/2 SPI Clock			
$t_{CS.LAG}$	CS lag time, Last clock to CS inactive	SPH=0	1/2 SPI Clock			
$t_{CS.LAG}$	CS lag time, Last clock to CS inactive	SPH=1	1 SPI Clock			
$t_{CS.ACC}$	CS access time, CS active to PICO data out				1/2 SPI Clock	
$t_{CS.DIS}$	CS disable time, CS inactive to PICO high impedance				1 SPI Clock	
$t_{SU.CI}$	POCI input data setup time (1)	2.7 < VDD < 3.6V, delayed sampling enabled	2.86			ns
$t_{SU.CI}$	POCI input data setup time (1)	1.62 < VDD < 2.7V, delayed sampling enabled	11.5			ns
$t_{SU.CI}$	POCI input data setup time (1)	2.7 < VDD < 3.6V, no delayed sampling	28			ns
$t_{SU.CI}$	POCI input data setup time (1)	1.62 < VDD < 2.7V, no delayed sampling	37			ns
$t_{HD.CI}$	POCI input data hold time	delayed sampling enabled	22			ns
$t_{HD.CI}$	POCI input data hold time	no delayed sampling	0			ns
$t_{VALID.CO}$	PICO output data valid time (2)				8	ns
$t_{HD.CO}$	PICO output data hold time (3)		0			ns
Peripheral						
$t_{CS.LEAD}$	CS lead-time, CS active to clock		11			ns
$t_{CS.LAG}$	CS lag time, Last clock to CS inactive		0			ns
$t_{CS.ACC}$	CS access time, CS active to POCI data out				44	ns
$t_{CS.DIS}$	CS disable time, CS inactive to POCI high impedance				44	ns
$t_{SU.PI}$	PICO input data setup time		14.5			ns
$t_{HD.PI}$	PICO input data hold time		3.1			ns
$t_{VALID.PO}$	POCI output data valid time (2)	2.7 < VDD < 3.6V			29	ns
$t_{VALID.PO}$	POCI output data valid time (2)	1.62 < VDD < 2.7V			31	ns
$t_{HD.PO}$	POCI output data hold time (3)		5			ns

(1) The POCI input data setup time can be fully compensated when delayed sampling feature is enabled.
(2) Specifies the time to drive the next valid data to the output after the output changing SCLK clock edge
(3) Specifies how long data on the output is valid after the output changing SCLK clock edge

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7.18.2 SPI Timing Diagram

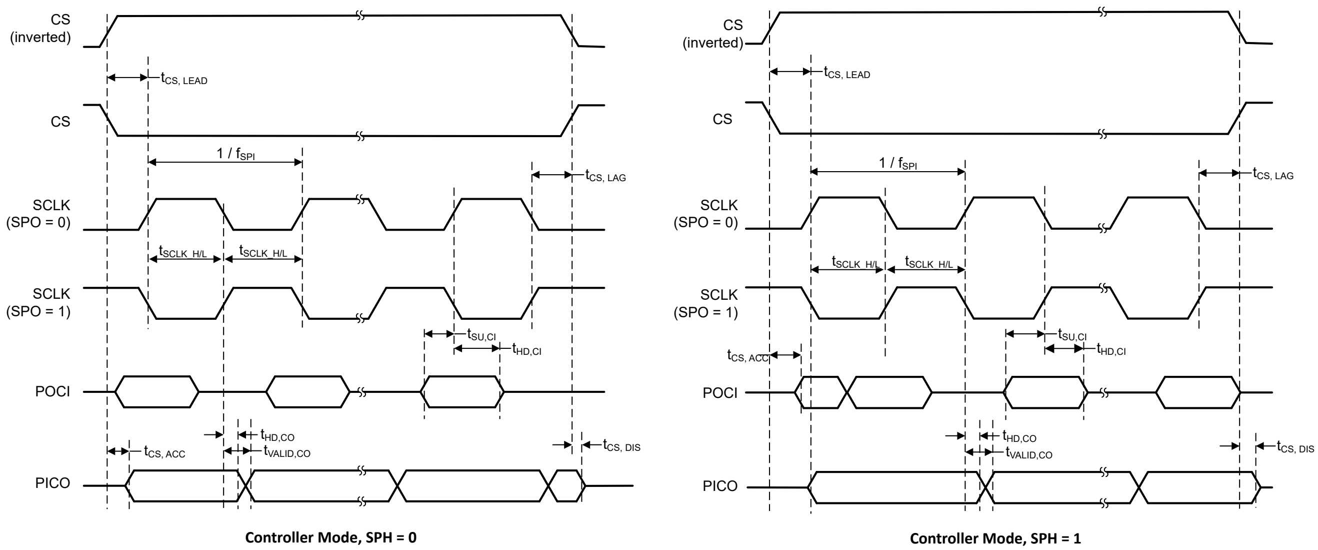

Figure 7-4. SPI timing diagram - Controller Mode

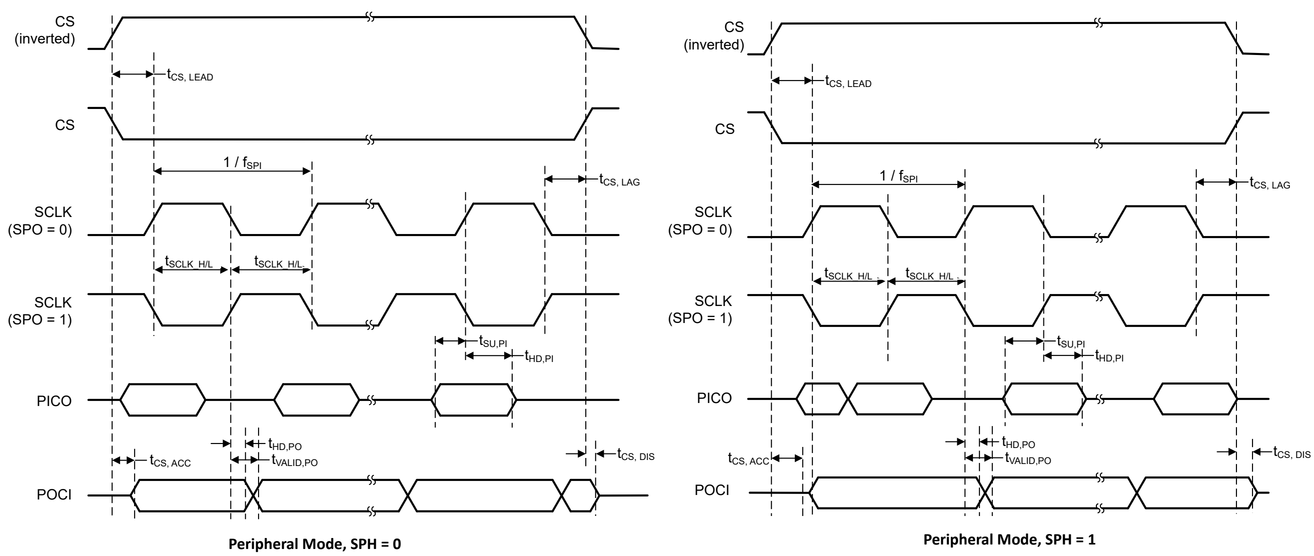

Figure 7-5. SPI timing diagram - Peripheral Mode

7.19 UART

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{UART}	UART input clock frequency	UART in Power Domain1			80	MHz
f_{UART}	UART input clock frequency	UART in Power Domain0			40	MHz
f_{BITCLK}	BITCLK clock frequency(equals baud rate in MBaud)	UART in Power Domain1			10	MHz
f_{BITCLK}	BITCLK clock frequency(equals baud rate in MBaud)	UART in Power Domain0			5	MHz

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SP}	Pulse duration of spikes suppressed by input filter	AGFSELx = 0		6		ns
		AGFSELx = 1		14	35	ns
		AGFSELx = 2		22	60	ns
		AGFSELx = 3		35	90	ns

7.20 TIMx

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{res}	Timer resolution time	TIMx in Power Domain 1, $f_{TIMxCLK}$ = 80MHz	12.5			ns
		TIMx in Power Domain 0, $f_{TIMxCLK}$ = 40MHz	25			ns
			1			$t_{TIMxCLK}$

7.21 TRNG

7.21.1 TRNG Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$TRNG_{IACT}$	TRNG active current	TRNG clock = 20MHz		115		µA

7.22 Emulation and Debug

7.22.1 SWD Timing

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SWD}	SWD frequency				10	MHz

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8 Detailed Description

The following sections describe all of the components that make up the devices in this data sheet. The peripherals integrated into these devices are configured by software through Memory Mapped Registers (MMRs). For more details, see the corresponding chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.1 Functional Block Diagram

Figure 8-1 shows the devices' detailed functional block diagram.

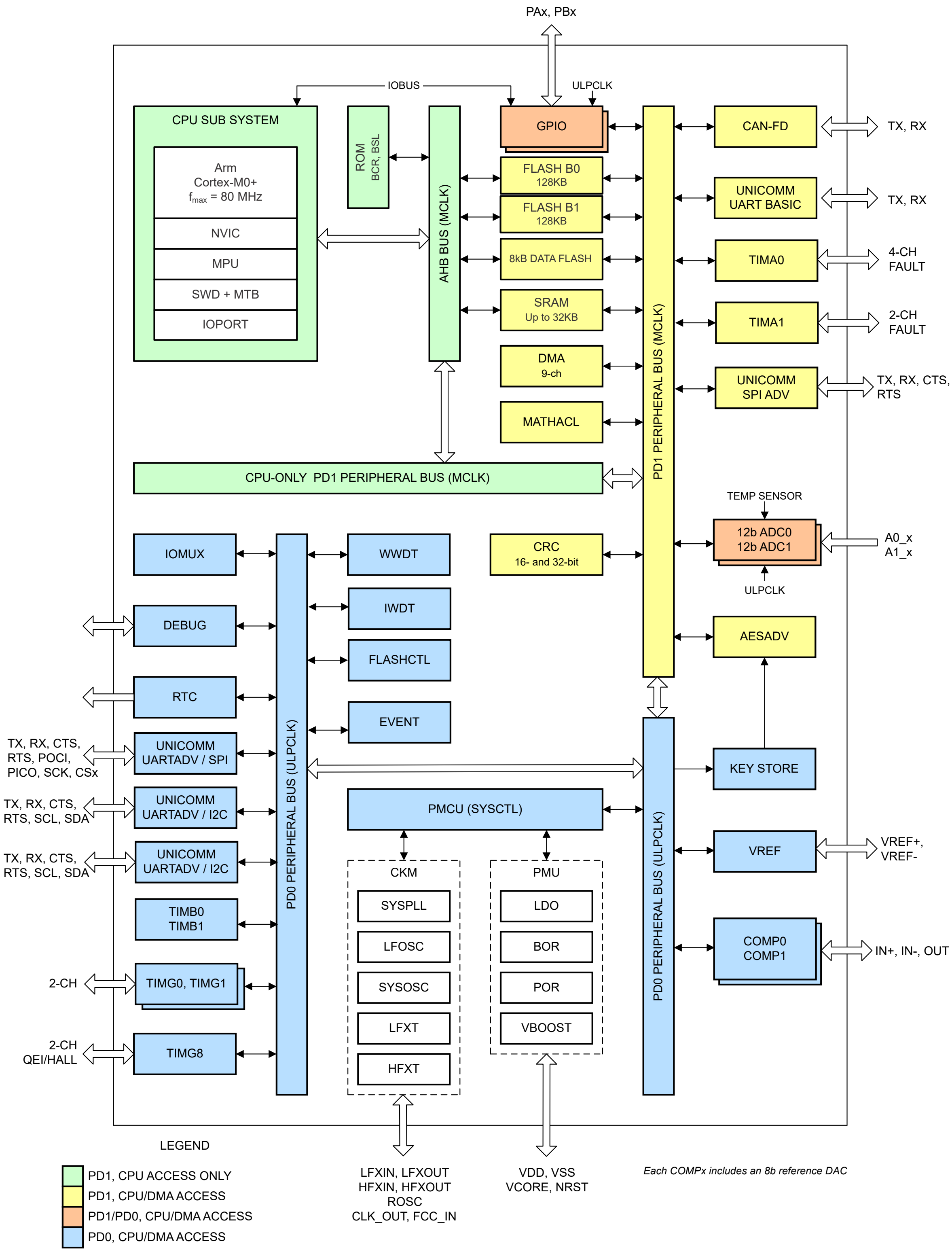

Figure 8-1. MSPM0G3218 Functional Block Diagram

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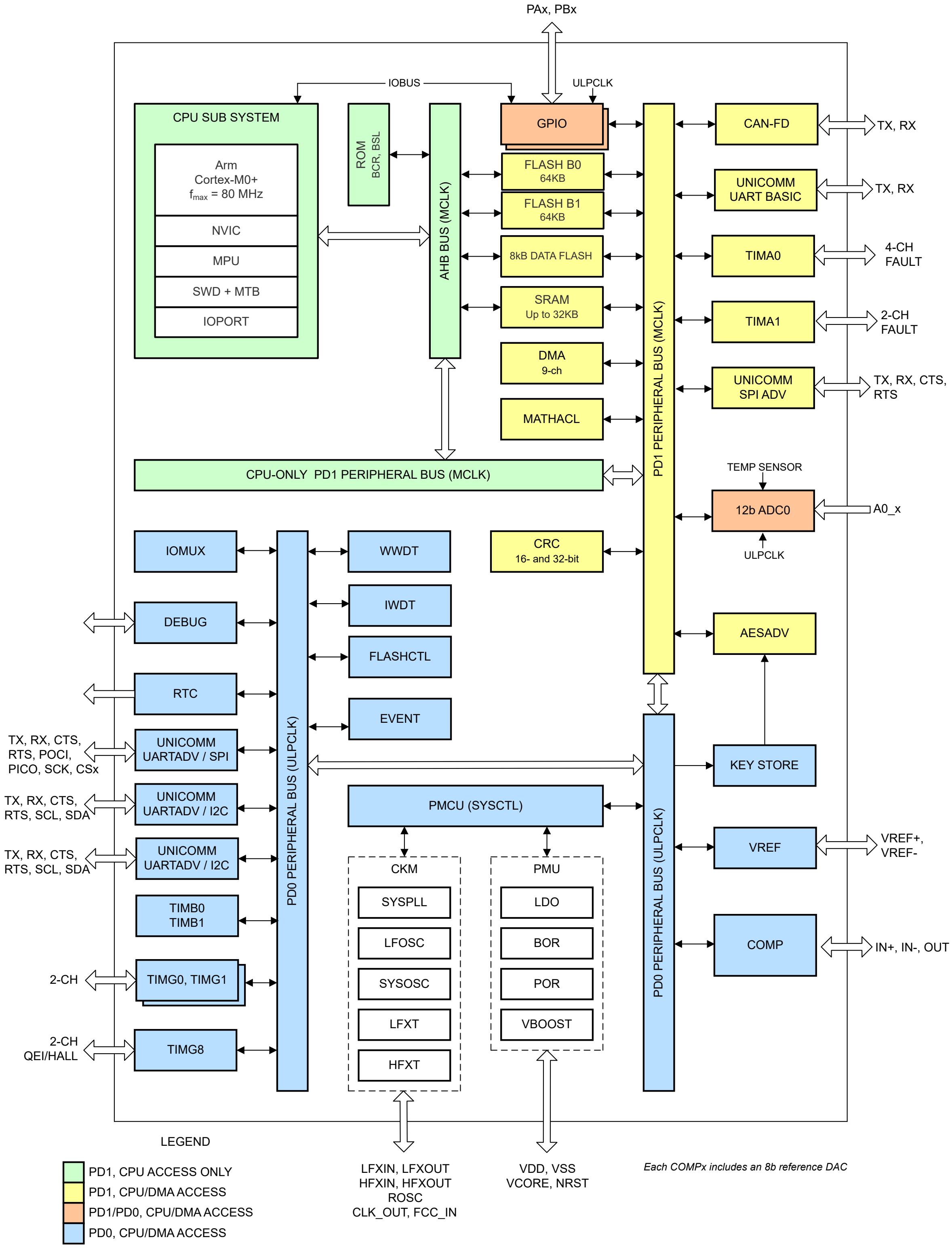

Figure 8-2. MSPM0G3207 Functional Block Diagram

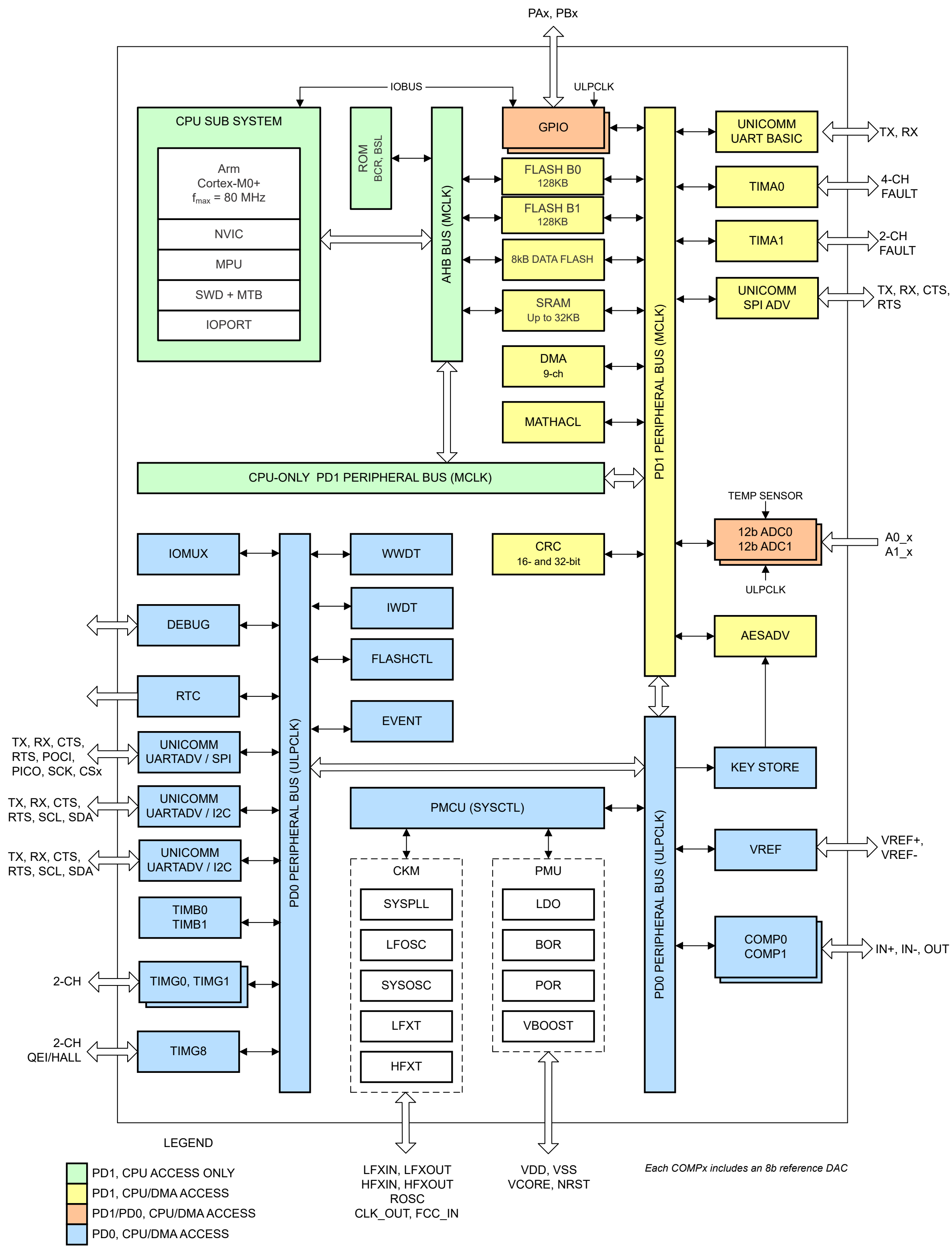

Figure 8-3. MSPM0G1218 Functional Block Diagram

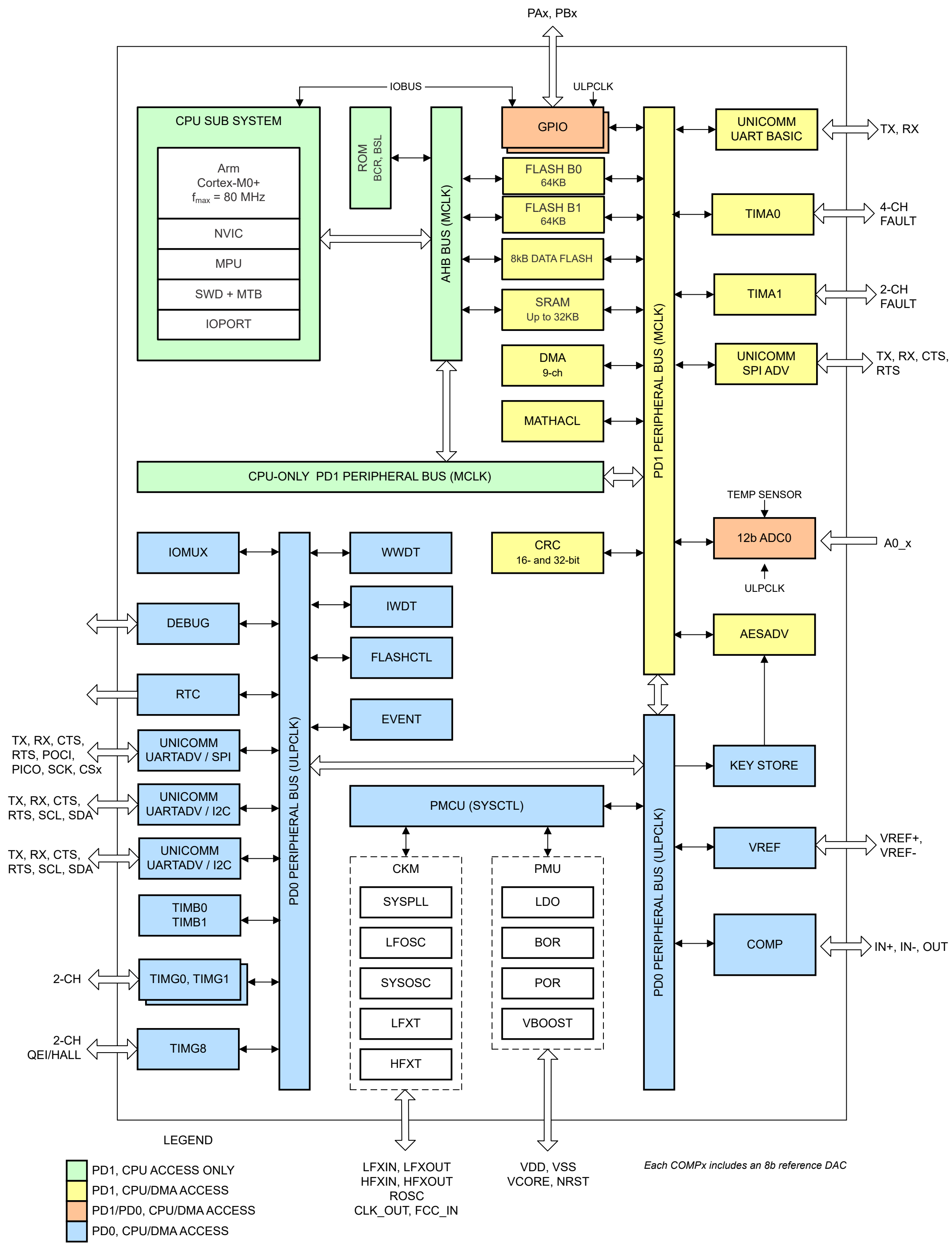

Figure 8-4. MSPM0G1207 Functional Block Diagram

8.2 CPU

The CPU sub system (MCPUSS) implements an ARM Cortex-M0+ CPU, an instruction pre-fetch/cache, a system timer, a memory protection unit, and interrupt management features. The ARM Cortex-M0+ is a cost-optimized, 32-bit CPU which delivers high performance and low power to embedded applications. Key features of the CPU Sub System include:

- ARM Cortex-M0+ CPU supporting clock frequencies from 32kHz to 80MHz
  - ARMv6-M Thumb instruction set (little endian) with single-cycle 32x32 multiply instruction
  - Single-cycle access to GPIO registers via ARM single-cycle IO port
- Pre-fetch logic to improve sequential code execution, and I-cache with 4 64-bit cache lines
- System timer (SysTick) with 24-bit down counter and automatic reload
- Memory protection unit (MPU) with 8 programmable regions
- Nested vectored interrupt controller (NVIC) with 4 programmable priority levels and tail-chaining
- Interrupt groups for expanding the total interrupt sources, with jump index for low interrupt latency

8.3 Operating Modes

MSPM0G MCUs provide five main operating modes (power modes) to allow for optimization of the device power consumption based on application requirements. In order of decreasing power, the modes are: RUN, SLEEP, STOP, STANDBY, and SHUTDOWN. The CPU is active executing code in RUN mode. Peripheral interrupt events can wake the device from SLEEP, STOP, or STANDBY mode to the RUN mode. SHUTDOWN mode completely disables the internal core regulator to minimize power consumption, and wake is only possible via NRST, SWD, or a logic level match on certain IOs. RUN, SLEEP, STOP, and STANDBY modes also include several configurable policy options (e.g. RUN.x) for balancing performance with power consumption.

To further balance performance and power consumption, MSPM0G devices implement two power domains: PD1 (for the CPU, memories, and high performance peripherals), and PD0 (for low speed, low power peripherals). PD1 is always powered in RUN and SLEEP modes, but is disabled in all other modes. PD0 is always powered in RUN, SLEEP, STOP, and STANDBY modes. PD1 and PD0 are both disabled in SHUTDOWN mode.

8.3.1 Functionality by Operating Mode (MSPM0Gx218, MSPM0Gx207, MSPM0G122x)

Supported functionality in each operating mode is given in Table 8-1.

Functional key:

- **EN**: The function is enabled in the specified mode.
- **DIS**: The function is disabled (either clock or power gated) in the specified mode, but the function's configuration is retained.
- **OPT**: The function is optional in the specified mode, and remains enabled if configured to be enabled.
- **NS**: The function is not automatically disabled in the specified mode, but it is not supported.
- **OFF**: The function is fully powered off in the specified mode, and no configuration information is retained. When waking up from an OFF state, all module registers must be re-configured to the desired settings by application software.

Table 8-1. Supported Functionality by Operating Mode

OPERATING MODE		RUN			SLEEP			STOP			STANDBY		SHUTDOWN
		RUN0	RUN1	RUN2	SLEEP0	SLEEP1	SLEEP2	STOP0	STOP1	STOP2	STANDBY0	STANDBY1	
Oscillators	SYSOSC	EN		DIS	EN		DIS	OPT(1)	EN	DIS	DIS		OFF
	LFOSC or LFXT	EN (LFOSC or LFXT)											OFF
	HFXT	OPT	DIS		OPT	DIS		DIS			DIS		OFF
	SYSPLL	OPT	DIS(4)		OPT	DIS(4)		DIS(4)			DIS(4)		OFF

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Table 8-1. Supported Functionality by Operating Mode (continued)

OPERATING MODE		RUN			SLEEP			STOP			STANDBY		SHUTDOWN
		RUN0	RUN1	RUN2	SLEEP0	SLEEP1	SLEEP2	STOP0	STOP1	STOP2	STANDBY0	STANDBY1	
Clocks	CPUCLK	80 MHz	32 kHz		DIS								OFF
	MCLK to PD1	80 MHz	32 kHz		80 MHz	32 kHz		DIS					OFF
	ULPCLK to PD0	40 MHz	32 kHz		40 MHz	32 kHz		4 MHz [1]	4 MHz	32 kHz	32 kHz	DIS	OFF
	ULPCLK to TIMG0/8	40 MHz	32 kHz		40 MHz	32 kHz		4 MHz [1]	4 MHz	32 kHz	32 kHz	32 kHz [2]	OFF
	RTCCLK	32 kHz											OFF
	MFCLK	OPT	DIS		OPT	DIS		OPT		DIS	DIS		OFF
	MFPCLK	OPT	DIS		OPT	DIS		OPT		DIS	DIS		OFF
	LFCLK to PD0/1	32 kHz										DIS	OFF
	LFCLK to TIMG0/8	32 kHz										32 kHz [2]	OFF
	LFCLK Monitor	OPT											OFF
	MCLK Monitor	OPT										DIS	OFF
PMU	POR monitor	EN											
	BOR monitor	EN											OFF
	Core regulator	FULL DRIVE						REDUCED DRIVE			LOW DRIVE		OFF
Core Functions	CPU	EN			DIS								OFF
	DMA	OPT						DIS (triggers supported)					OFF
	Flash	EN						DIS					OFF
	SRAM	EN						DIS					OFF
PD1 Peripherals	MATHACL	OPT						OFF					OFF
	MCAN0	OPT	OFF		OPT	OFF		OFF					OFF
	TIMA0/1	OPT						OFF					OFF
	AESADV	OPT						OFF					OFF
	CRC-P	OPT						DIS					OFF
	UC2	OPT						DIS					OFF
	UC9	OPT						DIS					OFF
PD0 Peripheral	GPIOA/B[3]	OPT										OPT[2]	OFF
	TIMG0/8	OPT											OFF
	TIMB0/1	OPT											OFF
	UC0	OPT										OPTOPT[2]	OFF
	UC4	OPT										OPTOPT[2]	OFF
	UC5	OPT										OPTOPT[2]	OPT
	WWDT0/1	OPT										DIS	OFF
	IWDT	OPT											OFF
	RTC_B	OPT											OFF
	Keystore	OPT											OFF

Table 8-1. Supported Functionality by Operating Mode (continued)

OPERATING MODE		RUN			SLEEP			STOP			STANDBY		SHUTDOWN
		RUN0	RUN1	RUN2	SLEEP0	SLEEP1	SLEEP2	STOP0	STOP1	STOP2	STANDBY0	STANDBY1	
Analog	VREF1	OPT											OFF
	VREF2	OPT								NS			OFF
	ADC0/1[3]	OPT								NS (triggers supported)			OFF
	COMP0/1	OPT	OPT (ULP)		OPT	OPT (ULP)		OPT		OPT (ULP)			OFF
	Temperature Sensor	OPT									OFF		OFF
IOMUX and IO Wakeup		EN											DIS w/ WAKE
Wake Sources		N/A			ANY IRQ			PD0 IRQ					IOMUX, NRST, SWD

(1) If STOP0 is entered from RUN1 (SYSOSC enabled but MCLK sourced from LFCLK), SYSOSC remains enabled as it was in RUN1, and ULPCLK remains at 32 kHz as it was in RUN1. If STOP0 is entered from RUN2 (SYSOSC was disabled and MCLK was sourced from LFCLK), SYSOSC remains disabled as it was in RUN2, and ULPCLK remains at 32 kHz as it was in RUN2.
(2) When using the STANDBY1 policy for STANDBY, only specific peripherals (TIMG0, TIMG8, and RTC) are clocked. Other PD0 peripherals can generate an asynchronous fast clock request upon external activity but are not actively clocked.
(3) For ADCx and GPIOx Ports, the digital logic is in PD0 and the register interface is in PD1. These peripherals support fast single-cycle register access when PD1 is active and also support basic operation down to STANDBY mode where PD0 is still active.
(4) SYSPLL is not automatically disabled, and needs to be manually disabled through the HSCLKEN.SYSPLLEN field within the SYSCTL registers in order to reduce power consumption.

8.4 Power Management Unit (PMU)

The power management unit (PMU) generates the internally regulated core supplies for the device and provides supervision of the external supply (VDD). The PMU also contains the bandgap voltage reference used by the PMU itself as well as analog peripherals. Key features of the PMU include:

- Power-on reset (POR) supply monitor
- Brown-out reset (BOR) supply monitor with early warning capability using three programmable thresholds
- Core regulator with support for RUN, SLEEP, STOP, and STANDBY operating modes to dynamically balance performance with power consumption
- Parity-protected trim to immediately generate a power-on reset (POR) in the event that a power management trim is corrupted

For more details, see the PMU chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.5 Clock Module (CKM)

The clock module provides the following oscillators:

- **LFOSC**: Internal low-frequency oscillator (32KHz)
- **SYSOSC**: Internal high-frequency oscillator (4MHz or 32MHz with factory trim, 16MHz or 24MHz with user trim)
- **LFXT/LFCKIN** : low-frequency external crystal oscillator or digital clock input (32KHz)
- **HFXT/HFCKIN**: high-frequency external crystal oscillator or digital clock input (4 to 48MHz)
- **SYSPLL**: system phase locked loop with 3 outputs (32 to 80MHz)

The following clocks are distributed by the clock module for use by the processor, bus, and peripherals:

- **MCLK**: Main system clock for PD1 peripherals, derived from SYSOSC, LFCLK, or HSCLK, active in RUN and SLEEP modes

- **CPUCLK**: Clock for the processor (derived from MCLK), active in RUN mode
- **ULPCLK**: Ultra-low power clock for PD0 peripherals, active in RUN, SLEEP, STOP, and STANDBY modes
- **MFCLK**: 4MHz fixed mid-frequency clock for peripherals, available in RUN, SLEEP, and STOP modes
- **LFCLK**: 32kHz fixed low-frequency clock for peripherals or MCLK, active in RUN, SLEEP, STOP, and STANDBY modes
- **ADCCLK**: ADC clock, available in RUN, SLEEP and STOP modes
- **CLK_OUT**: Used to output a clock externally, available in RUN, SLEEP, STOP, and STANDBY modes
- **HFCLK**: High frequency clock derived from HFXT or HFCLK_IN, available in RUN and SLEEP mode
- **HSCLK**: High speed clock derived from HFCLK or the SYSPLL, available in RUN and SLEEP mode
- **CANCLK**: CAN functional clock, derived from HFCLK or SYSPLL

For more details, see the CKM chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.6 DMA

The direct memory access (DMA) controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA can be used to move data from ADC conversion memory to SRAM. The DMA reduces system power consumption by allowing the CPU to remain in low power mode, without having to awaken to move data to or from a peripheral.

The DMA in these devices support the following key features:

- 9 independent DMA transfer channels
  - 5 full-feature channel (DMA0-DMA4), supporting repeated transfer modes
  - 4 basic channels (DMA5-DMA8) supporting single transfer modes
- Configurable DMA channel priorities
- Byte (8-bit), short word (16-bit), word (32-bit) and long word (64-bit) and long-long word (128-bit) or mixed byte and word transfer capability
- Transfer counter block size supports up to 64k transfers of any data type
- Configurable DMA transfer trigger selection
- Active channel interruption to service other channels
- Early interrupt generation for ping-pong buffer architecture
- Cascading channels upon completion of activity on another channel
- Stride mode to support data re-organization, such as 3-phase metering applications
- Gather mode

Table 8-2. DMA Features

Feature	FULL	BASIC
Channel#	0,1,2,3,4	5,6,7,8
Repeat Mode	Yes	-
Table & Fill Mode	Yes	-
Gather Mode	Yes	-
Pre-IRQ	Yes	-
Auto Enable	Yes	Yes
Long Long (128-bit) Transfer	Yes	Yes
Stride Mode	Yes	Yes
Cascading Channel Support	Yes	Yes

Table 8-3 lists the available triggers for the DMA which are configured using the DMATCTL.DMATSEL control bits in the DMA memory mapped registers.

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Table 8-3. DMA Trigger Mapping

DMACTL.DMATSEL	Trigger Source
0	Software
1	Generic Subscriber (FSUB_0)
2	Generic Subscriber (FSUB_1)
3	AESADV Publisher 1
4	AESADV Publisher 2
5	S0U2 RX Publisher 1
6	S0U2 TX Publisher 2
7	S0U3 UART RX Publisher 1
8	S0U3 TX Publisher 2
9	S0U4 RX Publisher 1
10	S0U4 TX Publisher 1
11	S1U0 RX Publisher 1
12	S1U0 TX Publisher 2
13	S1U2 RX Publisher 1
14	S1U2 TX Publisher 2
15	ADC0 DMA Trigger
16	ADC1 DMA Trigger

For more details, see the DMA chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.7 Events

The event manager transfers digital events from one entity (for example, a peripheral) to another (for example, a second peripheral, the DMA, or the CPU). The event manager implements event transfer through a defined set of event publishers (generators) and subscribers (receivers) which are interconnected through an event fabric containing a combination of static and programmable routes.

Events which are transferred by the event manager include:

- Peripheral event transferred to the CPU as an interrupt request (IRQ) (Static Event)
  - Example: RTC interrupt is sent to the CPU
- Peripheral event transferred to the DMA as a DMA trigger (DMA Event)
  - Example: UART data receive trigger to DMA to request a DMA transfer
- Peripheral event transferred to another peripheral to directly trigger an action in hardware (Generic Event)
  - Example: TIMx timer peripheral publishes a periodic event to the ADC subscriber port, and the ADC uses the event to trigger start-of-sampling

Refer to Event chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual* for more information.

Table 8-4. Generic Event Channels

A generic route is either a point-to-point (1:1) route or a point-to-two (1:2) splitter route route in which the peripheral publishing the event is configured to use one of several available generic route channels to publish its event to another entity (or entities, in the case of a splitter route), where an entity may be another peripheral, a generic DMA trigger event, or a generic CPU event.

CHANID	Generic Route Channel Selection	Channel Type
0	No generic event channel selected	N/A

Table 8-4. Generic Event Channels (continued)

A generic route is either a point-to-point (1:1) route or a point-to-two (1:2) splitter route route in which the peripheral publishing the event is configured to use one of several available generic route channels to publish its event to another entity (or entities, in the case of a splitter route), where an entity may be another peripheral, a generic DMA trigger event, or a generic CPU event.

CHANID	Generic Route Channel Selection	Channel Type
1	Generic event channel 1 selected	1 : 1
2	Generic event channel 2 selected	1 : 1
3	Generic event channel 3 selected	1 : 1
4	Generic event channel 4 selected	1 : 1
5	Generic event channel 5 selected	1 : 1
6	Generic event channel 6 selected	1 : 1
7	Generic event channel 7 selected	1 : 1
8	Generic event channel 8 selected	1 : 1
9	Generic event channel 9 selected	1 : 1
10	Generic event channel 10 selected	1 : 1
11	Generic event channel 11 selected	1 : 1
12	Generic event channel 12 selected	1 : 2 (splitter)
13	Generic event channel 13 selected	1 : 2 (splitter)
14	Generic event channel 14 selected	1 : 2 (splitter)
15	Generic event channel 15 selected	1 : 2 (splitter)

8.8 Memory

8.8.1 Memory Organization

Table 8-5 summarizes the memory map of the devices. For more information about the memory region detail, see the *Platform Memory Map* section in the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual* .

Table 8-5. Memory Organization - MSPM0Gx218 and MSPM0Gx207

MEMORY REGION	SUBREGION	MSPM0G3207, MSPM0G1207	MSPM0G3218, MSPM0G1218
Code (Flash Bank 0)	MAIN ECC Corrected	128KB	256KB
		0x0000.0000 to 0x0000.FFFF	0x0000.0000 to 0x0001.FFFF
	MAIN ECC Uncorrected	0x0040.0000 to 0x0040.FFFF	0x0040.0000 to 0x0041.FFFF
	Flash ECC code	0x4180.0000 to 0x4180.FFFF	0x4180.0000 to 0x4181.FFFF
Code (Flash Bank 1)	MAIN ECC Corrected	128KB	256KB
		0x0001.0000 to 0x0001.FFFF	0x0002.0000 to 0x0003.FFFF
	MAIN ECC Uncorrected	0x0041.0000 to 0x0041.FFFF	0x0042.0000 to 0x0043.FFFF
	Flash ECC code	0x4181.0000 to 0x4181.FFFF	0x4182.0000 to 0x4183.FFFF
Data Flash Bank	Data Flash ECC Corrected	16KB	16KB
		0x41D0.0000 to 0x41D0.1FFF	0x41D0.0000 to 0x41D0.1FFF
	Data Flash Unchecked	0x41E0.0000 to 0x41E0.1FFF	0x41E0.0000 to 0x41E0.1FFF
	Data Flash ECC code	0x41F0.0000 to 0x41F0.1FFF	0x41F0.0000 to 0x41F0.1FFF
SRAM	SRAM ECC Corrected	32KB	32KB
		0x2000.0000 to 0x2000.7FFF	0x2000.0000 to 0x2000.7FFF
	SRAM ECC code	0x2030.0000 to 0x2030.7FFF	0x2030.0000 to 0x2030.7FFF

Table 8-5. Memory Organization - MSPM0Gx218 and MSPM0Gx207 (continued)

MEMORY REGION	SUBREGION	MSPM0G3207, MSPM0G1207	MSPM0G3218, MSPM0G1218
Peripheral	Peripherals	0x4000.0000 to 0x40FF.FFFF	0x4000.0000 to 0x40FF.FFFF
	NONMAIN Corrected	2KB	2KB
		0x41C0.0000 to 0x41C0.07FF	0x41C0.0000 to 0x41C0.07FF
	NONMAIN Uncorrected	0x41C1.0000 to 0x41C1.07FF	0x41C1.0000 to 0x41C1.07FF
	NONMAIN ECC code	0x41C2.0000 to 0x41C2.07FF	0x41C2.0000 to 0x41C2.07FF
	FACTORY Corrected	512Bytes	512Bytes
		0x41C4.0000 to 0x41C4.01FF	0x41C4.0000 to 0x41C4.01FF
	FACTORY Uncorrected	0x41C5.0000 to 0x41C5.01FF	0x41C5.0000 to 0x41C5.01FF
	FACTORY ECC code	0x41C6.0000 to 0x41C6.01FF	0x41C6.0000 to 0x41C6.01FF
Subsystem		0x6000.0000 to 0x7FFF.FFFF	0x6000.0000 to 0x7FFF.FFFF
System PPB		0xE000.0000 to 0xE00F.FFFF	0xE000.0000 to 0xE00F.FFFF

8.8.2 Peripherals Summary

Table 8-6 lists the available peripherals and the register base address for each.

Table 8-6. Peripherals Summary

Peripheral name	Base Address	Size
ADC0	0x40004000	0x00002000
ADC1	0x40006000	0x00002000
COMP0	0x40008000	0x00001F00
COMP1	0x4000A000	0x00001F00
VREF	0x40030000	0x00001F00
WWDT0	0x40080000	0x00001500
WWDT1	0x40082000	0x00001500
TIMG0	0x40084000	0x00001F00
TIMG8	0x40090000	0x00001F00
LFSS	0x40094000	0x00001600
TIMG14	0x40096000	0x00001F00
GPIOA	0x400A0000	0x00001F00
GPIOB	0x400A2000	0x00001F00
KEYSTORECTL	0x400AC000	0x00002000
SYSCTL	0x400AF000	0x00003100
TIMB0	0x400B8000	0x00001C00
TIMB1	0x400BA000	0x00001C00
TIMB2	0x400BC000	0x00001C00
DEBUGSS	0x400C7000	0x00001F00
EVENTLP	0x400C9000	0x00003000
FLASHCTL	0x400CD000	0x00002000
CPUSS	0x40400000	0x00001F00
MATHACL	0x40410000	0x00001500
WUC	0x40424000	0x00000500
IOMUX	0x40428000	0x00002000
DMA	0x4042A000	0x00001F00
CRCP0	0x40440000	0x00002000

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Table 8-6. Peripherals Summary (continued)

Peripheral name	Base Address	Size
AESADVHP	0x40442000	0x00001200
TRNG	0x40444000	0x00001E00
CANFD0	0x40508000	0x00008000
ADC0_SVT	0x4055A000	0x00001000
ADC1_SVT	0x4055C000	0x00001000
TIMA0	0x40860000	0x00001F00
TIMG12	0x40870000	0x00001F00
UC0_0_UART	0x40A04000	0x00005500
UC0_1_UART	0x40A06000	0x00007500
UC5_UART	0x40A08000	0x00009500
UC0_0_I2CC	0x40A24000	0x00025500
UC0_1_I2CC	0x40A26000	0x00027500
UC5_I2CC	0x40A28000	0x00029500
UC0_0_I2CT	0x40A44000	0x00045500
UC0_1_I2CT	0x40A46000	0x00047500
UC5_I2CT	0x40A48000	0x00049500
UC0_0	0x40A84000	0x00085C00
UC0_1	0x40A86000	0x00087C00
UC5	0x40A88000	0x00089C00
SPG0	0x40A9F000	0x000A0C00
S1U0_UART	0x40B00000	0x00001500
S1U1_UART	0x40B02000	0x00003500
S1U0_SPI	0x40B60000	0x00061200
S1U1_SPI	0x40B62000	0x00063200
S1U2_SPI	0x40B64000	0x00065200
S1U0	0x40B80000	0x00081C00
S1U1	0x40B82000	0x00083C00
S1U2	0x40B84000	0x00084A00

8.8.3 Peripheral Interrupt Vector

Table 8-7 shows the IRQ number and the interrupt group number for each periperals in this device.

Table 8-7. Interrupt vector number

Peripheral Name	NVIC IRQ	Group IIDX
WWDT0	0	0
WWDT1	0	1
DEBUGSS	0	2
FLASHCTL	0	3
EVENT SUB PORT 0	0	4
EVENT SUB PORT 1	0	5
SYSCTL	0	6
GPIOA	1	0
GPIOB	1	1
COMP0	1	2
COMP1	1	3
TIMG8	2	-
ADC0	4	-
ADC1	5	-
CANFD0	6	-
S1U2	9	-
S1U0	13	-
S0U2	15	-
TIMG0	16	-
TIMA0	18	-
TIMA1	19	-
TIMB0	20	-
TIMB1	21	-
TIMG1	22	-
S0U3	24	-
S0U4	25	-
AESADV	28	-
RTC_B	30	-
DMA0	31	-

8.9 Flash Memory

A dual bank of non-volatile flash memory (up to 256kB total) and a separate data flash bank (8kB in MSPM0Gx218 and MSPM0Gx207) is provided for storing executable program code and application data.

Key features of the flash include:

- Hardware ECC protection (encode and decode) with single bit error correction and double bit error detection
- In-circuit program and erase operations supported across the entire recommended supply range
- Small 1kB sector sizes (minimum erase resolution of 1kB)
- Up to 100,000 program/erase cycles on the 32 selected sectors of the flash memory, with up to 10,000 program/erase cycles on the remaining flash memory (devices with 32kB support 100,000 cycles on the entire flash memory)
- Bank address swap for in-system, over-the-air (OTA) firmware updates

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For a complete description of the flash memory, see the NVM chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.10 SRAM

MSPM0 MCUs include a low power, high performance SRAM memory with zero wait state access across the supported CPU frequency range of the device. MSPM0 MCUs also provides up to 32KB SRAM with hardware ECC or parity. SRAM memory may be used for storing volatile information such as the call stack, heap, global data, and code. The SRAM memory content is fully retained in RUN, SLEEP, STOP, and STANDBY operating modes and is lost in SHUTDOWN mode.

A write-execute mutual exclusion mechanism is provided to allow the application to partition the SRAM into two sections: aread-write (RW) partitions and a read-execute (RX) partition. The RW partition occupies the lower portion of SRAM address space, while the RX partition occupies the upper portion of the SRAM address space. The SRAMBOUNDARY register in SYSCTL needs to be configured to set up these partitions. Write protection is useful when placing executable code into SRAM as it provides a level of protection against unintentional overwrites of code by either the CPU or DMA. Placing code in SRAM can improve performance of critical loops by enabling zero wait state operation and lower power consumption. Preventing code execution from the RW partition improves security by preventing self-modifying code execution ability.

8.11 GPIO

The general purpose input/output (GPIO) peripheral provides the user with a means to write data out and read data in to and from the device pins. Through the use of the Port A and Port B GPIO peripherals, these devices support up to 60 GPIO pins.

The key features of the GPIO module include:
- 0 wait state MMR access from CPU
- Set/Clear/Toggle multiple bits without the need of a read-modify-write construct in software
- GPIOs with "Standard with Wake" drive functionality able to wake the device from SHUTDOWN mode
- User controlled input filtering
- GPIO "FastWake" feature enables low-power wakeup from STOP and STANDBY modes for any GPIO port

For more details, see the GPIO chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.12 IOMUX

The IOMUX peripheral enables IO pad configuration and controls digital data flow to and from the device pins. The key features of the IOMUX include:
- IO Pad configuration registers allow for programmable drive strength, speed, pullup-down, and more
- Digital pin muxing allows for multiple peripheral signals to be routed to the same IO pad
- Pin functions and capabilities are user-configured using the PINCM register

For more details, see the IOMUX chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.13 ADC

Both 12-bit analog-to-digital converter (ADC) modules in these devices, ADC0 and ADC1, support fast 12-bit conversions with single-ended inputs and simultaneous sampling operation.

ADC features include:
- 12-bit output resolution at 1.6Msps
- HW averaging enables 14-bit effective resolution at 100ksps
- Up to 27 total external input channels
- 24 individual result storage registers (12 per ADC instance)
- Internal channels for temperature sensing and supply monitoring
- Software selectable reference:

- Configurable internal shared reference voltage (VREF1) of 1.4V and 2.5V (requires decoupling capacitor on VREF+/- pins) to support 1.6Msps
- Configurable internal only reference voltage (VREF2) of 1.4V and 2.5V to support 0.9Msps
- MCU supply voltage (VDD)
- External reference supplied to the ADC through the VREF+/- pins
- Operates in RUN, SLEEP, and STOP modes

Table 8-8 shows the ADC channel mapping in the device.

Table 8-8. ADC Channel Mapping

CHANNEL[0:8]	SIGNAL NAME(2)		CHANNEL[9:14,30,31]	SIGNAL NAME(1) (2)	
	ADC0	ADC1		ADC0	ADC1
0	A0_0	A1_0	9	A0_9	-
1	A0_1	A1_1	10	-	A1_10
2	A0_2	A1_2	11	*Temperature Sensor*	A1_11
3	A0_3	A1_3	12	A0_12	A1_12
4	A0_4	A1_4	13	A0_13	A1_13
5	A0_5	A1_5	14	A0_14	A1_14
6	A0_6	A1_6	30	VREF1	VREF2
7	A0_7	A1_7	31	*Supply/Battery Monitor*	*Supply/Battery Monitor*
8	A0_8	A1_8			

(1) *Italicized* signal names are purely internal to the device. These signals are used for internal peripheral interconnections.
(2) For more information about device analog connections please refer to *Device Analog Connections*

For more details, see the ADC chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.14 Temperature Sensor

The temperature sensor provides a voltage output that changes linearly with device temperature. The temperature sensor output is internally connected to one of ADC input channels to enable a temperature-to-digital conversion.

A unit-specific single-point calibration value for the temperature sensor is provided in the factory constants memory region. This calibration value represents the ADC conversion result (in ADC code format) corresponding to the temperature sensor being measured in 12-bit mode with the 1.4-V internal VREF at the factory trim temperature (TS_{TRIM}).

The ADC and VREF configuration for the above measurement is as the following: RES=0 (12-bit mode), VRSEL=2h (Internal reference), BUFCONFIG=1h (1.4V VREF), ADC t_{Sample}=10µs. This calibration value can be used with the temperature sensor temperature coefficient (TS_c) to estimate the device temperature.

See the temperature sensor section of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual* for guidance on estimating the device temperature with the factory trim value.

8.15 VREF

The shared voltage reference modules (VREF1 and VREF2) in these devices contain a configurable voltage reference buffer which allows users to supply a stable reference to on-board analog peripherals. It also supports bringing in an external reference for applications where higher accuracy is required.

VREF1 features include:

- 1.4V and 2.5V user-selectable internal references
- Internal reference supports full speed ADC operation at 1.6Msps

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- Support for comparator operation
- Support for bringing in an external reference on VREF+/- device pins
- Requires a decoupling capacitor placed on VREF+/- pins for proper operation. See *VREF* for more details.

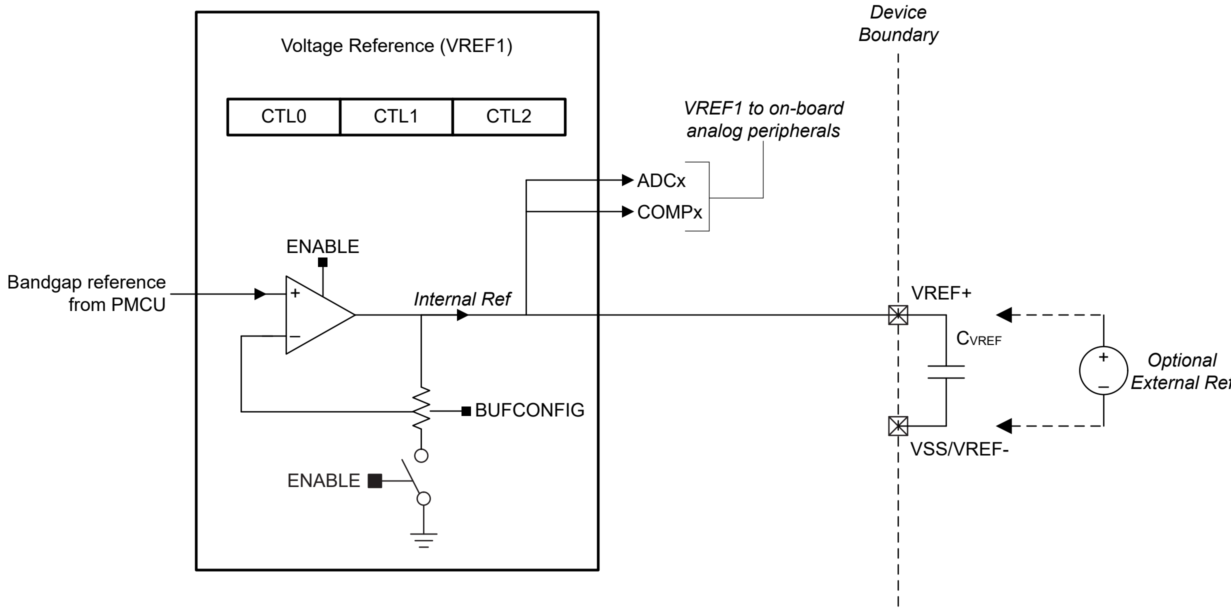

Figure 8-5. VREF1 module

VREF2 (VREFINT) features include:

- 1.4V and 2.5V user-selectable internal references
- Internal reference supports reduced speed ADC operation at 0.9Msps
- Does not require a decoupling capacitor placed on VREF+/- pins for proper operation.

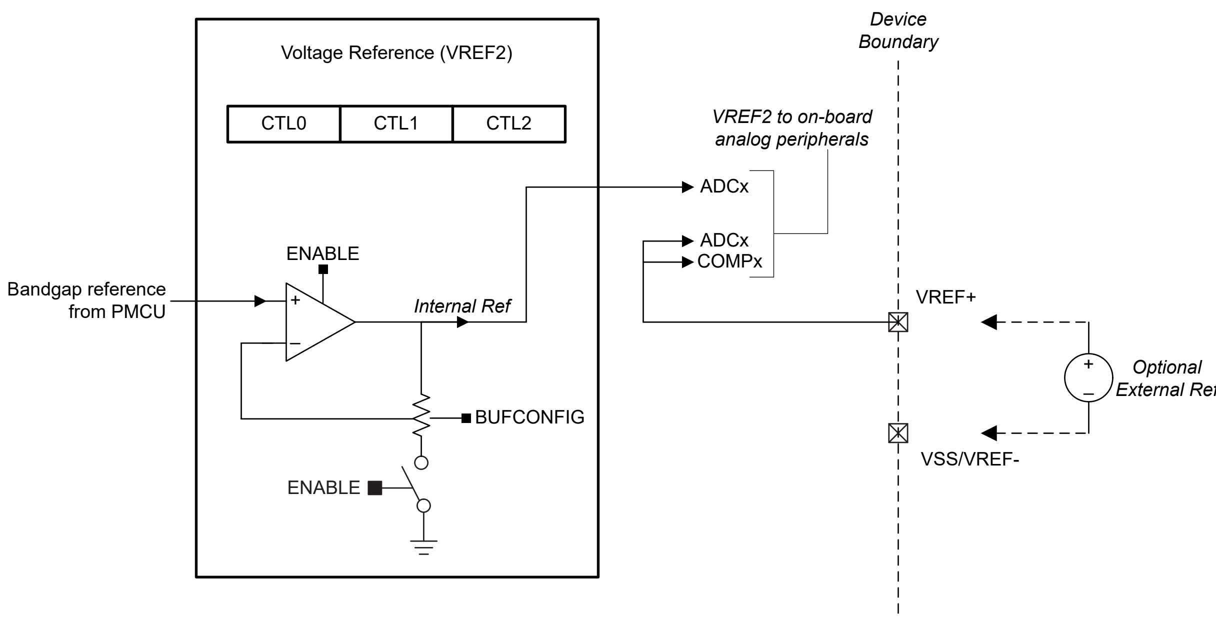

Figure 8-6. VREF2 (VREFINT) module

For more details, see the VREF chapter of the *MSPM0 G-Series 80-MHz Microcontrollers Technical Reference Manual*.

8.16 COMP

The comparator peripheral in the device compares the voltage levels on two inputs terminals and provides a digital output based on this comparison. It supports the following key features:

- Programmable hysteresis
- Programmable reference voltage:
  - External reference voltage (VREF IO)
  - Internal reference voltage (1.4V, 2.5V)
- Pin Feature:
  - Integrated 8-bit reference DAC

    Can be output with DACOUT signal
- Configurable operation modes:
  - High-speed mode
  - Low-power mode
- Programmable output glitch filter delay
- Supports 6 blanking sources from TIMx instances (see Table 8-9)
- Device wakeup from all low power modes using comparator output
- Output connected to advanced timer fault handling mechanism
- Selection of comparator channel inputs from device pins or internal analog module (see Table 8-10 and Table 8-11.)

Table 8-9. COMP Blanking Source Table

CTL2.BLANKSRC	BLANKING SOURCE
1	TIMA0.CC2
2	TIMA0.CC3
3	TIMA1.CC1
4	TIMG0.CC1
5	TIMG1.CC1
6	TIMG8.CC1

Table 8-10. COMP0 Input Channel Selection

IPSEL / IMSEL BITS	POSITIVE TERMINAL INPUT	NEGATIVE TERMINAL INPUT
0x0	COMP0_IN0+	COMP0_IN0-
0x1	COMP0_IN1+	COMP0_IN1-
0x2	COMP0_IN2+	COMP0_IN2-
0x3	COMP0_IN3+	-
0x5	-	Temperature Sensor
0x7	COMP1 positive terminal signal	-

Table 8-11. COMP1 Input Channel Selection

IPSEL / IMSEL BITS	POSITIVE TERMINAL INPUT	NEGATIVE TERMINAL INPUT
0x0	COMP1_IN0+	COMP1_IN0-
0x1	COMP1_IN1+	COMP1_IN1- / VREF+
0x2	COMP1_IN2+	COMP1_IN2-
0x3	COMP1_IN3+	-
0x7	COMP0 positive terminal signal	-

For more information about device analog connections, see *Device Analog Connections*.

For more details, see the COMP chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.17 Security

This device offers several security features, including:

- Debug security
- Device identify
- AES-128/256 accelerator with support for GCM/GMAC, CCM/CBC-MAC, CBC, CTR
- Flexible firewalls for protecting code and data
  - Flash write-erase protection
  - Flash read-execute protection
  - Flash IP protection
  - SRAM write-execute mutual exclusion
- Secure boot
- Secure firmware update
- Secure key storage for up to four AES keys
- Customer secure code
- Hardware monotonic counter
- Cyclic redundancy checker (CRC-16, CRC-32) with support for custom polynomial

For more details, see the Security chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.18 AESADV

The AES advanced (AESADV) accelerator module performs encryption and decryption of 128-bit data blocks with a 128-bit or 256-bit key in hardware according to the advanced encryption standard (AES). AES is a symmetric-key block cipher algorithm specified in FIPS PUB 197.

The AESADV accelerator features include:

- AES operation with 128-bit and 256-bit keys
- Key scheduling in hardware
- Enc/decrypt only modes: CBC, CFB-1, CFB-8, CFB-128, OFB-128, CTR/ICM
- Authentication only modes: CBC-MAC, CMAC
- AES-CCM
- AES-GCM
- AES-CCM and AES-GCM modes support continuation with hold/resume of payload data
- 32-bit word access to provide key data, input data, and output data
- AESADV ready interrupt
- DMA triggers for input/output data
- Supported in RUN and SLEEP (see the *Operating Modes* section of the device technical reference manual)

For more details, see the AESADV chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.19 Keystore

The Keystore controller provides secure management of the Advanced Encryption Engine (AES) keys. The use-model of the keystore controller is to securely deposit keys into it during the execution of customer secure code, and have the AES engine access them subsequently in a secure manner without leaking any key data to observers. Both 128 and 256-bit keys can be stored in the keystore's key slots. The keystore and its interaction with the AES engine are designed for secure operation including thwarting partial key modification attacks.

- Support for storage of up to 4 keys

For more details, see the KEYSTORE chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.20 CRC-P

The cyclical redundancy check (CRC) module provides a signature for an input data sequence. Key features of the CRC module include:

- Support for 16-bit CRC based on CRC16-CCITT
- Support for 32-bit CRC based on CRC32-ISO3309
- Support for bit reversal
- Support for custom polynomials

For more details, see the CRC chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.21 MATHACL

The math accelerator (MATHACL) is a collection of hardware accelerated 32-bit math functions to improve system computational throughput. The MATHACL offloads mathematical calculations performed by the CPU to improve efficiency and CoreMark performance.

The following hardware functions are available in the MATHACL:

- Sine/Cosine (SINCOS)
- Arc tangent (ATAN2)
- Square root (SQRT)
- Division (DIV)
- Multiply with 32-bit result (MPY32)
- Square with 32-bit result (SQUARE32)
- Multiply with 64-bit result (MPY64)
- Square with 64-bit result (SQUARE64)
- Multiply-accumulate (MAC)
- Square-accumulate (SAC)

For more details, see the MATHACL chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.22 UNICOMM (UART/SPI/I2C)

UNICOMM is a highly flexible peripheral which can be configured as a UART, SPI, I^{2}C-Controller or I^{2}C-Target function. The user can select one of the serial interfaces before configuration and data transfer. The peripheral uses a common FIFO per instance to maximize the device capability based on the operating state. A serial peripheral group combines one or more UNICOMM for special functions like I^{2}C loopback and is an optional configuration. Table 8-12 describes the grouping of UNICOMM, peripheral serial interfaces available and FIFO depth.

Table 8-12. UNICOMM (UCx) Serial Peripheral

UNICOMM INSTANCE	SERIAL PERIPHERAL GROUP	UART	I^{2}C Controller	I^{2}C Target	SPI	FIFO depth
UC0	SPG0 (PD0)	ADV	ADV	ADV	-	4
UC4		ADV	-	-	Basic	4
UC5		Min + LIN	ADV	ADV		4
UC2	SPG1 (PD1)	-	-	-	ADV	4
UC9		Min + LIN	-	-	-	4

For more details, see the UNICOMM chapter of the *MSPM0 G-Series 80-MHz Microcontrollers Technical Reference Manual*.

8.22.1 UART (UNICOMM)

The UNICOMM-UART peripheral function provide the following key features:

- Standard asynchronous communication bits for start, stop, and parity
- Fully programmable serial interface
  - 5, 6, 7 or 8 data bits
  - Even, odd, stick, or no-parity bit generation and detection
  - 1 or 2 stop bit generation
  - LSB-first or MSB-first data transmit and receive
  - Line-break detection
  - Programmable baud rate generation with oversampling by 16, 8 or 3
- Support for waking up SYSOSC via an asynchronous fast clock request upon start bit detection when operating in low power modes
- Support transmit and receive loopback mode operation
- See Table 8-13 for detail information on supported protocols and features

Table 8-13. UNICOMM-UART feature support

UNICOMM-UART Features		(Advanced)	(Basic w/ LIN)
Feature Tag	**Feature Description**	**UC0, UC4**	**UC5, UC9**
-	Active in Stop and Standby Mode	Yes	Yes
UART-RX-TIMEOUT	Receive timeout and Line timeout	Yes	Yes
UART-IDLELINE-MULTIPROC	Idle-Line Multiprocessor	Yes	Yes
UART-FLOW-CONTROL	Flow control (CTS/RTS) with support for RS-485	Yes	Yes
UART-MULTIDROP-9-BIT	9-bit UART mode for multidrop systems with addressable peripherals	Yes	Yes
UART-EXT-DRIVER	External driver output enable	Yes	-
UART-SMARTCARD	ISO7816 smart card mode	Yes	-
UART-LIN	Local Interconnect Network (LIN)	Yes	Yes
UART-DALI-MANCHESTER	IEC62386 Digital Addressable Lighting Interface (DALI)	Yes	-
UART-IRDA	IrDA encoding and decoding	Yes	-
UART-FIFO	RX and TX FIFO	4	4
UART-DMA	Direct memory access (DMA)	Yes	Yes

For more details, see the UART (UNICOMM) chapter of the *MSPM0 G-Series 80-MHz Microcontrollers Technical Reference Manual*.

8.22.2 I2C (UNICOMM)

The inter-integrated circuit interface (I^2C) peripherals in these devices provide bidirectional data transfer with other I2C devices on the bus and support the following key features:

- 7-bit and 10-bit addressing mode with multiple 7-bit target addresses
- Multiple-controller transmitter or receiver mode
- Target receiver or transmitter mode with configurable clock stretching
- Support Standard-mode (Sm), with a bit rate up to 100 kbit/s
- Support Fast-mode (Fm), with a bit rate up to 400 kbit/s
- Support Fast-mode Plus (Fm+), with a bit rate up to 1 Mbit/s
  - Supported on open drain IOs (ODIO) and high-drive (HDIO) IOs only
- Separated transmit and receive FIFOs support DMA data transfer
- Support SMBus 3.0 with PEC, ARP, timeout detection and host support
- Wakeup from low power mode on address match
- Support analog glitch filter for input signal glitch suppression
- 4-entry transmit and receive FIFOs

- See Table 8-14 and Table 8-15 for detailed information on supported features for controller and target functions

Table 8-14. I2C Controller (UNICOMM) Features

Supported Features	(Advanced)
UNICOMM Instance	**UC0, UC5**
Supports standard-mode (Sm)	Yes
Supports Fast-mode (Fm)	Yes
Supports Fast-mode Plus (Fm+)	Yes
Supports analog glitch filter	Yes
Supports digital glitch filter	-
Supports burst mode	Yes
Supports SMBus mode	Yes

Table 8-15. I2C Target (UNICOMM) Features

Supported Features	(Advanced)
UNICOMM Instance	**UC0, UC5**
Supports standard-mode (Sm)	Yes
Supports Fast-mode (Fm)	Yes
Supports Fast-mode Plus (Fm+)	Yes
Supports analog glitch filter	Yes
Supports digital glitch filter	-
Supports second target address & mask	Yes
Supports SMBus mode	Yes
Supports low power wakeup	Yes

For more details, see the I2C (UNICOMM) chapter of the *MSPM0 G-Series 80-MHz Microcontrollers Technical Reference Manual*.

8.22.3 SPI (UNICOMM)

The serial peripheral interface (SPI) peripherals in these devices support the following key features:

- Support ULPCLK/2 bit rate and up to 32Mbits/s in both controller and peripheral mode [1]
- Configurable as a controller or a peripheral
- Support for up to 4 chip select for both controller and peripheral
- Supports single parity for transmit and receive
- Programmable clock prescaler and bit rate
- Programmable data frame size from 4 bits to 16 bits (controller mode) and 7 bits to 16 bit (peripheral mode)
- Transmit and receive FIFOs (4 entries each with 16 bits per entry) supporting DMA data transfer
- Supports TI mode and Motorola mode
- Support single bit parity in both transmit and receive paths
- See Table 8-16 for detailed information on supported features

[1] Only SPI signals on HSIO pins support data rate > 16 Mbits/s; see *Pin Diagrams* for HSIO pins.

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Table 8-16. SPI (UNICOMM) Features

SPI Features	(Advanced)	SPI1 (Basic)
UNICOMM Instance	UC2	UC4
Controller and Peripheral mode	Yes	Yes
Supports Parity function	Yes	Yes
Supports Repeat mode transfer	Yes	-
Supports Receive timeout	Yes	-
Supports Command/Data control	Yes	-
Supports 4 chip selects	Yes	-

For more details, see the SPI (UNICOMM) chapter of the *MSPM0 G-Series 80-MHz Microcontrollers Technical Reference Manual*.

8.23 UART

The UART peripherals (UART0-UART1, UART3-UART7) provide the following key features:

- Standard asynchronous communication bits for start, stop, and parity
- Fully programmable serial interface
  - 5, 6, 7 or 8 data bits
  - Even, odd, stick, or no-parity -bit generation and detection
  - 1 or 2 stop bit generation
  - Line-break detection
  - Glitch filter on the input signals
  - Programmable baud rate generation with oversampling by 16, 8 or 3
  - Local Interconnect Network (LIN) mode support
- Separated transmit and receive FIFOs support DAM data transfer
- Support transmit and receive loopback mode operation
- See Table 8-17 for detail information on supported protocols

Table 8-17. UART Features

UART Features	UART0, UART7 (Extend, low-power)	UART1 (Main, low-power)	UART3-UART6 (Main)
Active in Stop and Standby Mode	Yes	Yes	-
Separate transmit and receive FIFOs	Yes	Yes	Yes
Support hardware flow control	Yes	Yes	Yes
Support 9-bit configuration	Yes	Yes	Yes
Support LIN mode	Yes	-	-
Support DALI	Yes	-	-
Support IrDA	Yes	-	-
Support ISO7816 Smart Card	Yes	-	-
Support Manchester coding	Yes	-	-

For more details, see the UART chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.24 I2C

The inter-integrated circuit interface (I^{2}C) peripherals in these devices provide bidirectional data transfer with other I2C devices on the bus and support the following key features:

- 7-bit and 10-bit addressing mode with multiple 7-bit target addresses
- Multiple-controller transmitter or receiver mode

- Target receiver or transmitter mode with configurable clock stretching
- Support Standard-mode (Sm), with a bit rate up to 100 kbit/s
- Support Fast-mode (Fm), with a bit rate up to 400 kbit/s
- Support Fast-mode Plus (Fm+), with a bit rate up to 1 Mbit/s
  - Supported on open drain IOs (ODIO) and high-drive (HDIO) IOs only
- Separated transmit and receive FIFOs support DMA data transfer
- Support SMBus 3.0 with PEC, ARP, timeout detection and host support
- Wakeup from low power mode on address match
- 4-entry transmit and receive FIFOs

For more details, see the I2C chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.25 SPI

The serial peripheral interface (SPI) peripherals in these devices support the following key features:

- Support MCLK/2 bit rate and up to 32Mbits/s in both controller and peripheral mode[2]
- Configurable as a controller or a peripheral
- Configurable chip select for both controller and peripheral
- Programmable clock prescaler and bit rate
- Programmable data frame size from 4 bits to 16 bits (controller mode) and 7 bits to 16 bit(peripheral mode)
- Supports PACKEN feature that allows the packing of 2 16 bit FIFO entries into a 32-bitvalue to improve CPU performance
- Transmit and receive FIFOs (4 entries each with 16 bits per entry) supporting DMA data transfer
- Supports TI mode, Motorola mode and National Microwire format

For more details, see the SPI chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.26 CAN-FD

The controller area network (CAN) controller enables communication with a CAN2.0A, CAN2.0B, or CAN-FD bus and is compliant to ISO 11898-1:2015 standard supporting up to 5M bit/s bit rate. Key features of the CAN-FD peripheral include:

- Full support for 64-byte CAN-FD frames
- Dedicated 1kB message SRAM with ECC
- Configurable transmit FIFO, transmit queue and event FIFO (up to 32 elements)
- Up to 32 dedicated transmit buffers and 64 dedicated receive buffers
- Two configurable receive FIFOs (up to 64 elements each)
- Up to 128 filter elements
- Two interrupt lines
- Power-down and wake-up support
- Timestamp counter

For more details, see the CAN-FD chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.27 Low-Frequency Sub System (LFSS)

The Low-Frequency Sub-System (LFSS) is a sub-system which combines several functional peripherals under one shared subsystem. These peripherals are clocked by the low freqency clock (LFCLK) or need to be active during low power modes. The LFCLK has a typical frequency of 32kHz and is mainly intended for long-term timekeeping.

LFSS_B is the specific LFSS variant in this device and contains the following components:

- Real-time clock (RTC_B) with additional prescalar extension and timestamp captures
- An asynchronous Independent Watchdog Timer (IWDT)

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[2] Only SPI signals on HSIO pins support data rate > 16 Mbits/s; see *Pin Diagrams* for HSIO pins.

For more details, see the LFSS chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.28 RTC_B

The RTC_B instance of the real-time clock operates off of a 32kHz input clock source (typically a low frequency crystal) and provides a time base to the application with multiple options for interrupts to the CPU. The RTC_B provides common key features in relation to the Low-Frequency Sub System (LFSS).

Common key features of the RTC_B include:

- Counters for seconds, minutes, hours, day of the week, day of the month, month, and year
- Binary or BCD format
- Leap-year handling
- One customizable alarm interrupt based on minute, hour, day of the week, and day of the month
- Interval alarm interrupt to wake every minute, every hour, at midnight, or at noon
- Interval alarm interrupt providing periodic wake-up at 4096, 2048, 1024, 512, 256, or 128 Hz
- Interval alarm interrupt providing periodic wake-up at 64, 32, 16, 8, 4, 2, 1, and 0.5 Hz
- Calibration for crystal offset error (up to +/- 240ppm)
- Compensation for temperature drift (up to +/- 240ppm)
- RTC clock output to pin for calibration

Table 8-18 shows the RTC features supported in this device.

Table 8-18. RTC_B Key Features

RTC Features	RTC_B
Power enable register	-
Real-time clock and calendar mode providing seconds, minutes, hours, day of week, day of month, and year	Yes
Selectable binary or binary-coded decimal (BCD) format	Yes
Leap-year correction (valid for year 1901 through 2099)	Yes
Two customizable calendar alarm interrupts based on minute, hour, day of the week, and day of the month	Yes
Interval alarm interrupt to wake every minute, every hour, at midnight, or at noon	Yes
Periodic interrupt to wake at 4096, 2048, 1024, 512, 256, or 128Hz	Yes
Periodic interrupt to wake at 64, 32, 16, 8, 4, 2, 1, and 0.5Hz	Yes
Interrupt capability down to STANDBY mode with STOPCLKSTBY	Yes
Calibration for crystal offset error and crystal temperature drift (up to ±240 ppm total)	Yes
RTC clock output to pin for calibration (GPIO)	Yes
RTC clock output to pin for calibration (TIO)	-
Three -bit prescaler for heartbeat function with interrupt generation	-
RTC external clock selection of untrimmed 32kHz, trimmed 512Hz, 256Hz or 1Hz	-
RTC time stamp capture upon detection of a timer stamp event, including: • TIO event • VDD fail event	-
RTC counter lock function	-

For more details, see the RTC chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.29 IWDT_B

The independent watchdog timer (IWDT) in the LFSS is a device-independent supervisor which monitors code execution and overall hang up scenarios of the device. Due to the nature of LFSS, this IWDT has its own system independent clock source. If the application software does not successfully reset the watchdog within the programmed time, the watchdog generates a POR reset to the device.

Key features of the IWDT include:

- A 25-bit counter
- Counter driven from LFOSC (fixed 32kHz clock path) with a programmable clock divider
- Eight selectable watchdog timer periods (2ms to 2hr)

For more details, see the IWDT chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.30 WWDT

The windowed watchdog timer (WWDT) can be used to supervise the operation of the device, specifically code execution. The WWDT can be used to generate a reset or an interrupt if the application software does not successfully reset the watchdog within a specified window of time. Key features of the WWDT include:

- 25-bit counter
- Programmable clock divider
- Eight software selectable watchdog timer periods
- Eight software selectable window sizes
- Support for stopping the WWDT automatically when entering a sleep mode
- Interval timer mode for applications which do not require watchdog functionality

For more details, see the WWDT chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.31 Timers (TIMx)

There are two types of timer peripherals in these devices support that following key features: TIMGx (general-purpose timer) and TIMAx (advanced timer). TIMGx is a subset of TIMAx, which means common features between timer instances are software compatible. For specific configurations, see Table 8-19:

Specific features for the general-purpose timer **(TIMGx)** include:

- 16-/32-bit up, down, up-down or down-up counter, with repeat-reload mode
- Selectable and configurable clock source
- 8-bit programmable prescaler to divide the counter clock frequency
- Two independent channels for
  - Output compare
  - Input capture
  - PWM output
  - One-shot mode
- Support quadrature encoder interface (QEI) and Hall sensor input logic available in TIMG8
- Support synchronization and cross trigger among different TIMx instances in the same power domain
- Support interrupt/DMA trigger generation and cross peripherals (such as ADC) trigger capability

Specific features for the advanced timer **(TIMAx)** include:

- 16-bit down or up-down counter, with repeat-reload mode
- Selectable and configurable clock source
- 8-bit programmable prescaler to divide the counter clock frequency
- Repeat counter to generate an interrupt or event only after a given number of cycles of the counter

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- Up to four independent channels for
  - Output compare
  - Input capture
  - PWM output
  - One-shot mode
- Shadow register for load and CC register available in both TIMA0 and TIMA1
- Complementary output PWM with programmable dead band insertion
- Asymmetric PWM
- Configurable fault handling mechanism for
  - Fast PWM responses (<40ns) to external fault inputs or comparator events
  - Outputting signals in a safe user-defined state when a latched fault condition has occurred
- Support synchronization and cross trigger among different TIMx instances in the same power domain
- Support interrupt and DMA trigger generation and cross peripherals (such as ADC) trigger capability
- Two additional capture/compare channels for internal events

Table 8-19. TIMx Configurations

TIMER NAME	POWER DOMAIN	RESOLUTION	PRESCALER	REPEAT COUNTER	CAPTURE / COMPARE CHANNELS	PHASE LOAD	SHADOW LOAD	SHADOW CC	DEADBAND	FAULT	QEI
TIMG0	PD0	16 bit	8 bit	–	2	–	–	–	–	–	–
TIMG1	PD0	16 bit	8 bit	-	2	-	-	-	-	-	-
TIMG8	PD0	16 bit	8 bit	–	2	–	–	–	–	–	Yes
TIMA0	PD1	16 bit	8 bit	8 bit	4	Yes	Yes	Yes	Yes	Yes	–
TIMA1	PD1	16 bit	8 bit	8 bit	2	Yes	Yes	Yes	Yes	Yes	–

Table 8-20. TIMx Cross Trigger Map (PD1)

TSEL.ETSEL Selection	TIMA0	TIMA1
0	TIMA0.TRIG0	TIMA0.TRIG0
1	TIMA1.TRIG0	TIMA1.TRIG0
2	TIMG8.TRIG0	TIMG8.TRIG0

Table 8-21. TIMx Cross Trigger Map (PD0)

TSEL.ETSEL Selection	TIMG0	TIMG1	TIMG8
0	TIMG0.TRIG0	TIMG0.TRIG0	TIMG0.TRIG0
1	TIMG1.TRUG0	TIMG1.TRIG0	TIMG1.TRIG0
2	TIMG8.TRIG0	TIMG8.TRIG0	TIMG8.TRIG0

For more details, see the TIMx chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.32 Input/Output Diagrams

The IOMUX manages the selection of which peripheral function is to be used on a digital IO. It also provides the controls for the output driver, input path, and the wake-up logic for wakeup from SHUTDOWN mode. For more information, refer to the IOMUX section of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

The mixed-signal IO pin slice diagram for a full featured IO pin is shown in Figure 8-7. Not all pins will have analog functions, wake-up logic, drive strength control, and pullup or pulldown resistors available. See the device-specific data sheet for detailed information on what features are supported for a specific pin.

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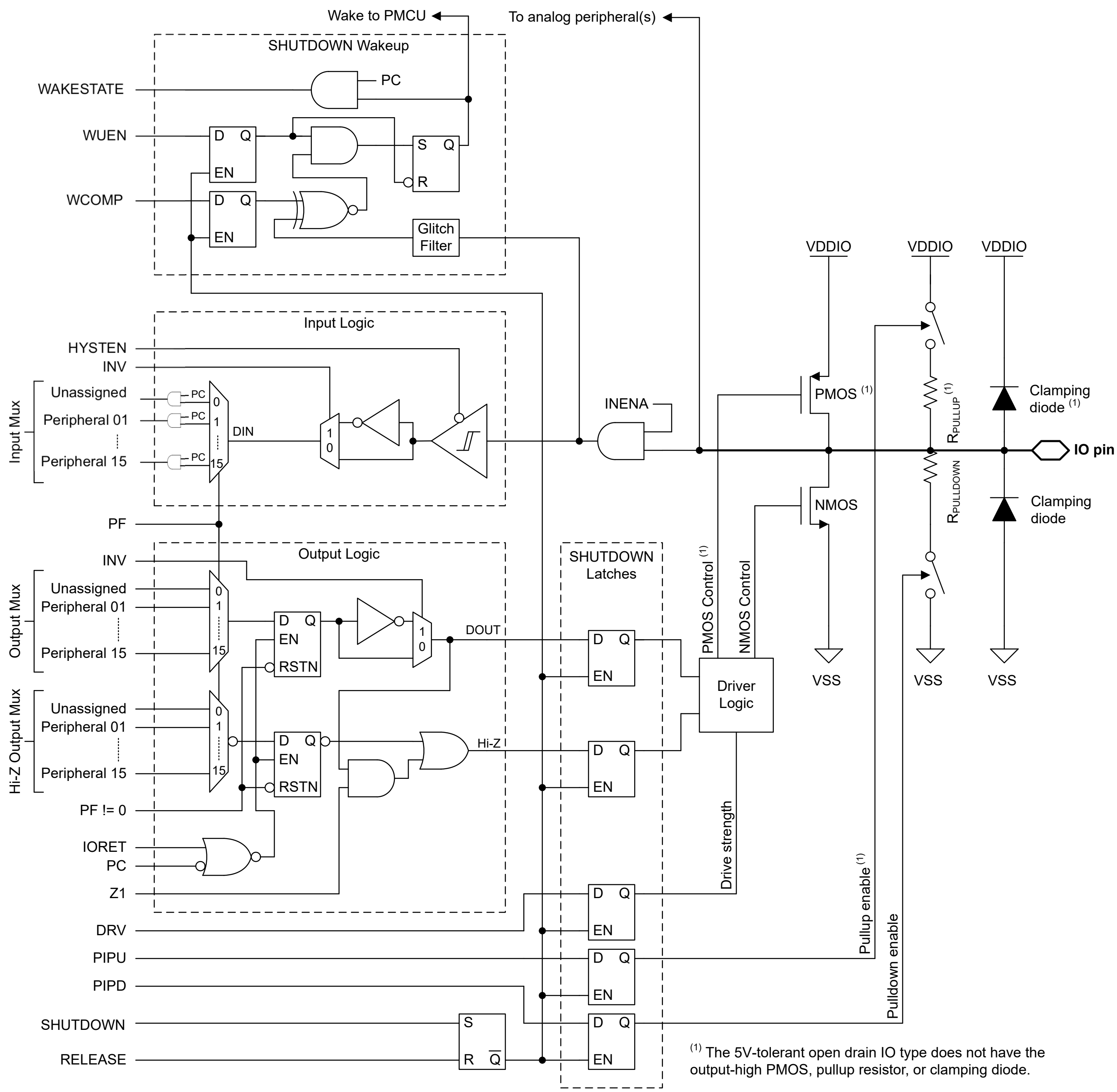

Figure 8-7. Superset Input/Output Diagram

8.33 Device Analog Connections

Figure 8-8 shows the internal analog connections of the device.

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ADVANCE INFORMATION

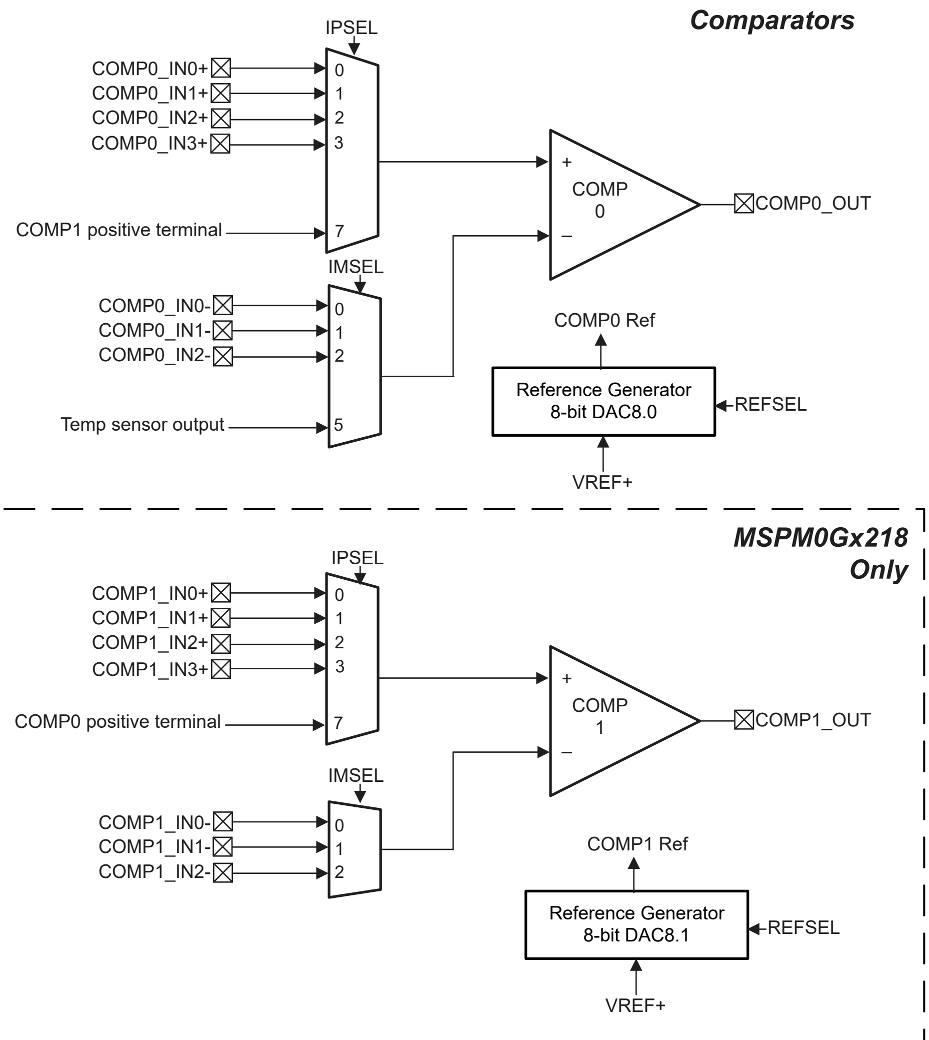

Figure 8-8. Comparator Analog Connections

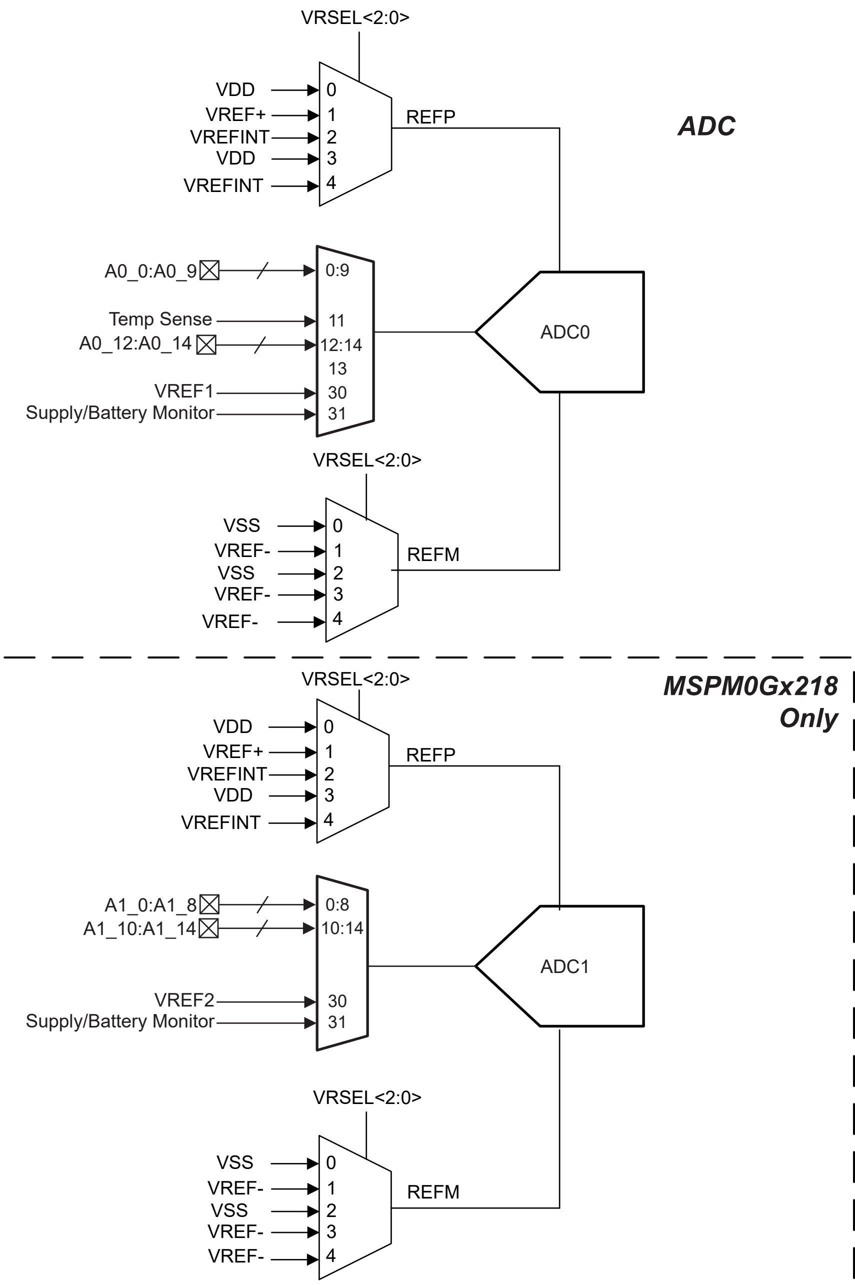

Figure 8-9. ADC Analog Connections

VREF

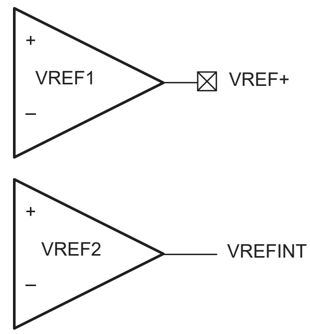

Figure 8-10. VREF Analog Connections

8.34 Serial Wire Debug Interface

A serial wire debug (SWD) two-wire interface is provided via an ARM compatible serial wire debug port (SW-DP) to enable access to multiple debug functions within the device. For a complete description of the debug functionality offered on MSPM0 devices, see the DEBUG chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

Table 8-22. Serial Wire Debug Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	SWD FUNCTION
SWCLK	Input	Serial wire clock from debug probe
SWDIO	Input/Output	Bi-directional (shared) serial wire data

8.35 Boot Strap Loader (BSL)

The boot strap loader (BSL) enables configuration of the device as well as programming of the device memory through a UART or I2C serial interface. Access to the device memory and configuration through the BSL is protected by a 256 bit user-defined password, and the BSL can be completely disabled in the device configuration, if desired. The BSL is enabled by default from TI to support use of the BSL for production programming.

A minimum of two pins are required to use the BSL: the BSLRX and BSLTX signals (for UART), or the BSLSCL and BSLSDA signals (for I^2C). Additionally, one or two additional pins (BSL_invoke and NRST) may be used for controlled invocation of the bootloader by an external host.

If enabled, the BSL may be invoked (started) in the following ways:

- The BSL is invoked during the boot process if the BSL_invoke pin state matches the defined BSL_invoke logic level. If the device fast boot mode is enabled, this invocation check is skipped. An external host can force the device into the BSL by asserting the invoke condition and applying a reset pulse to the NRST pin to trigger a BOOTRST, after which the device will verify the invoke condition during the reboot process and start the BSL if the invoke condition matches the expected logic level.
- The BSL is automatically invoked during the boot process if the reset vector and stack pointer are left unprogrammed. As a result, a blank device from TI will invoke the BSL during the boot process without any need to provide a hardware invoke condition on the BSL_invoke pin. This enables production programming using just the serial interface signals.
- The BSL may be invoked at runtime from application software by issuing a SYSRST with BSL entry command.

Table 8-23. BSL Pin Requirements and Functions

DEVICE SIGNAL	CONNECTION	BSL FUNCTION
BSLRX	Required for UART	UART receive signal (RXD), an input
BSLTX	Required for UART	UART transmit signal (TXD) an output

Table 8-23. BSL Pin Requirements and Functions (continued)

DEVICE SIGNAL	CONNECTION	BSL FUNCTION
BSLSCL	Required for I2C	I^2C BSL clock signal (SCL)
BSLSDA	Required for I2C	I^2C BSL data signal (SDA)
BSL_invoke	Optional	Active-high digital input used to start the BSL during boot
NRST	Optional	Active-low reset pin used to trigger a reset and subsequent check of the invoke signal (BSL_invoke)

For a complete description of the BSL functionality and command set, see the MSPM0 boot strap loader user's guide.

8.36 Device Factory Constants

All devices include a memory-mapped FACTORY region which provides read-only data describing the capabilities of a device as well as any factory-provided trim information for use by application software. Please refer to Factory Constants chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual* for more information.

Table 8-24. DEVICEID

DEVICEID address is 0x41C4.0004, PARTNUM is bit 12 to 27, MANUFACTURER is bit 1 to 11.

Device	PARTNUM	MANUFACTURER
MSPM0G3218, MSPM0G3207, MSPM0G1218, MSPM0G1207	0xBBCE	0x17

Table 8-25. USERID

USERID address is 0x41C4.0008, PART is bit 0 to 15, VARIANT is bit 16 to 23

Device	Part	Variant
MSPM0G3218SPMR	0xC415	0x17
MSPM0G3218SPTR	0xC415	0x12
MSPM0G3218SRGZR	0xC415	0x14
MSPM0G3218SRHBR	0xC415	0x15
MSPM0G3218SRGER	0xC415	0x13
MSPM0G3207SPMR	0x5114	0x17
MSPM0G3207SPTR	0x5114	0x12
MSPM0G3207SRGZR	0x5114	0x14
MSPM0G3207SRHBR	0x5114	0x15
MSPM0G3207SRGER	0x5114	0x13
MSPM0G1218SPMR	0x5A95	0x17
MSPM0G1218SPTR	0x5A95	0x12
MSPM0G1218SRGZR	0x5A95	0x14
MSPM0G1218SRHBR	0x5A95	0x15
MSPM0G1218SRUYR	0x5A95	0x16
MSPM0G1218S28DGSR	0x5A95	0x11
MSPM0G1218SRGER	0x5A95	0x13
MSPM0G1207SPMR	0xC2CE	0x17
MSPM0G1207SPTR	0xC2CE	0x12

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Table 8-25. USERID (continued)

USERID address is 0x41C4.0008, PART is bit 0 to 15, VARIANT is bit 16 to 23

Device	Part	Variant
MSPM0G1207SRGZR	0xC2CE	0x14
MSPM0G1207SRHBR	0xC2CE	0x15
MSPM0G1207SRUYR	0xC2CE	0x16
MSPM0G1207S28DGSR	0xC2CE	0x11

8.37 Identification

Revision and Device Identification

The hardware revision and device identification values are stored in the memory-mapped FACTORY region, refer to Device Factory Constants section, which provides read-only data describing the capabilities of a device as well as any factory-provided trim information for use by application software. Refer to Factory Constants chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual* for more information.

The device revision and identification information are also included as part of the top-side marking on the device package. The device-specific errata sheet describes these markings (see Section 10.4)

9 Applications, Implementation, and Layout

9.1 Typical Application

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1.1 Schematic

TI recommends connecting a combination of a 10µF and a 0.1µF low-ESR ceramic decoupling capacitor across the VDD and VSS pins, as well as placing these capacitors as close as possible to the supply pins that they decouple (within a few millimeters) to achieve a minimal loop area. The 10µF bulk decoupling capacitor is a recommended value for most applications, but this capacitance may be adjusted if needed based upon the PCB design and application requirements. For example, larger bulk capacitors can be used, but this can affect the supply rail ramp-up time.

The NRST reset pin must be pulled up to VDD (supply level) for the device to release from RESET state and start the boot process. TI recommends connecting an external 47kΩ pullup resistor with a 10nF pulldown capacitor for most applications, enabling the NRST pin to be controlled by another device or a debug probe.

The SYSOSC frequency correction loop (FCL) circuit utilizes an external 100kΩ with 0.1% tolerance resistor with a temperature coefficient (TCR) of 25ppm/C or better populated between the ROSC pin and VSS. This resistor establishes a reference current to stabilize the SYSOSC frequency through a correction loop. This resistor is required if the FCL feature is used for higher accuracy, and it is not required if the SYSOSC FCL is not enabled. When the FCL mode is not used, the PA2 pin may be used as a digital input/output pin.

A 0.47µF tank capacitor is required for the VCORE pin and must be placed close to the device with minimum distance to the device ground. Do not connect other circuits to the VCORE pin.

For the 5V-tolerant open drain (ODIO), a pullup resistor is required to output high for I2C and UART functions, as the open drain IO only implement a low-side NMOS driver and no high-side PMOS driver. The 5V-tolerant open drain IO are fail-safe and may have a voltage present even if VDD is not supplied.

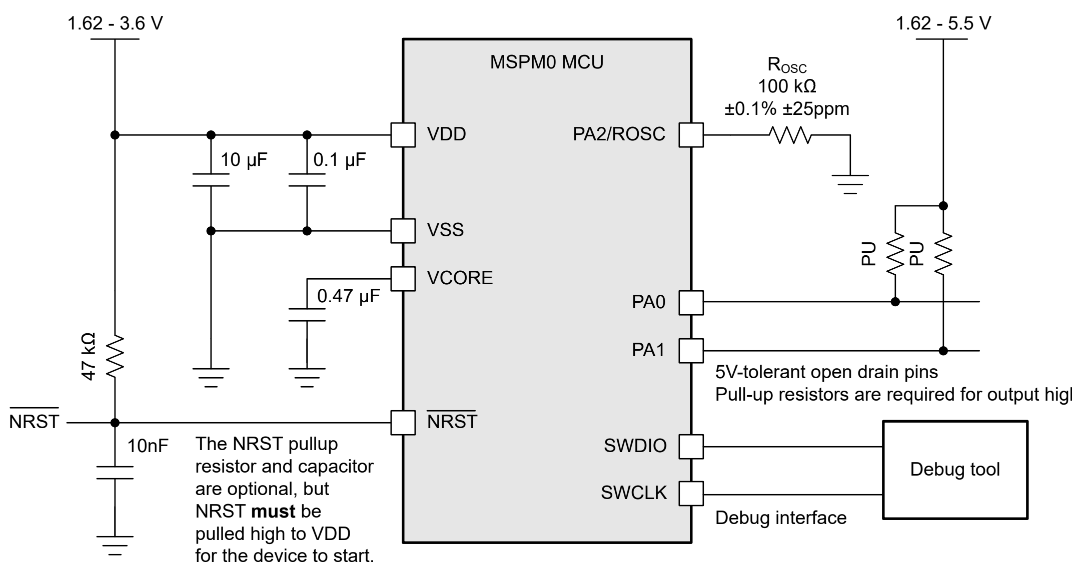

Figure 9-1. Basic Application Schematic

ADVANCE INFORMATION

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Getting Started and Next Steps

For more information on the MSP low-power microcontrollers and the tools and libraries that are available to help with development, visit the Texas Instruments *Arm Cortex-M0+ MCUs* page.

10.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP MCU devices and support tools. . Each MSP MCU commercial family member has one of two prefixes: MSP or X. These prefixes represent evolutionary stages of product development from engineering prototypes (X) through fully qualified production devices (MSP).

X – Experimental device that is not necessarily representative of the final device's electrical specifications

MSP – Fully qualified production device

X devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes." MSP devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies. Predictions show that prototype devices (X) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the temperature range, package type, and distribution format. Figure 10-1 provides a legend for reading the complete device name.

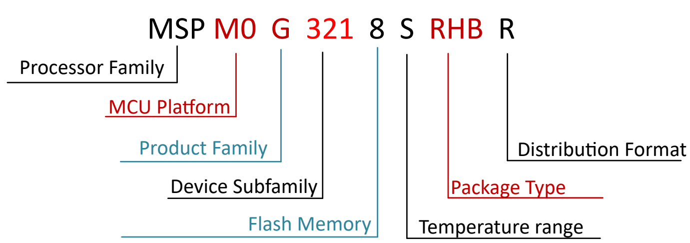

Figure 10-1. Device Nomenclature

Table 10-1. Device Nomenclature

Processor Family	**MSP = Mixed-signal processor** **X= Experimental silicon**
MCU Platform	M0 = Arm based 32-bit M0+
Product Family	G = 80MHz frequency
Device Subfamily	321 = 2x ADC, 2x COMP, CAN-FD, 32kB SRAM 320 = 1x ADC, 1x COMP, CAN-FD, 32kB SRAM 121 = 2x ADC, 2x COMP, 32kB SRAM 120 = 1x ADC, 1x COMP, 32kB SRAM
Flash Memory	8 = 256KB 7 = 128KB 6 = 64KB
Temperature Range	S = –40°C to 125°C
Package Type	See the Device Comparison section and https://www.ti.com/packaging

Table 10-1. Device Nomenclature (continued)

Processor Family	**MSP = Mixed-signal processor** **X= Experimental silicon**
Distribution Format	T = Small reel R = Large reel No marking = Tube or tray

For orderable part numbers of MSP devices in different package types, see the Package Option Addendum of this document, ti.com, or contact your TI sales representative.

10.3 Tools and Software

Design Kits and Evaluation Modules

MSPM0 LaunchPad (LP) Boards: LP-MSPM0G3519 Empowers you to immediately start developing on the industry's best integrated analog and most cost-optimized general purpose MSPM0 MCU family. Exposes all device pins and functionality; includes some built-in circuitry, out-of-box software demos, and on-board XDS110 debug probe for programming/debugging/ EnergyTrace.

The LP ecosystem includes dozens of BoosterPack stackable plug-in modules to extend functionality.

Embedded Software

MSPM0 Software Development Kit (SDK) Contains software drivers, middleware libraries, documentation, tools, and code examples that create a familiar and easy user experience for all MSPM0 devices.

Software Development Tools

TI Developer Zone Start your evaluation and development on a web browser without any installation. Cloud tools also have a downloadable, offline version.

TI Resource Explorer Online portal to TI SDKs. Accessible in CCS IDE or in TI Cloud Tools.

SysConfig Intuitive GUI to configure device and peripherals, resolve system conflicts, generate configuration code, and automate pin mux settings. Accessible in CCS IDE ,in TI Cloud Tools or a standalone version. (offline version)

MSP Academy Great starting point for all developers to learn about the MSPM0 MCU Platform with training modules that span a wide range of topics. Part of TIRex.

GUI Composer GUIs that simplify evaluation of certain MSPM0 features, such as configuring and monitoring a fully integrated analog signal chain without any code needed.

IDE & compiler toolchains

Code Composer Studio™ (CCS) Code Composer Studio is an integrated development environment (IDE) for TI's microcontrollers and processors. It comprises a suite of tools used to develop and debug embedded applications. CCS is completely free to use and is available on Eclipse and Theia frameworks.

IAR Embedded Workbench® IDE IAR Embedded Workbench for Arm delivers a complete development toolchain for building and debugging embedded applications for MSPM0.The included IAR C/C++ Compiler generates highly optimized code for your application, and the C-SPY Debugger is a fully integrated debugger for source and disassembly level debugging with support for complex code and data breakpoint.

Keil® MDK IDE Arm Keil MDK is a complete debugger and C/C++ compiler toolchain for building and debugging embedded applications for MSPM0.Keil MDK includes a fully

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	integrated debugger for source and disassembly level debugging.MDK provides full CMSIS compliance.
TI Arm-Clang	TI Arm Clang is included in Code Composer Studio.
GNU Arm Embedded Toolchain	The MSPM0 SDK supports development using the open-source Arm GNU Toolchain.Arm GCC is supported by Code Composer Studio (CCS).

10.4 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The following documents describe the MSPM0 MCUs. Copies of these documents are available on the Internet at www.ti.com.

Technical Reference Manual

MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual	This manual describes the modules and peripherals of the MSPM0G family of devices. Each description presents the module or peripheral in a general sense. Not all features and functions of all modules or peripherals are present on all devices. In addition, modules or peripherals can differ in their exact implementation on different devices. Pin functions, internal signal connections, and operational parameters differ from device to device. See the device-specific data sheet for these details.

10.5 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.6 Trademarks

Code Composer Studio™ and TI E2E™ are trademarks of Texas Instruments.
Arm® and Cortex® are registered trademarks of Arm Limited.
All trademarks are the property of their respective owners.

10.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.8 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
February 2026	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

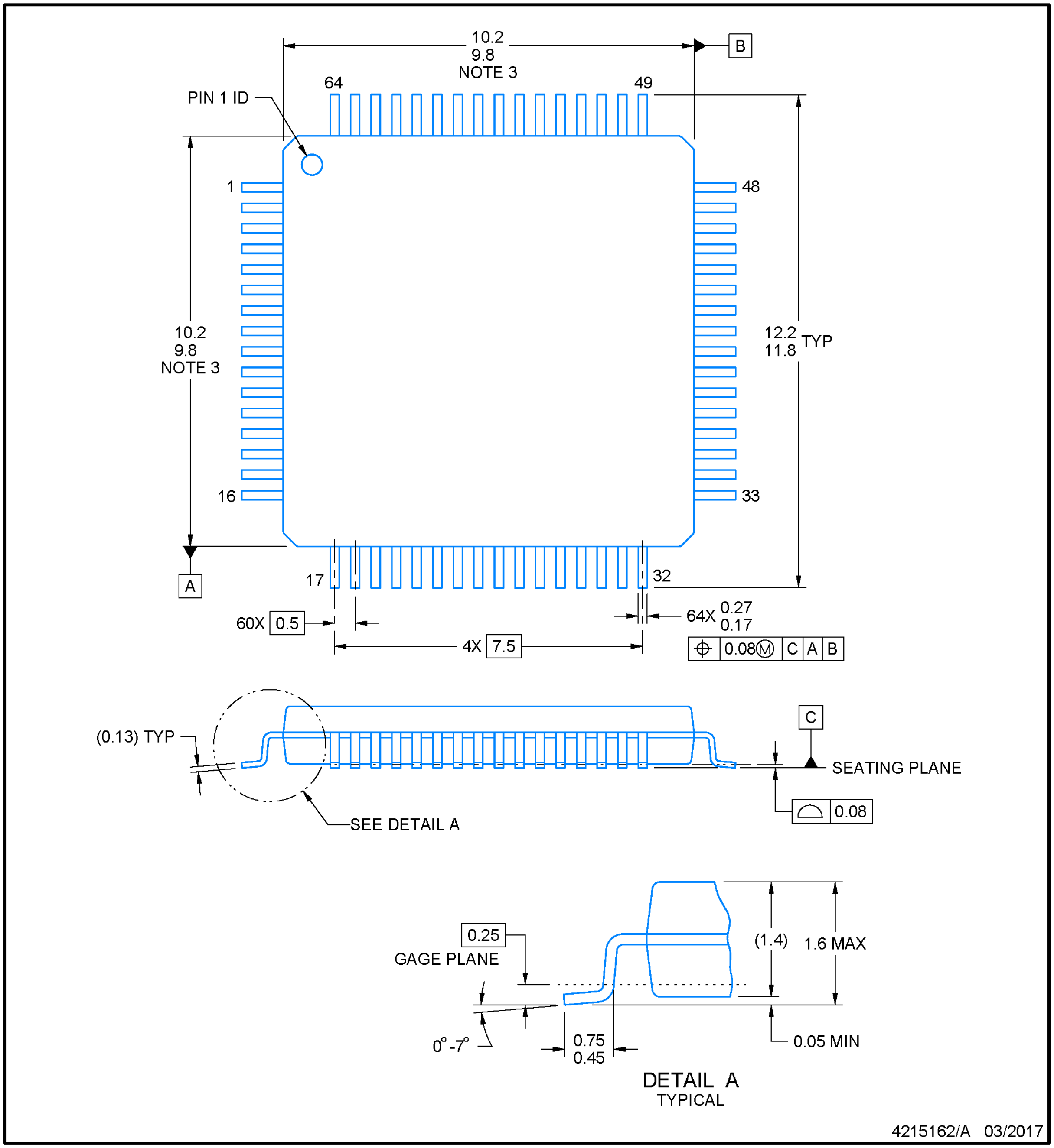
ADVANCE INFORMATION

PACKAGE OUTLINE

PM0064A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



4215162/A 03/2017

NOTES:

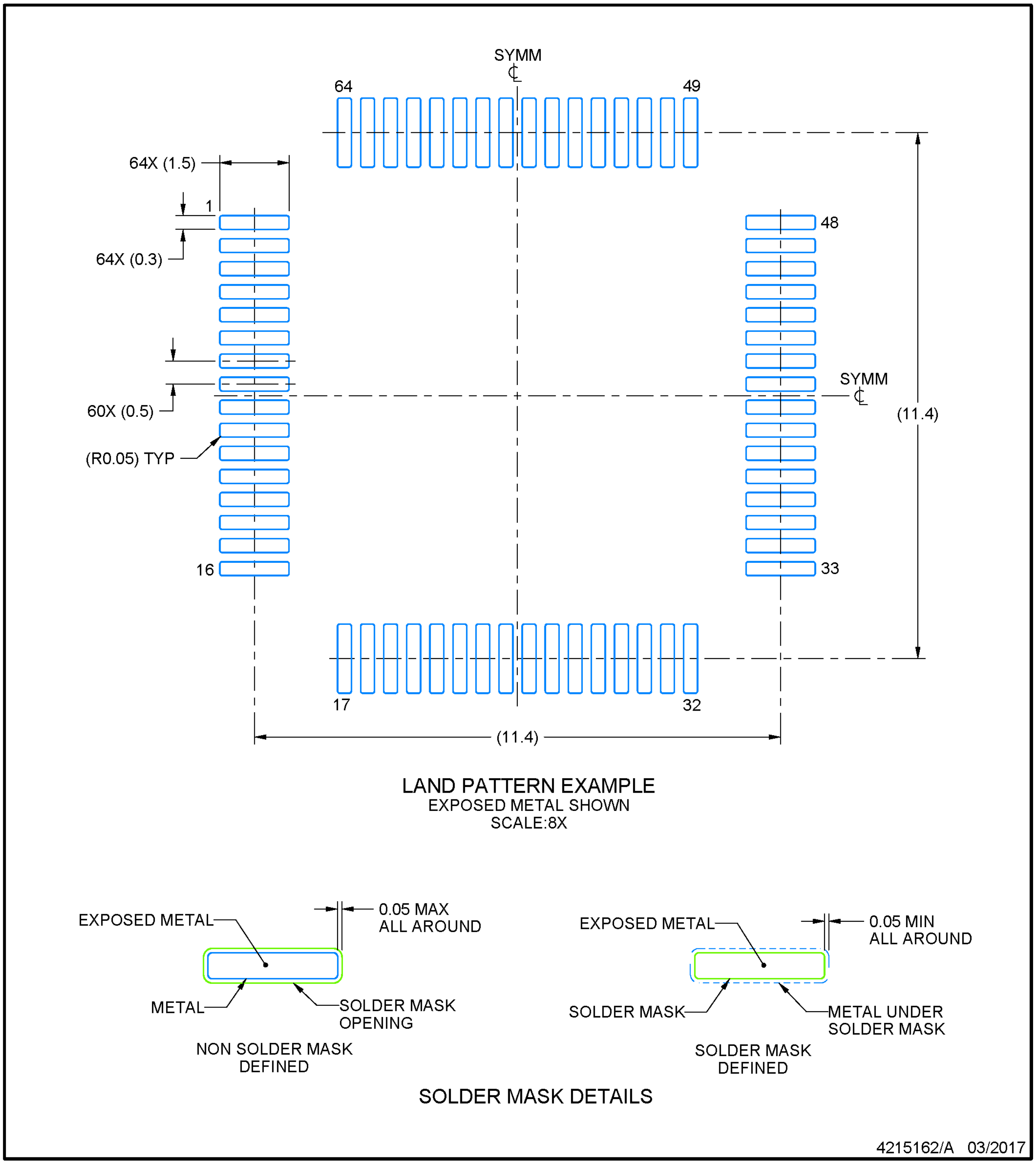
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.

EXAMPLE BOARD LAYOUT

PM0064A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



ADVANCE INFORMATION

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).

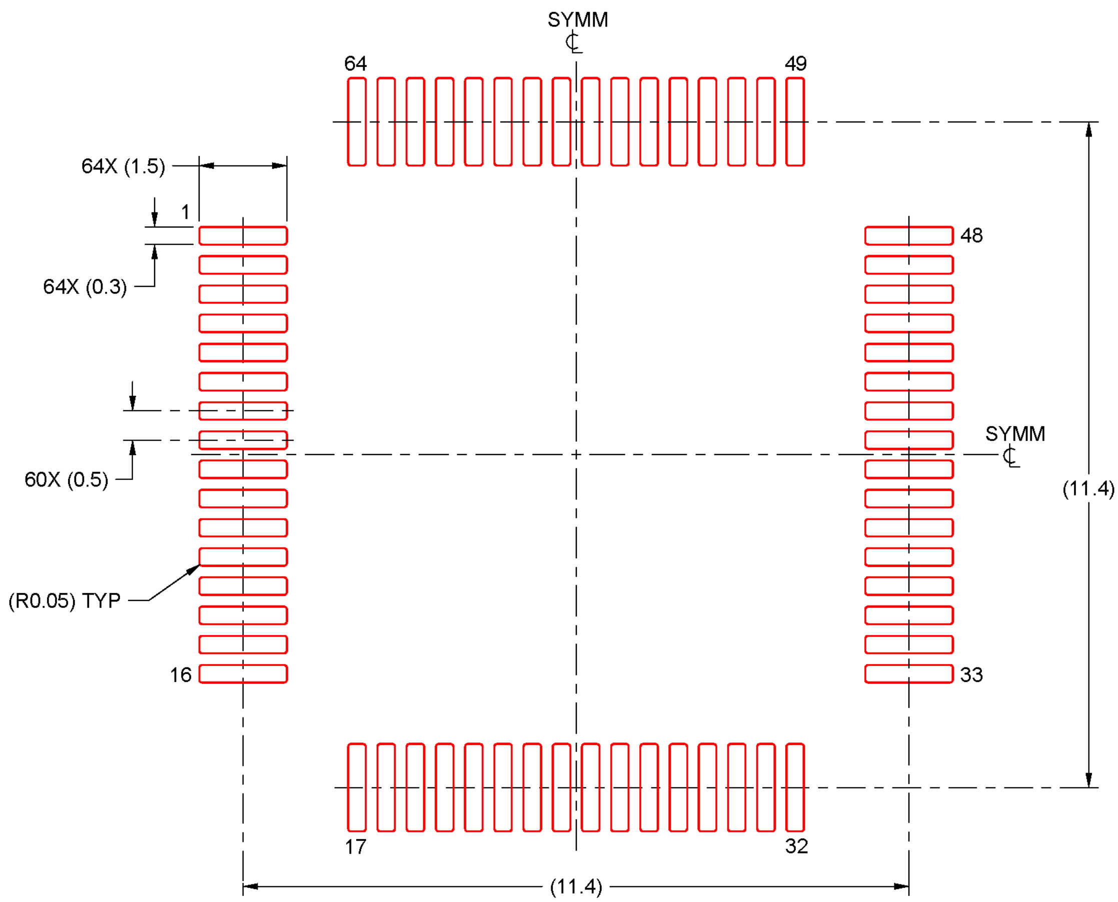
ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

PM0064A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK

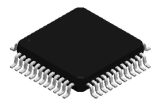


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4215162/A 03/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

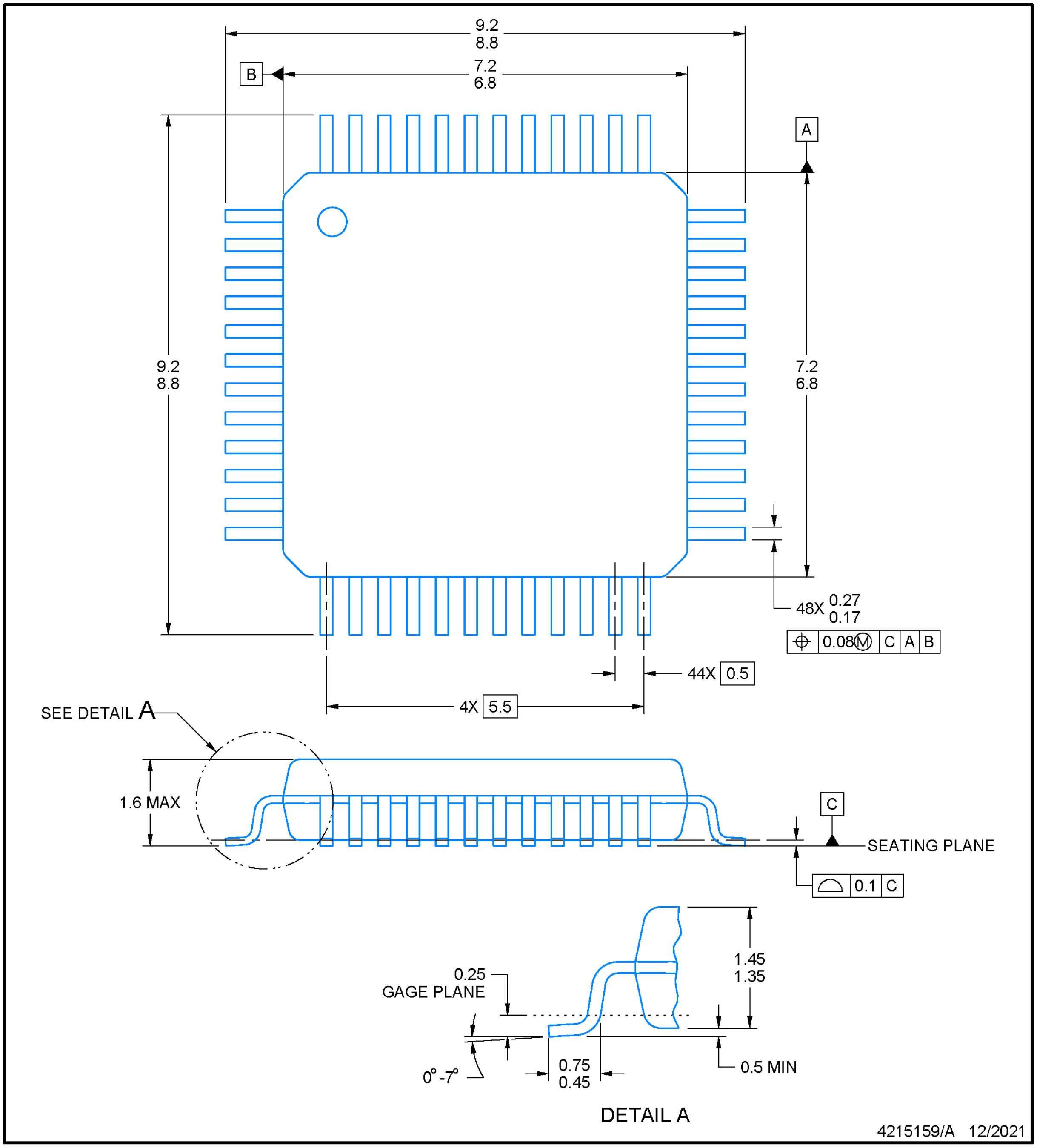


PACKAGE OUTLINE

PT0048A

LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.
4. This may also be a thermally enhanced plastic package with leads conected to the die pads.

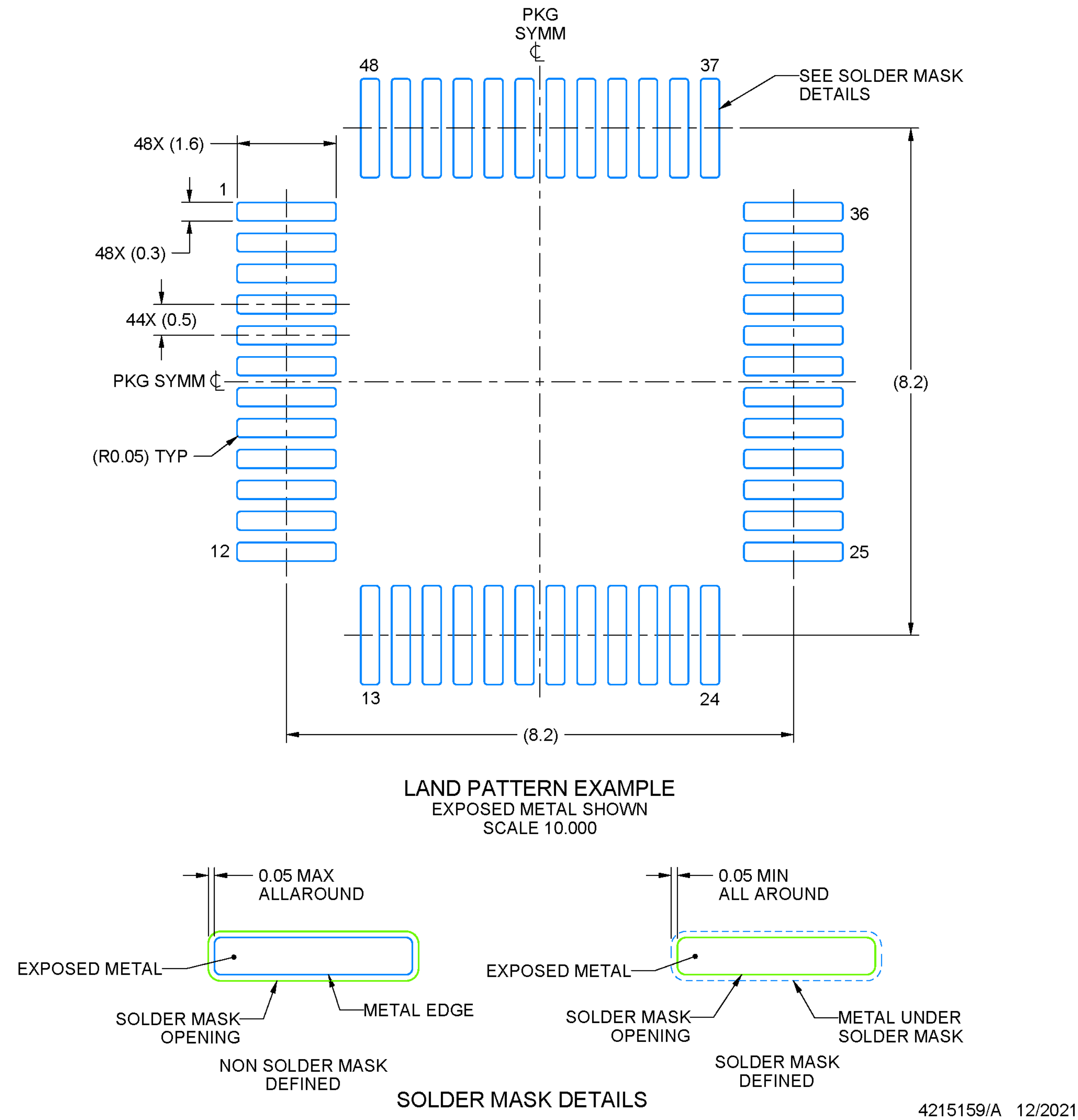
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

PT0048A

LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE 10.000

SOLDER MASK DETAILS

NOTES: (continued)

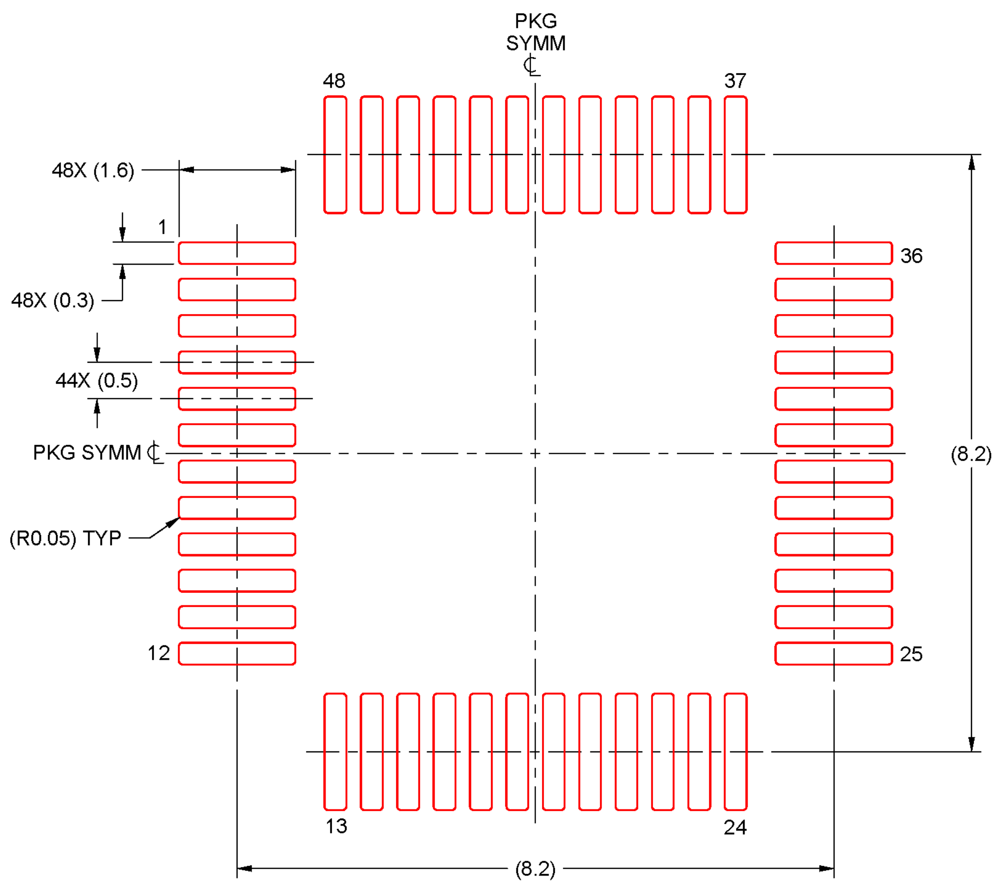
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PT0048A

LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 10X

4215159/A 12/2021

ADVANCE INFORMATION

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

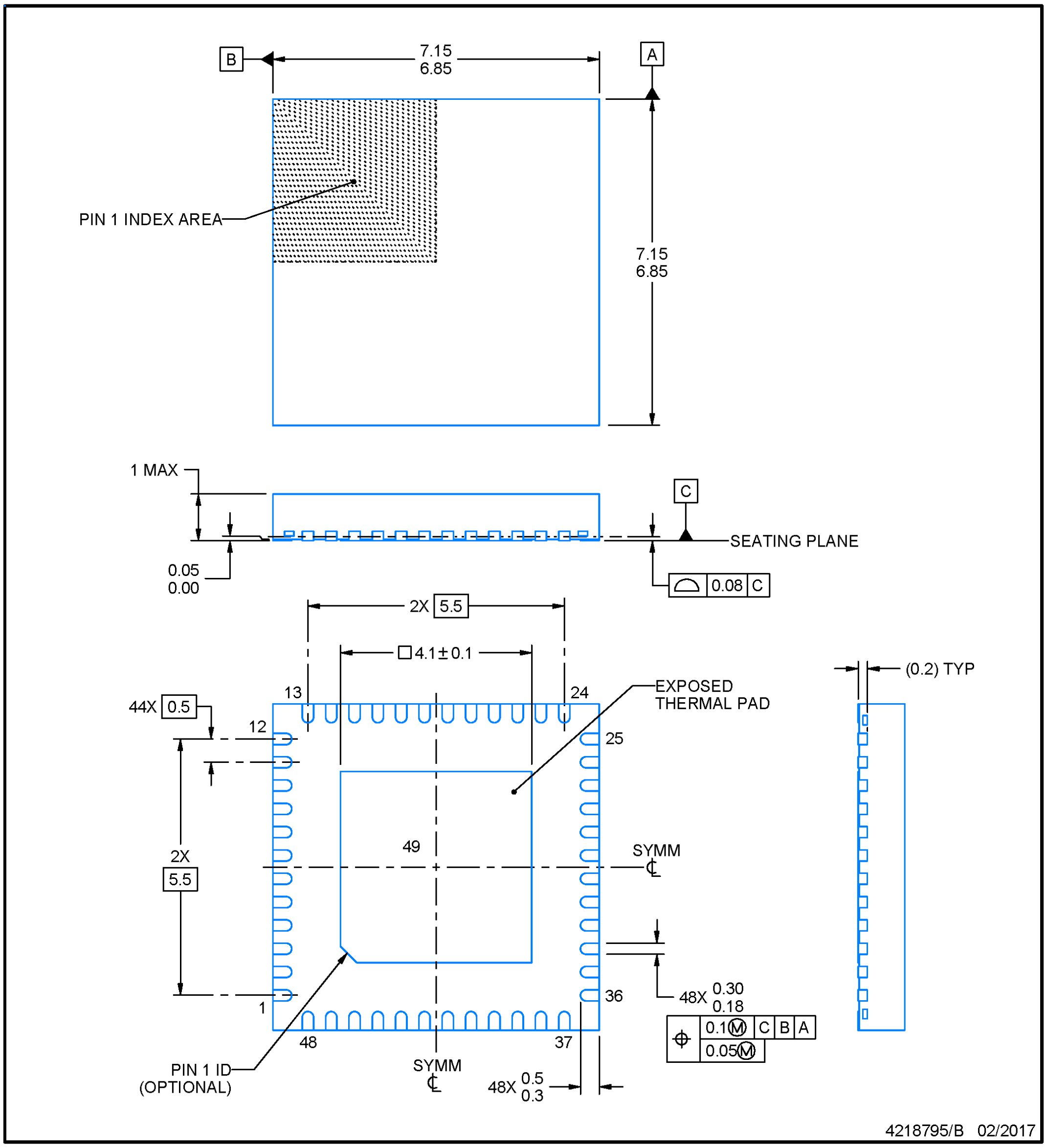
ADVANCE INFORMATION

PACKAGE OUTLINE

RGZ0048B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

TEXAS INSTRUMENTS
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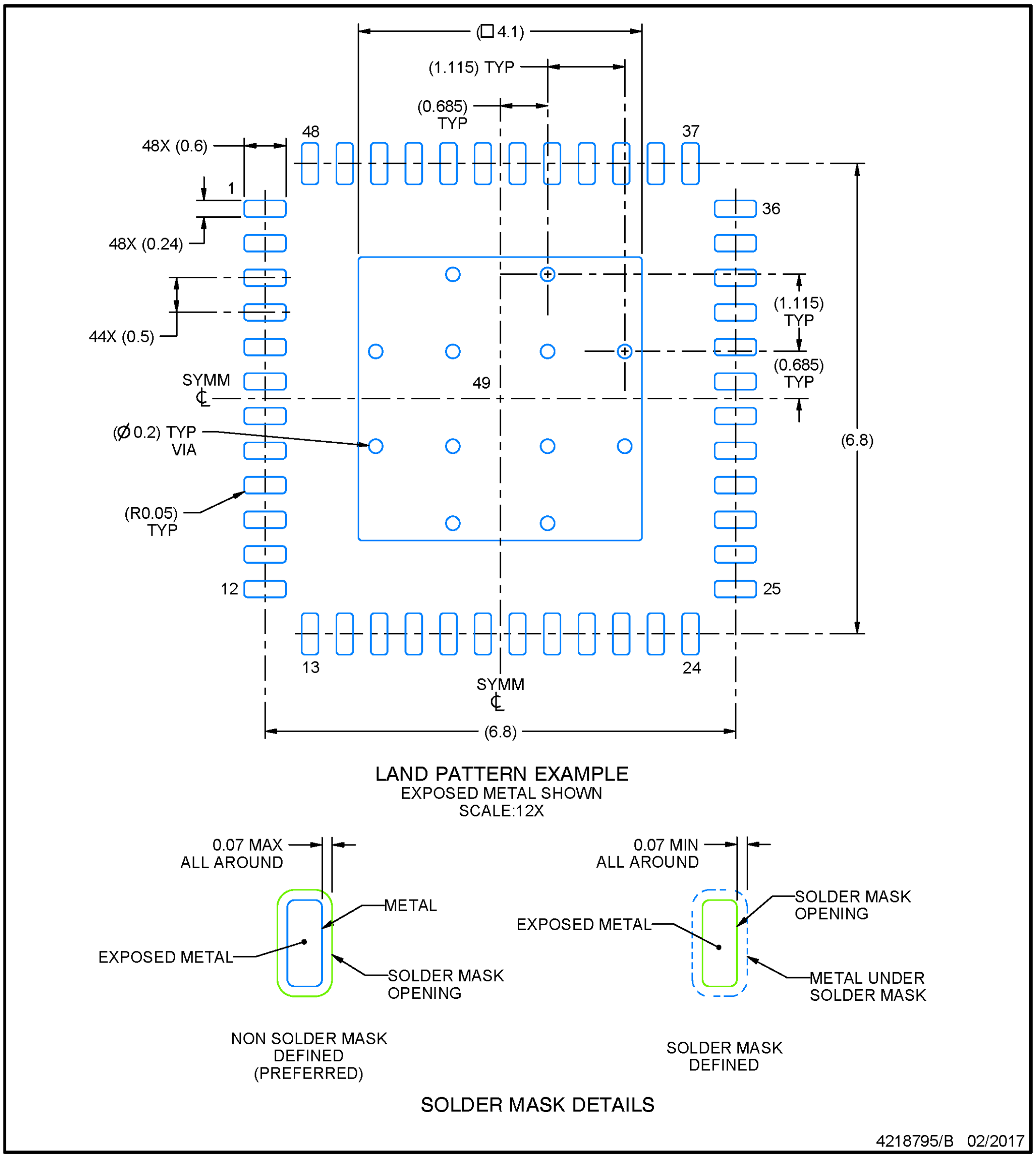
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

RGZ0048B **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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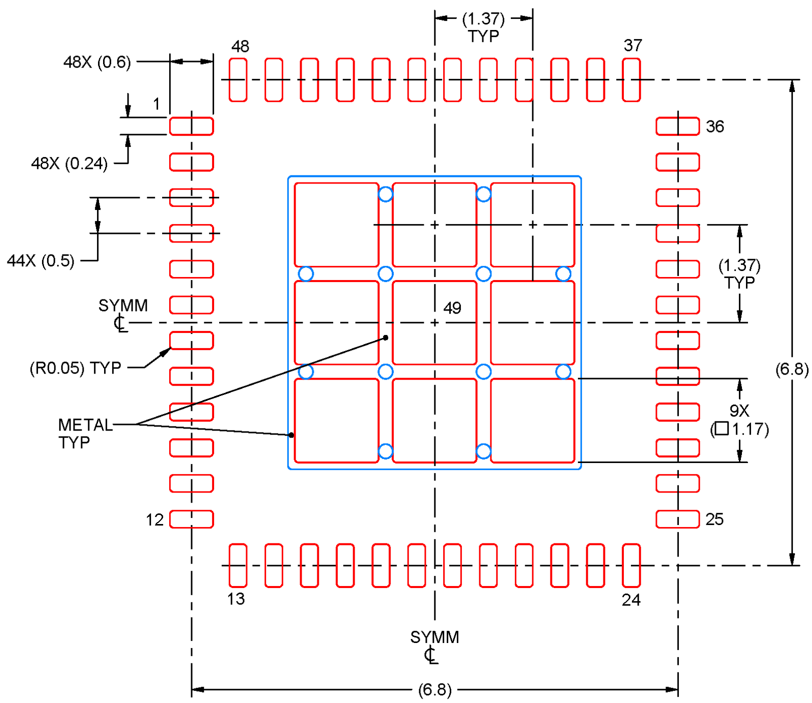
ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

RGZ0048B **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
73% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

4218795/B 02/2017

NOTES: (continued)

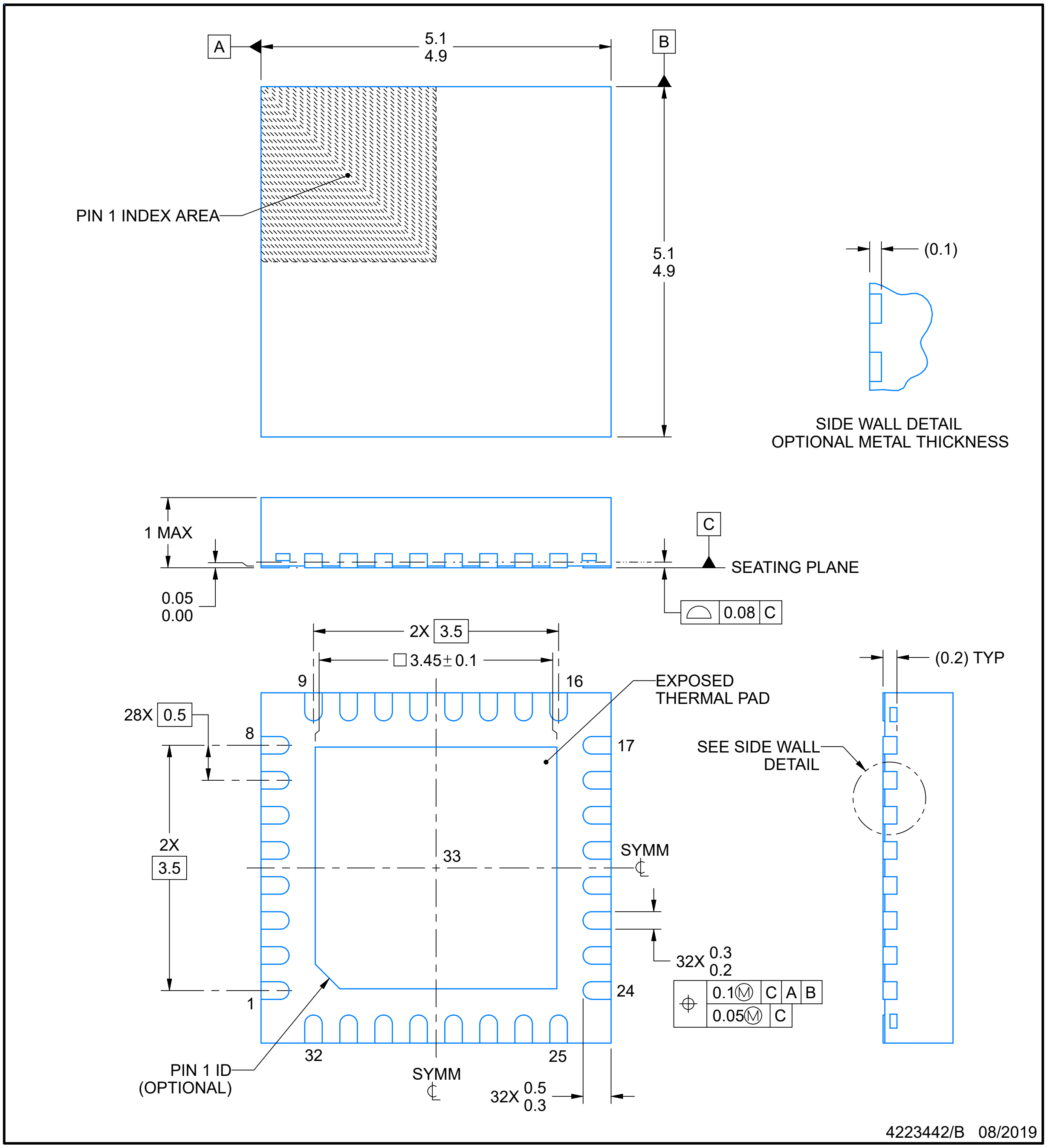
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

ADVANCE INFORMATION

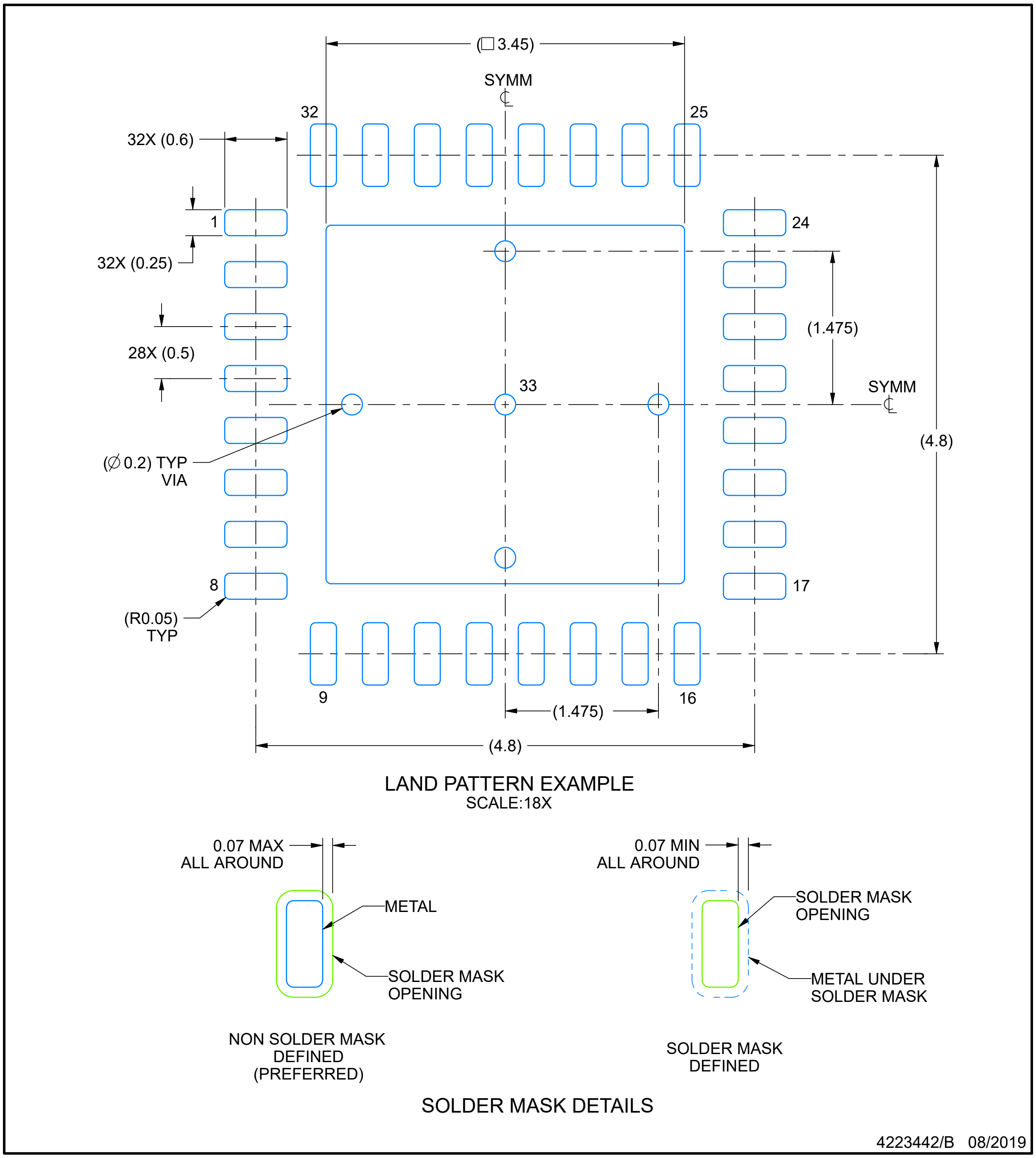
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

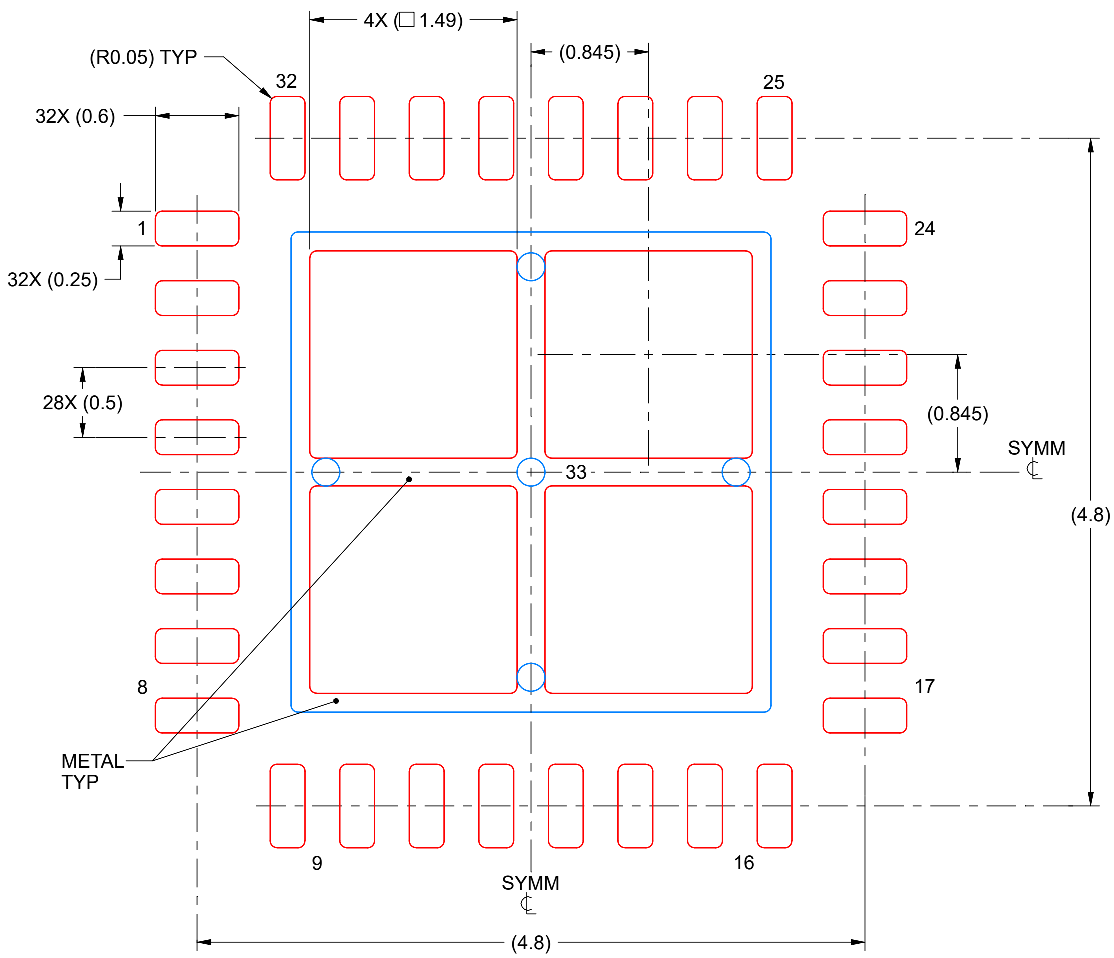
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4223442/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

ADVANCE INFORMATION

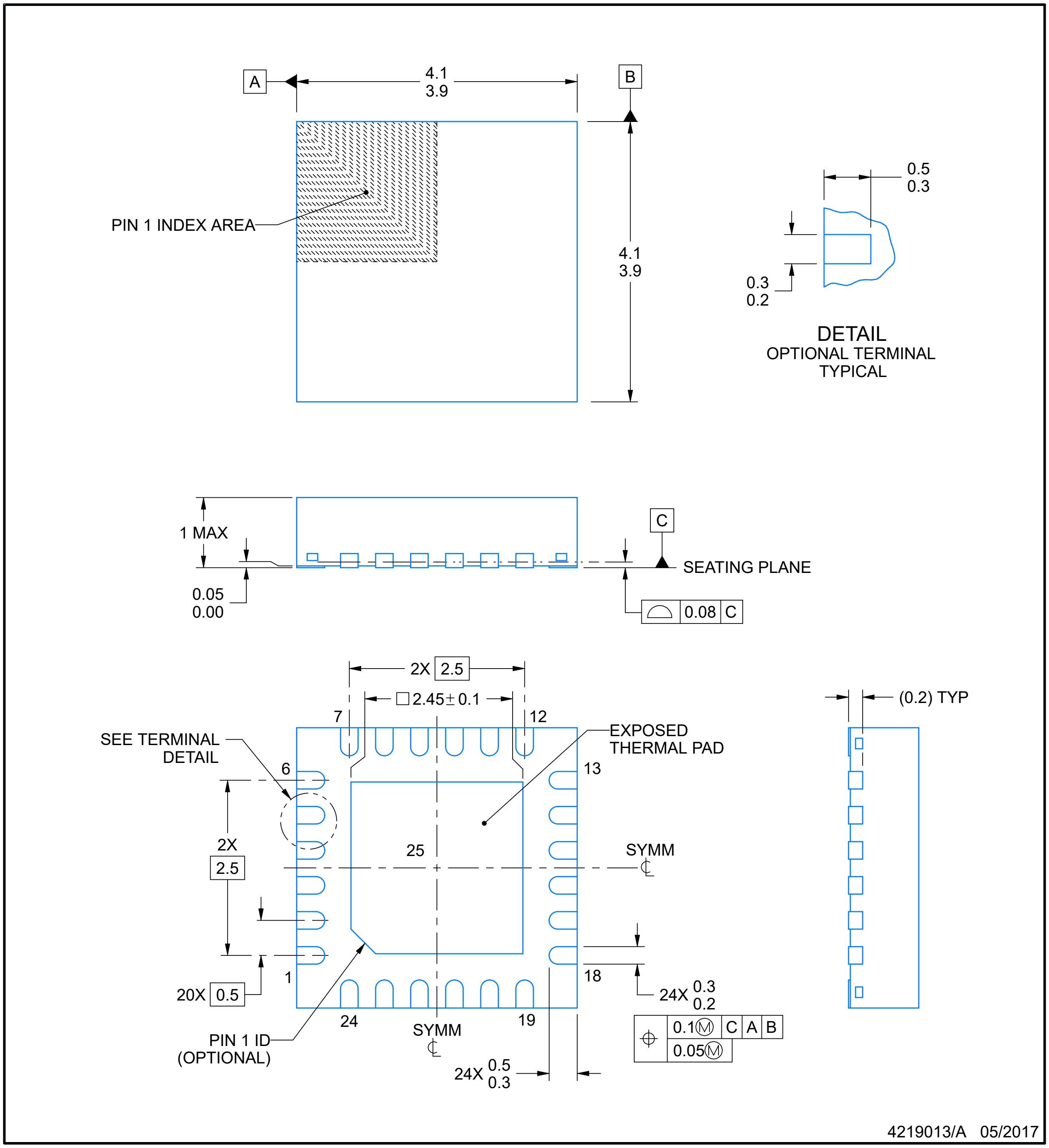
ADVANCE INFORMATION

PACKAGE OUTLINE

RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

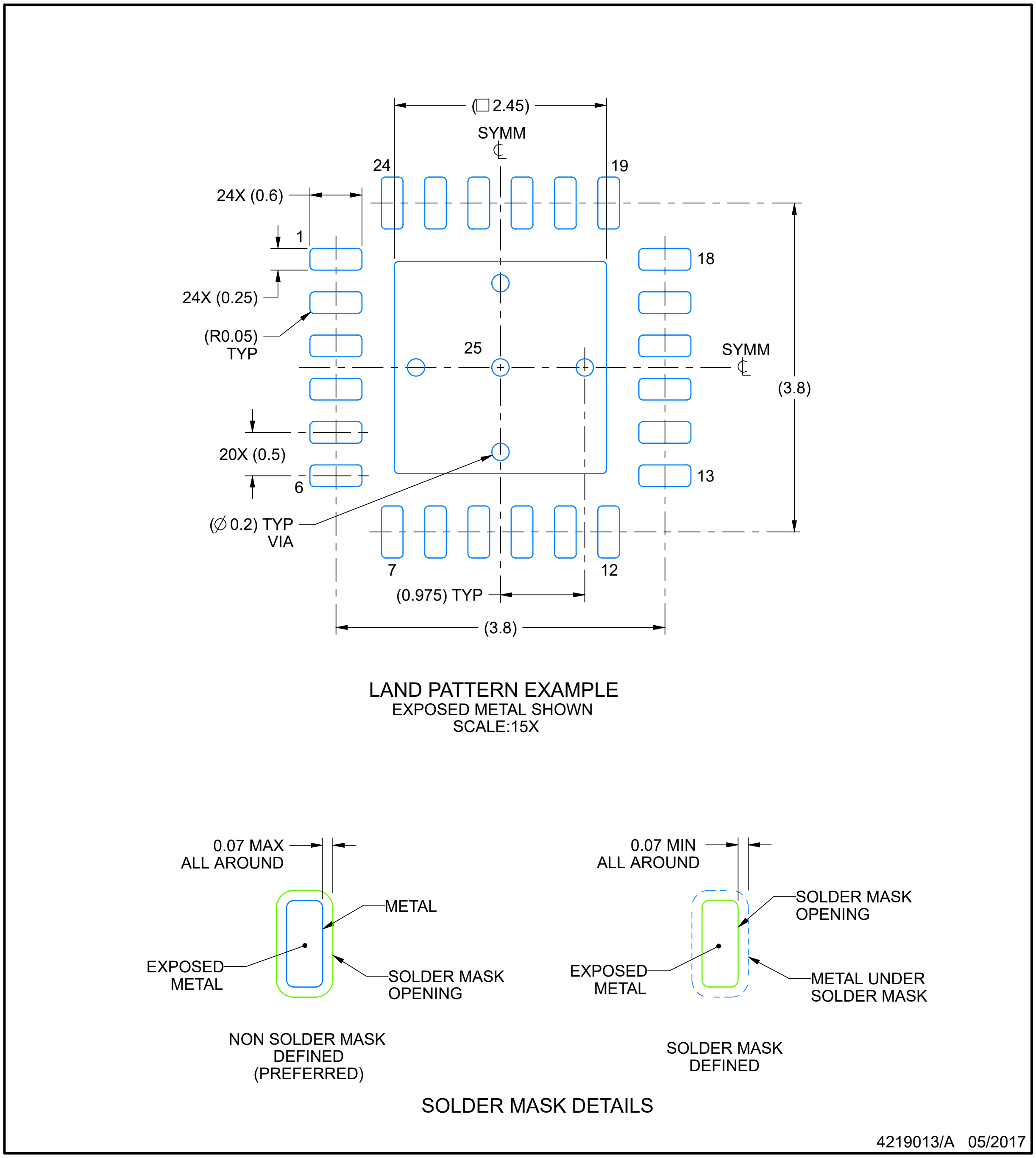
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

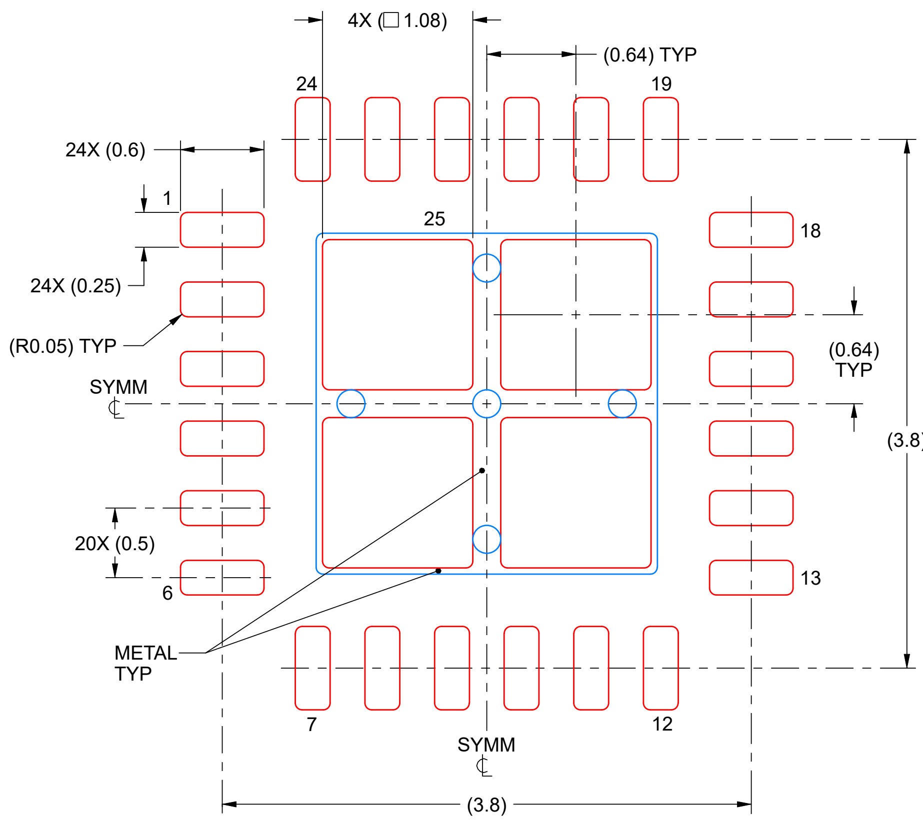
ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219013/A 05/2017

NOTES: (continued)

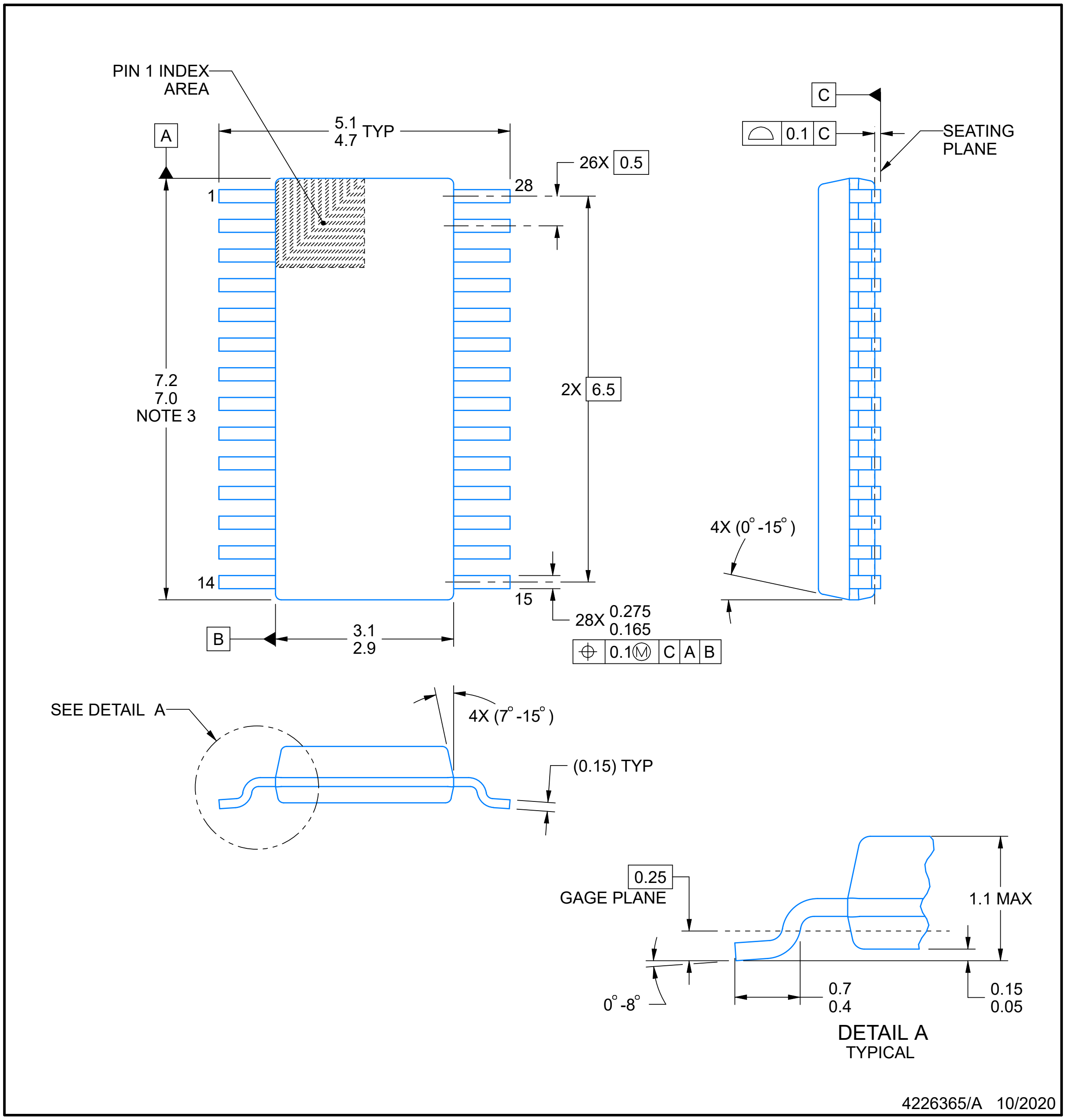
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DGS0028A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



PowerPAD is a trademark of Texas Instruments.

NOTES:

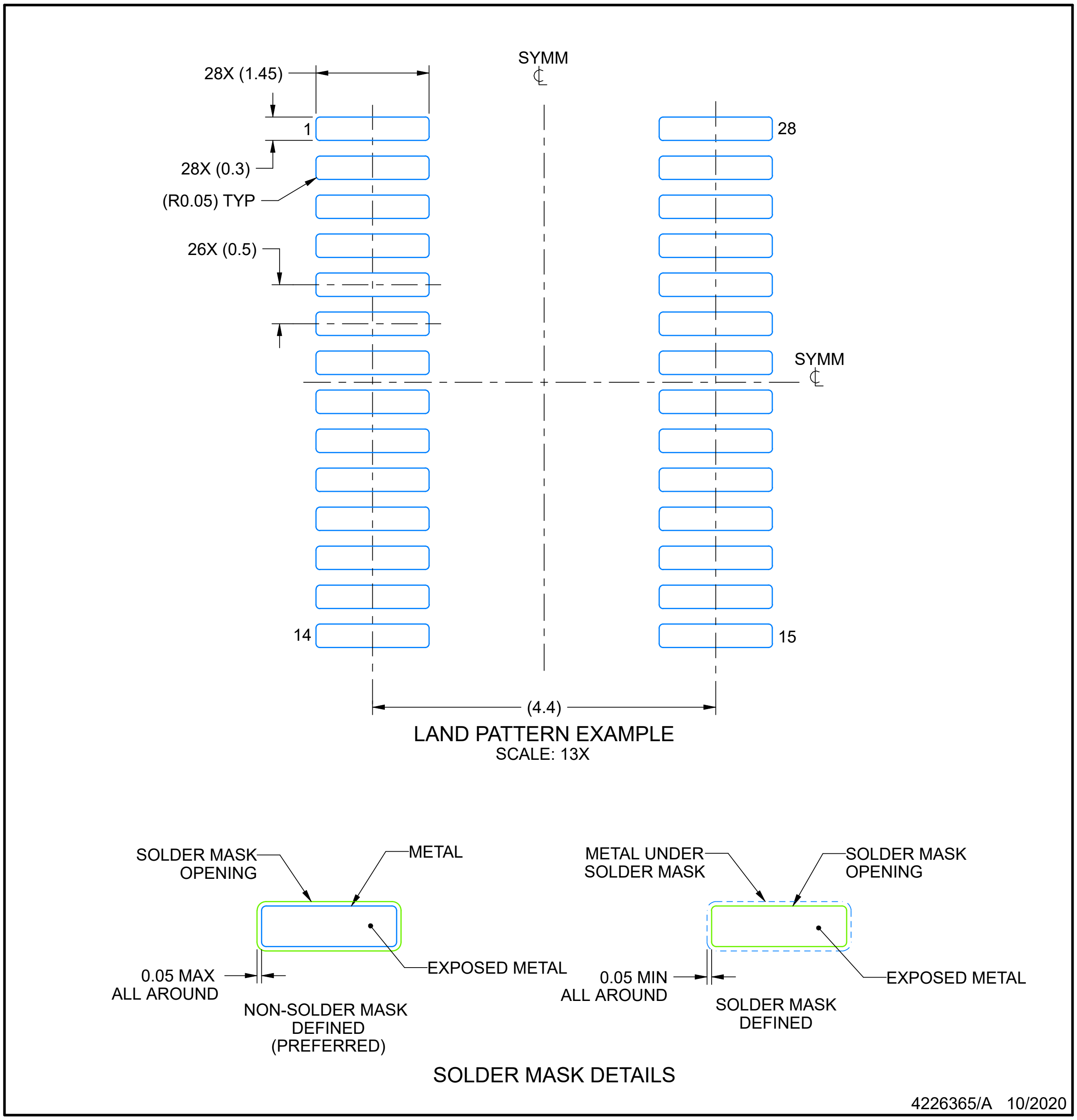
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.

ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

DGS0028A VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

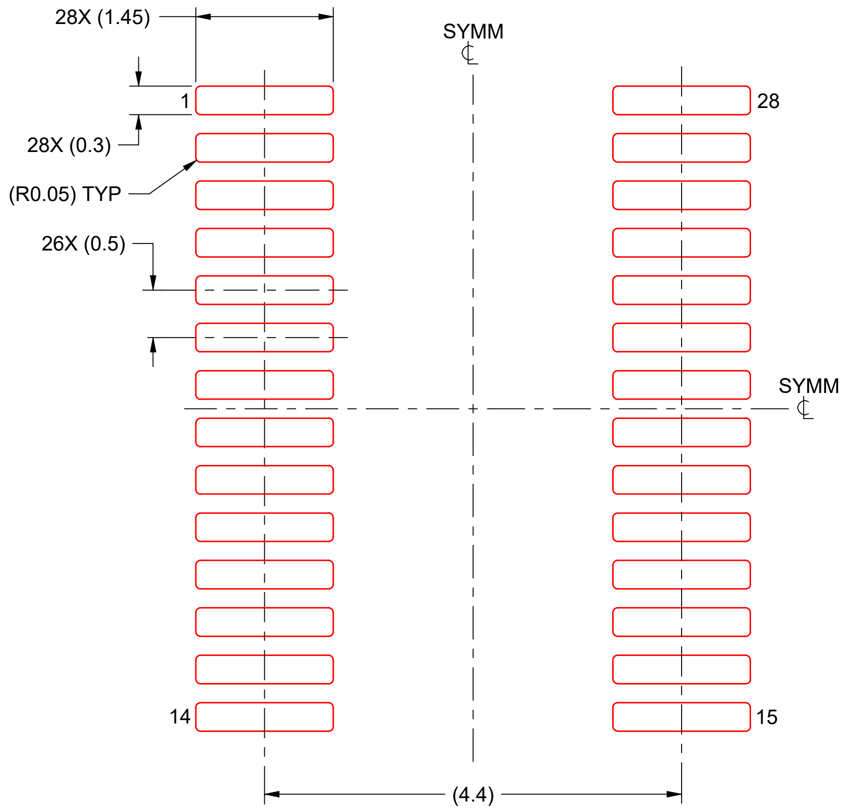
ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

DGS0028A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 13X

4226365/A 10/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

ADVANCE INFORMATION

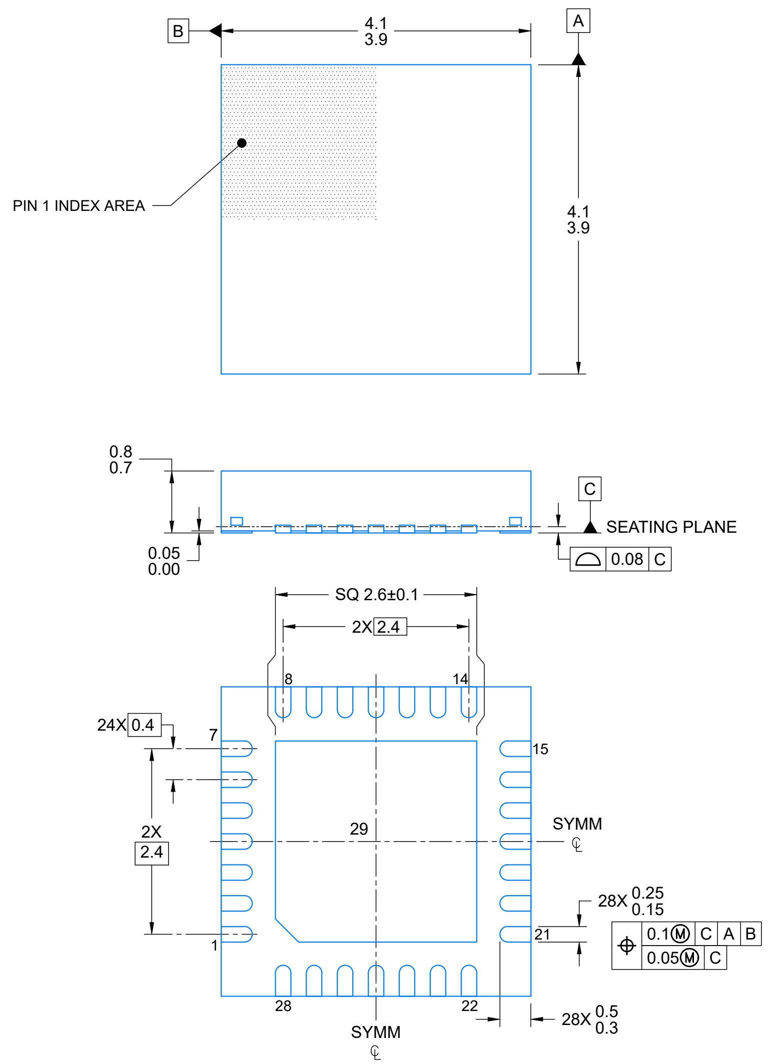
ADVANCE INFORMATION

PACKAGE OUTLINE

RUY0028A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



4219146/C 03/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

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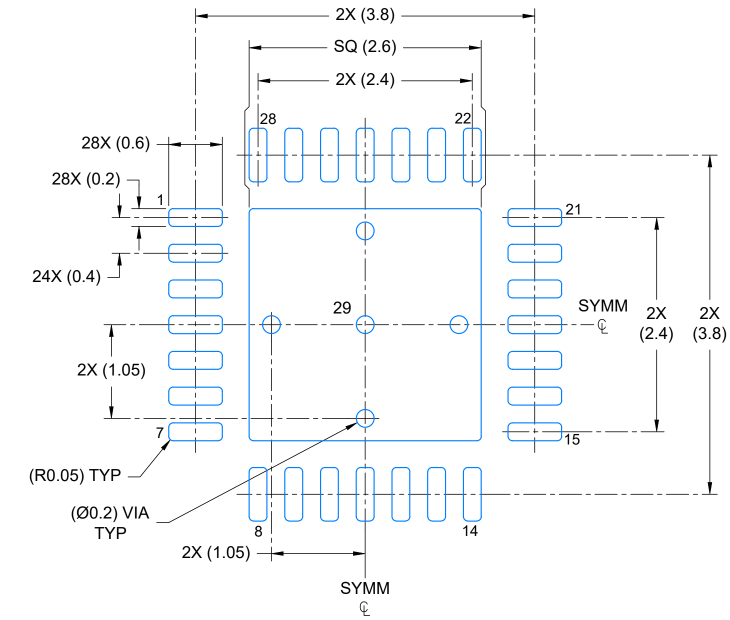
EXAMPLE BOARD LAYOUT

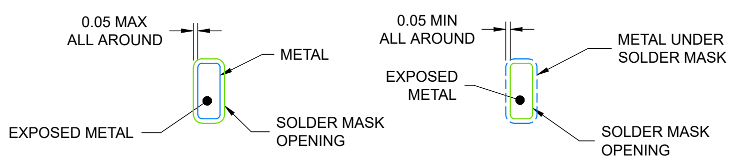
RUY0028A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4219146/C 03/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

ADVANCE INFORMATION

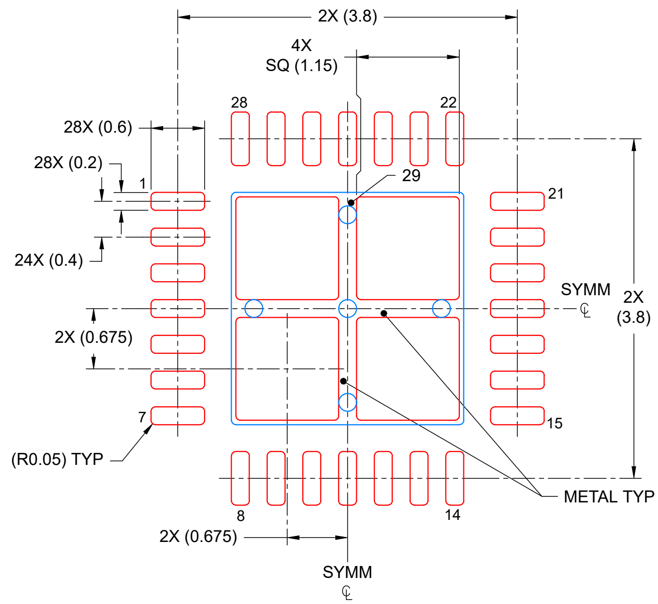
ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

RUY0028A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 15X

4219146/C 03/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
XMSPM0G1218SRGZR	Active	Preproduction	VQFN (RGZ) | 48	4000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
XMSPM0G1218SRHBR	Active	Preproduction	VQFN (RHB) | 32	5000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

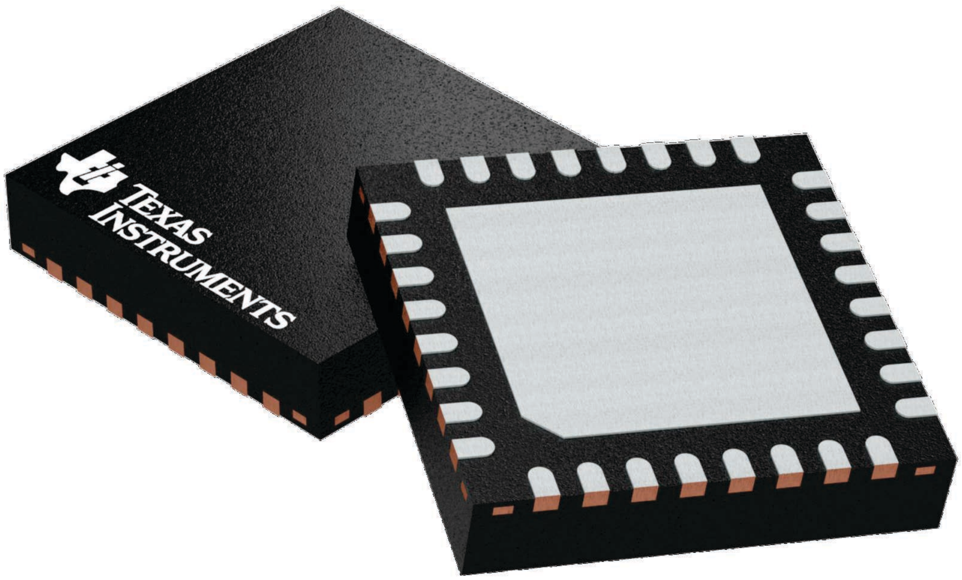
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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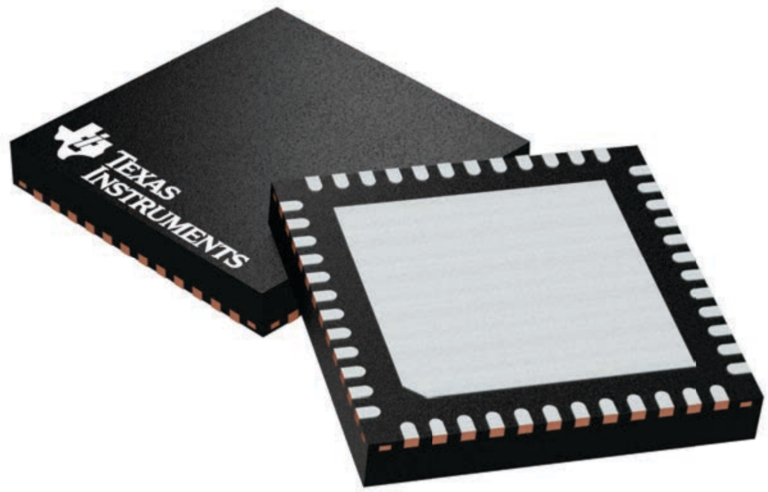
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



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Refer to the product data sheet for package details.

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