

## MSP430FR599x, MSP430FR596x Mixed-Signal Microcontrollers

### 1 Features

- Embedded microcontroller
  - 16-bit RISC architecture up to 16-MHz clock
  - Up to 256KB of ferroelectric random access memory (FRAM)
    - Ultra-low-power writes
    - Fast write at 125 ns per word (64KB in 4 ms)
    - Flexible allocation of data and application code in memory
    - 10<sup>15</sup> write cycle endurance
    - Radiation resistant and nonmagnetic
  - Wide supply voltage range from 3.6 V down to 1.8 V (minimum supply voltage is restricted by SVS levels, see the [SVS specifications](#))
- Optimized ultra-low-power modes
  - Active mode: 118 µA/MHz
  - Standby with VLO (LPM3): 500 nA
  - Standby with real-time clock (RTC) (LPM3.5): 350 nA (the RTC is clocked by a 3.7-pF crystal)
  - Shutdown (LPM4.5): 45 nA
- Low-energy accelerator (LEA) for signal processing (MSP430FR599x only)
  - Operation independent of CPU
  - 4KB of RAM shared with CPU
  - Efficient 256-point complex FFT: Up to 40x faster than Arm® Cortex®-M0+ core
- Intelligent digital peripherals
  - 32-bit hardware multiplier (MPY)
  - 6-channel internal DMA
  - RTC with calendar and alarm functions
  - Six 16-bit timers with up to seven capture/compare registers each
  - 32- and 16-bit cyclic redundancy check (CRC)
- High-performance analog
  - 16-channel analog comparator
  - 12-bit analog-to-digital converter (ADC) featuring window comparator, internal reference and sample-and-hold, up to 20 external input channels
- Multifunction input/output ports
  - All pins support capacitive-touch capability with no need for external components
  - Accessible bit-, byte-, and word-wise (in pairs)
  - Edge-selectable wake from LPM on all ports
  - Programmable pullup and pulldown on all ports
- Code security and encryption
  - 128- or 256-bit AES security encryption and decryption coprocessor
  - Random number seed for random number generation algorithms
  - IP encapsulation protects memory from external access
- Enhanced serial communication
  - Up to four eUSCI\_A serial communication ports
    - UART with automatic baud-rate detection
    - IrDA encode and decode
  - Up to four eUSCI\_B serial communication ports
    - I<sup>2</sup>C with multiple-slave addressing
  - Hardware UART or I<sup>2</sup>C bootloader (BSL)
- Flexible clock system
  - Fixed-frequency DCO with 10 selectable factory-trimmed frequencies
  - Low-power low-frequency internal clock source (VLO)
  - 32-kHz crystals (LFXT)
  - High-frequency crystals (HFXT)
- Development tools and software (also see [Tools and Software](#))
  - Development kits ([MSP-EXP430FR5994](#) LaunchPad™ development kit and [MSP-TS430PN80B](#) target socket board)
  - [MSP430Ware™](#) software for MSP430™ microcontrollers
- [Device Comparison](#) summarizes the available devices

### 2 Applications

- [Grid infrastructure](#)
- [Factory automation & control](#)
- [Building automation](#)
- [Wearable fitness & activity monitor](#)
- [Wearable electronics](#)



### 3 Description

The MSP430FR599x microcontrollers (MCUs) take low power and performance to the next level with the unique low-energy accelerator (LEA) for digital signal processing. This accelerator delivers 40x the performance of Arm® Cortex®-M0+ MCUs to help developers efficiently process data using complex functions such as FFT, FIR, and matrix multiplication. Implementation requires no DSP expertise with a free optimized DSP Library available. Additionally, with up to 256KB of unified memory with FRAM, these devices offer more space for advanced applications and flexibility for effortless implementation of over-the-air firmware updates.

The MSP ultra-low-power (ULP) FRAM microcontroller platform combines uniquely embedded FRAM and a holistic ultra-low-power system architecture, allowing system designers to increase performance while lowering energy consumption. FRAM technology combines the low-energy fast writes, flexibility, and endurance of RAM with the nonvolatile behavior of flash.

MSP430FR599x MCUs are supported by an extensive hardware and software ecosystem with reference designs and code examples to get your design started quickly. Development kits for the MSP430FR599x include the [MSP-EXP430FR5994 LaunchPad™ development kit](#) and the [MSP-TS430PN80B 80-pin target development board](#). TI also provides free [MSP430Ware™ software](#), which is available as a component of Code Composer Studio™ IDE desktop and cloud versions within TI Resource Explorer.

For complete module descriptions, see the [MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx Family User's Guide](#).

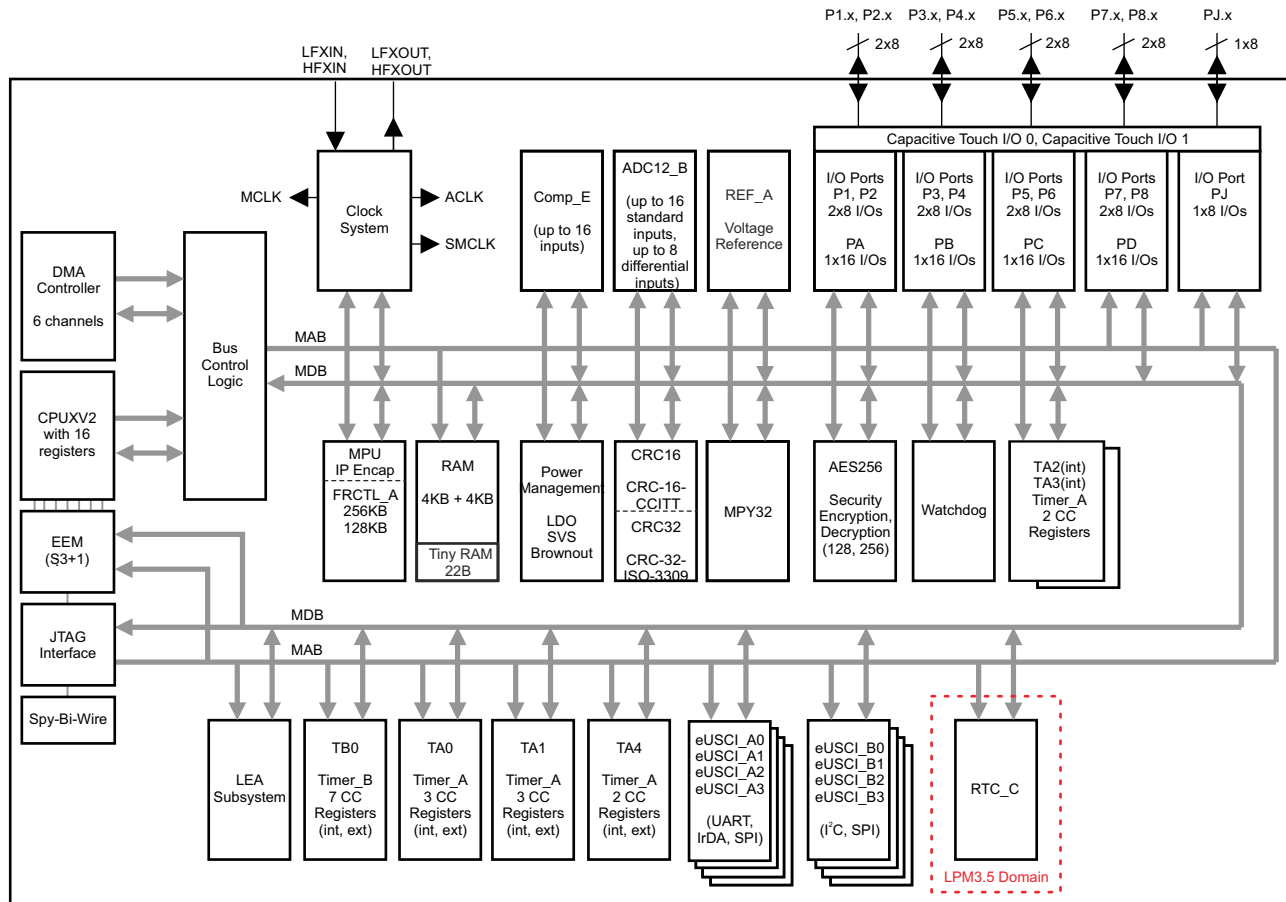
**Device Information**

| PART NUMBER <sup>(1) (2)</sup> | PACKAGE    | BODY SIZE <sup>(3)</sup> |
|--------------------------------|------------|--------------------------|
| MSP430FR5994IZVW               | NFBGA (87) | 6 mm × 6 mm              |
| MSP430FR5994IPN                | LQFP (80)  | 12 mm × 12 mm            |
| MSP430FR5994IPM                | LQFP (64)  | 10 mm × 10 mm            |
| MSP430FR5994IRGZ               | VQFN (48)  | 7 mm × 7 mm              |

- (1) For the most current part, package, and ordering information for all available devices, see the *Package Option Addendum* in [Section 12](#), or see the TI website at [www.ti.com](http://www.ti.com).
- (2) For a comparison of all available device variants, see [Section 6](#).
- (3) The sizes shown here are approximations. For the package dimensions with tolerances, see the *Mechanical Data* in [Section 12](#).

## 4 Functional Block Diagram

Figure 4-1 shows the functional block diagram of the devices.



- A. The device has 8KB of RAM, and 4KB of the RAM is shared with the LEA subsystem. The CPU has priority over the LEA subsystem.
- B. The LEA subsystem is available on the MSP430FR599x MCUs only.

**Figure 4-1. Functional Block Diagram**

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## 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from revision C to revision D

| Changes from August 31, 2018 to January 15, 2021                                                                                                                                                                                         | Page |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| • Updated the numbering format for tables, figures, and cross references throughout the document.....                                                                                                                                    | 1    |
| • Format updates and corrections to external links as needed.....                                                                                                                                                                        | 1    |
| • Changed the column "FRAM Program + Information (KB)" in <a href="#">Section 6, Device Comparison</a> .....                                                                                                                             | 7    |
| • Added ball L5 to the COUT signal on the ZVW package in <a href="#">Section 7.3, Signal Descriptions</a> .....                                                                                                                          | 20   |
| • Added the note that begins "XT1CLK and VLOCLK can be active during LPM4..." .....                                                                                                                                                      | 67   |
| • Added the INTERRUPT VECTOR REGISTER column, moved register names from the INTERRUPT FLAG column, and corrected interrupt flag names as necessary in <a href="#">Table 9-4, Interrupt Sources, Flags, Vectors, and Signatures</a> ..... | 70   |
| • Corrected the interrupt flags for Port 4 to Port 8 in <a href="#">Table 9-4, Interrupt Sources, Flags, and Vectors</a> .....                                                                                                           | 70   |
| • Corrected the note on the P1DIR.x column for the UCB0SOMI/UCB0SCL row (changed eUSCI_A0 to eUSCI_B0) in <a href="#">Table 9-22, Port P1 (P1.6 and P1.7) Pin Functions</a> .....                                                        | 91   |
| • Corrected the value of P5SEL1.5 (changed from 0 to 1) and P5SEL0.5 (from 1 to 0) for the N/A and DVSS rows on P5.5 in <a href="#">Table 9-31, Port P5 (P5.0 to P5.7) Pin Functions</a> .....                                           | 106  |
| • Corrected eUSCI module in the note "Direction controlled by eUSCI_B1 module" (changed from eUSCI_B0 to eUSCI_B1) .....                                                                                                                 | 106  |

Changes from revision B to revision C

| Changes from February 1, 2017 to August 30, 2018                                                                                                                                    | Page |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| • Updated <a href="#">Section 6.1, Related Products</a> .....                                                                                                                       | 8    |
| • Added note (1) to <a href="#">Section 8.12.1.2, SVS</a> .....                                                                                                                     | 38   |
| • Corrected the value of P6SEL1.x (changed from 0 to 1) for the N/A and DVSS rows on P6.5, P6.6, and P6.7 in <a href="#">Table 9-32, Port P6 (P6.0 to P6.7) Pin Functions</a> ..... | 108  |
| • Changed capacitor value from 4.7 $\mu$ F to 470 nF in <a href="#">Figure 10-5, ADC12_B Grounding and Noise Considerations</a> .....                                               | 151  |
| • Changed capacitor value from 4.7 $\mu$ F to 470 nF in the last paragraph of <a href="#">Section 10.2.1.2, Design Requirements</a> .....                                           | 151  |
| • Updated text and figure in <a href="#">Section 11.2, Device Nomenclature</a> .....                                                                                                | 153  |

Changes from revision A to revision B

| Changes from October 18, 2016 to January 31, 2017                                                               | Page |
|-----------------------------------------------------------------------------------------------------------------|------|
| • Changed document status from Advance Information to Production Data.....                                      | 1    |
| • Updated all electrical and timing specifications and typical characteristics graphs with production data..... | 29   |

Changes from initial release to revision A

| Changes from March 17, 2016 to October 17, 2016                                                                                                                                         | Page |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| • Changed from 35x Faster to Up to 40x Faster in the list item that starts "Efficient 256-Point Complex FFT..." in <a href="#">Section 1, Features</a> .....                            | 1    |
| • Added <a href="#">Section 6.1, Related Products</a> .....                                                                                                                             | 8    |
| • Added second row to $t_{\text{Sample}}$ parameter in <a href="#">Section 8.12.9.2, 12-Bit ADC, Timing Parameters</a> .....                                                            | 58   |
| • Removed ADC12DIV from equation for the $t_{\text{CONVERT}}$ TYP time, because ADC12CLK is after division.....                                                                         | 58   |
| • Added " $R_S < 10 \text{ k}\Omega$ " to the note that starts "Approximately 10 Tau ( $\tau$ ) are needed..." on <a href="#">Section 8.12.9.2, 12-Bit ADC, Timing Parameters</a> ..... | 58   |

- 
- Changed from "If the  $\overline{\text{RST}}/\text{NMI}$  pin is unused...with a 2.2-nF pulldown capacitor" to "If the  $\overline{\text{RST}}/\text{NMI}$  pin is unused...with a 10-nF pulldown capacitor" in [Section 10.1.4, Reset](#) ..... [150](#)
-

## 6 Device Comparison

Table 6-1 summarizes the available family members.

**Table 6-1. Device Comparison**

| DEVICE <sup>(1) (2)</sup> | FRAM<br>Program +<br>Information<br>(KB) | SRAM<br>(KB) | CLOCK<br>SYSTEM     | LEA | ADC12_B<br>(Channels)      | Comp_E | Timer_A <sup>(3)</sup>                       | Timer_B <sup>(4)</sup> | eUSCI_A <sup>(5)</sup> | eUSCI_B <sup>(6)</sup> | AES | BSL              | I/Os | PACKAGE                        |
|---------------------------|------------------------------------------|--------------|---------------------|-----|----------------------------|--------|----------------------------------------------|------------------------|------------------------|------------------------|-----|------------------|------|--------------------------------|
| MSP430FR5994              | 256 + 0.5                                | 8            | DCO<br>HFXT<br>LFXT | Yes | 20 external,<br>2 internal | 16 ch. | 3, 3 <sup>(7)</sup><br>2, 2,2 <sup>(8)</sup> | 7                      | 4                      | 4                      | Yes | UART             | 68   | 80 PN (LQFP)<br>87 ZVW (NFBGA) |
|                           |                                          |              |                     |     | 17 external,<br>2 internal |        |                                              |                        | 3                      | 3                      |     |                  | 54   | 64 PM (LQFP)                   |
|                           |                                          |              |                     |     | 16 external,<br>2 internal |        |                                              |                        | 2                      | 1                      |     |                  | 40   | 48 RGZ (VQFN)                  |
| MSP430FR5992              | 128 + 0.5                                | 8            | DCO<br>HFXT<br>LFXT | Yes | 20 external,<br>2 internal | 16 ch. | 3, 3 <sup>(7)</sup><br>2, 2,2 <sup>(8)</sup> | 7                      | 4                      | 4                      | Yes | UART             | 68   | 80 PN (LQFP)<br>87 ZVW (NFBGA) |
|                           |                                          |              |                     |     | 17 external,<br>2 internal |        |                                              |                        | 3                      | 3                      |     |                  | 54   | 64 PM (LQFP)                   |
|                           |                                          |              |                     |     | 16 external,<br>2 internal |        |                                              |                        | 2                      | 1                      |     |                  | 40   | 48 RGZ (VQFN)                  |
| MSP430FR5964              | 256 + 0.5                                | 8            | DCO<br>HFXT<br>LFXT | No  | 20 external,<br>2 internal | 16 ch. | 3, 3 <sup>(7)</sup><br>2, 2,2 <sup>(8)</sup> | 7                      | 4                      | 4                      | Yes | UART             | 68   | 80 PN (LQFP)<br>87 ZVW (NFBGA) |
|                           |                                          |              |                     |     | 17 external,<br>2 internal |        |                                              |                        | 3                      | 3                      |     |                  | 54   | 64 PM (LQFP)                   |
|                           |                                          |              |                     |     | 16 external,<br>2 internal |        |                                              |                        | 2                      | 1                      |     |                  | 40   | 48 RGZ (VQFN)                  |
| MSP430FR5962              | 128 + 0.5                                | 8            | DCO<br>HFXT<br>LFXT | No  | 20 external,<br>2 internal | 16 ch. | 3, 3 <sup>(7)</sup><br>2, 2,2 <sup>(8)</sup> | 7                      | 4                      | 4                      | Yes | UART             | 68   | 80 PN (LQFP)<br>87 ZVW (NFBGA) |
|                           |                                          |              |                     |     | 17 external,<br>2 internal |        |                                              |                        | 3                      | 3                      |     |                  | 54   | 64 PM (LQFP)                   |
|                           |                                          |              |                     |     | 16 external,<br>2 internal |        |                                              |                        | 2                      | 1                      |     |                  | 40   | 48 RGZ (VQFN)                  |
| MSP430FR59941             | 256 + 0.5                                | 8            | DCO<br>HFXT<br>LFXT | Yes | 20 external,<br>2 internal | 16 ch. | 3, 3 <sup>(7)</sup><br>2, 2,2 <sup>(8)</sup> | 7                      | 4                      | 4                      | Yes | I <sup>2</sup> C | 68   | 80 PN (LQFP)<br>87 ZVW (NFBGA) |
|                           |                                          |              |                     |     | 17 external,<br>2 internal |        |                                              |                        | 3                      | 3                      |     |                  | 54   | 64 PM (LQFP)                   |
|                           |                                          |              |                     |     | 16 external,<br>2 internal |        |                                              |                        | 2                      | 1                      |     |                  | 40   | 48 RGZ (VQFN)                  |

(1) For the most current package and ordering information, see the *Package Option Addendum* in Section 12, or see the TI website at [www.ti.com](http://www.ti.com).

(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/packaging](http://www.ti.com/packaging).

(3) Each number in the sequence represents an instantiation of Timer\_A with its associated number of capture/compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer\_A, the first instantiation having 3 capture/compare registers and PWM output generators and the second instantiation having 5 capture/compare registers and PWM output generators, respectively.

- (4) Each number in the sequence represents an instantiation of Timer\_B with its associated number of capture/compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer\_B, the first instantiation having 3 capture/compare registers and PWM output generators and the second instantiation having 5 capture/compare registers and PWM output generators, respectively.
- (5) eUSCI\_A supports UART with automatic baud-rate detection, IrDA encode and decode, and SPI.
- (6) eUSCI\_B supports I<sup>2</sup>C with multiple slave addresses and SPI.
- (7) Timers TA0 and TA1 provide internal and external capture/compare inputs and internal and external PWM outputs.
- (8) Timers TA2 and TA3 provide only internal capture/compare inputs and only internal PWM outputs (if any). Timer TA4 provides internal and external capture/compare inputs and internal and external PWM outputs.

Note: TA4 in the RGZ package provides only internal capture/compare inputs and only internal PWM outputs.

## 6.1 Related Products

For information about other devices in this family of products or related products, see the following links.

[16-bit and 32-bit microcontrollers](#)

High-performance, low-power solutions to enable the autonomous future

[Products for MSP430 ultra-low-power sensing & measurement MCUs](#)

One platform. One ecosystem. Endless possibilities.

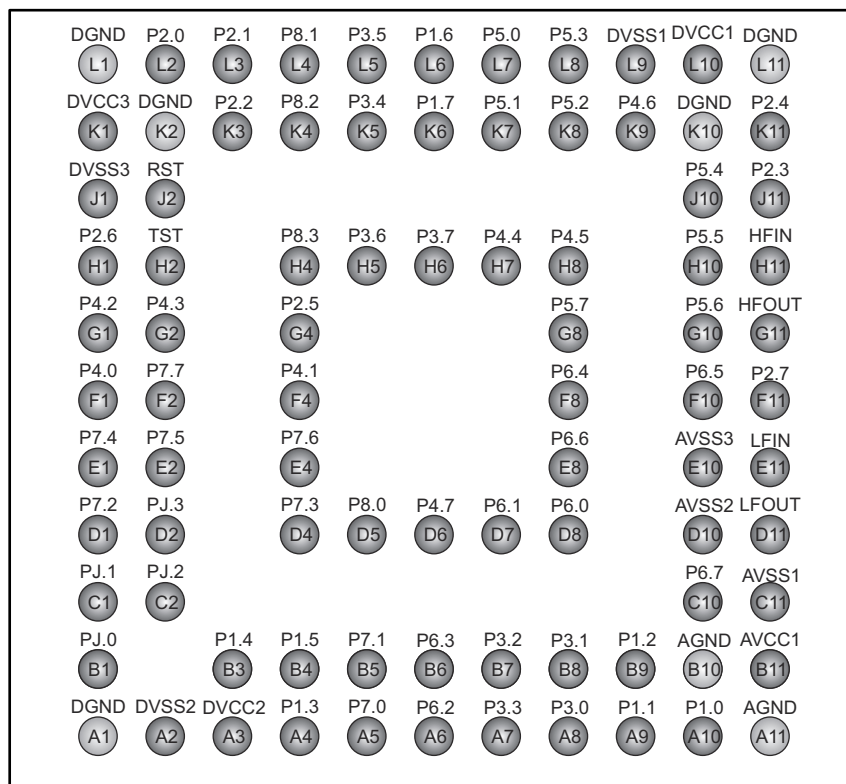
[Reference designs for MSP430FR5994](#)

Find reference designs leveraging the best in TI technology – from analog and power management to embedded processors.

## 7 Terminal Configuration and Functions

### 7.1 Pin Diagrams

Figure 7-1 shows the bottom view of the pinout of the 87-pin ZVW package, and Figure 7-2 shows the top view of the pinout.



On devices with UART BSL: P2.0 is BSLTX, P2.1 is BSLRX

On devices with I<sup>2</sup>C BSL: P1.6 is BSLSDA, P1.7 is BSLSCL

**Figure 7-1. 87-Pin ZVW Package (Bottom View)**

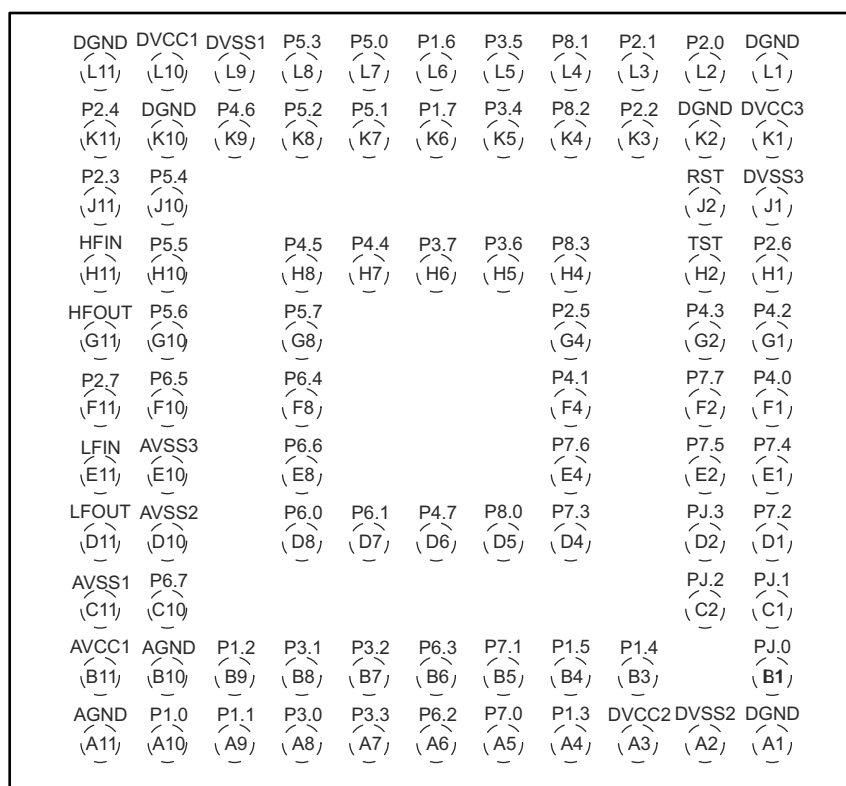
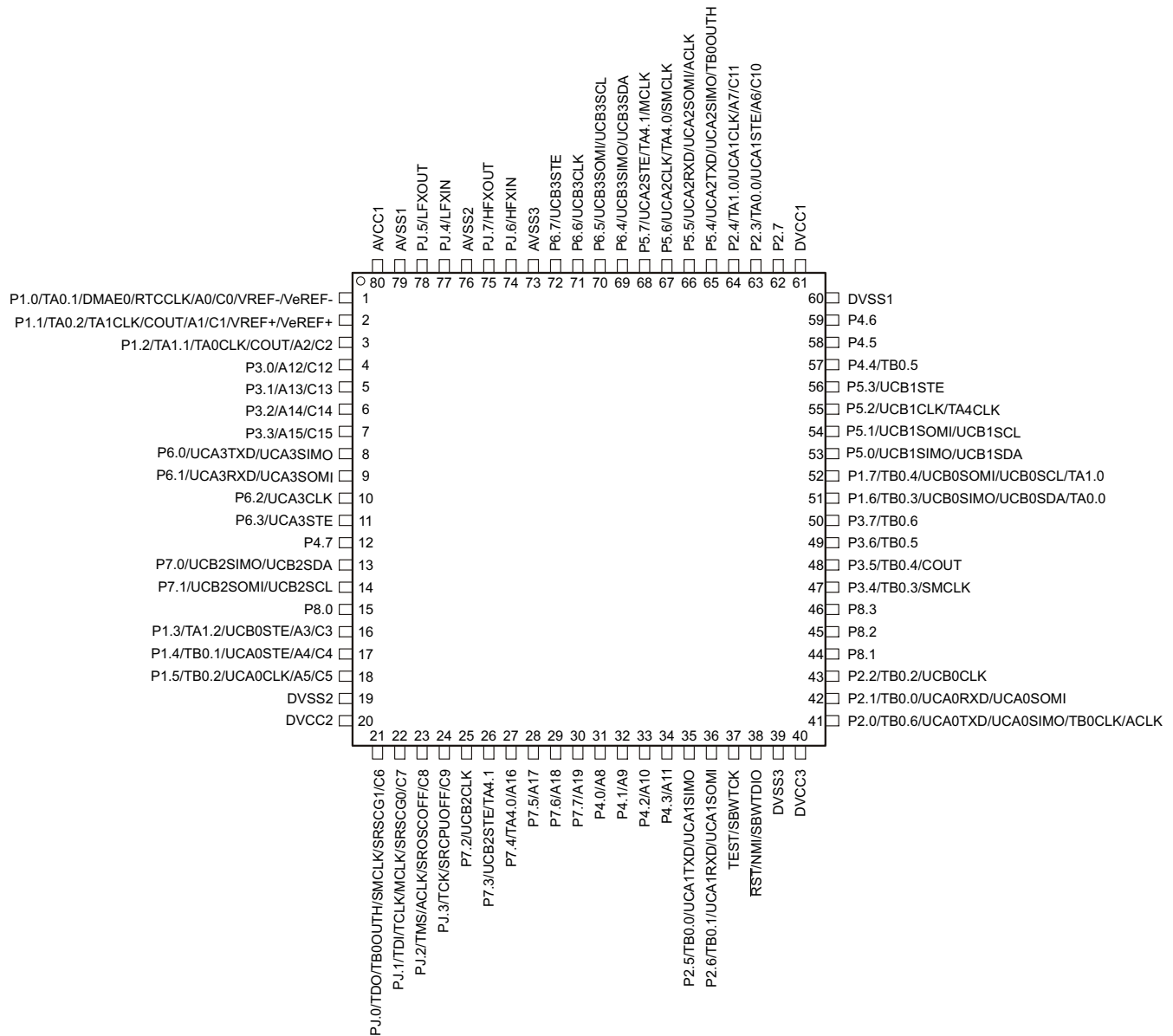


Figure 7-2. 87-Pin ZVW Package (Top View)

Figure 7-3 shows the pinout of the 80-pin PN package.

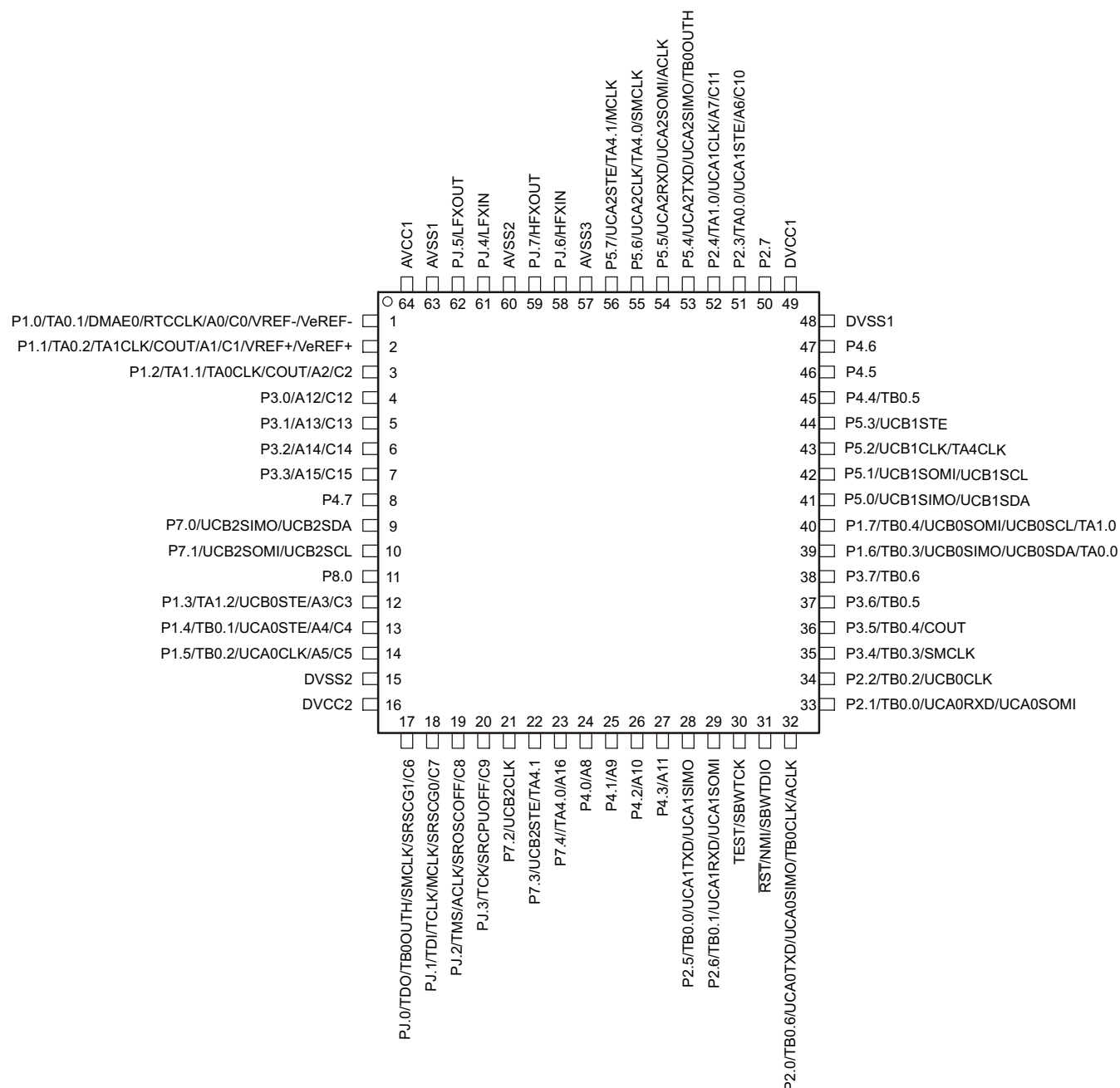


On devices with UART BSL: P2.0 is BSLTX, P2.1 is BSLRX

On devices with I<sup>2</sup>C BSL: P1.6 is BSLSDA, P1.7 is BSLSCL

**Figure 7-3. 80-Pin PN Package (Top View)**

Figure 7-4 shows the pinout of the 64-pin PM package.

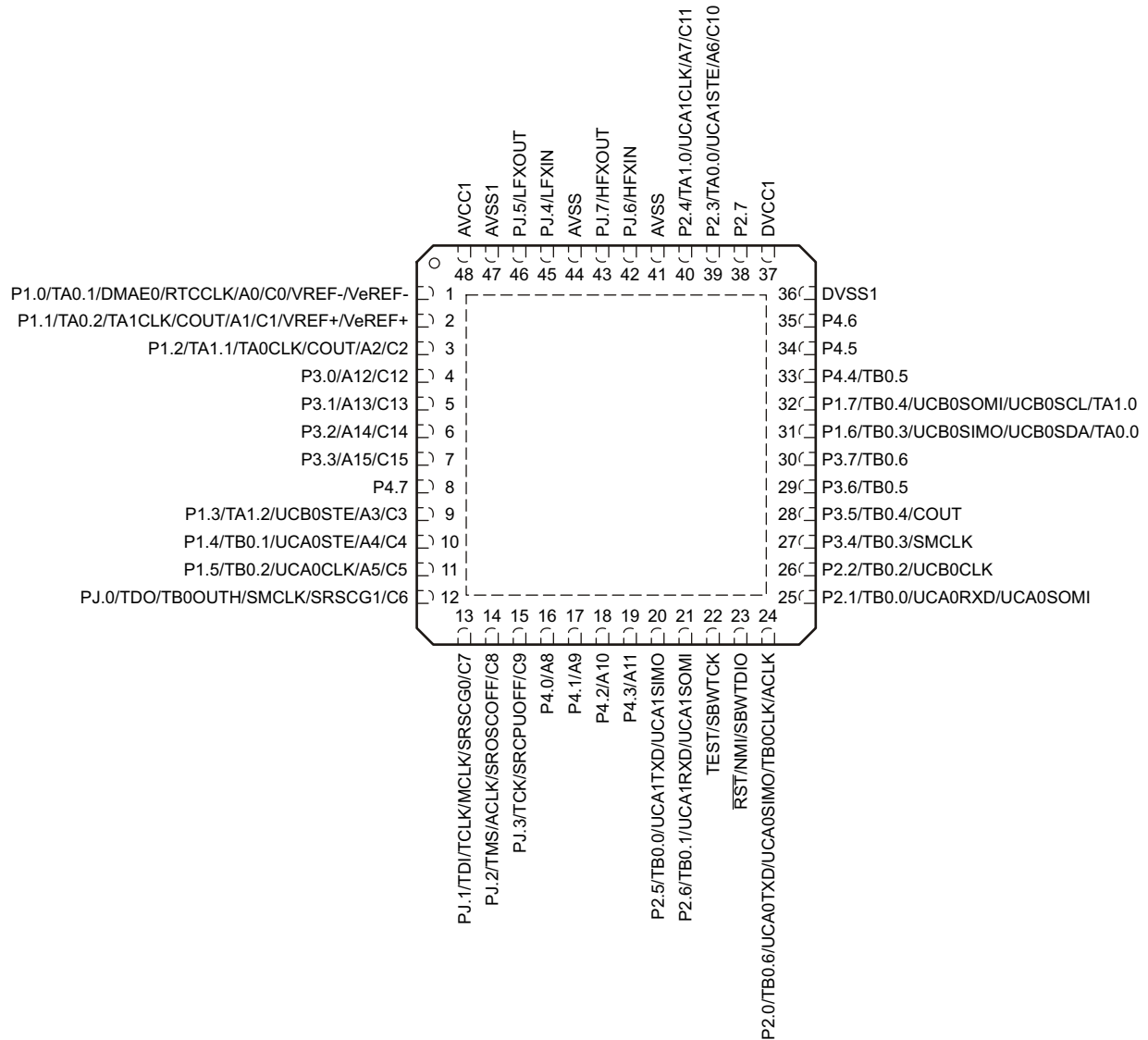


On devices with UART BSL: P2.0 is BSLTX, P2.1 is BSLRX

On devices with I<sup>2</sup>C BSL: P1.6 is BSLSDA, P1.7 is BSLSCL

**Figure 7-4. 64-Pin PM Package (Top View)**

Figure 7-5 shows the pinout of the 48-pin RGZ package.



TI recommends connecting the QFN thermal pad to  $V_{SS}$ .  
On devices with UART BSL: P2.0 is BSLTX, P2.1 is BSLRX  
On devices with I<sup>2</sup>C BSL: P1.6 is BSLSDA, P1.7 is BSLSCL

**Figure 7-5. 48-Pin RGZ Package (Top View)**

## 7.2 Pin Attributes

Table 7-1 summarizes the attributes of the pins.

**Table 7-1. Pin Attributes**

| PIN NUMBER <sup>(1)</sup> |    |     |     | SIGNAL NAME <sup>(2) (3)</sup> | SIGNAL TYPE <sup>(4)</sup> | BUFFER TYPE <sup>(5)</sup> | POWER SOURCE <sup>(6)</sup> | RESET STATE AFTER BOR <sup>(7)</sup> |
|---------------------------|----|-----|-----|--------------------------------|----------------------------|----------------------------|-----------------------------|--------------------------------------|
| PN                        | PM | RGZ | ZVW |                                |                            |                            |                             |                                      |
| 1                         | 1  | 1   | A10 | P1.0                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | TA0.1                          | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | DMAE0                          | I                          | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | RTCCLK                         | O                          | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | A0                             | I                          | Analog                     | DVCC                        | –                                    |
|                           |    |     |     | C0                             | I                          | Analog                     | DVCC                        | –                                    |
|                           |    |     |     | VREF-                          | O                          | Analog                     | DVCC                        | –                                    |
|                           |    |     |     | VeREF-                         | I                          | Analog                     | DVCC                        | –                                    |
| 2                         | 2  | 2   | A9  | P1.1                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | TA0.2                          | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | TA1CLK                         | I                          | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | COUT                           | O                          | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | A1                             | I                          | Analog                     | DVCC                        | –                                    |
|                           |    |     |     | C1                             | I                          | Analog                     | DVCC                        | –                                    |
|                           |    |     |     | VREF+                          | O                          | Analog                     | DVCC                        | –                                    |
|                           |    |     |     | VeREF+                         | I                          | Analog                     | DVCC                        | –                                    |
| 3                         | 3  | 3   | B9  | P1.2                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | TA1.1                          | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | TA0CLK                         | I                          | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | COUT                           | O                          | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | A2                             | I                          | Analog                     | DVCC                        | –                                    |
|                           |    |     |     | C2                             | I                          | Analog                     | DVCC                        | –                                    |
| 4                         | 4  | 4   | A8  | P3.0                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | A12                            | I                          | Analog                     | DVCC                        | –                                    |
|                           |    |     |     | C12                            | I                          | Analog                     | DVCC                        | –                                    |
| 5                         | 5  | 5   | B8  | P3.1                           | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | A13                            | I                          | Analog                     | DVCC                        | –                                    |
|                           |    |     |     | C13                            | I                          | Analog                     | DVCC                        | –                                    |
| 6                         | 6  | 6   | B7  | P3.2                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | A14                            | I                          | Analog                     | DVCC                        | –                                    |
|                           |    |     |     | C14                            | I                          | Analog                     | DVCC                        | –                                    |
| 7                         | 7  | 7   | A7  | P3.3                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | A15                            | I                          | Analog                     | DVCC                        | –                                    |
|                           |    |     |     | C15                            | I                          | Analog                     | DVCC                        | –                                    |
| 8                         | –  | –   | D8  | P6.0                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | UCA3TXD                        | O                          | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | UCA3SIMO                       | I/O                        | LVC MOS                    | DVCC                        | –                                    |
| 9                         | –  | –   | D7  | P6.1                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | UCA3RXD                        | I                          | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | UCA3SOMI                       | I/O                        | LVC MOS                    | DVCC                        | –                                    |

**Table 7-1. Pin Attributes (continued)**

| PIN NUMBER <sup>(1)</sup> |    |     |     | SIGNAL NAME <sup>(2) (3)</sup> | SIGNAL TYPE <sup>(4)</sup> | BUFFER TYPE <sup>(5)</sup> | POWER SOURCE <sup>(6)</sup> | RESET STATE AFTER BOR <sup>(7)</sup> |
|---------------------------|----|-----|-----|--------------------------------|----------------------------|----------------------------|-----------------------------|--------------------------------------|
| PN                        | PM | RGZ | ZVW |                                |                            |                            |                             |                                      |
| 10                        | –  | –   | A6  | P6.2                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | UCA3CLK                        | I/O                        | LVC MOS                    | DVCC                        | –                                    |
| 11                        | –  | –   | B6  | P6.3                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | UCA3STE                        | I/O                        | LVC MOS                    | DVCC                        | –                                    |
| 12                        | 8  | 8   | D6  | P4.7                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
| 13                        | 9  | –   | A5  | P7.0                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | UCB2SIMO                       | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | UCB2SDA                        | I/O                        | LVC MOS                    | DVCC                        | –                                    |
| 14                        | 10 | –   | B5  | P7.1                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | UCB2SOMI                       | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | UCB2SCL                        | I/O                        | LVC MOS                    | DVCC                        | –                                    |
| 15                        | 11 | –   | D5  | P8.0                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
| 16                        | 12 | 9   | A4  | P1.3                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | TA1.2                          | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | UCB0STE                        | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | A3                             | I                          | Analog                     | DVCC                        | –                                    |
|                           |    |     |     | C3                             | I                          | Analog                     | DVCC                        | –                                    |
| 17                        | 13 | 10  | B3  | P1.4                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | TB0.1                          | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | UCA0STE                        | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | A4                             | I                          | Analog                     | DVCC                        | –                                    |
|                           |    |     |     | C4                             | I                          | Analog                     | DVCC                        | –                                    |
| 18                        | 14 | 11  | B4  | P1.5                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | TB0.2                          | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | UCA0CLK                        | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | A5                             | I                          | Analog                     | DVCC                        | –                                    |
|                           |    |     |     | C5                             | I                          | Analog                     | DVCC                        | –                                    |
| 19                        | 15 | –   | A2  | DVSS2                          | P                          | Power                      | –                           | N/A                                  |
| 20                        | 16 | –   | A3  | DVCC2                          | P                          | Power                      | –                           | N/A                                  |
| 21                        | 17 | 12  | B1  | PJ.0                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | TDO                            | O                          | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | TB0OUTH                        | I                          | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | SMCLK                          | O                          | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | SRSCG1                         | O                          | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | C6                             | I                          | Analog                     | DVCC                        | –                                    |
| 22                        | 18 | 13  | C1  | PJ.1                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | TDI                            | I                          | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | TCLK                           | I                          | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | MCLK                           | O                          | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | SRSCG0                         | O                          | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | C7                             | I                          | Analog                     | DVCC                        | –                                    |

Table 7-1. Pin Attributes (continued)

| PIN NUMBER <sup>(1)</sup> |    |     |     | SIGNAL NAME <sup>(2) (3)</sup> | SIGNAL TYPE <sup>(4)</sup> | BUFFER TYPE <sup>(5)</sup> | POWER SOURCE <sup>(6)</sup> | RESET STATE AFTER BOR <sup>(7)</sup> |
|---------------------------|----|-----|-----|--------------------------------|----------------------------|----------------------------|-----------------------------|--------------------------------------|
| PN                        | PM | RGZ | ZVW |                                |                            |                            |                             |                                      |
| 23                        | 19 | 14  | C2  | PJ.2                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | TMS                            | I                          | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | ACLK                           | O                          | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | SROSCOFF                       | O                          | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | C8                             | I                          | Analog                     | DVCC                        | –                                    |
| 24                        | 20 | 15  | D2  | PJ.3                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | TCK                            | I                          | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | SRCPUOFF                       | O                          | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | C9                             | I                          | Analog                     | DVCC                        | –                                    |
| 25                        | 21 | –   | D1  | P7.2                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | UCB2CLK                        | I/O                        | LVC MOS                    | DVCC                        | –                                    |
| 26                        | 22 | –   | D4  | P7.3                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | UCB2STE                        | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | TA4.1                          | I/O                        | LVC MOS                    | DVCC                        | –                                    |
| 27                        | 23 | –   | E1  | P7.4                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | TA4.0                          | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | A16                            | I                          | Analog                     | DVCC                        | –                                    |
| 28                        | –  | –   | E2  | P7.5                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | A17                            | I                          | Analog                     | DVCC                        | –                                    |
| 29                        | –  | –   | E4  | P7.6                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | A18                            | I                          | Analog                     | DVCC                        | –                                    |
| 30                        | –  | –   | F2  | P7.7                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | A19                            | I                          | Analog                     | DVCC                        | –                                    |
| 31                        | 24 | 16  | F1  | P4.0                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | A8                             | I                          | Analog                     | DVCC                        | –                                    |
| 32                        | 25 | 17  | F4  | P4.1                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | A9                             | I                          | Analog                     | DVCC                        | –                                    |
| 33                        | 26 | 18  | G1  | P4.2                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | A10                            | I                          | Analog                     | DVCC                        | –                                    |
| 34                        | 27 | 19  | G2  | P4.3                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | A11                            | I                          | Analog                     | DVCC                        | –                                    |
| 35                        | 28 | 20  | G4  | P2.5                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | TB0.0                          | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | UCA1TXD                        | O                          | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | UCA1SIMO                       | I/O                        | LVC MOS                    | DVCC                        | –                                    |
| 36                        | 29 | 21  | H1  | P2.6                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | TB0.1                          | O                          | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | UCA1RXD                        | I                          | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | UCA1SOMI                       | I/O                        | LVC MOS                    | DVCC                        | –                                    |
| 37                        | 30 | 22  | H2  | TEST                           | I                          | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | SBWTCK                         | I                          | LVC MOS                    | DVCC                        | –                                    |
| 38                        | 31 | 23  | J2  | RST                            | I                          | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | NMI                            | I                          | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | SBWTDIO                        | I/O                        | LVC MOS                    | DVCC                        | –                                    |

**Table 7-1. Pin Attributes (continued)**

| PIN NUMBER <sup>(1)</sup> |    |     |     | SIGNAL NAME <sup>(2) (3)</sup> | SIGNAL TYPE <sup>(4)</sup> | BUFFER TYPE <sup>(5)</sup> | POWER SOURCE <sup>(6)</sup> | RESET STATE AFTER BOR <sup>(7)</sup> |
|---------------------------|----|-----|-----|--------------------------------|----------------------------|----------------------------|-----------------------------|--------------------------------------|
| PN                        | PM | RGZ | ZVW |                                |                            |                            |                             |                                      |
| 39                        | –  | –   | J1  | DVSS3                          | P                          | Power                      | –                           | N/A                                  |
| 40                        | –  | –   | K1  | DVCC3                          | P                          | Power                      | –                           | N/A                                  |
| 41                        | 32 | 24  | L2  | P2.0                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | TB0.6                          | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | UCA0TXD                        | O                          | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | BSLTX                          | O                          | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | UCA0SIMO                       | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | TB0CLK                         | I                          | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | ACLK                           | O                          | LVC MOS                    | DVCC                        | –                                    |
| 42                        | 33 | 25  | L3  | P2.1                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | TB0.0                          | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | UCA0RXD                        | I                          | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | BSLRX                          | I                          | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | UCA0SOMI                       | I/O                        | LVC MOS                    | DVCC                        | –                                    |
| 43                        | 34 | 26  | K3  | P2.2                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | TB0.2                          | O                          | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | UCB0CLK                        | I/O                        | LVC MOS                    | DVCC                        | –                                    |
| 44                        | –  | –   | L4  | P8.1                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
| 45                        | –  | –   | K4  | P8.2                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
| 46                        | –  | –   | H4  | P8.3                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
| 47                        | 35 | 27  | K5  | P3.4                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | TB0.3                          | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | SMCLK                          | O                          | LVC MOS                    | DVCC                        | –                                    |
| 48                        | 36 | 28  | L5  | P3.5                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | TB0.4                          | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | COUT                           | O                          | LVC MOS                    | DVCC                        | –                                    |
| 49                        | 37 | 29  | H5  | P3.6                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | TB0.5                          | I/O                        | LVC MOS                    | DVCC                        | –                                    |
| 50                        | 38 | 30  | H6  | P3.7                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | TB0.6                          | I/O                        | LVC MOS                    | DVCC                        | –                                    |
| 51                        | 39 | 31  | L6  | P1.6                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | TB0.3                          | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | UCB0SIMO                       | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | UCB0SDA                        | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | BSLSDA                         | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | TA0.0                          | I/O                        | LVC MOS                    | DVCC                        | –                                    |
| 52                        | 40 | 32  | K6  | P1.7                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | TB0.4                          | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | UCB0SOMI                       | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | UCB0SCL                        | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | BSLSCL                         | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | TA1.0                          | I/O                        | LVC MOS                    | DVCC                        | –                                    |

Table 7-1. Pin Attributes (continued)

| PIN NUMBER <sup>(1)</sup> |    |     |     | SIGNAL NAME <sup>(2) (3)</sup> | SIGNAL TYPE <sup>(4)</sup> | BUFFER TYPE <sup>(5)</sup> | POWER SOURCE <sup>(6)</sup> | RESET STATE AFTER BOR <sup>(7)</sup> |
|---------------------------|----|-----|-----|--------------------------------|----------------------------|----------------------------|-----------------------------|--------------------------------------|
| PN                        | PM | RGZ | ZVW |                                |                            |                            |                             |                                      |
| 53                        | 41 | –   | L7  | P5.0                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | UCB1SIMO                       | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | UCB1SDA                        | I/O                        | LVC MOS                    | DVCC                        | –                                    |
| 54                        | 42 | –   | K7  | P5.1                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | UCB1SOMI                       | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | UCB1SCL                        | I/O                        | LVC MOS                    | DVCC                        | –                                    |
| 55                        | 43 | –   | K8  | P5.2                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | UCB1CLK                        | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | TA4CLK                         | I                          | LVC MOS                    | DVCC                        | –                                    |
| 56                        | 44 | –   | L8  | P5.3                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | UCB1STE                        | I/O                        | LVC MOS                    | DVCC                        | –                                    |
| 57                        | 45 | 33  | H7  | P4.4                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | TB0.5                          | I/O                        | LVC MOS                    | DVCC                        | –                                    |
| 58                        | 46 | 34  | H8  | P4.5                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
| 59                        | 47 | 35  | K9  | P4.6                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
| 60                        | 48 | 36  | L9  | DVSS1                          | P                          | Power                      | –                           | N/A                                  |
| 61                        | 49 | 37  | L10 | DVCC1                          | P                          | Power                      | –                           | N/A                                  |
| 62                        | 50 | 38  | F11 | P2.7                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
| 63                        | 51 | 39  | J11 | P2.3                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | TA0.0                          | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | UCA1STE                        | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | A6                             | I                          | Analog                     | DVCC                        | –                                    |
|                           |    |     |     | C10                            | I                          | Analog                     | DVCC                        | –                                    |
| 64                        | 52 | 40  | K11 | P2.4                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | TA1.0                          | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | UCA1CLK                        | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | A7                             | I                          | Analog                     | DVCC                        | –                                    |
|                           |    |     |     | C11                            | I                          | Analog                     | DVCC                        | –                                    |
| 65                        | 53 | –   | J10 | P5.4                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | UCA2TXD                        | O                          | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | UCA2SIMO                       | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | TB0OUTH                        | I                          | LVC MOS                    | DVCC                        | –                                    |
| 66                        | 54 | –   | H10 | P5.5                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | UCA2RXD                        | I                          | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | UCA2SOMI                       | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | ACLK                           | O                          | LVC MOS                    | DVCC                        | –                                    |
| 67                        | 55 | –   | G10 | P5.6                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | UCA2CLK                        | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | TA4.0                          | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | SMCLK                          | O                          | LVC MOS                    | DVCC                        | –                                    |
| 68                        | 56 | –   | G8  | P5.7                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | UCA2STE                        | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | TA4.1                          | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | MCLK                           | O                          | LVC MOS                    | DVCC                        | –                                    |

**Table 7-1. Pin Attributes (continued)**

| PIN NUMBER <sup>(1)</sup> |    |     |     | SIGNAL NAME <sup>(2) (3)</sup> | SIGNAL TYPE <sup>(4)</sup> | BUFFER TYPE <sup>(5)</sup> | POWER SOURCE <sup>(6)</sup> | RESET STATE AFTER BOR <sup>(7)</sup> |
|---------------------------|----|-----|-----|--------------------------------|----------------------------|----------------------------|-----------------------------|--------------------------------------|
| PN                        | PM | RGZ | ZVW |                                |                            |                            |                             |                                      |
| 69                        | –  | –   | F8  | P6.4                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | UCB3SIMO                       | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | UCB3SDA                        | I/O                        | LVC MOS                    | DVCC                        | –                                    |
| 70                        | –  | –   | F10 | P6.5                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | UCB3SOMI                       | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | UCB3SCL                        | I/O                        | LVC MOS                    | DVCC                        | –                                    |
| 71                        | –  | –   | E8  | P6.6                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | UCB3CLK                        | I/O                        | LVC MOS                    | DVCC                        | –                                    |
| 72                        | –  | –   | C10 | P6.7                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | UCB3STE                        | I/O                        | LVC MOS                    | DVCC                        | –                                    |
| 73                        | 57 | 41  | E10 | AVSS3                          | P                          | Power                      | –                           | N/A                                  |
| 74                        | 58 | 42  | H11 | PJ.6                           | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|                           |    |     |     | HFXIN                          | I                          | Analog                     | DVCC                        | –                                    |
| 75                        | 59 | 43  | G11 | PJ.7                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | HFXOUT                         | O                          | Analog                     | DVCC                        | –                                    |
| 76                        | 60 | 44  | D10 | AVSS2                          | P                          | Power                      | –                           | N/A                                  |
| 77                        | 61 | 45  | E11 | PJ.4                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | LFXIN                          | I                          | Analog                     | DVCC                        | –                                    |
| 78                        | 62 | 46  | D11 | PJ.5                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|                           |    |     |     | LFXOUT                         | O                          | Analog                     | DVCC                        | –                                    |
| 79                        | 63 | 47  | C11 | AVSS1                          | P                          | Power                      | –                           | N/A                                  |
| 80                        | 64 | 48  | B11 | AVCC1                          | P                          | Power                      | –                           | N/A                                  |
| –                         | –  | –   | A1  | DGND                           | P                          | Power                      | –                           | N/A                                  |
| –                         | –  | –   | A11 | AGND                           | P                          | Power                      | –                           | N/A                                  |
| –                         | –  | –   | B10 | AGND                           | P                          | Power                      | –                           | N/A                                  |
| –                         | –  | –   | K2  | DGND                           | P                          | Power                      | –                           | N/A                                  |
| –                         | –  | –   | K10 | DGND                           | P                          | Power                      | –                           | N/A                                  |
| –                         | –  | –   | L1  | DGND                           | P                          | Power                      | –                           | N/A                                  |
| –                         | –  | –   | L11 | DGND                           | P                          | Power                      | –                           | N/A                                  |
| –                         | –  | Pad | –   | QFN Pad                        | P                          | Power                      | –                           | N/A                                  |

(1) N/A = not available

(2) The signal that is listed first for each pin is the reset default pin name.

(3) Signal Types: I = Input, O = Output, I/O = Input or Output.

(4) Buffer Types: LVC MOS, Analog, or Power (see [Table 7-3](#) for details)

(5) To determine the pin mux encodings for each pin, see [Section 9.13](#).

(6) The power source shown in this table is the I/O power source, which may differ from the module power source.

(7) Reset States:

OFF = High impedance with Schmitt-trigger input and pullup or pulldown (if available) disabled

N/A = Not applicable

## 7.3 Signal Descriptions

Section 7.3 describes the signals for all device variants and package options.

**Table 7-2. Signal Descriptions**

| FUNCTION               | SIGNAL NAME | PIN NO. <sup>(1)</sup> |                |                |          | PIN TYPE <sup>(2)</sup> | DESCRIPTION                                                 |
|------------------------|-------------|------------------------|----------------|----------------|----------|-------------------------|-------------------------------------------------------------|
|                        |             | ZVW                    | PN             | PM             | RGZ      |                         |                                                             |
| ADC                    | A0          | A10                    | 1              | 1              | 1        | I                       | ADC analog input A0                                         |
|                        | A1          | A9                     | 2              | 2              | 2        | I                       | ADC analog input A1                                         |
|                        | A2          | B9                     | 3              | 3              | 3        | I                       | ADC analog input A2                                         |
|                        | A3          | A4                     | 16             | 12             | 9        | I                       | ADC analog input A3                                         |
|                        | A4          | B3                     | 17             | 13             | 10       | I                       | ADC analog input A4                                         |
|                        | A5          | B4                     | 18             | 14             | 11       | I                       | ADC analog input A5                                         |
|                        | A6          | J11                    | 63             | 51             | 39       | I                       | ADC analog input A6                                         |
|                        | A7          | K11                    | 64             | 52             | 40       | I                       | ADC analog input A7                                         |
|                        | A8          | F1                     | 31             | 24             | 16       | I                       | ADC analog input A8                                         |
|                        | A9          | F4                     | 32             | 25             | 17       | I                       | ADC analog input A9                                         |
|                        | A10         | G1                     | 33             | 26             | 18       | I                       | ADC analog input A10                                        |
|                        | A11         | G2                     | 34             | 27             | 19       | I                       | ADC analog input A11                                        |
|                        | A12         | A8                     | 4              | 4              | 4        | I                       | ADC analog input A12                                        |
|                        | A13         | B8                     | 5              | 5              | 5        | I                       | ADC analog input A13                                        |
|                        | A14         | B7                     | 6              | 6              | 6        | I                       | ADC analog input A14                                        |
|                        | A15         | A7                     | 7              | 7              | 7        | I                       | ADC analog input A15                                        |
|                        | A16         | E1                     | 27             | 23             | –        | I                       | ADC analog input A16                                        |
|                        | A17         | E2                     | 28             | –              | –        | I                       | ADC analog input A17                                        |
|                        | A18         | E4                     | 29             | –              | –        | I                       | ADC analog input A18                                        |
|                        | A19         | F2                     | 30             | –              | –        | I                       | ADC analog input A19                                        |
| BSL (I <sup>2</sup> C) | VREF+       | A9                     | 2              | 2              | 2        | O                       | Output of positive reference voltage                        |
|                        | VREF-       | A10                    | 1              | 1              | 1        | O                       | Output of negative reference voltage                        |
| BSL (UART)             | VeREF+      | A9                     | 2              | 2              | 2        | I                       | Input for an external positive reference voltage to the ADC |
|                        | VeREF-      | A10                    | 1              | 1              | 1        | I                       | Input for an external negative reference voltage to the ADC |
| BSL (I <sup>2</sup> C) | BSLSCL      | K6                     | 52             | 40             | 32       | I/O                     | I <sup>2</sup> C BSL clock                                  |
|                        | BSLSDA      | L6                     | 51             | 39             | 31       | I/O                     | I <sup>2</sup> C BSL data                                   |
| BSL (UART)             | BSLRX       | L3                     | 42             | 33             | 25       | I                       | UART BSL receive                                            |
|                        | BSLTX       | L2                     | 41             | 32             | 24       | O                       | UART BSL transmit                                           |
| Clock                  | ACLK        | C2<br>H10              | 23<br>41<br>66 | 19<br>32<br>54 | 14<br>24 | O                       | ACLK output                                                 |
|                        | HFXIN       | H11                    | 74             | 58             | 42       | I                       | Input for high-frequency crystal oscillator HFXT            |
|                        | HFXOUT      | G11                    | 75             | 59             | 43       | O                       | Output for high-frequency crystal oscillator HFXT           |
|                        | LFXIN       | E11                    | 77             | 61             | 45       | I                       | Input for low-frequency crystal oscillator LFXT             |
|                        | LFXOUT      | D11                    | 78             | 62             | 46       | O                       | Output of low-frequency crystal oscillator LFXT             |
|                        | MCLK        | C1<br>G8               | 22<br>68       | 18<br>56       | 13       | O                       | MCLK output                                                 |
|                        | SMCLK       | B1<br>G10              | 21<br>47<br>67 | 17<br>35<br>55 | 12<br>27 | O                       | SMCLK output                                                |

**Table 7-2. Signal Descriptions (continued)**

| FUNCTION   | SIGNAL NAME | PIN NO. <sup>(1)</sup> |              |              |              | PIN TYPE <sup>(2)</sup> | DESCRIPTION                                     |
|------------|-------------|------------------------|--------------|--------------|--------------|-------------------------|-------------------------------------------------|
|            |             | ZVW                    | PN           | PM           | RGZ          |                         |                                                 |
| Comparator | C0          | A10                    | 1            | 1            | 1            | I                       | Comparator input C0                             |
|            | C1          | A9                     | 2            | 2            | 2            | I                       | Comparator input C1                             |
|            | C2          | B9                     | 3            | 3            | 3            | I                       | Comparator input C2                             |
|            | C3          | A4                     | 16           | 12           | 9            | I                       | Comparator input C3                             |
|            | C4          | B3                     | 17           | 13           | 10           | I                       | Comparator input C4                             |
|            | C5          | B4                     | 18           | 14           | 11           | I                       | Comparator input C5                             |
|            | C6          | B1                     | 21           | 17           | 12           | I                       | Comparator input C6                             |
|            | C7          | C1                     | 22           | 18           | 13           | I                       | Comparator input C7                             |
|            | C8          | C2                     | 23           | 19           | 14           | I                       | Comparator input C8                             |
|            | C9          | D2                     | 24           | 20           | 15           | I                       | Comparator input C9                             |
|            | C10         | J11                    | 63           | 51           | 39           | I                       | Comparator input C10                            |
|            | C11         | K11                    | 64           | 52           | 40           | I                       | Comparator input C11                            |
|            | C12         | A8                     | 4            | 4            | 4            | I                       | Comparator input C12                            |
|            | C13         | B8                     | 5            | 5            | 5            | I                       | Comparator input C13                            |
|            | C14         | B7                     | 6            | 6            | 6            | I                       | Comparator input C14                            |
|            | C15         | A7                     | 7            | 7            | 7            | I                       | Comparator input C15                            |
|            | COU         | A9<br>B9<br>L5         | 2<br>3<br>48 | 2<br>3<br>36 | 2<br>3<br>28 | O                       | Comparator output                               |
| DMA        | DMAE0       | A10                    | 1            | 1            | 1            | I                       | External DMA trigger                            |
| Debug      | SBWTCK      | H2                     | 37           | 30           | 22           | I                       | Spy-Bi-Wire input clock                         |
|            | SBWTDIO     | J2                     | 38           | 31           | 23           | I/O                     | Spy-Bi-Wire data input/output                   |
|            | SRCPUOFF    | D2                     | 24           | 20           | 15           | O                       | Low-power debug: CPU Status register bit CPUOFF |
|            | SROSCOFF    | C2                     | 23           | 19           | 14           | O                       | Low-power debug: CPU Status register bit OSCOFF |
|            | SRSCG0      | C1                     | 22           | 18           | 13           | O                       | Low-power debug: CPU Status register bit SCG0   |
|            | SRSCG1      | B1                     | 21           | 17           | 12           | O                       | Low-power debug: CPU Status register bit SCG1   |
|            | TCK         | D2                     | 24           | 20           | 15           | I                       | Test clock                                      |
|            | TCLK        | C1                     | 22           | 18           | 13           | I                       | Test clock input                                |
|            | TDI         | C1                     | 22           | 18           | 13           | I                       | Test data input                                 |
|            | TDO         | B1                     | 21           | 17           | 12           | O                       | Test data output port                           |
|            | TEST        | H2                     | 37           | 30           | 22           | I                       | Test mode pin – select digital I/O on JTAG pins |
|            | TMS         | C2                     | 23           | 19           | 14           | I                       | Test mode select                                |

**Table 7-2. Signal Descriptions (continued)**

| FUNCTION | SIGNAL NAME | PIN NO. <sup>(1)</sup> |    |    |     | PIN TYPE <sup>(2)</sup> | DESCRIPTION                                                             |
|----------|-------------|------------------------|----|----|-----|-------------------------|-------------------------------------------------------------------------|
|          |             | ZVW                    | PN | PM | RGZ |                         |                                                                         |
| GPIO     | P1.0        | A10                    | 1  | 1  | 1   | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|          | P1.1        | A9                     | 2  | 2  | 2   | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|          | P1.2        | B9                     | 3  | 3  | 3   | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|          | P1.3        | A4                     | 16 | 12 | 9   | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|          | P1.4        | B3                     | 17 | 13 | 10  | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|          | P1.5        | B4                     | 18 | 14 | 11  | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|          | P1.6        | L6                     | 51 | 39 | 31  | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|          | P1.7        | K6                     | 52 | 40 | 32  | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
| GPIO     | P2.0        | L2                     | 41 | 32 | 24  | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|          | P2.1        | L3                     | 42 | 33 | 25  | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|          | P2.2        | K3                     | 43 | 34 | 26  | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|          | P2.3        | J11                    | 63 | 51 | 39  | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|          | P2.4        | K11                    | 64 | 52 | 40  | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|          | P2.5        | G4                     | 35 | 28 | 20  | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|          | P2.6        | H1                     | 36 | 29 | 21  | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|          | P2.7        | F11                    | 62 | 50 | 38  | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
| GPIO     | P3.0        | A8                     | 4  | 4  | 4   | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|          | P3.1        | B8                     | 5  | 5  | 5   | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|          | P3.2        | B7                     | 6  | 6  | 6   | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|          | P3.3        | A7                     | 7  | 7  | 7   | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|          | P3.4        | K5                     | 47 | 35 | 27  | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|          | P3.5        | L5                     | 48 | 36 | 28  | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|          | P3.6        | H5                     | 49 | 37 | 29  | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|          | P3.7        | H6                     | 50 | 38 | 30  | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |

**Table 7-2. Signal Descriptions (continued)**

| FUNCTION | SIGNAL NAME | PIN NO. <sup>(1)</sup> |    |    |     | PIN TYPE <sup>(2)</sup> | DESCRIPTION                                                             |
|----------|-------------|------------------------|----|----|-----|-------------------------|-------------------------------------------------------------------------|
|          |             | ZVW                    | PN | PM | RGZ |                         |                                                                         |
| GPIO     | P4.0        | F1                     | 31 | 24 | 16  | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|          | P4.1        | F4                     | 32 | 25 | 17  | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|          | P4.2        | G1                     | 33 | 26 | 18  | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|          | P4.3        | G2                     | 34 | 27 | 19  | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|          | P4.4        | H7                     | 57 | 45 | 33  | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|          | P4.5        | H8                     | 58 | 46 | 34  | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|          | P4.6        | K9                     | 59 | 47 | 35  | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|          | P4.7        | D6                     | 12 | 8  | 8   | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
| GPIO     | P5.0        | L7                     | 53 | 41 | –   | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|          | P5.1        | K7                     | 54 | 42 | –   | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|          | P5.2        | K8                     | 55 | 43 | –   | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|          | P5.3        | L8                     | 56 | 44 | –   | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|          | P5.4        | J10                    | 65 | 53 | –   | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|          | P5.5        | H10                    | 66 | 54 | –   | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|          | P5.6        | G10                    | 67 | 55 | –   | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|          | P5.7        | G8                     | 68 | 56 | –   | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
| GPIO     | P6.0        | D8                     | 8  | –  | –   | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|          | P6.1        | D7                     | 9  | –  | –   | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|          | P6.2        | A6                     | 10 | –  | –   | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|          | P6.3        | B6                     | 11 | –  | –   | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|          | P6.4        | F8                     | 69 | –  | –   | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|          | P6.5        | F10                    | 70 | –  | –   | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|          | P6.6        | E8                     | 71 | –  | –   | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|          | P6.7        | C10                    | 72 | –  | –   | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |

**Table 7-2. Signal Descriptions (continued)**

| FUNCTION         | SIGNAL NAME | PIN NO. <sup>(1)</sup> |    |    |     | PIN TYPE <sup>(2)</sup> | DESCRIPTION                                                             |
|------------------|-------------|------------------------|----|----|-----|-------------------------|-------------------------------------------------------------------------|
|                  |             | ZVW                    | PN | PM | RGZ |                         |                                                                         |
| GPIO             | P7.0        | A5                     | 13 | 9  | –   | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|                  | P7.1        | B5                     | 14 | 10 | –   | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|                  | P7.2        | D1                     | 25 | 21 | –   | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|                  | P7.3        | D4                     | 26 | 22 | –   | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|                  | P7.4        | E1                     | 27 | 23 | –   | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|                  | P7.5        | E2                     | 28 | –  | –   | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|                  | P7.6        | E4                     | 29 | –  | –   | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|                  | P7.7        | F2                     | 30 | –  | –   | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
| GPIO             | P8.0        | D5                     | 15 | 11 | –   | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|                  | P8.1        | L4                     | 44 | –  | –   | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|                  | P8.2        | K4                     | 45 | –  | –   | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
|                  | P8.3        | H4                     | 46 | –  | –   | I/O                     | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
| GPIO             | PJ.0        | B1                     | 21 | 17 | 12  | I/O                     | General-purpose digital I/O                                             |
|                  | PJ.1        | C1                     | 22 | 18 | 13  | I/O                     | General-purpose digital I/O                                             |
|                  | PJ.2        | C2                     | 23 | 19 | 14  | I/O                     | General-purpose digital I/O                                             |
|                  | PJ.3        | D2                     | 24 | 20 | 15  | I/O                     | General-purpose digital I/O                                             |
|                  | PJ.4        | E11                    | 77 | 61 | 45  | I/O                     | General-purpose digital I/O                                             |
|                  | PJ.5        | D11                    | 78 | 62 | 46  | I/O                     | General-purpose digital I/O                                             |
|                  | PJ.6        | H11                    | 74 | 58 | 42  | I/O                     | General-purpose digital I/O                                             |
|                  | PJ.7        | G11                    | 75 | 59 | 43  | I/O                     | General-purpose digital I/O                                             |
| I <sup>2</sup> C | UCB0SCL     | K6                     | 52 | 40 | 32  | I/O                     | I <sup>2</sup> C clock – eUSCI_B0 I <sup>2</sup> C mode                 |
|                  | UCB0SDA     | L6                     | 51 | 39 | 31  | I/O                     | I <sup>2</sup> C data – eUSCI_B0 I <sup>2</sup> C mode                  |
|                  | UCB1SCL     | K7                     | 54 | 42 | –   | I/O                     | I <sup>2</sup> C clock – eUSCI_B1 I <sup>2</sup> C mode                 |
|                  | UCB1SDA     | L7                     | 53 | 41 | –   | I/O                     | I <sup>2</sup> C data – eUSCI_B1 I <sup>2</sup> C mode                  |
|                  | UCB2SCL     | B5                     | 14 | 10 | –   | I/O                     | I <sup>2</sup> C clock – eUSCI_B2 I <sup>2</sup> C mode                 |
|                  | UCB2SDA     | A5                     | 13 | 9  | –   | I/O                     | I <sup>2</sup> C data – eUSCI_B2 I <sup>2</sup> C mode                  |
|                  | UCB3SCL     | F10                    | 70 | –  | –   | I/O                     | I <sup>2</sup> C clock – eUSCI_B3 I <sup>2</sup> C mode                 |
|                  | UCB3SDA     | F8                     | 69 | –  | –   | I/O                     | I <sup>2</sup> C data – eUSCI_B3 I <sup>2</sup> C mode                  |

**Table 7-2. Signal Descriptions (continued)**

| FUNCTION | SIGNAL NAME | PIN NO. <sup>(1)</sup>       |    |    |     | PIN TYPE <sup>(2)</sup> | DESCRIPTION                                                                    |
|----------|-------------|------------------------------|----|----|-----|-------------------------|--------------------------------------------------------------------------------|
|          |             | ZVW                          | PN | PM | RGZ |                         |                                                                                |
| Power    | AGND        | B10<br>A11                   | –  | –  | –   | P                       | Analog ground                                                                  |
|          | AVCC1       | B11                          | 80 | 64 | 48  | P                       | Analog power supply                                                            |
|          | AVSS1       | C11                          | 79 | 63 | 47  | P                       | Analog ground supply                                                           |
|          | AVSS2       | D10                          | 76 | 60 | 44  | P                       | Analog ground supply                                                           |
|          | AVSS3       | E10                          | 73 | 57 | 41  | P                       | Analog ground supply                                                           |
|          | DGND        | A1<br>K2<br>K10<br>L1<br>L11 | –  | –  | –   | P                       | Digital ground                                                                 |
|          | DVCC1       | L10                          | 61 | 49 | 37  | P                       | Digital power supply                                                           |
|          | DVCC2       | A3                           | 20 | 16 | –   | P                       | Digital power supply                                                           |
|          | DVCC3       | K1                           | 40 | –  | –   | P                       | Digital power supply                                                           |
|          | DVSS1       | L9                           | 60 | 48 | 36  | P                       | Digital ground supply                                                          |
|          | DVSS2       | A2                           | 19 | 15 | –   | P                       | Digital ground supply                                                          |
|          | DVSS3       | J1                           | 39 | –  | –   | P                       | Digital ground supply                                                          |
|          | QFN Pad     | –                            | –  | –  | Pad | P                       | QFN package exposed thermal pad. TI recommends connection to V <sub>SS</sub> . |
| RTC      | RTCCLK      | A10                          | 1  | 1  | 1   | O                       | RTC clock calibration output (not available on MSP430FR5x5x devices)           |

Table 7-2. Signal Descriptions (continued)

| FUNCTION | SIGNAL NAME | PIN NO. <sup>(1)</sup> |    |    |     | PIN TYPE <sup>(2)</sup> | DESCRIPTION                                                                                    |
|----------|-------------|------------------------|----|----|-----|-------------------------|------------------------------------------------------------------------------------------------|
|          |             | ZVW                    | PN | PM | RGZ |                         |                                                                                                |
| SPI      | UCA0CLK     | B4                     | 18 | 14 | 11  | I/O                     | Clock signal input – eUSCI_A0 SPI slave mode<br>Clock signal output – eUSCI_A0 SPI master mode |
|          | UCA0SIMO    | L2                     | 41 | 32 | 24  | I/O                     | Slave in/master out – eUSCI_A0 SPI mode                                                        |
|          | UCA0SOMI    | L3                     | 42 | 33 | 25  | I/O                     | Slave out/master in – eUSCI_A0 SPI mode                                                        |
|          | UCA0STE     | B3                     | 17 | 13 | 10  | I/O                     | Slave transmit enable – eUSCI_A0 SPI mode                                                      |
|          | UCA1CLK     | K11                    | 64 | 52 | 40  | I/O                     | Clock signal input – eUSCI_A1 SPI slave mode<br>Clock signal output – eUSCI_A1 SPI master mode |
|          | UCA1SIMO    | G4                     | 35 | 28 | 20  | I/O                     | Slave in/master out – eUSCI_A1 SPI mode                                                        |
|          | UCA1SOMI    | H1                     | 36 | 29 | 21  | I/O                     | Slave out/master in – eUSCI_A1 SPI mode                                                        |
|          | UCA1STE     | J11                    | 63 | 51 | 39  | I/O                     | Slave transmit enable – eUSCI_A1 SPI mode                                                      |
|          | UCA2CLK     | G10                    | 67 | 55 | –   | I/O                     | Clock signal input – eUSCI_A2 SPI slave mode<br>Clock signal output – eUSCI_A2 SPI master mode |
|          | UCA2SIMO    | J10                    | 65 | 53 | –   | I/O                     | Slave in/master out – eUSCI_A2 SPI mode                                                        |
|          | UCA2SOMI    | H10                    | 66 | 54 | –   | I/O                     | Slave out/master in – eUSCI_A2 SPI mode                                                        |
|          | UCA2STE     | G8                     | 68 | 56 | –   | I/O                     | Slave transmit enable – eUSCI_A2 SPI mode                                                      |
|          | UCA3CLK     | A6                     | 10 | –  | –   | I/O                     | Clock signal input – eUSCI_A3 SPI slave mode<br>Clock signal output – eUSCI_A3 SPI master mode |
|          | UCA3SIMO    | D8                     | 8  | –  | –   | I/O                     | Slave in/master out – eUSCI_A3 SPI mode                                                        |
|          | UCA3SOMI    | D7                     | 9  | –  | –   | I/O                     | Slave out/master in – eUSCI_A3 SPI mode                                                        |
|          | UCA3STE     | B6                     | 11 | –  | –   | I/O                     | Slave transmit enable – eUSCI_A3 SPI mode                                                      |
|          | UCB0CLK     | K3                     | 43 | 34 | 26  | I/O                     | Clock signal input – eUSCI_B0 SPI slave mode<br>Clock signal output – eUSCI_B0 SPI master mode |
|          | UCB0SIMO    | L6                     | 51 | 39 | 31  | I/O                     | Slave in/master out – eUSCI_B0 SPI mode                                                        |
|          | UCB0SOMI    | K6                     | 52 | 40 | 32  | I/O                     | Slave out/master in – eUSCI_B0 SPI mode                                                        |
|          | UCB0STE     | A4                     | 16 | 12 | 9   | I/O                     | Slave transmit enable – eUSCI_B0 SPI mode                                                      |
|          | UCB1CLK     | K8                     | 55 | 43 | –   | I/O                     | Clock signal input – eUSCI_B1 SPI slave mode<br>Clock signal output – eUSCI_B1 SPI master mode |
|          | UCB1SIMO    | L7                     | 53 | 41 | –   | I/O                     | Slave in/master out – eUSCI_B1 SPI mode                                                        |
|          | UCB1SOMI    | K7                     | 54 | 42 | –   | I/O                     | Slave out/master in – eUSCI_B1 SPI mode                                                        |
|          | UCB1STE     | L8                     | 56 | 44 | –   | I/O                     | Slave transmit enable – eUSCI_B1 SPI mode                                                      |
|          | UCB2CLK     | D1                     | 25 | 21 | –   | I/O                     | Clock signal input – eUSCI_B2 SPI slave mode<br>Clock signal output – eUSCI_B2 SPI master mode |
|          | UCB2SIMO    | A5                     | 13 | 9  | –   | I/O                     | Slave in/master out – eUSCI_B2 SPI mode                                                        |
|          | UCB2SOMI    | B5                     | 14 | 10 | –   | I/O                     | Slave out/master in – eUSCI_B2 SPI mode                                                        |
|          | UCB2STE     | D4                     | 26 | 22 | –   | I/O                     | Slave transmit enable – eUSCI_B2 SPI mode                                                      |
|          | UCB3CLK     | E8                     | 71 | –  | –   | I/O                     | Clock signal input – eUSCI_B3 SPI slave mode<br>Clock signal output – eUSCI_B3 SPI master mode |
|          | UCB3SIMO    | F8                     | 69 | –  | –   | I/O                     | Slave in/master out – eUSCI_B3 SPI mode                                                        |
|          | UCB3SOMI    | F10                    | 70 | –  | –   | I/O                     | Slave out/master in – eUSCI_B3 SPI mode                                                        |
|          | UCB3STE     | C10                    | 72 | –  | –   | I/O                     | Slave transmit enable – eUSCI_B3 SPI mode                                                      |
| System   | NMI         | J2                     | 38 | 31 | 23  | I                       | Nonmaskable interrupt input                                                                    |
|          | RST         | J2                     | 38 | 31 | 23  | I                       | Reset input active low                                                                         |

**Table 7-2. Signal Descriptions (continued)**

| FUNCTION | SIGNAL NAME | PIN NO. <sup>(1)</sup> |          |          |     | PIN TYPE <sup>(2)</sup> | DESCRIPTION                                       |
|----------|-------------|------------------------|----------|----------|-----|-------------------------|---------------------------------------------------|
|          |             | ZVW                    | PN       | PM       | RGZ |                         |                                                   |
| Timer    | TA0.0       | L6                     | 51       | 39       | 31  | I/O                     | TA0 CCR0 capture: CCI0A input, compare: Out0      |
|          | TA0.0       | J11                    | 63       | 51       | 39  | I/O                     | TA0 CCR0 capture: CCI0B input, compare: Out0      |
|          | TA0.1       | A10                    | 1        | 1        | 1   | I/O                     | TA0 CCR1 capture: CCI1A input, compare: Out1      |
|          | TA0.2       | A9                     | 2        | 2        | 2   | I/O                     | TA0 CCR2 capture: CCI2A input, compare: Out2      |
|          | TA0CLK      | B9                     | 3        | 3        | 3   | I                       | TA0 input clock                                   |
|          | TA1.0       | K6                     | 52       | 40       | 32  | I/O                     | TA1 CCR0 capture: CCI0A input, compare: Out0      |
|          | TA1.0       | K11                    | 64       | 52       | 40  | I/O                     | TA1 CCR0 capture: CCI0B input, compare: Out0      |
|          | TA1.1       | B9                     | 3        | 3        | 3   | I/O                     | TA1 CCR1 capture: CCI1A input, compare: Out1      |
|          | TA1.2       | A4                     | 16       | 12       | 9   | I/O                     | TA1 CCR2 capture: CCI2A input, compare: Out2      |
|          | TA1CLK      | A9                     | 2        | 2        | 2   | I                       | TA1 input clock                                   |
|          | TA4.0       | E1                     | 27       | 23       | –   | I/O                     | TA4 CCR0 capture: CCI0B input, compare: Out0      |
|          | TA4.0       | G10                    | 67       | 55       | –   | I/O                     | TA4 CCR0 capture: CCI0A input, compare: Out0      |
|          | TA4.1       | D4                     | 26       | 22       | –   | I/O                     | TA4CCR1 capture: CCI1B input, compare: Out1       |
|          | TA4.1       | G8                     | 68       | 56       | –   | I/O                     | TA4 CCR1 capture: CCI1A input, compare: Out1      |
|          | TA4CLK      | K8                     | 55       | 43       | –   | I                       | TA4 input clock                                   |
|          | TB0.0       | G4                     | 35       | 28       | 20  | I/O                     | TB0 CCR0 capture: CCI0B input, compare: Out0      |
|          | TB0.0       | L3                     | 42       | 33       | 25  | I/O                     | TB0 CCR0 capture: CCI0A input, compare: Out0      |
|          | TB0.1       | B3                     | 17       | 13       | 10  | I/O                     | TB0 CCR1 capture: CCI1A input, compare: Out1      |
|          | TB0.1       | H1                     | 36       | 29       | 21  | O                       | TB0 CCR1 compare: Out1                            |
|          | TB0.2       | B4                     | 18       | 14       | 11  | I/O                     | TB0 CCR2 capture: CCI2A input, compare: Out2      |
|          | TB0.2       | K3                     | 43       | 34       | 26  | O                       | TB0 CCR2 compare: Out2                            |
|          | TB0.3       | K5                     | 47       | 35       | 27  | I/O                     | TB0 CCR3 capture: CCI3A input, compare: Out3      |
|          | TB0.3       | L6                     | 51       | 39       | 31  | I/O                     | TB0 CCR3 capture: CCI3B input, compare: Out3      |
|          | TB0.4       | L5                     | 48       | 36       | 28  | I/O                     | TB0 CCR4 capture: CCI4A input, compare: Out4      |
|          | TB0.4       | K6                     | 52       | 40       | 32  | I/O                     | TB0 CCR4 capture: CCI4B input, compare: Out4      |
|          | TB0.5       | H5                     | 49       | 37       | 29  | I/O                     | TB0 CCR5 capture: CCI5A input, compare: Out5      |
|          | TB0.5       | H7                     | 57       | 45       | 33  | I/O                     | TB0CCR5 capture: CCI5B input, compare: Out5       |
|          | TB0.6       | L2                     | 41       | 32       | 24  | I/O                     | TB0 CCR6 capture: CCI6B input, compare: Out6      |
|          | TB0.6       | H6                     | 50       | 38       | 30  | I/O                     | TB0 CCR6 capture: CCI6A input, compare: Out6      |
|          | TB0CLK      | L2                     | 41       | 32       | 24  | I                       | TB0 clock input                                   |
|          | TB0OUTH     | B1<br>J10              | 21<br>65 | 17<br>53 | 12  | I                       | Switch all PWM outputs high impedance input – TB0 |
| UART     | UCA0RXD     | L3                     | 42       | 33       | 25  | I                       | Receive data – eUSCI_A0 UART mode                 |
|          | UCA0TXD     | L2                     | 41       | 32       | 24  | O                       | Transmit data – eUSCI_A0 UART mode                |
|          | UCA1RXD     | H1                     | 36       | 29       | 21  | I                       | Receive data – eUSCI_A1 UART mode                 |
|          | UCA1TXD     | G4                     | 35       | 28       | 20  | O                       | Transmit data – eUSCI_A1 UART mode                |
|          | UCA2RXD     | H10                    | 66       | 54       | –   | I                       | Receive data – eUSCI_A2 UART mode                 |
|          | UCA2TXD     | J10                    | 65       | 53       | –   | O                       | Transmit data – eUSCI_A2 UART mode                |
|          | UCA3RXD     | D7                     | 9        | –        | –   | I                       | Receive data – eUSCI_A3 UART mode                 |
|          | UCA3TXD     | D8                     | 8        | –        | –   | O                       | Transmit data – eUSCI_A3 UART mode                |

(1) N/A = not available

(2) I = input, O = output, P = power

## 7.4 Pin Multiplexing

Pin multiplexing for these devices is controlled by both register settings and operating modes (for example, if the device is in test mode). For details of the settings for each pin and schematics of the multiplexed ports, see [Section 9.13](#).

## 7.5 Buffer Types

[Table 7-3](#) describes the buffer types that are referenced in [Table 7-1](#).

**Table 7-3. Buffer Type**

| BUFFER TYPE (STANDARD)               | NOMINAL VOLTAGE | HYSTERESIS         | PU OR PD <sup>(1)</sup> | NOMINAL PU OR PD STRENGTH ( $\mu$ A) <sup>(1)</sup> | OUTPUT DRIVE STRENGTH (mA) <sup>(1)</sup> | COMMENTS                                                    |
|--------------------------------------|-----------------|--------------------|-------------------------|-----------------------------------------------------|-------------------------------------------|-------------------------------------------------------------|
| Analog <sup>(2)</sup>                | 3.0 V           | No                 | N/A                     | N/A                                                 | N/A                                       | See analog modules in <a href="#">Section 8</a> for details |
| LVC MOS                              | 3.0 V           | Yes <sup>(3)</sup> | Programmable            | See <a href="#">Section 8.12.5</a>                  | See <a href="#">Section 8.12.5.3</a>      |                                                             |
| Power (DVCC) <sup>(4)</sup>          | 3.0 V           | No                 | N/A                     | N/A                                                 | N/A                                       | SVS enables hysteresis on DVCC                              |
| Power (AVCC) <sup>(4)</sup>          | 3.0 V           | No                 | N/A                     | N/A                                                 | N/A                                       |                                                             |
| Power (DVSS and AVSS) <sup>(4)</sup> | 0 V             | No                 | N/A                     | N/A                                                 | N/A                                       |                                                             |

(1) N/A = not applicable

(2) This is a switch, not a buffer.

(3) Only for input pins

(4) This is supply input, not a buffer.

## 7.6 Connection of Unused Pins

[Table 7-4](#) lists the correct termination of all unused pins.

**Table 7-4. Connection of Unused Pins**

| PIN <sup>(1)</sup>                           | POTENTIAL                           | COMMENT                                                                                                                                                                                                   |
|----------------------------------------------|-------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| AVCC                                         | DV <sub>CC</sub>                    |                                                                                                                                                                                                           |
| AVSS                                         | DV <sub>SS</sub>                    |                                                                                                                                                                                                           |
| Px.0 to Px.7                                 | Open                                | Switched to port function, output direction (PxDIR.n = 1)                                                                                                                                                 |
| RST/NMI                                      | DV <sub>CC</sub> or V <sub>CC</sub> | 47-k $\Omega$ pullup or internal pullup selected with 10-nF (2.2 nF <sup>(2)</sup> ) pulldown                                                                                                             |
| PJ.0/TDO<br>PJ.1/TDI<br>PJ.2/TMS<br>PJ.3/TCK | Open                                | The JTAG pins are shared with general-purpose I/O function (PJ.x). If not being used, these should be switched to port function, output direction. When used as JTAG pins, these pins should remain open. |
| TEST                                         | Open                                | This pin always has an internal pulldown enabled.                                                                                                                                                         |

(1) For any unused pin with a secondary function that is shared with general-purpose I/O, follow the guidelines for the Px.0 to Px.7 pins.

(2) The pulldown capacitor should not exceed 2.2 nF when using devices with Spy-Bi-Wire interface in Spy-Bi-Wire mode or in 4-wire JTAG mode with TI tools like FET interfaces or GANG programmers.

## 8 Specifications

### 8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                                                              | MIN  | MAX                                    | UNIT |
|--------------------------------------------------------------|------|----------------------------------------|------|
| Voltage applied at DVCC and AVCC pins to V <sub>SS</sub>     | −0.3 | 4.1                                    | V    |
| Voltage difference between DVCC and AVCC pins <sup>(1)</sup> |      | ±0.3                                   | V    |
| Voltage applied to any pin <sup>(2)</sup>                    | −0.3 | V <sub>CC</sub> + 0.3 V<br>(4.1 V Max) | V    |
| Diode current at any device pin                              |      | ±2                                     | mA   |
| Storage temperature, T <sub>stg</sub> <sup>(3)</sup>         | −40  | 125                                    | °C   |

- (1) Voltage differences between DVCC and AVCC exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and FRAM.
- (2) All voltages referenced to V<sub>SS</sub>.
- (3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

### 8.2 ESD Ratings

|                                            |                                                                                | VALUE | UNIT |
|--------------------------------------------|--------------------------------------------------------------------------------|-------|------|
| V <sub>(ESD)</sub> Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±1000 | V    |
|                                            | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±250  |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

### 8.3 Recommended Operating Conditions

TYP data are based on  $V_{CC} = 3.0\text{ V}$  and  $T_A = 25^\circ\text{C}$ , unless otherwise noted

|                     |                                                                               |                                                    | MIN                | NOM | MAX               | UNIT |
|---------------------|-------------------------------------------------------------------------------|----------------------------------------------------|--------------------|-----|-------------------|------|
| V <sub>CC</sub>     | Supply voltage range applied at all DVCC and AVCC pins <sup>(1) (2) (3)</sup> |                                                    | 1.8 <sup>(6)</sup> |     | 3.6               | V    |
| V <sub>SS</sub>     | Supply voltage applied at all DVSS and AVSS pins.                             |                                                    |                    | 0   |                   | V    |
| T <sub>A</sub>      | Operating free-air temperature                                                |                                                    | −40                |     | 85                | °C   |
| T <sub>J</sub>      | Operating junction temperature                                                |                                                    | −40                |     | 85                | °C   |
| C <sub>DVCC</sub>   | Capacitor value at DVCC <sup>(4)</sup>                                        |                                                    | 1–20%              |     |                   | μF   |
| f <sub>SYSTEM</sub> | Processor frequency (maximum MCLK frequency) <sup>(5)</sup>                   | No FRAM wait states (NWAITSx = 0)                  | 0                  |     | 8 <sup>(8)</sup>  | MHz  |
|                     |                                                                               | With FRAM wait states (NWAITSx = 1) <sup>(7)</sup> | 0                  |     | 16 <sup>(9)</sup> |      |
| f <sub>ACLK</sub>   | Maximum ACLK frequency                                                        |                                                    |                    |     | 50                | kHz  |
| f <sub>SMCLK</sub>  | Maximum SMCLK frequency                                                       |                                                    |                    |     | 16 <sup>(9)</sup> | MHz  |

- (1) TI recommends powering AVCC and DVCC pins from the same source. At a minimum, during power up, power down, and device operation, the voltage difference between AVCC and DVCC must not exceed the limits specified under *Absolute Maximum Ratings*. Exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and FRAM.
- (2) Fast supply voltage changes can trigger a BOR reset even within the recommended supply voltage range. To avoid unwanted BOR resets, the supply voltage must change by less than 0.05 V per microsecond ( $\pm 0.05\text{ V}/\mu\text{s}$ ). Following the data sheet recommendation for capacitor  $C_{DVCC}$  should limit the slopes accordingly.
- (3) Modules may have a different supply voltage range specification. See the specification of the respective module in this data sheet.
- (4) For each supply pin pair (DVCC and DVSS, AVCC and AVSS), place a low-ESR ceramic capacitor of 100 nF (minimum) as close as possible (within a few millimeters) to the respective pin pairs.
- (5) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.
- (6) The minimum supply voltage is defined by the supervisor SVS levels. See the PMM SVS threshold parameters for the exact values.
- (7) Wait states only occur on actual FRAM accesses; that is, on FRAM cache misses. RAM and peripheral accesses are always executed without wait states.
- (8) DCO settings and HF crystals with a typical value less than or equal to the specified MAX value are permitted.
- (9) DCO settings and HF crystals with a typical value less than or equal to the specified MAX value are permitted. If a clock sources with a higher typical value is used, the clock must be divided in the clock system.

## 8.4 Active Mode Supply Current Into $V_{CC}$ Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)<sup>(1) (2)</sup> (see [Figure 8-1](#))

| PARAMETER                                                    | EXECUTION MEMORY             | V <sub>CC</sub> | FREQUENCY (f <sub>MCLK</sub> = f <sub>SMCLK</sub> ) |     |                                                     |     |                                                     |      |                                                     |      |                                                     |      | UNIT |
|--------------------------------------------------------------|------------------------------|-----------------|-----------------------------------------------------|-----|-----------------------------------------------------|-----|-----------------------------------------------------|------|-----------------------------------------------------|------|-----------------------------------------------------|------|------|
|                                                              |                              |                 | 1 MHz<br>0 WAIT STATES<br>(NWAITS <sub>x</sub> = 0) |     | 4 MHz<br>0 WAIT STATES<br>(NWAITS <sub>x</sub> = 0) |     | 8 MHz<br>0 WAIT STATES<br>(NWAITS <sub>x</sub> = 0) |      | 12 MHz<br>1 WAIT STATE<br>(NWAITS <sub>x</sub> = 1) |      | 16 MHz<br>1 WAIT STATE<br>(NWAITS <sub>x</sub> = 1) |      |      |
|                                                              |                              |                 | TYP                                                 | MAX | TYP                                                 | MAX | TYP                                                 | MAX  | TYP                                                 | MAX  | TYP                                                 | MAX  |      |
| I <sub>AM, FRAM_UNI</sub><br>(Unified memory) <sup>(3)</sup> | FRAM                         | 3.0 V           | 225                                                 |     | 665                                                 |     | 1275                                                |      | 1550                                                |      | 1970                                                |      | μA   |
| I <sub>AM, FRAM</sub> (0%) <sup>(4) (5)</sup>                | FRAM<br>0% cache hit ratio   | 3.0 V           | 420                                                 |     | 1455                                                |     | 2850                                                |      | 2330                                                |      | 3000                                                |      | μA   |
| I <sub>AM, FRAM</sub> (50%) <sup>(4) (5)</sup>               | FRAM<br>50% cache hit ratio  | 3.0 V           | 275                                                 |     | 855                                                 |     | 1650                                                |      | 1770                                                |      | 2265                                                |      | μA   |
| I <sub>AM, FRAM</sub> (66%) <sup>(4) (5)</sup>               | FRAM<br>66% cache hit ratio  | 3.0 V           | 220                                                 |     | 650                                                 |     | 1240                                                |      | 1490                                                |      | 1880                                                |      | μA   |
| I <sub>AM, FRAM</sub> (75%) <sup>(4) (5)</sup>               | FRAM<br>75% cache hit ratio  | 3.0 V           | 192                                                 | 261 | 535                                                 |     | 1015                                                | 1170 | 1290                                                | 1490 | 1620                                                | 1870 | μA   |
| I <sub>AM, FRAM</sub> (100%) <sup>(4) (5)</sup>              | FRAM<br>100% cache hit ratio | 3.0 V           | 125                                                 |     | 255                                                 |     | 450                                                 |      | 670                                                 |      | 790                                                 |      | μA   |
| I <sub>AM, RAM</sub> <sup>(6) (5)</sup>                      | RAM                          | 3.0 V           | 140                                                 |     | 325                                                 |     | 590                                                 |      | 880                                                 |      | 1070                                                |      | μA   |
| I <sub>AM, RAM</sub> only <sup>(7) (5)</sup>                 | RAM                          | 3.0 V           | 90                                                  | 182 | 280                                                 |     | 540                                                 |      | 830                                                 |      | 1020                                                | 1313 | μA   |

(1) All inputs are tied to 0 V or to  $V_{CC}$ . Outputs do not source or sink any current.

(2) Characterized with program executing typical data processing.

$f_{ACLK} = 32768$  Hz,  $f_{MCLK} = f_{SMCLK} = f_{DCO}$  at specified frequency, except for 12 MHz. For 12 MHz,  $f_{DCO} = 24$  MHz and  $f_{MCLK} = f_{SMCLK} = f_{DCO} / 2$ .

At MCLK frequencies above 8 MHz, the FRAM requires wait states. When wait states are required, the effective MCLK frequency ( $f_{MCLK,eff}$ ) decreases. The effective MCLK frequency also depends on the cache hit ratio. SMCLK is not affected by the number of wait states or the cache hit ratio.

The following equation can be used to compute  $f_{MCLK,eff}$ :

$$f_{MCLK,eff} = f_{MCLK} / [\text{wait states} \times (1 - \text{cache hit ratio}) + 1]$$

For example, with 1 wait state and 75% cache hit ratio  $f_{MCLK,eff} = f_{MCLK} / [1 \times (1 - 0.75) + 1] = f_{MCLK} / 1.25$ .

(3) Represents typical program execution. Program and data reside entirely in FRAM. All execution is from FRAM.

(4) Program resides in FRAM. Data resides in SRAM. Average current dissipation varies with cache hit-to-miss ratio as specified. Cache hit ratio represents number cache accesses divided by the total number of FRAM accesses. For example, a 75% ratio implies three of every four accesses is from cache, and the remaining are FRAM accesses.

(5) See [Figure 8-1](#) for typical curves. The characteristic equation shown in the graph is computed using the least squares method for best linear fit using the typical data shown in [Section 8.4](#).

(6) Program and data reside entirely in RAM. All execution is from RAM.

(7) Program and data reside entirely in RAM. All execution is from RAM. FRAM is off.

## 8.5 Typical Characteristics, Active Mode Supply Currents

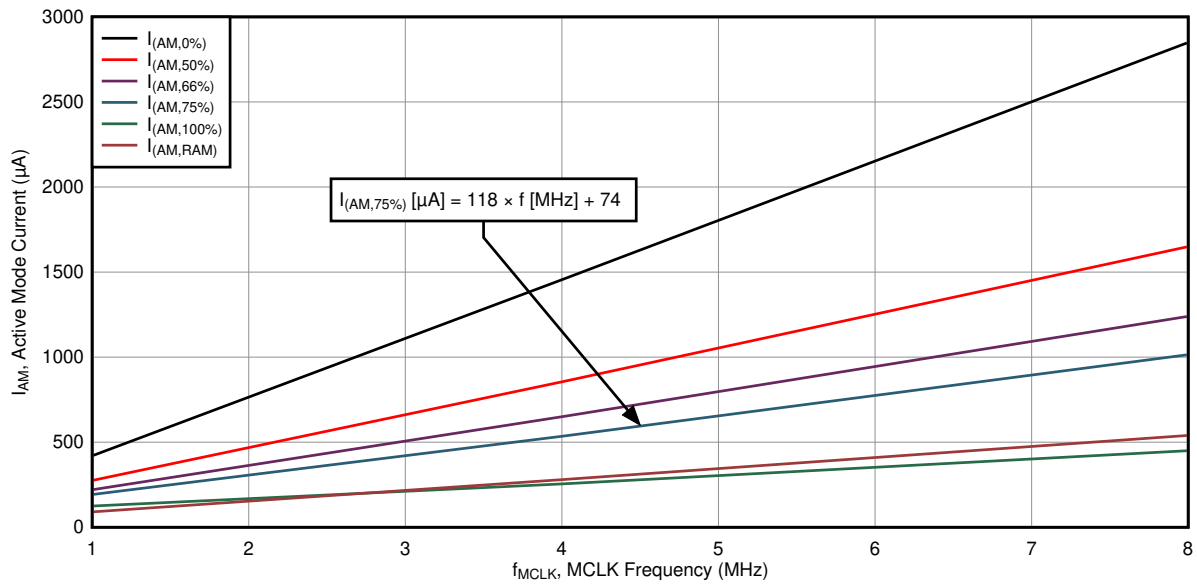


Figure 8-1. Typical Active Mode Supply Currents, No Wait States

## 8.6 Low-Power Mode (LPM0, LPM1) Supply Currents Into $V_{CC}$ Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)<sup>(1)</sup> <sup>(2)</sup>

| PARAMETER         | V <sub>CC</sub> | FREQUENCY (f <sub>SMCLK</sub> ) |     |       |     |       |     |        |     |        |     | UNIT |
|-------------------|-----------------|---------------------------------|-----|-------|-----|-------|-----|--------|-----|--------|-----|------|
|                   |                 | 1 MHz                           |     | 4 MHz |     | 8 MHz |     | 12 MHz |     | 16 MHz |     |      |
|                   |                 | TYP                             | MAX | TYP   | MAX | TYP   | MAX | TYP    | MAX | TYP    | MAX |      |
| I <sub>LPM0</sub> | 2.2 V           | 75                              |     | 105   |     | 165   |     | 240    |     | 220    |     | μA   |
|                   | 3.0 V           | 85                              | 135 | 115   |     | 175   |     | 250    |     | 240    | 290 |      |
| I <sub>LPM1</sub> | 2.2 V           | 40                              |     | 65    |     | 130   |     | 215    |     | 195    |     | μA   |
|                   | 3.0 V           | 40                              | 67  | 65    |     | 130   |     | 215    |     | 195    | 222 |      |

(1) All inputs are tied to 0 V or to  $V_{CC}$ . Outputs do not source or sink any current.

(2) Current for watchdog timer clocked by SMCLK included.

$f_{ACLK} = 32768$  Hz,  $f_{MCLK} = 0$  MHz,  $f_{SMCLK} = f_{DCO}$  at specified frequency - except for 12 MHz: here  $f_{DCO} = 24$  MHz and  $f_{SMCLK} = f_{DCO} / 2$ .

## 8.7 Low-Power Mode (LPM2, LPM3, LPM4) Supply Currents (Into $V_{CC}$ ) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) <sup>(1)</sup> (see [Figure 8-2](#) and [Figure 8-3](#))

| PARAMETER                                                                                                                                    | $V_{CC}$ | –40°C |     | 25°C |     | 60°C |     | 85°C |     | UNIT    |
|----------------------------------------------------------------------------------------------------------------------------------------------|----------|-------|-----|------|-----|------|-----|------|-----|---------|
|                                                                                                                                              |          | TYP   | MAX | TYP  | MAX | TYP  | MAX | TYP  | MAX |         |
| $I_{LPM2,XT12}$ Low-power mode 2, 12-pF crystal <sup>(2)</sup><br>(3) (4)                                                                    | 2.2 V    | 0.8   |     | 1.3  |     | 4.1  |     | 10.8 |     | $\mu A$ |
|                                                                                                                                              | 3.0 V    | 0.8   |     | 1.3  |     | 4.1  |     | 10.8 |     |         |
| $I_{LPM2,XT3.7}$ Low-power mode 2, 3.7-pF crystal <sup>(2)</sup><br>(5) (4)                                                                  | 2.2 V    | 0.6   |     | 1.2  |     | 4.0  |     | 10.7 |     | $\mu A$ |
|                                                                                                                                              | 3.0 V    | 0.6   |     | 1.2  |     | 4.0  |     | 10.7 |     |         |
| $I_{LPM2,VLO}$ Low-power mode 2, VLO, includes SVS <sup>(6)</sup>                                                                            | 2.2 V    | 0.5   |     | 1.0  |     | 3.8  |     | 10.5 |     | $\mu A$ |
|                                                                                                                                              | 3.0 V    | 0.5   |     | 1.0  |     | 3.8  |     | 10.5 |     |         |
| $I_{LPM3,XT12}$ Low-power mode 3, 12-pF crystal, includes SVS <sup>(2)</sup> (3) (7)                                                         | 2.2 V    | 0.8   |     | 1.0  |     | 2.2  |     | 4.5  |     | $\mu A$ |
|                                                                                                                                              | 3.0 V    | 0.8   |     | 1.0  |     | 2.2  |     | 4.5  |     |         |
| $I_{LPM3,XT3.7}$ Low-power mode 3, 3.7-pF crystal, excludes SVS <sup>(2)</sup> (5) (8)<br>(also see <a href="#">Figure 8-2</a> )             | 2.2 V    | 0.5   |     | 0.7  |     | 2.1  |     | 4.4  |     | $\mu A$ |
|                                                                                                                                              | 3.0 V    | 0.5   |     | 0.7  |     | 2.1  |     | 4.4  |     |         |
| $I_{LPM3,VLO}$ Low-power mode 3, VLO, excludes SVS <sup>(9)</sup>                                                                            | 2.2 V    | 0.4   |     | 0.5  |     | 1.9  |     | 4.2  |     | $\mu A$ |
|                                                                                                                                              | 3.0 V    | 0.4   |     | 0.5  |     | 1.9  |     | 4.2  |     |         |
| $I_{LPM3,VLO, RAMoff}$ Low-power mode 3, VLO, excludes SVS, RAM powered down completely <sup>(9)</sup>                                       | 2.2 V    | 0.36  |     | 0.47 |     | 1.4  |     | 2.6  |     | $\mu A$ |
|                                                                                                                                              | 3.0 V    | 0.36  |     | 0.47 |     | 1.4  |     | 2.6  |     |         |
| $I_{LPM4,SVS}$ Low-power mode 4, includes SVS <sup>(10)</sup>                                                                                | 2.2 V    | 0.5   |     | 0.6  |     | 1.9  |     | 4.3  |     | $\mu A$ |
|                                                                                                                                              | 3.0 V    | 0.5   |     | 0.6  |     | 1.9  |     | 4.3  |     |         |
| $I_{LPM4}$ Low-power mode 4, excludes SVS <sup>(11)</sup>                                                                                    | 2.2 V    | 0.3   |     | 0.4  |     | 1.7  |     | 4.0  |     | $\mu A$ |
|                                                                                                                                              | 3.0 V    | 0.3   |     | 0.4  |     | 1.7  |     | 4.0  |     |         |
| $I_{LPM4,RAMoff}$ Low-power mode 4, excludes SVS, RAM powered down completely <sup>(11)</sup>                                                | 2.2 V    | 0.3   |     | 0.37 |     | 1.2  |     | 2.5  |     | $\mu A$ |
|                                                                                                                                              | 3.0 V    | 0.3   |     | 0.37 |     | 1.2  |     | 2.5  |     |         |
| $I_{IDLE,GroupA}$ Additional idle current if one or more modules from Group A (see <a href="#">Table 9-3</a> ) are activated in LPM3 or LPM4 | 3.0 V    |       |     | 0.02 |     |      |     | 0.3  |     | $\mu A$ |
| $I_{IDLE,GroupB}$ Additional idle current if one or more modules from Group B (see <a href="#">Table 9-3</a> ) are activated in LPM3 or LPM4 | 3.0 V    |       |     | 0.02 |     |      |     | 0.35 |     | $\mu A$ |
| $I_{IDLE,GroupC}$ Additional idle current if one or more modules from Group C (see <a href="#">Table 9-3</a> ) are activated in LPM3 or LPM4 | 3.0 V    |       |     | 0.02 |     |      |     | 0.38 |     | $\mu A$ |

(1) All inputs are tied to 0 V or to  $V_{CC}$ . Outputs do not source or sink any current.

(2) Not applicable for devices with HF crystal oscillator only.

(3) Characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF load.

(4) Low-power mode 2, crystal oscillator test conditions:  
Current for watchdog timer clocked by ACLK and RTC clocked by XT1 included. Current for brownout and SVS included.  
CPUOFF = 1, SCG0 = 0 SCG1 = 1, OSCOFF = 0 (LPM2),  
 $f_{XT1}$  = 32768 Hz,  $f_{ACLK}$  =  $f_{XT1}$ ,  $f_{MCLK}$  =  $f_{SMCLK}$  = 0 MHz

(5) Characterized with a Seiko SSP-T7-FL (SMD) crystal with a load capacitance of 3.7 pF. The internal and external load capacitance are chosen to closely match the required 3.7-pF load.

(6) Low-power mode 2, VLO test conditions:  
Current for watchdog timer clocked by ACLK included. RTC disabled (RTCHOLD = 1). Current for brownout and SVS included.  
CPUOFF = 1, SCG0 = 0 SCG1 = 1, OSCOFF = 0 (LPM2),  
 $f_{XT1}$  = 0 Hz,  $f_{ACLK}$  =  $f_{VLO}$ ,  $f_{MCLK}$  =  $f_{SMCLK}$  = 0 MHz

(7) Low-power mode 3, 12-pF crystal including SVS test conditions:  
Current for watchdog timer clocked by ACLK and RTC clocked by XT1 included. Current for brownout and SVS included (SVSHE = 1).  
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3),

$f_{XT1} = 32768 \text{ Hz}$ ,  $f_{ACLK} = f_{XT1}$ ,  $f_{MCLK} = f_{SMCLK} = 0 \text{ MHz}$

Activating additional peripherals increases the current consumption due to active supply current contribution and due to additional idle current. See the idle currents specified for the respective peripheral groups.

- (8) Low-power mode 3, 3.7-pF crystal excluding SVS test conditions:  
Current for watchdog timer clocked by ACLK and RTC clocked by XT1 included. Current for brownout included. SVS disabled (SVSHE = 0).  
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3),  
 $f_{XT1} = 32768 \text{ Hz}$ ,  $f_{ACLK} = f_{XT1}$ ,  $f_{MCLK} = f_{SMCLK} = 0 \text{ MHz}$   
Activating additional peripherals increases the current consumption due to active supply current contribution and due to additional idle current. See the idle currents specified for the respective peripheral groups.
- (9) Low-power mode 3, VLO excluding SVS test conditions:  
Current for watchdog timer clocked by ACLK included. RTC disabled (RTCHOLD = 1). RAM disabled (RCCTL0 = 5A55h). Current for brownout included. SVS disabled (SVSHE = 0).  
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3),  
 $f_{XT1} = 0 \text{ Hz}$ ,  $f_{ACLK} = f_{VLO}$ ,  $f_{MCLK} = f_{SMCLK} = 0 \text{ MHz}$   
Activating additional peripherals increases the current consumption due to active supply current contribution and due to additional idle current. See the idle currents specified for the respective peripheral groups.
- (10) Low-power mode 4 including SVS test conditions:  
Current for brownout and SVS included (SVSHE = 1).  
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPM4),  
 $f_{XT1} = 0 \text{ Hz}$ ,  $f_{ACLK} = 0 \text{ Hz}$ ,  $f_{MCLK} = f_{SMCLK} = 0 \text{ MHz}$   
Activating additional peripherals increases the current consumption due to active supply current contribution and due to additional idle current. See the idle currents specified for the respective peripheral groups.
- (11) Low-power mode 4 excluding SVS test conditions:  
Current for brownout included. SVS disabled (SVSHE = 0). RAM disabled (RCCTL0 = 5A55h).  
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPM4),  
 $f_{XT1} = 0 \text{ Hz}$ ,  $f_{ACLK} = 0 \text{ Hz}$ ,  $f_{MCLK} = f_{SMCLK} = 0 \text{ MHz}$   
Activating additional peripherals increases the current consumption due to active supply current contribution and due to additional idle current. See the idle currents specified for the respective peripheral groups.

## 8.8 Low-Power Mode (LPMx.5) Supply Currents (Into $V_{CC}$ ) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)<sup>(1)</sup>(see [Figure 8-4](#) and [Figure 8-5](#))

| PARAMETER                                                                                  | $V_{CC}$ | –40°C |     | 25°C  |     | 60°C  |     | 85°C |     | UNIT    |
|--------------------------------------------------------------------------------------------|----------|-------|-----|-------|-----|-------|-----|------|-----|---------|
|                                                                                            |          | TYP   | MAX | TYP   | MAX | TYP   | MAX | TYP  | MAX |         |
| $I_{LPM3.5,XT12}$ Low-power mode 3.5, 12-pF crystal including SVS <sup>(2) (3) (4)</sup>   | 2.2 V    | 0.45  |     | 0.5   |     | 0.55  |     | 0.75 |     | $\mu A$ |
|                                                                                            | 3.0 V    | 0.45  |     | 0.5   |     | 0.55  |     | 0.75 |     |         |
| $I_{LPM3.5,XT3.7}$ Low-power mode 3.5, 3.7-pF crystal excluding SVS <sup>(2) (5) (6)</sup> | 2.2 V    | 0.3   |     | 0.35  |     | 0.4   |     | 0.65 |     | $\mu A$ |
|                                                                                            | 3.0 V    | 0.3   |     | 0.35  |     | 0.4   |     | 0.65 |     |         |
| $I_{LPM4.5,SVS}$ Low-power mode 4.5, including SVS <sup>(7)</sup>                          | 2.2 V    | 0.23  |     | 0.25  |     | 0.28  |     | 0.4  |     | $\mu A$ |
|                                                                                            | 3.0 V    | 0.23  |     | 0.25  |     | 0.28  |     | 0.4  |     |         |
| $I_{LPM4.5}$ Low-power mode 4.5, excluding SVS <sup>(8)</sup>                              | 2.2 V    | 0.035 |     | 0.045 |     | 0.075 |     | 0.15 |     | $\mu A$ |
|                                                                                            | 3.0 V    | 0.035 |     | 0.045 |     | 0.075 |     | 0.15 |     |         |

- (1) All inputs are tied to 0 V or to VCC. Outputs do not source or sink any current
- (2) Not applicable for devices with HF crystal oscillator only.
- (3) Characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF load.
- (4) Low-power mode 3.5, 1-pF crystal including SVS test conditions:  
Current for RTC clocked by XT1 included. Current for brownout and SVS included (SVSHE = 1). Core regulator disabled.  
PMMREGOFF = 1; CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),  
 $f_{XT1} = 32768$  Hz,  $f_{ACLK} = f_{XT1}$ ,  $f_{MCLK} = f_{SMCLK} = 0$  MHz
- (5) Characterized with a Seiko SSP-T7-FL (SMD) crystal with a load capacitance of 3.7 pF. The internal and external load capacitance are chosen to closely match the required 3.7-pF load.
- (6) Low-power mode 3.5, 3.7-pF crystal excluding SVS test conditions:  
Current for RTC clocked by XT1 included. Current for brownout included. SVS disabled (SVSHE = 0). Core regulator disabled.  
PMMREGOFF = 1; CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),  
 $f_{XT1} = 32768$  Hz,  $f_{ACLK} = f_{XT1}$ ,  $f_{MCLK} = f_{SMCLK} = 0$  MHz
- (7) Low-power mode 4.5 including SVS test conditions:  
Current for brownout and SVS included (SVSHE = 1). Core regulator disabled.  
PMMREGOFF = 1; CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),  
 $f_{XT1} = 0$  Hz,  $f_{ACLK} = 0$  Hz,  $f_{MCLK} = f_{SMCLK} = 0$  MHz
- (8) Low-power mode 4.5 excluding SVS test conditions:  
Current for brownout included. SVS disabled (SVSHE = 0). Core regulator disabled.  
PMMREGOFF = 1; CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),  
 $f_{XT1} = 0$  Hz,  $f_{ACLK} = 0$  Hz,  $f_{MCLK} = f_{SMCLK} = 0$  MHz

## 8.9 Typical Characteristics, Low-Power Mode Supply Currents

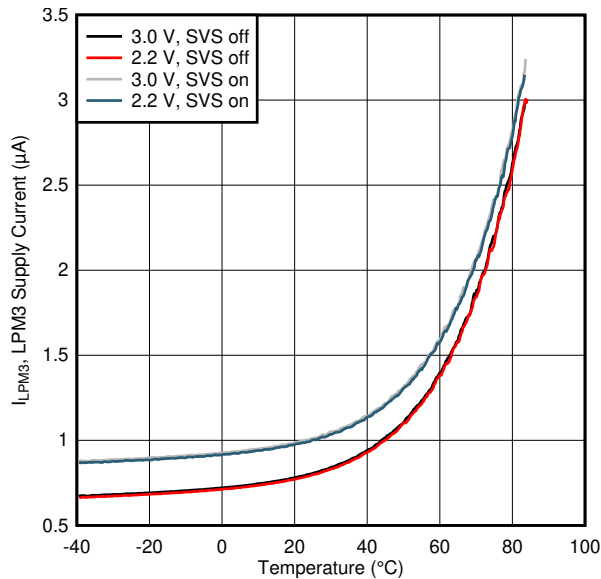


Figure 8-2. LPM3 Supply Current vs Temperature

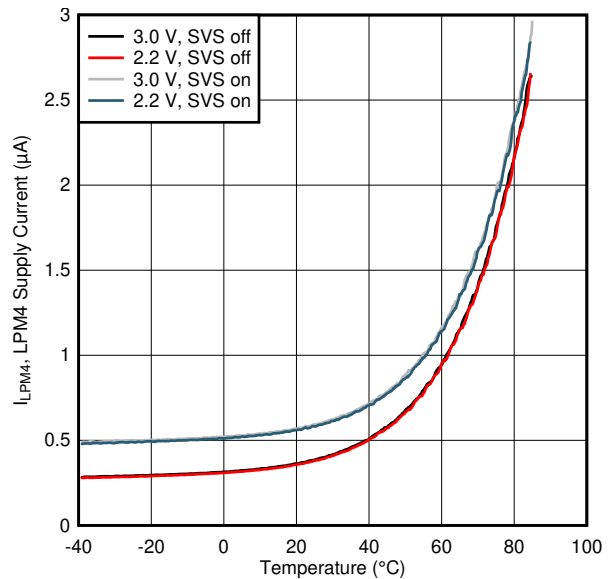


Figure 8-3. LPM4 Supply Current vs Temperature

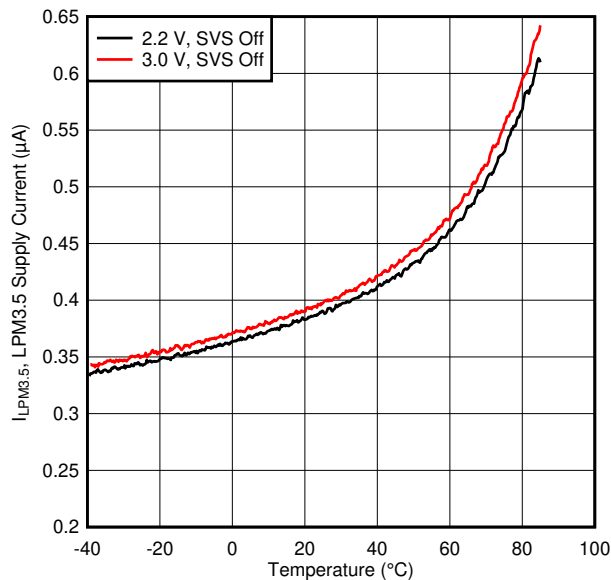


Figure 8-4. LPM3.5 Supply Current vs Temperature

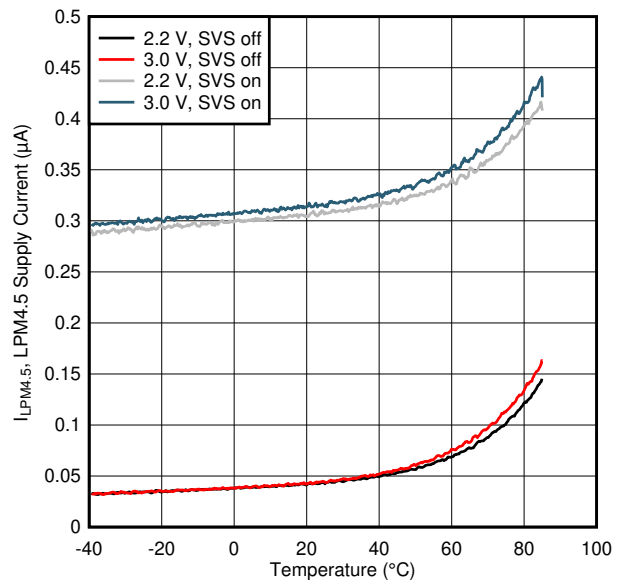


Figure 8-5. LPM4.5 Supply Current vs Temperature

## 8.10 Typical Characteristics, Current Consumption per Module

| MODULE  | TEST CONDITIONS <sup>(1)</sup>        | REFERENCE CLOCK    | MIN | TYP | MAX | UNIT   |
|---------|---------------------------------------|--------------------|-----|-----|-----|--------|
| Timer_A |                                       | Module input clock |     | 3   |     | μA/MHz |
| Timer_B |                                       | Module input clock |     | 5   |     | μA/MHz |
| eUSCI_A | UART mode                             | Module input clock |     | 6.3 |     | μA/MHz |
| eUSCI_A | SPI mode                              | Module input clock |     | 4   |     | μA/MHz |
| eUSCI_B | SPI mode                              | Module input clock |     | 4   |     | μA/MHz |
| eUSCI_B | I <sup>2</sup> C mode, 100 kbaud      | Module input clock |     | 4   |     | μA/MHz |
| RTC_C   |                                       | 32 kHz             |     | 100 |     | nA     |
| MPY     | Only from start to end of operation   | MCLK               |     | 28  |     | μA/MHz |
| CRC16   | Only from start to end of operation   | MCLK               |     | 3.3 |     | μA/MHz |
| CRC32   | Only from start to end of operation   | MCLK               |     | 3.3 |     | μA/MHz |
| LEA     | 256 Point Complex FFT, Data = nonzero | MCLK               |     | 86  |     | μA/MHz |
|         | 256 Point Complex FFT, Data = zero    |                    |     | 66  |     |        |

(1) For other module currents not listed here, see the module-specific parameter sections.

## 8.11 Thermal Packaging Characteristics

| THERMAL METRIC <sup>(1) (2)</sup> |                                                      | PACKAGE      | VALUE | UNIT |
|-----------------------------------|------------------------------------------------------|--------------|-------|------|
| R <sub>θJA</sub>                  | Junction-to-ambient thermal resistance, still air    | QFN-48 (RGZ) | 27.5  | °C/W |
| R <sub>θJC(TOP)</sub>             | Junction-to-case (top) thermal resistance            |              | 12.5  | °C/W |
| R <sub>θJB</sub>                  | Junction-to-board thermal resistance                 |              | 4.4   | °C/W |
| Ψ <sub>JB</sub>                   | Junction-to-board thermal characterization parameter |              | 4.4   | °C/W |
| Ψ <sub>JT</sub>                   | Junction-to-top thermal characterization parameter   |              | 0.2   | °C/W |
| R <sub>θJC(BOTTOM)</sub>          | Junction-to-case (bottom) thermal resistance         |              | 0.8   | °C/W |
| R <sub>θJA</sub>                  | Junction-to-ambient thermal resistance, still air    | QFP-64 (PM)  | 53.2  | °C/W |
| R <sub>θJC(TOP)</sub>             | Junction-to-case (top) thermal resistance            |              | 14.3  | °C/W |
| R <sub>θJB</sub>                  | Junction-to-board thermal resistance                 |              | 24.7  | °C/W |
| Ψ <sub>JB</sub>                   | Junction-to-board thermal characterization parameter |              | 24.4  | °C/W |
| Ψ <sub>JT</sub>                   | Junction-to-top thermal characterization parameter   |              | 0.6   | °C/W |
| R <sub>θJA</sub>                  | Junction-to-ambient thermal resistance, still air    | QFP-80 (PN)  | 47.9  | °C/W |
| R <sub>θJC(TOP)</sub>             | Junction-to-case (top) thermal resistance            |              | 13.0  | °C/W |
| R <sub>θJB</sub>                  | Junction-to-board thermal resistance                 |              | 22.5  | °C/W |
| Ψ <sub>JB</sub>                   | Junction-to-board thermal characterization parameter |              | 22.2  | °C/W |
| Ψ <sub>JT</sub>                   | Junction-to-top thermal characterization parameter   |              | 0.6   | °C/W |
| R <sub>θJA</sub>                  | Junction-to-ambient thermal resistance, still air    | BGA-87 (ZVW) | 60.6  | °C/W |
| R <sub>θJC(TOP)</sub>             | Junction-to-case (top) thermal resistance            |              | 18.1  | °C/W |
| R <sub>θJB</sub>                  | Junction-to-board thermal resistance                 |              | 31.8  | °C/W |
| Ψ <sub>JB</sub>                   | Junction-to-board thermal characterization parameter |              | 30.1  | °C/W |
| Ψ <sub>JT</sub>                   | Junction-to-top thermal characterization parameter   |              | 0.7   | °C/W |

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

(2) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC (R<sub>θJC</sub>) value, which is based on a JEDEC-defined 1S0P system) and will change based on environment and application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

## 8.12 Timing and Switching Characteristics

### 8.12.1 Power Supply Sequencing

TI recommends powering AVCC and DVCC pins from the same source. At a minimum, during power up, power down, and device operation, the voltage difference between AVCC and DVCC must not exceed the limits specified in [Section 8.1](#). Exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and FRAM.

[Section 8.12.1.1](#) lists the power ramp requirements.

#### 8.12.1.1 Brownout and Device Reset Power Ramp Requirements

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                      | TEST CONDITIONS                              | MIN  | MAX  | UNIT |
|----------------------------------------------------------------|----------------------------------------------|------|------|------|
| V <sub>VCC_BOR-</sub> Brownout power-down level <sup>(1)</sup> | dV <sub>CC</sub> /dt  < 3 V/s                | 0.73 | 1.66 | V    |
| V <sub>VCC_BOR+</sub> Brownout power-up level <sup>(1)</sup>   | dV <sub>CC</sub> /dt  < 3 V/s <sup>(2)</sup> | 0.79 | 1.75 | V    |

(1) Fast supply voltage changes can trigger a BOR reset even within the recommended supply voltage range. To avoid unwanted BOR resets, the supply voltage must change by less than 0.05 volts per microsecond ( $\pm 0.05$  V/ $\mu$ s). Following the data sheet recommendation for capacitor C<sub>DVCC</sub> should limit the slopes accordingly.

(2) The brownout levels are measured with a slowly changing supply.

[Section 8.12.1.2](#) lists the supply voltage supervisor characteristics.

#### 8.12.1.2 SVS

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                                   | TEST CONDITIONS                         | MIN  | TYP  | MAX  | UNIT    |
|-----------------------------------------------------------------------------|-----------------------------------------|------|------|------|---------|
| I <sub>SVSH_LPM</sub> SVS <sub>H</sub> current consumption, low power modes |                                         |      | 170  | 300  | nA      |
| V <sub>SVSH-</sub> SVS <sub>H</sub> power-down level <sup>(1)</sup>         |                                         | 1.75 | 1.80 | 1.85 | V       |
| V <sub>SVSH+</sub> SVS <sub>H</sub> power-up level <sup>(1)</sup>           |                                         | 1.77 | 1.88 | 1.99 | V       |
| V <sub>SVSH_hys</sub> SVS <sub>H</sub> hysteresis                           |                                         | 40   |      | 150  | mV      |
| t <sub>PD,SVSH,AM</sub> SVS <sub>H</sub> propagation delay, active mode     | dV <sub>VCC</sub> /dt = -10 mV/ $\mu$ s |      |      | 10   | $\mu$ s |

(1) For additional information, see the [Dynamic Voltage Scaling Power Solution for MSP430 Devices With Single-Channel LDO Reference Design](#).

### 8.12.2 Reset Timing

[Section 8.12.2.1](#) lists the input requirements of the reset pin.

#### 8.12.2.1 Reset Input

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

|                                                                                            | V <sub>CC</sub> | MIN | MAX | UNIT    |
|--------------------------------------------------------------------------------------------|-----------------|-----|-----|---------|
| t <sub>(RST)</sub> External reset pulse duration on $\overline{\text{RST}}$ <sup>(1)</sup> | 2.2 V, 3.0 V    | 2   |     | $\mu$ s |

(1) Not applicable if  $\overline{\text{RST}}$ /NMI pin configured as NMI.

### 8.12.3 Clock Specifications

LFXTCLK (see [Section 8.12.3.1](#)) is a low-frequency oscillator that can be used either with low-frequency 32768-Hz watch crystals, standard crystals, resonators, or external clock sources in the 50 kHz or below range. When in bypass mode, LFXTCLK can be driven with an external square-wave signal.

#### 8.12.3.1 Low-Frequency Crystal Oscillator, LFXT

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER <sup>(1)</sup>                                                              | TEST CONDITIONS                                                                                                                      | V <sub>CC</sub> | MIN  | TYP    | MAX  | UNIT |
|---------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------|-----------------|------|--------|------|------|
| I <sub>VCC,LFXT</sub> Current consumption                                             | f <sub>OSC</sub> = 32768 Hz,<br>LFXTBYPASS = 0, LFXTDRIVE = {0},<br>T <sub>A</sub> = 25°C, C <sub>L,eff</sub> = 3.7 pF, ESR ≈ 44 kΩ  | 3.0 V           |      | 180    |      | nA   |
|                                                                                       | f <sub>OSC</sub> = 32768 Hz,<br>LFXTBYPASS = 0, LFXTDRIVE = {1},<br>T <sub>A</sub> = 25°C, C <sub>L,eff</sub> = 6 pF, ESR ≈ 40 kΩ    |                 |      | 185    |      |      |
|                                                                                       | f <sub>OSC</sub> = 32768 Hz,<br>LFXTBYPASS = 0, LFXTDRIVE = {2},<br>T <sub>A</sub> = 25°C, C <sub>L,eff</sub> = 9 pF, ESR ≈ 40 kΩ    |                 |      | 225    |      |      |
|                                                                                       | f <sub>OSC</sub> = 32768 Hz,<br>LFXTBYPASS = 0, LFXTDRIVE = {3},<br>T <sub>A</sub> = 25°C, C <sub>L,eff</sub> = 12.5 pF, ESR ≈ 40 kΩ |                 |      | 330    |      |      |
| f <sub>LFXT</sub> LFXT oscillator crystal frequency                                   | LFXTBYPASS = 0                                                                                                                       |                 |      | 32768  |      | Hz   |
| DC <sub>LFXT</sub> LFXT oscillator duty cycle                                         | Measured at ACLK,<br>f <sub>LFXT</sub> = 32768 Hz                                                                                    |                 | 30%  |        | 70%  |      |
| f <sub>LFXT,SW</sub> LFXT oscillator logic-level square-wave input frequency          | LFXTBYPASS = 1 <sup>(2) (3)</sup>                                                                                                    |                 | 10.5 | 32.768 | 50   | kHz  |
| DC <sub>LFXT,SW</sub> LFXT oscillator logic-level square-wave input duty cycle        | LFXTBYPASS = 1                                                                                                                       |                 | 30%  |        | 70%  |      |
| OA <sub>LFXT</sub> Oscillation allowance for LF crystals <sup>(4)</sup>               | LFXTBYPASS = 0, LFXTDRIVE = {1},<br>f <sub>LFXT</sub> = 32768 Hz, C <sub>L,eff</sub> = 6 pF                                          |                 |      | 210    |      | kΩ   |
|                                                                                       | LFXTBYPASS = 0, LFXTDRIVE = {3},<br>f <sub>LFXT</sub> = 32768 Hz, C <sub>L,eff</sub> = 12.5 pF                                       |                 |      | 300    |      |      |
| C <sub>LFXIN</sub> Integrated load capacitance at LFXIN terminal <sup>(5) (6)</sup>   |                                                                                                                                      |                 |      | 2      |      | pF   |
| C <sub>LFXOUT</sub> Integrated load capacitance at LFXOUT terminal <sup>(5) (6)</sup> |                                                                                                                                      |                 |      | 2      |      | pF   |
| t <sub>START,LFXT</sub> Start-up time <sup>(7)</sup>                                  | f <sub>OSC</sub> = 32768 Hz<br>LFXTBYPASS = 0, LFXTDRIVE = {0},<br>T <sub>A</sub> = 25°C, C <sub>L,eff</sub> = 3.7 pF,               | 3.0 V           |      | 800    |      | ms   |
|                                                                                       | f <sub>OSC</sub> = 32768 Hz<br>LFXTBYPASS = 0, LFXTDRIVE = {3},<br>T <sub>A</sub> = 25°C, C <sub>L,eff</sub> = 12.5 pF               | 3.0 V           |      | 1000   |      |      |
| f <sub>Fault,LFXT</sub> Oscillator fault frequency <sup>(8) (9)</sup>                 |                                                                                                                                      |                 | 0    |        | 3500 | Hz   |

- (1) To improve EMI on the LFXT oscillator, the following guidelines should be observed.
  - Keep the trace between the device and the crystal as short as possible.
  - Design a good ground plane around the oscillator pins.
  - Prevent crosstalk from other clock or data lines into oscillator pins LFXIN and LFXOUT.
  - Avoid running PCB traces underneath or adjacent to the LFXIN and LFXOUT pins.
  - Use assembly materials and processes that avoid any parasitic load on the oscillator LFXIN and LFXOUT pins.
  - If conformal coating is used, ensure that it does not induce capacitive or resistive leakage between the oscillator pins.
- (2) When LFXTBYPASS is set, LFXT circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this datasheet. Duty cycle requirements are defined by DC<sub>LFXT,SW</sub>.
- (3) Maximum frequency of operation of the entire device cannot be exceeded.
- (4) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the LFXTDRIVE settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:

- For LFXTDRIVE = {0},  $C_{L,eff} = 3.7 \text{ pF}$
  - For LFXTDRIVE = {1},  $C_{L,eff} = 6 \text{ pF}$
  - For LFXTDRIVE = {2},  $6 \text{ pF} \leq C_{L,eff} \leq 9 \text{ pF}$
  - For LFXTDRIVE = {3},  $9 \text{ pF} \leq C_{L,eff} \leq 12.5 \text{ pF}$
- (5) This represents all the parasitic capacitance present at the LFXIN and LFXOUT terminals, respectively, including parasitic bond and package capacitance. The effective load capacitance,  $C_{L,eff}$  can be computed as  $C_{IN} \times C_{OUT} / (C_{IN} + C_{OUT})$ , where  $C_{IN}$  and  $C_{OUT}$  are the total capacitance at the LFXIN and LFXOUT terminals, respectively.
  - (6) Requires external capacitors at both terminals to meet the effective load capacitance specified by crystal manufacturers. Recommended effective load capacitance values supported are 3.7 pF, 6 pF, 9 pF, and 12.5 pF. Maximum shunt capacitance of 1.6 pF. The PCB adds additional capacitance, so it must also be considered in the overall capacitance. Verify that the recommended effective load capacitance of the selected crystal is met.
  - (7) Includes startup counter of 1024 clock cycles.
  - (8) Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specification may set the flag. A static condition or stuck at fault condition will set the flag.
  - (9) Measured with logic-level input frequency but also applies to operation with crystals.

HFXTCLK (see [Section 8.12.3.2](#)) is a high-frequency oscillator that can be used with standard crystals or resonators in the 4-MHz to 24-MHz range. When in bypass mode, HFXTCLK can be driven with an external square-wave signal.

### 8.12.3.2 High-Frequency Crystal Oscillator, HFXT

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER <sup>(1)</sup> |                                                                            | TEST CONDITIONS                                                                                                                                                                  | V <sub>CC</sub> | MIN   | TYP | MAX | UNIT |
|--------------------------|----------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|-------|-----|-----|------|
| I <sub>DVCC,HFXT</sub>   | HFXT oscillator crystal current<br>HF mode at typical ESR                  | f <sub>OSC</sub> = 4 MHz,<br>HFXTBYPASS = 0, HFXTDRIVE = 0,<br>HFFREQ = 1 <sup>(2)</sup> , T <sub>A</sub> = 25°C,<br>C <sub>L,eff</sub> = 18 pF, typical ESR, C <sub>shunt</sub> | 3.0 V           |       | 75  |     | μA   |
|                          |                                                                            | f <sub>OSC</sub> = 8 MHz,<br>HFXTBYPASS = 0, HFXTDRIVE = 1,<br>HFFREQ = 1, T <sub>A</sub> = 25°C,<br>C <sub>L,eff</sub> = 18 pF, typical ESR, C <sub>shunt</sub>                 |                 |       | 120 |     |      |
|                          |                                                                            | f <sub>OSC</sub> = 16 MHz,<br>HFXTBYPASS = 0, HFXTDRIVE = 2,<br>HFFREQ = 2, T <sub>A</sub> = 25°C<br>C <sub>L,eff</sub> = 18 pF, typical ESR, C <sub>shunt</sub>                 |                 |       | 190 |     |      |
|                          |                                                                            | f <sub>OSC</sub> = 24 MHz<br>HFXTBYPASS = 0, HFXTDRIVE = 3,<br>HFFREQ = 3, T <sub>A</sub> = 25°C<br>C <sub>L,eff</sub> = 18 pF, typical ESR, C <sub>shunt</sub>                  |                 |       | 250 |     |      |
| f <sub>HFXT</sub>        | HFXT oscillator crystal<br>frequency, crystal mode                         | HFXTBYPASS = 0, HFFREQ = 1 <sup>(2)</sup> <sup>(3)</sup>                                                                                                                         |                 | 4     |     | 8   | MHz  |
|                          |                                                                            | HFXTBYPASS = 0, HFFREQ = 2 <sup>(3)</sup>                                                                                                                                        |                 | 8.01  |     | 16  |      |
|                          |                                                                            | HFXTBYPASS = 0, HFFREQ = 3 <sup>(3)</sup>                                                                                                                                        |                 | 16.01 |     | 24  |      |
| DC <sub>HFXT</sub>       | HFXT oscillator duty cycle.                                                | Measured at SMCLK,<br>f <sub>HFXT</sub> = 16 MHz                                                                                                                                 |                 | 40%   | 50% | 60% |      |
| f <sub>HFXT,SW</sub>     | HFXT oscillator logic-level<br>square-wave input frequency,<br>bypass mode | HFXTBYPASS = 1, HFFREQ = 0 <sup>(4)</sup> <sup>(3)</sup>                                                                                                                         |                 | 0.9   |     | 4   | MHz  |
|                          |                                                                            | HFXTBYPASS = 1, HFFREQ = 1 0 <sup>(4)</sup> <sup>(3)</sup>                                                                                                                       |                 | 4.01  |     | 8   |      |
|                          |                                                                            | HFXTBYPASS = 1, HFFREQ = 20 <sup>(4)</sup> <sup>(3)</sup>                                                                                                                        |                 | 8.01  |     | 16  |      |
|                          |                                                                            | HFXTBYPASS = 1, HFFREQ = 3 0 <sup>(4)</sup> <sup>(3)</sup>                                                                                                                       |                 | 16.01 |     | 24  |      |
| DC <sub>HFXT, SW</sub>   | HFXT oscillator logic-level<br>square-wave input duty cycle                | HFXTBYPASS = 1                                                                                                                                                                   |                 | 40%   |     | 60% |      |

### 8.12.3.2 High-Frequency Crystal Oscillator, HFXT (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER <sup>(1)</sup> |                                                                   | TEST CONDITIONS                                                                                                         | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|--------------------------|-------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------|-----------------|-----|-----|-----|------|
| OA <sub>HFXT</sub>       | Oscillation allowance for HFXT crystals <sup>(5)</sup>            | HFXTBYPASS = 0, HFXTDRIVE = 0, HFFREQ = 1 <sup>(2)</sup> , f <sub>HFXT,HF</sub> = 4 MHz, C <sub>L,eff</sub> = 16 pF     |                 |     | 450 |     | Ω    |
|                          |                                                                   | HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 1, f <sub>HFXT,HF</sub> = 8 MHz, C <sub>L,eff</sub> = 16 pF                     |                 |     | 320 |     |      |
|                          |                                                                   | HFXTBYPASS = 0, HFXTDRIVE = 2, HFFREQ = 2, f <sub>HFXT,HF</sub> = 16 MHz, C <sub>L,eff</sub> = 16 pF                    |                 |     | 200 |     |      |
|                          |                                                                   | HFXTBYPASS = 0, HFXTDRIVE = 3, HFFREQ = 3, f <sub>HFXT,HF</sub> = 24 MHz, C <sub>L,eff</sub> = 16 pF                    |                 |     | 200 |     |      |
| t <sub>START,HFXT</sub>  | Startup time <sup>(6)</sup>                                       | f <sub>OSC</sub> = 4 MHz, HFXTBYPASS = 0, HFXTDRIVE = 0, HFFREQ = 1, T <sub>A</sub> = 25°C, C <sub>L,eff</sub> = 16 pF  | 3.0 V           |     | 1.6 |     | ms   |
|                          |                                                                   | f <sub>OSC</sub> = 24 MHz, HFXTBYPASS = 0, HFXTDRIVE = 3, HFFREQ = 3, T <sub>A</sub> = 25°C, C <sub>L,eff</sub> = 16 pF |                 |     | 0.6 |     |      |
| C <sub>HFXIN</sub>       | Integrated load capacitance at HFXIN terminal <sup>(7) (8)</sup>  |                                                                                                                         |                 |     | 2   |     | pF   |
| C <sub>HFXOUT</sub>      | Integrated load capacitance at HFXOUT terminal <sup>(7) (8)</sup> |                                                                                                                         |                 |     | 2   |     | pF   |
| f <sub>Fault,HFXT</sub>  | Oscillator fault frequency <sup>(9) (10)</sup>                    |                                                                                                                         |                 | 0   |     | 800 | kHz  |

- (1) To improve EMI on the HFXT oscillator the following guidelines should be observed.
  - Keep the traces between the device and the crystal as short as possible.
  - Design a good ground plane around the oscillator pins.
  - Prevent crosstalk from other clock or data lines into oscillator pins HFXIN and HFXOUT.
  - Avoid running PCB traces underneath or adjacent to the HFXIN and HFXOUT pins.
  - Use assembly materials and processes that avoid any parasitic load on the oscillator HFXIN and HFXOUT pins.
  - If conformal coating is used, ensure that it does not induce capacitive or resistive leakage between the oscillator pins.
- (2) HFFREQ = {0} is not supported for HFXT crystal mode of operation.
- (3) Maximum frequency of operation of the entire device cannot be exceeded.
- (4) When HFXTBYPASS is set, HFXT circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this datasheet. Duty cycle requirements are defined by DC<sub>HFXT, SW</sub>.
- (5) Oscillation allowance is based on a safety factor of 5 for recommended crystals.
- (6) Includes startup counter of 1024 clock cycles.
- (7) This represents all the parasitic capacitance present at the HFXIN and HFXOUT terminals, respectively, including parasitic bond and package capacitance. The effective load capacitance, C<sub>L,eff</sub> can be computed as C<sub>IN</sub> × C<sub>OUT</sub> / (C<sub>IN</sub> + C<sub>OUT</sub>), where C<sub>IN</sub> and C<sub>OUT</sub> is the total capacitance at the HFXIN and HFXOUT terminals, respectively.
- (8) Requires external capacitors at both terminals to meet the effective load capacitance specified by crystal manufacturers. Recommended effective load capacitance values supported are 14 pF, 16 pF, and 18 pF. Maximum shunt capacitance of 7 pF. The PCB adds additional capacitance, so it must also be considered in the overall capacitance. Verify that the recommended effective load capacitance of the selected crystal is met.
- (9) Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX might set the flag. A static condition or stuck at fault condition will set the flag.
- (10) Measured with logic-level input frequency but also applies to operation with crystals.

The DCO (see [Section 8.12.3.3](#)) is an internal digitally controlled oscillator (DCO) with selectable frequencies.

### 8.12.3.3 DCO

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                |                                         | TEST CONDITIONS                                                                                                                                                                           | V <sub>CC</sub> | MIN | TYP   | MAX   | UNIT |
|--------------------------|-----------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|-----|-------|-------|------|
| f <sub>DCO1</sub>        | DCO frequency range<br>1 MHz, trimmed   | Measured at SMCLK, divide by 1,<br>DCORSEL = 0, DCOFSEL = 0,<br>DCORSEL = 1, DCOFSEL = 0                                                                                                  |                 |     | 1     | ±3.5% | MHz  |
| f <sub>DCO2.7</sub>      | DCO frequency range<br>2.7 MHz, trimmed | Measured at SMCLK, divide by 1,<br>DCORSEL = 0, DCOFSEL = 1                                                                                                                               |                 |     | 2.667 | ±3.5% | MHz  |
| f <sub>DCO3.5</sub>      | DCO frequency range<br>3.5 MHz, trimmed | Measured at SMCLK, divide by 1,<br>DCORSEL = 0, DCOFSEL = 2                                                                                                                               |                 |     | 3.5   | ±3.5% | MHz  |
| f <sub>DCO4</sub>        | DCO frequency range<br>4 MHz, trimmed   | Measured at SMCLK, divide by 1<br>DCORSEL = 0, DCOFSEL = 3                                                                                                                                |                 |     | 4     | ±3.5% | MHz  |
| f <sub>DCO5.3</sub>      | DCO frequency range<br>5.3 MHz, trimmed | Measured at SMCLK, divide by 1,<br>DCORSEL = 0, DCOFSEL = 4,<br>DCORSEL = 1, DCOFSEL = 1                                                                                                  |                 |     | 5.333 | ±3.5% | MHz  |
| f <sub>DCO7</sub>        | DCO frequency range<br>7 MHz, trimmed   | Measured at SMCLK, divide by 1,<br>DCORSEL = 0, DCOFSEL = 5,<br>DCORSEL = 1, DCOFSEL = 2                                                                                                  |                 |     | 7     | ±3.5% | MHz  |
| f <sub>DCO8</sub>        | DCO frequency range<br>8 MHz, trimmed   | Measured at SMCLK, divide by 1,<br>DCORSEL = 0, DCOFSEL = 6,<br>DCORSEL = 1, DCOFSEL = 3                                                                                                  |                 |     | 8     | ±3.5% | MHz  |
| f <sub>DCO16</sub>       | DCO frequency range<br>16 MHz, trimmed  | Measured at SMCLK, divide by 1,<br>DCORSEL = 1, DCOFSEL = 4                                                                                                                               |                 |     | 16    | ±3.5% | MHz  |
| f <sub>DCO21</sub>       | DCO frequency range<br>21 MHz, trimmed  | Measured at SMCLK, divide by 2,<br>DCORSEL = 1, DCOFSEL = 5                                                                                                                               |                 |     | 21    | ±3.5% | MHz  |
| f <sub>DCO24</sub>       | DCO frequency range<br>24 MHz, trimmed  | Measured at SMCLK, divide by 2,<br>DCORSEL = 1, DCOFSEL = 6                                                                                                                               |                 |     | 24    | ±3.5% | MHz  |
| f <sub>DCO,DC</sub>      | Duty cycle                              | Measured at SMCLK, divide by 1,<br>No external divide, all DCORSEL and<br>DCOFSEL settings except DCORSEL = 1<br>with DCOFSEL = 5, and DCORSEL = 1 with<br>DCOFSEL = 6                    |                 | 48% | 50%   | 52%   |      |
| t <sub>DCO, JITTER</sub> | DCO jitter                              | Based on f <sub>signal</sub> = 10 kHz and DCO used for<br>12-bit SAR ADC sampling source. This<br>achieves greater than 74-dB SNR due to<br>jitter (that is, limited by ADC performance). |                 |     | 2     | 3     | ns   |
| df <sub>DCO</sub> /dT    | DCO temperature drift <sup>(1)</sup>    |                                                                                                                                                                                           | 3.0 V           |     | 0.01  |       | %/°C |

(1) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))

### 8.12.3.4 Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                           |                                    | TEST CONDITIONS                 | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|-------------------------------------|------------------------------------|---------------------------------|-----------------|-----|-----|-----|------|
| I <sub>VLO</sub>                    | Current consumption                |                                 |                 |     | 100 |     | nA   |
| f <sub>VLO</sub>                    | VLO frequency <sup>(1)</sup>       | Measured at ACLK                |                 | 6   | 9.4 | 14  | kHz  |
| df <sub>VLO</sub> /dT               | VLO frequency temperature drift    | Measured at ACLK <sup>(2)</sup> |                 |     | 0.2 |     | %/°C |
| df <sub>VLO</sub> /dV <sub>CC</sub> | VLO frequency supply voltage drift | Measured at ACLK <sup>(3)</sup> |                 |     | 0.7 |     | %/V  |
| f <sub>VLO,DC</sub>                 | Duty cycle                         | Measured at ACLK                |                 | 40% | 50% | 60% |      |

(1) VLO frequency may decrease in LPM3 or LPM4 mode. The typical ratio of VLO frequencies (LPM3/4 to AM) is 85%.

(2) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))

(3) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

The module oscillator (MODOSC) is an internal low-power oscillator with 5-MHz typical frequency (see [Section 8.12.3.5](#)).

### 8.12.3.5 Module Oscillator (MODOSC)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                             |                                                      | TEST CONDITIONS                | MIN | TYP  | MAX | UNIT |
|---------------------------------------|------------------------------------------------------|--------------------------------|-----|------|-----|------|
| I <sub>MODOSC</sub>                   | Current consumption                                  | Enabled                        |     | 25   |     | μA   |
| f <sub>MODOSC</sub>                   | MODOSC frequency                                     |                                | 4.0 | 4.8  | 5.4 | MHz  |
| f <sub>MODOSC</sub> /dT               | MODOSC frequency temperature drift <sup>(1)</sup>    |                                |     | 0.08 |     | %/°C |
| f <sub>MODOSC</sub> /dV <sub>CC</sub> | MODOSC frequency supply voltage drift <sup>(2)</sup> |                                |     | 1.4  |     | %/V  |
| DC <sub>MODOSC</sub>                  | Duty cycle                                           | Measured at SMCLK, divide by 1 | 40% | 50%  | 60% |      |

(1) Calculated using the box method: (MAX(−40°C to 85°C) – MIN(−40°C to 85°C)) / MIN(−40°C to 85°C) / (85°C – (−40°C))

(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

### 8.12.4 Wake-up Characteristics

[Section 8.12.4.1](#) lists the wake-up times.

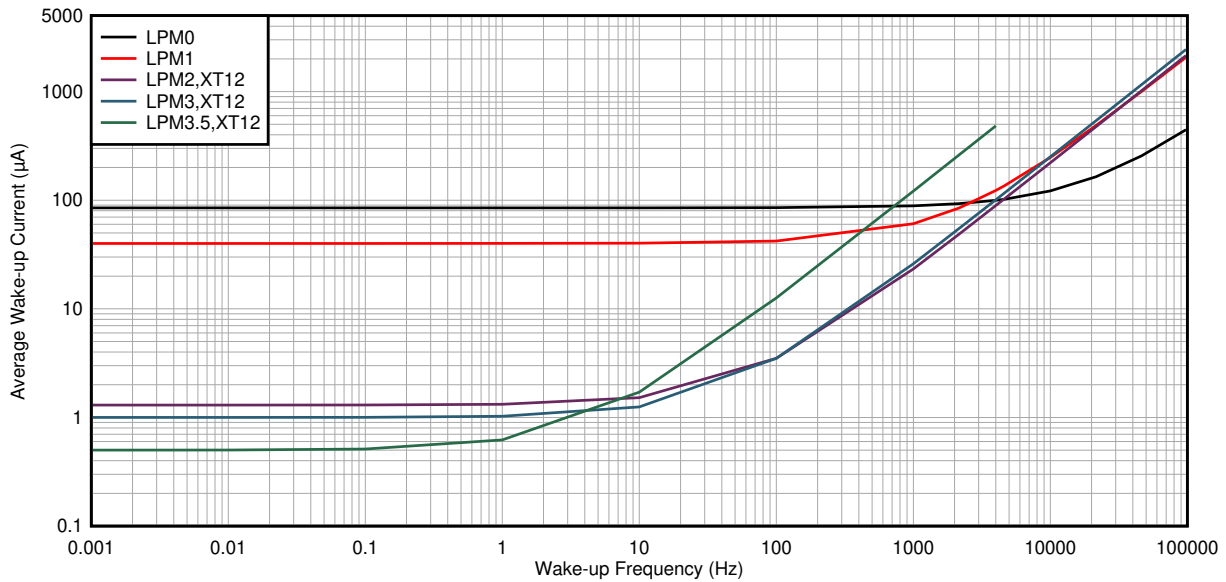
#### 8.12.4.1 Wake-up Times From Low-Power Modes and Reset

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 8-6](#) and [Figure 8-7](#))

| PARAMETER                   |                                                                                                                                                                  | TEST CONDITIONS | V <sub>CC</sub> | MIN | TYP                                | MAX                             | UNIT |
|-----------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|-----------------|-----|------------------------------------|---------------------------------|------|
| t <sub>WAKE-UP FRAM</sub>   | (Additional) wake-up time to activate the FRAM in AM if previously disabled by the FRAM controller or from an LPM if immediate activation is selected for wakeup |                 |                 |     | 6                                  | 10                              | μs   |
| t <sub>WAKE-UP LPM0</sub>   | Wake-up time from LPM0 to active mode <sup>(1)</sup>                                                                                                             |                 | 2.2 V, 3.0 V    |     | 400 ns +<br>1.5 / f <sub>DCO</sub> |                                 |      |
| t <sub>WAKE-UP LPM1</sub>   | Wake-up time from LPM1 to active mode <sup>(1)</sup>                                                                                                             |                 | 2.2 V, 3.0 V    |     | 6                                  |                                 | μs   |
| t <sub>WAKE-UP LPM2</sub>   | Wake-up time from LPM2 to active mode <sup>(1)</sup>                                                                                                             |                 | 2.2 V, 3.0 V    |     | 6                                  |                                 | μs   |
| t <sub>WAKE-UP LPM3</sub>   | Wake-up time from LPM3 to active mode <sup>(1)</sup>                                                                                                             |                 | 2.2 V, 3.0 V    |     | 6.6 +<br>2.0 / f <sub>DCO</sub>    | 9.6 +<br>2.5 / f <sub>DCO</sub> | μs   |
| t <sub>WAKE-UP LPM4</sub>   | Wake-up time from LPM4 to active mode <sup>(1)</sup>                                                                                                             |                 | 2.2 V, 3.0 V    |     | 6.6 +<br>2.0 / f <sub>DCO</sub>    | 9.6 +<br>2.5 / f <sub>DCO</sub> | μs   |
| t <sub>WAKE-UP LPM3.5</sub> | Wake-up time from LPM3.5 to active mode <sup>(2)</sup>                                                                                                           |                 | 2.2 V, 3.0 V    |     | 250                                | 350                             | μs   |
| t <sub>WAKE-UP LPM4.5</sub> | Wake-up time from LPM4.5 to active mode <sup>(2)</sup>                                                                                                           | SVSHE = 1       | 2.2 V, 3.0 V    |     | 250                                | 350                             | μs   |
|                             |                                                                                                                                                                  | SVSHE = 0       | 2.2 V, 3.0 V    |     | 0.4                                | 0.8                             | ms   |
| t <sub>WAKE-UP-RST</sub>    | Wake-up time from a $\overline{\text{RST}}$ pin triggered reset to active mode <sup>(2)</sup>                                                                    |                 | 2.2 V, 3.0 V    |     | 300                                | 403                             | μs   |
| t <sub>WAKE-UP-BOR</sub>    | Wake-up time from power-up to active mode <sup>(2)</sup>                                                                                                         |                 | 2.2 V, 3.0 V    |     | 0.5                                | 1                               | ms   |

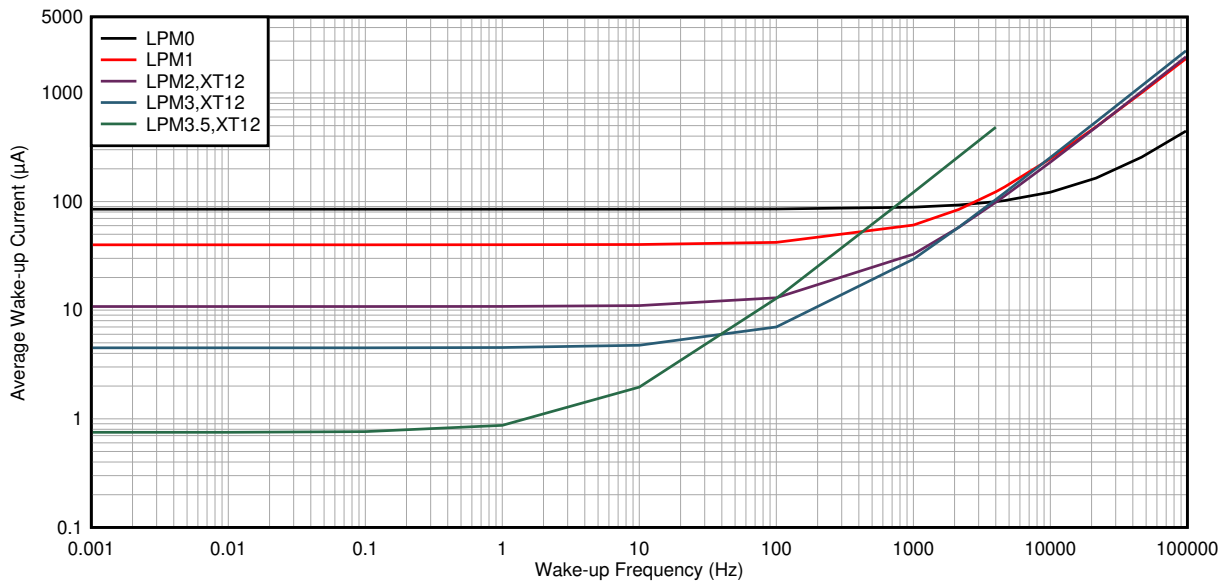
- (1) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) to the first externally observable MCLK clock edge with MCLKREQEN = 1. This time includes the activation of the FRAM during wake up. With MCLKREQEN = 0, the externally observable MCLK clock is gated one additional cycle.
- (2) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) until the first instruction of the user program is executed.

#### 8.12.4.2 Typical Characteristics, Average LPM Currents vs Wake-up Frequency



The average wake-up current does not include the energy required in active mode; for example, for an interrupt service routine (ISR) or to reconfigure the device.

**Figure 8-6. Average LPM Currents vs Wake-up Frequency at 25°C**



The average wake-up current does not include the energy required in active mode; for example, for an ISR or to reconfigure the device.

**Figure 8-7. Average LPM Currents vs Wake-up Frequency at 85°C**

### 8.12.4.3 Typical Wake-up Charge

Section 8.12.4.3 lists the typical charge required to wake up from LPM or reset.

| PARAMETER <sup>(1)</sup>    |                                                                                                                      | TEST CONDITIONS | MIN | TYP  | MAX | UNIT |
|-----------------------------|----------------------------------------------------------------------------------------------------------------------|-----------------|-----|------|-----|------|
| Q <sub>WAKE-UP FRAM</sub>   | Charge used for activating the FRAM in AM or during wake-up from LPM0 if previously disabled by the FRAM controller. |                 |     | 16.5 |     | nAs  |
| Q <sub>WAKE-UP LPM0</sub>   | Charge used for wake-up from LPM0 to active mode (with FRAM active)                                                  |                 |     | 3.8  |     | nAs  |
| Q <sub>WAKE-UP LPM1</sub>   | Charge used for wake-up from LPM1 to active mode (with FRAM active)                                                  |                 |     | 21   |     | nAs  |
| Q <sub>WAKE-UP LPM2</sub>   | Charge used for wake-up from LPM2 to active mode (with FRAM active)                                                  |                 |     | 22   |     | nAs  |
| Q <sub>WAKE-UP LPM3</sub>   | Charge used for wake-up from LPM3 to active mode (with FRAM active)                                                  |                 |     | 25   |     | nAs  |
| Q <sub>WAKE-UP LPM4</sub>   | Charge used for wake-up from LPM4 to active mode (with FRAM active)                                                  |                 |     | 25   |     | nAs  |
| Q <sub>WAKE-UP LPM3.5</sub> | Charge used for wake-up from LPM3.5 to active mode <sup>(2)</sup>                                                    |                 |     | 121  |     | nAs  |
| Q <sub>WAKE-UP LPM4.5</sub> | Charge used for wake-up from LPM4.5 to active mode <sup>(2)</sup>                                                    | SVSHE = 1       |     | 123  |     | nAs  |
|                             |                                                                                                                      | SVSHE = 0       |     | 121  |     |      |
| Q <sub>WAKE-UP-RESET</sub>  | Charge used for reset from RST or BOR event to active mode <sup>(2)</sup>                                            |                 |     | 102  |     | nAs  |

(1) Charge used during the wake-up time from a given low-power mode to active mode. This does not include the energy required in active mode (for example, for an ISR).

(2) Charge required until start of user code. This does not include the energy required to reconfigure the device.

## 8.12.5 Digital I/Os

Section 8.12.5.1 lists the characteristics of the digital inputs.

### 8.12.5.1 Digital Inputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                                                                           | TEST CONDITIONS                                                                                                             | V <sub>CC</sub> | MIN  | TYP | MAX  | UNIT |
|---------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------|-----------------|------|-----|------|------|
| V <sub>IT+</sub> Positive-going input threshold voltage                                                             |                                                                                                                             | 2.2 V           | 1.2  |     | 1.65 | V    |
|                                                                                                                     |                                                                                                                             | 3.0 V           | 1.65 |     | 2.25 |      |
| V <sub>IT-</sub> Negative-going input threshold voltage                                                             |                                                                                                                             | 2.2 V           | 0.55 |     | 1.00 | V    |
|                                                                                                                     |                                                                                                                             | 3.0 V           | 0.75 |     | 1.35 |      |
| V <sub>hys</sub> Input voltage hysteresis (V <sub>IT+</sub> – V <sub>IT-</sub> )                                    |                                                                                                                             | 2.2 V           | 0.44 |     | 0.98 | V    |
|                                                                                                                     |                                                                                                                             | 3.0 V           | 0.60 |     | 1.30 |      |
| R <sub>Pull</sub> Pullup or pulldown resistor                                                                       | For pullup: V <sub>IN</sub> = V <sub>SS</sub> .<br>For pulldown: V <sub>IN</sub> = V <sub>CC</sub>                          |                 | 20   | 35  | 50   | kΩ   |
| C <sub>I,dig</sub> Input capacitance, digital only port pins                                                        | V <sub>IN</sub> = V <sub>SS</sub> or V <sub>CC</sub>                                                                        |                 |      | 3   |      | pF   |
| C <sub>I,ana</sub> Input capacitance, port pins with shared analog functions <sup>(1)</sup>                         | V <sub>IN</sub> = V <sub>SS</sub> or V <sub>CC</sub>                                                                        |                 |      | 5   |      | pF   |
| I <sub>lkg(Px.y)</sub> High-impedance input leakage current                                                         | See <sup>(2)</sup> <sup>(3)</sup>                                                                                           | 2.2 V,<br>3.0 V | –20  |     | +20  | nA   |
| t <sub>(int)</sub> External interrupt timing (external trigger pulse duration to set interrupt flag) <sup>(4)</sup> | Ports with interrupt capability (see the <a href="#">Functional Block Diagram</a> and <a href="#">Signal Descriptions</a> ) | 2.2 V,<br>3.0 V | 20   |     |      | ns   |
| t <sub>(RST)</sub> External reset pulse duration on $\overline{\text{RST}}$ <sup>(5)</sup>                          |                                                                                                                             | 2.2 V,<br>3.0 V | 2    |     |      | μs   |

- (1) If the port pins PJ.4/LFXIN and PJ.5/LFXOUT are used as digital I/Os, they are connected by a 4-pF capacitor and a 35-MΩ resistor in series. At frequencies of approximately 1 kHz and lower, the 4-pF capacitor can add to the pin capacitance of PJ.4/LFXIN and/or PJ.5/LFXOUT.
- (2) The input leakage current is measured with V<sub>SS</sub> or V<sub>CC</sub> applied to the corresponding pins, unless otherwise noted.
- (3) The input leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.
- (4) An external signal sets the interrupt flag every time the minimum interrupt pulse duration t<sub>(int)</sub> is met. It may be set by trigger signals shorter than t<sub>(int)</sub>.
- (5) Not applicable if  $\overline{\text{RST}}$ /NMI pin configured as NMI.

Section 8.12.5.2 lists the characteristics of the digital outputs.

### 8.12.5.2 Digital Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                                           | TEST CONDITIONS                                                                       | V <sub>CC</sub> | MIN                    | TYP | MAX                    | UNIT |
|-------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|-----------------|------------------------|-----|------------------------|------|
| V <sub>OH</sub> High-level output voltage<br>(see Figure 8-10 and Figure 8-11)      | I <sub>(OHmax)</sub> = –1 mA <sup>(1)</sup>                                           | 2.2 V           | V <sub>CC</sub> – 0.25 |     | V <sub>CC</sub>        | V    |
|                                                                                     | I <sub>(OHmax)</sub> = –3 mA <sup>(2)</sup>                                           |                 | V <sub>CC</sub> – 0.60 |     | V <sub>CC</sub>        |      |
|                                                                                     | I <sub>(OHmax)</sub> = –2 mA <sup>(1)</sup>                                           | 3.0 V           | V <sub>CC</sub> – 0.25 |     | V <sub>CC</sub>        |      |
|                                                                                     | I <sub>(OHmax)</sub> = –6 mA <sup>(2)</sup>                                           |                 | V <sub>CC</sub> – 0.60 |     | V <sub>CC</sub>        |      |
| V <sub>OL</sub> Low-level output voltage<br>(see Figure 8-8 and Figure 8-9)         | I <sub>(OLmax)</sub> = 1 mA <sup>(1)</sup>                                            | 2.2 V           | V <sub>SS</sub>        |     | V <sub>SS</sub> + 0.25 | V    |
|                                                                                     | I <sub>(OLmax)</sub> = 3 mA <sup>(2)</sup>                                            |                 | V <sub>SS</sub>        |     | V <sub>SS</sub> + 0.60 |      |
|                                                                                     | I <sub>(OLmax)</sub> = 2 mA <sup>(1)</sup>                                            | 3.0 V           | V <sub>SS</sub>        |     | V <sub>SS</sub> + 0.25 |      |
|                                                                                     | I <sub>(OLmax)</sub> = 6 mA <sup>(2)</sup>                                            |                 | V <sub>SS</sub>        |     | V <sub>SS</sub> + 0.60 |      |
| f <sub>Px,y</sub> Port output frequency (with load) <sup>(3)</sup>                  | C <sub>L</sub> = 20 pF, R <sub>L</sub> <sup>(4)</sup> <sup>(5)</sup>                  | 2.2 V           | 16                     |     |                        | MHz  |
|                                                                                     |                                                                                       | 3.0 V           | 16                     |     |                        |      |
| f <sub>Port_CLK</sub> Clock output frequency <sup>(3)</sup>                         | ACLK, MCLK, or SMCLK at configured output port, C <sub>L</sub> = 20 pF <sup>(5)</sup> | 2.2 V           | 16                     |     |                        | MHz  |
|                                                                                     |                                                                                       | 3.0 V           | 16                     |     |                        |      |
| t <sub>rise,dig</sub> Port output rise time, digital only port pins                 | C <sub>L</sub> = 20 pF                                                                | 2.2 V           |                        | 4   | 15                     | ns   |
|                                                                                     |                                                                                       | 3.0 V           |                        | 3   | 15                     |      |
| t <sub>fall,dig</sub> Port output fall time, digital only port pins                 | C <sub>L</sub> = 20 pF                                                                | 2.2 V           |                        | 4   | 15                     | ns   |
|                                                                                     |                                                                                       | 3.0 V           |                        | 3   | 15                     |      |
| t <sub>rise,ana</sub> Port output rise time, port pins with shared analog functions | C <sub>L</sub> = 20 pF                                                                | 2.2 V           |                        | 6   | 15                     | ns   |
|                                                                                     |                                                                                       | 3.0 V           |                        | 4   | 15                     |      |
| t <sub>fall,ana</sub> Port output fall time, port pins with shared analog functions | C <sub>L</sub> = 20 pF                                                                | 2.2 V           |                        | 6   | 15                     | ns   |
|                                                                                     |                                                                                       | 3.0 V           |                        | 4   | 15                     |      |

- (1) The maximum total current, I<sub>(OHmax)</sub> and I<sub>(OLmax)</sub>, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
- (2) The maximum total current, I<sub>(OHmax)</sub> and I<sub>(OLmax)</sub>, for all outputs combined should not exceed ±100 mA to hold the maximum voltage drop specified.
- (3) The port can output frequencies at least up to the specified limit, and it might support higher frequencies.
- (4) A resistive divider with 2 × R1 and R1 = 1.6 kΩ between V<sub>CC</sub> and V<sub>SS</sub> is used as load. The output is connected to the center tap of the divider. C<sub>L</sub> = 20 pF is connected from the output to V<sub>SS</sub>.
- (5) The output voltage reaches at least 10% and 90% V<sub>CC</sub> at the specified toggle frequency.

### 8.12.5.3 Typical Characteristics, Digital Outputs at 3.0 V and 2.2 V

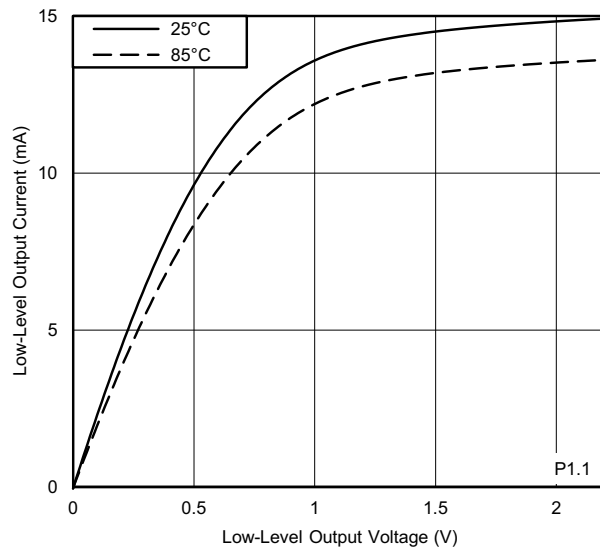


Figure 8-8. Typical Low-Level Output Current vs Low-Level Output Voltage

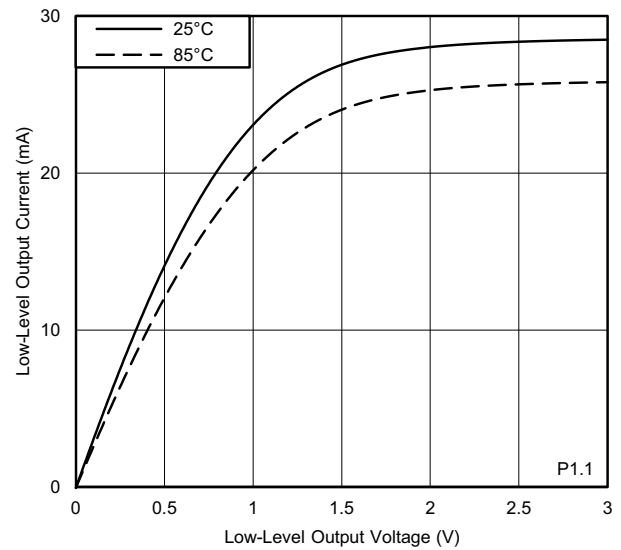


Figure 8-9. Typical Low-Level Output Current vs Low-Level Output Voltage

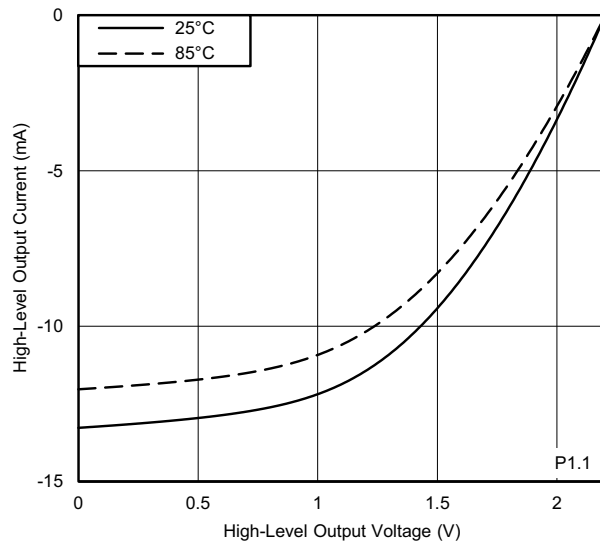


Figure 8-10. Typical High-Level Output Current vs High-Level Output Voltage

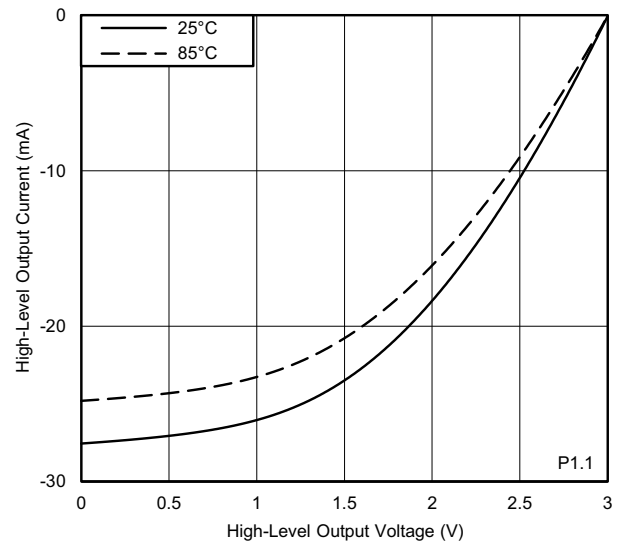


Figure 8-11. Typical High-Level Output Current vs High-Level Output Voltage

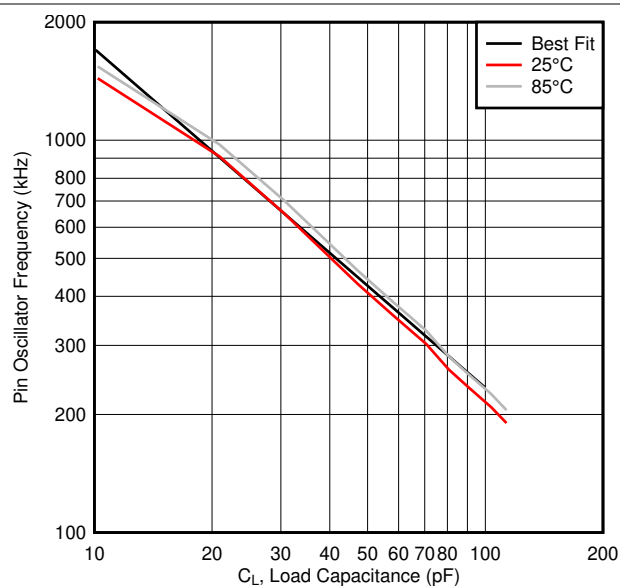
### 8.12.5.4 Pin-Oscillator Frequency, Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

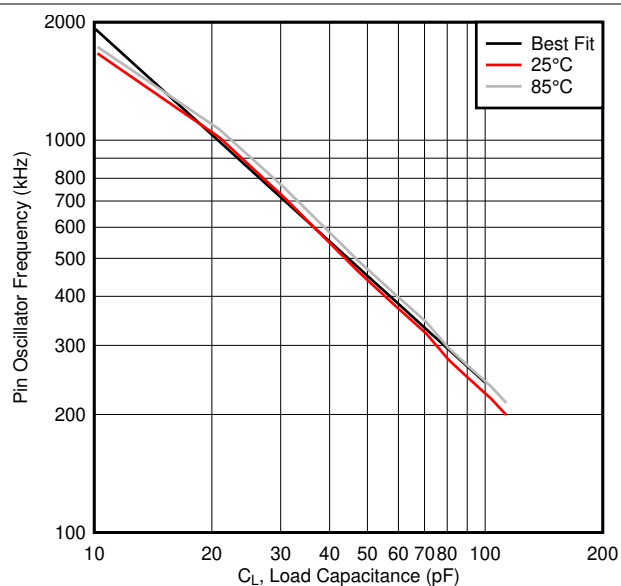
| PARAMETER                                                                 | TEST CONDITIONS                   | $V_{CC}$ | MIN | TYP  | MAX | UNIT |
|---------------------------------------------------------------------------|-----------------------------------|----------|-----|------|-----|------|
| $f_{oPx,y}$ Pin-oscillator frequency<br>(see Figure 8-12 and Figure 8-13) | Px.y, $C_L = 10 \text{ pF}^{(1)}$ | 3.0 V    |     | 1200 |     | kHz  |
|                                                                           | Px.y, $C_L = 20 \text{ pF}^{(1)}$ | 3.0 V    |     | 650  |     | kHz  |

(1)  $C_L$  is the external load capacitance connected from the output to  $V_{SS}$  and includes all parasitic effects such as PCB traces.

### 8.12.5.5 Typical Characteristics, Pin-Oscillator Frequency



**Figure 8-12. Typical Oscillation Frequency vs Load Capacitance**



**Figure 8-13. Typical Oscillation Frequency vs Load Capacitance**

### 8.12.6 LEA (Low-Energy Accelerator) (MSP430FR599x Only)

The LEA module is a hardware engine designed for operations that involve vector-based signal processing. [Section 8.12.6.1](#) lists the performance characteristics of the LEA module.

#### 8.12.6.1 Low Energy Accelerator Performance

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER |                                                 | TEST CONDITIONS                                                                    |                                            | MIN | TYP | MAX | UNIT          |
|-----------|-------------------------------------------------|------------------------------------------------------------------------------------|--------------------------------------------|-----|-----|-----|---------------|
| $f_{LEA}$ | Frequency for specified performance             | MCLK                                                                               |                                            |     | 16  |     | MHz           |
| W_LEA_FFT | LEA subsystem energy on fast Fourier transform  | Complex FFT 128-point Q.15 with random data in LEA-RAM                             | $V_{Core} = 3\text{ V}$ ,<br>MCLK = 16 MHz |     | 350 |     | nJ            |
| W_LEA_FIR | LEA subsystem energy on finite impulse response | Real FIR on random Q.31 data with 128 taps on 24 points                            | $V_{Core} = 3\text{ V}$ ,<br>MCLK = 16 MHz |     | 2.6 |     | $\mu\text{J}$ |
| W_LEA_ADD | LEA subsystem energy on additions               | On 32 Q.31 elements with random value out of LEA-RAM with linear address increment | $V_{Core} = 3\text{ V}$ ,<br>MCLK = 16 MHz |     | 6.6 |     | nJ            |

### 8.12.7 Timer\_A and Timer\_B

Timer\_A and Timer\_B are 16-bit timers and counters with multiple capture/compare registers. [Section 8.12.7.1](#) lists the Timer\_A characteristics, and [Section 8.12.7.2](#) lists the Timer\_B characteristics.

#### 8.12.7.1 Timer\_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER    |                               | TEST CONDITIONS                                                            | $V_{CC}$     | MIN | MAX | UNIT |
|--------------|-------------------------------|----------------------------------------------------------------------------|--------------|-----|-----|------|
| $f_{TA}$     | Timer_A input clock frequency | Internal: SMCLK or ACLK,<br>External: TACLK,<br>Duty cycle = 50% $\pm$ 10% | 2.2 V, 3.0 V |     | 16  | MHz  |
| $t_{TA,cap}$ | Timer_A capture timing        | All capture inputs, minimum pulse duration required for capture            | 2.2 V, 3.0 V | 20  |     | ns   |

#### 8.12.7.2 Timer\_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER    |                               | TEST CONDITIONS                                                            | $V_{CC}$     | MIN | MAX | UNIT |
|--------------|-------------------------------|----------------------------------------------------------------------------|--------------|-----|-----|------|
| $f_{TB}$     | Timer_B input clock frequency | Internal: SMCLK or ACLK,<br>External: TBCLK,<br>Duty cycle = 50% $\pm$ 10% | 2.2 V, 3.0 V |     | 16  | MHz  |
| $t_{TB,cap}$ | Timer_B capture timing        | All capture inputs, minimum pulse duration required for capture            | 2.2 V, 3.0 V | 20  |     | ns   |

## 8.12.8 eUSCI

The enhanced universal serial communication interface (eUSCI) supports multiple serial communication modes with one hardware module. The eUSCI\_A module supports UART and SPI modes. The eUSCI\_B module supports I<sup>2</sup>C and SPI modes.

Section 8.12.8.1 lists the UART clock frequencies.

### 8.12.8.1 eUSCI (UART Mode) Clock Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                              | TEST CONDITIONS                                                      | MIN | MAX | UNIT |
|------------------------------------------------------------------------|----------------------------------------------------------------------|-----|-----|------|
| f <sub>eUSCI</sub> eUSCI input clock frequency                         | Internal: SMCLK or ACLK,<br>External: UCLK,<br>Duty cycle = 50% ±10% |     | 16  | MHz  |
| f <sub>BITCLK</sub> BITCLK clock frequency (equals baud rate in MBaud) |                                                                      |     | 4   | MHz  |

Section 8.12.8.2 lists the UART operating characteristics.

### 8.12.8.2 eUSCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                | TEST CONDITIONS | V <sub>CC</sub> | MIN | MAX | UNIT |
|----------------------------------------------------------|-----------------|-----------------|-----|-----|------|
| t <sub>t</sub> UART receive deglitch time <sup>(1)</sup> | UCGLITx = 0     | 2.2 V, 3.0 V    | 5   | 30  | ns   |
|                                                          | UCGLITx = 1     |                 | 20  | 90  |      |
|                                                          | UCGLITx = 2     |                 | 35  | 160 |      |
|                                                          | UCGLITx = 3     |                 | 50  | 220 |      |

- (1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. Thus the selected deglitch time can limit the maximum useable baud rate. To ensure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.

Section 8.12.8.3 lists the SPI master mode clock frequencies.

### 8.12.8.3 eUSCI (SPI Master Mode) Clock Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                               | TEST CONDITIONS                                        | MIN | MAX | UNIT |
|-----------------------------------------|--------------------------------------------------------|-----|-----|------|
| $f_{eUSCI}$ eUSCI input clock frequency | Internal: SMCLK or ACLK,<br>Duty cycle = 50% $\pm$ 10% |     | 16  | MHz  |

Section 8.12.8.4 lists the SPI master mode operating characteristics.

### 8.12.8.4 eUSCI (SPI Master Mode)

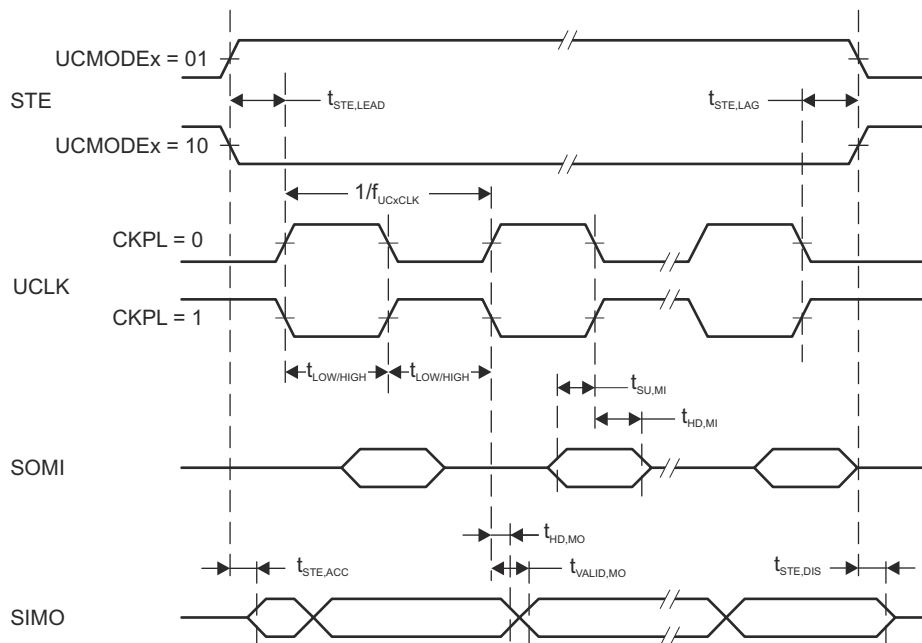
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)<sup>(1)</sup>

| PARAMETER                                                           | TEST CONDITIONS                           | V <sub>CC</sub> | MIN | TYP | MAX | UNIT          |
|---------------------------------------------------------------------|-------------------------------------------|-----------------|-----|-----|-----|---------------|
| $t_{STE,LEAD}$ STE lead time, STE active to clock                   | UCSTEM = 1, UCMODEx = 01 or 10            |                 | 1   |     |     | UCxCLK cycles |
| $t_{STE,LAG}$ STE lag time, Last clock to STE inactive              | UCSTEM = 1, UCMODEx = 01 or 10            |                 | 1   |     |     |               |
| $t_{STE,ACC}$ STE access time, STE active to SIMO data out          | UCSTEM = 0, UCMODEx = 01 or 10            | 2.2 V,<br>3.0 V |     |     | 60  | ns            |
| $t_{STE,DIS}$ STE disable time, STE inactive to SOMI high impedance | UCSTEM = 0, UCMODEx = 01 or 10            | 2.2 V,<br>3.0 V |     |     | 80  | ns            |
| $t_{SU,MI}$ SOMI input data setup time                              |                                           | 2.2 V           | 40  |     |     | ns            |
|                                                                     |                                           | 3.0 V           | 40  |     |     |               |
| $t_{HD,MI}$ SOMI input data hold time                               |                                           | 2.2 V           | 0   |     |     | ns            |
|                                                                     |                                           | 3.0 V           | 0   |     |     |               |
| $t_{VALID,MO}$ SIMO output data valid time <sup>(2)</sup>           | UCLK edge to SIMO valid,<br>$C_L = 20$ pF | 2.2 V           |     |     | 11  | ns            |
|                                                                     |                                           | 3.0 V           |     |     | 10  |               |
| $t_{HD,MO}$ SIMO output data hold time <sup>(3)</sup>               | $C_L = 20$ pF                             | 2.2 V           |     | 0   |     | ns            |
|                                                                     |                                           | 3.0 V           |     | 0   |     |               |

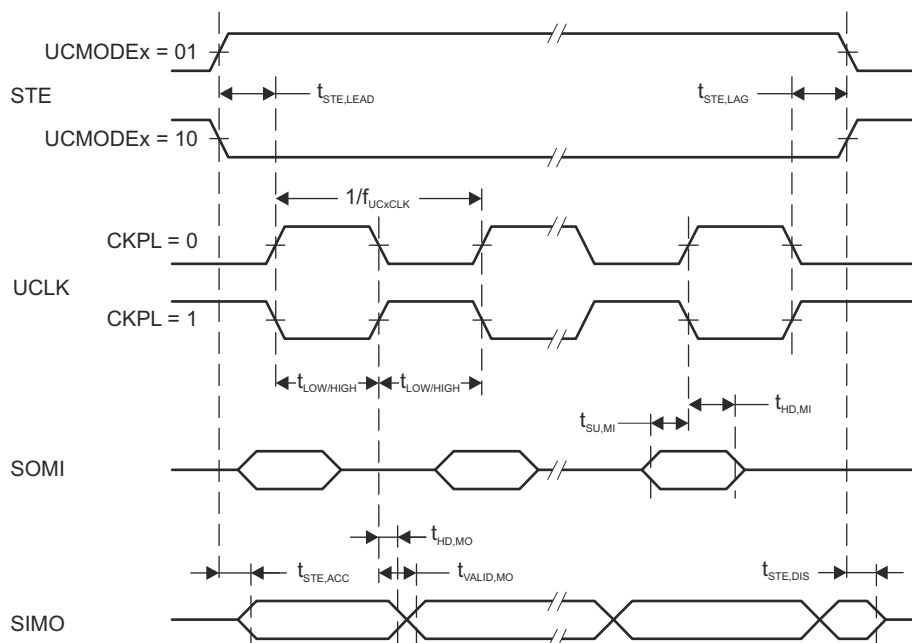
(1)  $f_{UCxCLK} = 1/2 t_{LO/HI}$  with  $t_{LO/HI} = \max(t_{VALID,MO}(eUSCI) + t_{SU,SI}(Slave), t_{SU,MI}(eUSCI) + t_{VALID,SO}(Slave))$

For the slave parameters  $t_{SU,SI}(Slave)$  and  $t_{VALID,SO}(Slave)$ , see the SPI parameters of the attached slave.

- (2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in [Figure 8-14](#) and [Figure 8-15](#).
- (3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in [Figure 8-14](#) and [Figure 8-15](#).



**Figure 8-14. SPI Master Mode, CKPH = 0**



**Figure 8-15. SPI Master Mode, CKPH = 1**

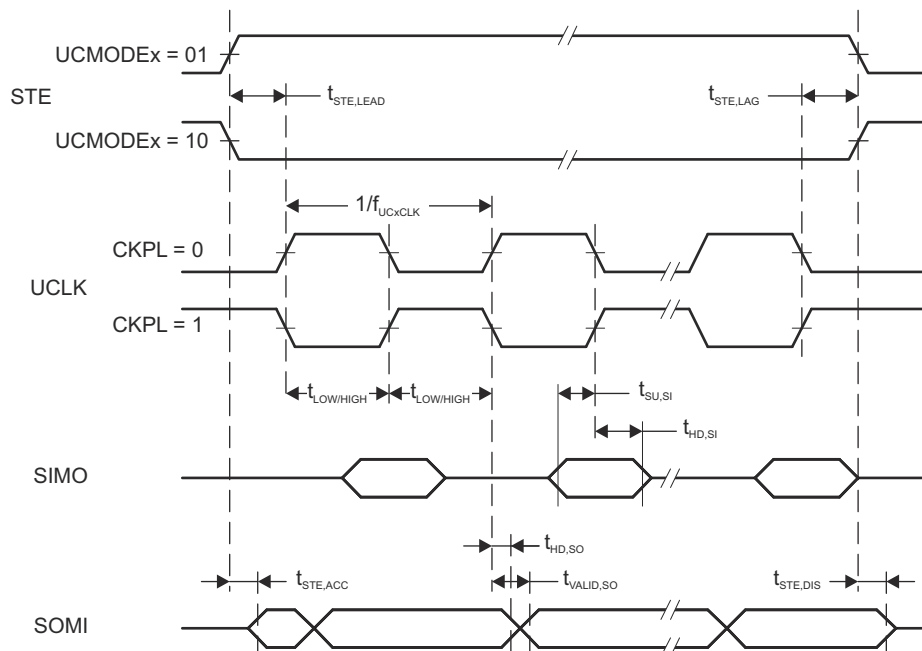
Section 8.12.8.5 lists the SPI slave mode operating characteristics.

#### 8.12.8.5 eUSCI (SPI Slave Mode)

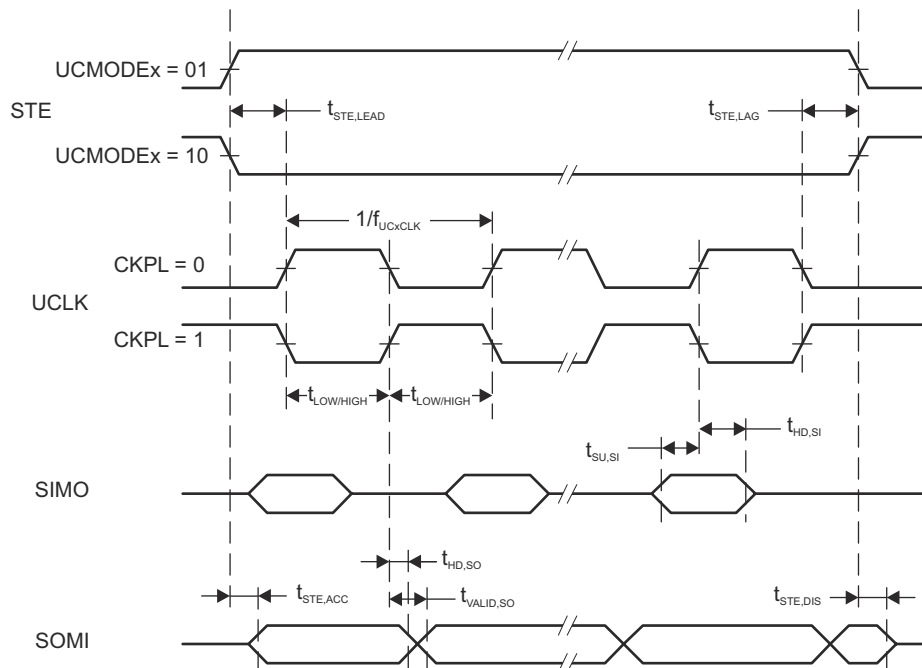
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)<sup>(1)</sup>

| PARAMETER             |                                                       | TEST CONDITIONS                                    | V <sub>CC</sub> | MIN | MAX | UNIT |
|-----------------------|-------------------------------------------------------|----------------------------------------------------|-----------------|-----|-----|------|
| t <sub>STE,LEAD</sub> | STE lead time, STE active to clock                    |                                                    | 2.2 V           | 45  |     | ns   |
|                       |                                                       |                                                    | 3.0 V           | 40  |     |      |
| t <sub>STE,LAG</sub>  | STE lag time, Last clock to STE inactive              |                                                    | 2.2 V           | 2   |     | ns   |
|                       |                                                       |                                                    | 3.0 V           | 3   |     |      |
| t <sub>STE,ACC</sub>  | STE access time, STE active to SOMI data out          |                                                    | 2.2 V           |     | 45  | ns   |
|                       |                                                       |                                                    | 3.0 V           |     | 40  |      |
| t <sub>STE,DIS</sub>  | STE disable time, STE inactive to SOMI high impedance |                                                    | 2.2 V           |     | 50  | ns   |
|                       |                                                       |                                                    | 3.0 V           |     | 45  |      |
| t <sub>SU,SI</sub>    | SIMO input data setup time                            |                                                    | 2.2 V           | 4   |     | ns   |
|                       |                                                       |                                                    | 3.0 V           | 4   |     |      |
| t <sub>HD,SI</sub>    | SIMO input data hold time                             |                                                    | 2.2 V           | 7   |     | ns   |
|                       |                                                       |                                                    | 3.0 V           | 7   |     |      |
| t <sub>VALID,SO</sub> | SOMI output data valid time <sup>(2)</sup>            | UCLK edge to SOMI valid,<br>C <sub>L</sub> = 20 pF | 2.2 V           |     | 35  | ns   |
|                       |                                                       |                                                    | 3.0 V           |     | 35  |      |
| t <sub>HD,SO</sub>    | SOMI output data hold time <sup>(3)</sup>             | C <sub>L</sub> = 20 pF                             | 2.2 V           | 0   |     | ns   |
|                       |                                                       |                                                    | 3.0 V           | 0   |     |      |

- (1)  $f_{\text{UCXCLK}} = 1/2 t_{\text{LO/Hi}}$  with  $t_{\text{LO/Hi}} \geq \max(t_{\text{VALID,MO(Master)}} + t_{\text{SU,SI(eUSCI)}}, t_{\text{SU,MI(Master)}} + t_{\text{VALID,SO(eUSCI)}})$   
For the master parameters  $t_{\text{SU,MI(Master)}}$  and  $t_{\text{VALID,MO(Master)}}$ , see the SPI parameters of the attached master.
- (2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in [Figure 8-16](#) and [Figure 8-17](#).
- (3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in [Figure 8-16](#) and [Figure 8-17](#).



**Figure 8-16. SPI Slave Mode, CKPH = 0**



**Figure 8-17. SPI Slave Mode, CKPH = 1**

Section 8.12.8.6 lists the I<sup>2</sup>C mode operating characteristics.

### 8.12.8.6 eUSCI (I<sup>2</sup>C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 8-18)

| PARAMETER            | TEST CONDITIONS                                                                                     | V <sub>CC</sub>                                          | MIN         | TYP | MAX  | UNIT |
|----------------------|-----------------------------------------------------------------------------------------------------|----------------------------------------------------------|-------------|-----|------|------|
| f <sub>eUSCI</sub>   | eUSCI input clock frequency<br>Internal: SMCLK or ACLK,<br>External: UCLK,<br>Duty cycle = 50% ±10% |                                                          |             |     | 16   | MHz  |
| f <sub>SCL</sub>     | SCL clock frequency                                                                                 | 2.2 V, 3.0 V                                             | 0           |     | 400  | kHz  |
| t <sub>HD,STA</sub>  | Hold time (repeated) START                                                                          | f <sub>SCL</sub> = 100 kHz<br>f <sub>SCL</sub> > 100 kHz | 4.0<br>0.6  |     |      | μs   |
| t <sub>SU,STA</sub>  | Setup time for a repeated START                                                                     | f <sub>SCL</sub> = 100 kHz<br>f <sub>SCL</sub> > 100 kHz | 4.7<br>0.6  |     |      | μs   |
| t <sub>HD,DAT</sub>  | Data hold time                                                                                      | 2.2 V, 3.0 V                                             | 0           |     |      | ns   |
| t <sub>SU,DAT</sub>  | Data setup time                                                                                     | 2.2 V, 3.0 V                                             | 100         |     |      | ns   |
| t <sub>SU,STO</sub>  | Setup time for STOP                                                                                 | f <sub>SCL</sub> = 100 kHz<br>f <sub>SCL</sub> > 100 kHz | 4.0<br>0.6  |     |      | μs   |
| t <sub>SP</sub>      | Pulse duration of spikes suppressed by input filter                                                 | 2.2 V, 3.0 V                                             | UCGLITx = 0 |     | 50   | ns   |
|                      |                                                                                                     |                                                          | UCGLITx = 1 |     | 25   |      |
|                      |                                                                                                     |                                                          | UCGLITx = 2 |     | 12.5 |      |
|                      |                                                                                                     |                                                          | UCGLITx = 3 |     | 6.3  |      |
| t <sub>TIMEOUT</sub> | Clock low time-out                                                                                  | 2.2 V, 3.0 V                                             | UCCLTOx = 1 |     | 27   | ms   |
|                      |                                                                                                     |                                                          | UCCLTOx = 2 |     | 30   |      |
|                      |                                                                                                     |                                                          | UCCLTOx = 3 |     | 33   |      |

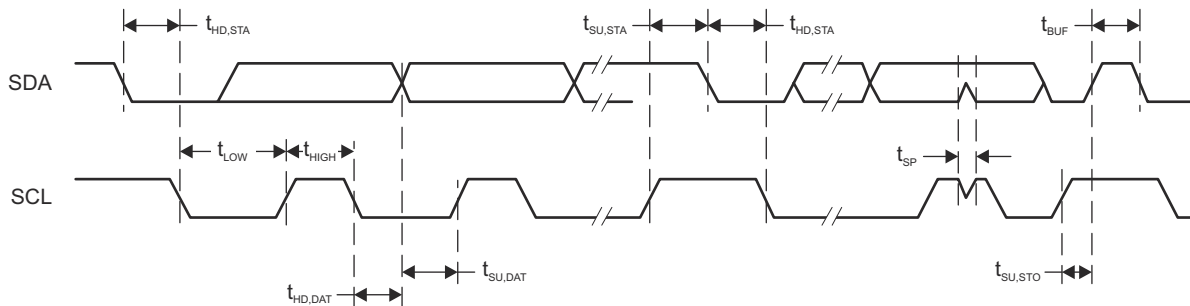


Figure 8-18. I<sup>2</sup>C Mode Timing

## 8.12.9 ADC12\_B

The ADC12\_B module supports fast 12-bit analog-to-digital conversions. The module implements a 12-bit SAR core, sample select control, and up to 32 independent conversion-and-control buffers. The conversion-and-control buffer allows up to 32 independent analog-to-digital converter (ADC) samples to be converted and stored without any CPU intervention.

Section 8.12.9.1 lists the power supply and input range conditions.

### 8.12.9.1 12-Bit ADC, Power Supply and Input Range Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                 |                                                                              | TEST CONDITIONS                                                                                                                | V <sub>CC</sub> | MIN | NOM | MAX  | UNIT |
|-----------------------------------------------------------|------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------|-----------------|-----|-----|------|------|
| V <sub>(Ax)</sub>                                         | Analog input voltage range <sup>(1)</sup>                                    | All ADC12 analog input pins Ax                                                                                                 |                 | 0   |     | AVCC | V    |
| I <sub>(ADC12_B)</sub><br>single-ended<br>mode            | Operating supply current into<br>AVCC plus DVCC terminals <sup>(2)</sup> (3) | f <sub>ADC12CLK</sub> = MODCLK, ADC12ON = 1,<br>ADC12PWRMD = 0, ADC12DIF = 0,<br>REFON = 0, ADC12SHTx = 0,<br>ADC12DIV = 0     | 3.0 V           |     | 145 | 199  | μA   |
|                                                           |                                                                              |                                                                                                                                | 2.2 V           |     | 140 | 190  |      |
| I <sub>(ADC12_B)</sub><br>differential mode               | Operating supply current into<br>AVCC plus DVCC terminals <sup>(2)</sup> (3) | f <sub>ADC12CLK</sub> = MODCLK, ADC12ON = 1,<br>ADC12PWRMD = 0, ADC12DIF = 1,<br>REFON = 0, ADC12SHTx = 0,<br>ADC12DIV = 0     | 3.0 V           |     | 175 | 245  | μA   |
|                                                           |                                                                              |                                                                                                                                | 2.2 V           |     | 170 | 230  |      |
| I <sub>(ADC12_B)</sub><br>single-ended<br>low-power mode  | Operating supply current into<br>AVCC plus DVCC terminals <sup>(2)</sup> (3) | f <sub>ADC12CLK</sub> = MODCLK / 4, ADC12ON = 1,<br>ADC12PWRMD = 1, ADC12DIF = 0,<br>REFON = 0, ADC12SHTx = 0,<br>ADC12DIV = 0 | 3.0 V           |     | 85  | 125  | μA   |
|                                                           |                                                                              |                                                                                                                                | 2.2 V           |     | 83  | 120  |      |
| I <sub>(ADC12_B)</sub><br>differential low-<br>power mode | Operating supply current into<br>AVCC plus DVCC terminals <sup>(2)</sup> (3) | f <sub>ADC12CLK</sub> = MODCLK / 4, ADC12ON = 1,<br>ADC12PWRMD = 1, ADC12DIF = 1,<br>REFON = 0, ADC12SHTx = 0,<br>ADC12DIV = 0 | 3.0 V           |     | 110 | 165  | μA   |
|                                                           |                                                                              |                                                                                                                                | 2.2 V           |     | 109 | 160  |      |
| C <sub>I</sub>                                            | Input capacitance                                                            | Only one terminal Ax can be selected at<br>one time                                                                            | 2.2 V           |     | 10  | 15   | pF   |
| R <sub>I</sub>                                            | Input MUX ON-resistance                                                      | 0 V ≤ V <sub>(Ax)</sub> ≤ AV <sub>CC</sub>                                                                                     | >2 V            |     | 0.5 | 4    | kΩ   |
|                                                           |                                                                              |                                                                                                                                | <2 V            |     | 1   | 10   |      |

(1) The analog input voltage range must be within the selected reference voltage range V<sub>R+</sub> to V<sub>R-</sub> for valid conversion results.

(2) The internal reference supply current is not included in current consumption parameter I<sub>(ADC12\_B)</sub>.

(3) Approximately 60% (typical) of the total current into the AVCC and DVCC terminals is from AVCC.

Section 8.12.9.2 lists the timing parameters.

### 8.12.9.2 12-Bit ADC, Timing Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER             |                                                       | TEST CONDITIONS                                                                                                                                | MIN  | TYP    | MAX | UNIT          |
|-----------------------|-------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------|------|--------|-----|---------------|
| $f_{\text{ADC12CLK}}$ | Frequency for specified performance                   | For specified performance of ADC12 linearity parameters with ADC12PWRMD = 0.<br>If ADC12PWRMD = 1, the maximum is 1/4 of the value shown here. | 0.45 |        | 5.4 | MHz           |
| $f_{\text{ADC12CLK}}$ | Frequency for reduced performance                     | Linearity parameters have reduced performance                                                                                                  |      | 32.768 |     | kHz           |
| $f_{\text{ADC12OSC}}$ | Internal oscillator <sup>(3)</sup>                    | ADC12DIV = 0, $f_{\text{ADC12CLK}} = f_{\text{ADC12OSC}}$ from MODCLK                                                                          | 4    | 4.8    | 5.4 | MHz           |
| $t_{\text{CONVERT}}$  | Conversion time                                       | REFON = 0, Internal oscillator,<br>$f_{\text{ADC12CLK}} = f_{\text{ADC12OSC}}$ from MODCLK, ADC12WINC = 0                                      | 2.6  |        | 3.5 | $\mu\text{s}$ |
|                       |                                                       | External $f_{\text{ADC12CLK}}$ from ACLK, MCLK, or SMCLK,<br>ADC12SSEL $\neq$ 0                                                                |      | (2)    |     |               |
| $t_{\text{ADC12ON}}$  | Turnon settling time of the ADC                       | See (1)                                                                                                                                        |      |        | 100 | ns            |
| $t_{\text{ADC12OFF}}$ | Time ADC must be off before it can be turned on again | $t_{\text{ADC12OFF}}$ must be met to make sure that $t_{\text{ADC12ON}}$ time holds                                                            | 100  |        |     | ns            |
| $t_{\text{Sample}}$   | Sampling time                                         | $R_S = 400\ \Omega$ , $R_I = 4\ \text{k}\Omega$ ,<br>$C_I = 15\ \text{pF}$ , $C_{\text{pext}} = 8\ \text{pF}$ <sup>(4)</sup>                   | 1    |        |     | $\mu\text{s}$ |
|                       |                                                       | Extended sample mode<br>(ADC12SHP = 0) with<br>unbuffered reference<br>(ADC12VRSEL = 0x0, 0x2, 0x4,<br>0x6, 0xC, 0xE)                          | (5)  |        |     |               |

(1) The condition is that the error in a conversion started after  $t_{\text{ADC12ON}}$  is less than  $\pm 0.5$  LSB. The reference and input signal are already settled.

(2)  $14 \times 1 / f_{\text{ADC12CLK}}$ . If ADC12WINC = 1 then  $15 \times 1 / f_{\text{ADC12CLK}}$

(3) The ADC12OSC is sourced directly from MODOSC inside the UCS.

(4) Approximately 10 Tau ( $\tau$ ) are needed to get an error of less than  $\pm 0.5$  LSB:  $t_{\text{sample}} = \ln(2^{n+2}) \times (R_S + R_I) \times (C_I + C_{\text{pext}})$ , where  $n$  = ADC resolution = 12,  $R_S$  = external source resistance,  $C_{\text{pext}}$  = external parasitic capacitance.

(5)  $6 \times 1 / f_{\text{ADC12CLK}}$

Section 8.12.9.3 lists the linearity parameters.

### 8.12.9.3 12-Bit ADC, Linearity Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER      |                                                        | TEST CONDITIONS                                                                                                                                            | MIN   | TYP   | MAX   | UNIT |
|----------------|--------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|-------|-------|------|
| E <sub>I</sub> | Integral linearity error (INL) for differential input  | With external voltage reference (ADC12VRSEL = 0x2, 0x3, 0x4, 0x14, 0x15), 1.2 V ≤ (V <sub>R+</sub> – V <sub>R-</sub> ) ≤ AV <sub>CC</sub>                  |       |       | ±1.8  | LSB  |
|                | Integral linearity error (INL) for single-ended inputs |                                                                                                                                                            |       |       | ±2.2  |      |
| E <sub>D</sub> | Differential linearity error (DNL)                     | With external voltage reference (ADC12VRSEL = 0x2, 0x3, 0x4, 0x14, 0x15)                                                                                   | -0.99 |       | +1.0  | LSB  |
| E <sub>O</sub> | Offset error <sup>(1) (2)</sup>                        | ADC12VRSEL = 0x1 without TLV calibration, TLV calibration data can be used to improve the parameter <sup>(3)</sup>                                         |       | ±0.5  | ±1.5  | mV   |
| E <sub>G</sub> | Gain error                                             | With internal voltage reference VREF = 2.5 V (ADC12VRSEL = 0x1, 0x7, 0x9, 0xB, or 0xD)                                                                     |       | ±0.2% | ±1.7% | LSB  |
|                |                                                        | With internal voltage reference VREF = 1.2 V (ADC12VRSEL = 0x1, 0x7, 0x9, 0xB, or 0xD)                                                                     |       | ±0.2% | ±2.5% |      |
|                |                                                        | With external voltage reference without internal buffer (ADC12VRSEL = 0x2 or 0x4) without TLV calibration, V <sub>R+</sub> = 2.5 V, V <sub>R-</sub> = AVSS |       | ±1    | ±3    |      |
|                |                                                        | With external voltage reference with internal buffer (ADC12VRSEL = 0x3), V <sub>R+</sub> = 2.5 V, V <sub>R-</sub> = AVSS                                   |       | ±2    | ±27   |      |
| E <sub>T</sub> | Total unadjusted error                                 | With internal voltage reference VREF = 2.5 V (ADC12VRSEL = 0x1, 0x7, 0x9, 0xB, or 0xD)                                                                     |       | ±0.2% | ±1.8% | LSB  |
|                |                                                        | With internal voltage reference VREF = 1.2 V (ADC12VRSEL = 0x1, 0x7, 0x9, 0xB, or 0xD)                                                                     |       | ±0.2% | ±2.6% |      |
|                |                                                        | With external voltage reference without internal buffer (ADC12VRSEL = 0x2 or 0x4) without TLV calibration, V <sub>R+</sub> = 2.5 V, V <sub>R-</sub> = AVSS |       | ±1    | ±5    |      |
|                |                                                        | With external voltage reference with internal buffer (ADC12VRSEL = 0x3), V <sub>R+</sub> = 2.5 V, V <sub>R-</sub> = AVSS                                   |       | ±1    | ±28   |      |

(1) Offset is measured as the input voltage (at which ADC output transitions from 0 to 1) minus 0.5 LSB.

(2) Offset increases as I<sub>R</sub> drop increases when V<sub>R-</sub> is AVSS.

(3) For details, see the *Device Descriptor Table* section in the [MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide](#).

### 8.12.9.4 12-Bit ADC, Dynamic Performance With External Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER  |                                                                                     | TEST CONDITIONS                                                                                                            | MIN | TYP  | MAX | UNIT |
|------------|-------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------|-----|------|-----|------|
| Resolution | Number of no missing code output-code bits                                          |                                                                                                                            | 12  |      |     | bits |
| SNR        | Signal-to-noise with differential inputs                                            | V <sub>R+</sub> = 2.5 V, V <sub>R-</sub> = AVSS                                                                            |     | 71   |     | dB   |
|            | Signal-to-noise with single-ended inputs                                            | V <sub>R+</sub> = 2.5 V, V <sub>R-</sub> = AVSS                                                                            |     | 70   |     |      |
| ENOB       | Effective number of bits with differential inputs <sup>(1)</sup>                    | V <sub>R+</sub> = 2.5 V, V <sub>R-</sub> = AVSS                                                                            |     | 11.4 |     | bits |
|            | Effective number of bits with single-ended inputs <sup>(1)</sup>                    | V <sub>R+</sub> = 2.5 V, V <sub>R-</sub> = AVSS                                                                            |     | 11.1 |     |      |
|            | Effective number of bits with 32.768-kHz clock (reduced performance) <sup>(1)</sup> | Reduced performance with f <sub>ADC12CLK</sub> from ACLK, LFXT 32.768 kHz, V <sub>R+</sub> = 2.5 V, V <sub>R-</sub> = AVSS |     | 10.9 |     |      |

(1) ENOB = (SINAD – 1.76) / 6.02

Section 8.12.9.5 lists the dynamic performance characteristics when using an internal reference.

#### 8.12.9.5 12-Bit ADC, Dynamic Performance With Internal Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER  |                                                                                     | TEST CONDITIONS                                                                                                 | MIN | TYP  | MAX | UNIT |
|------------|-------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------|-----|------|-----|------|
| Resolution | Number of no missing code output code bits                                          |                                                                                                                 | 12  |      |     | bits |
| SNR        | Signal-to-noise with differential inputs                                            | $V_{R+} = 2.5\text{ V}$ , $V_{R-} = AV_{SS}$                                                                    |     | 70   |     | dB   |
|            | Signal-to-noise with single-ended inputs                                            | $V_{R+} = 2.5\text{ V}$ , $V_{R-} = AV_{SS}$                                                                    |     | 69   |     |      |
| ENOB       | Effective number of bits with differential inputs <sup>(1)</sup>                    | $V_{R+} = 2.5\text{ V}$ , $V_{R-} = AV_{SS}$                                                                    |     | 11.4 |     | bits |
|            | Effective number of bits with single-ended inputs <sup>(1)</sup>                    | $V_{R+} = 2.5\text{ V}$ , $V_{R-} = AV_{SS}$                                                                    |     | 11.0 |     |      |
|            | Effective number of bits with 32.768-kHz clock (reduced performance) <sup>(1)</sup> | Reduced performance with $f_{ADC12CLK}$ from ACLK LFXT 32.768 kHz, $V_{R+} = 2.5\text{ V}$ , $V_{R-} = AV_{SS}$ |     | 10.9 |     |      |

(1)  $ENOB = (SINAD - 1.76) / 6.02$

Section 8.12.9.6 lists the temperature sensor and built-in  $V_{1/2}$  characteristics.

#### 8.12.9.6 12-Bit ADC, Temperature Sensor and Built-In $V_{1/2}$

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER             |                                                                                       | TEST CONDITIONS                                                             | MIN   | TYP | MAX   | UNIT                 |
|-----------------------|---------------------------------------------------------------------------------------|-----------------------------------------------------------------------------|-------|-----|-------|----------------------|
| $V_{SENSOR}$          | Temperature sensor voltage <sup>(1) (2)</sup> (see Figure 8-19)                       | ADC12ON = 1, ADC12TCMAP = 1, $T_A = 0^\circ\text{C}$                        |       | 700 |       | mV                   |
| $TC_{SENSOR}$         | See <sup>(2)</sup>                                                                    | ADC12ON = 1, ADC12TCMAP = 1                                                 |       | 2.5 |       | mV/ $^\circ\text{C}$ |
| $t_{SENSOR(sample)}$  | Sample time required if ADCTCMAP = 1 and channel (MAX – 1) is selected <sup>(3)</sup> | ADC12ON = 1, ADC12TCMAP = 1, Error of conversion result $\leq 1\text{ LSB}$ | 30    |     |       | $\mu\text{s}$        |
| $V_{1/2}$             | AVCC voltage divider for ADC12BATMAP = 1 on MAX input channel                         | ADC12ON = 1, ADC12BATMAP = 1                                                | 47.5% | 50% | 52.5% |                      |
| $I_{V\ 1/2}$          | Current for battery monitor during sample time                                        | ADC12ON = 1, ADC12BATMAP = 1                                                |       | 38  | 72    | $\mu\text{A}$        |
| $t_{V\ 1/2 (sample)}$ | Sample time required if ADC12BATMAP = 1 and channel MAX is selected <sup>(4)</sup>    | ADC12ON = 1, ADC12BATMAP = 1                                                | 1.7   |     |       | $\mu\text{s}$        |

- (1) The temperature sensor offset can be as much as  $\pm 30^\circ\text{C}$ . TI recommends a single-point calibration to minimize the offset error of the built-in temperature sensor.
- (2) The device descriptor structure contains calibration values for  $30^\circ\text{C} \pm 3^\circ\text{C}$  and  $85^\circ\text{C} \pm 3^\circ\text{C}$  for each of the available reference voltage levels. The sensor voltage can be computed as  $V_{SENSE} = TC_{SENSOR} \times (\text{Temperature}, ^\circ\text{C}) + V_{SENSOR}$ , where  $TC_{SENSOR}$  and  $V_{SENSOR}$  can be computed from the calibration values for higher accuracy.
- (3) The typical equivalent impedance of the sensor is 250 k $\Omega$ . The sample time required includes the sensor on time ( $t_{SENSOR(on)}$ ).
- (4) The on time ( $t_{V1/2(on)}$ ) is included in the sampling time ( $t_{V1/2(sample)}$ ); no additional on time is needed.

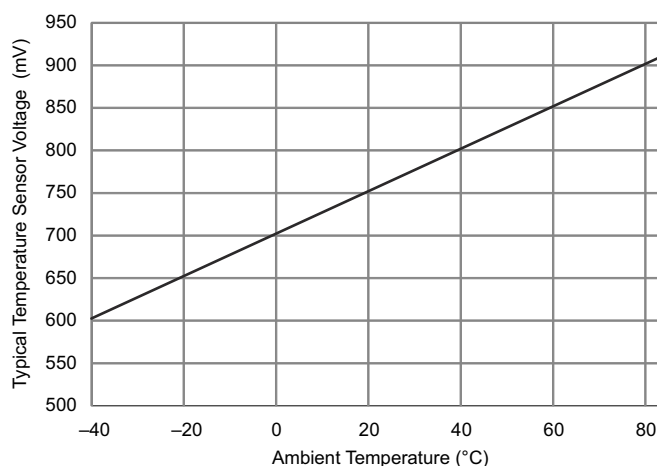


Figure 8-19. Typical Temperature Sensor Voltage

Section 8.12.9.7 lists the external reference characteristics.

#### 8.12.9.7 12-Bit ADC, External Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)<sup>(1)</sup>

| PARAMETER                      |                                                                                              | TEST CONDITIONS                                                                                                                                                    | MIN | MAX       | UNIT          |
|--------------------------------|----------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----------|---------------|
| $V_{R+}$                       | Positive external reference voltage input $V_{eREF+}$ or $V_{eREF-}$ based on ADC12VRSEL bit | $V_{R+} > V_{R-}$                                                                                                                                                  | 1.2 | $AV_{CC}$ | V             |
| $V_{R-}$                       | Negative external reference voltage input $V_{eREF+}$ or $V_{eREF-}$ based on ADC12VRSEL bit | $V_{R+} > V_{R-}$                                                                                                                                                  | 0   | 1.2       | V             |
| $V_{R+} - V_{R-}$              | Differential external reference voltage input                                                | $V_{R+} > V_{R-}$                                                                                                                                                  | 1.2 | $AV_{CC}$ | V             |
| $I_{VeREF+}$ ,<br>$I_{VeREF-}$ | Static input current singled-ended input mode                                                | $1.2\text{ V} \leq V_{eREF+} \leq V_{AVCC}$ , $V_{eREF-} = 0\text{ V}$<br>$f_{ADC12CLK} = 5\text{ MHz}$ , $ADC12SHTx = 1h$ ,<br>$ADC12DIF = 0$ , $ADC12PWRMD = 0$  |     | $\pm 10$  | $\mu\text{A}$ |
|                                |                                                                                              | $1.2\text{ V} \leq V_{eREF+} \leq V_{AVCC}$ , $V_{eREF-} = 0\text{ V}$<br>$f_{ADC12CLK} = 5\text{ MHz}$ , $ADC12SHTx = 8h$ ,<br>$ADC12DIF = 0$ , $ADC12PWRMD = 01$ |     | $\pm 2.5$ |               |
| $I_{VeREF+}$ ,<br>$I_{VeREF-}$ | Static input current differential input mode                                                 | $1.2\text{ V} \leq V_{eREF+} \leq V_{AVCC}$ , $V_{eREF-} = 0\text{ V}$<br>$f_{ADC12CLK} = 5\text{ MHz}$ , $ADC12SHTx = 1h$ ,<br>$ADC12DIF = 1$ , $ADC12PWRMD = 0$  |     | $\pm 20$  | $\mu\text{A}$ |
|                                |                                                                                              | $1.2\text{ V} \leq V_{eREF+} \leq V_{AVCC}$ , $V_{eREF-} = 0\text{ V}$<br>$f_{ADC12CLK} = 5\text{ MHz}$ , $ADC12SHTx = 8h$ ,<br>$ADC12DIF = 1$ , $ADC12PWRMD = 1$  |     | $\pm 5$   |               |
| $I_{VeREF+}$                   | Peak input current with single-ended input                                                   | $0\text{ V} \leq V_{eREF+} \leq V_{AVCC}$ , $ADC12DIF = 0$                                                                                                         |     | 1.5       | mA            |
| $I_{VeREF+}$                   | Peak input current with differential input                                                   | $0\text{ V} \leq V_{eREF+} \leq V_{AVCC}$ , $ADC12DIF = 1$                                                                                                         |     | 3         | mA            |
| $C_{VeREF+/-}$                 | Capacitance at $V_{eREF+}$ or $V_{eREF-}$ terminal                                           | See <sup>(2)</sup>                                                                                                                                                 | 10  |           | $\mu\text{F}$ |

- (1) The external reference is used during ADC conversion to charge and discharge the capacitance array. The input capacitance,  $C_i$ , is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.
- (2) Two decoupling capacitors, 10  $\mu\text{F}$  and 470 nF, should be connected to  $V_{eREF}$  to decouple the dynamic current required for an external reference source if it is used for the ADC12\_B. Also see the [MSP430FR58xx](#), [MSP430FR59xx](#), [MSP430FR68xx](#), and [MSP430FR69xx Family User's Guide](#).

## 8.12.10 Reference

The reference module (REF) generates all of the critical reference voltages that can be used by various analog peripherals in a given device. The heart of the reference system is the bandgap from which all other references are derived by unity or noninverting gain stages. The REFGEN subsystem consists of the bandgap, the bandgap bias, and the noninverting buffer stage, which generates the three primary voltage reference available in the system (1.2 V, 2.0 V, and 2.5 V).

Section 8.12.10.1 lists the operating characteristics of the built-in reference.

### 8.12.10.1 REF, Built-In Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                 | TEST CONDITIONS                                            | V <sub>CC</sub>                                                                                                                                        | MIN | TYP       | MAX  | UNIT  |
|-------------------------------------------|------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----------|------|-------|
| V <sub>REF+</sub>                         | REFVSEL = {2} for 2.5 V, REFON = 1                         | 2.7 V                                                                                                                                                  |     | 2.5 ±1.5% |      | V     |
|                                           | REFVSEL = {1} for 2.0 V, REFON = 1                         | 2.2 V                                                                                                                                                  |     | 2.0 ±1.5% |      |       |
|                                           | REFVSEL = {0} for 1.2 V, REFON = 1                         | 1.8 V                                                                                                                                                  |     | 1.2 ±1.8% |      |       |
| Noise                                     | RMS noise at VREF <sup>(1)</sup>                           | From 0.1 Hz to 10 Hz, REFVSEL = {0}                                                                                                                    |     | 30        | 130  | μV    |
| V <sub>OS_BUF_INT</sub>                   | VREF ADC BUF_INT buffer offset <sup>(3)</sup>              | T <sub>A</sub> = 25°C, ADC on, REFVSEL = {0}, REFON = 1, REFOUT = 0                                                                                    |     | –16       | +16  | mV    |
| V <sub>OS_BUF_EXT</sub>                   | VREF ADC BUF_EXT buffer offset <sup>(2)</sup>              | T <sub>A</sub> = 25°C, REFVSEL = {0}, REFOUT = 1, REFON = 1 or ADC on                                                                                  |     | –16       | +16  | mV    |
| AV <sub>CC(min)</sub>                     | REFVSEL = {0} for 1.2 V                                    |                                                                                                                                                        |     | 1.8       |      | V     |
|                                           | REFVSEL = {1} for 2.0 V                                    |                                                                                                                                                        |     | 2.2       |      |       |
|                                           | REFVSEL = {2} for 2.5 V                                    |                                                                                                                                                        |     | 2.7       |      |       |
| I <sub>REF+</sub>                         | Operating supply current into AVCC terminal <sup>(4)</sup> | REFON = 1                                                                                                                                              | 3 V | 19        | 26   | μA    |
| I <sub>REF+_ADC_BUF</sub>                 | ADC on, REFOUT = 0, REFVSEL = {0, 1, 2}, ADC12PWRMD = 0,   | 3 V                                                                                                                                                    |     | 247       | 400  | μA    |
|                                           | ADC on, REFOUT = 1, REFVSEL = {0, 1, 2}, ADC12PWRMD = 0    |                                                                                                                                                        |     | 1053      | 1820 |       |
|                                           | ADC on, REFOUT = 0, REFVSEL = {0, 1, 2}, ADC12PWRMD = 1    |                                                                                                                                                        |     | 153       | 240  |       |
|                                           | ADC on, REFOUT = 1, REFVSEL = {0, 1, 2}, ADC12PWRMD = 1    |                                                                                                                                                        |     | 581       | 1030 |       |
|                                           | ADC OFF, REFON = 1, REFOUT = 1, REFVSEL = {0, 1, 2}        |                                                                                                                                                        |     | 1105      | 1890 |       |
| I <sub>O(VREF+)</sub>                     | VREF maximum load current, VREF+ terminal                  | REFVSEL = {0, 1, 2}, AV <sub>CC</sub> = AV <sub>CC(min)</sub> for each reference level, REFON = REFOUT = 1                                             |     | –1000     | 10   | μA    |
| ΔV <sub>out</sub> /ΔI <sub>O(VREF+)</sub> | Load-current regulation, VREF+ terminal                    | REFVSEL = {0, 1, 2}, I <sub>O(VREF+)</sub> = +10 μA or –1000 μA, AV <sub>CC</sub> = AV <sub>CC(min)</sub> for each reference level, REFON = REFOUT = 1 |     |           | 1500 | μV/mA |
| C <sub>VREF+/-</sub>                      | Capacitance at VREF+ and VREF- terminals                   | REFON = REFOUT = 1                                                                                                                                     |     | 0         | 100  | pF    |
| TC <sub>REF+</sub>                        | Temperature coefficient of built-in reference              | REFVSEL = {0, 1, 2}, REFON = REFOUT = 1, T <sub>A</sub> = –40°C to 85°C <sup>(5)</sup>                                                                 |     | 24        | 50   | ppm/K |
| PSRR <sub>DC</sub>                        | Power supply rejection ratio (DC)                          | AV <sub>CC</sub> = AV <sub>CC(min)</sub> to AV <sub>CC(max)</sub> , T <sub>A</sub> = 25°C, REFVSEL = {0, 1, 2}, REFON = REFOUT = 1                     |     | 100       | 400  | μV/V  |
| PSRR <sub>AC</sub>                        | Power supply rejection ratio (AC)                          | dAV <sub>CC</sub> = 0.1 V at 1 kHz                                                                                                                     |     | 3.0       |      | mV/V  |
| t <sub>SETTLE</sub>                       | Settling time of reference voltage <sup>(6)</sup>          | AV <sub>CC</sub> = AV <sub>CC(min)</sub> to AV <sub>CC(max)</sub> , REFVSEL = {0, 1, 2}, REFON = 0 → 1                                                 |     | 40        | 80   | μs    |

### 8.12.10.1 REF, Built-In Reference (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER               | TEST CONDITIONS                                              | V <sub>CC</sub>                                                                                                                                                    | MIN | TYP | MAX | UNIT |
|-------------------------|--------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|------|
| T <sub>buf_settle</sub> | Settling time of ADC reference voltage buffer <sup>(6)</sup> | AV <sub>CC</sub> = AV <sub>CC(min)</sub> to AV <sub>CC(max)</sub> ,<br>REFVSEL = {0, 1, 2}, REFON = 1 (internal note should be for buf_int REFOUT=0 or buf_ext=1 ) |     | 0.4 | 2   | μs   |

- (1) Internal reference noise affects ADC performance when ADC uses internal reference. See [Designing With the MSP430FR58xx, FR59xx, FR68xx, and FR69xx ADC](#) for details on optimizing ADC performance for your application with the choice of internal or external reference.
- (2) Buffer offset affects ADC gain error and thus total unadjusted error.
- (3) Buffer offset affects ADC gain error and thus total unadjusted error.
- (4) The internal reference current is supplied through the AV<sub>CC</sub> terminal.
- (5) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C)/(85°C – (–40°C)).
- (6) The condition is that the error in a conversion started after t<sub>REFON</sub> is less than ±0.5 LSB.

### 8.12.11 Comparator

The COMP\_E module supports precision slope analog-to-digital conversions, supply voltage supervision, and monitoring of external analog signals. [Section 8.12.11.1](#) lists the comparator characteristics.

#### 8.12.11.1 Comparator\_E

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                  | TEST CONDITIONS                                                         | V <sub>CC</sub> | MIN   | TYP                 | MAX   | UNIT |
|----------------------------|-------------------------------------------------------------------------|-----------------|-------|---------------------|-------|------|
| I <sub>AVCC_COMP</sub>     | CEPWRMD = 00, CEON = 1, CERSx = 00 (fast)                               | 2.2 V, 3.0 V    |       | 12                  | 16    | μA   |
|                            | CEPWRMD = 01, CEON = 1, CERSx = 00 (medium)                             |                 |       | 10                  | 14    |      |
|                            | CEPWRMD = 10, CEON = 1, CERSx = 00 (slow), T <sub>A</sub> = 30°C        |                 |       | 0.1                 | 0.3   |      |
|                            | CEPWRMD = 10, CEON = 1, CERSx = 00 (slow), T <sub>A</sub> = 85°C        |                 |       | 0.3                 | 1.3   |      |
| I <sub>AVCC_COMP_REF</sub> | CEPWRMD = 10, CEREF <sub>Lx</sub> = 01, CERSx = 10, CEON = 1, REFON = 0 | 2.2 V, 3.0 V    |       | 31                  | 38    | μA   |
|                            | CEREFACC = 0                                                            |                 |       | 16                  | 19    |      |
| V <sub>REF</sub>           | CERSx = 11, CEREF <sub>Lx</sub> = 01, CEREFACC = 0                      | 1.8 V           | 1.152 | 1.2                 | 1.248 | V    |
|                            | CERSx = 11, CEREF <sub>Lx</sub> = 10, CEREFACC = 0                      | 2.2 V           | 1.92  | 2.0                 | 2.08  |      |
|                            | CERSx = 11, CEREF <sub>Lx</sub> = 11, CEREFACC = 0                      | 2.7 V           | 2.40  | 2.5                 | 2.60  |      |
|                            | CERSx = 11, CEREF <sub>Lx</sub> = 01, CEREFACC = 1                      | 1.8 V           | 1.10  | 1.2                 | 1.245 |      |
|                            | CERSx = 11, CEREF <sub>Lx</sub> = 10, CEREFACC = 1                      | 2.2 V           | 1.90  | 2.0                 | 2.08  |      |
|                            | CERSx = 11, CEREF <sub>Lx</sub> = 11, CEREFACC = 1                      | 2.7 V           | 2.35  | 2.5                 | 2.60  |      |
| V <sub>IC</sub>            | Common mode input range                                                 |                 | 0     | V <sub>CC</sub> – 1 |       | V    |
| V <sub>OFFSET</sub>        | CEPWRMD = 00                                                            |                 | –16   |                     | 16    | mV   |
|                            | CEPWRMD = 01                                                            |                 | –12   |                     | 12    |      |
|                            | CEPWRMD = 10                                                            |                 | –37   |                     | 37    |      |
| C <sub>IN</sub>            | CEPWRMD = 00 or CEPWRMD = 01                                            |                 |       | 10                  |       | pF   |
|                            | CEPWRMD = 10                                                            |                 |       | 10                  |       |      |

### 8.12.11.1 Comparator\_E (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                                                  | TEST CONDITIONS                                                                                                                  | V <sub>CC</sub> | MIN                                  | TYP                                | MAX                                  | UNIT |
|--------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------|-----------------|--------------------------------------|------------------------------------|--------------------------------------|------|
| R <sub>SIN</sub> Series input resistance                                                   | On (switch closed)                                                                                                               |                 |                                      | 1                                  | 3                                    | kΩ   |
|                                                                                            | Off (switch open)                                                                                                                |                 | 50                                   |                                    |                                      | MΩ   |
| t <sub>PD</sub> Propagation delay, response time                                           | CEF = 0, Overdrive ≥ 20 mV                                                                                                       |                 |                                      | 193                                | 330                                  | ns   |
|                                                                                            |                                                                                                                                  |                 |                                      | 230                                | 400                                  |      |
|                                                                                            |                                                                                                                                  |                 |                                      | 5                                  | 15                                   | μs   |
| t <sub>PD,filter</sub> Propagation delay with filter active                                | CEPWRMD = 00 or 01, CEF = 1, Overdrive ≥ 20 mV                                                                                   |                 |                                      | 700                                | 1000                                 | ns   |
|                                                                                            |                                                                                                                                  |                 |                                      | 1.0                                | 1.9                                  | μs   |
|                                                                                            |                                                                                                                                  |                 |                                      | 2.0                                | 3.7                                  |      |
|                                                                                            |                                                                                                                                  |                 |                                      | 4.0                                | 7.7                                  |      |
| t <sub>EN_CMP</sub> Comparator enable time                                                 | CEON = 0 → 1, V <sub>IN+</sub> and V <sub>IN-</sub> from pins, Overdrive ≥ 20 mV                                                 |                 |                                      | 0.9                                | 1.5                                  | μs   |
|                                                                                            |                                                                                                                                  |                 |                                      | 0.9                                | 1.5                                  |      |
|                                                                                            |                                                                                                                                  |                 |                                      | 15                                 | 65                                   |      |
| t <sub>EN_CMP_VREF</sub> Comparator and reference ladder and reference voltage enable time | CEON = 0 → 1, CEREF <sub>FLX</sub> = 10, CERS <sub>x</sub> = 10 or 11, CEREF <sub>0</sub> = CEREF <sub>1</sub> = 0x0F, REFON = 0 |                 |                                      | 120                                | 220                                  | μs   |
| t <sub>EN_CMP_RL</sub> Comparator and reference ladder enable time                         | CEON = 0 → 1, CEREF <sub>FLX</sub> = 10, CERS <sub>x</sub> = 10, REFON = 1, CEREF <sub>0</sub> = CEREF <sub>1</sub> = 0x0F       |                 |                                      | 10                                 | 30                                   | μs   |
| V <sub>CE_REF</sub> Reference voltage for a given tap                                      | VIN = reference into resistor ladder (n = 0 to 31)                                                                               |                 | $\frac{V_{IN} \times (n + 0.5)}{32}$ | $\frac{V_{IN} \times (n + 1)}{32}$ | $\frac{V_{IN} \times (n + 1.5)}{32}$ | V    |

### 8.12.12 FRAM

FRAM is a nonvolatile memory that reads and writes like standard SRAM. The FRAM can be read in a similar fashion to SRAM and needs no special requirements. Similarly, any writes to unprotected segments can be written in the same fashion as SRAM.

Section 8.12.12.1 lists the operating characteristics of the FRAM.

#### 8.12.12.1 FRAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                      | TEST CONDITIONS         | MIN              | TYP                                    | MAX | UNIT   |
|------------------------------------------------|-------------------------|------------------|----------------------------------------|-----|--------|
| Read and write endurance                       |                         | 10 <sup>15</sup> |                                        |     | cycles |
| t <sub>Retention</sub> Data retention duration | T <sub>J</sub> = 25°C   | 100              |                                        |     | years  |
|                                                | T <sub>J</sub> = 70°C   | 40               |                                        |     |        |
|                                                | T <sub>J</sub> = 85°C   | 10               |                                        |     |        |
| I <sub>WRITE</sub> Current to write into FRAM  |                         |                  | I <sub>READ</sub> <sup>(1)</sup>       |     | nA     |
| I <sub>ERASE</sub> Erase current               |                         |                  | n/a <sup>(2)</sup>                     |     | nA     |
| t <sub>WRITE</sub> Write time                  |                         |                  | t <sub>READ</sub> <sup>(3)</sup>       |     | ns     |
| t <sub>READ</sub> Read time                    | NWAITS <sub>x</sub> = 0 |                  | 1 / f <sub>SYSTEM</sub> <sup>(4)</sup> |     | ns     |
|                                                | NWAITS <sub>x</sub> = 1 |                  | 2 / f <sub>SYSTEM</sub> <sup>(4)</sup> |     |        |

(1) Writing to FRAM does not require a setup sequence or additional power when compared to reading from FRAM. The FRAM read current (I<sub>READ</sub>) is included in the active mode current consumption, I<sub>AM,FRAM</sub>.

(2) FRAM does not require a special erase sequence.

(3) Writing into FRAM is as fast as reading.

(4) The maximum read (and write) speed is specified by f<sub>SYSTEM</sub> using the appropriate wait state settings (NWAITS<sub>x</sub>).

### 8.12.13 Emulation and Debug

The MSP family supports the standard JTAG interface, which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/Os. The TEST/SBWTCK pin is used to enable the connection of external development tools with the device through Spy-Bi-Wire or JTAG debug protocols. The connection is usually enabled when the TEST/SBWTCK is high. When the connection is enabled, the device enters a debug mode. In the debug mode, the times for entry to and wake up from low-power modes may be different compared to normal operation. Pay careful attention to the real-time behavior when using low-power modes with the device connected to a development tool.

Section 8.12.13.1 lists the JTAG and Spy-Bi-Wire interface characteristics.

#### 8.12.13.1 JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                       |                                                                                                                             | V <sub>CC</sub> | MIN  | TYP | MAX | UNIT |
|---------------------------------|-----------------------------------------------------------------------------------------------------------------------------|-----------------|------|-----|-----|------|
| I <sub>JTAG</sub>               | Supply current adder when JTAG active (but not clocked)                                                                     | 2.2 V, 3.0 V    |      | 40  | 100 | μA   |
| f <sub>SBW</sub>                | Spy-Bi-Wire input frequency                                                                                                 | 2.2 V, 3.0 V    | 0    |     | 10  | MHz  |
| t <sub>SBW,Low</sub>            | Spy-Bi-Wire low clock pulse duration                                                                                        | 2.2 V, 3.0 V    | 0.04 |     | 15  | μs   |
| t <sub>SBW,En</sub>             | Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge) <sup>(1)</sup>                                        | 2.2 V, 3.0 V    |      |     | 110 | μs   |
| t <sub>SBW,Rst</sub>            | Spy-Bi-Wire return to normal operation time                                                                                 |                 | 15   |     | 100 | μs   |
| f <sub>TCK</sub>                | TCK input frequency, 4-wire JTAG <sup>(2)</sup>                                                                             | 2.2 V           | 0    |     | 16  | MHz  |
|                                 |                                                                                                                             | 3.0 V           | 0    |     | 16  |      |
| R <sub>internal</sub>           | Internal pulldown resistance on TEST                                                                                        | 2.2 V, 3.0 V    | 20   | 35  | 50  | kΩ   |
| f <sub>TCLK</sub>               | TCLK and MCLK frequency during JTAG access, no FRAM access (limited by f <sub>SYSTEM</sub> )                                |                 |      |     | 16  | MHz  |
| t <sub>TCLK,Low/High</sub>      | TCLK low or high clock pulse duration, no FRAM access                                                                       |                 |      |     | 25  | ns   |
| f <sub>TCLK,FRAM</sub>          | TCLK and MCLK frequency during JTAG access, including FRAM access (limited by f <sub>SYSTEM</sub> with no FRAM wait states) |                 |      |     | 4   | MHz  |
| t <sub>TCLK,FRAM,Low/High</sub> | TCLK low or high clock pulse duration, including FRAM accesses                                                              |                 |      |     | 100 | ns   |

- (1) Tools that access the Spy-Bi-Wire and the BSL interfaces must wait for the t<sub>SBW,En</sub> time after the first transition of the TEST/SBWTCK pin (low to high), before the second transition of the pin (high to low) during the entry sequence.
- (2) f<sub>TCK</sub> may be restricted to meet the timing requirements of the module selected.

## 9 Detailed Description

### 9.1 Overview

The TI MSP430FR59xx family of ultra-low-power microcontrollers consists of several devices featuring different sets of peripherals. The architecture, combined with seven low-power modes, is optimized to achieve extended battery life for example in portable measurement applications. The devices features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency.

The device is an MSP430FR59xx family device with Low-Energy Accelerator (LEA) (available only on the MSP430FR599x MCUs), up to six 16-bit timers, up to eight eUSCs that support UART, SPI, and I<sup>2</sup>C, a comparator, a hardware multiplier, an AES accelerator, a 6-channel DMA, an RTC module with alarm capabilities, up to 67 I/O pins, and a high-performance 12-bit ADC.

### 9.2 CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses. The peripherals can be managed with all instructions.

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data.

### 9.3 Low-Energy Accelerator (LEA) for Signal Processing (MSP430FR599x Only)

The LEA module is a hardware engine designed for operations that involve vector-based signal processing, such as FIR, IIR, and FFT. The subsystem offers fast performance and low energy consumption when performing vector-based digital signal processing computations; for performance benchmarks comparing the LEA module to using the CPU or other processors, see [Benchmarking the Signal Processing Capabilities of the Low-Energy Accelerator on MSP MCUs](#).

The LEA module requires MCLK to be operational; therefore, the subsystem can run only in active mode or LPM0 (see [Table 9-1](#)). While the LEA module is running, the LEA data operations are performed on a shared 4KB of RAM out of the 8KB of total RAM (see [Table 9-41](#)). This shared RAM can also be used by the regular application. The MSP CPU and the LEA module can run simultaneously and independently unless they access the same system RAM.

Direct access to LEA registers is not supported, and TI recommends using the optimized [Digital Signal Processing \(DSP\) Library for MSP Microcontrollers](#) for the operations that the LEA module supports.

## 9.4 Operating Modes

The MCU has one active mode and seven software selectable low-power modes of operation. An interrupt event can wake up the device from low-power modes LPM0 through LPM4, service the request, and restore back to the low-power mode on return from the interrupt program. Low-power modes LPM3.5 and LPM4.5 disable the core supply to minimize power consumption.

### Note

XT1CLK and VLOCLK can be active during LPM4 if requested by low-frequency peripherals such as RTC or WDT.

**Table 9-1. Operating Modes**

| MODE                                               | AM                      |                                 | LPM0                                | LPM1                    | LPM2                     | LPM3                     | LPM4                     | LPM3.5                  | LPM4.5            |                      |
|----------------------------------------------------|-------------------------|---------------------------------|-------------------------------------|-------------------------|--------------------------|--------------------------|--------------------------|-------------------------|-------------------|----------------------|
|                                                    | ACTIVE                  | ACTIVE, FRAM OFF <sup>(1)</sup> | CPU OFF <sup>(2)</sup>              | CPU OFF                 | STANDBY                  | STANDBY                  | OFF                      | RTC ONLY                | SHUTDOWN WITH SVS | SHUTDOWN WITHOUT SVS |
| Maximum system clock                               | 16 MHz                  |                                 | 16 MHz                              | 16 MHz                  | 50 kHz                   | 50 kHz                   | 0 <sup>(3)</sup>         | 50 kHz                  | 0 <sup>(3)</sup>  |                      |
| Typical current consumption, T <sub>A</sub> = 25°C | 120 µA/MHz              | 65 µA/MHz                       | 92 µA at 1 MHz                      | 40 µA at 1 MHz          | 1.0 µA                   | 0.7 µA                   | 0.5 µA                   | 0.45 µA                 | 0.3 µA            | 0.07 µA              |
| Typical wake-up time                               | N/A                     |                                 | Instant                             | 6 µs                    | 6 µs                     | 7 µs                     | 7 µs                     | 250 µs                  | 250 µs            | 400 µs               |
| Wake-up events                                     | N/A                     |                                 | All                                 | All                     | LF<br>RTC<br>I/O<br>Comp | LF<br>RTC<br>I/O<br>Comp | I/O<br>Comp              | RTC<br>I/O              | I/O               |                      |
| CPU                                                | On                      |                                 | Off                                 | Off                     | Off                      | Off                      | Off                      | Reset                   | Reset             |                      |
| LEA (MSP430FR599x only)                            | On                      |                                 | On <sup>(4)</sup>   Off             | Off                     | Off                      | Off                      | Off                      | Reset                   | Reset             |                      |
| FRAM                                               | On                      | Off <sup>(1)</sup>              | Standby<br>(or off <sup>(1)</sup> ) | Off                     | Off                      | Off                      | Off                      | Off                     | Off               |                      |
| High-frequency peripherals <sup>(5)</sup>          | Available               |                                 | Available                           | Available               | Off                      | Off                      | Off                      | Reset                   | Reset             |                      |
| Low-frequency peripherals <sup>(5)</sup>           | Available               |                                 | Available                           | Available               | Available                | Available <sup>(6)</sup> | Off                      | RTC                     | Reset             |                      |
| Unclocked peripherals <sup>(5)</sup>               | Available               |                                 | Available                           | Available               | Available                | Available <sup>(6)</sup> | Available <sup>(6)</sup> | Reset                   | Reset             |                      |
| MCLK                                               | On                      |                                 | On <sup>(4)</sup>   Off             | Off                     | Off                      | Off                      | Off                      | Off                     | Off               |                      |
| SMCLK                                              | Optional <sup>(7)</sup> |                                 | Optional <sup>(7)</sup>             | Optional <sup>(7)</sup> | Off                      | Off                      | Off                      | Off                     | Off               |                      |
| ACLK                                               | On                      |                                 | On                                  | On                      | On                       | On                       | Off                      | Off                     | Off               |                      |
| Full retention                                     | Yes                     |                                 | Yes                                 | Yes                     | Yes                      | Yes                      | Yes                      | No                      | No                |                      |
| SVS                                                | Always                  |                                 | Always                              | Always                  | Optional <sup>(8)</sup>  | Optional <sup>(8)</sup>  | optional <sup>(8)</sup>  | Optional <sup>(8)</sup> | On <sup>(9)</sup> | Off <sup>(10)</sup>  |
| Brownout                                           | Always                  |                                 | Always                              | Always                  | Always                   | Always                   | Always                   | Always                  | Always            |                      |

(1) FRAM disabled in FRAM controller A

(2) Disabling the FRAM through the FRAM controller A allows the application to lower the LPM current consumption but the wake-up time increases when FRAM is accessed (for example, to fetch an interrupt vector). For a wake up that does not access FRAM (for example, a DMA transfer to RAM) the wake-up time is not increased.

(3) All clocks disabled

(4) Only while the LEA module is performing the task enabled by CPU during AM. The LEA module cannot be enabled in LPM0.

(5) See [Section 9.4.1](#) for a detailed description of high-frequency, low-frequency, and unlocked peripherals.

(6) See [Section 9.4.2](#), which describes the use of peripherals in LPM3 and LPM4.

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- (7) Controlled by SMCLKOFF
- (8) Activate SVS (SVSHE = 1) results in higher current consumption. SVS is not included in typical current consumption.
- (9) SVSHE = 1
- (10) SVSHE = 0

### 9.4.1 Peripherals in Low-Power Modes

Peripherals can be in different states that impact the achievable power modes of the device. The states depend on the operational modes of the peripherals (see [Table 9-2](#)). The states are:

- A peripheral is in a *high-frequency state* if it requires or uses a clock with a "high" frequency of more than 50 kHz.
- A peripheral is in a *low-frequency state* if it requires or uses a clock with a "low" frequency of 50 kHz or less.
- A peripheral is in an *unlocked state* if it does not require or use an internal clock.

If the CPU requests a power mode that does not support the current state of all active peripherals, the device does not enter the requested power mode, but it does enter a power mode that still supports the current state of the peripherals, except if an external clock is used. If an external clock is used, the application must use the correct frequency range for the requested power mode.

**Table 9-2. Peripheral States**

| PERIPHERAL                                           | IN HIGH-FREQUENCY STATE <sup>(1)</sup>                | IN LOW-FREQUENCY STATE <sup>(2)</sup>                | IN UNLOCKED STATE <sup>(3)</sup>                                 |
|------------------------------------------------------|-------------------------------------------------------|------------------------------------------------------|------------------------------------------------------------------|
| WDT                                                  | Clocked by SMCLK                                      | Clocked by ACLK                                      | Not applicable                                                   |
| DMA <sup>(4)</sup>                                   | Not applicable                                        | Not applicable                                       | Waiting for a trigger                                            |
| RTC_C                                                | Not applicable                                        | Clocked by LFXT                                      | Not applicable                                                   |
| Timer_A TA <sub>x</sub>                              | Clocked by SMCLK or clocked by external clock >50 kHz | Clocked by ACLK or clocked by external clock ≤50 kHz | Clocked by external clock ≤50 kHz                                |
| Timer_B TB <sub>x</sub>                              | Clocked by SMCLK or clocked by external clock >50 kHz | Clocked by ACLK or clocked by external clock ≤50 kHz | Clocked by external clock ≤50 kHz                                |
| eUSCI_A <sub>x</sub> in UART mode                    | Clocked by SMCLK                                      | Clocked by ACLK                                      | Waiting for first edge of START bit.                             |
| eUSCI_A <sub>x</sub> in SPI master mode              | Clocked by SMCLK                                      | Clocked by ACLK                                      | Not applicable                                                   |
| eUSCI_A <sub>x</sub> in SPI slave mode               | Clocked by external clock >50 kHz                     | Clocked by external clock ≤50 kHz                    | Clocked by external clock ≤50 kHz                                |
| eUSCI_B <sub>x</sub> in I <sup>2</sup> C master mode | Clocked by SMCLK or clocked by external clock >50 kHz | Clocked by ACLK or clocked by external clock ≤50 kHz | Not applicable                                                   |
| eUSCI_B <sub>x</sub> in I <sup>2</sup> C slave mode  | Clocked by external clock >50 kHz                     | Clocked by external clock ≤50 kHz                    | Waiting for START condition or clocked by external clock ≤50 kHz |
| eUSCI_B <sub>x</sub> in SPI master mode              | Clocked by SMCLK                                      | Clocked by ACLK                                      | Not applicable                                                   |
| eUSCI_B <sub>x</sub> in SPI slave mode               | Clocked by external clock >50 kHz                     | Clocked by external clock ≤50 kHz                    | Clocked by external clock ≤50 kHz                                |
| ADC12_B                                              | Clocked by SMCLK or by MODOSC                         | Clocked by ACLK                                      | Waiting for a trigger                                            |
| REF_A                                                | Not applicable                                        | Not applicable                                       | Always                                                           |
| COMP_E                                               | Not applicable                                        | Not applicable                                       | Always                                                           |
| CRC <sup>(5)</sup>                                   | Not applicable                                        | Not applicable                                       | Not applicable                                                   |
| MPY <sup>(5)</sup>                                   | Not applicable                                        | Not applicable                                       | Not applicable                                                   |
| AES <sup>(5)</sup>                                   | Not applicable                                        | Not applicable                                       | Not applicable                                                   |

- (1) Peripherals are in a state that requires or uses a clock with a "high" frequency of more than 50 kHz
- (2) Peripherals are in a state that requires or uses a clock with a "low" frequency of 50 kHz or less.
- (3) Peripherals are in a state that does not require or does not use an internal clock.
- (4) The DMA always transfers data in active mode but can wait for a trigger in any low-power mode. A DMA trigger during a low-power mode causes a temporary transition into active mode for the time of the transfer.
- (5) This peripheral operates during active mode only and will delay the transition into a low-power mode until its operation is completed.

## 9.4.2 Idle Currents of Peripherals in LPM3 and LPM4

Most peripherals can be operational in LPM3 if clocked by ACLK. Some modules are operational in LPM4, because they do not require a clock to operate (for example, the comparator). Activating a peripheral in LPM3 or LPM4 increases the current consumption due to its active supply current contribution but also due to an additional idle current. To reduce the idle current adder, certain peripherals are grouped together (see [Table 9-3](#)). To achieve optimal current consumption, use modules within one group and limit the number of groups with active modules. Modules not listed in [Table 9-3](#) are either already included in the standard LPM3 current consumption or cannot be used in LPM3 or LPM4.

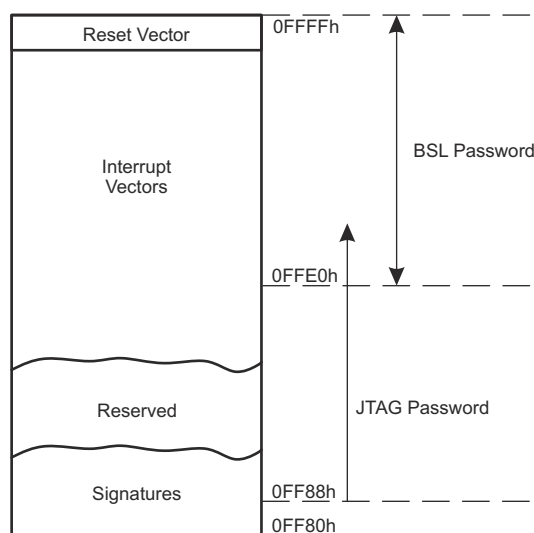
The idle current adder is very small at room temperature (25°C) but increases at high temperatures (85°C). See the  $I_{IDLE}$  current parameters in [Section 8](#) for details.

**Table 9-3. Peripheral Groups**

| GROUP A   | GROUP B    | GROUP C   |
|-----------|------------|-----------|
| Timer TA1 | Timer TA0  | Timer TA4 |
| Timer TA2 | Timer TA3  | eUSCI_A2  |
| Timer TB0 | Comparator | eUSCI_A3  |
| eUSCI_A0  | ADC12_B    | eUSCI_B1  |
| eUSCI_A1  | REF_A      | eUSCI_B2  |
| eUSCI_B0  |            | eUSCI_B3  |

## 9.5 Interrupt Vector Table and Signatures

The interrupt vectors, the power-up start address and signatures are in the address range 0FFFFh to 0FF80h. [Figure 9-1](#) summarizes the content of this address range.



**Figure 9-1. Interrupt Vectors, Signatures and Passwords**

The power-up start address or reset vector is at 0FFFFh to 0FFFEh. This location contains a 16-bit address pointing to the start address of the application program.

The interrupt vectors start at 0FFFDh and extend to lower addresses. Each vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence. [Table 9-4](#) shows the device specific interrupt vector locations.

The vectors programmed into the address range from 0FFFFh to 0FFE0h are used as BSL password (if enabled by the corresponding signature).

The signatures are at 0FF80h and extend to higher addresses. Signatures are evaluated during device start-up. [Table 9-5](#) lists the device-specific signature locations.

A JTAG password can be programmed starting at address 0FF88h and extending to higher addresses. The password can extend into the interrupt vector locations using the interrupt vector addresses as additional bits for the password. The length of the JTAG password depends on the JTAG signature.

See the *System Resets, Interrupts, and Operating Modes, System Control Module (SYS)* chapter in the *MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx Family User's Guide* for details.

**Table 9-4. Interrupt Sources, Flags, and Vectors**

| INTERRUPT SOURCE                                                                                                                                                                                                                                                            | INTERRUPT FLAG                                                                                                                                                                                     | INTERRUPT VECTOR REGISTER | SYSTEM INTERRUPT             | WORD ADDRESS | PRIORITY |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------|------------------------------|--------------|----------|
| <b>System Reset</b><br>Power up, brownout, supply supervisor<br>External reset, $\overline{RST}$<br>Watchdog time-out (watchdog mode)<br>WDT, FRCTL MPU, CS, PMM password violation<br>FRAM uncorrectable bit error detection<br>MPU segment violation<br>Software POR, BOR | SVSHIFG<br><br>PMMRSTIFG<br>WDTIFG<br><br>WDTPW, FRCTLPW, MPUPW, CSPW, PMMPW<br><br>UBDIFG<br><br>MPUSEG1IFG, MPUSEG11IFG, MPUSEG2IFG, MPUSEG3IFG<br>PMPORIFG, PMMBORIFG                           | SYSRSTIV <sup>(1)</sup>   | Reset                        | 0FFFEh       | Highest  |
| <b>System NMI</b><br>Vacant memory access <sup>(2)</sup><br>JTAG mailbox<br>FRAM access time error<br>FRAM write protection error<br>FRAM bit error detection<br>MPU segment violation                                                                                      | VMAIFG<br>JMBINIFG, JMBOUTIFG<br>ACCTEIFG<br>WPIFG<br><br>CBDIFG, UBDIFG<br>MPUSEG1IFG, MPUSEG11IFG, MPUSEG2IFG, MPUSEG3IFG                                                                        | SYSSNIV <sup>(1)</sup>    | (Non)maskable <sup>(3)</sup> | 0FFFCh       |          |
| <b>User NMI</b><br>External NMI<br>Oscillator fault                                                                                                                                                                                                                         | NMIIFG<br>OFIFG                                                                                                                                                                                    | SYSUNIV <sup>(1)</sup>    | (Non)maskable <sup>(3)</sup> | 0FFFAh       |          |
| Comparator_E                                                                                                                                                                                                                                                                | CEIFG, CEIIFG                                                                                                                                                                                      | CEIV <sup>(1)</sup>       | Maskable                     | 0FFF8h       |          |
| TB0                                                                                                                                                                                                                                                                         | TB0CCR0 CCIFG                                                                                                                                                                                      |                           | Maskable                     | 0FFF6h       |          |
| TB0                                                                                                                                                                                                                                                                         | TB0CCR1 CCIFG to TB0CCR6 CCIFG, TB0CTL.TBIFG                                                                                                                                                       | TB0IV <sup>(1)</sup>      | Maskable                     | 0FFF4h       |          |
| Watchdog timer (interval timer mode)                                                                                                                                                                                                                                        | WDTIFG                                                                                                                                                                                             |                           | Maskable                     | 0FFF2h       |          |
| eUSCI_A0 receive or transmit                                                                                                                                                                                                                                                | UCRXIFG, UCTXIFG (SPI mode)<br>UCSTTIFG, UCTXCFIFG, UCRXIFG, UCTXIFG (UART mode)                                                                                                                   | UCA0IV <sup>(1)</sup>     | Maskable                     | 0FFF0h       |          |
| eUSCI_B0 receive or transmit                                                                                                                                                                                                                                                | UCRXIFG, UCTXIFG (SPI mode)<br>UCALIFG, UCNACKIFG, UCSTTIFG, UCSTPIFG, UCRXIFG0, UCTXIFG0, UCRXIFG1, UCTXIFG1, UCRXIFG2, UCTXIFG2, UCRXIFG3, UCTXIFG3, UCCNTIFG, UCBIT9IFG (I <sup>2</sup> C mode) | UCB0IV <sup>(1)</sup>     | Maskable                     | 0FFEEh       |          |
| ADC12_B <sup>(4)</sup>                                                                                                                                                                                                                                                      | ADC12IFG0 to ADC12IFG31, ADC12LOIFG, ADC12INIFG, ADC12HIIFG, ADC12RDYIFG, ADC21OVIFG, ADC12TOVIFG                                                                                                  | ADC12IV <sup>(1)</sup>    | Maskable                     | 0FFECCh      |          |

**Table 9-4. Interrupt Sources, Flags, and Vectors (continued)**

| INTERRUPT SOURCE             | INTERRUPT FLAG                                                                                                                                                                                     | INTERRUPT VECTOR REGISTER | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------|------------------|--------------|----------|
| TA0                          | TA0CCR0 CCIFG                                                                                                                                                                                      |                           | Maskable         | 0FFEAh       |          |
| TA0                          | TA0CCR1 CCIFG, TA0CCR2 CCIFG, TA0CTL.TAIFG                                                                                                                                                         | TA0IV <sup>(1)</sup>      | Maskable         | 0FFE8h       |          |
| eUSCI_A1 receive or transmit | UCRXIFG, UCTXIFG (SPI mode)<br>UCSTTIFG, UCTXCFIFG, UCRXIFG, UCTXIFG (UART mode)                                                                                                                   | UCA1IV <sup>(1)</sup>     | Maskable         | 0FFE6h       |          |
| DMA                          | DMA0CTL.DMAIFG, DMA1CTL.DMAIFG, DMA2CTL.DMAIFG                                                                                                                                                     | DMAIV <sup>(1)</sup>      | Maskable         | 0FFE4h       |          |
| TA1                          | TA1CCR0 CCIFG                                                                                                                                                                                      |                           | Maskable         | 0FFE2h       |          |
| TA1                          | TA1CCR1 CCIFG, TA1CCR2 CCIFG, TA1CTL.TAIFG                                                                                                                                                         | TA1IV <sup>(1)</sup>      | Maskable         | 0FFE0h       |          |
| I/O port P1                  | P1IFG.0 to P1IFG.7                                                                                                                                                                                 | P1IV <sup>(1)</sup>       | Maskable         | 0FFDEh       |          |
| TA2                          | TA2CCR0 CCIFG                                                                                                                                                                                      |                           | Maskable         | 0FFDCh       |          |
| TA2                          | TA2CCR1 CCIFG, TA2CTL.TAIFG                                                                                                                                                                        | TA2IV <sup>(1)</sup>      | Maskable         | 0FFDAh       |          |
| I/O port P2                  | P2IFG.0 to P2IFG.7                                                                                                                                                                                 | P2IV <sup>(1)</sup>       | Maskable         | 0FFD8h       |          |
| TA3                          | TA3CCR0 CCIFG                                                                                                                                                                                      |                           | Maskable         | 0FFD6h       |          |
| TA3                          | TA3CCR1 CCIFG, TA3CTL.TAIFG                                                                                                                                                                        | TA3IV <sup>(1)</sup>      | Maskable         | 0FFD4h       |          |
| I/O port P3                  | P3IFG.0 to P3IFG.7                                                                                                                                                                                 | P3IV <sup>(1)</sup>       | Maskable         | 0FFD2h       |          |
| I/O port P4                  | P4IFG.0 to P4IFG.7                                                                                                                                                                                 | P4IV <sup>(1)</sup>       | Maskable         | 0FFD0h       |          |
| RTC_C                        | RTCRDYIFG, RTCTEVIFG, RTCAIFG, RT0PSIFG, RT1PSIFG, RTCOFIFG                                                                                                                                        | RTCIV <sup>(1)</sup>      | Maskable         | 0FFCEh       |          |
| AES                          | AESRDYIFG                                                                                                                                                                                          |                           | Maskable         | 0FFCCh       |          |
| TA4                          | TA4CCR0 CCIFG                                                                                                                                                                                      |                           | Maskable         | 0FFCAh       |          |
| TA4                          | TA4CCR1 CCIFG, TA4CTL.TAIFG                                                                                                                                                                        | TA4IV <sup>(1)</sup>      | Maskable         | 0FFC8h       |          |
| I/O port P5                  | P5IFG.0 to P5IFG.7                                                                                                                                                                                 | P5IV <sup>(1)</sup>       | Maskable         | 0FFC6h       |          |
| I/O port P6                  | P6IFG.0 to P6IFG.7                                                                                                                                                                                 | P6IV <sup>(1)</sup>       | Maskable         | 0FFC4h       |          |
| eUSCI_A2 receive or transmit | UCRXIFG, UCTXIFG (SPI mode)<br>UCSTTIFG, UCTXCFIFG, UCRXIFG, UCTXIFG (UART mode)                                                                                                                   | UCA2IV <sup>(1)</sup>     | Maskable         | 0FFC2h       |          |
| eUSCI_A3 receive or transmit | UCRXIFG, UCTXIFG (SPI mode)<br>UCSTTIFG, UCTXCFIFG, UCRXIFG, UCTXIFG (UART mode)                                                                                                                   | UCA3IV <sup>(1)</sup>     | Maskable         | 0FFC0h       |          |
| eUSCI_B1 receive or transmit | UCRXIFG, UCTXIFG (SPI mode)<br>UCALIFG, UCNACKIFG, UCSTTIFG, UCSTPIFG, UCRXIFG0, UCTXIFG0, UCRXIFG1, UCTXIFG1, UCRXIFG2, UCTXIFG2, UCRXIFG3, UCTXIFG3, UCCNTIFG, UCBIT9IFG (I <sup>2</sup> C mode) | UCB1IV <sup>(1)</sup>     | Maskable         | 0FFBEh       |          |
| eUSCI_B2 receive or transmit | UCRXIFG, UCTXIFG (SPI mode)<br>UCALIFG, UCNACKIFG, UCSTTIFG, UCSTPIFG, UCRXIFG0, UCTXIFG0, UCRXIFG1, UCTXIFG1, UCRXIFG2, UCTXIFG2, UCRXIFG3, UCTXIFG3, UCCNTIFG, UCBIT9IFG (I <sup>2</sup> C mode) | UCB2IV <sup>(1)</sup>     | Maskable         | 0FFBCh       |          |
| eUSCI_B3 receive or transmit | UCRXIFG, UCTXIFG (SPI mode)<br>UCALIFG, UCNACKIFG, UCSTTIFG, UCSTPIFG, UCRXIFG0, UCTXIFG0, UCRXIFG1, UCTXIFG1, UCRXIFG2, UCTXIFG2, UCRXIFG3, UCTXIFG3, UCCNTIFG, UCBIT9IFG (I <sup>2</sup> C mode) | UCB3IV <sup>(1)</sup>     | Maskable         | 0FFBAh       |          |

**Table 9-4. Interrupt Sources, Flags, and Vectors (continued)**

| INTERRUPT SOURCE        | INTERRUPT FLAG                        | INTERRUPT VECTOR REGISTER | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|-------------------------|---------------------------------------|---------------------------|------------------|--------------|----------|
| I/O port P7             | P7IFG.0 to P7IFG.7                    | P7IV <sup>(1)</sup>       | Maskable         | 0FFB8h       |          |
| I/O port P8             | P8IFG.0 to P8IFG.7                    | P8IV <sup>(1)</sup>       | Maskable         | 0FFB6h       |          |
| LEA (MSP430FR599x only) | CMDIFG, SDIIFG, OORIFG, TIFG, COVLIFG | LEAIV <sup>(1)</sup>      | Maskable         | 0FFB4h       | Lowest   |

- (1) Multiple source flags  
(2) A reset is generated if the CPU tries to fetch instructions from peripheral space.  
(3) (Non)maskable: the individual interrupt enable bit can disable an interrupt event, but the general interrupt enable bit cannot disable it.  
(4) Only on devices with ADC, otherwise reserved.

**Table 9-5. Signatures**

| SIGNATURE                                   | WORD ADDRESS |
|---------------------------------------------|--------------|
| IP Encapsulation Signature 2                | 0FF8Ah       |
| IP Encapsulation Signature 1 <sup>(1)</sup> | 0FF88h       |
| BSL Signature 2                             | 0FF86h       |
| BSL Signature 1                             | 0FF84h       |
| JTAG Signature 2                            | 0FF82h       |
| JTAG Signature 1                            | 0FF80h       |

- (1) Must not contain 0AAAAh if used as the JTAG password.

## 9.6 Bootloader (BSL)

The BSL can program the FRAM or RAM using a UART serial interface (FRxxxx devices) or an I<sup>2</sup>C interface (FRxxxx1 devices). Access to the device memory through the BSL is protected by a user-defined password. [Table 9-6](#) lists the pins that are required to use the BSL. BSL entry requires a specific entry sequence on the RST/NMI/SBWTIO and TEST/SBWTCK pins. For a complete description of the features of the BSL and its implementation, see the [MSP430 FRAM Devices Bootloader \(BSL\) User's Guide](#). Visit [Bootloader \(BSL\) for MSP low-power microcontrollers](#) for more information.

**Table 9-6. BSL Pin Requirements and Functions**

| DEVICE SIGNAL  | BSL FUNCTION                                       |
|----------------|----------------------------------------------------|
| RST/NMI/SBWTIO | Entry sequence signal                              |
| TEST/SBWTCK    | Entry sequence signal                              |
| P2.0           | Devices with UART BSL (FRxxxx): Data transmit      |
| P2.1           | Devices with UART BSL (FRxxxx): Data receive       |
| P1.6           | Devices with I <sup>2</sup> C BSL (FRxxxx1): Data  |
| P1.7           | Devices with I <sup>2</sup> C BSL (FRxxxx1): Clock |
| DVCC           | Power supply                                       |
| DVSS           | Ground supply                                      |

## 9.7 JTAG Operation

### 9.7.1 JTAG Standard Interface

The MSP family supports the standard JTAG interface, which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/O. The TEST/SBWTCK pin is used to enable the JTAG signals. In addition to these signals, the  $\overline{\text{RST}}$ /NMI/SBWDIO is required to interface with MSP development tools and device programmers. Table 9-7 lists the JTAG pin requirements. For further details on interfacing to development tools and device programmers, see the [MSP430 Hardware Tools User's Guide](#). For a complete description of the features of the JTAG interface and its implementation, see [MSP430 Programming With the JTAG Interface](#).

**Table 9-7. JTAG Pin Requirements and Functions**

| DEVICE SIGNAL                       | DIRECTION | FUNCTION                    |
|-------------------------------------|-----------|-----------------------------|
| PJ.3/TCK                            | IN        | JTAG clock input            |
| PJ.2/TMS                            | IN        | JTAG state control          |
| PJ.1/TDI/TCLK                       | IN        | JTAG data input, TCLK input |
| PJ.0/TDO                            | OUT       | JTAG data output            |
| TEST/SBWTCK                         | IN        | Enable JTAG pins            |
| $\overline{\text{RST}}$ /NMI/SBWDIO | IN        | External reset              |
| DVCC                                |           | Power supply                |
| DVSS                                |           | Ground supply               |

### 9.7.2 Spy-Bi-Wire Interface

In addition to the standard JTAG interface, the MSP family supports the two wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP development tools and device programmers. The Spy-Bi-Wire interface pin requirements are shown in Table 9-8. For further details on interfacing to development tools and device programmers, see the [MSP430 Hardware Tools User's Guide](#). For a complete description of the features of the JTAG interface and its implementation, see [MSP430 Programming With the JTAG Interface](#).

**Table 9-8. Spy-Bi-Wire Pin Requirements and Functions**

| DEVICE SIGNAL                       | DIRECTION | FUNCTION                          |
|-------------------------------------|-----------|-----------------------------------|
| TEST/SBWTCK                         | IN        | Spy-Bi-Wire clock input           |
| $\overline{\text{RST}}$ /NMI/SBWDIO | IN, OUT   | Spy-Bi-Wire data input and output |
| DVCC                                |           | Power supply                      |
| DVSS                                |           | Ground supply                     |

## 9.8 FRAM Controller A (FRCTL\_A)

The FRAM can be programmed through the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in system by the CPU (also see [Table 9-45](#) for control and configuration registers). Features of the FRAM include:

- Ultra-low-power ultra-fast-write nonvolatile memory
- Byte and word access capability
- Programmable wait state generation
- Error correction coding (ECC)

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### Note

#### Wait States

For MCLK frequencies > 8 MHz, wait states must be configured following the flow described in the "Wait State Control" section of the *FRAM Controller A (FRCTL\_A)* chapter in the [MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx Family User's Guide](#).

For important software design information regarding FRAM including but not limited to partitioning the memory layout according to application-specific code, constant, and data space requirements, the use of FRAM to optimize application energy consumption, and the use of the Memory Protection Unit (MPU) to maximize application robustness by protecting the program code against unintended write accesses, see [MSP430™ FRAM Technology – How To and Best Practices](#).

## 9.9 RAM

The RAM is made up of three sectors: Sector 0 = 2KB, Sector 1 = 2KB, and Sector 2 = 4KB (shared with the LEA module). Each sector can be individually powered down in LPM3 and LPM4 to save leakage. Data is lost when sectors are powered down in LPM3 and LPM4. See [Table 9-47](#) for control and configuration registers.

## 9.10 Tiny RAM

Tiny RAM provides 22 bytes of RAM in addition to the complete RAM (see [Table 9-41](#)). This memory is always available, even in LPM3 and LPM4, while the complete RAM can be powered down in LPM3 and LPM4. Tiny RAM can be used to hold data or a very small stack when the complete RAM is powered down in LPM3 and LPM4. No memory is available in LPMx.5.

## 9.11 Memory Protection Unit (MPU) Including IP Encapsulation

The FRAM can be protected by the MPU from inadvertent CPU execution, read access, or write access. See [Table 9-67](#) for control and configuration registers. Features of the MPU include:

- IP encapsulation with programmable boundaries in steps of 1KB (prevents reads from "outside"; for example, through JTAG or by non-IP software).
- Main memory partitioning is programmable up to three segments in steps of 1KB.
- Access rights of each segment can be individually selected (main and information memory).
- Access violation flags with interrupt capability for easy servicing of access violations.

## 9.12 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. The peripherals can be managed using all instructions. For complete module descriptions, see the [MSP430FR58xx](#), [MSP430FR59xx](#), and [MSP430FR6xx Family User's Guide](#).

### 9.12.1 Digital I/O

Up to nine 8-bit I/O ports are implemented (see [Table 9-52](#) through [Table 9-56](#) for control and configuration registers):

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Programmable pullup or pulldown on all ports.
- Edge-selectable interrupt and LPM3.5 and LPM4.5 wake-up input capability is available for all pins of ports P1 to P8.
- Read and write access to port control registers is supported by all instructions.
- Ports can be accessed byte-wise or word-wise in pairs.
- All pins of ports P1 to P8, and PJ support capacitive touch functionality.
- No cross-currents during start-up.

---

#### Note

##### Configuration of Digital I/Os After BOR Reset

To prevent any cross currents during start-up of the device, all port pins are high-impedance with Schmitt triggers and their module functions disabled. To enable the I/O functionality after a BOR reset, first configure the ports and then clear the LOCKLPM5 bit. For details, see the *Configuration After Reset* section of the *Digital I/O* chapter in the [MSP430FR58xx](#), [MSP430FR59xx](#), and [MSP430FR6xx Family User's Guide](#).

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### 9.12.2 Oscillator and Clock System (CS)

The clock system includes support for a 32-kHz watch-crystal oscillator XT1 (LF), an internal very-low-power low-frequency oscillator (VLO), an integrated internal digitally controlled oscillator (DCO), and a high-frequency crystal oscillator XT2 (HF). The clock system module is designed to meet the requirements of both low system cost and low power consumption. A fail-safe mechanism exists for all crystal sources. See [Table 9-49](#) for control and configuration registers.

The clock system module provides the following clock signals:

- Auxiliary clock (ACLK). ACLK can be sourced from a 32-kHz watch crystal (LFXT1), the internal VLO, or a digital external low-frequency (<50 kHz) clock source.
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced from a high-frequency crystal (HFXT2), the internal DCO, a 32-kHz watch crystal (LFXT1), the internal VLO, or a digital external clock source.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by same sources made available to MCLK.

### 9.12.3 Power-Management Module (PMM)

The PMM includes an integrated voltage regulator that supplies the core voltage to the device. The PMM also includes supply voltage supervisor (SVS) and brownout protection. The brownout circuit provides the proper internal reset signal to the device during power on and power off. The SVS circuitry detects if the supply voltage drops below a safe level and below a user-selectable level. SVS circuitry is available on the primary and core supplies. See [Table 9-44](#) for control and configuration registers.

### 9.12.4 Hardware Multiplier (MPY)

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-, 24-, 16-, and 8-bit operands. The module supports signed multiplication, unsigned multiplication, signed multiply-and-accumulate, and unsigned multiply-and-accumulate operations. See [Table 9-65](#) for control and configuration registers.

### 9.12.5 Real-Time Clock (RTC\_C)

The RTC\_C module contains an integrated real-time clock (RTC) with the following features:

- Calendar mode with leap year correction
- General-purpose counter mode

The internal calendar compensates for months with fewer than 31 days and includes leap year correction. The RTC\_C also supports flexible alarm functions and offset-calibration hardware. RTC operation is available in LPM3.5 modes to minimize power consumption. See [Table 9-64](#) for control and configuration registers.

### 9.12.6 Watchdog Timer (WDT\_A)

The primary function of the WDT\_A module is to perform a controlled system restart if a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals. [Table 9-9](#) lists the clocks that can source WDT\_A. See [Table 9-48](#) for control and configuration registers.

**Table 9-9. WDT\_A Clocks**

| WDTSEL | NORMAL OPERATION<br>(WATCHDOG AND INTERVAL TIMER<br>MODE) |
|--------|-----------------------------------------------------------|
| 00     | SMCLK                                                     |
| 01     | ACLK                                                      |
| 10     | VLOCLK                                                    |
| 11     | LFMODCLK                                                  |

### 9.12.7 System Module (SYS)

The SYS module manages many of the system functions within the device. These include power-on reset (POR) and power-up clear (PUC) handling, NMI source selection and management, reset interrupt vector generators (see [Table 9-10](#)), bootloader (BSL) entry mechanisms, and configuration management (device descriptors). The SYS module also includes a data exchange mechanism through JTAG called a JTAG mailbox that can be used in the application. See [Table 9-50](#) for control and configuration registers.

**Table 9-10. System Module Interrupt Vector Registers**

| INTERRUPT VECTOR REGISTER | ADDRESS | INTERRUPT EVENT                                           | VALUE      | PRIORITY |
|---------------------------|---------|-----------------------------------------------------------|------------|----------|
| SYSRSTIV, System Reset    | 019Eh   | No interrupt pending                                      | 00h        |          |
|                           |         | Brownout (BOR)                                            | 02h        | Highest  |
|                           |         | RSTIFG RST/NMI (BOR)                                      | 04h        |          |
|                           |         | PMMSWBOR software BOR (BOR)                               | 06h        |          |
|                           |         | LPMx.5 wake up (BOR)                                      | 08h        |          |
|                           |         | Security violation (BOR)                                  | 0Ah        |          |
|                           |         | Reserved                                                  | 0Ch        |          |
|                           |         | SVSHIFG SVSH event (BOR)                                  | 0Eh        |          |
|                           |         | Reserved                                                  | 10h        |          |
|                           |         | Reserved                                                  | 12h        |          |
|                           |         | PMMSWPOR software POR (POR)                               | 14h        |          |
|                           |         | WDTIFG watchdog timeout (PUC)                             | 16h        |          |
|                           |         | WDTPW password violation (PUC)                            | 18h        |          |
|                           |         | FRCTLPW password violation (PUC)                          | 1Ah        |          |
|                           |         | Uncorrectable FRAM bit error detection (PUC)              | 1Ch        |          |
|                           |         | Peripheral area fetch (PUC)                               | 1Eh        |          |
|                           |         | PMMPW PMM password violation (PUC)                        | 20h        |          |
|                           |         | MPUPW MPU password violation (PUC)                        | 22h        |          |
|                           |         | CSPW CS password violation (PUC)                          | 24h        |          |
|                           |         | MPUSEG1IFG encapsulated IP memory segment violation (PUC) | 26h        |          |
|                           |         | MPUSEG2IFG information memory segment violation (PUC)     | 28h        |          |
|                           |         | MPUSEG1IFG segment 1 memory violation (PUC)               | 2Ah        |          |
|                           |         | MPUSEG2IFG segment 2 memory violation (PUC)               | 2Ch        |          |
|                           |         | MPUSEG3IFG segment 3 memory violation (PUC)               | 2Eh        |          |
| SYSSNIV, System NMI       | 019Ch   | Reserved                                                  | 30h to 3Eh | Lowest   |
|                           |         | No interrupt pending                                      | 00h        |          |
|                           |         | Reserved                                                  | 02h        | Highest  |
|                           |         | Uncorrectable FRAM bit error detection                    | 04h        |          |
|                           |         | FRAM access time error                                    | 06h        |          |
|                           |         | MPUSEG1IFG encapsulated IP memory segment violation       | 08h        |          |
|                           |         | MPUSEG2IFG information memory segment violation           | 0Ah        |          |
|                           |         | MPUSEG1IFG segment 1 memory violation                     | 0Ch        |          |
|                           |         | MPUSEG2IFG segment 2 memory violation                     | 0Eh        |          |
|                           |         | MPUSEG3IFG segment 3 memory violation                     | 10h        |          |
|                           |         | VMAIFG vacant memory access                               | 12h        |          |
|                           |         | JMBINIFG JTAG mailbox input                               | 14h        |          |
|                           |         | JMBOUTIFG JTAG mailbox output                             | 16h        |          |
|                           |         | Correctable FRAM bit error detection                      | 18h        |          |
|                           |         | FRAM write protection detection                           | 1Ah        |          |
|                           |         | LEA time-out fault <sup>(1)</sup>                         | 1Ch        |          |
|                           |         | LEA command fault <sup>(1)</sup>                          | 1Eh        | Lowest   |

**Table 9-10. System Module Interrupt Vector Registers (continued)**

| INTERRUPT VECTOR REGISTER | ADDRESS | INTERRUPT EVENT        | VALUE      | PRIORITY |
|---------------------------|---------|------------------------|------------|----------|
| SYSUNIV, User NMI         | 019Ah   | No interrupt pending   | 00h        |          |
|                           |         | NMIIFG NMI pin         | 02h        | Highest  |
|                           |         | OFIFG oscillator fault | 04h        |          |
|                           |         | Reserved               | 06h        |          |
|                           |         | Reserved               | 08h        |          |
|                           |         | Reserved               | 0Ah to 1Eh | Lowest   |

(1) Reserved on MSP430FR596x.

### 9.12.8 DMA Controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC12\_B conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode, without having to awaken to move data to or from a peripheral. See [Table 9-66](#) for control and configuration registers. [Table 9-11](#) lists the available DMA triggers.

**Table 9-11. DMA Trigger Assignments**

| TRIGGER<br>(1) | CHANNEL 0                                        | CHANNEL 1                                        | CHANNEL 2                                        | CHANNEL 3                                        | CHANNEL 4                                        | CHANNEL 5                                        |
|----------------|--------------------------------------------------|--------------------------------------------------|--------------------------------------------------|--------------------------------------------------|--------------------------------------------------|--------------------------------------------------|
| 0              | DMAREQ                                           | DMAREQ                                           | DMAREQ                                           | DMAREQ                                           | DMAREQ                                           | DMAREQ                                           |
| 1              | TA0CCR0 CCIFG                                    | TA0CCR0 CCIFG                                    | TA0CCR0 CCIFG                                    | TA0CCR0 CCIFG                                    | TA0CCR0 CCIFG                                    | TA0CCR0 CCIFG                                    |
| 2              | TA0CCR2 CCIFG                                    | TA0CCR2 CCIFG                                    | TA0CCR2 CCIFG                                    | TA0CCR2 CCIFG                                    | TA0CCR2 CCIFG                                    | TA0CCR2 CCIFG                                    |
| 3              | TA1CCR0 CCIFG                                    | TA1CCR0 CCIFG                                    | TA1CCR0 CCIFG                                    | TA1CCR0 CCIFG                                    | TA1CCR0 CCIFG                                    | TA1CCR0 CCIFG                                    |
| 4              | TA1CCR2 CCIFG                                    | TA1CCR2 CCIFG                                    | TA1CCR2 CCIFG                                    | TA1CCR2 CCIFG                                    | TA1CCR2 CCIFG                                    | TA1CCR2 CCIFG                                    |
| 5              | TA2CCR0 CCIFG                                    | TA2CCR0 CCIFG                                    | TA2CCR0 CCIFG                                    | TA2CCR0 CCIFG                                    | TA2CCR0 CCIFG                                    | TA2CCR0 CCIFG                                    |
| 6              | TA3CCR0 CCIFG                                    | TA3CCR0 CCIFG                                    | TA3CCR0 CCIFG                                    | TA3CCR0 CCIFG                                    | TA3CCR0 CCIFG                                    | TA3CCR0 CCIFG                                    |
| 7              | TB0CCR0 CCIFG                                    | TB0CCR0 CCIFG                                    | TB0CCR0 CCIFG                                    | TB0CCR0 CCIFG                                    | TB0CCR0 CCIFG                                    | TB0CCR0 CCIFG                                    |
| 8              | TB0CCR2 CCIFG                                    | TB0CCR2 CCIFG                                    | TB0CCR2 CCIFG                                    | TB0CCR2 CCIFG                                    | TB0CCR2 CCIFG                                    | TB0CCR2 CCIFG                                    |
| 9              | TA4CCR0 CCIFG                                    | TA4CCR0 CCIFG                                    | TA4CCR0 CCIFG                                    | TA4CCR0 CCIFG                                    | TA4CCR0 CCIFG                                    | TA4CCR0 CCIFG                                    |
| 10             | Reserved                                         | Reserved                                         | Reserved                                         | Reserved                                         | Reserved                                         | Reserved                                         |
| 11             | AES Trigger 0                                    | AES Trigger 0                                    | AES Trigger 0                                    | AES Trigger 0                                    | AES Trigger 0                                    | AES Trigger 0                                    |
| 12             | AES Trigger 1                                    | AES Trigger 1                                    | AES Trigger 1                                    | AES Trigger 1                                    | AES Trigger 1                                    | AES Trigger 1                                    |
| 13             | AES Trigger 2                                    | AES Trigger 2                                    | AES Trigger 2                                    | AES Trigger 2                                    | AES Trigger 2                                    | AES Trigger 2                                    |
| 14             | UCA0RXIFG                                        | UCA0RXIFG                                        | UCA0RXIFG                                        | UCA2RXIFG                                        | UCA2RXIFG                                        | UCA2RXIFG                                        |
| 15             | UCA0TXIFG                                        | UCA0TXIFG                                        | UCA0TXIFG                                        | UCA2TXIFG                                        | UCA2TXIFG                                        | UCA2TXIFG                                        |
| 16             | UCA1RXIFG                                        | UCA1RXIFG                                        | UCA1RXIFG                                        | UCA3RXIFG                                        | UCA3RXIFG                                        | UCA3RXIFG                                        |
| 17             | UCA1TXIFG                                        | UCA1TXIFG                                        | UCA1TXIFG                                        | UCA3TXIFG                                        | UCA3TXIFG                                        | UCA3TXIFG                                        |
| 18             | UCB0RXIFG (SPI)<br>UCB0RXIFG0 (I <sup>2</sup> C) | UCB0RXIFG (SPI)<br>UCB0RXIFG0 (I <sup>2</sup> C) | UCB0RXIFG (SPI)<br>UCB0RXIFG0 (I <sup>2</sup> C) | UCB1RXIFG (SPI)<br>UCB1RXIFG0 (I <sup>2</sup> C) | UCB2RXIFG (SPI)<br>UCB2RXIFG0 (I <sup>2</sup> C) | UCB3RXIFG (SPI)<br>UCB3RXIFG0 (I <sup>2</sup> C) |
| 19             | UCB0TXIFG (SPI)<br>UCB0TXIFG0 (I <sup>2</sup> C) | UCB0TXIFG (SPI)<br>UCB0TXIFG0 (I <sup>2</sup> C) | UCB0TXIFG (SPI)<br>UCB0TXIFG0 (I <sup>2</sup> C) | UCB1TXIFG (SPI)<br>UCB1TXIFG0 (I <sup>2</sup> C) | UCB2TXIFG (SPI)<br>UCB2TXIFG0 (I <sup>2</sup> C) | UCB3TXIFG (SPI)<br>UCB3TXIFG0 (I <sup>2</sup> C) |
| 20             | UCB0RXIFG1 (I <sup>2</sup> C)                    | UCB0RXIFG1 (I <sup>2</sup> C)                    | UCB0RXIFG1 (I <sup>2</sup> C)                    | UCB1RXIFG1 (I <sup>2</sup> C)                    | UCB2RXIFG1 (I <sup>2</sup> C)                    | UCB3RXIFG1 (I <sup>2</sup> C)                    |
| 21             | UCB0TXIFG1 (I <sup>2</sup> C)                    | UCB0TXIFG1 (I <sup>2</sup> C)                    | UCB0TXIFG1 (I <sup>2</sup> C)                    | UCB1TXIFG1 (I <sup>2</sup> C)                    | UCB2TXIFG1 (I <sup>2</sup> C)                    | UCB3TXIFG1 (I <sup>2</sup> C)                    |
| 22             | UCB0RXIFG2 (I <sup>2</sup> C)                    | UCB0RXIFG2 (I <sup>2</sup> C)                    | UCB0RXIFG2 (I <sup>2</sup> C)                    | UCB1RXIFG2 (I <sup>2</sup> C)                    | UCB2RXIFG2 (I <sup>2</sup> C)                    | UCB3RXIFG2 (I <sup>2</sup> C)                    |
| 23             | UCB0TXIFG2 (I <sup>2</sup> C)                    | UCB0TXIFG2 (I <sup>2</sup> C)                    | UCB0TXIFG2 (I <sup>2</sup> C)                    | UCB1TXIFG2 (I <sup>2</sup> C)                    | UCB2TXIFG2 (I <sup>2</sup> C)                    | UCB3TXIFG2 (I <sup>2</sup> C)                    |
| 24             | UCB0RXIFG3 (I <sup>2</sup> C)                    | UCB0RXIFG3 (I <sup>2</sup> C)                    | UCB0RXIFG3 (I <sup>2</sup> C)                    | UCB1RXIFG3 (I <sup>2</sup> C)                    | UCB2RXIFG3 (I <sup>2</sup> C)                    | UCB3RXIFG3 (I <sup>2</sup> C)                    |
| 25             | UCB0TXIFG3 (I <sup>2</sup> C)                    | UCB0TXIFG3 (I <sup>2</sup> C)                    | UCB0TXIFG3 (I <sup>2</sup> C)                    | UCB1TXIFG3 (I <sup>2</sup> C)                    | UCB2TXIFG3 (I <sup>2</sup> C)                    | UCB3TXIFG3 (I <sup>2</sup> C)                    |
| 26             | ADC12 end of conversion                          | ADC12 end of conversion                          | ADC12 end of conversion                          | ADC12 end of conversion                          | ADC12 end of conversion                          | ADC12 end of conversion                          |
| 27             | LEA ready <sup>(2)</sup>                         | LEA ready <sup>(2)</sup>                         | LEA ready <sup>(2)</sup>                         | LEA ready <sup>(2)</sup>                         | LEA ready <sup>(2)</sup>                         | LEA ready <sup>(2)</sup>                         |

**Table 9-11. DMA Trigger Assignments (continued)**

| TRIGGER<br>(1) | CHANNEL 0 | CHANNEL 1 | CHANNEL 2 | CHANNEL 3 | CHANNEL 4 | CHANNEL 5 |
|----------------|-----------|-----------|-----------|-----------|-----------|-----------|
| 28             | Reserved  | Reserved  | Reserved  | Reserved  | Reserved  | Reserved  |
| 29             | MPY ready | MPY ready | MPY ready | MPY ready | MPY ready | MPY ready |
| 30             | DMA2IFG   | DMA0IFG   | DMA1IFG   | DMA5IFG   | DMA3IFG   | DMA4IFG   |
| 31             | DMAE0     | DMAE0     | DMAE0     | DMAE0     | DMAE0     | DMAE0     |

(1) If a reserved trigger source is selected, no trigger is generated.

(2) Reserved on MSP430FR596x.

### 9.12.9 Enhanced Universal Serial Communication Interface (eUSCI)

The eUSCI modules are used for serial data communication. The eUSCI module supports synchronous communication protocols such as SPI (3 pin or 4 pin) and I<sup>2</sup>C, and asynchronous communication protocols such as UART, enhanced UART with automatic baud-rate detection, and IrDA.

The eUSCI\_An module provides support for SPI (3 pin or 4 pin), UART, enhanced UART, and IrDA.

The eUSCI\_Bn module provides support for SPI (3 pin or 4 pin) and I<sup>2</sup>C.

Up to four eUSCI\_A modules and up to four eUSCI\_B modules are implemented. See [Table 9-68](#) through [Table 9-75](#) for control and configuration registers.

### 9.12.10 TA0, TA1, and TA4

TA0, TA1, and TA4 are 16-bit timers and counters (Timer\_A type) with three (TA0 and TA1) or two (TA4) capture/compare registers each. Each timer can support multiple captures or compares, PWM outputs, and interval timing (see [Table 9-12](#), [Table 9-13](#), and [Table 9-14](#)). Each timer has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers. See [Table 9-57](#), [Table 9-58](#), and [Table 9-76](#) for control and configuration registers.

**Table 9-12. TA0 Signal Connections**

| INPUT PORT PIN | DEVICE INPUT SIGNAL        | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PORT PIN                                   |
|----------------|----------------------------|---------------------|--------------|----------------------|----------------------|---------------------------------------------------|
| P1.2           | TA0CLK                     | TACLK               | Timer        | N/A                  | N/A                  |                                                   |
|                | ACLK (internal)            | ACLK                |              |                      |                      |                                                   |
|                | SMCLK (internal)           | SMCLK               |              |                      |                      |                                                   |
| P1.2           | $\overline{\text{TA0CLK}}$ | INCLK               |              |                      |                      |                                                   |
| P1.6           | TA0.0                      | CC10A               | CCR0         | TA0                  | TA0.0                | P1.6                                              |
| P2.3           | TA0.0                      | CC10B               |              |                      |                      | P2.3                                              |
|                | DVSS                       | GND                 |              |                      |                      |                                                   |
|                | DVCC                       | V <sub>CC</sub>     |              |                      |                      |                                                   |
| P1.0           | TA0.1                      | CC11A               | CCR1         | TA1                  | TA0.1                | P1.0                                              |
|                | COUT (internal)            | CC11B               |              |                      |                      | ADC12(internal) <sup>(1)</sup><br>ADC12SHSx = {1} |
|                | DVSS                       | GND                 |              |                      |                      |                                                   |
|                | DVCC                       | V <sub>CC</sub>     |              |                      |                      |                                                   |
| P1.1           | TA0.2                      | CC12A               | CCR2         | TA2                  | TA0.2                | P1.1                                              |
|                | ACLK (internal)            | CC12B               |              |                      |                      |                                                   |
|                | DVSS                       | GND                 |              |                      |                      |                                                   |
|                | DVCC                       | V <sub>CC</sub>     |              |                      |                      |                                                   |

(1) Only on devices with ADC

**Table 9-13. TA1 Signal Connections**

| INPUT PORT PIN | DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PORT PIN                                   |
|----------------|---------------------|---------------------|--------------|----------------------|----------------------|---------------------------------------------------|
| P1.1           | TA1CLK              | TACLK               | Timer        | N/A                  | N/A                  |                                                   |
|                | ACLK (internal)     | ACLK                |              |                      |                      |                                                   |
|                | SMCLK (internal)    | SMCLK               |              |                      |                      |                                                   |
| P1.1           | TA1CLK              | INCLK               |              |                      |                      |                                                   |
| P1.7           | TA1.0               | CCI0A               | CCR0         | TA0                  | TA1.0                | P1.7                                              |
| P2.4           | TA1.0               | CCI0B               |              |                      |                      | P2.4                                              |
|                | DVSS                | GND                 |              |                      |                      |                                                   |
|                | DVCC                | V <sub>CC</sub>     |              |                      |                      |                                                   |
| P1.2           | TA1.1               | CCI1A               | CCR1         | TA1                  | TA1.1                | P1.2                                              |
|                | COUT (internal)     | CCI1B               |              |                      |                      | ADC12(internal) <sup>(1)</sup><br>ADC12SHSx = {4} |
|                | DVSS                | GND                 |              |                      |                      |                                                   |
|                | DVCC                | V <sub>CC</sub>     |              |                      |                      |                                                   |
| P1.3           | TA1.2               | CCI2A               | CCR2         | TA2                  | TA1.2                | P1.3                                              |
|                | ACLK (internal)     | CCI2B               |              |                      |                      |                                                   |
|                | DVSS                | GND                 |              |                      |                      |                                                   |
|                | DVCC                | V <sub>CC</sub>     |              |                      |                      |                                                   |

(1) Only on devices with ADC

**Table 9-14. TA4 Signal Connections**

| INPUT PORT PIN | DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PORT PIN                                   |
|----------------|---------------------|---------------------|--------------|----------------------|----------------------|---------------------------------------------------|
| P5.2           | TA4CLK              | TACLK               | Timer        | N/A                  | N/A                  |                                                   |
|                | ACLK (internal)     | ACLK                |              |                      |                      |                                                   |
|                | SMCLK (internal)    | SMCLK               |              |                      |                      |                                                   |
| P5.2           | TA4CLK              | INCLK               |              |                      |                      |                                                   |
| P5.6           | TA4.0               | CCI0A               | CCR0         | TA0                  | TA4.0                |                                                   |
| P7.4           | TA4.0               | CCI0B               |              |                      |                      |                                                   |
|                | DVSS                | GND                 |              |                      |                      |                                                   |
|                | DVCC                | V <sub>CC</sub>     |              |                      |                      |                                                   |
| P5.7           | TA4.1               | CCI1A               | CCR1         | TA1                  | TA4.1                |                                                   |
| P7.3           | TA4.1               | CCI1B               |              |                      |                      | ADC12(internal) <sup>(1)</sup><br>ADC12SHSx = {7} |
|                | DVSS                | GND                 |              |                      |                      |                                                   |
|                | DVCC                | V <sub>CC</sub>     |              |                      |                      |                                                   |

### 9.12.11 TA2 and TA3

TA2 and TA3 are 16-bit timers and counters (Timer\_A type) with two capture/compare registers each and with internal connections only. Each timer can support multiple captures or compares, PWM outputs, and interval timing (see [Table 9-15](#) and [Table 9-16](#)). Each timer has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers. See [Table 9-60](#) and [Table 9-62](#) for control and configuration registers.

**Table 9-15. TA2 Signal Connections**

| DEVICE INPUT SIGNAL                    | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL                              |
|----------------------------------------|-------------------|--------------|----------------------|---------------------------------------------------|
| COUT (internal)                        | TACLK             | Timer        | N/A                  |                                                   |
| ACLK (internal)                        | ACLK              |              |                      |                                                   |
| SMCLK (internal)                       | SMCLK             |              |                      |                                                   |
| From Capacitive Touch I/O 0 (internal) | INCLK             |              |                      |                                                   |
| TA3 CCR0 output (internal)             | CCI0A             | CCR0         | TA0                  | TA3 CCI0A input                                   |
| ACLK (internal)                        | CCI0B             |              |                      |                                                   |
| DVSS                                   | GND               |              |                      |                                                   |
| DVCC                                   | V <sub>CC</sub>   |              |                      |                                                   |
| From Capacitive Touch I/O 0 (internal) | CCI1A             | CCR1         | TA1                  | ADC12(internal) <sup>(1)</sup><br>ADC12SHSx = {5} |
| COUT (internal)                        | CCI1B             |              |                      |                                                   |
| DVSS                                   | GND               |              |                      |                                                   |
| DVCC                                   | V <sub>CC</sub>   |              |                      |                                                   |

(1) Only on devices with ADC

**Table 9-16. TA3 Signal Connections**

| DEVICE INPUT SIGNAL                    | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL                              |
|----------------------------------------|-------------------|--------------|----------------------|---------------------------------------------------|
| COUT (internal)                        | TACLK             | Timer        | N/A                  |                                                   |
| ACLK (internal)                        | ACLK              |              |                      |                                                   |
| SMCLK (internal)                       | SMCLK             |              |                      |                                                   |
| From Capacitive Touch I/O 1 (internal) | INCLK             |              |                      |                                                   |
| TA2 CCR0 output (internal)             | CCI0A             | CCR0         | TA0                  | TA2 CCI0A input                                   |
| ACLK (internal)                        | CCI0B             |              |                      |                                                   |
| DVSS                                   | GND               |              |                      |                                                   |
| DVCC                                   | V <sub>CC</sub>   |              |                      |                                                   |
| From Capacitive Touch I/O 1 (internal) | CCI1A             | CCR1         | TA1                  | ADC12(internal) <sup>(1)</sup><br>ADC12SHSx = {6} |
| COUT (internal)                        | CCI1B             |              |                      |                                                   |
| DVSS                                   | GND               |              |                      |                                                   |
| DVCC                                   | V <sub>CC</sub>   |              |                      |                                                   |

(1) Only on devices with ADC

## 9.12.12 TB0

TB0 is a 16-bit timer and counter (Timer\_B type) with seven capture/compare registers. TB0 can support multiple captures or compares, PWM outputs, and interval timing (see [Table 9-17](#)). TB0 has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers. See [Table 9-59](#) for control and configuration registers.

**Table 9-17. TB0 Signal Connections**

| INPUT PORT PIN | DEVICE INPUT SIGNAL         | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PORT PIN                                    |
|----------------|-----------------------------|---------------------|--------------|----------------------|----------------------|----------------------------------------------------|
| P2.0           | TB0CLK                      | TBCLK               | Timer        | N/A                  | N/A                  |                                                    |
|                | ACLK (internal)             | ACLK                |              |                      |                      |                                                    |
|                | SMCLK (internal)            | SMCLK               |              |                      |                      |                                                    |
| P2.0           | $\overline{\text{TB0CLK}}$  | INCLK               |              |                      |                      |                                                    |
| P2.1           | TB0.0                       | CCI0A               | CCR0         | TB0                  | TB0.0                | P2.1                                               |
| P2.5           | TB0.0                       | CCI0B               |              |                      |                      | P2.5                                               |
|                | DVSS                        | GND                 |              |                      |                      | ADC12 (internal) <sup>(1)</sup><br>ADC12SHSx = {2} |
|                | DVCC                        | V <sub>CC</sub>     |              |                      |                      |                                                    |
| P1.4           | TB0.1                       | CCI1A               | CCR1         | TB1                  | TB0.1                | P1.4                                               |
|                | COU <sub>T</sub> (internal) | CCI1B               |              |                      |                      | P2.6                                               |
|                | DVSS                        | GND                 |              |                      |                      | ADC12 (internal) <sup>(1)</sup><br>ADC12SHSx = {3} |
|                | DVCC                        | V <sub>CC</sub>     |              |                      |                      |                                                    |
| P1.5           | TB0.2                       | CCI2A               | CCR2         | TB2                  | TB0.2                | P1.5                                               |
|                | ACLK (internal)             | CCI2B               |              |                      |                      | P2.2                                               |
|                | DVSS                        | GND                 |              |                      |                      |                                                    |
|                | DVCC                        | V <sub>CC</sub>     |              |                      |                      |                                                    |
| P3.4           | TB0.3                       | CCI3A               | CCR3         | TB3                  | TB0.3                | P3.4                                               |
| P1.6           | TB0.3                       | CCI3B               |              |                      |                      | P1.6                                               |
|                | DVSS                        | GND                 |              |                      |                      |                                                    |
|                | DVCC                        | V <sub>CC</sub>     |              |                      |                      |                                                    |
| P3.5           | TB0.4                       | CCI4A               | CCR4         | TB4                  | TB0.4                | P3.5                                               |
| P1.7           | TB0.4                       | CCI4B               |              |                      |                      | P1.7                                               |
|                | DVSS                        | GND                 |              |                      |                      |                                                    |
|                | DVCC                        | V <sub>CC</sub>     |              |                      |                      |                                                    |
| P3.6           | TB0.5                       | CCI5A               | CCR5         | TB5                  | TB0.5                | P3.6                                               |
| P4.4           | TB0.5                       | CCI5B               |              |                      |                      | P4.4                                               |
|                | DVSS                        | GND                 |              |                      |                      |                                                    |
|                | DVCC                        | V <sub>CC</sub>     |              |                      |                      |                                                    |
| P3.7           | TB0.6                       | CCI6A               | CCR6         | TB6                  | TB0.6                | P3.7                                               |
| P2.0           | TB0.6                       | CCI6B               |              |                      |                      | P2.0                                               |
|                | DVSS                        | GND                 |              |                      |                      |                                                    |
|                | DVCC                        | V <sub>CC</sub>     |              |                      |                      |                                                    |

(1) Only on devices with ADC

### 9.12.13 ADC12\_B

The ADC12\_B module supports fast 12-bit analog-to-digital conversions with differential and single-ended inputs. The module implements a 12-bit SAR core, sample select control, a reference generator, and a conversion result buffer. A window comparator with lower and upper limits allows CPU-independent result monitoring with three window comparator interrupt flags. See [Table 9-77](#) for control and configuration registers.

[Table 9-18](#) summarizes the available external trigger sources.

[Table 9-19](#) lists the available multiplexing between internal and external analog inputs.

**Table 9-18. ADC12\_B Trigger Signal Connections**

| ADC12SHSx |         | CONNECTED TRIGGER SOURCE |
|-----------|---------|--------------------------|
| BINARY    | DECIMAL |                          |
| 000       | 0       | Software (ADC12SC)       |
| 001       | 1       | TA0 CCR1 output          |
| 010       | 2       | TB0 CCR0 output          |
| 011       | 3       | TB0 CCR1 output          |
| 100       | 4       | TA1 CCR1 output          |
| 101       | 5       | TA2 CCR1 output          |
| 110       | 6       | TA3 CCR1 output          |
| 111       | 7       | TA4 CCR1 output          |

**Table 9-19. ADC12\_B External and Internal Signal Mapping**

| CONTROL BIT IN ADC12CTL3 REGISTER | EXTERNAL ADC INPUT (CONTROL BIT = 0) | INTERNAL ADC INPUT (CONTROL BIT = 1) |
|-----------------------------------|--------------------------------------|--------------------------------------|
| ADC12BATMAP                       | A31                                  | Battery monitor                      |
| ADC12TCMAP                        | A30                                  | Temperature sensor                   |
| ADC12CH0MAP                       | A29                                  | N/A <sup>(1)</sup>                   |
| ADC12CH1MAP                       | A28                                  | N/A <sup>(1)</sup>                   |
| ADC12CH2MAP                       | A27                                  | N/A <sup>(1)</sup>                   |
| ADC12CH3MAP                       | A26                                  | N/A <sup>(1)</sup>                   |

(1) N/A = No internal signal is available on this device.

### 9.12.14 Comparator\_E

The primary function of the Comparator\_E module is to support precision slope analog-to-digital conversions, battery voltage supervision, and monitoring of external analog signals. See [Table 9-78](#) for control and configuration registers.

### 9.12.15 CRC16

The CRC16 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC16 module signature is based on the CRC-CCITT standard. See [Table 9-46](#) for control and configuration registers.

### 9.12.16 CRC32

The CRC32 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC32 signature is based on the ISO 3309 standard. See [Table 9-79](#) for control and configuration registers.

### 9.12.17 AES256 Accelerator

The AES accelerator module performs encryption and decryption of 128-bit data with 128-, 192-, or 256-bit keys according to the Advanced Encryption Standard (AES) (FIPS PUB 197) in hardware. See [Table 9-80](#) for control and configuration registers.

### 9.12.18 True Random Seed

The Device Descriptor Information (TLV) section contains a 128-bit true random seed that can be used to implement a deterministic random number generator.

### 9.12.19 Shared Reference (REF)

The REF module generates all critical reference voltages that can be used by the various analog peripherals in the device.

### 9.12.20 Embedded Emulation

#### 9.12.20.1 Embedded Emulation Module (EEM) (S Version)

The EEM supports real-time in-system debugging. The S version of the EEM has the following features:

- Three hardware triggers or breakpoints on memory access
- One hardware trigger or breakpoint on CPU register write access
- Up to four hardware triggers can be combined to form complex triggers or breakpoints
- One cycle counter
- Clock control on module level

#### 9.12.20.2 EnergyTrace++ Technology

The devices implement circuitry to support EnergyTrace++ technology. The EnergyTrace++ technology allows you to observe information about the internal states of the microcontroller. These states include the CPU program counter (PC), the ON or OFF status of the peripherals and the system clocks (regardless of the clock source), and the low-power mode currently in use. These states can always be read by a debug tool, even when the microcontroller sleeps in LPMx.5 modes.

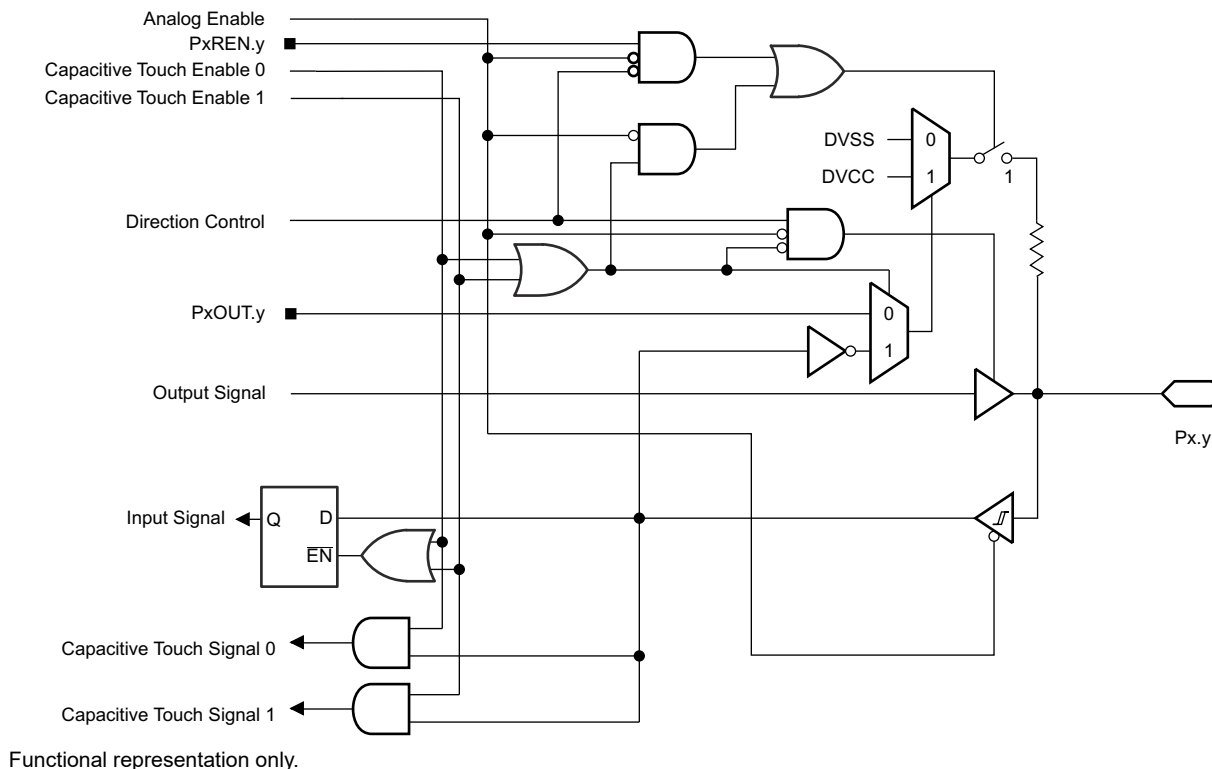
The activity of the following modules can be observed:

- LEA is running (MSP430FR599x only).
- MPY is calculating.
- WDT is counting.
- RTC is counting.
- ADC: a sequence, sample, or conversion is active.
- REF: REFBG or REFGEN active and BG in static mode.
- COMP is on.
- AES is encrypting or decrypting.
- eUSCI\_A0 is transferring (receiving or transmitting) data.
- eUSCI\_A1 is transferring (receiving or transmitting) data.
- eUSCI\_A2 is transferring (receiving or transmitting) data.
- eUSCI\_A3 is transferring (receiving or transmitting) data.
- eUSCI\_B0 is transferring (receiving or transmitting) data.
- eUSCI\_B1 is transferring (receiving or transmitting) data.
- eUSCI\_B2 is transferring (receiving or transmitting) data.
- eUSCI\_B3 is transferring (receiving or transmitting) data.
- TB0 is counting.
- TA0 is counting.
- TA1 is counting.
- TA2 is counting.
- TA3 is counting.
- TA4 is counting.

## 9.13 Input/Output Diagrams

### 9.13.1 Capacitive Touch Functionality on Ports P1 to P8, and PJ

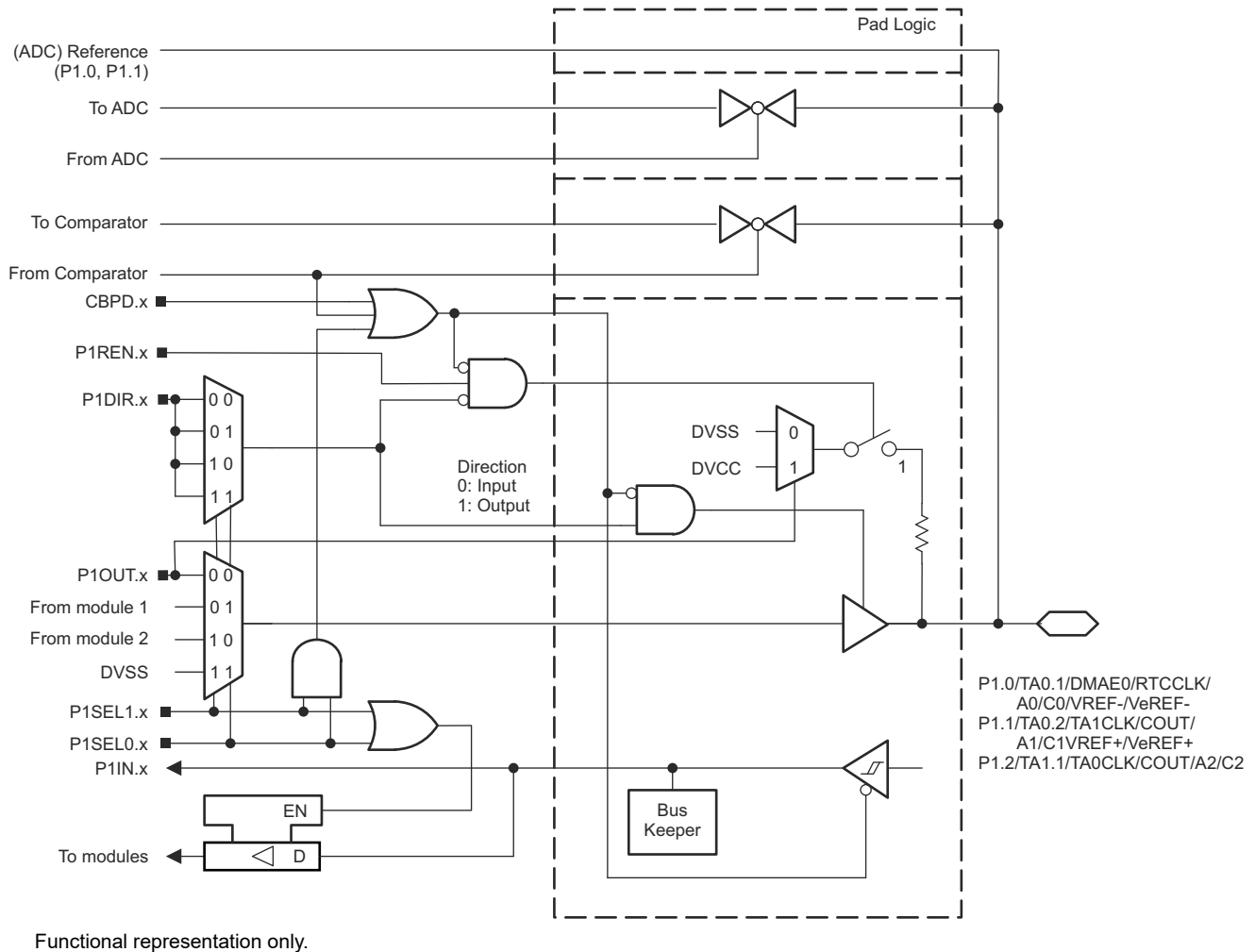
All port pins provide the Capacitive Touch functionality (see [Figure 9-2](#)). The Capacitive Touch functionality is controlled using the Capacitive Touch I/O control registers CAPTIO0CTL and CAPTIO1CTL as described in the [MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx Family User's Guide](#). The Capacitive Touch functionality is not shown in the individual pin schematics in the following sections.



**Figure 9-2. Capacitive Touch Functionality on Ports**

### 9.13.2 Port P1 (P1.0 to P1.2) Input/Output With Schmitt Trigger

Figure 9-3 shows the port diagram. Table 9-20 summarizes the selection of the pin functions.



**Figure 9-3. Port P1 (P1.0 to P1.2) Diagram**

**Table 9-20. Port P1 (P1.0 to P1.2) Pin Functions**

| PIN NAME (P1.x)                                | x | FUNCTION                                 | CONTROL BITS AND SIGNALS <sup>(1)</sup> |          |          |
|------------------------------------------------|---|------------------------------------------|-----------------------------------------|----------|----------|
|                                                |   |                                          | P1DIR.x                                 | P1SEL1.x | P1SEL0.x |
| P1.0/TA0.1/DMAE0/RTCCLK/A0/C0/<br>VREF-/VeREF- | 0 | P1.0 (I/O)                               | 0 = Input,<br>1 = Output                | 0        | 0        |
|                                                |   | TA0.CCI1A                                | 0                                       | 0        | 1        |
|                                                |   | TA0.1                                    | 1                                       |          |          |
|                                                |   | DMAE0                                    | 0                                       | 1        | 0        |
|                                                |   | RTCCLK <sup>(4)</sup>                    | 1                                       |          |          |
|                                                |   | A0, C0, VREF-, VeREF- <sup>(2) (3)</sup> | X                                       | 1        | 1        |
| P1.1/TA0.2/TA1CLK/COUT/A1/C1/ VREF<br>+/VeREF+ | 1 | P1.1 (I/O)                               | 0 = Input,<br>1 = Output                | 0        | 0        |
|                                                |   | TA0.CCI2A                                | 0                                       | 0        | 1        |
|                                                |   | TA0.2                                    | 1                                       |          |          |
|                                                |   | TA1CLK                                   | 0                                       | 1        | 0        |
|                                                |   | COUT <sup>(5)</sup>                      | 1                                       |          |          |
|                                                |   | A1, C1, VREF+, VeREF+ <sup>(2) (3)</sup> | X                                       | 1        | 1        |
| P1.2/TA1.1/TA0CLK/COUT/A2/C2                   | 2 | P1.2 (I/O)                               | 0 = Input,<br>1 = Output                | 0        | 0        |
|                                                |   | TA1.CCI1A                                | 0                                       | 0        | 1        |
|                                                |   | TA1.1                                    | 1                                       |          |          |
|                                                |   | TA0CLK                                   | 0                                       | 1        | 0        |
|                                                |   | COUT <sup>(5)</sup>                      | 1                                       |          |          |
|                                                |   | A2, C2 <sup>(2) (3)</sup>                | X                                       | 1        | 1        |

(1) X = Don't care

(2) Setting P1SEL1.x and P1SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

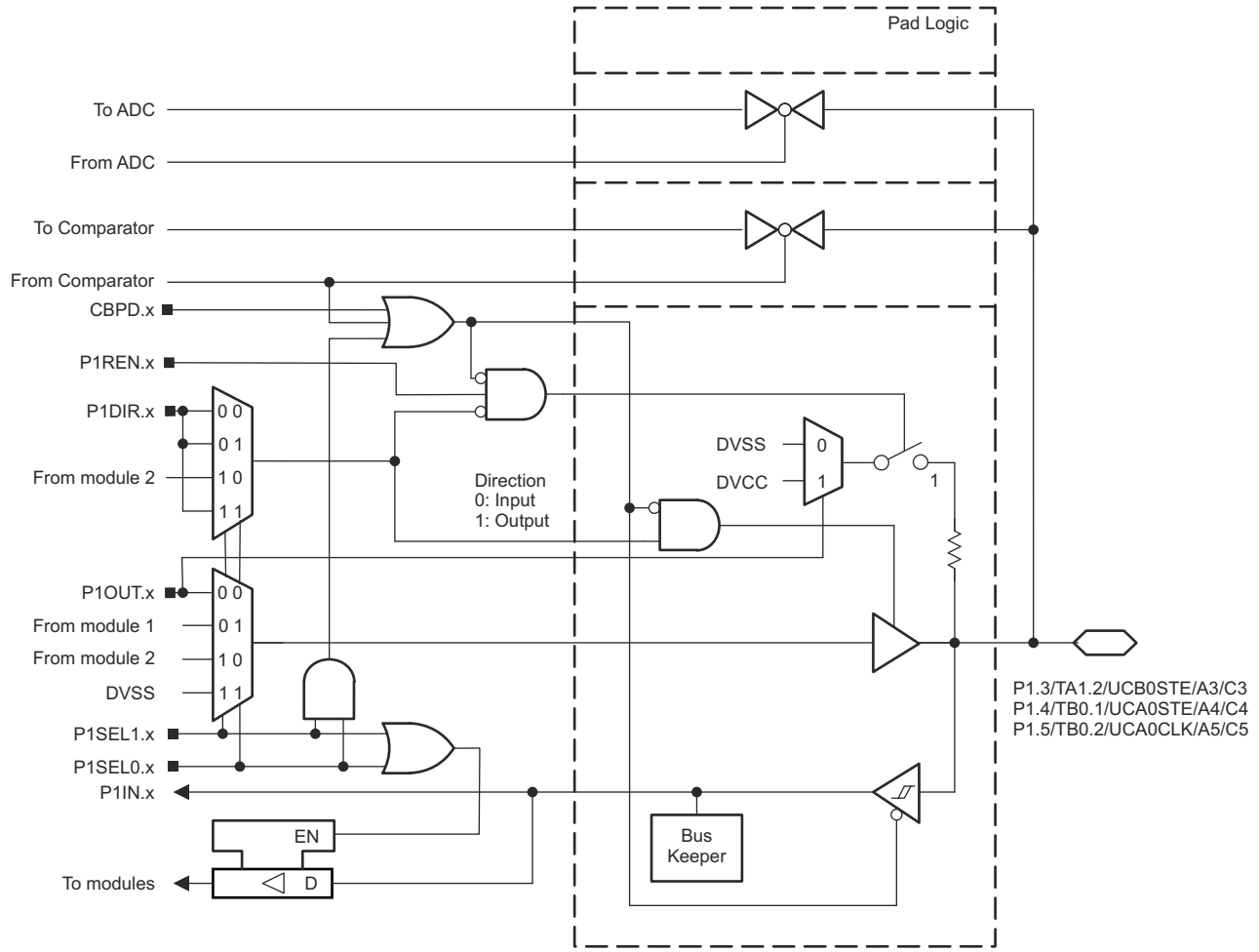
(3) Setting the CEPDx bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the Cx input pin to the comparator multiplexer with the input select bits in the comparator module automatically disables output driver and input buffer for that pin, regardless of the state of the associated CEPDx bit.

(4) Do not use this pin as RTCCLK output if the DMAE0 functionality is used on any other pin. Select an alternate RTCCLK output pin.

(5) Do not use this pin as COUT output if the TA1CLK functionality is used on any other pin. Select an alternate COUT output pin.

### 9.13.3 Port P1 (P1.3 to P1.5) Input/Output With Schmitt Trigger

Figure 9-4 shows the port diagram. Table 9-21 summarizes the selection of the pin functions.



Functional representation only.

**Figure 9-4. Port P1 (P1.3 to P1.5) Diagram**

**Table 9-21. Port P1 (P1.3 to P1.5) Pin Functions**

| PIN NAME (P1.x)          | x | FUNCTION                  | CONTROL BITS AND SIGNALS <sup>(1)</sup> |          |          |
|--------------------------|---|---------------------------|-----------------------------------------|----------|----------|
|                          |   |                           | P1DIR.x                                 | P1SEL1.x | P1SEL0.x |
| P1.3/TA1.2/UCB0STE/A3/C3 | 3 | P1.3 (I/O)                | 0 = Input,<br>1 = Output                | 0        | 0        |
|                          |   | TA1.CCI2A                 | 0                                       | 0        | 1        |
|                          |   | TA1.2                     | 1                                       |          |          |
|                          |   | UCB0STE                   | X <sup>(2)</sup>                        | 1        | 0        |
|                          |   | A3, C3 <sup>(4) (5)</sup> | X                                       | 1        | 1        |
| P1.4/TB0.1/UCA0STE/A4/C4 | 4 | P1.4 (I/O)                | 0 = Input,<br>1 = Output                | 0        | 0        |
|                          |   | TB0.CCI1A                 | 0                                       | 0        | 1        |
|                          |   | TB0.1                     | 1                                       |          |          |
|                          |   | UCA0STE                   | X <sup>(3)</sup>                        | 1        | 0        |
|                          |   | A4, C4 <sup>(4) (5)</sup> | X                                       | 1        | 1        |
| P1.5/TB0.2/UCA0CLK/A5/C5 | 5 | P1.5 (I/O)                | 0 = Input,<br>1 = Output                | 0        | 0        |
|                          |   | TB0.CCI2A                 | 0                                       | 0        | 1        |
|                          |   | TB0.2                     | 1                                       |          |          |
|                          |   | UCA0CLK                   | X <sup>(3)</sup>                        | 1        | 0        |
|                          |   | A5, C5 <sup>(4) (5)</sup> | X                                       | 1        | 1        |

(1) X = Don't care

(2) Direction controlled by eUSCI\_B0 module.

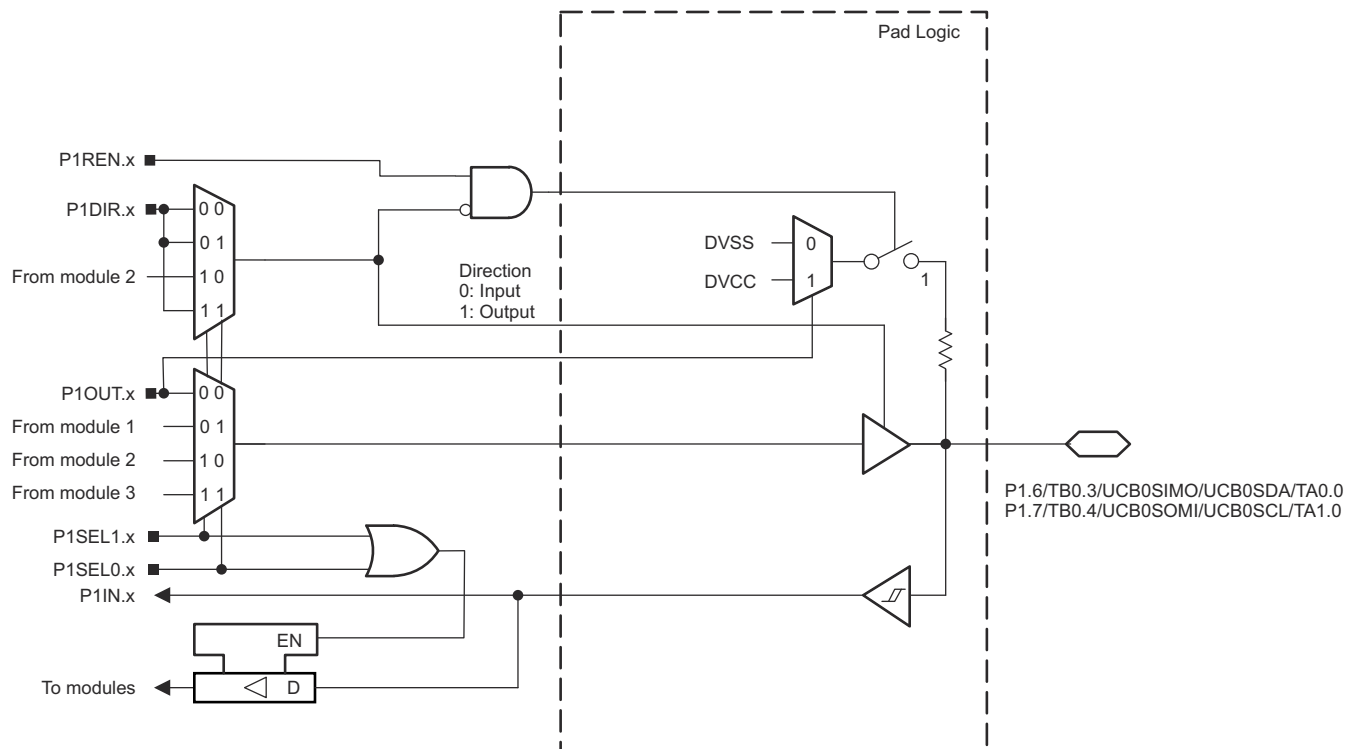
(3) Direction controlled by eUSCI\_A0 module.

(4) Setting P1SEL1.x and P1SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

(5) Setting the CEPDx bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the Cx input pin to the comparator multiplexer with the input select bits in the comparator module automatically disables output driver and input buffer for that pin, regardless of the state of the associated CEPDx bit.

### 9.13.4 Port P1 (P1.6 and P1.7) Input/Output With Schmitt Trigger

Figure 9-5 shows the port diagram. Table 9-22 summarizes the selection of the pin functions.



Functional representation only.

**Figure 9-5. Port P1 (P1.6 and P1.7) Diagram**

**Table 9-22. Port P1 (P1.6 and P1.7) Pin Functions**

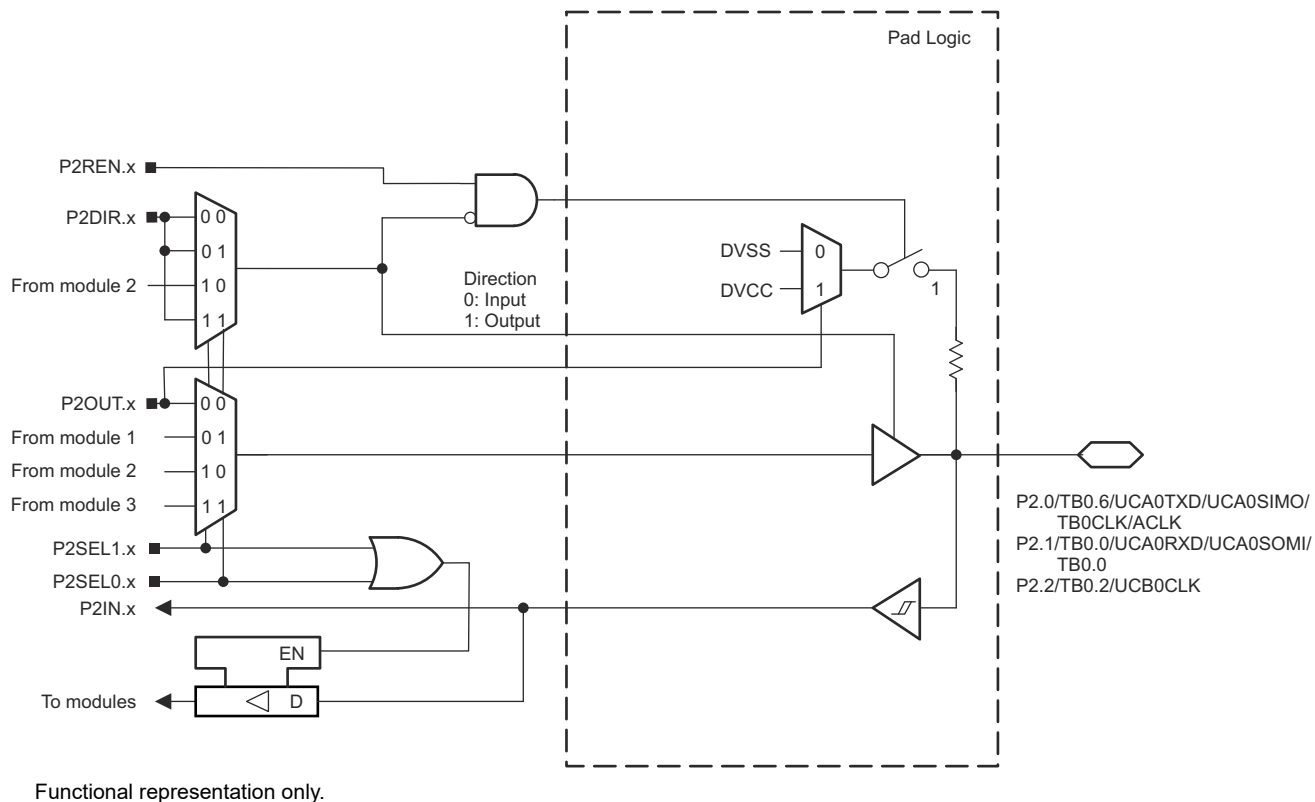
| PIN NAME (P1.x)                   | x | FUNCTION         | CONTROL BITS AND SIGNALS <sup>(1)</sup> |          |          |
|-----------------------------------|---|------------------|-----------------------------------------|----------|----------|
|                                   |   |                  | P1DIR.x                                 | P1SEL1.x | P1SEL0.x |
| P1.6/TB0.3/UCB0SIMO/UCB0SDA/TA0.0 | 6 | P1.6 (I/O)       | 0 = Input,<br>1 = Output                | 0        | 0        |
|                                   |   | TB0.CCI3B        | 0                                       | 0        | 1        |
|                                   |   | TB0.3            | 1                                       |          |          |
|                                   |   | UCB0SIMO/UCB0SDA | X <sup>(2)</sup>                        | 1        | 0        |
|                                   |   | TA0.CCI0A        | 0                                       | 1        | 1        |
|                                   |   | TA0.0            | 1                                       |          |          |
| P1.7/TB0.4/UCB0SOMI/UCB0SCL/TA1.0 | 7 | P1.7 (I/O)       | 0 = Input,<br>1 = Output                | 0        | 0        |
|                                   |   | TB0.CCI4B        | 0                                       | 0        | 1        |
|                                   |   | TB0.4            | 1                                       |          |          |
|                                   |   | UCB0SOMI/UCB0SCL | X <sup>(2)</sup>                        | 1        | 0        |
|                                   |   | TA1.CCI0A        | 0                                       | 1        | 1        |
|                                   |   | TA1.0            | 1                                       |          |          |

(1) X = Don't care

(2) Direction controlled by eUSCI\_B0 module.

### 9.13.5 Port P2 (P2.0 to P2.2) Input/Output With Schmitt Trigger

Figure 9-6 shows the port diagram. Table 9-23 summarizes the selection of the pin functions.



Functional representation only.

**Figure 9-6. Port P2 (P2.0 to P2.2) Diagram**

**Table 9-23. Port P2 (P2.0 to P2.2) Pin Functions**

| PIN NAME (P2.x)                             | x | FUNCTION                | CONTROL BITS AND SIGNALS <sup>(1)</sup> |          |          |
|---------------------------------------------|---|-------------------------|-----------------------------------------|----------|----------|
|                                             |   |                         | P2DIR.x                                 | P2SEL1.x | P2SEL0.x |
| P2.0/TB0.6/UCA0TXD/UCA0SIMO/<br>TB0CLK/ACLK | 0 | P2.0 (I/O)              | 0 = Input,<br>1 = Output                | 0        | 0        |
|                                             |   | TB0.CCI6B               | 0                                       | 0        | 1        |
|                                             |   | TB0.6                   | 1                                       |          |          |
|                                             |   | UCA0TXD/UCA0SIMO        | X <sup>(2)</sup>                        | 1        | 0        |
|                                             |   | TB0CLK                  | 0                                       | 1        | 1        |
|                                             |   | ACLK <sup>(4)</sup>     | 1                                       |          |          |
| P2.1/TB0.0/UCA0RXD/UCA0SOMI                 | 1 | P2.1 (I/O)              | 0 = Input,<br>1 = Output                | 0        | 0        |
|                                             |   | TB0.CCI0A               | 0                                       | X        | 1        |
|                                             |   | TB0.0                   | 1                                       |          |          |
|                                             |   | UCA0RXD/UCA0SOMI        | X <sup>(2)</sup>                        | 1        | 0        |
| P2.2/TB0.2/UCB0CLK                          | 2 | P2.2 (I/O)              | 0 = Input,<br>1 = Output                | 0        | 0        |
|                                             |   | N/A                     | 0                                       | 0        | 1        |
|                                             |   | TB0.2                   | 1                                       |          |          |
|                                             |   | UCB0CLK                 | X <sup>(3)</sup>                        | 1        | 0        |
|                                             |   | N/A                     | 0                                       | 1        | 1        |
|                                             |   | Internally tied to DVSS | 1                                       |          |          |

(1) X = Don't care

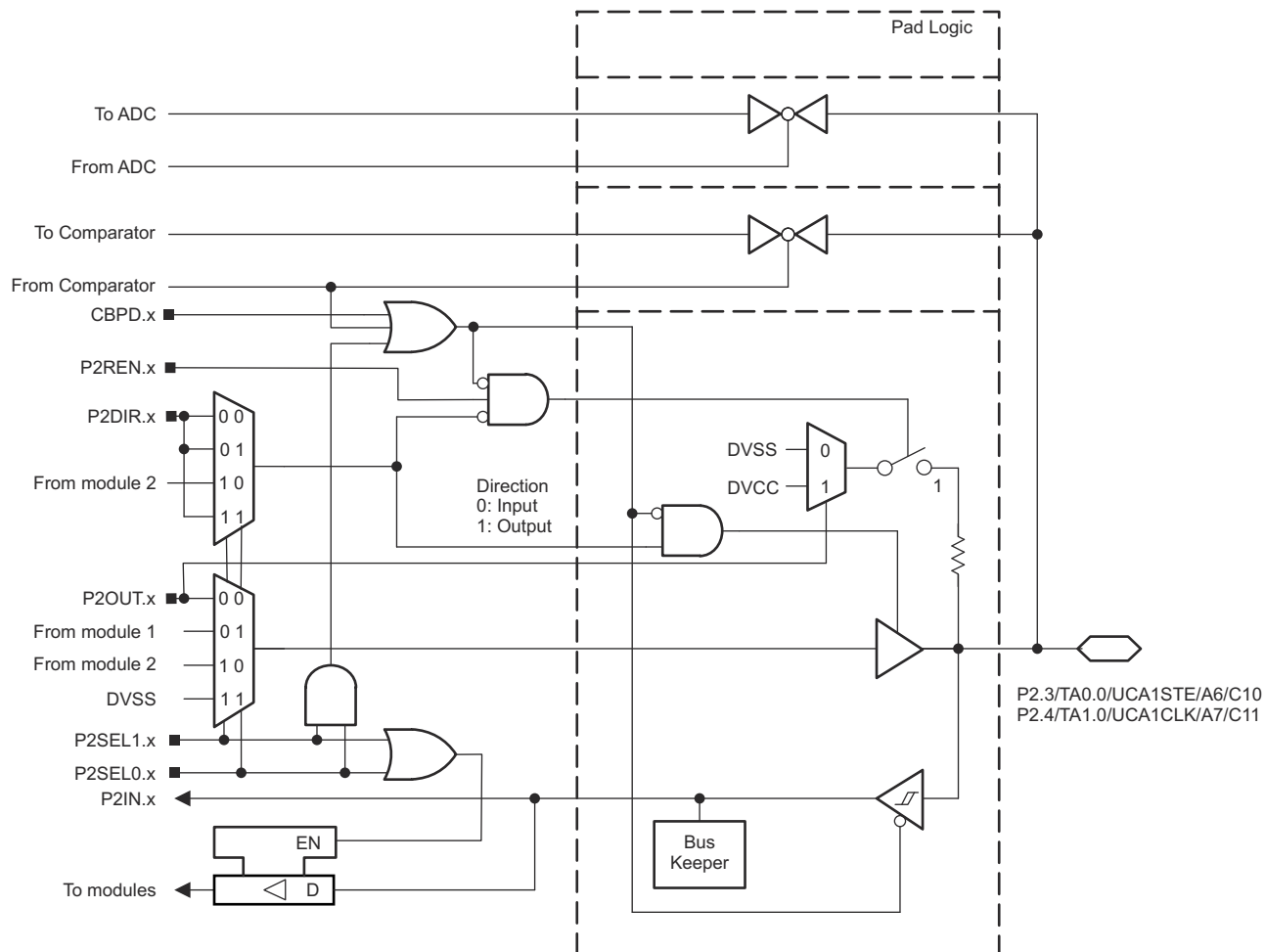
(2) Direction controlled by eUSCI\_A0 module.

(3) Direction controlled by eUSCI\_B0 module.

(4) Do not use this pin as ACLK output if the TB0CLK functionality is used on any other pin. Select an alternate ACLK output pin.

### 9.13.6 Port P2 (P2.3 and P2.4) Input/Output With Schmitt Trigger

Figure 9-7 shows the port diagram. Table 9-24 summarizes the selection of the pin functions.



Functional representation only.

**Figure 9-7. Port P2 (P2.3 and P2.4) Diagram**

**Table 9-24. Port P2 (P2.3 and P2.4) Pin Functions**

| PIN NAME (P2.x)           | x | FUNCTION                   | CONTROL BITS AND SIGNALS <sup>(1)</sup> |          |          |
|---------------------------|---|----------------------------|-----------------------------------------|----------|----------|
|                           |   |                            | P2DIR.x                                 | P2SEL1.x | P2SEL0.x |
| P2.3/TA0.0/UCA1STE/A6/C10 | 3 | P2.3 (I/O)                 | 0 = Input,<br>1 = Output                | 0        | 0        |
|                           |   | TA0.CCI0B                  | 0                                       | 0        | 1        |
|                           |   | TA0.0                      | 1                                       |          |          |
|                           |   | UCA1STE                    | X <sup>(2)</sup>                        | 1        | 0        |
|                           |   | A6, C10 <sup>(3) (4)</sup> | X                                       | 1        | 1        |
| P2.4/TA1.0/UCA1CLK/A7/C11 | 4 | P2.4 (I/O)                 | 0 = Input,<br>1 = Output                | 0        | 0        |
|                           |   | TA1.CCI0B                  | 0                                       | 0        | 1        |
|                           |   | TA1.0                      | 1                                       |          |          |
|                           |   | UCA1CLK                    | X <sup>(2)</sup>                        | 1        | 0        |
|                           |   | A7, C11 <sup>(3) (4)</sup> | X                                       | 1        | 1        |

(1) X = Don't care

(2) Direction controlled by eUSCI\_A1 module.

(3) Setting P2SEL1.x and P2SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

(4) Setting the CEPDx bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the Cx input pin to the comparator multiplexer with the input select bits in the comparator module automatically disables output driver and input buffer for that pin, regardless of the state of the associated CEPDx bit.

### 9.13.7 Port P2 (P2.5 and P2.6) Input/Output With Schmitt Trigger

Figure 9-8 shows the port diagram. Table 9-25 summarizes the selection of the pin functions.

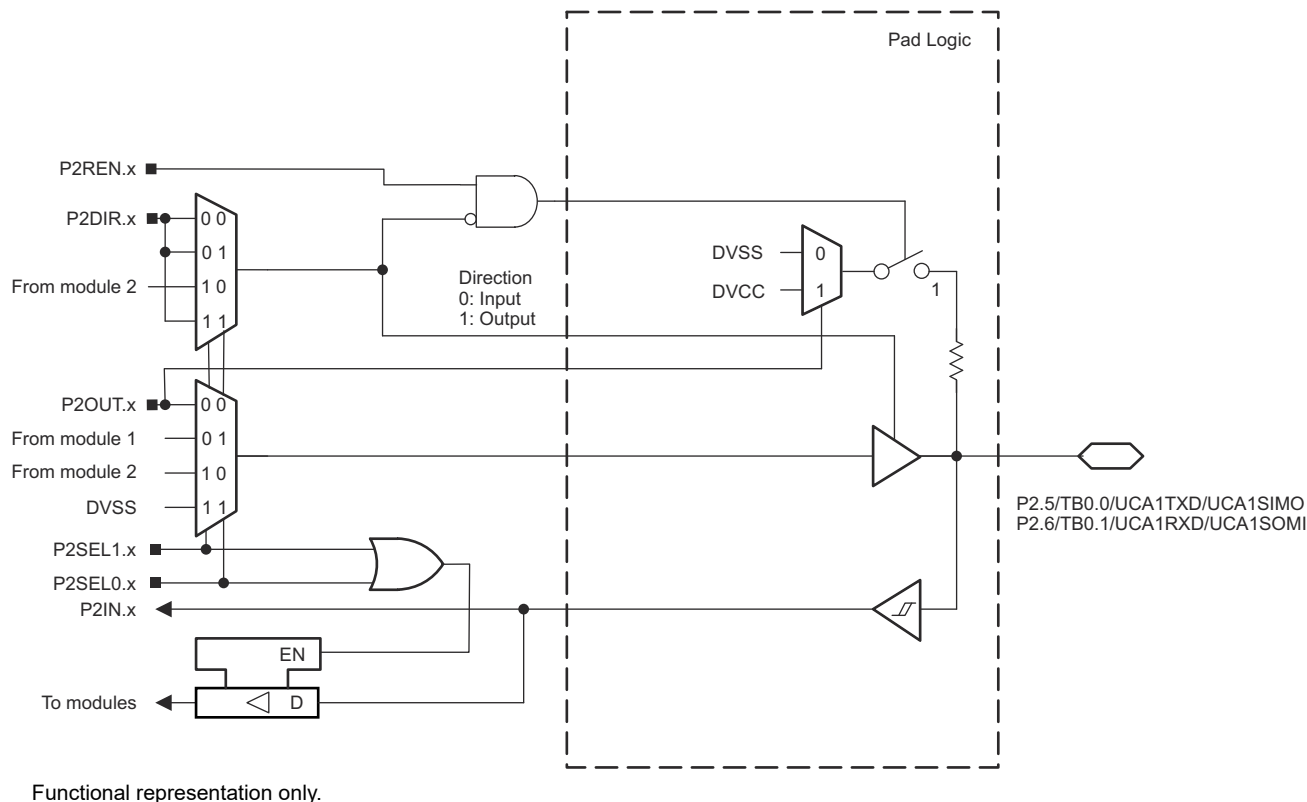


Figure 9-8. Port P2 (P2.5 and P2.6) Diagram

Table 9-25. Port P2 (P2.5 and P2.6) Pin Functions

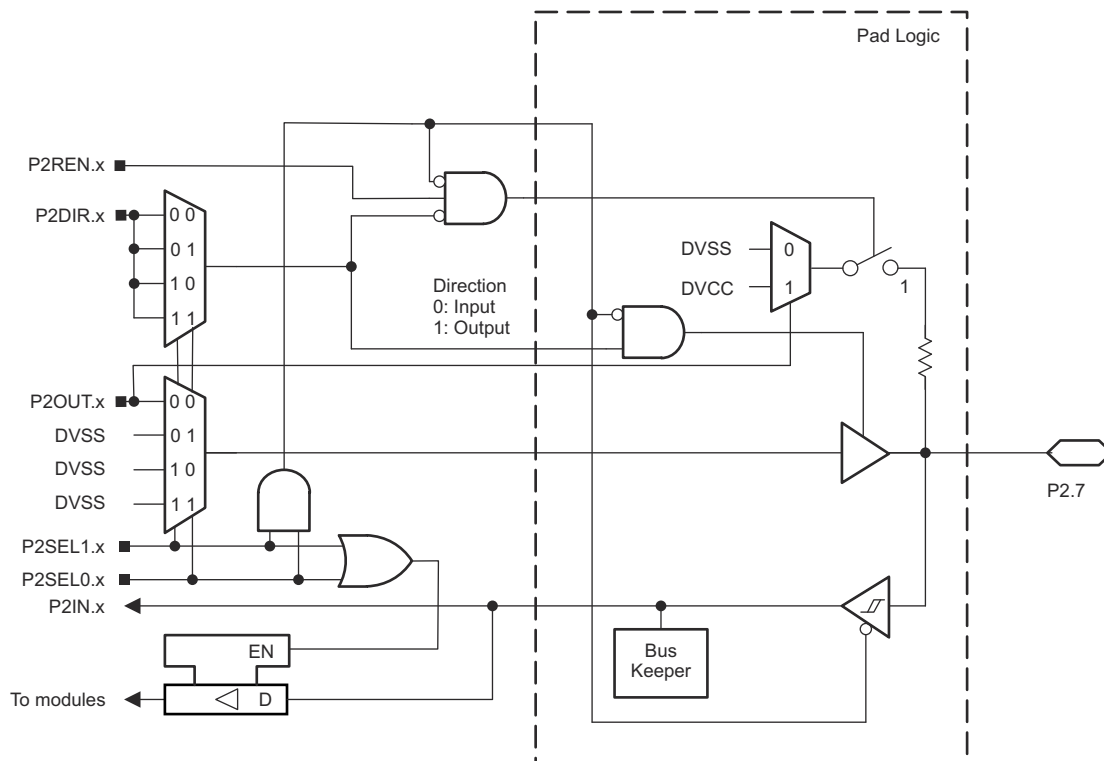
| PIN NAME (P2.x)             | x | FUNCTION                | CONTROL BITS AND SIGNALS <sup>(1)</sup> |          |          |
|-----------------------------|---|-------------------------|-----------------------------------------|----------|----------|
|                             |   |                         | P2DIR.x                                 | P2SEL1.x | P2SEL0.x |
| P2.5/TB0.0/UCA1TXD/UCA1SIMO | 5 | P2.5(I/O)               | 0 = Input,<br>1 = Output                | 0        | 0        |
|                             |   | TB0.CCI0B               | 0                                       | 0        | 1        |
|                             |   | TB0.0                   | 1                                       |          | 0        |
|                             |   | UCA1TXD/UCA1SIMO        | X <sup>(2)</sup>                        | 1        | 0        |
|                             |   | N/A                     | 0                                       | 1        | 1        |
|                             |   | Internally tied to DVSS | 1                                       |          | 1        |
| P2.6/TB0.1/UCA1RXD/UCA1SOMI | 6 | P2.6(I/O)               | 0 = Input,<br>1 = Output                | 0        | 0        |
|                             |   | N/A                     | 0                                       | 0        | 1        |
|                             |   | TB0.1                   | 1                                       |          | 0        |
|                             |   | UCA1RXD/UCA1SOMI        | X <sup>(2)</sup>                        | 1        | 0        |
|                             |   | N/A                     | 0                                       | 1        | 1        |
|                             |   | Internally tied to DVSS | 1                                       |          | 1        |

(1) X = Don't care

(2) Direction controlled by eUSCI\_A1 module.

### 9.13.8 Port P2 (P2.7) Input/Output With Schmitt Trigger

Figure 9-9 shows the port diagram. Table 9-26 summarizes the selection of the pin functions.



Functional representation only.

**Figure 9-9. Port P2 (P2.7) Diagram**

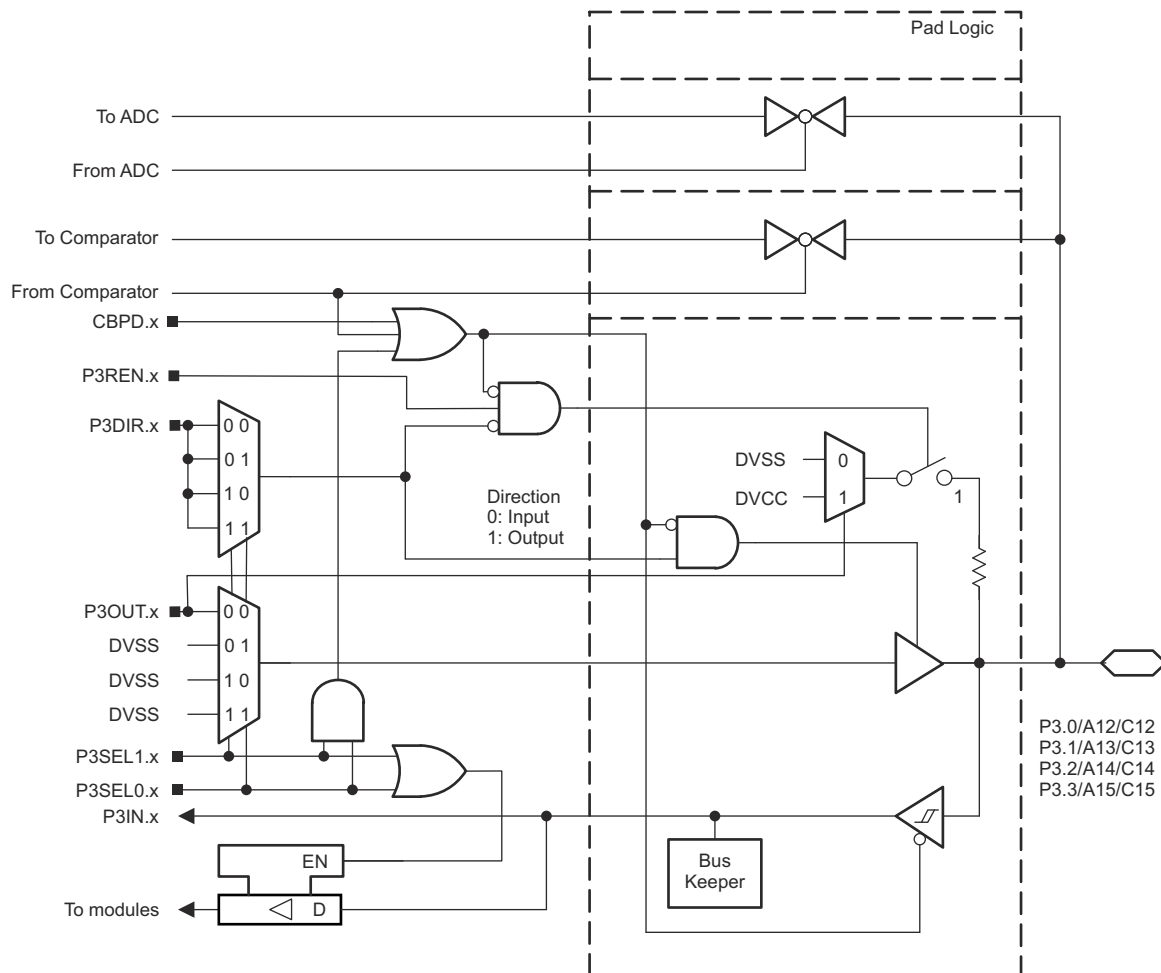
**Table 9-26. Port P2 (P2.7) Pin Functions**

| PIN NAME (P2.x) | x | FUNCTION                | CONTROL BITS AND SIGNALS <sup>(1)</sup> |          |          |
|-----------------|---|-------------------------|-----------------------------------------|----------|----------|
|                 |   |                         | P2DIR.x                                 | P2SEL1.x | P2SEL0.x |
| P2.7            | 7 | P2.7(I/O)               | 0 = Input,<br>1 = Output                | 0        | 0        |
|                 |   | N/A                     | 0                                       | 0        | 1        |
|                 |   | Internally tied to DVSS | 1                                       |          |          |
|                 |   | N/A                     | 0                                       | 1        | X        |
|                 |   | Internally tied to DVSS | 1                                       |          |          |

(1) X = Don't care

### 9.13.9 Port P3 (P3.0 to P3.3) Input/Output With Schmitt Trigger

Figure 9-10 shows the port diagram. Table 9-27 summarizes the selection of the pin functions.



Functional representation only.

**Figure 9-10. Port P3 (P3.0 to P3.3) Diagram**

**Table 9-27. Port P3 (P3.0 to P3.3) Pin Functions**

| PIN NAME (P3.x) | x | FUNCTION                   | CONTROL BITS AND SIGNALS <sup>(1)</sup> |          |          |
|-----------------|---|----------------------------|-----------------------------------------|----------|----------|
|                 |   |                            | P3DIR.x                                 | P3SEL1.x | P3SEL0.x |
| P3.0/A12/C12    | 0 | P3.0 (I/O)                 | 0 = Input,<br>1 = Output                | 0        | 0        |
|                 |   | N/A                        | 0                                       | 0        | 1        |
|                 |   | Internally tied to DVSS    | 1                                       |          |          |
|                 |   | N/A                        | 0                                       | 1        | 0        |
|                 |   | Internally tied to DVSS    | 1                                       |          |          |
|                 |   | A12/C12 <sup>(2) (3)</sup> | X                                       | 1        | 1        |
| P3.1/A13/C13    | 1 | P3.1 (I/O)                 | 0 = Input,<br>1 = Output                | 0        | 0        |
|                 |   | N/A                        | 0                                       | 0        | 1        |
|                 |   | Internally tied to DVSS    | 1                                       |          |          |
|                 |   | N/A                        | 0                                       | 1        | 0        |
|                 |   | Internally tied to DVSS    | 1                                       |          |          |
|                 |   | A13/C13 <sup>(2) (3)</sup> | X                                       | 1        | 1        |
| P3.2/A14/C14    | 2 | P3.2 (I/O)                 | 0 = Input,<br>1 = Output                | 0        | 0        |
|                 |   | N/A                        | 0                                       | 0        | 1        |
|                 |   | Internally tied to DVSS    | 1                                       |          |          |
|                 |   | N/A                        | 0                                       | 1        | 0        |
|                 |   | Internally tied to DVSS    | 1                                       |          |          |
|                 |   | A14/C14 <sup>(2) (3)</sup> | X                                       | 1        | 1        |
| P3.3/A15/C15    | 3 | P3.3 (I/O)                 | 0 = Input,<br>1 = Output                | 0        | 0        |
|                 |   | N/A                        | 0                                       | 0        | 1        |
|                 |   | Internally tied to DVSS    | 1                                       |          |          |
|                 |   | N/A                        | 0                                       | 1        | 0        |
|                 |   | Internally tied to DVSS    | 1                                       |          |          |
|                 |   | A15/C15 <sup>(2) (3)</sup> | X                                       | 1        | 1        |

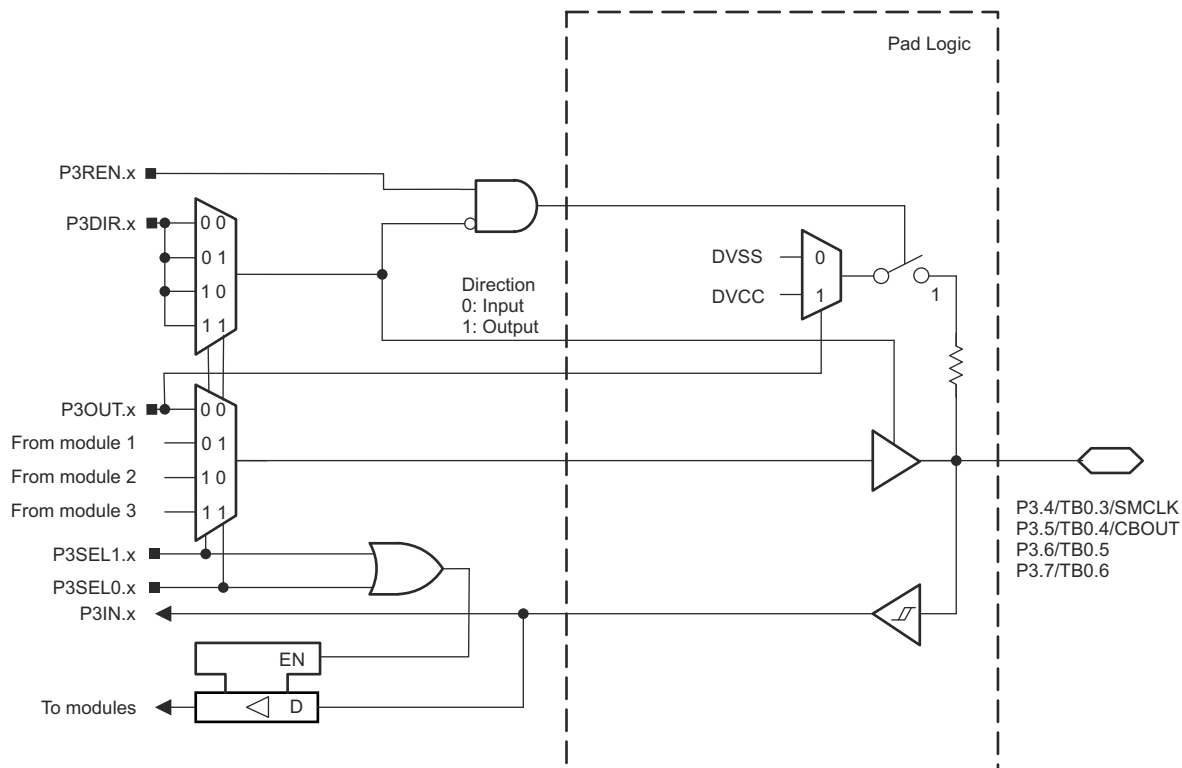
(1) X = Don't care

(2) Setting P3SEL1.x and P3SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

(3) Setting the CEPDx bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the Cx input pin to the comparator multiplexer with the input select bits in the comparator module automatically disables output driver and input buffer for that pin, regardless of the state of the associated CEPDx bit.

### 9.13.10 Port P3 (P3.4 to P3.7) Input/Output With Schmitt Trigger

Figure 9-11 shows the port diagram. Table 9-28 summarizes the selection of the pin functions.



Functional representation only.

**Figure 9-11. Port P3 (P3.4 to P3.7) Diagram**

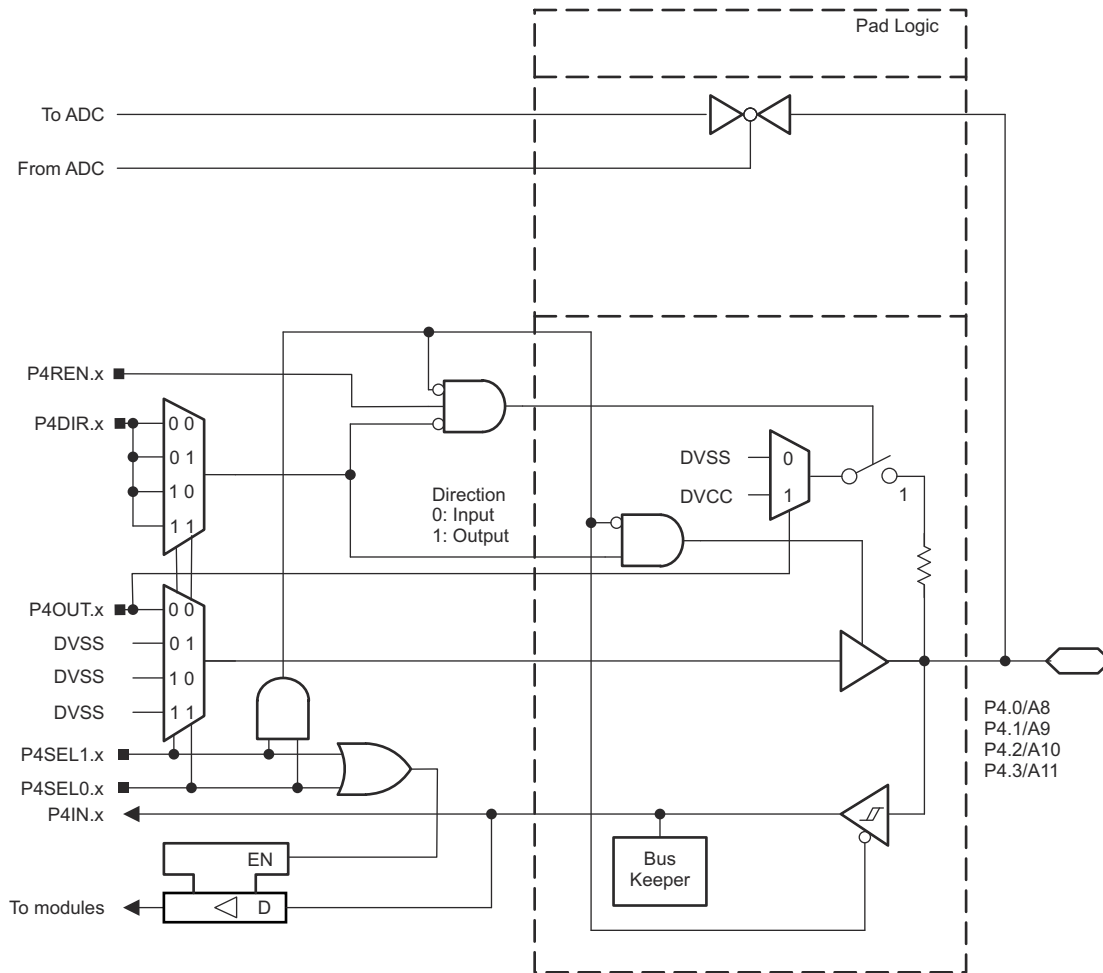
**Table 9-28. Port P3 (P3.4 to P3.7) Pin Functions**

| PIN NAME (P3.x)  | x | FUNCTION                | CONTROL BITS AND SIGNALS <sup>(1)</sup> |          |          |
|------------------|---|-------------------------|-----------------------------------------|----------|----------|
|                  |   |                         | P3DIR.x                                 | P3SEL1.x | P3SEL0.x |
| P3.4/TB0.3/SMCLK | 4 | P3.4 (I/O)              | 0 = Input,<br>1 = Output                | 0        | 0        |
|                  |   | TB0.CCI3A               | 0                                       | 0        | 1        |
|                  |   | TB0.3                   | 1                                       |          |          |
|                  |   | N/A                     | 0                                       | 1        | X        |
|                  |   | SMCLK                   | 1                                       |          |          |
| P3.5/TB0.4/COUT  | 5 | P3.5 (I/O)              | 0 = Input,<br>1 = Output                | 0        | 0        |
|                  |   | TB0.CCI4A               | 0                                       | 0        | 1        |
|                  |   | TB0.4                   | 1                                       |          |          |
|                  |   | N/A                     | 0                                       | 1        | X        |
|                  |   | COUT                    | 1                                       |          |          |
| P3.6/TB0.5       | 6 | P3.6 (I/O)              | 0 = Input,<br>1 = Output                | 0        | 0        |
|                  |   | TB0.CCI5A               | 0                                       | 0        | 1        |
|                  |   | TB0.5                   | 1                                       |          |          |
|                  |   | N/A                     | 0                                       | 1        | X        |
|                  |   | Internally tied to DVSS | 1                                       |          |          |
| P3.7/TB0.6       | 7 | P3.7 (I/O)              | 0 = Input,<br>1 = Output                | 0        | 0        |
|                  |   | TB0.CCI6A               | 0                                       | 0        | 1        |
|                  |   | TB0.6                   | 1                                       |          |          |
|                  |   | N/A                     | 0                                       | 1        | X        |
|                  |   | Internally tied to DVSS | 1                                       |          |          |

(1) X = Don't care

### 9.13.11 Port P4 (P4.0 to P4.3) Input/Output With Schmitt Trigger

Figure 9-12 shows the port diagram. Table 9-29 summarizes the selection of the pin functions.



Functional representation only.

**Figure 9-12. Port P4 (P4.0 to P4.3) Diagram**

**Table 9-29. Port P4 (P4.0 to P4.3) Pin Functions**

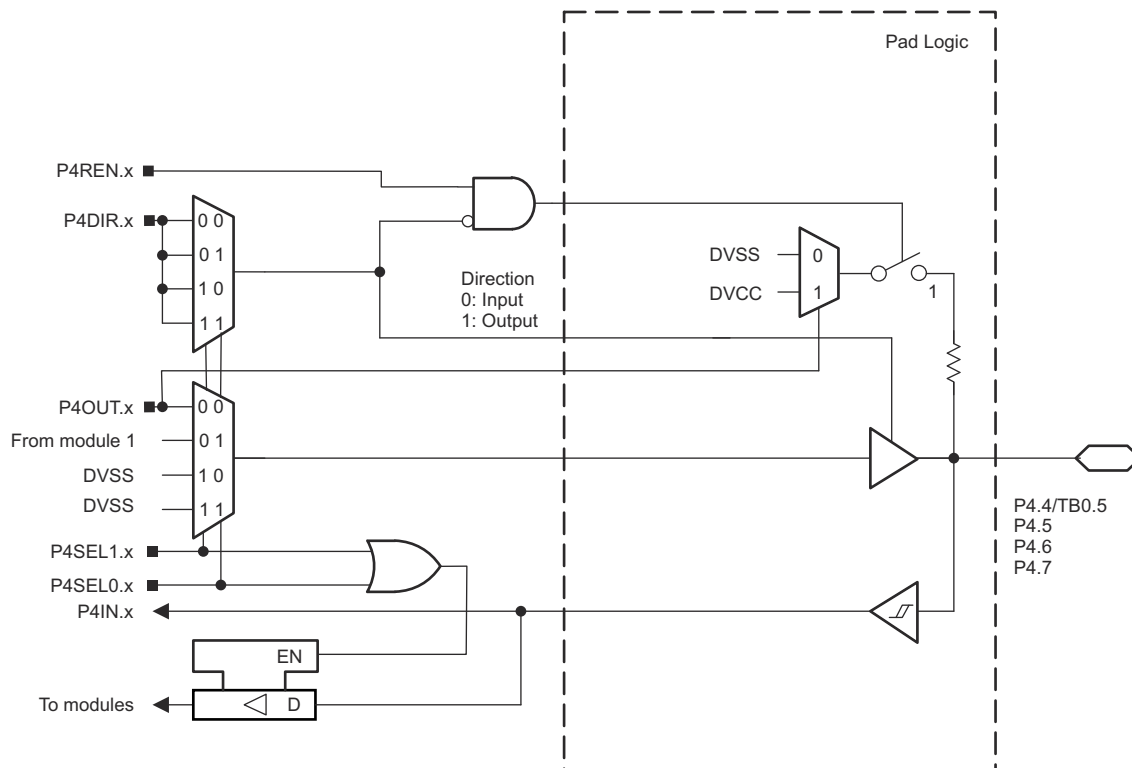
| PIN NAME (P4.x) | x | FUNCTION                | CONTROL BITS AND SIGNALS <sup>(1)</sup> |          |          |
|-----------------|---|-------------------------|-----------------------------------------|----------|----------|
|                 |   |                         | P4DIR.x                                 | P4SEL1.x | P4SEL0.x |
| P4.0/A8         | 0 | P4.0 (I/O)              | 0 = Input,<br>1 = Output                | 0        | 0        |
|                 |   | N/A                     | 0                                       | 0        | 1        |
|                 |   | Internally tied to DVSS | 1                                       |          |          |
|                 |   | N/A                     | 0                                       | 1        | 0        |
|                 |   | Internally tied to DVSS | 1                                       |          |          |
|                 |   | A8 <sup>(2)</sup>       | X                                       | 1        | 1        |
| P4.1/A9         | 1 | P4.1 (I/O)              | 0 = Input,<br>1 = Output                | 0        | 0        |
|                 |   | N/A                     | 0                                       | 0        | 1        |
|                 |   | Internally tied to DVSS | 1                                       |          |          |
|                 |   | N/A                     | 0                                       | 1        | 0        |
|                 |   | Internally tied to DVSS | 1                                       |          |          |
|                 |   | A9 <sup>(2)</sup>       | X                                       | 1        | 1        |
| P4.2/A10        | 2 | P4.2 (I/O)              | 0 = Input,<br>1 = Output                | 0        | 0        |
|                 |   | N/A                     | 0                                       | 0        | 1        |
|                 |   | Internally tied to DVSS | 1                                       |          |          |
|                 |   | N/A                     | 0                                       | 1        | 0        |
|                 |   | Internally tied to DVSS | 1                                       |          |          |
|                 |   | A10 <sup>(2)</sup>      | X                                       | 1        | 1        |
| P4.3/A11        | 3 | P4.3 (I/O)              | 0 = Input,<br>1 = Output                | 0        | 0        |
|                 |   | N/A                     | 0                                       | 0        | 1        |
|                 |   | Internally tied to DVSS | 1                                       |          |          |
|                 |   | N/A                     | 0                                       | 1        | 0        |
|                 |   | Internally tied to DVSS | 1                                       |          |          |
|                 |   | A11 <sup>(2)</sup>      | X                                       | 1        | 1        |

(1) X = Don't care

(2) Setting P4SEL1.x and P4SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

### 9.13.12 Port P4 (P4.4 to P4.7) Input/Output With Schmitt Trigger

Figure 9-13 shows the port diagram. Table 9-30 summarizes the selection of the pin functions.



Functional representation only.

**Figure 9-13. Port P4 (P4.4 to P4.7) Diagram**

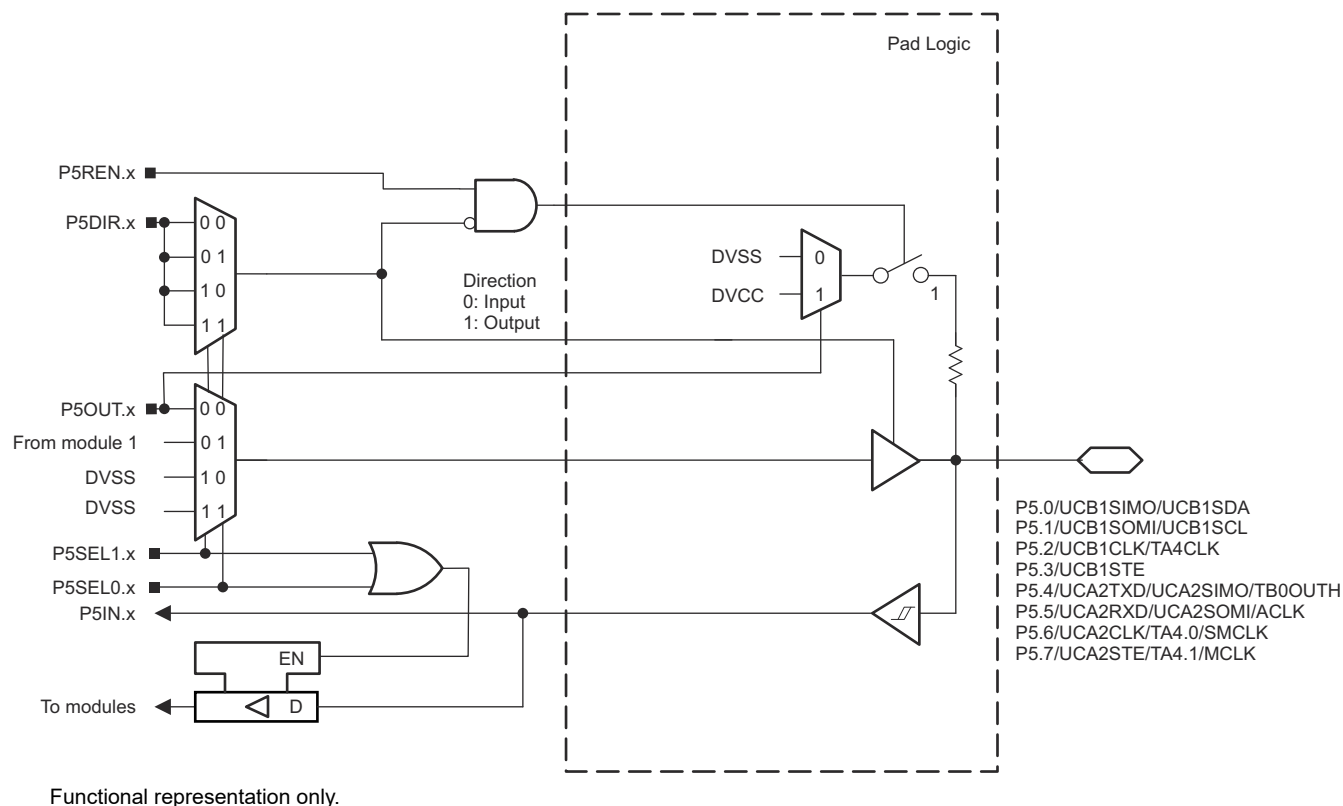
**Table 9-30. Port P4 (P4.4 to P4.7) Pin Functions**

| PIN NAME (P4.x) | x | FUNCTION                | CONTROL BITS AND SIGNALS <sup>(1)</sup> |          |          |
|-----------------|---|-------------------------|-----------------------------------------|----------|----------|
|                 |   |                         | P4DIR.x                                 | P4SEL1.x | P4SEL0.x |
| P4.4/TB0.5      | 4 | P4.4 (I/O)              | 0 = Input,<br>1 = Output                | 0        | 0        |
|                 |   | TB0.CCI5B               | 0                                       | 0        | 1        |
|                 |   | TB0.5                   | 1                                       |          |          |
|                 |   | N/A                     | 0                                       | 1        | X        |
|                 |   | Internally tied to DVSS | 1                                       |          |          |
| P4.5            | 5 | P4.5 (I/O)              | 0 = Input,<br>1 = Output                | 0        | 0        |
|                 |   | N/A                     | 0                                       | 0        | 1        |
|                 |   | Internally tied to DVSS | 1                                       |          |          |
|                 |   | N/A                     | 0                                       | 1        | X        |
|                 |   | Internally tied to DVSS | 1                                       |          |          |
| P4.6            | 6 | P4.6 (I/O)              | 0 = Input,<br>1 = Output                | 0        | 0        |
|                 |   | N/A                     | 0                                       | 0        | 1        |
|                 |   | Internally tied to DVSS | 1                                       |          |          |
|                 |   | N/A                     | 0                                       | 1        | X        |
|                 |   | Internally tied to DVSS | 1                                       |          |          |
| P4.7            | 7 | P4.7 (I/O)              | 0 = Input,<br>1 = Output                | 0        | 0        |
|                 |   | N/A                     | 0                                       | 0        | 1        |
|                 |   | Internally tied to DVSS | 1                                       |          |          |
|                 |   | N/A                     | 0                                       | 1        | X        |
|                 |   | Internally tied to DVSS | 1                                       |          |          |

(1) X = Don't care

### 9.13.13 Port P5 (P5.0 to P5.7) Input/Output With Schmitt Trigger

Figure 9-14 shows the port diagram. Table 9-31 summarizes the selection of the pin functions.



**Figure 9-14. Port P5 (P5.0 to P5.7) Diagram**

### Table 9-31. Port P5 (P5.0 to P5.7) Pin Functions

| PIN NAME (P5.x)       | x | FUNCTION                | CONTROL BITS AND SIGNALS <sup>(1)</sup> |          |          |
|-----------------------|---|-------------------------|-----------------------------------------|----------|----------|
|                       |   |                         | P5DIR.x                                 | P5SEL1.x | P5SEL0.x |
| P5.0/UCB1SIMO/UCB1SDA | 0 | P5.0 (I/O)              | 0 = Input,<br>1 = Output                | 0        | 0        |
|                       |   | UCB1SIMO/UCB1SDA        | X <sup>(2)</sup>                        | 0        | 1        |
|                       |   | N/A                     | 0                                       | 1        | X        |
|                       |   | Internally tied to DVSS | 1                                       |          |          |
| P5.1/UCB1SOMI/UCB1SCL | 1 | P5.1 (I/O)              | 0 = Input,<br>1 = Output                | 0        | 0        |
|                       |   | UCB1SOMI/UCB1SCL        | X <sup>(2)</sup>                        | 0        | 1        |
|                       |   | N/A                     | 0                                       | 1        | X        |
|                       |   | Internally tied to DVSS | 1                                       |          |          |
| P5.2/UCB1CLK/TA4CLK   | 2 | P5.2 (I/O)              | 0 = Input,<br>1 = Output                | 0        | 0        |
|                       |   | UCB1CLK                 | X <sup>(2)</sup>                        | 0        | 1        |
|                       |   | TA4CLK                  | 0                                       | 1        | 0        |
|                       |   | Internally tied to DVSS | 1                                       |          |          |
|                       |   | N/A                     | 0                                       | 1        | 1        |
|                       |   | Internally tied to DVSS | 1                                       |          |          |

**Table 9-31. Port P5 (P5.0 to P5.7) Pin Functions (continued)**

| PIN NAME (P5.x)                   | x | FUNCTION                | CONTROL BITS AND SIGNALS <sup>(1)</sup> |          |          |
|-----------------------------------|---|-------------------------|-----------------------------------------|----------|----------|
|                                   |   |                         | P5DIR.x                                 | P5SEL1.x | P5SEL0.x |
| P5.3/UCB1STE                      | 3 | P5.3 (I/O)              | 0 = Input,<br>1 = Output                | 0        | 0        |
|                                   |   | UCB1STE                 | X <sup>(2)</sup>                        | 0        | 1        |
|                                   |   | N/A                     | 0                                       | 1        | 1        |
|                                   |   | Internally tied to DVSS | 1                                       |          |          |
| P5.4/UCA2TXD/UCA2SIMO/<br>TB0OUTH | 4 | P5.4 (I/O)              | 0 = Input,<br>1 = Output                | 0        | 0        |
|                                   |   | UCA2TXD/UCA2SIMO        | X <sup>(3)</sup>                        | 0        | 1        |
|                                   |   | N/A                     | 0                                       | 1        | 0        |
|                                   |   | Internally tied to DVSS | 1                                       |          |          |
|                                   |   | TB0OUTH                 | 0                                       | 1        | 1        |
|                                   |   | Internally tied to DVSS | 1                                       |          |          |
| P5.5/UCA2RXD/UCA2SOMI/<br>ACLK    | 5 | P5.5 (I/O)              | 0 = Input,<br>1 = Output                | 0        | 0        |
|                                   |   | UCA2RXD/UCA2SOMI        | X <sup>(3)</sup>                        | 0        | 1        |
|                                   |   | N/A                     | 0                                       | 1        | 0        |
|                                   |   | Internally tied to DVSS | 1                                       |          |          |
|                                   |   | N/A                     | 0                                       | 1        | 1        |
|                                   |   | ACLK                    | 1                                       |          |          |
| P5.6/UCA2CLK/TA4.0/SMCLK          | 6 | P5.6 (I/O)              | 0 = Input,<br>1 = Output                | 0        | 0        |
|                                   |   | UCA2CLK                 | X <sup>(3)</sup>                        | 0        | 1        |
|                                   |   | TA4.CCI0A               | 0                                       | 1        | 0        |
|                                   |   | TA4.0                   | 1                                       |          |          |
|                                   |   | N/A                     | 0                                       | 1        | 1        |
|                                   |   | SMCLK                   | 1                                       |          |          |
| P5.7/UCA2STE/TA4.1/MCLK           | 7 | P5.7 (I/O)              | 0 = Input,<br>1 = Output                | 0        | 0        |
|                                   |   | UCA2STE                 | X <sup>(3)</sup>                        | 0        | 1        |
|                                   |   | TA4.CCI1A               | 0                                       | 1        | 0        |
|                                   |   | TA4.1                   | 1                                       |          |          |
|                                   |   | NA                      | 0                                       | 1        | 1        |
|                                   |   | MCLK                    | 1                                       |          |          |

(1) X = Don't care

(2) Direction controlled by eUSCI\_B1 module.

(3) Direction controlled by eUSCI\_A2 module.

Figure 9-15 shows the port diagram. Table 9-32 summarizes the selection of the pin functions.



**Figure 9-15. Port P6 (P6.0 to P6.7) Diagram**

**Table 9-32. Port P6 (P6.0 to P6.7) Pin Functions**

| PIN NAME (P6.x)       | x | FUNCTION                | CONTROL BITS AND SIGNALS <sup>(1)</sup> |          |          |
|-----------------------|---|-------------------------|-----------------------------------------|----------|----------|
|                       |   |                         | P6DIR.x                                 | P6SEL1.x | P6SEL0.x |
| P6.0/UCA3TXD/UCA3SIMO | 0 | P6.0 (I/O)              | 0 = Input,<br>1 = Output                | 0        | 0        |
|                       |   | UCA3TXD/UCA3SIMO        | X <sup>(3)</sup>                        | 0        | 1        |
|                       |   | N/A                     | 0                                       | 1        | X        |
|                       |   | Internally tied to DVSS | 1                                       |          |          |
| P6.1/UCA3RXD/UCA3SOMI | 1 | P6.1 (I/O)              | 0 = Input,<br>1 = Output                | 0        | 0        |
|                       |   | UCA3RXD/UCA3SOMI        | X <sup>(3)</sup>                        | 0        | 1        |
|                       |   | N/A                     | 0                                       | 1        | X        |
|                       |   | Internally tied to DVSS | 1                                       |          |          |
| P6.2/UCA3CLK          | 2 | P6.2 (I/O)              | 0 = Input,<br>1 = Output                | 0        | 0        |
|                       |   | UCA3CLK                 | X <sup>(3)</sup>                        | 0        | 1        |
|                       |   | N/A                     | 0                                       | 1        | X        |
|                       |   | Internally tied to DVSS | 1                                       |          |          |
| P6.3/UCA3STE          | 3 | P6.3 (I/O)              | 0 = Input,<br>1 = Output                | 0        | 0        |
|                       |   | UCA3STE                 | X <sup>(3)</sup>                        | 0        | 1        |
|                       |   | N/A                     | 0                                       | 1        | X        |
|                       |   | Internally tied to DVSS | 1                                       |          |          |
| P6.4/UCB3SIMO/UCB3SDA | 4 | P6.4 (I/O)              | 0 = Input,<br>1 = Output                | 0        | 0        |
|                       |   | UCB3SIMO/UCB3SDA        | X <sup>(2)</sup>                        | 0        | 1        |
|                       |   | N/A                     | 0                                       | 1        | X        |
|                       |   | Internally tied to DVSS | 1                                       |          |          |
| P6.5/UCB3SOMI/UCB3SCL | 5 | P6.5 (I/O)              | 0 = Input,<br>1 = Output                | 0        | 0        |
|                       |   | UCB3SOMI/UCB3SCL        | X <sup>(2)</sup>                        | 0        | 1        |
|                       |   | N/A                     | 0                                       | 1        | X        |
|                       |   | Internally tied to DVSS | 1                                       |          |          |
| P6.6/UCB3CLK          | 6 | P6.6 (I/O)              | 0 = Input,<br>1 = Output                | 0        | 0        |
|                       |   | UCB3CLK                 | X <sup>(2)</sup>                        | 0        | 1        |
|                       |   | N/A                     | 0                                       | 1        | X        |
|                       |   | Internally tied to DVSS | 1                                       |          |          |
| P6.7/UCB3STE          | 7 | P6.7 (I/O)              | 0 = Input,<br>1 = Output                | 0        | 0        |
|                       |   | UCB3STE                 | X <sup>(2)</sup>                        | 0        | 1        |
|                       |   | N/A                     | 0                                       | 1        | X        |
|                       |   | Internally tied to DVSS | 1                                       |          |          |

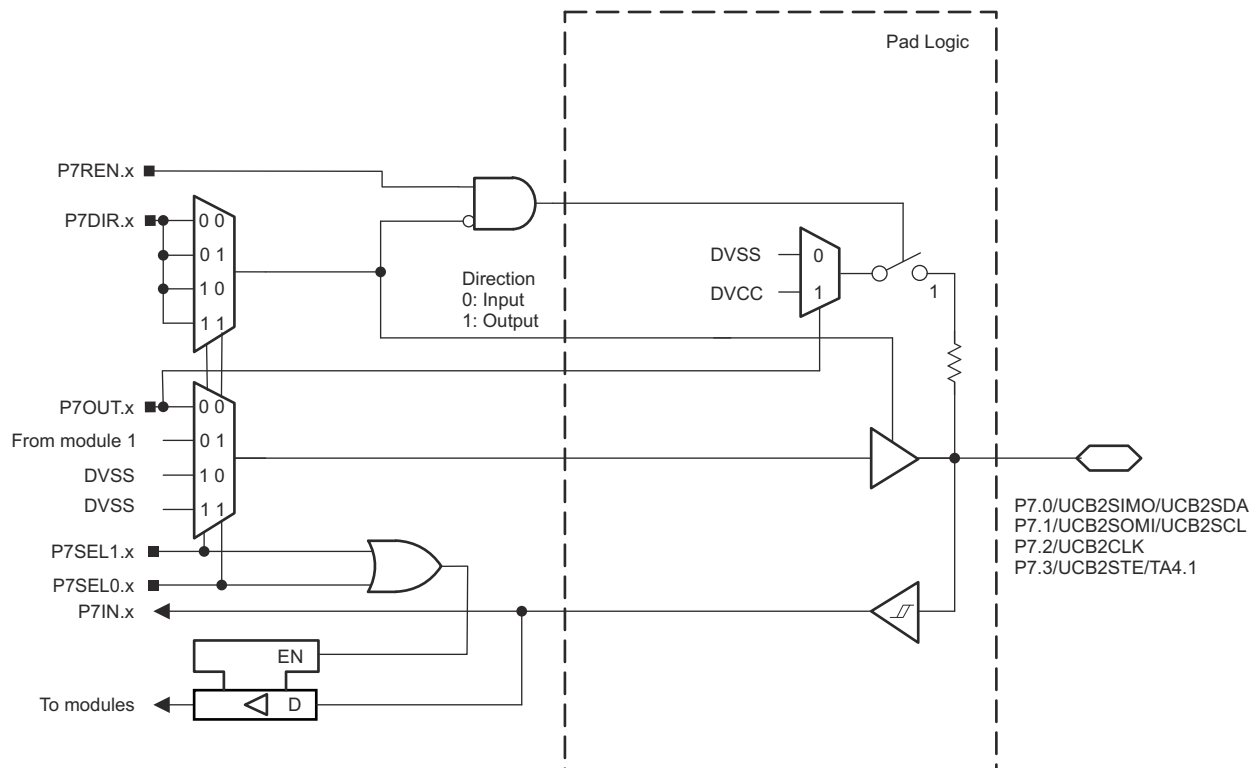
(1) X = Don't care

(2) Direction controlled by eUSCI\_B3 module.

(3) Direction controlled by eUSCI\_A3 module.

### 9.13.15 Port P7 (P7.0 to P7.3) Input/Output With Schmitt Trigger

Figure 9-16 shows the port diagram. Table 9-33 summarizes the selection of the pin functions.



Functional representation only.

**Figure 9-16. Port P7 (P7.0 to P7.3) Diagram**

**Table 9-33. Port P7 (P7.0 to P7.3) Pin Functions**

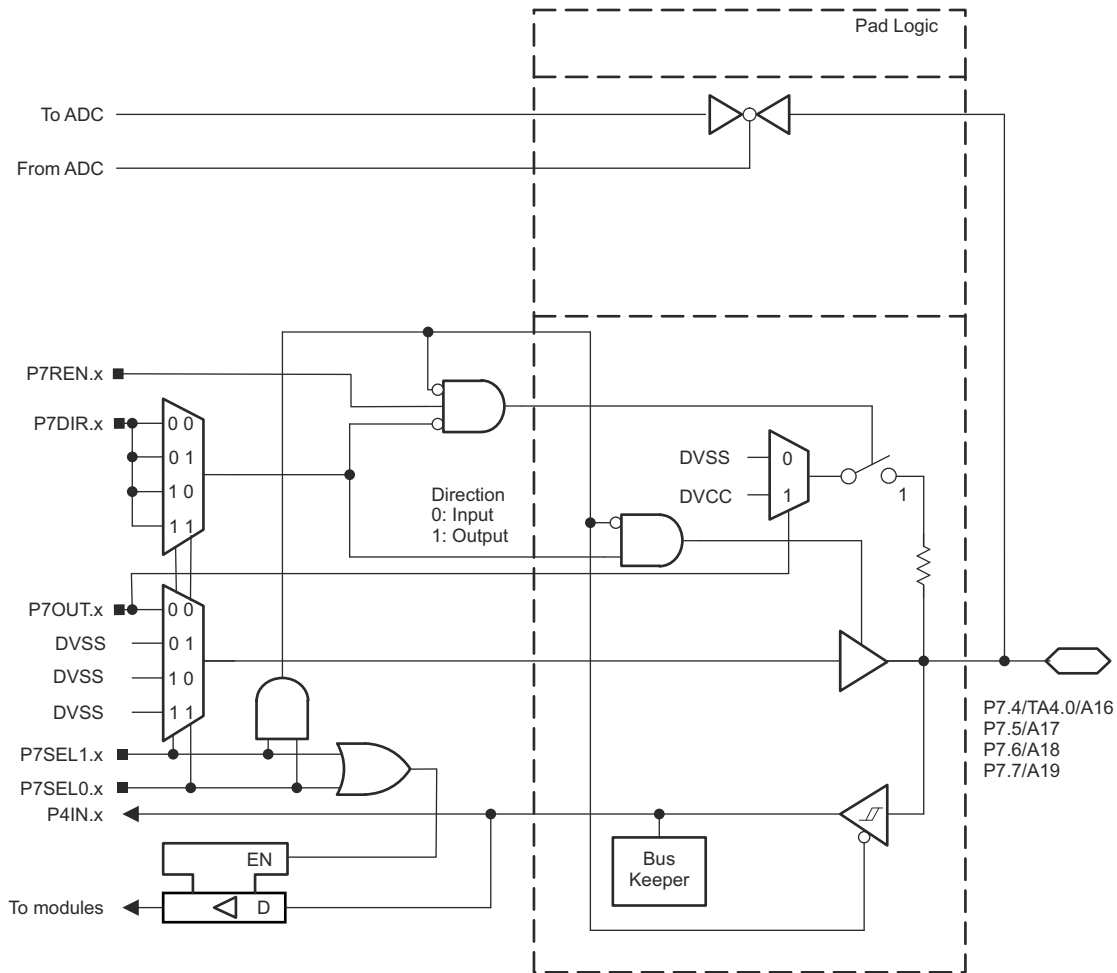
| PIN NAME (P7.x)       | x | FUNCTION                | CONTROL BITS AND SIGNALS <sup>(1)</sup> |          |          |
|-----------------------|---|-------------------------|-----------------------------------------|----------|----------|
|                       |   |                         | P7DIR.x                                 | P7SEL1.x | P7SEL0.x |
| P7.0/UCB2SIMO/UCB2SDA | 0 | P7.0 (I/O)              | 0 = Input,<br>1 = Output                | 0        | 0        |
|                       |   | UCB2SIMO/UCB2SDA        | X <sup>(2)</sup>                        | 0        | 1        |
|                       |   | N/A                     | 0                                       | 1        | X        |
|                       |   | Internally tied to DVSS | 1                                       |          |          |
| P7.1/UCB2SOMI/UCB2SCL | 1 | P7.1 (I/O)              | 0 = Input,<br>1 = Output                | 0        | 0        |
|                       |   | UCB2SOMI/UCB2SCL        | X <sup>(2)</sup>                        | 0        | 1        |
|                       |   | N/A                     | 0                                       | 1        | X        |
|                       |   | Internally tied to DVSS | 1                                       |          |          |
| P7.2/UCB2CLK          | 2 | P7.2 (I/O)              | 0 = Input,<br>1 = Output                | 0        | 0        |
|                       |   | UCB2CLK                 | X <sup>(2)</sup>                        | 0        | 1        |
|                       |   | N/A                     | 0                                       | 1        | X        |
|                       |   | Internally tied to DVSS | 1                                       |          |          |
| P7.3/UCB2STE/TA4.1    | 3 | P7.3 (I/O)              | 0 = Input,<br>1 = Output                | 0        | 0        |
|                       |   | UCB2STE                 | X <sup>(2)</sup>                        | 0        | 1        |
|                       |   | TA4.CCI1B               | 0                                       | 1        | 0        |
|                       |   | TA4.1                   | 1                                       |          |          |
|                       |   | N/A                     | 0                                       | 1        | 1        |
|                       |   | Internally tied to DVSS | 1                                       |          |          |

(1) X = Don't care

(2) Direction controlled by eUSCI\_B2 module.

### 9.13.16 Port P7 (P7.4 to P7.7) Input/Output With Schmitt Trigger

Figure 9-17 shows the port diagram. Table 9-34 summarizes the selection of the pin functions.



Functional representation only.

**Figure 9-17. Port P7 (P7.3 to P7.7) Diagram**

**Table 9-34. Port P7 (P7.3 to P7.7) Pin Functions**

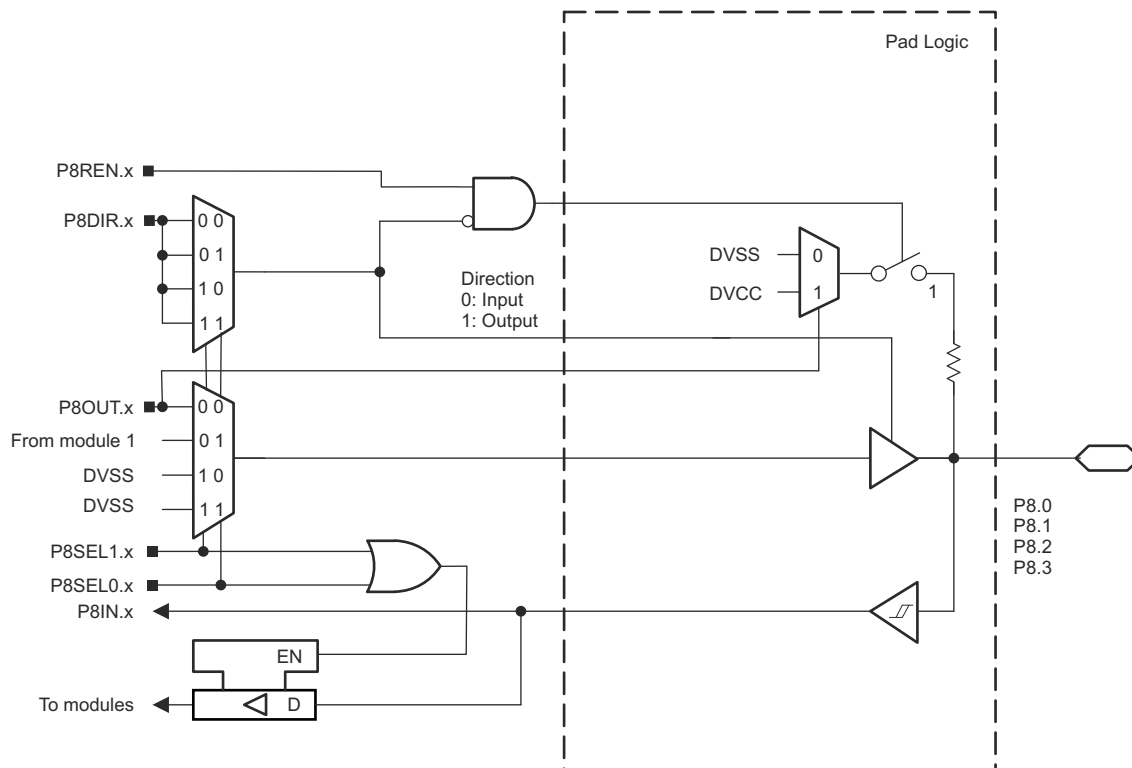
| PIN NAME (P7.x) | x | FUNCTION                | CONTROL BITS AND SIGNALS <sup>(1)</sup> |          |          |
|-----------------|---|-------------------------|-----------------------------------------|----------|----------|
|                 |   |                         | P7DIR.x                                 | P7SEL1.x | P7SEL0.x |
| P7.4/TA4.0/A16  | 4 | P7.4 (I/O)              | 0 = Input,<br>1 = Output                | 0        | 0        |
|                 |   | N/A                     | 0                                       | 0        | 1        |
|                 |   | Internally tied to DVSS | 1                                       |          |          |
|                 |   | TA4.CCI0B               | 0                                       | 1        | 0        |
|                 |   | TA4.0                   | 1                                       |          |          |
|                 |   | A16 <sup>(2)</sup>      | X                                       | 1        | 1        |
| P7.5/A17        | 5 | P7.5 (I/O)              | 0 = Input,<br>1 = Output                | 0        | 0        |
|                 |   | N/A                     | 0                                       | 0        | 1        |
|                 |   | Internally tied to DVSS | 1                                       |          |          |
|                 |   | N/A                     | 0                                       | 1        | 0        |
|                 |   | Internally tied to DVSS | 1                                       |          |          |
|                 |   | A17 <sup>(2)</sup>      | X                                       | 1        | 1        |
| P7.6/A18        | 6 | P7.6 (I/O)              | 0 = Input,<br>1 = Output                | 0        | 0        |
|                 |   | N/A                     | 0                                       | 0        | 1        |
|                 |   | Internally tied to DVSS | 1                                       |          |          |
|                 |   | N/A                     | 0                                       | 1        | 0        |
|                 |   | Internally tied to DVSS | 1                                       |          |          |
|                 |   | A18 <sup>(2)</sup>      | X                                       | 1        | 1        |
| P7.7/A19        | 7 | P7.7 (I/O)              | 0 = Input,<br>1 = Output                | 0        | 0        |
|                 |   | N/A                     | 0                                       | 0        | 1        |
|                 |   | Internally tied to DVSS | 1                                       |          |          |
|                 |   | N/A                     | 0                                       | 1        | 0        |
|                 |   | Internally tied to DVSS | 1                                       |          |          |
|                 |   | A19 <sup>(2)</sup>      | X                                       | 1        | 1        |

(1) X = Don't care

(2) Setting P7SEL1.x and P7SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

### 9.13.17 Port P8 (P8.0 to P8.3) Input/Output With Schmitt Trigger

Figure 9-18 shows the port diagram. Table 9-35 summarizes the selection of the pin functions.



Functional representation only.

**Figure 9-18. Port P8 (P8.0 to P8.3) Diagram**

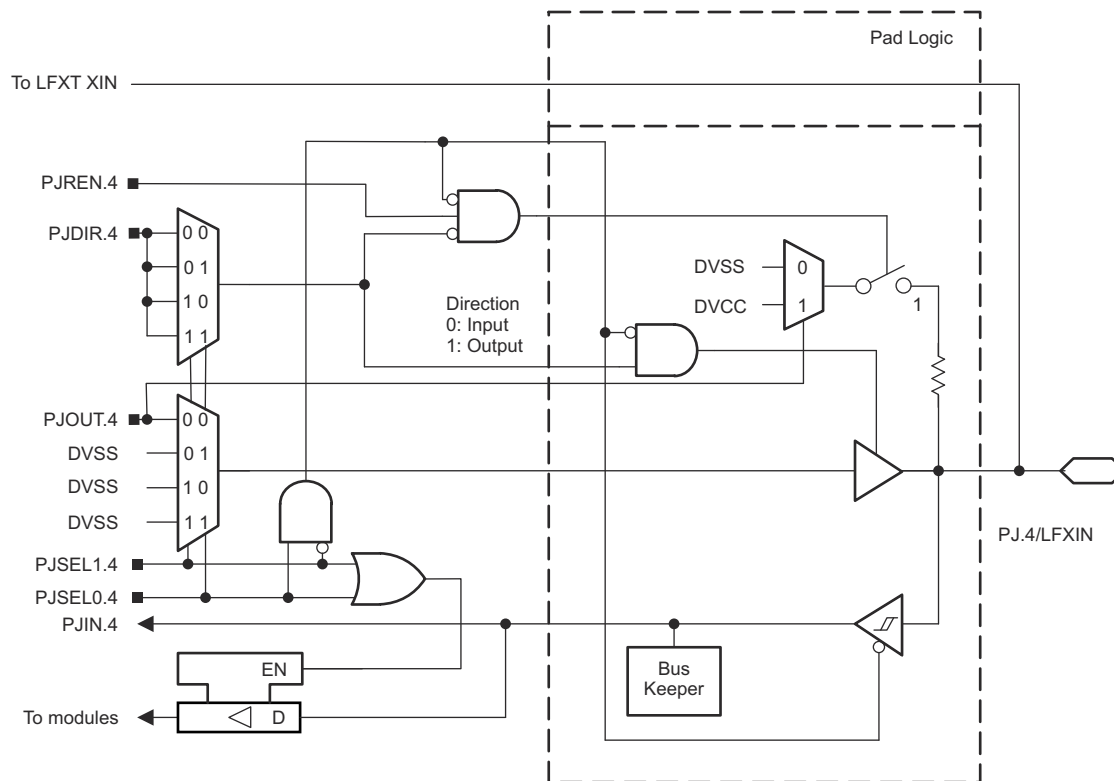
**Table 9-35. Port P8 (P8.0 to P8.3) Pin Functions**

| PIN NAME (P8.x) | x | FUNCTION                | CONTROL BITS AND SIGNALS <sup>(1)</sup> |          |          |
|-----------------|---|-------------------------|-----------------------------------------|----------|----------|
|                 |   |                         | P8DIR.x                                 | P8SEL1.x | P8SEL0.x |
| P8.0            | 0 | P8.0(I/O)               | 0 = Input,<br>1 = Output                | 0        | 0        |
|                 |   | N/A                     | 0                                       | 0        | 1        |
|                 |   | Internally tied to DVSS | 1                                       |          |          |
|                 |   | N/A                     | 0                                       | 1        | X        |
|                 |   | Internally tied to DVSS | 1                                       |          |          |
| P8.1            | 1 | P8.1 (I/O)              | 0 = Input,<br>1 = Output                | 0        | 0        |
|                 |   | N/A                     | 0                                       | 0        | 1        |
|                 |   | Internally tied to DVSS | 1                                       |          |          |
|                 |   | N/A                     | 0                                       | 1        | X        |
|                 |   | Internally tied to DVSS | 1                                       |          |          |
| P8.2            | 2 | P8.2 (I/O)              | 0 = Input,<br>1 = Output                | 0        | 0        |
|                 |   | N/A                     | 0                                       | 0        | 1        |
|                 |   | Internally tied to DVSS | 1                                       |          |          |
|                 |   | N/A                     | 0                                       | 1        | X        |
|                 |   | Internally tied to DVSS | 1                                       |          |          |
| P8.3            | 3 | P8.3 (I/O)              | 0 = Input,<br>1 = Output                | 0        | 0        |
|                 |   | N/A                     | 0                                       | 0        | 1        |
|                 |   | Internally tied to DVSS | 1                                       |          |          |
|                 |   | N/A                     | 0                                       | 1        | X        |
|                 |   | Internally tied to DVSS | 1                                       |          |          |

(1) X = Don't care

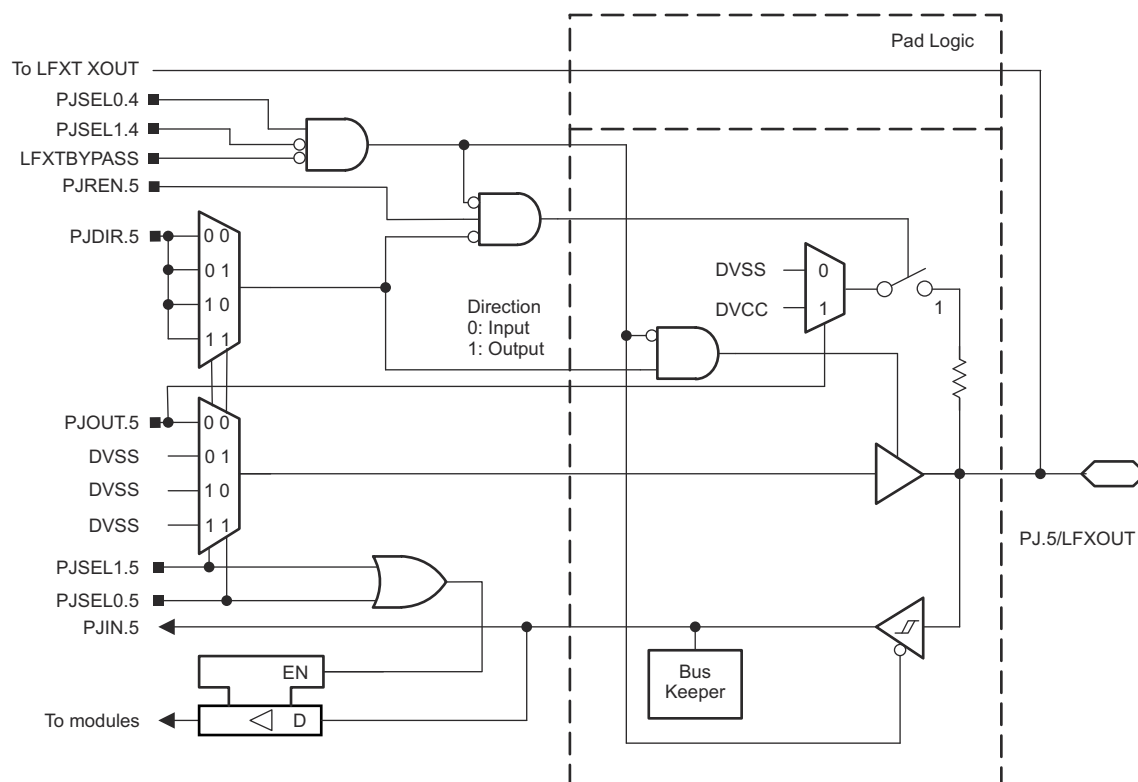
### 9.13.18 Port PJ (PJ.4 and PJ.5) Input/Output With Schmitt Trigger

Figure 9-19 and Figure 9-20 show the port diagrams. Table 9-36 summarizes the selection of the pin functions.



Functional representation only.

**Figure 9-19. Port PJ (PJ.4) Diagram**



Functional representation only.

**Figure 9-20. Port PJ (PJ.5) Diagram**

**Table 9-36. Port PJ (PJ.4 and PJ.5) Pin Functions**

| PIN NAME (PJ.x) | x | FUNCTION                           | CONTROL BITS AND SIGNALS <sup>(1)</sup> |                    |                    |          |          | LFXT BYPASS |
|-----------------|---|------------------------------------|-----------------------------------------|--------------------|--------------------|----------|----------|-------------|
|                 |   |                                    | PJDIR.x                                 | PJSEL1.5           | PJSEL0.5           | PJSEL1.4 | PJSEL0.4 |             |
| PJ.4/LFXIN      | 4 | PJ.4 (I/O)                         | 0 = Input,<br>1 = Output                | X                  | X                  | 0        | 0        | X           |
|                 |   | N/A                                | 0                                       | X                  | X                  | 1        | X        | X           |
|                 |   | Internally tied to DVSS            | 1                                       |                    |                    |          |          |             |
|                 |   | LFXIN crystal mode <sup>(3)</sup>  | X                                       | X                  | X                  | 0        | 1        | 0           |
|                 |   | LFXIN bypass mode <sup>(3)</sup>   | X                                       | X                  | X                  | 0        | 1        | 1           |
| PJ.5/LFXOUT     | 5 | PJ.5 (I/O)                         | 0 = Input,<br>1 = Output                | 0                  | 0                  | 0        | 0        | 0           |
|                 |   |                                    |                                         |                    |                    | 1        | X        |             |
|                 |   |                                    |                                         |                    |                    | X        | X        |             |
|                 |   | N/A                                | 0                                       | See <sup>(2)</sup> | See <sup>(2)</sup> | 0        | 0        | 0           |
|                 |   |                                    |                                         |                    |                    | 1        | X        |             |
|                 |   |                                    |                                         |                    |                    | X        | X        |             |
|                 |   | Internally tied to DVSS            | 1                                       | See <sup>(2)</sup> | See <sup>(2)</sup> | 0        | 0        | 0           |
|                 |   |                                    |                                         |                    |                    | 1        | X        |             |
|                 |   |                                    |                                         |                    |                    | X        | X        |             |
|                 |   | LFXOUT crystal mode <sup>(3)</sup> | X                                       | X                  | X                  | 0        | 1        | 0           |

(1) X = Don't care

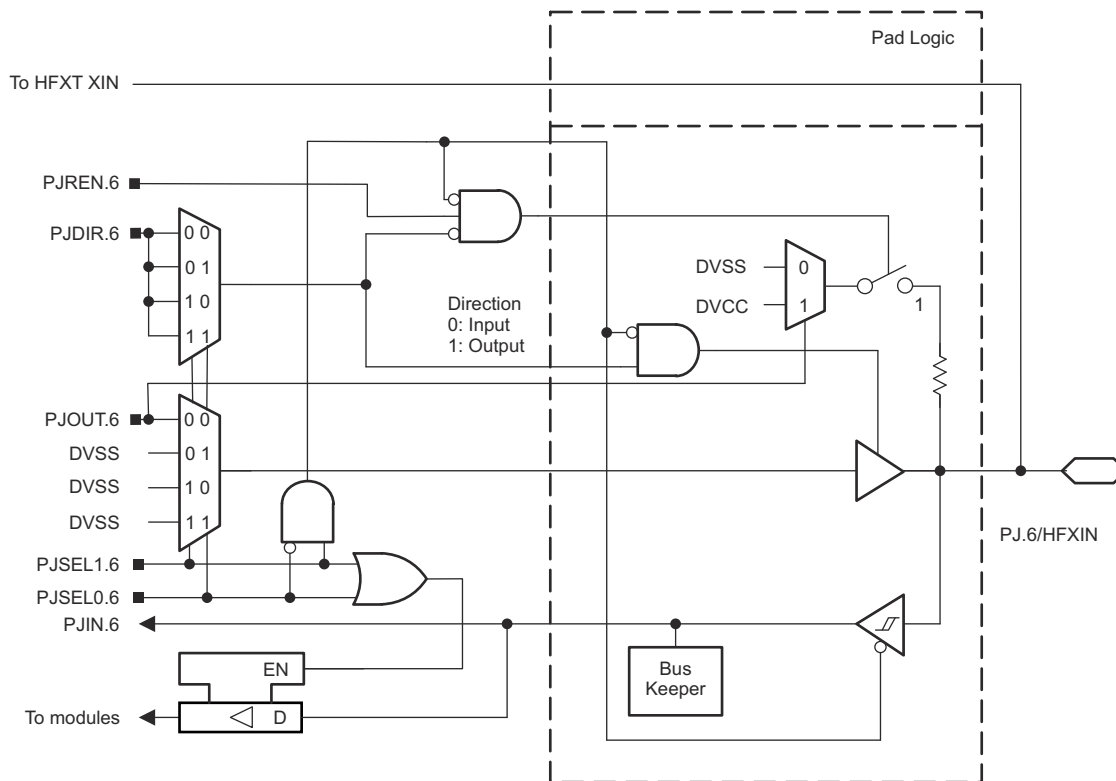
(2) If PJSEL0.5 = 1 or PJSEL1.5 = 1, the general-purpose I/O functionality is disabled. No input function is available. Configured as output, the pin is actively pulled to zero.

(3) If PJSEL1.4 = 0 and PJSEL0.4 = 1, the general-purpose I/O is disabled. When LFXTBYPASS = 0, PJ.4 and PJ.5 are configured for crystal operation and PJSEL1.5 and PJSEL0.5 are don't care. When LFXTBYPASS = 1, PJ.4 is configured for bypass operation and PJ.5 is configured as general-purpose I/O.

(4) When PJ.4 is configured in bypass mode, PJ.5 is configured as general-purpose I/O.

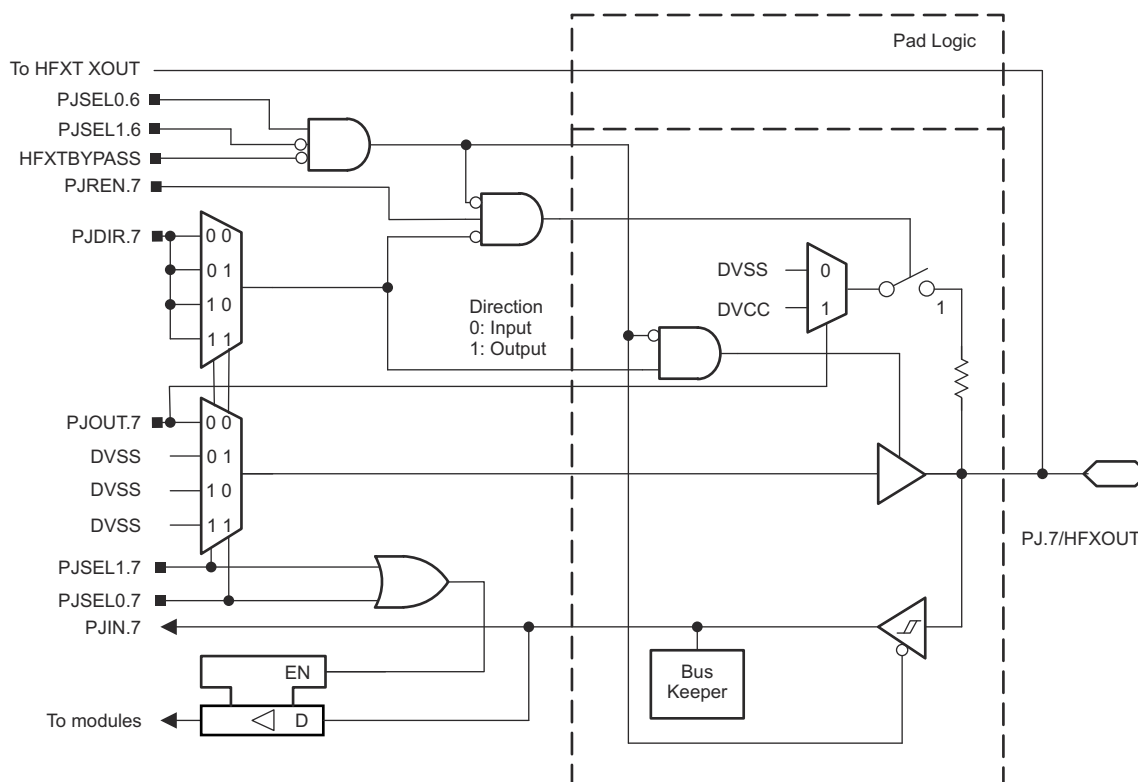
### 9.13.19 Port PJ (PJ.6 and PJ.7) Input/Output With Schmitt Trigger

Figure 9-21 and Figure 9-22 show the port diagrams. Table 9-37 summarizes the selection of the pin functions.



Functional representation only.

**Figure 9-21. Port PJ (PJ.6) Diagram**



Functional representation only.

**Figure 9-22. Port PJ (PJ.7) Diagram**

**Table 9-37. Port PJ (PJ.6 and PJ.7) Pin Functions**

| PIN NAME (PJ.x) | x | FUNCTION                           | CONTROL BITS AND SIGNALS <sup>(1)</sup> |                    |                    |          |          |                  |
|-----------------|---|------------------------------------|-----------------------------------------|--------------------|--------------------|----------|----------|------------------|
|                 |   |                                    | PJDIR.x                                 | PJSEL1.7           | PJSEL0.7           | PJSEL1.6 | PJSEL0.6 | HFXTBYPASS       |
| PJ.6/HFXIN      | 6 | PJ.6 (I/O)                         | 0 = Input,<br>1 = Output                | X                  | X                  | 0        | 0        | X                |
|                 |   | N/A                                | 0                                       | X                  | X                  | 1        | X        | X                |
|                 |   | Internally tied to DVSS            | 1                                       |                    |                    |          |          |                  |
|                 |   | HFXIN crystal mode <sup>(3)</sup>  | X                                       | X                  | X                  | 0        | 1        | 0                |
|                 |   | HFXIN bypass mode <sup>(3)</sup>   | X                                       | X                  | X                  | 0        | 1        | 1                |
| PJ.7/HFXOUT     | 7 | PJ.7 (I/O) <sup>(2)</sup>          | 0 = Input,<br>1 = Output                | 0                  | 0                  | 0        | 0        | 0                |
|                 |   |                                    |                                         |                    |                    | 1        | X        |                  |
|                 |   |                                    |                                         |                    |                    | X        | X        | 1 <sup>(4)</sup> |
|                 |   | N/A                                | 0                                       | See <sup>(2)</sup> | See <sup>(2)</sup> | 0        | 0        | 0                |
|                 |   |                                    |                                         |                    |                    | 1        | X        |                  |
|                 |   |                                    |                                         |                    |                    | X        | X        | 1 <sup>(4)</sup> |
|                 |   | Internally tied to DVSS            | 1                                       | See <sup>(2)</sup> | See <sup>(2)</sup> | 0        | 0        | 0                |
|                 |   |                                    |                                         |                    |                    | 1        | X        |                  |
|                 |   | HFXOUT crystal mode <sup>(3)</sup> | X                                       | X                  | X                  | 0        | 1        | 0                |

(1) X = Don't care

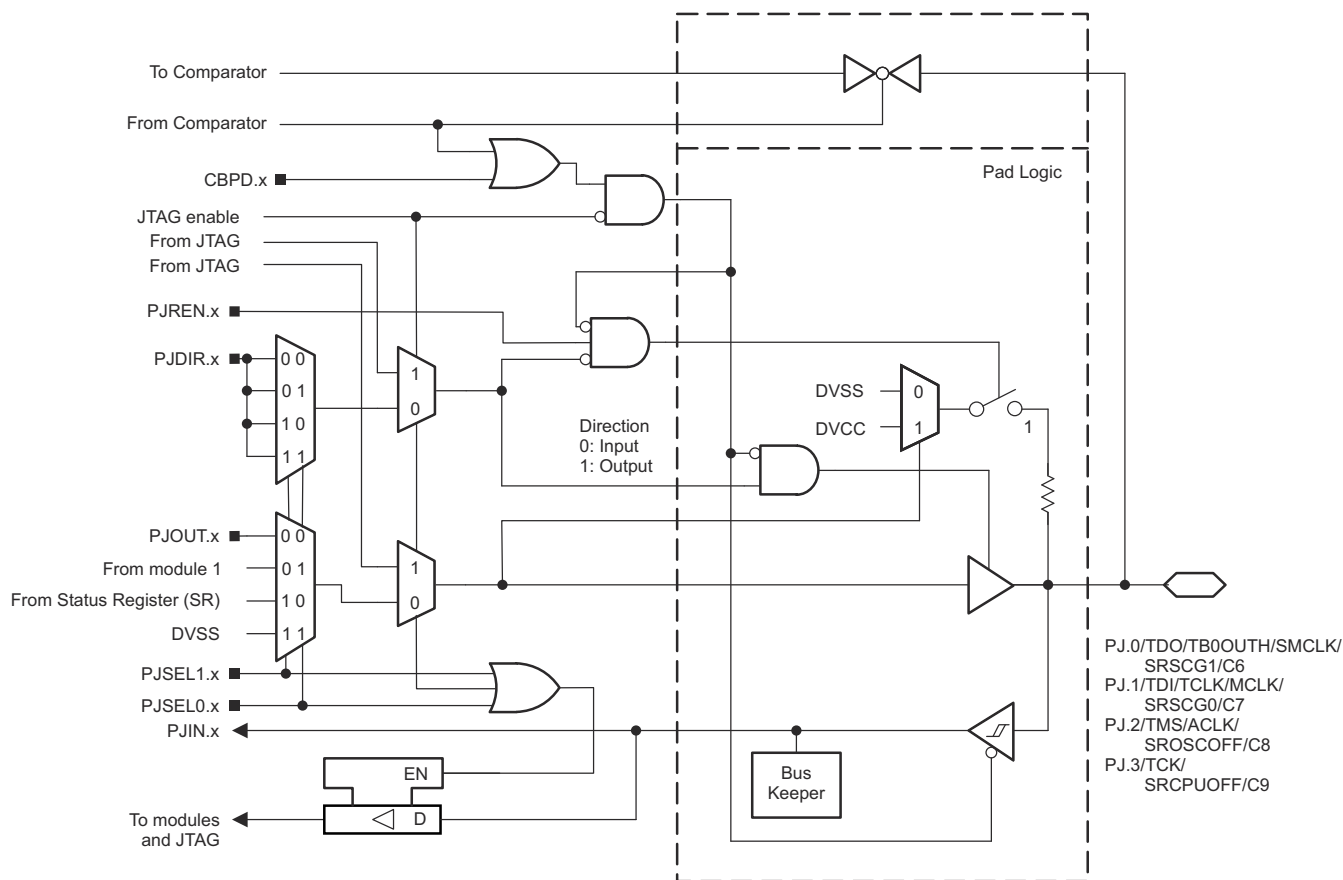
(2) With PJSEL0.7 = 1 or PJSEL1.7 = 1 the general-purpose I/O functionality is disabled. No input function is available. Configured as output the pin is actively pulled to zero.

(3) Setting PJSEL1.6 = 0 and PJSEL0.6 = 1 causes the general-purpose I/O to be disabled. When HFXTBYPASS = 0, PJ.6 and PJ.7 are configured for crystal operation and PJSEL1.6 and PJSEL0.7 are do not care. When HFXTBYPASS = 1, PJ.6 is configured for bypass operation and PJ.7 is configured as general-purpose I/O.

(4) When PJ.6 is configured in bypass mode, PJ.7 is configured as general-purpose I/O.

### 9.13.20 Port PJ (PJ.0 to PJ.3) JTAG Pins TDO, TMS, TCK, TDI/TCLK, Input/Output With Schmitt Trigger

Figure 9-23 shows the port diagram. Table 9-38 summarizes the selection of the pin functions.



Functional representation only.

**Figure 9-23. Port PJ (PJ.0 to PJ.3) Diagram**

**Table 9-38. Port PJ (PJ.0 to PJ.3) Pin Functions**

| PIN NAME (PJ.x)                      | x | FUNCTION                     | CONTROL BITS OR SIGNALS <sup>(1)</sup> |          |          |            |
|--------------------------------------|---|------------------------------|----------------------------------------|----------|----------|------------|
|                                      |   |                              | PJDIR.x                                | PJSEL1.x | PJSEL0.x | CEPDx (Cx) |
| PJ.0/TDO/TB0OUTH/<br>SMCLK/SRSCG1/C6 | 0 | PJ.0 (I/O) <sup>(2)</sup>    | 0 = Input,<br>1 = Output               | 0        | 0        | 0          |
|                                      |   | TDO <sup>(3)</sup>           | X                                      | X        | X        | 0          |
|                                      |   | TB0OUTH                      | 0                                      | 0        | 1        | 0          |
|                                      |   | SMCLK <sup>(6)</sup>         | 1                                      |          |          |            |
|                                      |   | N/A                          | 0                                      | 1        | 0        | 0          |
|                                      |   | CPU Status Register Bit SCG1 | 1                                      |          |          |            |
|                                      |   | N/A                          | 0                                      | 1        | 1        | 0          |
|                                      |   | Internally tied to DVSS      | 1                                      |          |          |            |
|                                      |   | C6 <sup>(5)</sup>            | X                                      | X        | X        | 1          |

**Table 9-38. Port PJ (PJ.0 to PJ.3) Pin Functions (continued)**

| PIN NAME (PJ.x)                  | x | FUNCTION                       | CONTROL BITS OR SIGNALS <sup>(1)</sup> |          |          |            |
|----------------------------------|---|--------------------------------|----------------------------------------|----------|----------|------------|
|                                  |   |                                | PJDIR.x                                | PJSEL1.x | PJSEL0.x | CEPDx (Cx) |
| PJ.1/TDI/TCLK/MCLK/<br>SRSCG0/C7 | 1 | PJ.1 (I/O) <sup>(2)</sup>      | 0 = Input,<br>1 = Output               | 0        | 0        | 0          |
|                                  |   | TDI/TCLK <sup>(3) (4)</sup>    | X                                      | X        | X        | 0          |
|                                  |   | N/A                            | 0                                      | 0        | 1        | 0          |
|                                  |   | MCLK                           | 1                                      |          |          |            |
|                                  |   | N/A                            | 0                                      | 1        | 0        | 0          |
|                                  |   | CPU Status Register Bit SCG0   | 1                                      |          |          |            |
|                                  |   | N/A                            | 0                                      | 1        | 1        | 0          |
|                                  |   | Internally tied to DVSS        | 1                                      |          |          |            |
|                                  |   | C7 <sup>(5)</sup>              | X                                      | X        | X        | 1          |
| PJ.2/TMS/ACLK/<br>SROSCOFF/C8    | 2 | PJ.2 (I/O) <sup>(2)</sup>      | 0 = Input,<br>1 = Output               | 0        | 0        | 0          |
|                                  |   | TMS <sup>(3) (4)</sup>         | X                                      | X        | X        | 0          |
|                                  |   | N/A                            | 0                                      | 0        | 1        | 0          |
|                                  |   | ACLK                           | 1                                      |          |          |            |
|                                  |   | N/A                            | 0                                      | 1        | 0        | 0          |
|                                  |   | CPU Status Register Bit OSCOFF | 1                                      |          |          |            |
|                                  |   | N/A                            | 0                                      | 1        | 1        | 0          |
|                                  |   | Internally tied to DVSS        | 1                                      |          |          |            |
|                                  |   | C8 <sup>(5)</sup>              | X                                      | X        | X        | 1          |
| PJ.3/TCK/SRCPUOFF/C9             | 3 | PJ.3 (I/O) <sup>(2)</sup>      | 0 = Input,<br>1 = Output               | 0        | 0        | 0          |
|                                  |   | TCK <sup>(3) (4)</sup>         | X                                      | X        | X        | 0          |
|                                  |   | N/A                            | 0                                      | 0        | 1        | 0          |
|                                  |   | Internally tied to DVSS        | 1                                      |          |          |            |
|                                  |   | N/A                            | 0                                      | 1        | 0        | 0          |
|                                  |   | CPU Status Register Bit CPUOFF | 1                                      |          |          |            |
|                                  |   | N/A                            | 0                                      | 1        | 1        | 0          |
|                                  |   | Internally tied to DVSS        | 1                                      |          |          |            |
|                                  |   | C9 <sup>(5)</sup>              | X                                      | X        | X        | 1          |

(1) X = Don't care

(2) Default condition

(3) The pin direction is controlled by the JTAG module. JTAG mode selection is made through the SYS module or by the Spy-Bi-Wire four-wire entry sequence. Neither PJSEL1.x and PJSEL0.x nor CEPDx bits have an effect in these cases.

(4) In JTAG mode, pullups are activated automatically on TMS, TCK, and TDI/TCLK. PJREN.x are don't care.

(5) Setting the CEPDx bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the Cx input pin to the comparator multiplexer with the input select bits in the comparator module automatically disables the output driver and input buffer for that pin, regardless of the state of the associated CEPDx bit.

(6) Do not use this pin as SMCLK output if the TB0OUTH functionality is used on any other pin. Select an alternate SMCLK output pin.

## 9.14 Device Descriptors (TLV)

[Table 9-40](#) lists the contents of the device descriptor tag-length-value (TLV) structure for MSP430FR59xx(1) devices including AES. [Table 9-39](#) summarizes the Device IDs of the MSP430FR59xx(1) devices.

**Table 9-39. Device IDs**

| DEVICE        | PACKAGE              | DEVICE ID |        |
|---------------|----------------------|-----------|--------|
|               |                      | 01A05h    | 01A04h |
| MSP430FR5994  | ZVW, PN, PM, and RGZ | 0x82      | 0xA1   |
| MSP430FR59941 | ZVW, PN, PM, and RGZ | 0x82      | 0xA2   |
| MSP430FR5992  | ZVW, PN, PM, and RGZ | 0x82      | 0xA3   |
| MSP430FR5964  | ZVW, PN, PM, and RGZ | 0x82      | 0xA4   |
| MSP430FR5962  | ZVW, PN, PM, and RGZ | 0x82      | 0xA6   |

**Table 9-40. Device Descriptor Table**

| DESCRIPTION <sup>(1)</sup> |                   | MSP430FR59xx (UART BSL) |                                | MSP430FR59941 (I <sup>2</sup> C BSL) |                                |
|----------------------------|-------------------|-------------------------|--------------------------------|--------------------------------------|--------------------------------|
|                            |                   | ADDRESS                 | VALUE                          | ADDRESS                              | VALUE                          |
| Info Block                 | Info Length       | 01A00h                  | 06h                            | 01A00h                               | 06h                            |
|                            | CRC Length        | 01A01h                  | 06h                            | 01A01h                               | 06h                            |
|                            | CRC Value         | 01A02h                  | Per unit                       | 01A02h                               | Per unit                       |
|                            |                   | 01A03h                  | Per unit                       | 01A03h                               | Per unit                       |
|                            | Device ID         | 01A04h                  | See <a href="#">Table 9-39</a> | 01A04h                               | See <a href="#">Table 9-39</a> |
|                            |                   | 01A05h                  |                                |                                      |                                |
|                            | Hardware Revision | 01A06h                  | Per unit                       | 01A06h                               | Per unit                       |
|                            | Firmware Revision | 01A07h                  | Per unit                       | 01A07h                               | Per unit                       |
| Die Record                 | Die Record Tag    | 01A08h                  | 08h                            | 01A08h                               | 08h                            |
|                            | Die Record length | 01A09h                  | 0Ah                            | 01A09h                               | 0Ah                            |
|                            | Lot/Wafer ID      | 01A0Ah                  | Per unit                       | 01A0Ah                               | Per unit                       |
|                            |                   | 01A0Bh                  | Per unit                       | 01A0Bh                               | Per unit                       |
|                            |                   | 01A0Ch                  | Per unit                       | 01A0Ch                               | Per unit                       |
|                            |                   | 01A0Dh                  | Per unit                       | 01A0Dh                               | Per unit                       |
|                            | Die X Position    | 01A0Eh                  | Per unit                       | 01A0Eh                               | Per unit                       |
|                            |                   | 01A0Fh                  | Per unit                       | 01A0Fh                               | Per unit                       |
|                            | Die Y Position    | 01A10h                  | Per unit                       | 01A10h                               | Per unit                       |
|                            |                   | 01A11h                  | Per unit                       | 01A11h                               | Per unit                       |
|                            | Test Results      | 01A12h                  | Per unit                       | 01A12h                               | Per unit                       |
|                            |                   | 01A13h                  | Per unit                       | 01A13h                               | Per unit                       |

**Table 9-40. Device Descriptor Table (continued)**

| DESCRIPTION <sup>(1)</sup> |                                                | MSP430FR59xx (UART BSL) |          | MSP430FR59941 (I <sup>2</sup> C BSL) |          |
|----------------------------|------------------------------------------------|-------------------------|----------|--------------------------------------|----------|
|                            |                                                | ADDRESS                 | VALUE    | ADDRESS                              | VALUE    |
| ADC12 Calibration          | ADC12 Calibration Tag                          | 01A14h                  | 11h      | 01A14h                               | 11h      |
|                            | ADC12 Calibration Length                       | 01A15h                  | 10h      | 01A15h                               | 10h      |
|                            | ADC Gain Factor <sup>(2)</sup>                 | 01A16h                  | Per unit | 01A16h                               | Per unit |
|                            |                                                | 01A17h                  | Per unit | 01A17h                               | Per unit |
|                            | ADC Offset <sup>(3)</sup>                      | 01A18h                  | Per unit | 01A18h                               | Per unit |
|                            |                                                | 01A19h                  | Per unit | 01A19h                               | Per unit |
|                            | ADC 1.2-V Reference<br>Temperature Sensor 30°C | 01A1Ah                  | Per unit | 01A1Ah                               | Per unit |
|                            |                                                | 01A1Bh                  | Per unit | 01A1Bh                               | Per unit |
|                            | ADC 1.2-V Reference<br>Temperature Sensor 85°C | 01A1Ch                  | Per unit | 01A1Ch                               | Per unit |
|                            |                                                | 01A1Dh                  | Per unit | 01A1Dh                               | Per unit |
|                            | ADC 2.0-V Reference<br>Temperature Sensor 30°C | 01A1Eh                  | Per unit | 01A1Eh                               | Per unit |
|                            |                                                | 01A1Fh                  | Per unit | 01A1Fh                               | Per unit |
|                            | ADC 2.0-V Reference<br>Temperature Sensor 85°C | 01A20h                  | Per unit | 01A20h                               | Per unit |
|                            |                                                | 01A21h                  | Per unit | 01A21h                               | Per unit |
| REF Calibration            | REF Calibration Tag                            | 01A22h                  | Per unit | 01A22h                               | Per unit |
|                            |                                                | 01A23h                  | Per unit | 01A23h                               | Per unit |
|                            | REF Calibration Length                         | 01A24h                  | Per unit | 01A24h                               | Per unit |
|                            |                                                | 01A25h                  | Per unit | 01A25h                               | Per unit |
|                            | REF 1.2-V Reference                            | 01A26h                  | 12h      | 01A26h                               | 12h      |
|                            |                                                | 01A27h                  | 06h      | 01A27h                               | 06h      |
|                            | REF 2.0-V Reference                            | 01A28h                  | Per unit | 01A28h                               | Per unit |
|                            |                                                | 01A29h                  | Per unit | 01A29h                               | Per unit |
| Random Number              | 128-Bit Random Number Tag                      | 01A2Ah                  | Per unit | 01A2Ah                               | Per unit |
|                            |                                                | 01A2Bh                  | Per unit | 01A2Bh                               | Per unit |
|                            | Random Number Length                           | 01A2Ch                  | Per unit | 01A2Ch                               | Per unit |
|                            |                                                | 01A2Dh                  | Per unit | 01A2Dh                               | Per unit |
|                            | 128-Bit Random Number <sup>(4)</sup>           | 01A2Eh                  | 15h      | 01A2Eh                               | 15h      |
|                            |                                                | 01A2Fh                  | 10h      | 01A2Fh                               | 10h      |
|                            |                                                | 01A30h                  | Per unit | 01A30h                               | Per unit |
|                            |                                                | 01A31h                  | Per unit | 01A31h                               | Per unit |
|                            |                                                | 01A32h                  | Per unit | 01A32h                               | Per unit |
|                            |                                                | 01A33h                  | Per unit | 01A33h                               | Per unit |
|                            |                                                | 01A34h                  | Per unit | 01A34h                               | Per unit |
|                            |                                                | 01A35h                  | Per unit | 01A35h                               | Per unit |
|                            |                                                | 01A36h                  | Per unit | 01A36h                               | Per unit |
|                            |                                                | 01A37h                  | Per unit | 01A37h                               | Per unit |
|                            |                                                | 01A38h                  | Per unit | 01A38h                               | Per unit |
|                            |                                                | 01A39h                  | Per unit | 01A39h                               | Per unit |
|                            |                                                | 01A3Ah                  | Per unit | 01A3Ah                               | Per unit |
|                            |                                                | 01A3Bh                  | Per unit | 01A3Bh                               | Per unit |
|                            |                                                | 01A3Ch                  | Per unit | 01A3Ch                               | Per unit |
|                            |                                                | 01A3Dh                  | Per unit | 01A3Dh                               | Per unit |
|                            |                                                | 01A3Eh                  | Per unit | 01A3Eh                               | Per unit |
|                            |                                                | 01A3Fh                  | Per unit | 01A3Fh                               | Per unit |

**Table 9-40. Device Descriptor Table (continued)**

| DESCRIPTION <sup>(1)</sup> |                             | MSP430FR59xx (UART BSL) |       | MSP430FR59941 (I <sup>2</sup> C BSL) |       |
|----------------------------|-----------------------------|-------------------------|-------|--------------------------------------|-------|
|                            |                             | ADDRESS                 | VALUE | ADDRESS                              | VALUE |
| BSL Configuration          | BSL Tag                     | 01A40h                  | 1Ch   | 01A40h                               | 1Ch   |
|                            | BSL Length                  | 01A41h                  | 02h   | 01A41h                               | 02h   |
|                            | BSL Interface               | 01A42h                  | 00h   | 01A42h                               | 01h   |
|                            | BSL Interface Configuration | 01A43h                  | 00h   | 01A43h                               | 48h   |

- (1) NA = Not applicable, Per unit = content can differ among individual units
- (2) ADC Gain: the gain correction factor is measured at room temperature using a 2.5-V external voltage reference without internal buffer (ADC12VRSEL = 0x2, 0x4, or 0xE). Other settings (for example, using internal reference) can result in different correction factors.
- (3) ADC Offset: the offset correction factor is measured at room temperature using ADC12VRSEL= 0x2 or 0x4, an external reference,  $V_{R+}$  = external 2.5 V,  $V_{R-}$  = AVSS.
- (4) 128-Bit Random Number: The random number is generated during production test using Microsoft's CryptGenRandom() function.

## 9.15 Memory Map

Table 9-41 summarizes the memory map for all device variants.

**Table 9-41. Memory Organization**

| (1)                                                                          |            | MSP430FR5994, MSP430FR5964                        | MSP430FR5992, MSP430FR5962                         |
|------------------------------------------------------------------------------|------------|---------------------------------------------------|----------------------------------------------------|
| Memory (FRAM)<br>Main: interrupt vectors and signatures<br>Main: code memory | Total size | 256KB<br>00FFFFh to 00FF80h<br>043FFFh to 004000h | 128KB<br>00FFFFh to 00FF80h<br>0023FFFh to 004000h |
| RAM<br>(shared with LEA on MSP430FR599x)                                     |            | 4KB<br>003BFFh to 002C00h                         | 4KB<br>003BFFh to 002C00h                          |
| RAM                                                                          |            | 4KB<br>002BFFh to 001C00h                         | 4KB<br>002BFFh to 001C00h                          |
| Device descriptor (TLV) (FRAM)                                               |            | 256 bytes<br>001AFFh to 001A00h                   | 256 bytes<br>001AFFh to 001A00h                    |
| Information memory (FRAM)                                                    | Info A     | 128 bytes<br>0019FFh to 001980h                   | 128 bytes<br>0019FFh to 001980h                    |
|                                                                              | Info B     | 128 bytes<br>00197Fh to 001900h                   | 128 bytes<br>00197Fh to 001900h                    |
|                                                                              | Info C     | 128 bytes<br>0018FFh to 001880h                   | 128 bytes<br>0018FFh to 001880h                    |
|                                                                              | Info D     | 128 bytes<br>00187Fh to 001800h                   | 128 bytes<br>00187Fh to 001800h                    |
| Bootloader (BSL) memory (ROM)                                                | BSL 3      | 512 bytes<br>0017FFh to 001600h                   | 512 bytes<br>0017FFh to 001600h                    |
|                                                                              | BSL 2      | 512 bytes<br>0015FFh to 001400h                   | 512 bytes<br>0015FFh to 001400h                    |
|                                                                              | BSL 1      | 512 bytes<br>0013FFh to 001200h                   | 512 bytes<br>0013FFh to 001200h                    |
|                                                                              | BSL 0      | 512 bytes<br>0011FFh to 001000h                   | 512 bytes<br>0011FFh to 001000h                    |
| Peripherals                                                                  | Size       | 4KB<br>000FFFh to 000020h                         | 4KB<br>000FFFh to 000020h                          |
| Tiny RAM                                                                     | Size       | 22 bytes<br>000001Fh to 00000Ah                   | 22 bytes<br>000001Fh to 00000Ah                    |
| Reserved                                                                     | Size       | 10 bytes<br>000009h to 000000h                    | 10 bytes<br>000009h to 000000h                     |

(1) All address space not listed is considered vacant memory.

### 9.15.1 Peripheral File Map

Table 9-42 lists the base address and offset range for the supported module registers. For complete module register descriptions, see the [MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx Family User's Guide](#).

**Table 9-42. Peripherals**

| MODULE NAME                                                  | BASE ADDRESS | OFFSET ADDRESS RANGE |
|--------------------------------------------------------------|--------------|----------------------|
| Special Functions (see <a href="#">Table 9-43</a> )          | 0100h        | 000h to 01Fh         |
| PMM (see <a href="#">Table 9-44</a> )                        | 0120h        | 000h to 01Fh         |
| FRAM Controller A (see <a href="#">Table 9-45</a> )          | 0140h        | 000h to 00Fh         |
| CRC16 (see <a href="#">Table 9-46</a> )                      | 0150h        | 000h to 007h         |
| RAM Controller (see <a href="#">Table 9-47</a> )             | 0158h        | 000h to 00Fh         |
| Watchdog (see <a href="#">Table 9-48</a> )                   | 015Ch        | 000h to 001h         |
| CS (see <a href="#">Table 9-49</a> )                         | 0160h        | 000h to 00Fh         |
| SYS (see <a href="#">Table 9-50</a> )                        | 0180h        | 000h to 01Fh         |
| Shared Reference (see <a href="#">Table 9-51</a> )           | 01B0h        | 000h to 001h         |
| Port P1, P2 (see <a href="#">Table 9-52</a> )                | 0200h        | 000h to 01Fh         |
| Port P3, P4 (see <a href="#">Table 9-53</a> )                | 0220h        | 000h to 01Fh         |
| Port P5, P6 (see <a href="#">Table 9-54</a> )                | 0240h        | 000h to 01Fh         |
| Port P7, P8 (see <a href="#">Table 9-55</a> )                | 0260h        | 000h to 01Fh         |
| Port PJ (see <a href="#">Table 9-56</a> )                    | 0320h        | 000h to 01Fh         |
| TA0 (see <a href="#">Table 9-57</a> )                        | 0340h        | 000h to 02Fh         |
| TA1 (see <a href="#">Table 9-58</a> )                        | 0380h        | 000h to 02Fh         |
| TB0 (see <a href="#">Table 9-59</a> )                        | 03C0h        | 000h to 02Fh         |
| TA2 (see <a href="#">Table 9-60</a> )                        | 0400h        | 000h to 02Fh         |
| Capacitive Touch I/O 0 (see <a href="#">Table 9-61</a> )     | 0430h        | 000h to 00Fh         |
| TA3 (see <a href="#">Table 9-62</a> )                        | 0440h        | 000h to 02Fh         |
| Capacitive Touch I/O 1 (see <a href="#">Table 9-63</a> )     | 0470h        | 000h to 00Fh         |
| Real-Time Clock (RTC_C) (see <a href="#">Table 9-64</a> )    | 04A0h        | 000h to 01Fh         |
| 32-Bit Hardware Multiplier (see <a href="#">Table 9-65</a> ) | 04C0h        | 000h to 02Fh         |
| DMA General Control (see <a href="#">Table 9-66</a> )        | 0500h        | 000h to 00Fh         |
| DMA Channel 0 (see <a href="#">Table 9-66</a> )              | 0510h        | 000h to 00Fh         |
| DMA Channel 1 (see <a href="#">Table 9-66</a> )              | 0520h        | 000h to 00Fh         |
| DMA Channel 2 (see <a href="#">Table 9-66</a> )              | 0530h        | 000h to 00Fh         |
| DMA Channel 3 (see <a href="#">Table 9-66</a> )              | 0540h        | 000h to 00Fh         |
| DMA Channel 4 (see <a href="#">Table 9-66</a> )              | 0550h        | 000h to 00Fh         |
| DMA Channel 5 (see <a href="#">Table 9-66</a> )              | 0560h        | 000h to 00Fh         |
| MPU Control (see <a href="#">Table 9-67</a> )                | 05A0h        | 000h to 00Fh         |
| eUSCI_A0 (see <a href="#">Table 9-68</a> )                   | 05C0h        | 000h to 01Fh         |
| eUSCI_A1 (see <a href="#">Table 9-69</a> )                   | 05E0h        | 000h to 01Fh         |
| eUSCI_A2 (see <a href="#">Table 9-70</a> )                   | 0600h        | 000h to 01Fh         |
| eUSCI_A3 (see <a href="#">Table 9-71</a> )                   | 0620h        | 000h to 01Fh         |
| eUSCI_B0 (see <a href="#">Table 9-72</a> )                   | 0640h        | 000h to 02Fh         |
| eUSCI_B1 (see <a href="#">Table 9-73</a> )                   | 0680h        | 000h to 02Fh         |
| eUSCI_B2 (see <a href="#">Table 9-74</a> )                   | 06C0h        | 000h to 02Fh         |
| eUSCI_B3 (see <a href="#">Table 9-75</a> )                   | 0700h        | 000h to 02Fh         |
| TA4 (see <a href="#">Table 9-76</a> )                        | 07C0h        | 000h to 02Fh         |
| ADC12_B (see <a href="#">Table 9-77</a> )                    | 0800h        | 000h to 09Fh         |

**Table 9-42. Peripherals (continued)**

| MODULE NAME                                    | BASE ADDRESS | OFFSET ADDRESS RANGE |
|------------------------------------------------|--------------|----------------------|
| Comparator_E (see <a href="#">Table 9-78</a> ) | 08C0h        | 000h to 00Fh         |
| CRC32 (see <a href="#">Table 9-79</a> )        | 0980h        | 000h to 02Fh         |
| AES (see <a href="#">Table 9-80</a> )          | 09C0h        | 000h to 00Fh         |
| LEA <sup>(1)</sup> (MSP430FR599x only)         | 0A80h        | 000h to 07Fh         |

- (1) Direct access to LEA registers is not supported, and TI recommends using the optimized [Digital Signal Processing \(DSP\) Library for MSP Microcontrollers](#) for the operations that the LEA module supports.

**Table 9-43. Special Function Registers (Base Address: 0100h)**

| REGISTER DESCRIPTION  | ACRONYM | OFFSET |
|-----------------------|---------|--------|
| SFR interrupt enable  | SFRIE1  | 00h    |
| SFR interrupt flag    | SFRIFG1 | 02h    |
| SFR reset pin control | SFRRPCR | 04h    |

**Table 9-44. PMM Registers (Base Address: 0120h)**

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|----------------------|---------|--------|
| PMM control 0        | PMMCTL0 | 00h    |
| PMM interrupt flags  | PMMIFG  | 0Ah    |
| PM5 control 0        | PM5CTL0 | 10h    |

**Table 9-45. FRAM Controller A (FRCTL\_A) Control Registers (Base Address: 0140h)**

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|----------------------|---------|--------|
| FRAM control 0       | FRCTL0  | 00h    |
| General control 0    | GCCTL0  | 04h    |
| General control 1    | GCCTL1  | 06h    |

**Table 9-46. CRC16 Registers (Base Address: 0150h)**

| REGISTER DESCRIPTION          | ACRONYM   | OFFSET |
|-------------------------------|-----------|--------|
| CRC data input                | CRC16DI   | 00h    |
| CRC data input reverse byte   | CRCDIRB   | 02h    |
| CRC initialization and result | CRCINIRES | 04h    |
| CRC result reverse byte       | CRCRESR   | 06h    |

**Table 9-47. RAM Controller Registers (Base Address: 0158h)**

| REGISTER DESCRIPTION     | ACRONYM | OFFSET |
|--------------------------|---------|--------|
| RAM controller control 0 | RCCTL0  | 00h    |

**Table 9-48. Watchdog Registers (Base Address: 015Ch)**

| REGISTER DESCRIPTION   | ACRONYM | OFFSET |
|------------------------|---------|--------|
| Watchdog timer control | WDTCTL  | 00h    |

**Table 9-49. CS Registers (Base Address: 0160h)**

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|----------------------|---------|--------|
| CS control 0         | CSCTL0  | 00h    |
| CS control 1         | CSCTL1  | 02h    |
| CS control 2         | CSCTL2  | 04h    |
| CS control 3         | CSCTL3  | 06h    |
| CS control 4         | CSCTL4  | 08h    |
| CS control 5         | CSCTL5  | 0Ah    |
| CS control 6         | CSCTL6  | 0Ch    |

**Table 9-50. SYS Registers (Base Address: 0180h)**

| REGISTER DESCRIPTION        | ACRONYM  | OFFSET |
|-----------------------------|----------|--------|
| System control              | SYSCTL   | 00h    |
| JTAG mailbox control        | SYSJMBC  | 06h    |
| JTAG mailbox input 0        | SYSJMBI0 | 08h    |
| JTAG mailbox input 1        | SYSJMBI1 | 0Ah    |
| JTAG mailbox output 0       | SYSJMBO0 | 0Ch    |
| JTAG mailbox output 1       | SYSJMBO1 | 0Eh    |
| User NMI vector generator   | SYSUNIV  | 1Ah    |
| System NMI vector generator | SYSSNIV  | 1Ch    |
| Reset vector generator      | SYSRSTIV | 1Eh    |

**Table 9-51. Shared Reference Registers (Base Address: 01B0h)**

| REGISTER DESCRIPTION     | ACRONYM | OFFSET |
|--------------------------|---------|--------|
| Shared reference control | REFCTL  | 00h    |

**Table 9-52. Port P1, P2 Registers (Base Address: 0200h)**

| REGISTER DESCRIPTION          | ACRONYM | OFFSET |
|-------------------------------|---------|--------|
| Port P1 input                 | P1IN    | 00h    |
| Port P1 output                | P1OUT   | 02h    |
| Port P1 direction             | P1DIR   | 04h    |
| Port P1 resistor enable       | P1REN   | 06h    |
| Port P1 selection 0           | P1SEL0  | 0Ah    |
| Port P1 selection 1           | P1SEL1  | 0Ch    |
| Port P1 interrupt vector word | P1IV    | 0Eh    |
| Port P1 complement selection  | P1SELC  | 16h    |
| Port P1 interrupt edge select | P1IES   | 18h    |
| Port P1 interrupt enable      | P1IE    | 1Ah    |
| Port P1 interrupt flag        | P1IFG   | 1Ch    |
| Port P2 input                 | P2IN    | 01h    |
| Port P2 output                | P2OUT   | 03h    |
| Port P2 direction             | P2DIR   | 05h    |
| Port P2 resistor enable       | P2REN   | 07h    |
| Port P2 selection 0           | P2SEL0  | 0Bh    |
| Port P2 selection 1           | P2SEL1  | 0Dh    |
| Port P2 complement selection  | P2SELC  | 17h    |
| Port P2 interrupt vector word | P2IV    | 1Eh    |
| Port P2 interrupt edge select | P2IES   | 19h    |
| Port P2 interrupt enable      | P2IE    | 1Bh    |
| Port P2 interrupt flag        | P2IFG   | 1Dh    |

**Table 9-53. Port P3, P4 Registers (Base Address: 0220h)**

| REGISTER DESCRIPTION          | ACRONYM | OFFSET |
|-------------------------------|---------|--------|
| Port P3 input                 | P3IN    | 00h    |
| Port P3 output                | P3OUT   | 02h    |
| Port P3 direction             | P3DIR   | 04h    |
| Port P3 resistor enable       | P3REN   | 06h    |
| Port P3 selection 0           | P3SEL0  | 0Ah    |
| Port P3 selection 1           | P3SEL1  | 0Ch    |
| Port P3 interrupt vector word | P3IV    | 0Eh    |
| Port P3 complement selection  | P3SELC  | 16h    |
| Port P3 interrupt edge select | P3IES   | 18h    |
| Port P3 interrupt enable      | P3IE    | 1Ah    |
| Port P3 interrupt flag        | P3IFG   | 1Ch    |
| Port P4 input                 | P4IN    | 01h    |
| Port P4 output                | P4OUT   | 03h    |
| Port P4 direction             | P4DIR   | 05h    |
| Port P4 resistor enable       | P4REN   | 07h    |
| Port P4 selection 0           | P4SEL0  | 0Bh    |
| Port P4 selection 1           | P4SEL1  | 0Dh    |
| Port P4 complement selection  | P4SELC  | 17h    |
| Port P4 interrupt vector word | P4IV    | 1Eh    |
| Port P4 interrupt edge select | P4IES   | 19h    |
| Port P4 interrupt enable      | P4IE    | 1Bh    |
| Port P4 interrupt flag        | P4IFG   | 1Dh    |

**Table 9-54. Port P5, P6 Registers (Base Address: 0240h)**

| REGISTER DESCRIPTION          | ACRONYM | OFFSET |
|-------------------------------|---------|--------|
| Port P5 input                 | P5IN    | 00h    |
| Port P5 output                | P5OUT   | 02h    |
| Port P5 direction             | P5DIR   | 04h    |
| Port P5 resistor enable       | P5REN   | 06h    |
| Port P5 selection 0           | P5SEL0  | 0Ah    |
| Port P5 selection 1           | P5SEL1  | 0Ch    |
| Port P5 interrupt vector word | P5IV    | 0Eh    |
| Port P5 complement selection  | P5SELC  | 16h    |
| Port P5 interrupt edge select | P5IES   | 18h    |
| Port P5 interrupt enable      | P5IE    | 1Ah    |
| Port P5 interrupt flag        | P5IFG   | 1Ch    |
| Port P6 input                 | P6IN    | 01h    |
| Port P6 output                | P6OUT   | 03h    |
| Port P6 direction             | P6DIR   | 05h    |
| Port P6 resistor enable       | P6REN   | 07h    |
| Port P6 selection 0           | P6SEL0  | 0Bh    |
| Port P6 selection 1           | P6SEL1  | 0Dh    |
| Port P6 complement selection  | P6SELC  | 17h    |
| Port P6 interrupt vector word | P6IV    | 1Eh    |
| Port P6 interrupt edge select | P6IES   | 19h    |
| Port P6 interrupt enable      | P6IE    | 1Bh    |
| Port P6 interrupt flag        | P6IFG   | 1Dh    |

**Table 9-55. Port P7, P8 Registers (Base Address: 0260h)**

| REGISTER DESCRIPTION          | ACRONYM | OFFSET |
|-------------------------------|---------|--------|
| Port P7 input                 | P7IN    | 00h    |
| Port P7 output                | P7OUT   | 02h    |
| Port P7 direction             | P7DIR   | 04h    |
| Port P7 resistor enable       | P7REN   | 06h    |
| Port P7 selection 0           | P7SEL0  | 0Ah    |
| Port P7 selection 1           | P7SEL1  | 0Ch    |
| Port P7 interrupt vector word | P7IV    | 0Eh    |
| Port P7 complement selection  | P7SELC  | 16h    |
| Port P7 interrupt edge select | P7IES   | 18h    |
| Port P7 interrupt enable      | P7IE    | 1Ah    |
| Port P7 interrupt flag        | P7IFG   | 1Ch    |
| Port P8 input                 | P8IN    | 01h    |
| Port P8 output                | P8OUT   | 03h    |
| Port P8 direction             | P8DIR   | 05h    |
| Port P8 resistor enable       | P8REN   | 07h    |
| Port P8 selection 0           | P8SEL0  | 0Bh    |
| Port P8 selection 1           | P8SEL1  | 0Dh    |
| Port P8 complement selection  | P8SELC  | 17h    |
| Port P8 interrupt vector word | P8IV    | 1Eh    |
| Port P8 interrupt edge select | P8IES   | 19h    |
| Port P8 interrupt enable      | P8IE    | 1Bh    |
| Port P8 interrupt flag        | P8IFG   | 1Dh    |

**Table 9-56. Port PJ Registers (Base Address: 0320h)**

| REGISTER DESCRIPTION         | ACRONYM | OFFSET |
|------------------------------|---------|--------|
| Port PJ input                | PJIN    | 00h    |
| Port PJ output               | PJOUT   | 02h    |
| Port PJ direction            | PJDIR   | 04h    |
| Port PJ resistor enable      | PJREN   | 06h    |
| Port PJ selection 0          | PJSEL0  | 0Ah    |
| Port PJ selection 1          | PJSEL1  | 0Ch    |
| Port PJ complement selection | PJSELC  | 16h    |

**Table 9-57. TA0 Registers (Base Address: 0340h)**

| REGISTER DESCRIPTION      | ACRONYM  | OFFSET |
|---------------------------|----------|--------|
| TA0 control               | TA0CTL   | 00h    |
| Capture/compare control 0 | TA0CCTL0 | 02h    |
| Capture/compare control 1 | TA0CCTL1 | 04h    |
| Capture/compare control 2 | TA0CCTL2 | 06h    |
| TA0 counter               | TA0R     | 10h    |
| Capture/compare 0         | TA0CCR0  | 12h    |
| Capture/compare 1         | TA0CCR1  | 14h    |
| Capture/compare 2         | TA0CCR2  | 16h    |
| TA0 expansion 0           | TA0EX0   | 20h    |
| TA0 interrupt vector      | TA0IV    | 2Eh    |

**Table 9-58. TA1 Registers (Base Address: 0380h)**

| REGISTER DESCRIPTION      | ACRONYM  | OFFSET |
|---------------------------|----------|--------|
| TA1 control               | TA1CTL   | 00h    |
| Capture/compare control 0 | TA1CCTL0 | 02h    |
| Capture/compare control 1 | TA1CCTL1 | 04h    |
| Capture/compare control 2 | TA1CCTL2 | 06h    |
| TA1 counter               | TA1R     | 10h    |
| Capture/compare 0         | TA1CCR0  | 12h    |
| Capture/compare 1         | TA1CCR1  | 14h    |
| Capture/compare 2         | TA1CCR2  | 16h    |
| TA1 expansion 0           | TA1EX0   | 20h    |
| TA1 interrupt vector      | TA1IV    | 2Eh    |

**Table 9-59. TB0 Registers (Base Address: 03C0h)**

| REGISTER DESCRIPTION      | ACRONYM  | OFFSET |
|---------------------------|----------|--------|
| TB0 control               | TB0CTL   | 00h    |
| Capture/compare control 0 | TB0CCTL0 | 02h    |
| Capture/compare control 1 | TB0CCTL1 | 04h    |
| Capture/compare control 2 | TB0CCTL2 | 06h    |
| Capture/compare control 3 | TB0CCTL3 | 08h    |
| Capture/compare control 4 | TB0CCTL4 | 0Ah    |
| Capture/compare control 5 | TB0CCTL5 | 0Ch    |
| Capture/compare control 6 | TB0CCTL6 | 0Eh    |
| TB0 counter               | TB0R     | 10h    |
| Capture/compare 0         | TB0CCR0  | 12h    |
| Capture/compare 1         | TB0CCR1  | 14h    |
| Capture/compare 2         | TB0CCR2  | 16h    |
| Capture/compare 3         | TB0CCR3  | 18h    |
| Capture/compare 4         | TB0CCR4  | 1Ah    |
| Capture/compare 5         | TB0CCR5  | 1Ch    |
| Capture/compare 6         | TB0CCR6  | 1Eh    |
| TB0 expansion 0           | TB0EX0   | 20h    |
| TB0 interrupt vector      | TB0IV    | 2Eh    |

**Table 9-60. TA2 Registers (Base Address: 0400h)**

| REGISTER DESCRIPTION      | ACRONYM  | OFFSET |
|---------------------------|----------|--------|
| TA2 control               | TA2CTL   | 00h    |
| Capture/compare control 0 | TA2CCTL0 | 02h    |
| Capture/compare control 1 | TA2CCTL1 | 04h    |
| TA2 counter               | TA2R     | 10h    |
| Capture/compare 0         | TA2CCR0  | 12h    |
| Capture/compare 1         | TA2CCR1  | 14h    |
| TA2 expansion 0           | TA2EX0   | 20h    |
| TA2 interrupt vector      | TA2IV    | 2Eh    |

**Table 9-61. Capacitive Touch I/O 0 Registers (Base Address: 0430h)**

| REGISTER DESCRIPTION           | ACRONYM    | OFFSET |
|--------------------------------|------------|--------|
| Capacitive Touch I/O 0 control | CAPTIO0CTL | 0Eh    |

**Table 9-62. TA3 Registers (Base Address: 0440h)**

| REGISTER DESCRIPTION      | ACRONYM  | OFFSET |
|---------------------------|----------|--------|
| TA3 control               | TA3CTL   | 00h    |
| Capture/compare control 0 | TA3CCTL0 | 02h    |
| Capture/compare control 1 | TA3CCTL1 | 04h    |
| TA3 counter               | TA3R     | 10h    |
| Capture/compare 0         | TA3CCR0  | 12h    |
| Capture/compare 1         | TA3CCR1  | 14h    |
| TA3 expansion 0           | TA3EX0   | 20h    |
| TA3 interrupt vector      | TA3IV    | 2Eh    |

**Table 9-63. Capacitive Touch I/O 1 Registers (Base Address: 0470h)**

| REGISTER DESCRIPTION           | ACRONYM    | OFFSET |
|--------------------------------|------------|--------|
| Capacitive Touch I/O 1 control | CAPTIO1CTL | 0Eh    |

**Table 9-64. RTC\_C Registers (Base Address: 04A0h)**

| REGISTER DESCRIPTION         | ACRONYM        | OFFSET |
|------------------------------|----------------|--------|
| RTC control 0                | RTCCTL0        | 00h    |
| RTC password                 | RTCPWD         | 01h    |
| RTC control 1                | RTCCTL1        | 02h    |
| RTC control 3                | RTCCTL3        | 03h    |
| RTC offset calibration       | RTCOCAL        | 04h    |
| RTC temperature compensation | RTCTCMP        | 06h    |
| RTC prescaler 0 control      | RTCPS0CTL      | 08h    |
| RTC prescaler 1 control      | RTCPS1CTL      | 0Ah    |
| RTC prescaler 0              | RTCPS0         | 0Ch    |
| RTC prescaler 1              | RTCPS1         | 0Dh    |
| RTC interrupt vector word    | RTCIV          | 0Eh    |
| RTC seconds/counter 1        | RTCSEC/RTCNT1  | 10h    |
| RTC minutes/counter 2        | RTCMIN/RTCNT2  | 11h    |
| RTC hours/counter 3          | RTCHOUR/RTCNT3 | 12h    |
| RTC day of week/counter 4    | RTCDOW/RTCNT4  | 13h    |
| RTC days                     | RTCDAY         | 14h    |
| RTC month                    | RTCMON         | 15h    |
| RTC year                     | RTCYEAR        | 16h    |
| RTC alarm minutes            | RTCAMIN        | 18h    |
| RTC alarm hours              | RTCAHOUR       | 19h    |
| RTC alarm day of week        | RTCADOW        | 1Ah    |
| RTC alarm days               | RTCADAY        | 1Bh    |
| Binary-to-BCD conversion     | BIN2BCD        | 1Ch    |
| BCD-to-binary conversion     | BCD2BIN        | 1Eh    |

**Table 9-65. 32-Bit Hardware Multiplier Registers (Base Address: 04C0h)**

| REGISTER DESCRIPTION                                    | ACRONYM   | OFFSET |
|---------------------------------------------------------|-----------|--------|
| 16-bit operand 1 – multiply                             | MPY       | 00h    |
| 16-bit operand 1 – signed multiply                      | MPYS      | 02h    |
| 16-bit operand 1 – multiply accumulate                  | MAC       | 04h    |
| 16-bit operand 1 – signed multiply accumulate           | MACS      | 06h    |
| 16-bit operand 2                                        | OP2       | 08h    |
| 16 × 16 result low word                                 | RESLO     | 0Ah    |
| 16 × 16 result high word                                | RESHI     | 0Ch    |
| 16 × 16 sum extension                                   | SUMEXT    | 0Eh    |
| 32-bit operand 1 – multiply low word                    | MPY32L    | 10h    |
| 32-bit operand 1 – multiply high word                   | MPY32H    | 12h    |
| 32-bit operand 1 – signed multiply low word             | MPYS32L   | 14h    |
| 32-bit operand 1 – signed multiply high word            | MPYS32H   | 16h    |
| 32-bit operand 1 – multiply accumulate low word         | MAC32L    | 18h    |
| 32-bit operand 1 – multiply accumulate high word        | MAC32H    | 1Ah    |
| 32-bit operand 1 – signed multiply accumulate low word  | MACS32L   | 1Ch    |
| 32-bit operand 1 – signed multiply accumulate high word | MACS32H   | 1Eh    |
| 32-bit operand 2 – low word                             | OP2L      | 20h    |
| 32-bit operand 2 – high word                            | OP2H      | 22h    |
| 32 × 32 result 0 – least significant word               | RES0      | 24h    |
| 32 × 32 result 1                                        | RES1      | 26h    |
| 32 × 32 result 2                                        | RES2      | 28h    |
| 32 × 32 result 3 – most significant word                | RES3      | 2Ah    |
| MPY32 control 0                                         | MPY32CTL0 | 2Ch    |

**Table 9-66. DMA Registers (Base Address DMA General Control: 0500h,  
Channel 0: 0510h, Channel 1: 0520h, Channel 2: 0530h,  
Channel 3: 0540h, Channel 4: 0550h, Channel 5: 0560h)**

| REGISTER DESCRIPTION                   | ACRONYM | OFFSET |
|----------------------------------------|---------|--------|
| DMA channel 0 control                  | DMA0CTL | 00h    |
| DMA channel 0 source address low       | DMA0SAL | 02h    |
| DMA channel 0 source address high      | DMA0SAH | 04h    |
| DMA channel 0 destination address low  | DMA0DAL | 06h    |
| DMA channel 0 destination address high | DMA0DAH | 08h    |
| DMA channel 0 transfer size            | DMA0SZ  | 0Ah    |
| DMA channel 1 control                  | DMA1CTL | 00h    |
| DMA channel 1 source address low       | DMA1SAL | 02h    |
| DMA channel 1 source address high      | DMA1SAH | 04h    |
| DMA channel 1 destination address low  | DMA1DAL | 06h    |
| DMA channel 1 destination address high | DMA1DAH | 08h    |
| DMA channel 1 transfer size            | DMA1SZ  | 0Ah    |
| DMA channel 2 control                  | DMA2CTL | 00h    |
| DMA channel 2 source address low       | DMA2SAL | 02h    |
| DMA channel 2 source address high      | DMA2SAH | 04h    |
| DMA channel 2 destination address low  | DMA2DAL | 06h    |
| DMA channel 2 destination address high | DMA2DAH | 08h    |
| DMA channel 2 transfer size            | DMA2SZ  | 0Ah    |
| DMA channel 3 control                  | DMA3CTL | 00h    |
| DMA channel 3 source address low       | DMA3SAL | 02h    |
| DMA channel 3 source address high      | DMA3SAH | 04h    |
| DMA channel 3 destination address low  | DMA3DAL | 06h    |
| DMA channel 3 destination address high | DMA3DAH | 08h    |
| DMA channel 3 transfer size            | DMA3SZ  | 0Ah    |
| DMA channel 4 control                  | DMA4CTL | 00h    |
| DMA channel 4 source address low       | DMA4SAL | 02h    |
| DMA channel 4 source address high      | DMA4SAH | 04h    |
| DMA channel 4 destination address low  | DMA4DAL | 06h    |
| DMA channel 4 destination address high | DMA4DAH | 08h    |
| DMA channel 4 transfer size            | DMA4SZ  | 0Ah    |
| DMA channel 5 control                  | DMA5CTL | 00h    |
| DMA channel 5 source address low       | DMA5SAL | 02h    |
| DMA channel 5 source address high      | DMA5SAH | 04h    |
| DMA channel 5 destination address low  | DMA5DAL | 06h    |
| DMA channel 5 destination address high | DMA5DAH | 08h    |
| DMA channel 5 transfer size            | DMA5SZ  | 0Ah    |
| DMA module control 0                   | DMACTL0 | 00h    |
| DMA module control 1                   | DMACTL1 | 02h    |
| DMA module control 2                   | DMACTL2 | 04h    |
| DMA module control 3                   | DMACTL3 | 06h    |
| DMA module control 4                   | DMACTL4 | 08h    |
| DMA interrupt vector                   | DMAIV   | 0Eh    |

**Table 9-67. MPU Control Registers (Base Address: 05A0h)**

| REGISTER DESCRIPTION                  | ACRONYM    | OFFSET |
|---------------------------------------|------------|--------|
| MPU control 0                         | MPUCTL0    | 00h    |
| MPU control 1                         | MPUCTL1    | 02h    |
| MPU segmentation border 2             | MPUSEGB2   | 04h    |
| MPU segmentation border 1             | MPUSEGB1   | 06h    |
| MPU access management                 | MPUSAM     | 08h    |
| MPU IP control 0                      | MPUIPC0    | 0Ah    |
| MPU IP encapsulation segment border 2 | MPUIPSEGB2 | 0Ch    |
| MPU IP encapsulation segment border 1 | MPUIPSEGB1 | 0Eh    |

**Table 9-68. eUSCI\_A0 Registers (Base Address: 05C0h)**

| REGISTER DESCRIPTION          | ACRONYM    | OFFSET |
|-------------------------------|------------|--------|
| eUSCI_A control word 0        | UCA0CTLW0  | 00h    |
| eUSCI_A control word 1        | UCA0CTLW1  | 02h    |
| eUSCI_A baud rate 0           | UCA0BR0    | 06h    |
| eUSCI_A baud rate 1           | UCA0BR1    | 07h    |
| eUSCI_A modulation control    | UCA0MCTLW  | 08h    |
| eUSCI_A status word           | UCA0STATW  | 0Ah    |
| eUSCI_A receive buffer        | UCA0RXBUF  | 0Ch    |
| eUSCI_A transmit buffer       | UCA0TXBUF  | 0Eh    |
| eUSCI_A LIN control           | UCA0ABCTL  | 10h    |
| eUSCI_A IrDA transmit control | UCA0IRTCTL | 12h    |
| eUSCI_A IrDA receive control  | UCA0IRRCTL | 13h    |
| eUSCI_A interrupt enable      | UCA0IE     | 1Ah    |
| eUSCI_A interrupt flags       | UCA0IFG    | 1Ch    |
| eUSCI_A interrupt vector word | UCA0IV     | 1Eh    |

**Table 9-69. eUSCI\_A1 Registers (Base Address: 05E0h)**

| REGISTER DESCRIPTION          | ACRONYM    | OFFSET |
|-------------------------------|------------|--------|
| eUSCI_A control word 0        | UCA1CTLW0  | 00h    |
| eUSCI_A control word 1        | UCA1CTLW1  | 02h    |
| eUSCI_A baud rate 0           | UCA1BR0    | 06h    |
| eUSCI_A baud rate 1           | UCA1BR1    | 07h    |
| eUSCI_A modulation control    | UCA1MCTLW  | 08h    |
| eUSCI_A status word           | UCA1STATW  | 0Ah    |
| eUSCI_A receive buffer        | UCA1RXBUF  | 0Ch    |
| eUSCI_A transmit buffer       | UCA1TXBUF  | 0Eh    |
| eUSCI_A LIN control           | UCA1ABCTL  | 10h    |
| eUSCI_A IrDA transmit control | UCA1IRTCTL | 12h    |
| eUSCI_A IrDA receive control  | UCA1IRRCTL | 13h    |
| eUSCI_A interrupt enable      | UCA1IE     | 1Ah    |
| eUSCI_A interrupt flags       | UCA1IFG    | 1Ch    |
| eUSCI_A interrupt vector word | UCA1IV     | 1Eh    |

**Table 9-70. eUSCI\_A2 Registers (Base Address:0600h)**

| REGISTER DESCRIPTION          | ACRONYM    | OFFSET |
|-------------------------------|------------|--------|
| eUSCI_A control word 0        | UCA2CTLW0  | 00h    |
| eUSCI_A control word 1        | UCA2CTLW1  | 02h    |
| eUSCI_A baud rate 0           | UCA2BR0    | 06h    |
| eUSCI_A baud rate 1           | UCA2BR1    | 07h    |
| eUSCI_A modulation control    | UCA2MCTLW  | 08h    |
| eUSCI_A status word           | UCA2STATW  | 0Ah    |
| eUSCI_A receive buffer        | UCA2RXBUF  | 0Ch    |
| eUSCI_A transmit buffer       | UCA2TXBUF  | 0Eh    |
| eUSCI_A LIN control           | UCA2ABCTL  | 10h    |
| eUSCI_A IrDA transmit control | UCA2IRTCTL | 12h    |
| eUSCI_A IrDA receive control  | UCA2IRRCTL | 13h    |
| eUSCI_A interrupt enable      | UCA2IE     | 1Ah    |
| eUSCI_A interrupt flags       | UCA2IFG    | 1Ch    |
| eUSCI_A interrupt vector word | UCA2IV     | 1Eh    |

**Table 9-71. eUSCI\_A3 Registers (Base Address:0620h)**

| REGISTER DESCRIPTION          | ACRONYM    | OFFSET |
|-------------------------------|------------|--------|
| eUSCI_A control word 0        | UCA3CTLW0  | 00h    |
| eUSCI_A control word 1        | UCA3CTLW1  | 02h    |
| eUSCI_A baud rate 0           | UCA3BR0    | 06h    |
| eUSCI_A baud rate 1           | UCA3BR1    | 07h    |
| eUSCI_A modulation control    | UCA3MCTLW  | 08h    |
| eUSCI_A status word           | UCA3STATW  | 0Ah    |
| eUSCI_A receive buffer        | UCA3RXBUF  | 0Ch    |
| eUSCI_A transmit buffer       | UCA3TXBUF  | 0Eh    |
| eUSCI_A LIN control           | UCA3ABCTL  | 10h    |
| eUSCI_A IrDA transmit control | UCA3IRTCTL | 12h    |
| eUSCI_A IrDA receive control  | UCA3IRRCTL | 13h    |
| eUSCI_A interrupt enable      | UCA3IE     | 1Ah    |
| eUSCI_A interrupt flags       | UCA3IFG    | 1Ch    |
| eUSCI_A interrupt vector word | UCA3IV     | 1Eh    |

**Table 9-72. eUSCI\_B0 Registers (Base Address: 0640h)**

| REGISTER DESCRIPTION           | ACRONYM     | OFFSET |
|--------------------------------|-------------|--------|
| eUSCI_B control word 0         | UCB0CTLW0   | 00h    |
| eUSCI_B control word 1         | UCB0CTLW1   | 02h    |
| eUSCI_B bit rate 0             | UCB0BR0     | 06h    |
| eUSCI_B bit rate 1             | UCB0BR1     | 07h    |
| eUSCI_B status word            | UCB0STATW   | 08h    |
| eUSCI_B byte counter threshold | UCB0TBCNT   | 0Ah    |
| eUSCI_B receive buffer         | UCB0RXBUF   | 0Ch    |
| eUSCI_B transmit buffer        | UCB0TXBUF   | 0Eh    |
| eUSCI_B I2C own address 0      | UCB0I2COA0  | 14h    |
| eUSCI_B I2C own address 1      | UCB0I2COA1  | 16h    |
| eUSCI_B I2C own address 2      | UCB0I2COA2  | 18h    |
| eUSCI_B I2C own address 3      | UCB0I2COA3  | 1Ah    |
| eUSCI_B received address       | UCB0ADDRX   | 1Ch    |
| eUSCI_B address mask           | UCB0ADDMASK | 1Eh    |
| eUSCI I2C slave address        | UCB0I2CSA   | 20h    |
| eUSCI interrupt enable         | UCB0IE      | 2Ah    |
| eUSCI interrupt flags          | UCB0IFG     | 2Ch    |
| eUSCI interrupt vector word    | UCB0IV      | 2Eh    |

**Table 9-73. eUSCI\_B1 Registers (Base Address: 0680h)**

| REGISTER DESCRIPTION           | ACRONYM     | OFFSET |
|--------------------------------|-------------|--------|
| eUSCI_B control word 0         | UCB1CTLW0   | 00h    |
| eUSCI_B control word 1         | UCB1CTLW1   | 02h    |
| eUSCI_B bit rate 0             | UCB1BR0     | 06h    |
| eUSCI_B bit rate 1             | UCB1BR1     | 07h    |
| eUSCI_B status word            | UCB1STATW   | 08h    |
| eUSCI_B byte counter threshold | UCB1TBCNT   | 0Ah    |
| eUSCI_B receive buffer         | UCB1RXBUF   | 0Ch    |
| eUSCI_B transmit buffer        | UCB1TXBUF   | 0Eh    |
| eUSCI_B I2C own address 0      | UCB1I2COA0  | 14h    |
| eUSCI_B I2C own address 1      | UCB1I2COA1  | 16h    |
| eUSCI_B I2C own address 2      | UCB1I2COA2  | 18h    |
| eUSCI_B I2C own address 3      | UCB1I2COA3  | 1Ah    |
| eUSCI_B received address       | UCB1ADDRX   | 1Ch    |
| eUSCI_B address mask           | UCB1ADDMASK | 1Eh    |
| eUSCI I2C slave address        | UCB1I2CSA   | 20h    |
| eUSCI interrupt enable         | UCB1IE      | 2Ah    |
| eUSCI interrupt flags          | UCB1IFG     | 2Ch    |
| eUSCI interrupt vector word    | UCB1IV      | 2Eh    |

**Table 9-74. eUSCI\_B2 Registers (Base Address: 06C0h)**

| REGISTER DESCRIPTION           | ACRONYM     | OFFSET |
|--------------------------------|-------------|--------|
| eUSCI_B control word 0         | UCB2CTLW0   | 00h    |
| eUSCI_B control word 1         | UCB2CTLW1   | 02h    |
| eUSCI_B bit rate 0             | UCB2BR0     | 06h    |
| eUSCI_B bit rate 1             | UCB2BR1     | 07h    |
| eUSCI_B status word            | UCB2STATW   | 08h    |
| eUSCI_B byte counter threshold | UCB2TBCNT   | 0Ah    |
| eUSCI_B receive buffer         | UCB2RXBUF   | 0Ch    |
| eUSCI_B transmit buffer        | UCB2TXBUF   | 0Eh    |
| eUSCI_B I2C own address 0      | UCB2I2COA0  | 14h    |
| eUSCI_B I2C own address 1      | UCB2I2COA1  | 16h    |
| eUSCI_B I2C own address 2      | UCB2I2COA2  | 18h    |
| eUSCI_B I2C own address 3      | UCB2I2COA3  | 1Ah    |
| eUSCI_B received address       | UCB2ADDRX   | 1Ch    |
| eUSCI_B address mask           | UCB2ADDMASK | 1Eh    |
| eUSCI I2C slave address        | UCB2I2CSA   | 20h    |
| eUSCI interrupt enable         | UCB2IE      | 2Ah    |
| eUSCI interrupt flags          | UCB2IFG     | 2Ch    |
| eUSCI interrupt vector word    | UCB2IV      | 2Eh    |

**Table 9-75. eUSCI\_B3 Registers (Base Address: 0700h)**

| REGISTER DESCRIPTION           | ACRONYM     | OFFSET |
|--------------------------------|-------------|--------|
| eUSCI_B control word 0         | UCB3CTLW0   | 00h    |
| eUSCI_B control word 1         | UCB3CTLW1   | 02h    |
| eUSCI_B bit rate 0             | UCB3BR0     | 06h    |
| eUSCI_B bit rate 1             | UCB3BR1     | 07h    |
| eUSCI_B status word            | UCB3STATW   | 08h    |
| eUSCI_B byte counter threshold | UCB3TBCNT   | 0Ah    |
| eUSCI_B receive buffer         | UCB3RXBUF   | 0Ch    |
| eUSCI_B transmit buffer        | UCB3TXBUF   | 0Eh    |
| eUSCI_B I2C own address 0      | UCB3I2COA0  | 14h    |
| eUSCI_B I2C own address 1      | UCB3I2COA1  | 16h    |
| eUSCI_B I2C own address 2      | UCB3I2COA2  | 18h    |
| eUSCI_B I2C own address 3      | UCB3I2COA3  | 1Ah    |
| eUSCI_B received address       | UCB3ADDRX   | 1Ch    |
| eUSCI_B address mask           | UCB3ADDMASK | 1Eh    |
| eUSCI I2C slave address        | UCB3I2CSA   | 20h    |
| eUSCI interrupt enable         | UCB3IE      | 2Ah    |
| eUSCI interrupt flags          | UCB3IFG     | 2Ch    |
| eUSCI interrupt vector word    | UCB3IV      | 2Eh    |

**Table 9-76. TA4 Registers (Base Address: 07C0h)**

| REGISTER DESCRIPTION      | ACRONYM  | OFFSET |
|---------------------------|----------|--------|
| TA4 control               | TA4CTL   | 00h    |
| Capture/compare control 0 | TA4CCTL0 | 02h    |
| Capture/compare control 1 | TA4CCTL1 | 04h    |
| TA4 counter               | TA4R     | 10h    |
| Capture/compare 0         | TA4CCR0  | 12h    |
| Capture/compare 1         | TA4CCR1  | 14h    |
| TA4 expansion 0           | TA4EX0   | 20h    |
| TA4 interrupt vector      | TA4IV    | 2Eh    |

**Table 9-77. ADC12\_B Registers (Base Address: 0800h)**

| REGISTER DESCRIPTION                              | ACRONYM     | OFFSET |
|---------------------------------------------------|-------------|--------|
| ADC12_B control 0                                 | ADC12CTL0   | 00h    |
| ADC12_B control 1                                 | ADC12CTL1   | 02h    |
| ADC12_B control 2                                 | ADC12CTL2   | 04h    |
| ADC12_B control 3                                 | ADC12CTL3   | 06h    |
| ADC12_B window comparator low threshold register  | ADC12LO     | 08h    |
| ADC12_B window comparator high threshold register | ADC12HI     | 0Ah    |
| ADC12_B interrupt flag register 0                 | ADC12IFGR0  | 0Ch    |
| ADC12_B interrupt flag register 1                 | ADC12IFGR1  | 0Eh    |
| ADC12_B interrupt flag register 2                 | ADC12IFGR2  | 10h    |
| ADC12_B interrupt enable register 0               | ADC12IER0   | 12h    |
| ADC12_B interrupt enable register 1               | ADC12IER1   | 14h    |
| ADC12_B interrupt enable register 2               | ADC12IER2   | 16h    |
| ADC12_B interrupt vector                          | ADC12IV     | 18h    |
| ADC12_B memory control 0                          | ADC12MCTL0  | 20h    |
| ADC12_B memory control 1                          | ADC12MCTL1  | 22h    |
| ADC12_B memory control 2                          | ADC12MCTL2  | 24h    |
| ADC12_B memory control 3                          | ADC12MCTL3  | 26h    |
| ADC12_B memory control 4                          | ADC12MCTL4  | 28h    |
| ADC12_B memory control 5                          | ADC12MCTL5  | 2Ah    |
| ADC12_B memory control 6                          | ADC12MCTL6  | 2Ch    |
| ADC12_B memory control 7                          | ADC12MCTL7  | 2Eh    |
| ADC12_B memory control 8                          | ADC12MCTL8  | 30h    |
| ADC12_B memory control 9                          | ADC12MCTL9  | 32h    |
| ADC12_B memory control 10                         | ADC12MCTL10 | 34h    |
| ADC12_B memory control 11                         | ADC12MCTL11 | 36h    |
| ADC12_B memory control 12                         | ADC12MCTL12 | 38h    |
| ADC12_B memory control 13                         | ADC12MCTL13 | 3Ah    |
| ADC12_B memory control 14                         | ADC12MCTL14 | 3Ch    |
| ADC12_B memory control 15                         | ADC12MCTL15 | 3Eh    |
| ADC12_B memory control 16                         | ADC12MCTL16 | 40h    |
| ADC12_B memory control 17                         | ADC12MCTL17 | 42h    |
| ADC12_B memory control 18                         | ADC12MCTL18 | 44h    |
| ADC12_B memory control 19                         | ADC12MCTL19 | 46h    |
| ADC12_B memory control 20                         | ADC12MCTL20 | 48h    |
| ADC12_B memory control 21                         | ADC12MCTL21 | 4Ah    |

**Table 9-77. ADC12\_B Registers (Base Address: 0800h) (continued)**

| REGISTER DESCRIPTION      | ACRONYM     | OFFSET |
|---------------------------|-------------|--------|
| ADC12_B memory control 22 | ADC12MCTL22 | 4Ch    |
| ADC12_B memory control 23 | ADC12MCTL23 | 4Eh    |
| ADC12_B memory control 24 | ADC12MCTL24 | 50h    |
| ADC12_B memory control 25 | ADC12MCTL25 | 52h    |
| ADC12_B memory control 26 | ADC12MCTL26 | 54h    |
| ADC12_B memory control 27 | ADC12MCTL27 | 56h    |
| ADC12_B memory control 28 | ADC12MCTL28 | 58h    |
| ADC12_B memory control 29 | ADC12MCTL29 | 5Ah    |
| ADC12_B memory control 30 | ADC12MCTL30 | 5Ch    |
| ADC12_B memory control 31 | ADC12MCTL31 | 5Eh    |
| ADC12_B memory 0          | ADC12MEM0   | 60h    |
| ADC12_B memory 1          | ADC12MEM1   | 62h    |
| ADC12_B memory 2          | ADC12MEM2   | 64h    |
| ADC12_B memory 3          | ADC12MEM3   | 66h    |
| ADC12_B memory 4          | ADC12MEM4   | 68h    |
| ADC12_B memory 5          | ADC12MEM5   | 6Ah    |
| ADC12_B memory 6          | ADC12MEM6   | 6Ch    |
| ADC12_B memory 7          | ADC12MEM7   | 6Eh    |
| ADC12_B memory 8          | ADC12MEM8   | 70h    |
| ADC12_B memory 9          | ADC12MEM9   | 72h    |
| ADC12_B memory 10         | ADC12MEM10  | 74h    |
| ADC12_B memory 11         | ADC12MEM11  | 76h    |
| ADC12_B memory 12         | ADC12MEM12  | 78h    |
| ADC12_B memory 13         | ADC12MEM13  | 7Ah    |
| ADC12_B memory 14         | ADC12MEM14  | 7Ch    |
| ADC12_B memory 15         | ADC12MEM15  | 7Eh    |
| ADC12_B memory 16         | ADC12MEM16  | 80h    |
| ADC12_B memory 17         | ADC12MEM17  | 82h    |
| ADC12_B memory 18         | ADC12MEM18  | 84h    |
| ADC12_B memory 19         | ADC12MEM19  | 86h    |
| ADC12_B memory 20         | ADC12MEM20  | 88h    |
| ADC12_B memory 21         | ADC12MEM21  | 8Ah    |
| ADC12_B memory 22         | ADC12MEM22  | 8Ch    |
| ADC12_B memory 23         | ADC12MEM23  | 8Eh    |
| ADC12_B memory 24         | ADC12MEM24  | 90h    |
| ADC12_B memory 25         | ADC12MEM25  | 92h    |
| ADC12_B memory 26         | ADC12MEM26  | 94h    |
| ADC12_B memory 27         | ADC12MEM27  | 96h    |
| ADC12_B memory 28         | ADC12MEM28  | 98h    |
| ADC12_B memory 29         | ADC12MEM29  | 9Ah    |
| ADC12_B memory 30         | ADC12MEM30  | 9Ch    |
| ADC12_B memory 31         | ADC12MEM31  | 9Eh    |

**Table 9-78. Comparator\_E Registers (Base Address: 08C0h)**

| REGISTER DESCRIPTION               | ACRONYM | OFFSET |
|------------------------------------|---------|--------|
| Comparator_E control 0             | CECTL0  | 00h    |
| Comparator_E control 1             | CECTL1  | 02h    |
| Comparator_E control 2             | CECTL2  | 04h    |
| Comparator_E control 3             | CECTL3  | 06h    |
| Comparator_E interrupt             | CEINT   | 0Ch    |
| Comparator_E interrupt vector word | CEIV    | 0Eh    |

**Table 9-79. CRC32 Registers (Base Address: 0980h)**

| REGISTER DESCRIPTION                   | ACRONYM       | OFFSET |
|----------------------------------------|---------------|--------|
| CRC32 data input                       | CRC32DIW0     | 00h    |
| Reserved                               |               | 02h    |
| Reserved                               |               | 04h    |
| CRC32 data input reverse               | CRC32DIRBW0   | 06h    |
| CRC32 initialization and result word 0 | CRC32INIRESW0 | 08h    |
| CRC32 initialization and result word 1 | CRC32INIRESW1 | 0Ah    |
| CRC32 result reverse word 1            | CRC32RESRW1   | 0Ch    |
| CRC32 result reverse word 0            | CRC32RESRW0   | 0Eh    |
| CRC16 data input                       | CRC16DIW0     | 10h    |
| Reserved                               |               | 12h    |
| Reserved                               |               | 14h    |
| CRC16 data input reverse               | CRC16DIRBW0   | 16h    |
| CRC16 initialization and result word 0 | CRC16INIRESW0 | 18h    |
| Reserved                               |               | 1Ah    |
| Reserved                               |               | 1Ch    |
| CRC16 result reverse word 0            | CRC16RESRW0   | 1Eh    |
| Reserved                               |               | 20h    |
| Reserved                               |               | 22h    |
| Reserved                               |               | 24h    |
| Reserved                               |               | 26h    |
| Reserved                               |               | 28h    |
| Reserved                               |               | 2Ah    |
| Reserved                               |               | 2Ch    |
| Reserved                               |               | 2Eh    |

**Table 9-80. AES Accelerator Registers (Base Address: 09C0h)**

| REGISTER DESCRIPTION                       | ACRONYM  | OFFSET |
|--------------------------------------------|----------|--------|
| AES accelerator control 0                  | AESACTL0 | 00h    |
| Reserved                                   |          | 02h    |
| AES accelerator status                     | AESASTAT | 04h    |
| AES accelerator key                        | AESAKEY  | 06h    |
| AES accelerator data in                    | AESADIN  | 008h   |
| AES accelerator data out                   | AESADOUT | 00Ah   |
| AES accelerator XORed data in              | AESAXDIN | 00Ch   |
| AES accelerator XORed data in (no trigger) | AESAXIN  | 00Eh   |

## 9.16 Identification

### 9.16.1 Revision Identification

The device revision information is shown as part of the top-side marking on the device package. The device-specific errata sheet describes these markings. For links to all of the errata sheets for the devices in this data sheet, see [Section 11.4](#).

The hardware revision is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the Hardware Revision entry in [Section 9.14](#).

### 9.16.2 Device Identification

The device type can be identified from the top-side marking on the device package. The device-specific errata sheet describes these markings. For links to all of the errata sheets for the devices in this data sheet, see [Section 11.4](#).

A device identification value is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the Device ID entry in [Section 9.14](#).

### 9.16.3 JTAG Identification

Programming through the JTAG interface, including reading and identifying the JTAG ID, is described in detail in [MSP430 Programming With the JTAG Interface](#).

## 10 Applications, Implementation, and Layout

### Note

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Device Connection and Layout Fundamentals

This section discusses the recommended guidelines when designing with the MSP MCU. These guidelines are to make sure that the device has proper connections for powering, programming, debugging, and optimum analog performance.

#### 10.1.1 Power Supply Decoupling and Bulk Capacitors

TI recommends connecting a combination of a 1- $\mu$ F plus a 100-nF low-ESR ceramic decoupling capacitor to each AVCC and DVCC pin. Higher-value capacitors may be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimeters). Additionally, TI recommends separated grounds with a single-point connection for better noise isolation from digital to analog circuits on the board and to achieve high analog accuracy.

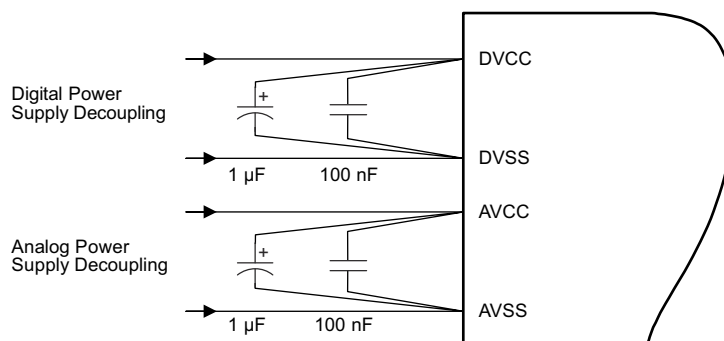


Figure 10-1. Power Supply Decoupling

#### 10.1.2 External Oscillator

Depending on the device variant (see [Section 6](#)), the device can support a low-frequency crystal (32 kHz) on the LFXT pins, a high-frequency crystal on the HFXT pins, or both. External bypass capacitors for the crystal oscillator pins are required.

It is also possible to apply digital clock signals to the LFXIN and HFXIN input pins that meet the specifications of the respective oscillator if the appropriate LFXTBYPASS or HFXTBYPASS mode is selected. In this case, the associated LFXOUT and HFXOUT pins can be used for other purposes. If they are left unused, they must be terminated according to [Section 7.6](#).

[Figure 10-2](#) shows a typical connection diagram.

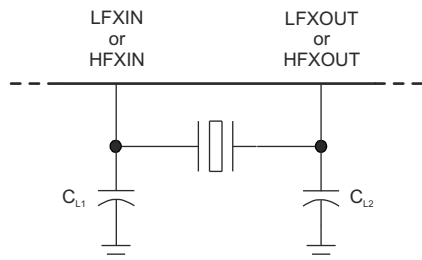


Figure 10-2. Typical Crystal Connection

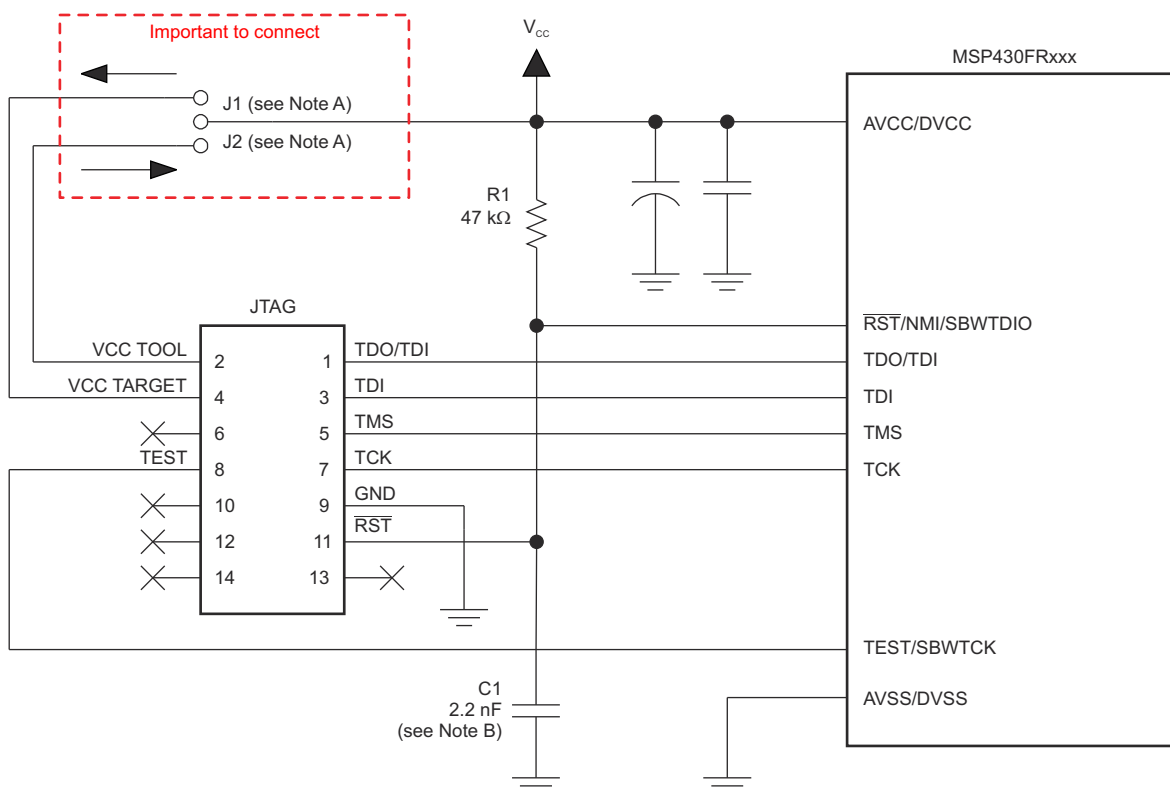
See [MSP430 32-kHz Crystal Oscillators](#) for more information on selecting, testing, and designing a crystal oscillator with the MSP MCUs.

### 10.1.3 JTAG

With the proper connections, the debugger and a hardware JTAG interface (such as the MSP-FET or MSP-FET430UIF) can be used to program and debug code on the target board. In addition, the connections also support the MSP-GANG production programmers, thus providing an easy way to program prototype boards, if desired. [Figure 10-3](#) shows the connections between the 14-pin JTAG connector and the target device required to support in-system programming and debugging for 4-wire JTAG communication. [Figure 10-4](#) shows the connections for 2-wire JTAG mode (Spy-Bi-Wire).

The connections for the MSP-FET and MSP-FET430UIF interface modules and the MSP-GANG are identical. Both can supply VCC to the target board (through pin 2). In addition, the MSP-FET and MSP-FET430UIF interface modules and MSP-GANG have a VCC sense feature that, if used, requires an alternate connection (pin 4 instead of pin 2). The VCC-sense feature senses the local VCC present on the target board (that is, a battery or other local power supply) and adjusts the output signals accordingly. [Figure 10-3](#) and [Figure 10-4](#) show a jumper block that supports both scenarios of supplying VCC to the target board. If this flexibility is not required, the desired VCC connections may be hard-wired to eliminate the jumper block. Pins 2 and 4 must not be connected at the same time.

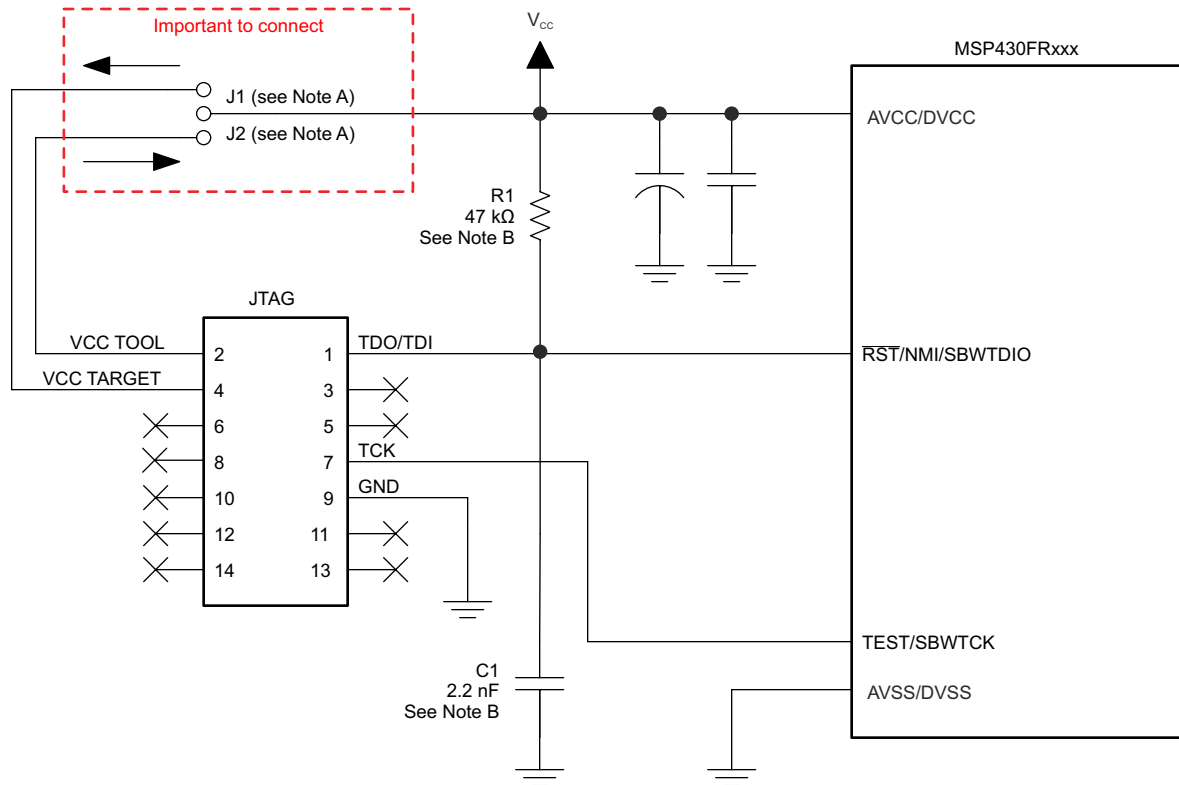
For additional design information regarding the JTAG interface, see the [MSP430 Hardware Tools User's Guide](#).



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- A. If a local target power supply is used, make connection J1. If power from the debug or programming adapter is used, make connection J2.
- B. The upper limit for C1 is 2.2 nF when using current TI tools.

**Figure 10-3. Signal Connections for 4-Wire JTAG Communication**



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- A. Make connection J1 if a local target power supply is used, or make connection J2 if the target is powered from the debug or programming adapter.
- B. The device  $\overline{\text{RST}}/\text{NMI}/\text{SBWDIO}$  pin is used in 2-wire mode for bidirectional communication with the device during JTAG access, and any capacitance that is attached to this signal may affect the ability to establish a connection with the device. The upper limit for C1 is 2.2 nF when using current TI tools.

**Figure 10-4. Signal Connections for 2-Wire JTAG Communication (Spy-Bi-Wire)**

#### 10.1.4 Reset

The reset pin can be configured as a reset function (default) or as an NMI function in the SFRRPCR register.

In reset mode, the  $\overline{\text{RST}}/\text{NMI}$  pin is active low, and a pulse applied to this pin that meets the reset timing specifications generates a BOR-type device reset.

Setting SYSNMI causes the  $\overline{\text{RST}}/\text{NMI}$  pin to be configured as an external NMI source. The external NMI is edge sensitive, and its edge is selectable by SYSNMIIES. Setting the NMIIE enables the interrupt of the external NMI. When an external NMI event occurs, the NMIIFG is set.

The  $\overline{\text{RST}}/\text{NMI}$  pin can have either a pullup or pulldown that is enabled or not. SYSRSTUP selects either pullup or pulldown, and SYSRSTRE causes the pullup (default) or pulldown to be enabled (default) or not. If the  $\overline{\text{RST}}/\text{NMI}$  pin is unused, it is required either to select and enable the internal pullup or to connect an external 47-kΩ pullup resistor to the  $\overline{\text{RST}}/\text{NMI}$  pin with a 10-nF pulldown capacitor. The pulldown capacitor should not exceed 2.2 nF when using devices with Spy-Bi-Wire interface in Spy-Bi-Wire mode or in 4-wire JTAG mode with TI tools like FET interfaces or GANG programmers.

See the [MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx Family User's Guide](#) for more information on the referenced control registers and bits.

#### 10.1.5 Unused Pins

For details on the connection of unused pins, see [Section 7.6](#).

## 10.1.6 General Layout Recommendations

- Proper grounding and short traces for external crystal to reduce parasitic capacitance. See [MSP430 32-kHz Crystal Oscillators](#) for recommended layout guidelines.
- Proper bypass capacitors on DVCC, AVCC, and reference pins if used.
- Avoid routing any high-frequency signal close to an analog signal line. For example, keep digital switching signals such as PWM or JTAG signals away from the oscillator circuit.
- Proper ESD level protection should be considered to protect the device from unintended high-voltage electrostatic discharge. See [MSP430 System-Level ESD Considerations](#) for guidelines.

## 10.1.7 Do's and Don'ts

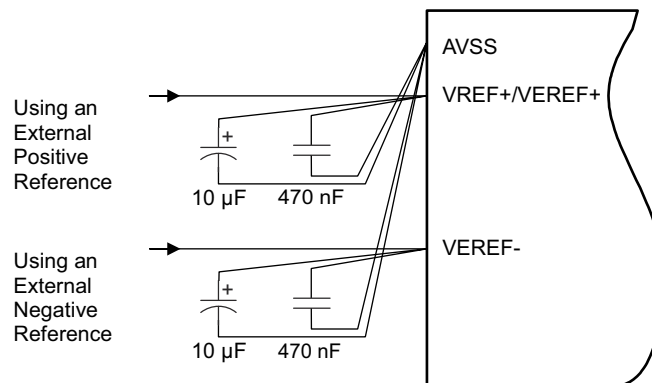
TI recommends powering AVCC and DVCC pins from the same source. At a minimum, during power up, power down, and device operation, the voltage difference between AVCC and DVCC must not exceed the limits specified in [Section 8.1](#). Exceeding the specified limits may cause malfunction of the device, including erroneous writes to RAM and FRAM.

## 10.2 Peripheral- and Interface-Specific Design Information

### 10.2.1 ADC12\_B Peripheral

#### 10.2.1.1 Partial Schematic

[Figure 10-5](#) shows the recommended decoupling circuit when an external voltage reference is used. The internal reference module has a maximum drive current as specified in the  $I_{O(VREF+)}$  parameter of the REF module.



**Figure 10-5. ADC12\_B Grounding and Noise Considerations**

#### 10.2.1.2 Design Requirements

As with any high-resolution ADC, the appropriate printed-circuit-board layout and grounding techniques should be followed to eliminate ground loops, unwanted parasitic effects, and noise.

Ground loops are formed when return current from the ADC flows through paths that are common with other analog or digital circuitry. If care is not taken, this current can generate small, unwanted offset voltages that can add to or subtract from the reference or input voltages of the ADC. The general guidelines in [Section 10.1.1](#), combined with the connections shown in [Section 10.2.1.1](#), prevent these offsets.

In addition to grounding, ripple and noise spikes on the power-supply lines that are caused by digital switching or switching power supplies can corrupt the conversion result. TI recommends a noise-free design using separate analog and digital ground planes with a single-point connection to achieve high accuracy.

The reference voltage must be a stable voltage for accurate measurements. The capacitor values that are selected in the general guidelines filter out the high- and low-frequency ripple before the reference voltage enters the device. In this case, the 10-µF capacitor is used to buffer the reference pin and filter any low-frequency ripple. A 470-nF bypass capacitor filters out any high-frequency noise.

### 10.2.1.3 Detailed Design Procedure

For additional design information, see [Designing With the MSP430FR58xx, FR59xx, FR68xx, and FR69xx ADC](#).

### 10.2.1.4 Layout Guidelines

Components that are shown in the partial schematic (see [Figure 10-5](#)) should be placed as close as possible to the respective device pins. Avoid long traces, because they add additional parasitic capacitance, inductance, and resistance on the signal.

Avoid routing analog input signals close to a high-frequency pin (for example, a high-frequency PWM), because the high-frequency switching can be coupled into the analog signal.

If differential mode is used for the ADC12\_B, the analog differential input signals must be routed closely together to minimize the effect of noise on the resulting signal.

## 11 Device and Documentation Support

### 11.1 Getting Started

For more information on the MSP family of microcontrollers and the tools and libraries that are available to help with your development, visit the [MSP430 ultra-low-power sensing & measurement MCUs overview](#).

### 11.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP MCU devices. Each MSP MCU commercial family member has one of two prefixes: MSP or XMS. These prefixes represent evolutionary stages of product development from engineering prototypes (XMS) through fully qualified production devices (MSP).

**XMS** – Experimental device that is not necessarily representative of the final device's electrical specifications

**MSP** – Fully qualified production device

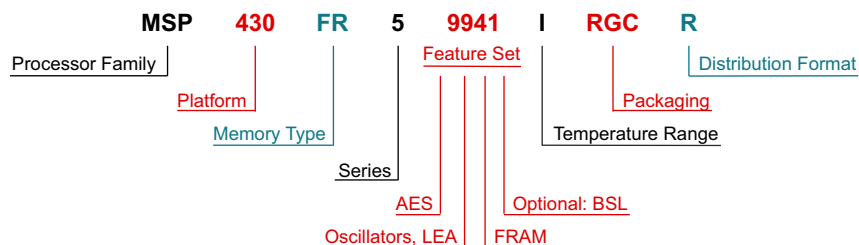
XMS devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

MSP devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (XMS) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the temperature range, package type, and distribution format. [Figure 11-1](#) provides a legend for reading the complete device name.



|                            |                                                                |                                                                                 |                                                     |                                                                              |
|----------------------------|----------------------------------------------------------------|---------------------------------------------------------------------------------|-----------------------------------------------------|------------------------------------------------------------------------------|
| <b>Processor Family</b>    | MSP = Mixed Signal Processor<br>XMS = Experimental Silicon     |                                                                                 |                                                     |                                                                              |
| <b>Platform</b>            | 430 = TI's 16-bit MSP430 Low-Power Microcontroller Platform    |                                                                                 |                                                     |                                                                              |
| <b>Memory Type</b>         | FR = FRAM                                                      |                                                                                 |                                                     |                                                                              |
| <b>Series</b>              | 5 = Up to 16 MHz without LCD                                   |                                                                                 |                                                     |                                                                              |
| <b>Feature Set</b>         | <b>First Digit: AES</b><br>9 = AES                             | <b>Second Digit: Oscillators, LEA</b><br>9 = HFXT/LFXT and LEA<br>6 = HFXT/LFXT | <b>Third Digit: FRAM (KB)</b><br>4 = 256<br>2 = 128 | <b>Optional Fourth Digit: BSL</b><br>1 = I <sup>2</sup> C<br>No value = UART |
| <b>Temperature Range</b>   | I = -40°C to 85°C                                              |                                                                                 |                                                     |                                                                              |
| <b>Packaging</b>           | <a href="http://www.ti.com/packaging">www.ti.com/packaging</a> |                                                                                 |                                                     |                                                                              |
| <b>Distribution Format</b> | T = Small reel<br>R = Large reel<br>No markings = Tube or tray |                                                                                 |                                                     |                                                                              |

**Figure 11-1. Device Nomenclature**

## 11.3 Tools and Software

All MSP microcontrollers are supported by a wide variety of software and hardware development tools. Tools are available from TI and various third parties. See them all at [MSP430 ultra-low-power MCUs – Design & development](#).

Table 11-1 lists the debug features supported in the hardware of the MSP430FR599x and MSP430FR596x MCUs. See the [Code Composer Studio™ IDE for MSP430™ MCUs User's Guide](#) for details on the available hardware features.

**Table 11-1. Debug Features**

| MSP ARCHITECTURE | 4-WIRE JTAG | 2-WIRE JTAG | BREAK-POINTS (N) | RANGE BREAK-POINTS | CLOCK CONTROL | STATE SEQUENCER | TRACE BUFFER | LPMx.5 DEBUGGING SUPPORT | EnergyTrace++ TECHNOLOGY |
|------------------|-------------|-------------|------------------|--------------------|---------------|-----------------|--------------|--------------------------|--------------------------|
| MSP430Xv2        | Yes         | Yes         | 3                | Yes                | Yes           | No              | No           | Yes                      | Yes                      |

EnergyTrace™ technology is supported with Code Composer Studio IDE version 6.0 and newer. It requires specialized debugger circuitry, which is supported with the second-generation onboard eZ-FET flash emulation tool and second-generation stand-alone MSP-FET JTAG emulator. See the following documents for detailed information:

[MSP430 Advanced Power Optimizations: ULP Advisor™ and EnergyTrace™ Technology](#)

[Advanced Debugging Using the Enhanced Emulation Module \(EEM\) With Code Composer Studio™ IDE](#)

[MSP430™ Hardware Tools User's Guide](#)

### Design Kits and Evaluation Modules

#### MSP430FR5994 LaunchPad™ Development Kit

The MSP-EXP430FR5994 LaunchPad Development Kit is an easy-to-use Evaluation Module (EVM) for the MSP430FR5994 microcontroller (MCU). It contains everything needed to start developing on the ultra-low-power MSP430FRx FRAM microcontroller platform, including an onboard debug probe for programming, debugging, and energy measurements.

#### 80-pin Target Development Board and MSP-FET Programmer Bundle for MSP430F599x MCUs

The target socket boards allow easy programming and debugging of the device using JTAG. They also feature header pinouts for prototyping. Target socket boards are orderable individually or as a kit with the JTAG programmer and debugger included.

#### 80-pin Target Development Board for MSP430F599x MCUs

The MSP-TS430PN80B is a stand-alone 80-pin ZIF socket target board that is used to program and debug the MSP430 MCU in-system through the JTAG interface or the Spy Bi-Wire (2-wire JTAG) protocol.

### Software

#### MSP430Ware™ Software

MSP430Ware software is a collection of code examples, data sheets, and other design resources for all MSP430 devices delivered in a convenient package. In addition to providing a complete collection of existing MSP430 MCU design resources, MSP430Ware software also includes a high-level API called MSP Driver Library. This library makes it easy to program MSP430 hardware. MSP430Ware software is available as a component of CCS or as a stand-alone package.

#### MSP430FR599x, MSP430FR596x Code Examples

C code examples are available for every MSP device that configures each of the integrated peripherals for various application needs.

### [Capacitive Touch Software Library](#)

Free C libraries for enabling capacitive touch capabilities on MSP430 MCUs. The library features several capacitive touch implementations including the RO and RC method. In addition to the full C code libraries, hardware design considerations are also provided as a simple guide for including capacitive touch into any MSP430 MCU-based application.

### [MSP EnergyTrace Technology](#)

EnergyTrace technology for MSP430 microcontrollers is an energy-based code analysis tool that measures and displays the application's energy profile and helps to optimize it for ultra-low-power consumption.

### [MSP Driver Library](#)

Driver Library's abstracted API keeps you above the bits and bytes of the MSP430 hardware by providing easy-to-use function calls. Thorough documentation is delivered through a helpful API Guide, which includes details on each function call and the recognized parameters. Developers can use Driver Library functions to write complete projects with minimal overhead.

### [Digital Signal Processing Library](#)

The Texas Instruments Digital Signal Processing library is a set of highly optimized functions to perform many common signal processing operations on fixed-point numbers for MSP430™ and MSP432™ microcontrollers. This function set is typically used for applications where processing-intensive transforms are done in real-time for minimal energy and with very high accuracy. This library's optimal utilization of the MSP families' intrinsic hardware for fixed-point math allows for significant performance gains.

### [FRAM Embedded Software Utilities for MSP Ultra-Low-Power Microcontrollers](#)

The FRAM Utilities is designed to grow as a collection of embedded software utilities that leverage the ultra-low-power and virtually unlimited write endurance of FRAM. The utilities are available for MSP430FRxx FRAM microcontrollers and provide example code to help start application development. Included utilities include Compute Through Power Loss (CTPL). CTPL is utility API set that enables ease of use with LPMx.5 low-power modes and a powerful shutdown mode that allows an application to save and restore critical system components when a power loss is detected.

## **Development Tools**

### [Code Composer Studio Integrated Development Environment for MSP Microcontrollers](#)

Code Composer Studio is an integrated development environment (IDE) that supports all MSP microcontroller devices. Code Composer Studio comprises a suite of embedded software utilities used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features.

### [Uniflash Standalone Flash Tool for TI Microcontrollers](#)

CCS Uniflash is a stand-alone tool used to program on-chip flash memory on TI MCUs and on-board flash memory for Sitara processors. Uniflash has a GUI, command line, and scripting interface. CCS Uniflash is available free of charge.

### [MSP MCU Programmer and Debugger](#)

The MSP-FET is a powerful emulation development tool – often called a debug probe – that allows users to quickly begin application development on MSP low-power microcontrollers (MCU). Creating MCU software usually requires downloading the resulting binary program to the MSP device for validation and debugging. The MSP-FET provides a debug communication pathway between a host computer and the target MSP.

## MSP-GANG Production Programmer

The MSP Gang Programmer is an MSP430 or MSP432 device programmer that can program up to eight identical MSP430 or MSP432 Flash or FRAM devices at the same time. The MSP Gang Programmer connects to a host PC using a standard RS-232 or USB connection and provides flexible programming options that allow the user to fully customize the process. The MSP Gang Programmer is provided with an expansion board, called the Gang Splitter, that implements the interconnections between the MSP Gang Programmer and multiple target devices.

## 11.4 Documentation Support

The following documents describe the MSP430FR599x and MSP430FR596x MCUs. Copies of these documents are available on the Internet at [www.ti.com](http://www.ti.com).

### Receiving notification of document updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on [ti.com](http://ti.com) (for links to the product folders, see [Section 11.5](#)). In the upper right corner, click the "Alert me" button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

### Errata

#### [MSP430FR5994 Device Erratasheet](#)

Describes the known exceptions to the functional specifications.

#### [MSP430FR59941 Device Erratasheet](#)

Describes the known exceptions to the functional specifications.

#### [MSP430FR5992 Device Erratasheet](#)

Describes the known exceptions to the functional specifications.

#### [MSP430FR5964 Device Erratasheet](#)

Describes the known exceptions to the functional specifications.

#### [MSP430FR5962 Device Erratasheet](#)

Describes the known exceptions to the functional specifications.

### User's Guides

#### [MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx Family User's Guide](#)

Detailed description of all modules and peripherals available in this device family.

#### [MSP430 FRAM Device Bootloader \(BSL\) User's Guide](#)

The bootloader (BSL) on MSP430 MCUs lets users communicate with embedded memory in the MSP430 MCU during the prototyping phase, final production, and in service. Both the programmable memory (FRAM) and the data memory (RAM) can be modified as required.

#### [MSP430 Programming With the JTAG Interface](#)

This document describes the functions that are required to erase, program, and verify the memory module of the MSP430 flash-based and FRAM-based microcontroller families using the JTAG communication port. In addition, it describes how to program the JTAG access security fuse that is available on all MSP430 devices. This document describes device access using both the standard 4-wire JTAG interface and the 2-wire JTAG interface, which is also referred to as Spy-Bi-Wire (SBW).

## MSP430 Hardware Tools User's Guide

This manual describes the hardware of the TI MSP-FET430 Flash Emulation Tool (FET). The FET is the program development tool for the MSP430 ultra-low-power microcontroller. Both available interface types, the parallel port interface and the USB interface, are described.

## Application Reports

### MSP430 32-kHz Crystal Oscillators

Selection of the right crystal, correct load circuit, and proper board layout are important for a stable crystal oscillator. This application report summarizes crystal oscillator function and explains the parameters to select the correct crystal for MSP430 ultra-low-power operation. In addition, hints and examples for correct board layout are given. The document also contains detailed information on the possible oscillator tests to ensure stable oscillator operation in mass production.

### MSP430 System-Level ESD Considerations

System-level ESD has become increasingly demanding with silicon technology scaling towards lower voltages and the need for designing cost-effective and ultra-low-power components. This application report addresses three different ESD topics to help board designers and OEMs understand and design robust system-level designs: (1) Component-level ESD testing and system-level ESD testing; (2) General design guidelines for system-level ESD protection at different levels; (3) Introduction to System Efficient ESD Design (SEED).

### MSP430™ FRAM Technology – How To and Best Practices

FRAM is a nonvolatile memory technology that behaves similar to SRAM while enabling a whole host of new applications, but also changing the way firmware should be designed. This application report outlines the how to and best practices of using FRAM technology in MSP430 MCUs from an embedded software development perspective. It discusses how to implement a memory layout according to application-specific code, constant, data space requirements, the use of FRAM to optimize application energy consumption, and the use of the Memory Protection Unit (MPU) to maximize application robustness by protecting the program code against unintended write accesses.

## 11.5 Related Links

**Table 11-2** lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 11-2. Related Links**

| PARTS         | PRODUCT FOLDER             | ORDER NOW                  | TECHNICAL DOCUMENTS        | TOOLS & SOFTWARE           | SUPPORT & COMMUNITY        |
|---------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| MSP430FR5994  | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| MSP430FR59941 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| MSP430FR5992  | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| MSP430FR5964  | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| MSP430FR5962  | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |

## 11.6 Support Resources

**TI E2E™ support forums** are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

## 11.7 Trademarks

LaunchPad™, MSP430Ware™, MSP430™, Code Composer Studio™, EnergyTrace™, MSP432™, and TI E2E™ are trademarks of Texas Instruments.

Arm® and Cortex® are registered trademarks of Arm Limited.

All trademarks are the property of their respective owners.

## 11.8 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.9 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

## 11.10 Glossary

**TI Glossary** This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number             | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-----------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">MSP430FR5962IPMR</a>  | Active        | Production           | LQFP (PM)   64   | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5962              |
| MSP430FR5962IPMR.A                | Active        | Production           | LQFP (PM)   64   | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5962              |
| MSP430FR5962IPMR.B                | Active        | Production           | LQFP (PM)   64   | 1000   LARGE T&R      | -           | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5962              |
| <a href="#">MSP430FR5962IPNR</a>  | Active        | Production           | LQFP (PN)   80   | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5962              |
| MSP430FR5962IPNR.A                | Active        | Production           | LQFP (PN)   80   | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5962              |
| MSP430FR5962IPNR.B                | Active        | Production           | LQFP (PN)   80   | 1000   LARGE T&R      | -           | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5962              |
| <a href="#">MSP430FR5962IRGZR</a> | Active        | Production           | VQFN (RGZ)   48  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5962              |
| MSP430FR5962IRGZR.A               | Active        | Production           | VQFN (RGZ)   48  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5962              |
| <a href="#">MSP430FR5962IZVWR</a> | Active        | Production           | NFBGA (ZVW)   87 | 1000   LARGE T&R      | Yes         | SNAGCU                               | Level-3-260C-168 HR               | -40 to 85    | FR5962              |
| MSP430FR5962IZVWR.A               | Active        | Production           | NFBGA (ZVW)   87 | 1000   LARGE T&R      | Yes         | SNAGCU                               | Level-3-260C-168 HR               | -40 to 85    | FR5962              |
| <a href="#">MSP430FR5964IPMR</a>  | Active        | Production           | LQFP (PM)   64   | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5964              |
| MSP430FR5964IPMR.A                | Active        | Production           | LQFP (PM)   64   | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5964              |
| MSP430FR5964IPMR.B                | Active        | Production           | LQFP (PM)   64   | 1000   LARGE T&R      | -           | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5964              |
| <a href="#">MSP430FR5964IPNR</a>  | Active        | Production           | LQFP (PN)   80   | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5964              |
| MSP430FR5964IPNR.A                | Active        | Production           | LQFP (PN)   80   | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5964              |
| MSP430FR5964IPNR.B                | Active        | Production           | LQFP (PN)   80   | 1000   LARGE T&R      | -           | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5964              |
| <a href="#">MSP430FR5964IRGZR</a> | Active        | Production           | VQFN (RGZ)   48  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5964              |
| MSP430FR5964IRGZR.A               | Active        | Production           | VQFN (RGZ)   48  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5964              |
| <a href="#">MSP430FR5964IZVWR</a> | Active        | Production           | NFBGA (ZVW)   87 | 1000   LARGE T&R      | Yes         | SNAGCU                               | Level-3-260C-168 HR               | -40 to 85    | FR5964              |
| MSP430FR5964IZVWR.A               | Active        | Production           | NFBGA (ZVW)   87 | 1000   LARGE T&R      | Yes         | SNAGCU                               | Level-3-260C-168 HR               | -40 to 85    | FR5964              |
| <a href="#">MSP430FR5992IPMR</a>  | Active        | Production           | LQFP (PM)   64   | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5992              |
| MSP430FR5992IPMR.A                | Active        | Production           | LQFP (PM)   64   | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5992              |
| MSP430FR5992IPMR.B                | Active        | Production           | LQFP (PM)   64   | 1000   LARGE T&R      | -           | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5992              |
| <a href="#">MSP430FR5992IPNR</a>  | Active        | Production           | LQFP (PN)   80   | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5992              |
| MSP430FR5992IPNR.A                | Active        | Production           | LQFP (PN)   80   | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5992              |
| MSP430FR5992IPNR.B                | Active        | Production           | LQFP (PN)   80   | 1000   LARGE T&R      | -           | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5992              |
| <a href="#">MSP430FR5992IRGZR</a> | Active        | Production           | VQFN (RGZ)   48  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5992              |
| MSP430FR5992IRGZR.A               | Active        | Production           | VQFN (RGZ)   48  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5992              |
| <a href="#">MSP430FR5992IZVWR</a> | Active        | Production           | NFBGA (ZVW)   87 | 1000   LARGE T&R      | Yes         | SNAGCU                               | Level-3-260C-168 HR               | -40 to 85    | FR5992              |

| Orderable part number              | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier   | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------------|---------------|----------------------|------------------|-------------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| MSP430FR5992IZVWR.A                | Active        | Production           | NFBGA (ZVW)   87 | 1000   LARGE T&R        | Yes         | SNAGCU                               | Level-3-260C-168 HR               | -40 to 85    | FR5992              |
| <a href="#">MSP430FR59941IPM</a>   | Active        | Production           | LQFP (PM)   64   | 160   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR59941             |
| MSP430FR59941IPM.A                 | Active        | Production           | LQFP (PM)   64   | 160   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR59941             |
| MSP430FR59941IPM.B                 | Active        | Production           | LQFP (PM)   64   | 160   JEDEC TRAY (10+1) | -           | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR59941             |
| <a href="#">MSP430FR59941IPMR</a>  | Active        | Production           | LQFP (PM)   64   | 1000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR59941             |
| MSP430FR59941IPMR.A                | Active        | Production           | LQFP (PM)   64   | 1000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR59941             |
| <a href="#">MSP430FR59941IPN</a>   | Active        | Production           | LQFP (PN)   80   | 119   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR59941             |
| MSP430FR59941IPN.A                 | Active        | Production           | LQFP (PN)   80   | 119   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR59941             |
| MSP430FR59941IPN.B                 | Active        | Production           | LQFP (PN)   80   | 119   JEDEC TRAY (10+1) | -           | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR59941             |
| <a href="#">MSP430FR59941IPNR</a>  | Active        | Production           | LQFP (PN)   80   | 1000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR59941             |
| MSP430FR59941IPNR.A                | Active        | Production           | LQFP (PN)   80   | 1000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR59941             |
| <a href="#">MSP430FR59941IRGZR</a> | Active        | Production           | VQFN (RGZ)   48  | 2500   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR59941             |
| MSP430FR59941IRGZR.A               | Active        | Production           | VQFN (RGZ)   48  | 2500   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR59941             |
| <a href="#">MSP430FR59941IRGZT</a> | Active        | Production           | VQFN (RGZ)   48  | 250   SMALL T&R         | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR59941             |
| MSP430FR59941IRGZT.A               | Active        | Production           | VQFN (RGZ)   48  | 250   SMALL T&R         | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR59941             |
| <a href="#">MSP430FR59941IZVW</a>  | Active        | Production           | NFBGA (ZVW)   87 | 250   JEDEC TRAY (10+1) | Yes         | SNAGCU                               | Level-3-260C-168 HR               | -40 to 85    | FR59941             |
| MSP430FR59941IZVW.A                | Active        | Production           | NFBGA (ZVW)   87 | 250   JEDEC TRAY (10+1) | Yes         | SNAGCU                               | Level-3-260C-168 HR               | -40 to 85    | FR59941             |
| <a href="#">MSP430FR59941IZVWR</a> | Active        | Production           | NFBGA (ZVW)   87 | 1000   LARGE T&R        | Yes         | SNAGCU                               | Level-3-260C-168 HR               | -40 to 85    | FR59941             |
| MSP430FR59941IZVWR.A               | Active        | Production           | NFBGA (ZVW)   87 | 1000   LARGE T&R        | Yes         | SNAGCU                               | Level-3-260C-168 HR               | -40 to 85    | FR59941             |
| <a href="#">MSP430FR59941IPM</a>   | Active        | Production           | LQFP (PM)   64   | 160   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5994              |
| MSP430FR59941IPM.A                 | Active        | Production           | LQFP (PM)   64   | 160   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5994              |
| MSP430FR59941IPM.B                 | Active        | Production           | LQFP (PM)   64   | 160   JEDEC TRAY (10+1) | -           | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5994              |
| <a href="#">MSP430FR59941IPMR</a>  | Active        | Production           | LQFP (PM)   64   | 1000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5994              |

| Orderable part number             | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier   | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-----------------------------------|---------------|----------------------|------------------|-------------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| MSP430FR5994IPMR.A                | Active        | Production           | LQFP (PM)   64   | 1000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5994              |
| MSP430FR5994IPMR.B                | Active        | Production           | LQFP (PM)   64   | 1000   LARGE T&R        | -           | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5994              |
| MSP430FR5994IPMRG4                | Active        | Production           | LQFP (PM)   64   | 1000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5994              |
| MSP430FR5994IPMRG4.A              | Active        | Production           | LQFP (PM)   64   | 1000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5994              |
| <a href="#">MSP430FR5994IPN</a>   | Active        | Production           | LQFP (PN)   80   | 119   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5994              |
| MSP430FR5994IPN.A                 | Active        | Production           | LQFP (PN)   80   | 119   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5994              |
| MSP430FR5994IPN.B                 | Active        | Production           | LQFP (PN)   80   | 119   JEDEC TRAY (10+1) | -           | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5994              |
| <a href="#">MSP430FR5994IPNR</a>  | Active        | Production           | LQFP (PN)   80   | 1000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5994              |
| MSP430FR5994IPNR.A                | Active        | Production           | LQFP (PN)   80   | 1000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5994              |
| MSP430FR5994IPNR.B                | Active        | Production           | LQFP (PN)   80   | 1000   LARGE T&R        | -           | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5994              |
| <a href="#">MSP430FR5994IRGZR</a> | Active        | Production           | VQFN (RGZ)   48  | 2500   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5994              |
| MSP430FR5994IRGZR.A               | Active        | Production           | VQFN (RGZ)   48  | 2500   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5994              |
| <a href="#">MSP430FR5994IRGZT</a> | Active        | Production           | VQFN (RGZ)   48  | 250   SMALL T&R         | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5994              |
| MSP430FR5994IRGZT.A               | Active        | Production           | VQFN (RGZ)   48  | 250   SMALL T&R         | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5994              |
| <a href="#">MSP430FR5994IZVW</a>  | Active        | Production           | NFBGA (ZVW)   87 | 250   JEDEC TRAY (10+1) | Yes         | SNAGCU                               | Level-3-260C-168 HR               | -40 to 85    | FR5994              |
| MSP430FR5994IZVW.A                | Active        | Production           | NFBGA (ZVW)   87 | 250   JEDEC TRAY (10+1) | Yes         | SNAGCU                               | Level-3-260C-168 HR               | -40 to 85    | FR5994              |
| MSP430FR5994IZVW.B                | Active        | Production           | NFBGA (ZVW)   87 | 250   JEDEC TRAY (10+1) | -           | SNAGCU                               | Level-3-260C-168 HR               | -40 to 85    | FR5994              |
| <a href="#">MSP430FR5994IZVWR</a> | Active        | Production           | NFBGA (ZVW)   87 | 1000   LARGE T&R        | Yes         | SNAGCU                               | Level-3-260C-168 HR               | -40 to 85    | FR5994              |
| MSP430FR5994IZVWR.A               | Active        | Production           | NFBGA (ZVW)   87 | 1000   LARGE T&R        | Yes         | SNAGCU                               | Level-3-260C-168 HR               | -40 to 85    | FR5994              |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

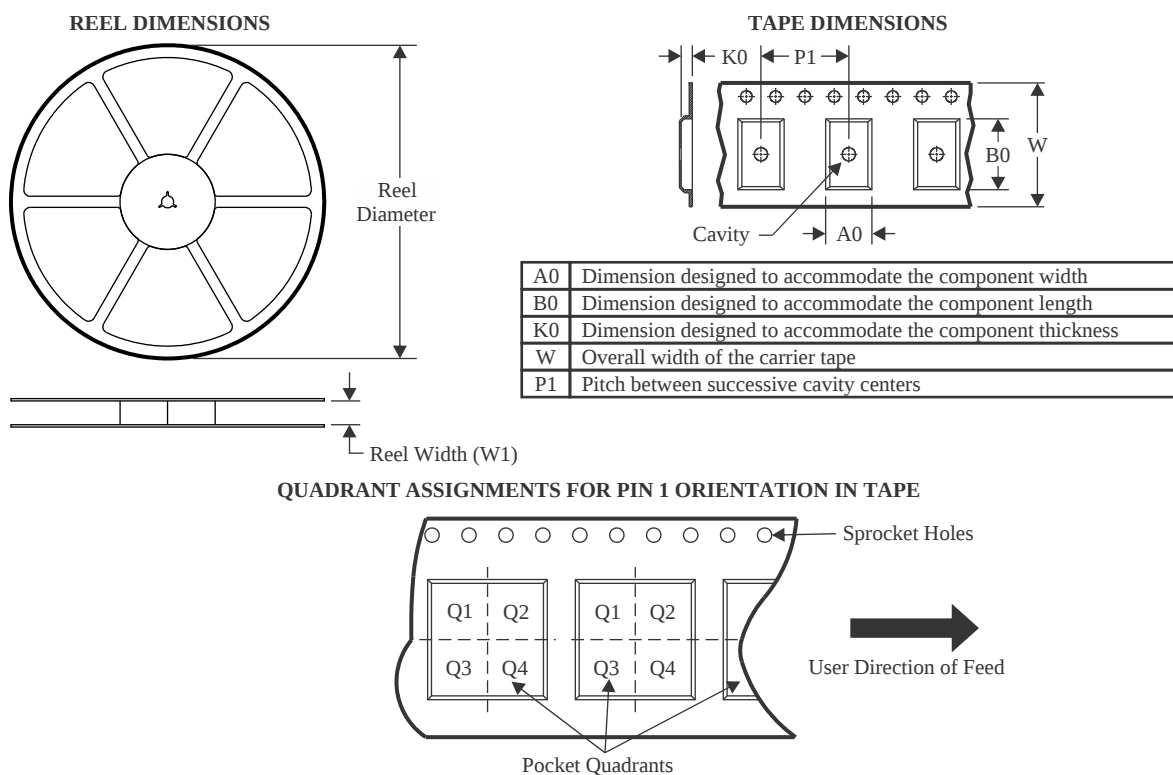
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION

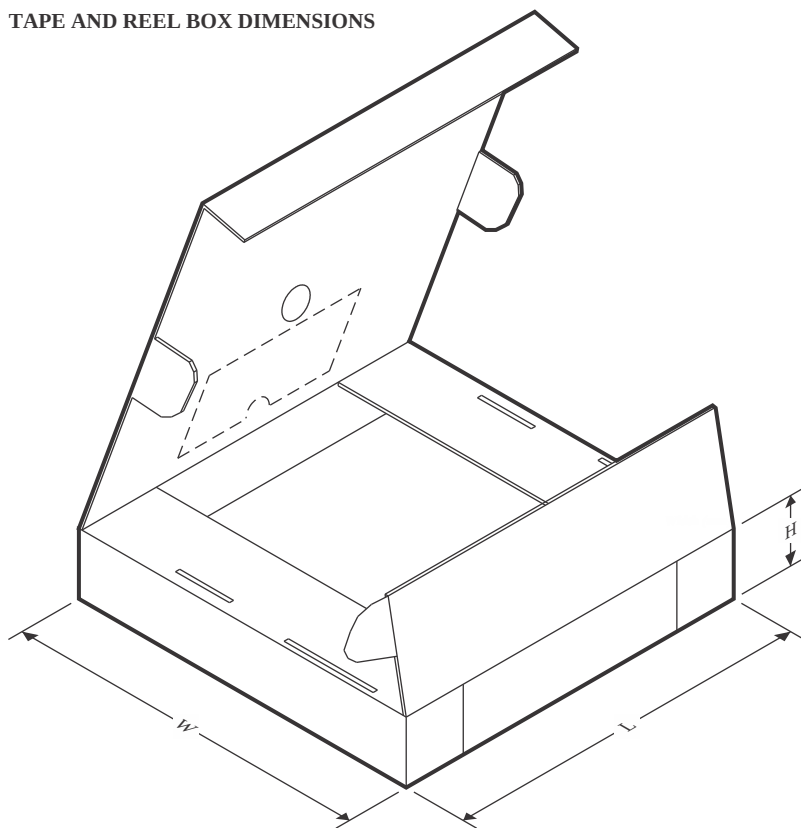


\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| MSP430FR5962IPMR   | LQFP         | PM              | 64   | 1000 | 330.0              | 24.4               | 13.0    | 13.0    | 2.1     | 16.0    | 24.0   | Q2            |
| MSP430FR5962IPNR   | LQFP         | PN              | 80   | 1000 | 330.0              | 24.4               | 16.0    | 16.0    | 2.0     | 24.0    | 24.0   | Q2            |
| MSP430FR5962IRGZR  | VQFN         | RGZ             | 48   | 2500 | 330.0              | 16.4               | 7.3     | 7.3     | 1.1     | 12.0    | 16.0   | Q2            |
| MSP430FR5962IZVWR  | NFBGA        | ZVW             | 87   | 1000 | 330.0              | 16.4               | 6.3     | 6.3     | 1.5     | 12.0    | 16.0   | Q1            |
| MSP430FR5964IPMR   | LQFP         | PM              | 64   | 1000 | 330.0              | 24.4               | 13.0    | 13.0    | 2.1     | 16.0    | 24.0   | Q2            |
| MSP430FR5964IPNR   | LQFP         | PN              | 80   | 1000 | 330.0              | 24.4               | 16.0    | 16.0    | 2.0     | 24.0    | 24.0   | Q2            |
| MSP430FR5964IRGZR  | VQFN         | RGZ             | 48   | 2500 | 330.0              | 16.4               | 7.3     | 7.3     | 1.1     | 12.0    | 16.0   | Q2            |
| MSP430FR5964IZVWR  | NFBGA        | ZVW             | 87   | 1000 | 330.0              | 16.4               | 6.3     | 6.3     | 1.5     | 12.0    | 16.0   | Q1            |
| MSP430FR5992IPMR   | LQFP         | PM              | 64   | 1000 | 330.0              | 24.4               | 13.0    | 13.0    | 2.1     | 16.0    | 24.0   | Q2            |
| MSP430FR5992IPNR   | LQFP         | PN              | 80   | 1000 | 330.0              | 24.4               | 16.0    | 16.0    | 2.0     | 24.0    | 24.0   | Q2            |
| MSP430FR5992IRGZR  | VQFN         | RGZ             | 48   | 2500 | 330.0              | 16.4               | 7.3     | 7.3     | 1.1     | 12.0    | 16.0   | Q2            |
| MSP430FR5992IZVWR  | NFBGA        | ZVW             | 87   | 1000 | 330.0              | 16.4               | 6.3     | 6.3     | 1.5     | 12.0    | 16.0   | Q1            |
| MSP430FR59941IPMR  | LQFP         | PM              | 64   | 1000 | 330.0              | 24.4               | 13.0    | 13.0    | 2.1     | 16.0    | 24.0   | Q2            |
| MSP430FR59941IPNR  | LQFP         | PN              | 80   | 1000 | 330.0              | 24.4               | 16.0    | 16.0    | 2.0     | 24.0    | 24.0   | Q2            |
| MSP430FR59941IRGZR | VQFN         | RGZ             | 48   | 2500 | 330.0              | 16.4               | 7.3     | 7.3     | 1.1     | 12.0    | 16.0   | Q2            |
| MSP430FR59941IRGZT | VQFN         | RGZ             | 48   | 250  | 180.0              | 16.4               | 7.3     | 7.3     | 1.1     | 12.0    | 16.0   | Q2            |

| Device             | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| MSP430FR59941IZVWR | NFBGA        | ZVW             | 87   | 1000 | 330.0              | 16.4               | 6.3     | 6.3     | 1.5     | 12.0    | 16.0   | Q1            |
| MSP430FR5994IPMR   | LQFP         | PM              | 64   | 1000 | 330.0              | 24.4               | 13.0    | 13.0    | 2.1     | 16.0    | 24.0   | Q2            |
| MSP430FR5994IPMRG4 | LQFP         | PM              | 64   | 1000 | 330.0              | 24.4               | 13.0    | 13.0    | 2.1     | 16.0    | 24.0   | Q2            |
| MSP430FR5994IPNR   | LQFP         | PN              | 80   | 1000 | 330.0              | 24.4               | 16.0    | 16.0    | 2.0     | 24.0    | 24.0   | Q2            |
| MSP430FR5994IRGZR  | VQFN         | RGZ             | 48   | 2500 | 330.0              | 16.4               | 7.3     | 7.3     | 1.1     | 12.0    | 16.0   | Q2            |
| MSP430FR5994IRGZT  | VQFN         | RGZ             | 48   | 250  | 180.0              | 16.4               | 7.3     | 7.3     | 1.1     | 12.0    | 16.0   | Q2            |
| MSP430FR5994IZVWR  | NFBGA        | ZVW             | 87   | 1000 | 330.0              | 16.4               | 6.3     | 6.3     | 1.5     | 12.0    | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



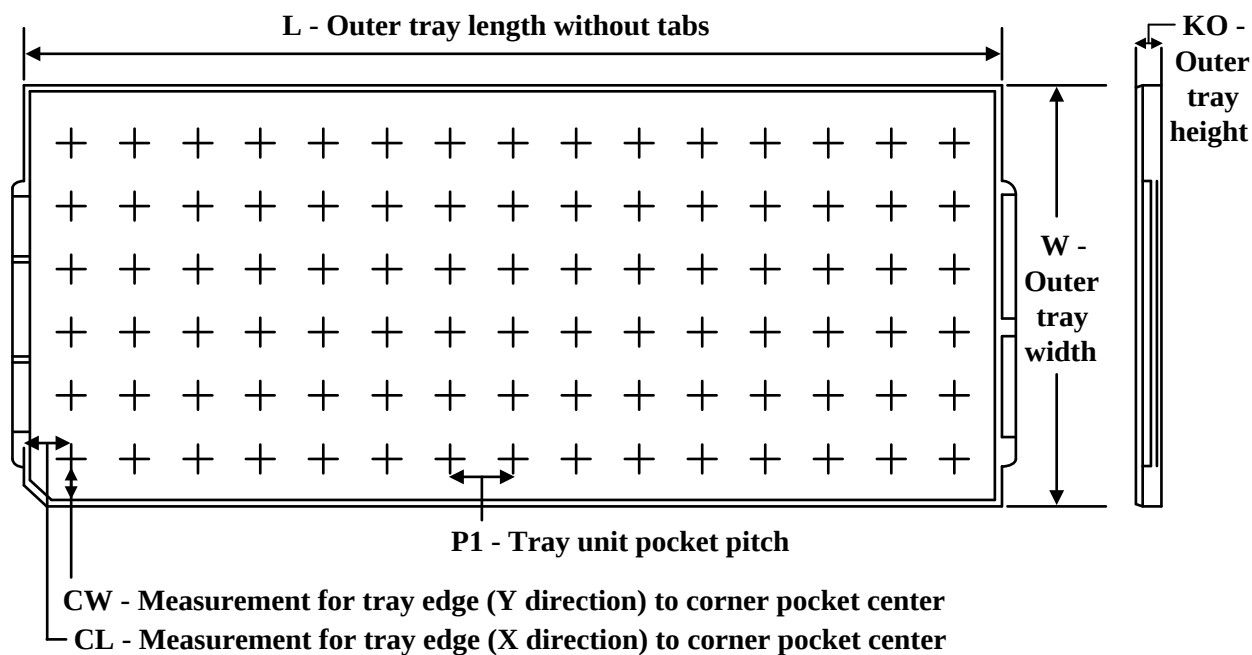
\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| MSP430FR5962IPMR   | LQFP         | PM              | 64   | 1000 | 336.6       | 336.6      | 41.3        |
| MSP430FR5962IPNR   | LQFP         | PN              | 80   | 1000 | 367.0       | 367.0      | 55.0        |
| MSP430FR5962IRGZR  | VQFN         | RGZ             | 48   | 2500 | 367.0       | 367.0      | 38.0        |
| MSP430FR5962IZVWR  | NFBGA        | ZVW             | 87   | 1000 | 336.6       | 336.6      | 31.8        |
| MSP430FR5964IPMR   | LQFP         | PM              | 64   | 1000 | 336.6       | 336.6      | 41.3        |
| MSP430FR5964IPNR   | LQFP         | PN              | 80   | 1000 | 367.0       | 367.0      | 55.0        |
| MSP430FR5964IRGZR  | VQFN         | RGZ             | 48   | 2500 | 367.0       | 367.0      | 38.0        |
| MSP430FR5964IZVWR  | NFBGA        | ZVW             | 87   | 1000 | 336.6       | 336.6      | 31.8        |
| MSP430FR5992IPMR   | LQFP         | PM              | 64   | 1000 | 336.6       | 336.6      | 41.3        |
| MSP430FR5992IPNR   | LQFP         | PN              | 80   | 1000 | 367.0       | 367.0      | 55.0        |
| MSP430FR5992IRGZR  | VQFN         | RGZ             | 48   | 2500 | 367.0       | 367.0      | 38.0        |
| MSP430FR5992IZVWR  | NFBGA        | ZVW             | 87   | 1000 | 336.6       | 336.6      | 31.8        |
| MSP430FR59941IPMR  | LQFP         | PM              | 64   | 1000 | 336.6       | 336.6      | 41.3        |
| MSP430FR59941IPNR  | LQFP         | PN              | 80   | 1000 | 367.0       | 367.0      | 55.0        |
| MSP430FR59941IRGZR | VQFN         | RGZ             | 48   | 2500 | 367.0       | 367.0      | 38.0        |
| MSP430FR59941IRGZT | VQFN         | RGZ             | 48   | 250  | 210.0       | 185.0      | 35.0        |
| MSP430FR59941IZVWR | NFBGA        | ZVW             | 87   | 1000 | 336.6       | 336.6      | 31.8        |
| MSP430FR59941IPMR  | LQFP         | PM              | 64   | 1000 | 336.6       | 336.6      | 41.3        |

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| Device             | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| MSP430FR5994IPMRG4 | LQFP         | PM              | 64   | 1000 | 336.6       | 336.6      | 41.3        |
| MSP430FR5994IPNR   | LQFP         | PN              | 80   | 1000 | 367.0       | 367.0      | 55.0        |
| MSP430FR5994IRGZR  | VQFN         | RGZ             | 48   | 2500 | 367.0       | 367.0      | 38.0        |
| MSP430FR5994IRGZT  | VQFN         | RGZ             | 48   | 250  | 210.0       | 185.0      | 35.0        |
| MSP430FR5994IZVWR  | NFBGA        | ZVW             | 87   | 1000 | 336.6       | 336.6      | 31.8        |

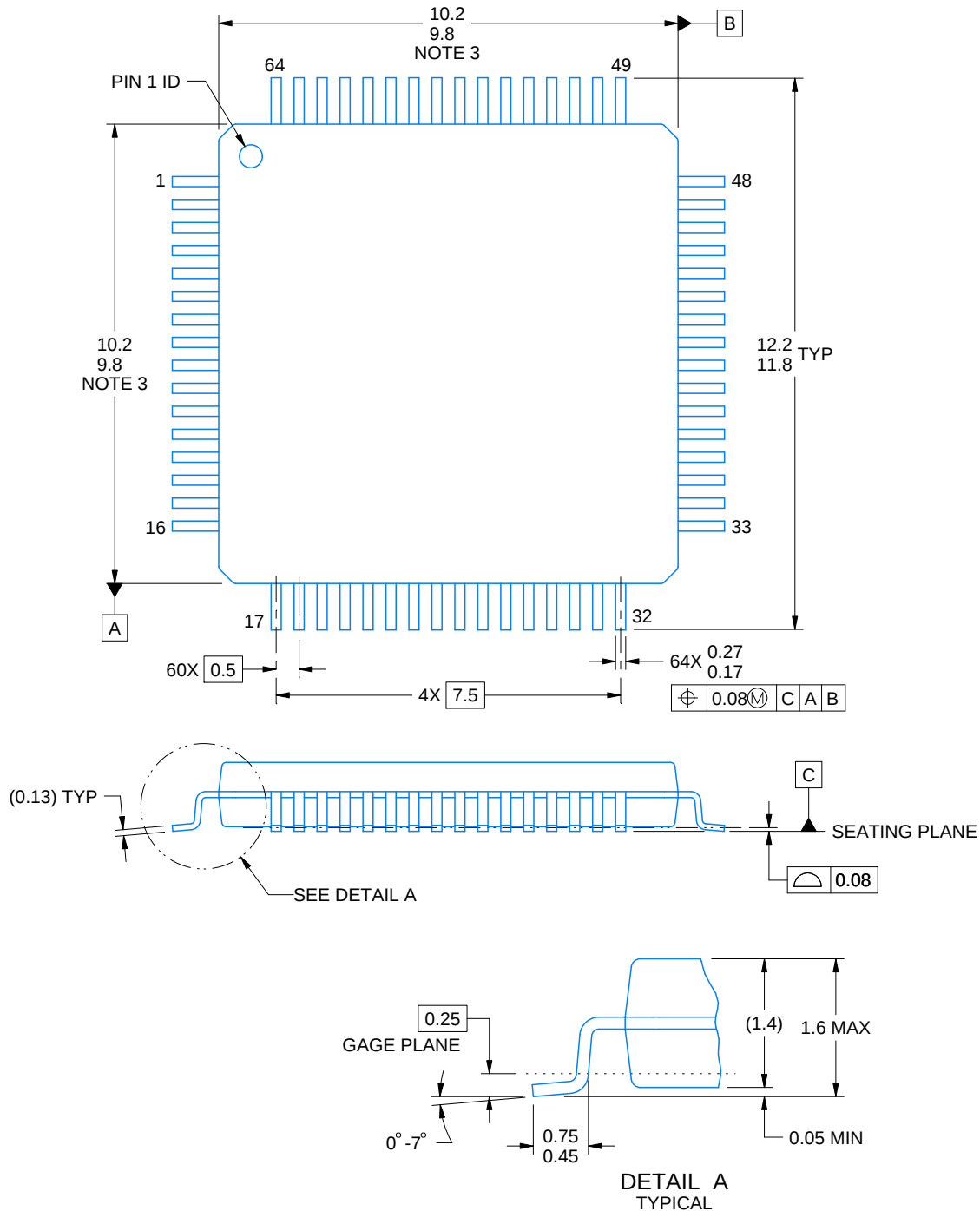
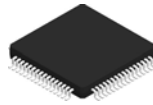
## TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

\*All dimensions are nominal

| Device             | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (μm) | P1 (mm) | CL (mm) | CW (mm) |
|--------------------|--------------|--------------|------|-----|-------------------|----------------------|--------|--------|---------|---------|---------|---------|
| MSP430FR59941IPM   | PM           | LQFP         | 64   | 160 | 8 X 20            | 150                  | 315    | 135.9  | 7620    | 15.2    | 13.1    | 13      |
| MSP430FR59941IPM.A | PM           | LQFP         | 64   | 160 | 8 X 20            | 150                  | 315    | 135.9  | 7620    | 15.2    | 13.1    | 13      |
| MSP430FR59941IPM.B | PM           | LQFP         | 64   | 160 | 8 X 20            | 150                  | 315    | 135.9  | 7620    | 15.2    | 13.1    | 13      |
| MSP430FR59941IPN   | PN           | LQFP         | 80   | 119 | 7 X 17            | 150                  | 315    | 135.9  | 7620    | 17.9    | 14.3    | 13.95   |
| MSP430FR59941IPN.A | PN           | LQFP         | 80   | 119 | 7 X 17            | 150                  | 315    | 135.9  | 7620    | 17.9    | 14.3    | 13.95   |
| MSP430FR59941IPN.B | PN           | LQFP         | 80   | 119 | 7 X 17            | 150                  | 315    | 135.9  | 7620    | 17.9    | 14.3    | 13.95   |
| MSP430FR5994IPM    | PM           | LQFP         | 64   | 160 | 8 X 20            | 150                  | 315    | 135.9  | 7620    | 15.2    | 13.1    | 13      |
| MSP430FR5994IPM.A  | PM           | LQFP         | 64   | 160 | 8 X 20            | 150                  | 315    | 135.9  | 7620    | 15.2    | 13.1    | 13      |
| MSP430FR5994IPM.B  | PM           | LQFP         | 64   | 160 | 8 X 20            | 150                  | 315    | 135.9  | 7620    | 15.2    | 13.1    | 13      |
| MSP430FR5994IPN    | PN           | LQFP         | 80   | 119 | 7 X 17            | 150                  | 315    | 135.9  | 7620    | 17.9    | 14.3    | 13.95   |
| MSP430FR5994IPN.A  | PN           | LQFP         | 80   | 119 | 7 X 17            | 150                  | 315    | 135.9  | 7620    | 17.9    | 14.3    | 13.95   |
| MSP430FR5994IPN.B  | PN           | LQFP         | 80   | 119 | 7 X 17            | 150                  | 315    | 135.9  | 7620    | 17.9    | 14.3    | 13.95   |



4215162/A 03/2017

## NOTES:

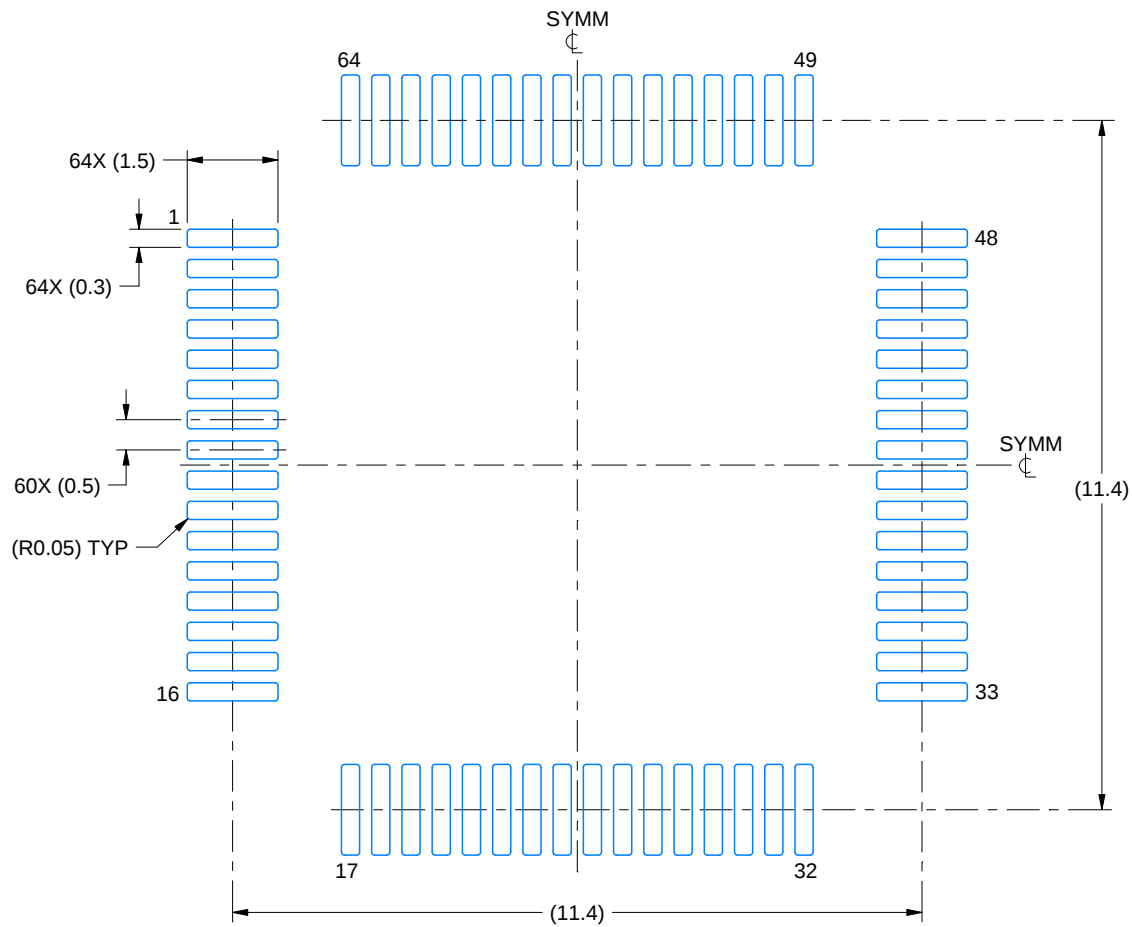
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.

# EXAMPLE BOARD LAYOUT

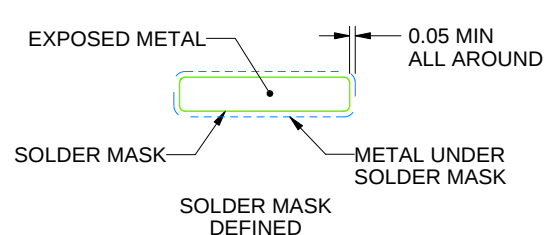
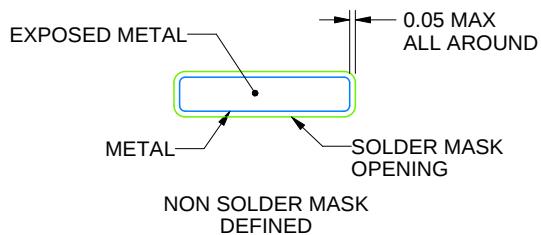
PM0064A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4215162/A 03/2017

NOTES: (continued)

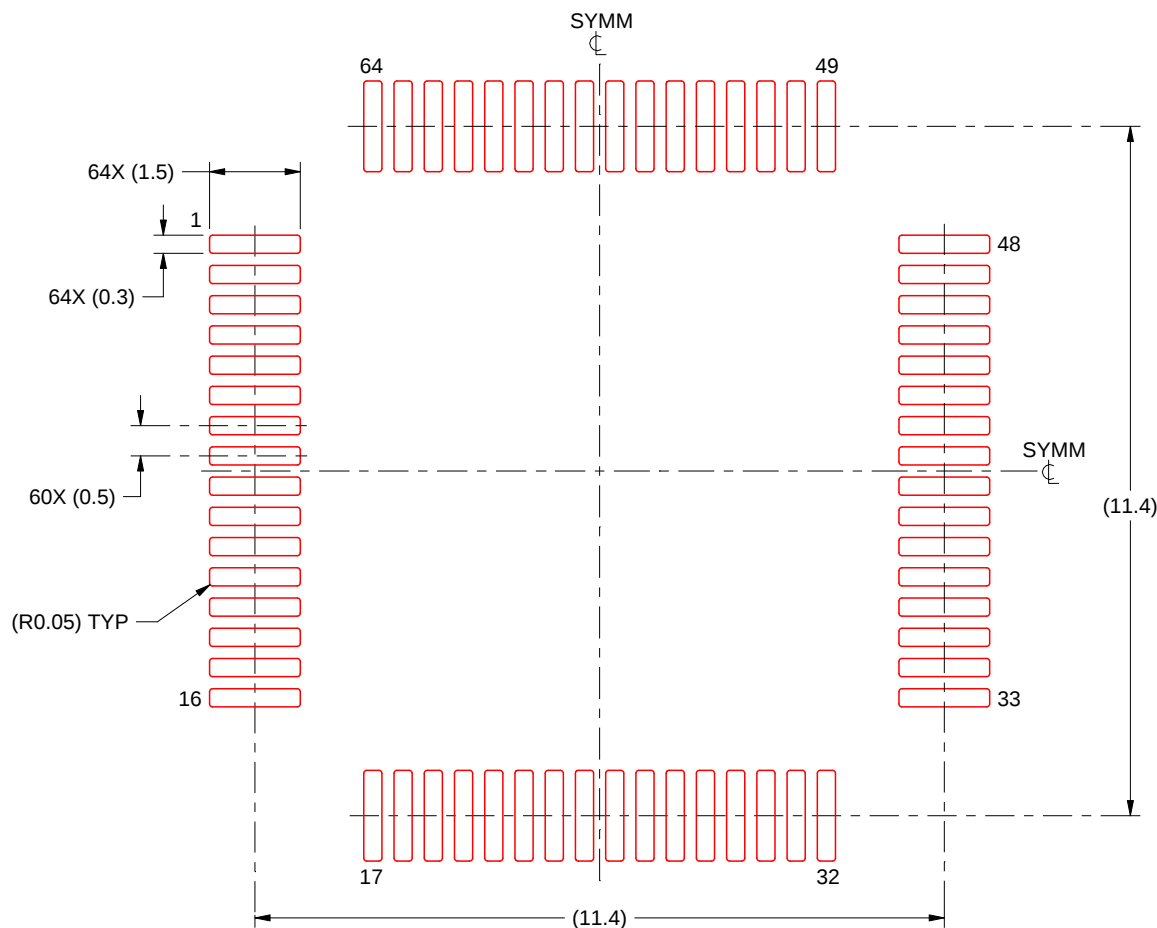
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).

# EXAMPLE STENCIL DESIGN

PM0064A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE  
 BASED ON 0.125 mm THICK STENCIL  
 SCALE:8X

4215162/A 03/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

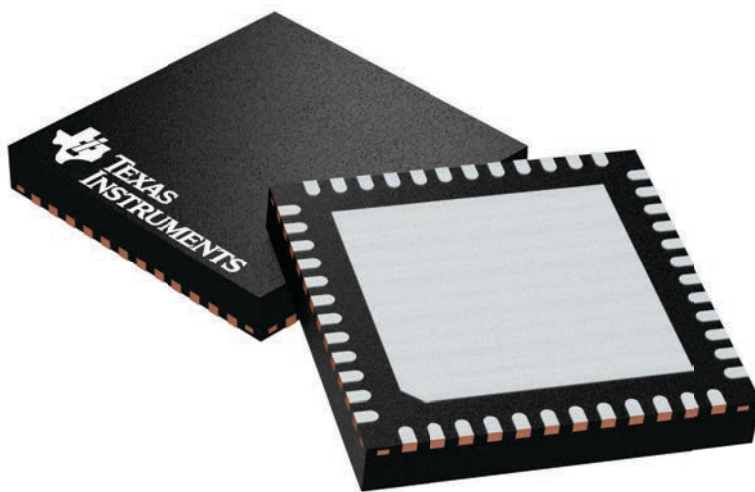
## GENERIC PACKAGE VIEW

**RGZ 48**

**VQFN - 1 mm max height**

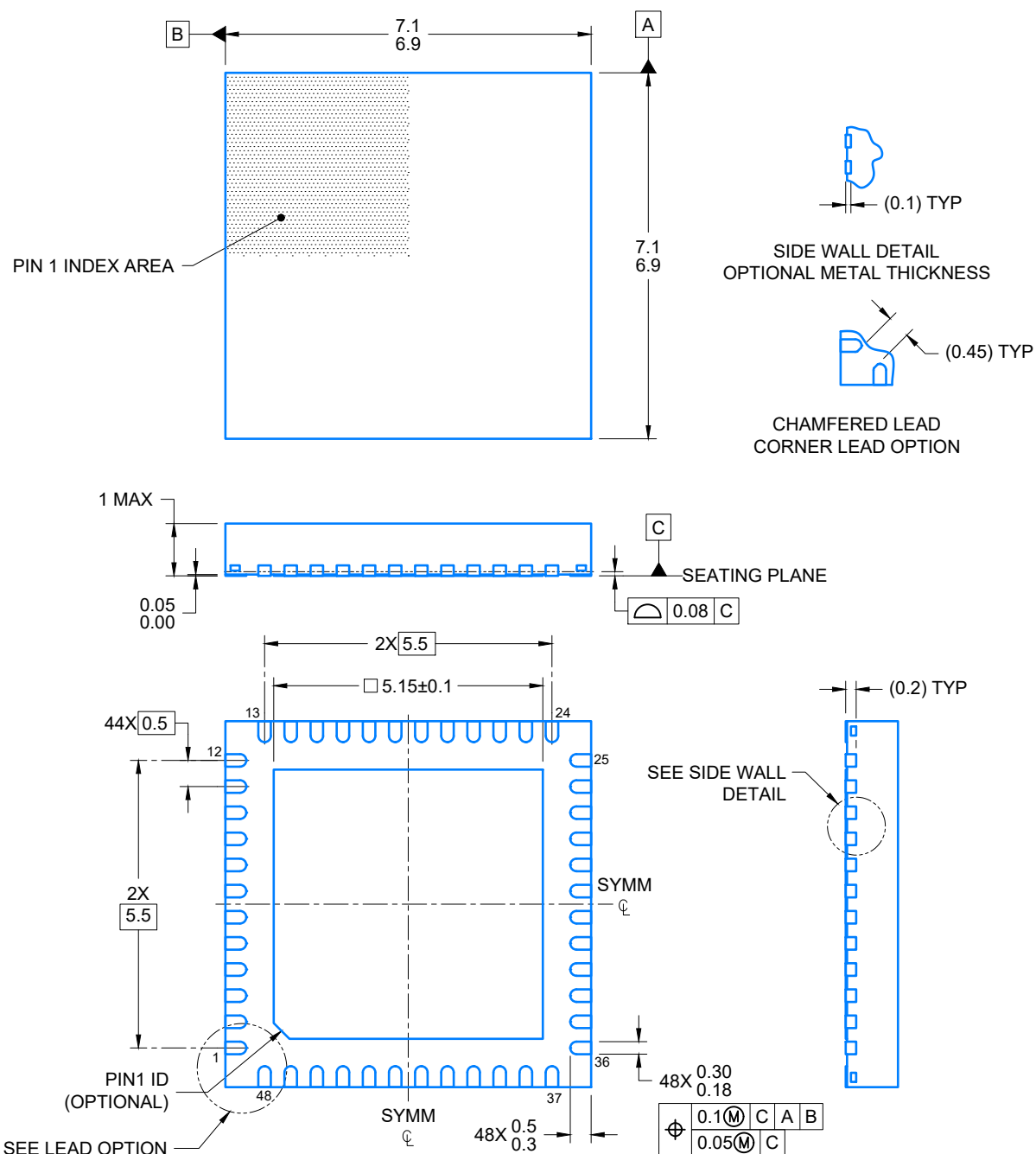
7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

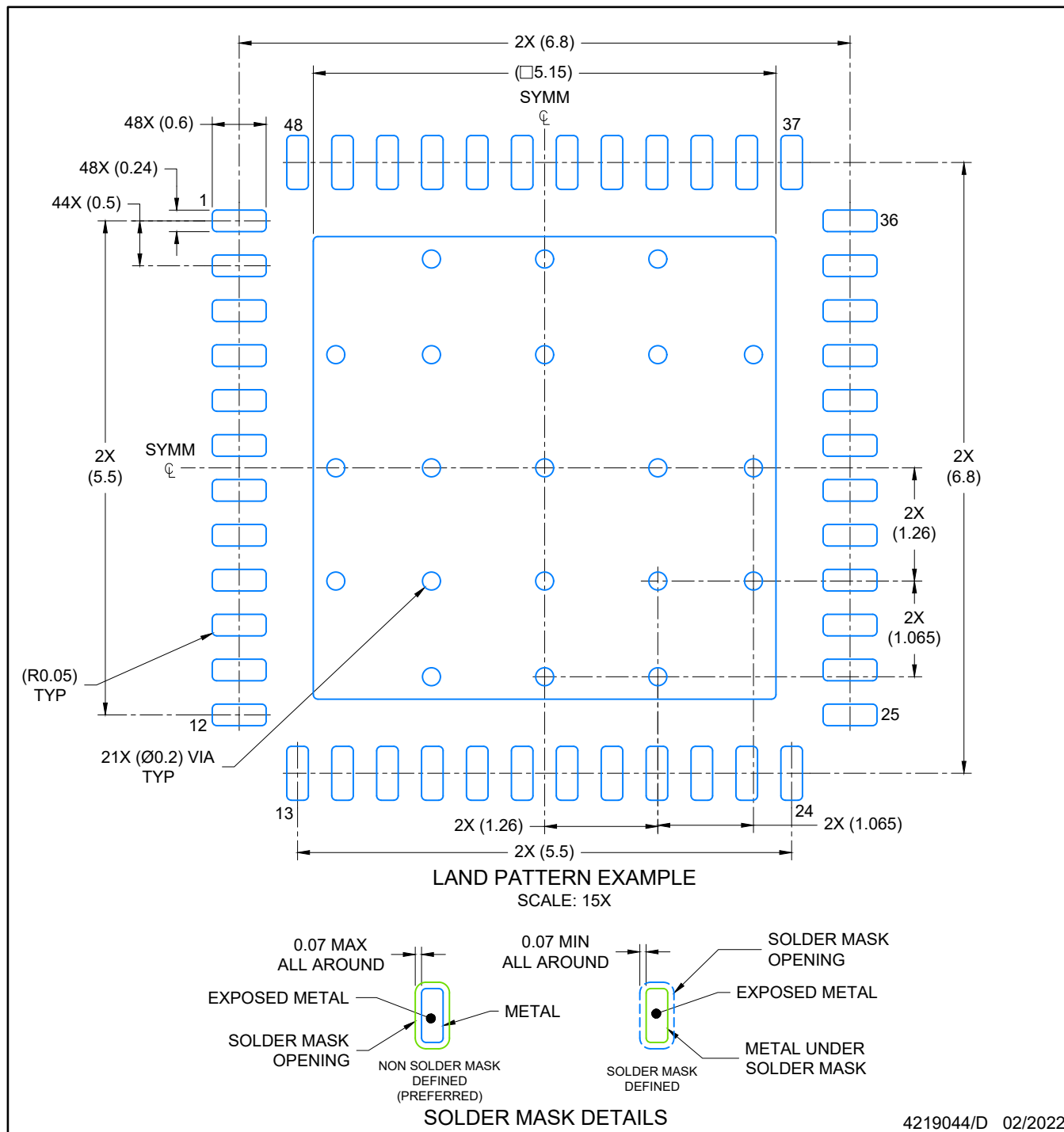
4224671/A



4219044/D 02/2022

## NOTES:

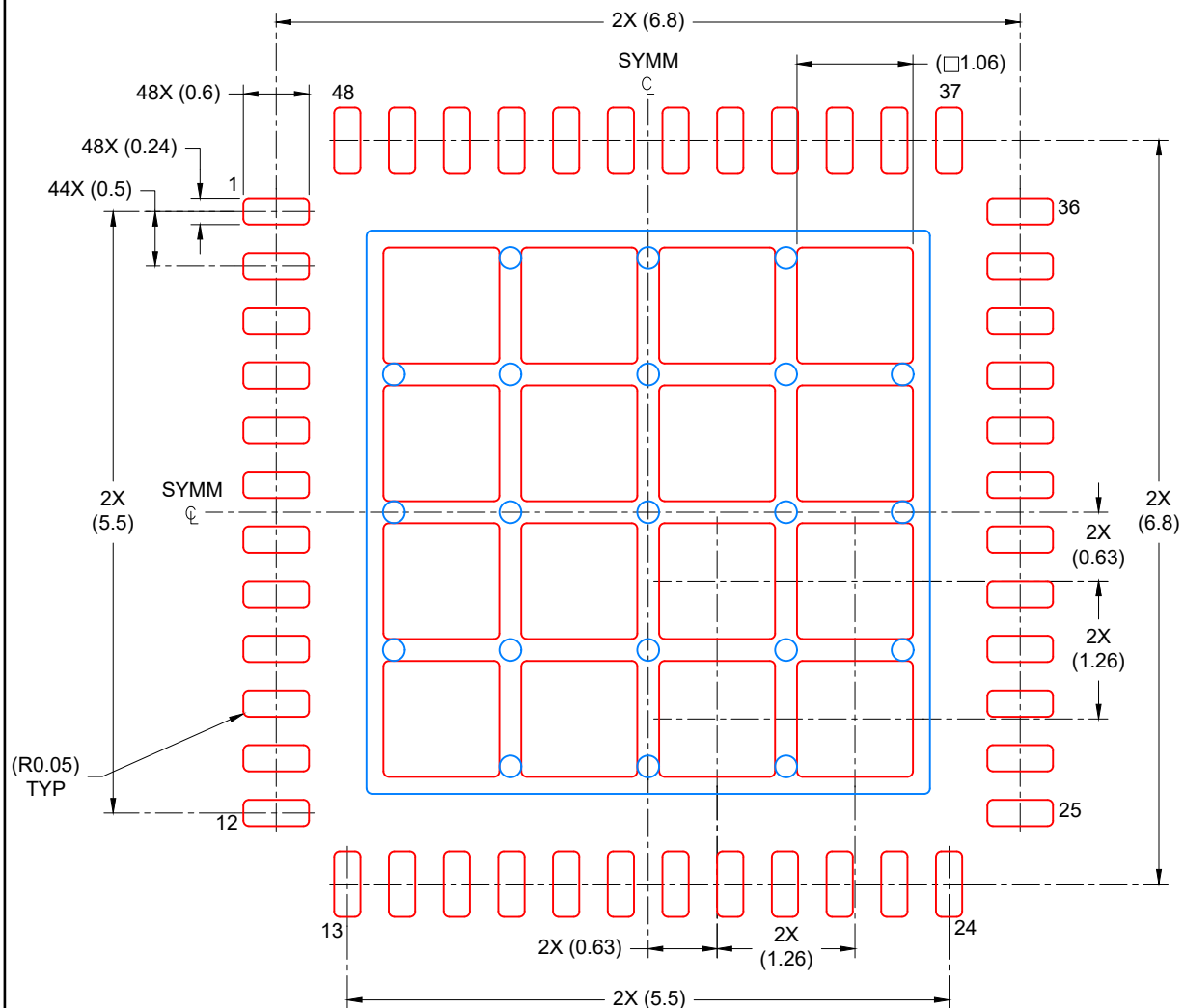
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



4219044/D 02/2022

NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
67% PRINTED COVERAGE BY AREA  
SCALE: 15X

4219044/D 02/2022

NOTES: (continued)

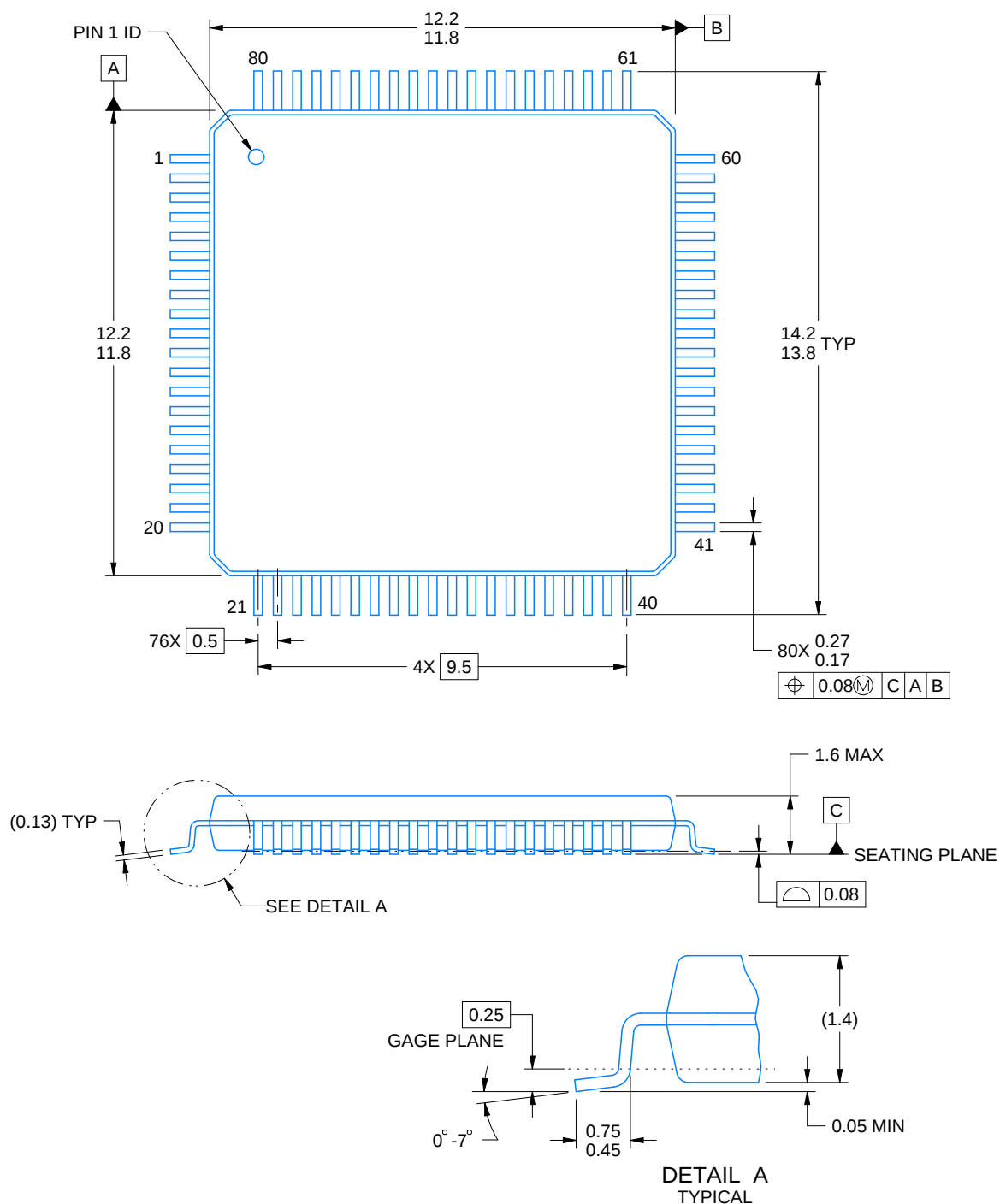
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



## PACKAGE OUTLINE

### LQFP - 1.6 mm max height

## PLASTIC QUAD FLATPACK



4215166/A 08/2022

NOTES:

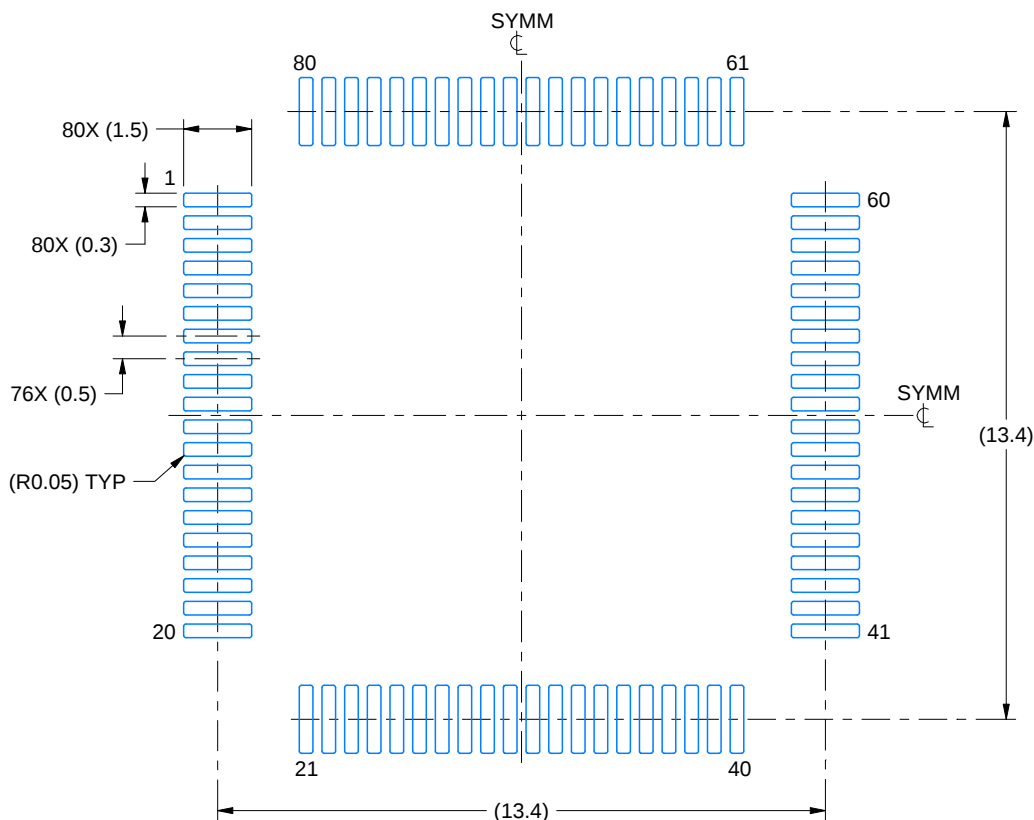
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.

# EXAMPLE BOARD LAYOUT

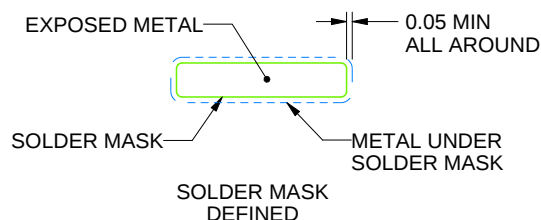
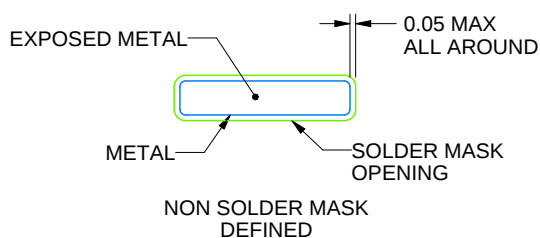
PN0080A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:6X



SOLDER MASK DETAILS

4215166/A 08/2022

NOTES: (continued)

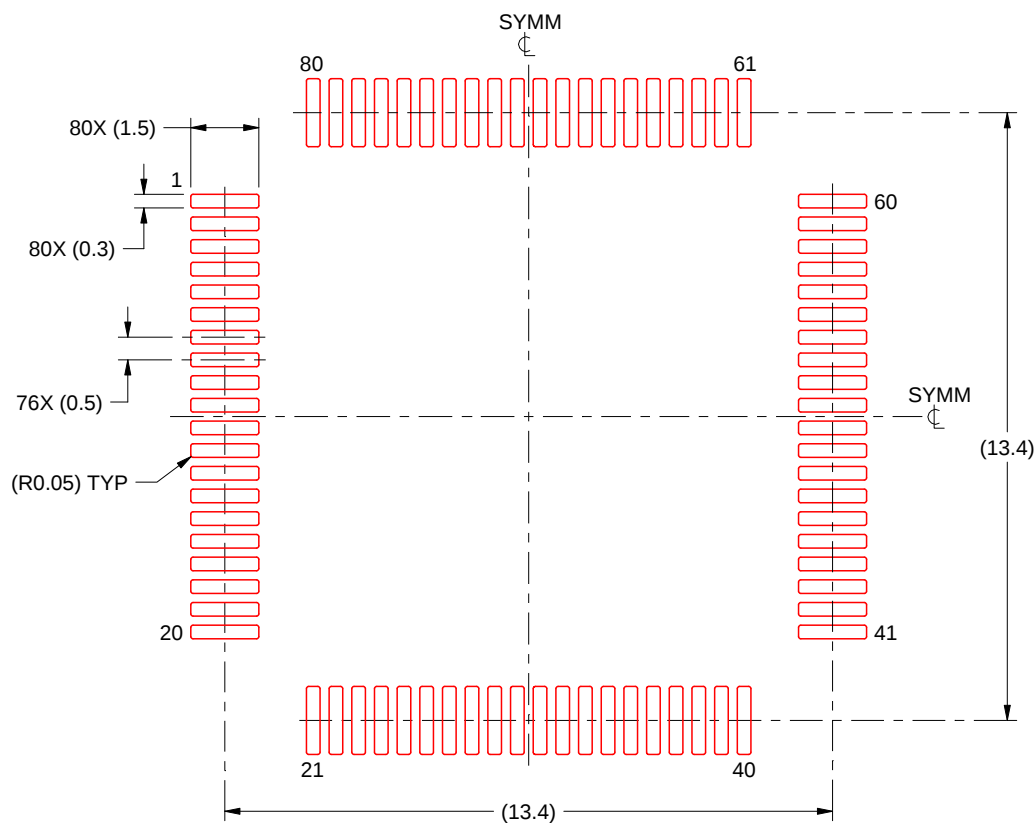
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. For more information, see Texas Instruments literature number SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).

# EXAMPLE STENCIL DESIGN

PN0080A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:6X

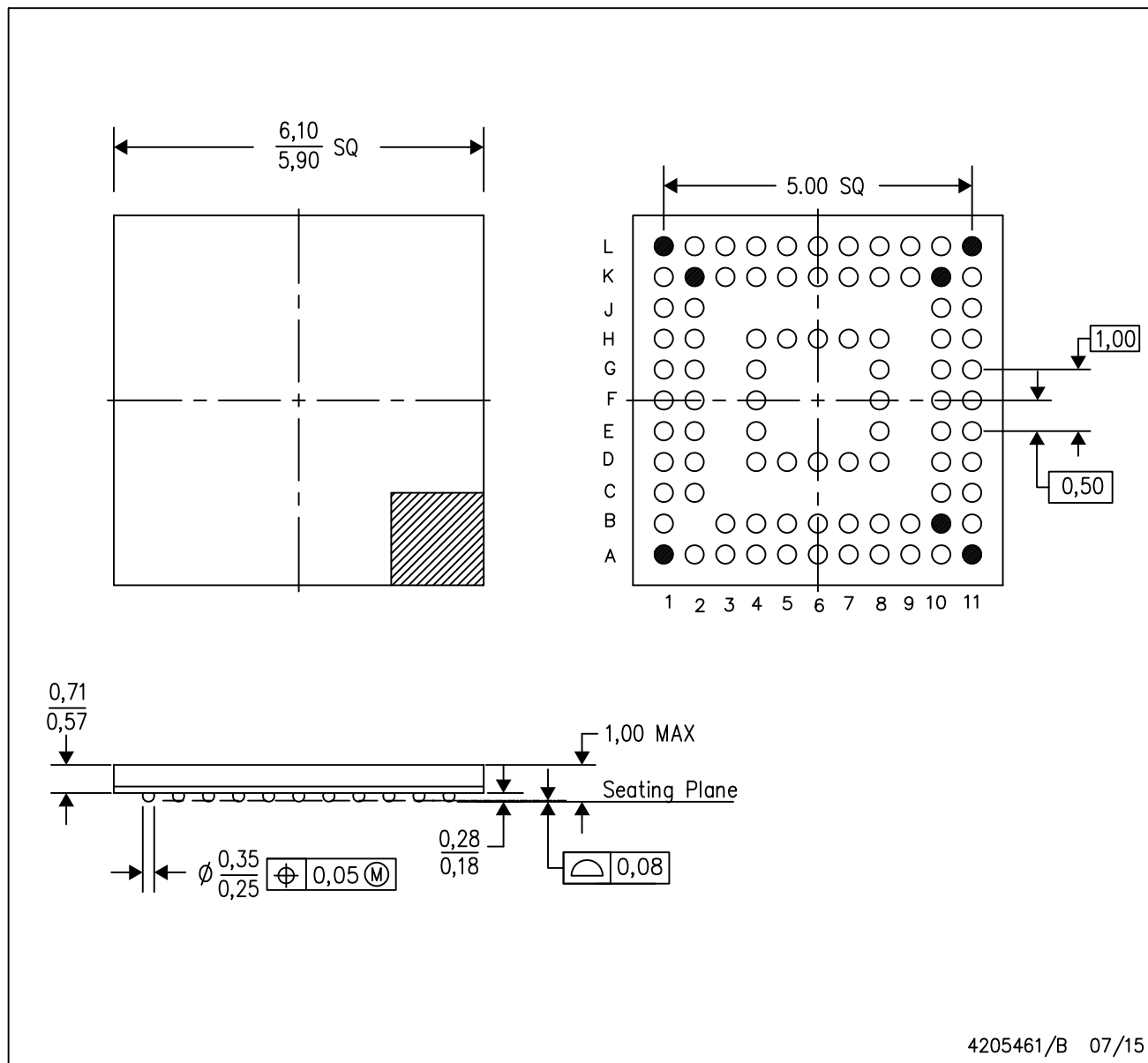
4215166/A 08/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

ZVW (S-PBGA-N87)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. nFBGA configuration.
  - D. A1, A11, L1, L11, B10, K2, K10 to be dummy balls.
  - E. This package is Pb-free.

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