MCP629x 10-MHz, Rail-to-Rail Operational Amplifier

1 Features

- Gain bandwidth product: 10-MHz typical
- Operating supply voltage: 2.4 V to 5.5 V
- Rail-to-rail input/output
- Low input bias current: 1 pA
- Low quiescent current: 0.6 mA
- Input voltage noise: 8.7 nV/√Hz at f = 10 kHz
- Internal RF and EMI filter
- Extended temperature range: –40°C to 125°C
- Unity-gain stable
- Easier to stabilize with higher capacitive load due to resistive open-loop output impedance

2 Applications

- Power modules
- Smoke detectors
- HVAC: heating, ventilating, and air conditioning
- Battery-powered applications
- Sensor signal conditioning
- Photodiode amplifier
- Analog filters
- Medical instrumentation
- Notebooks and PDAs
- Barcode scanners
- Audio receiver
- Automotive infotainment

3 Description

The MCP6291 (single), MCP6292 (dual), and MCP6294 (quad) devices comprise a family of general-purpose, low-power operational amplifiers. Features such as rail-to-rail input and output swings, low quiescent current (600-µA/ch typical) combined with a wide bandwidth of 10 MHz, and low noise (8.7 nV/√Hz at 10 kHz) make this family attractive for a variety of applications that require a balance between cost and performance. The low input bias current enables the family to be used in applications with high-source impedances.

The robust design of the MCP629x provides ease-of-use to the circuit designer: a unity-gain stable, integrated RFI and EMI rejection filter, no phase reversal in overdrive condition, and high electrostatic discharge (ESD) protection (4-kV HBM).

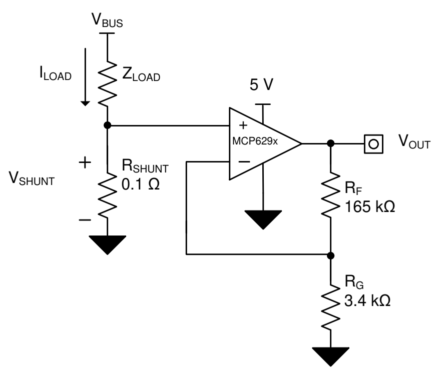
The MCP629x family operates over the extended temperature range of –40°C to 125°C. The family has a power supply range of 2.4 V to 5.5 V.

Device Information(1)

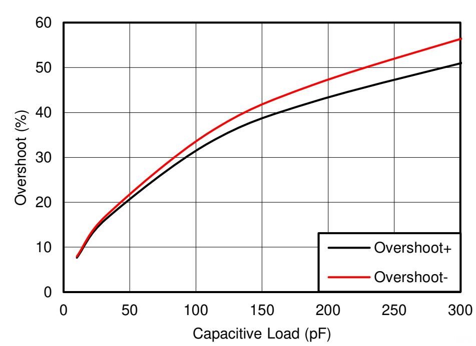
PART NUMBER	PACKAGE	BODY SIZE (NOM)
MCP6291	SOT-23 (5)	1.60 mm × 2.90 mm
	SC70 (5)	1.25 mm × 2.00 mm
MCP6292	SOIC (8)	3.91 mm × 4.90 mm
	VSSOP (8)	3.00 mm × 3.00 mm
	SOT-23 (8)	1.60 mm × 2.90 mm
MCP6294	SOIC (14)	8.65 mm × 3.91 mm
	TSSOP (14)	4.40 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Low-Side Motor Control



Small-Signal Overshoot vs Load Capacitance



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4 Revision History

Changes from Revision C (January 2019) to Revision D	Page
• Added SOT-23 (8) (DDF) package to data sheet	1

Changes from Revision B (April 2018) to Revision C	Page
• Deleted SOT-23 package preview notation in *Device Information* table	1
• Added SC70 package to *Device Information* table	1
• Added DCK package information to *Device Comparison Table*	4
• Deleted DBV package preview notation from *Pin Configuration and Functions* section	5
• Added DCK package drawing and pin functions to *Pin Configuration and Functions* section	5
• Added DBV (SOT-23) and DCK (SC70) thermal information	8

Changes from Revision A (October 2017) to Revision B	Page
• Added DGK package to *Thermal Information* table	9

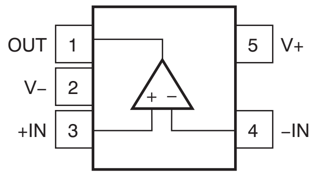
Changes from Original (July 2017) to Revision A	Page
• Deleted MCP6291 SC70, SOT-553, and SOIC packages from *Device Information* table	1
• Deleted MCP6292 WSON and VSSOP (10) packages from *Device Information* table	1
• Changed MCP6294 14-pin SOIC package from preview to production data in *Device Information* table	1
• Deleted DCK, DRL, DSG, RTE and 8-pin D packages from *Device Comparison* table	4
• Deleted DRL (SOT-533) package from MCP6291 pinout image and table in *Pin Configuration and Functions* section	5
• Deleted MCP6291 DCK (SC70) and D (SOIC) package pinout drawings and pin information from *Pin Configuration and Functions* section	5
• Deleted MCP6292 DSG (WSON) and DGS (VSSOP) package pinout drawings and pin table information in *Pin Configuration and Functions* section	6

5 Device Comparison Table

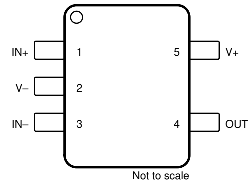
DEVICE	NO. OF CHANNELS	PACKAGE LEADS					
		DBV	DCK	D	DGK	PW	DDF
MCP6291	1	5	5	—	—	—	—
MCP6292	2	—	—	8	8	—	8
MCP6294	4	—	—	14	—	14	—

6 Pin Configuration and Functions

MCP6291 DBV Package
5-Pin SOT-23
Top View



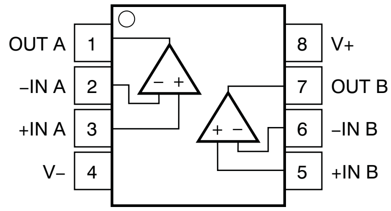
MCP6291 DCK Package
5-Pin SC70
Top View



Pin Functions: MCP6921

PIN			I/O	DESCRIPTION
NAME	NO.			
	SOT-23 (DBV)	SC70 (DCK)		
–IN	4	3	I	Inverting input
+IN	3	1	I	Noninverting input
OUT	1	4	O	Output
V–	2	8	—	Negative (lowest) supply or ground (for single-supply operation)
V+	5	5	—	Positive (highest) supply

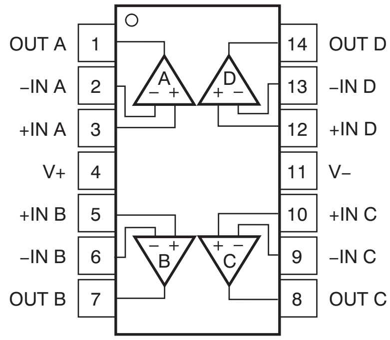
MCP6292 D, DGK, DDF Packages
8-Pin SOIC, VSSOP
Top View



Pin Functions: MCP6292

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V–	4	—	Negative (lowest) supply or ground (for single-supply operation)
V+	8	—	Positive (highest) supply

MCP6294 D, PW Packages
14-Pin SOIC, TSSOP
Top View



Pin Functions: MCP6294

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
–IN C	9	I	Inverting input, channel C
+IN C	10	I	Noninverting input, channel C
–IN D	13	I	Inverting input, channel D
+IN D	12	I	Noninverting input, channel D
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
OUT C	8	O	Output, channel C
OUT D	14	O	Output, channel D
V–	11	—	Negative (lowest) supply or ground (for single-supply operation)
V+	4	—	Positive (highest) supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)(1)

			MIN	MAX	UNIT
Supply voltage				6	V
Signal input pins	Voltage(2)	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential		(V+) – (V–) + 0.2	
	Current(2)		–10	10	mA
Output short-circuit(3)			Continuous		mA
Specified, T_A			–40	125	°C
Junction, T_J				150	°C
Storage, T_{stg}			–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Current limit input signals that can swing more than 0.5 V beyond the supply rails to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

over operating free-air temperature range (unless otherwise noted)

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage	2.4	5.5	V
	Specified temperature	–40	125	°C

7.4 Thermal Information: MCP6291

THERMAL METRIC(1)		MCP6291		UNIT
		DBV (SOT-23)	DCK (SC70)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	221.7	263.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	144.7	75.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.7	51.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	26.1	1.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	49.0	50.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Thermal Information: MCP6292

THERMAL METRIC[(1)]		MCP6292			UNIT
		D (SOIC)	DGK (VSSOP)	DDF (SOT-23)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	157.6	201.2	184.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	104.6	85.7	112.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	99.7	122.9	99.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	55.6	21.2	18.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	99.2	121.4	99.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.6 Thermal Information: MCP6294

THERMAL METRIC[(1)]		MCP6294		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	106.9	135.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	64	64	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63	79	°C/W
ψ_{JT}	Junction-to-top characterization parameter	25.9	15.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.7	78.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.7 Electrical Characteristics: V_S (Total Supply Voltage) = (V+) – (V–) = 2.4 V to 5.5 V

at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 5 V		±0.3	±3	mV
		V_S = 5 V, T_A = –40°C to 125°C			±5	
dV_{OS}/dT	Drift	V_S = 5 V, T_A = –40°C to 125°C		±1.1		µV/°C
PSRR	Power-supply rejection ratio	V_S = 2.4 V – 5.5 V, V_{CM} = (V–)		±7		µV/V
	Channel separation, DC	At DC		100		dB
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	V_S = 2.4 V to 5.5 V	(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	V_S = 5.5 V (V–) – 0.1 V < V_{CM} < (V+) – 1.4 V T_A = –40°C to 125°C	80	103		dB
		V_S = 5.5 V V_{CM} = –0.1 V to 5.6 V T_A = –40°C to 125°C	57	87		
		V_S = 2.4 V (V–) – 0.1 V < V_{CM} < (V+) – 1.4 V T_A = –40°C to 125°C		88		
		V_S = 2.4 V V_{CM} = –0.1 V to 1.9 V T_A = –40°C to 125°C		81		
INPUT BIAS CURRENT						
I_B	Input bias current			±1		pA
I_{OS}	Input offset current			±0.05		pA
NOISE						
E_n	Input voltage noise (peak-to-peak)	V_S = 5 V, f = 0.1 Hz to 10 Hz		4.77		$µV_{PP}$
e_n	Input voltage noise density	V_S = 5 V, f = 10 kHz, R_L = 10 kΩ		8.7		nV/√Hz
		V_S = 5 V, f = 1 kHz, R_L = 10 kΩ		16		
i_n	Input current noise density	f = 1 kHz		10		fA/√Hz
INPUT CAPACITANCE						
C_{ID}	Differential			2		pF
C_{IC}	Common-mode			4		pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	V_S = 2.4 V (V–) + 0.04 V < V_O < (V+) – 0.04 V R_L = 10 kΩ		100		dB
		V_S = 5.5 V (V–) + 0.05 V < V_O < (V+) – 0.05 V R_L = 10 kΩ	104	130		
		V_S = 2.4 V (V–) + 0.06 V < V_O < (V+) – 0.06 V R_L = 2 kΩ		100		
		V_S = 5.5 V (V–) + 0.15 V < V_O < (V+) – 0.15 V R_L = 2 kΩ		130		
FREQUENCY RESPONSE						
GBP	Gain bandwidth product	V_S = 5 V, G = 1		10		MHz
$φ_m$	Phase margin	V_S = 5 V, G = 1		55		°
SR	Slew rate	V_S = 5 V, G = 1		6.5		V/µs
t_S	Settling time	To 0.1%, V_S = 5 V, 2-V step , G = 1 C_L = 100 pF		0.5		µs
		To 0.01%, V_S = 5 V, 2-V step , G = 1 C_L = 100 pF		1		
t_{OR}	Overload recovery time	V_S = 5 V V_{IN} × gain > V_S		0.2		µs

Electrical Characteristics: V_S (Total Supply Voltage) = (V+) – (V–) = 2.4 V to 5.5 V (continued)

at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THD + N	Total harmonic distortion + noise(1)	V_S = 5 V V_O = 1 V_{RMS} G = 1, f = 1 kHz		0.0008%		
OUTPUT						
V_O	Voltage output swing from supply rails	V_S = 5.5 V, R_L = 10 kΩ			15	mV
		V_S = 5.5 V, R_L = 2 kΩ			50	
I_{SC}	Short-circuit current	V_S = 5 V		±50		mA
Z_O	Open-loop output impedance	V_S = 5 V, f = 10 MHz		100		Ω
POWER SUPPLY						
I_Q	Quiescent current per amplifier	V_S = 5.5 V, I_O = 0 mA		600	1300	µA

(1) Third-order filter; bandwidth = 80 kHz at –3 dB.

7.8 Typical Characteristics

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

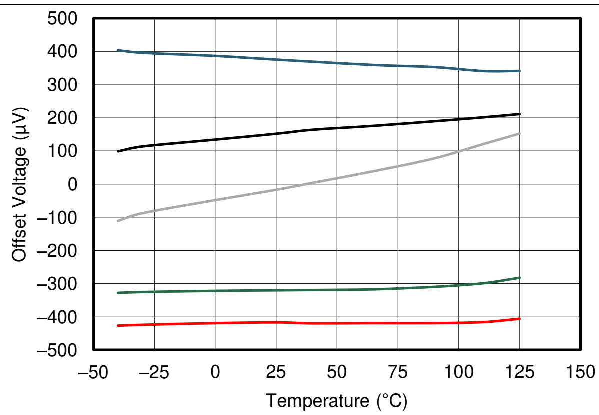
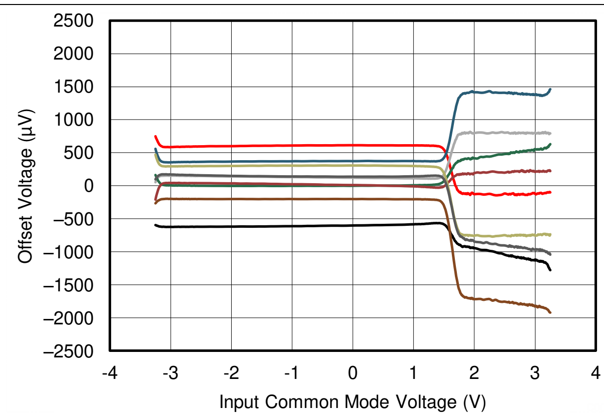
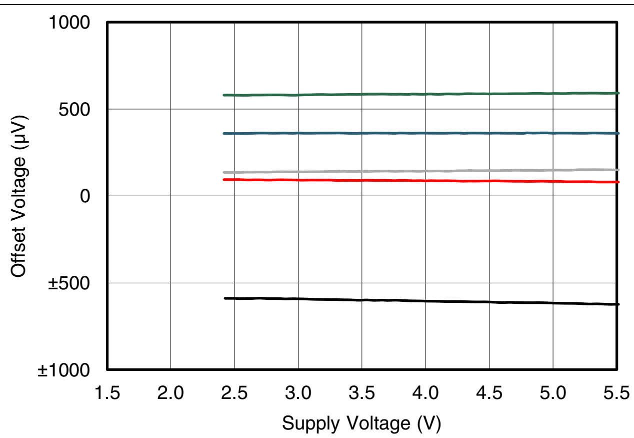


Figure 1. Offset Voltage vs Temperature



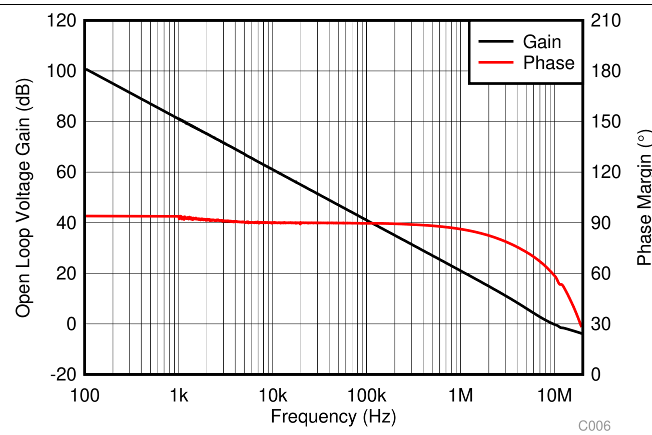
V+ = 2.75 V, V– = –2.75 V

Figure 2. Offset Voltage vs Common-Mode Voltage



V_S = 2.4 V to 5.5 V

Figure 3. Offset Voltage vs Power Supply



C_L = 10 pF

Figure 4. Open-Loop Gain and Phase vs Frequency

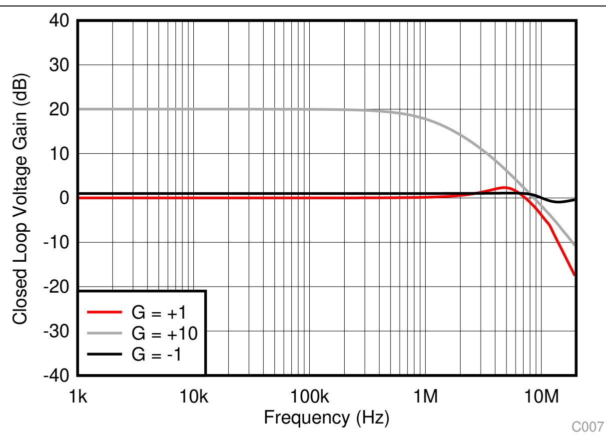


Figure 5. Closed-Loop Gain vs Frequency

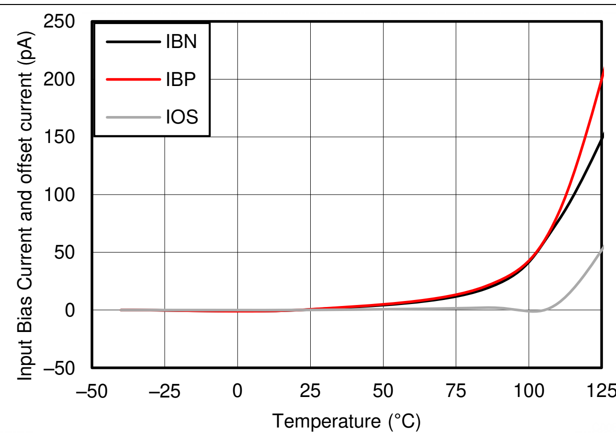
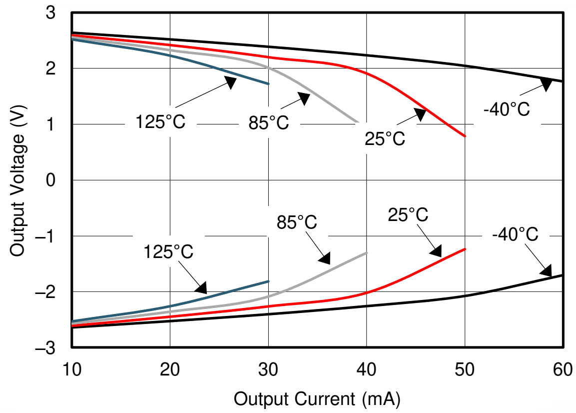


Figure 6. Input Bias Current vs Temperature

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



V+ = 2.75 V, V– = –2.75 V

Figure 7. Output Voltage Swing vs Output Current

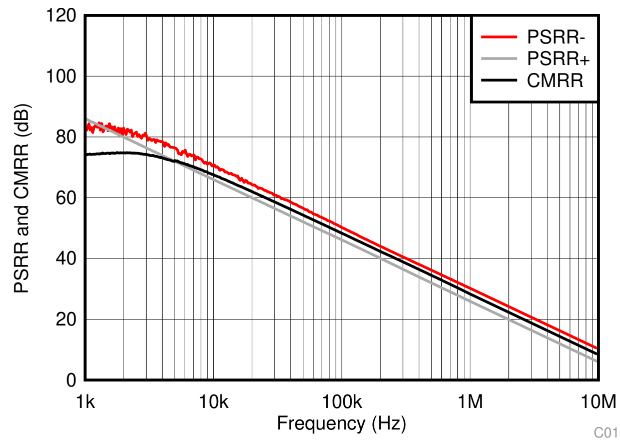
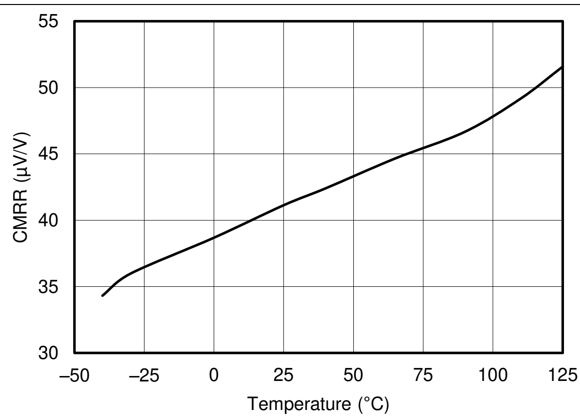
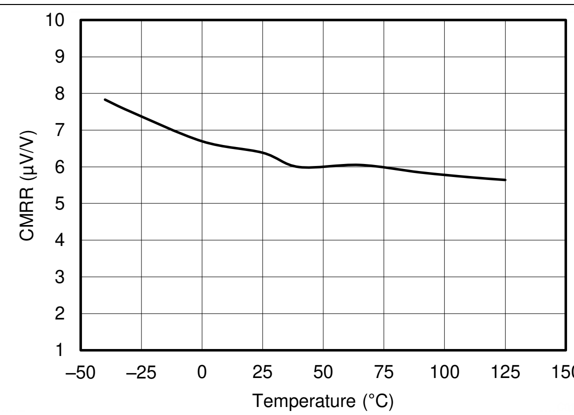


Figure 8. CMRR and PSRR vs Frequency (Referred to Input)



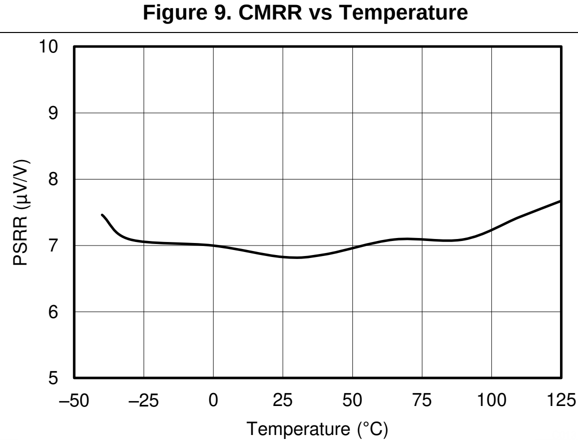
V_S = 5.5 V
V_{CM} = (V–) – 0.1 V to (V+) + 0.1 V
T_A= –40°C to 125°C
R_L= 10 kΩ

Figure 9. CMRR vs Temperature



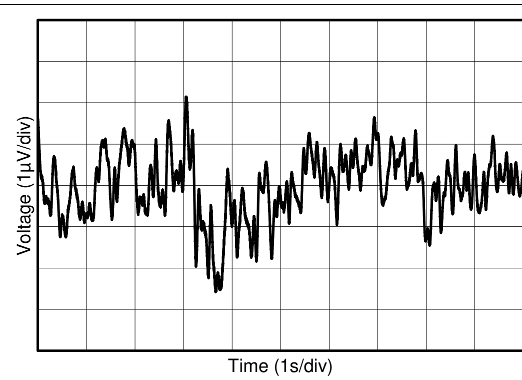
V_S = 5.5 V
V_{CM} = (V–) – 0.1 V to (V+) – 1.4 V
R_L= 10 kΩ
T_A= –40°C to 125°C

Figure 10. CMRR vs Temperature



V_S = 2.4 V to 5.5 V

Figure 11. PSRR vs Temperature



V_S = 2.4 V to 5.5 V

Figure 12. 0.1-Hz to 10-Hz Input Voltage Noise

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

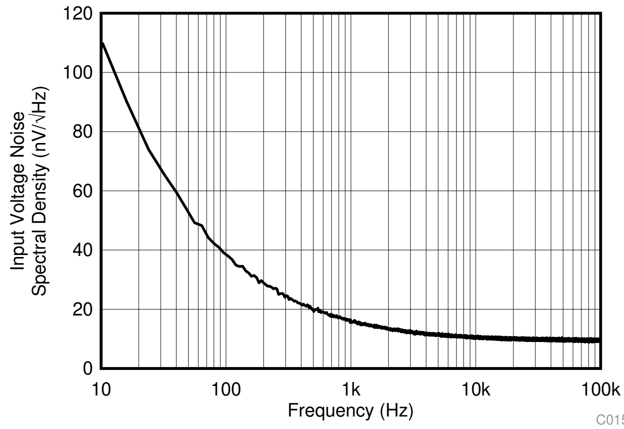


Figure 13. Input Voltage Noise Spectral Density vs Frequency

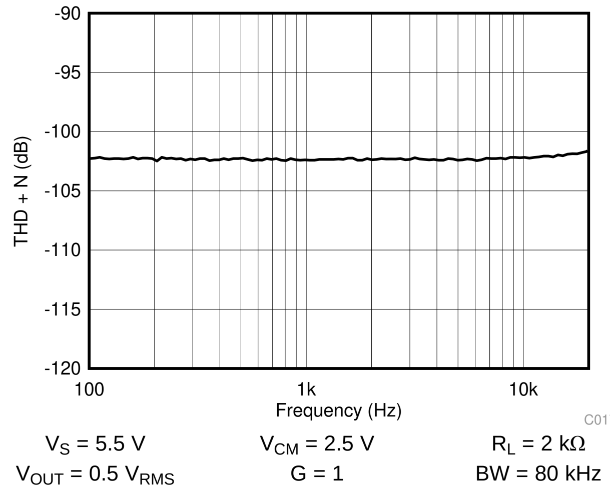


Figure 14. THD + N vs Frequency

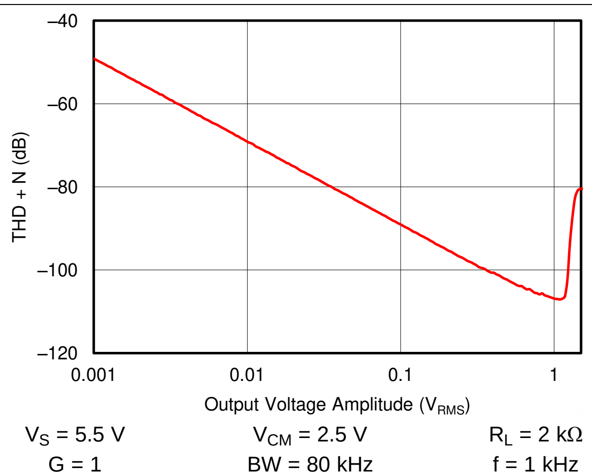


Figure 15. THD + N vs Amplitude

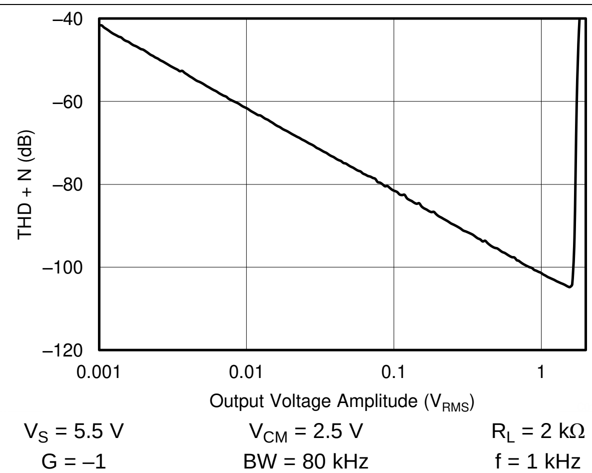


Figure 16. THD + N vs Amplitude

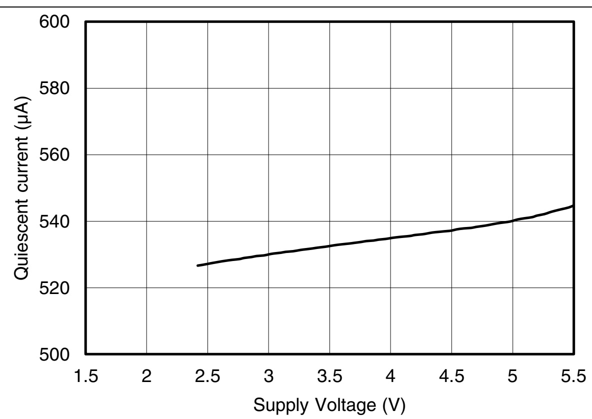


Figure 17. Quiescent Current vs Supply Voltage

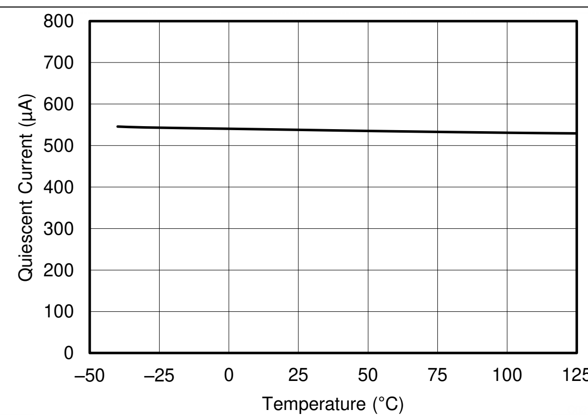


Figure 18. Quiescent Current vs Temperature

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

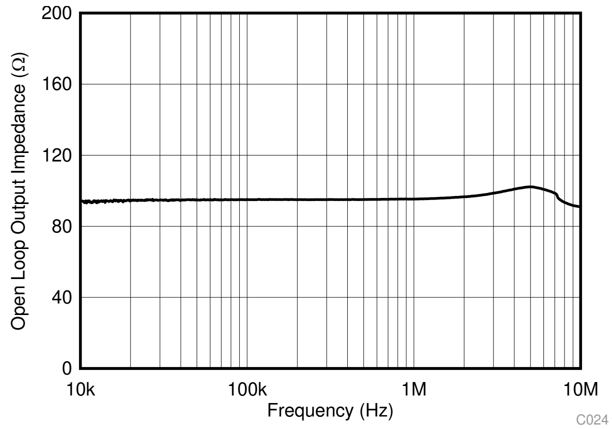


Figure 19. Open-Loop Output Impedance vs Frequency

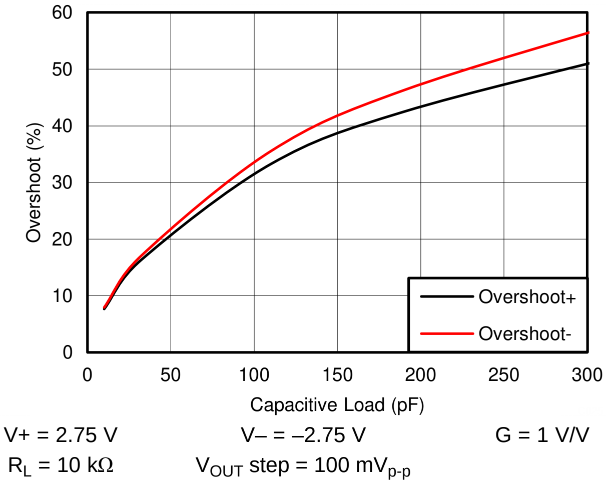


Figure 20. Small-Signal Overshoot vs Load Capacitance

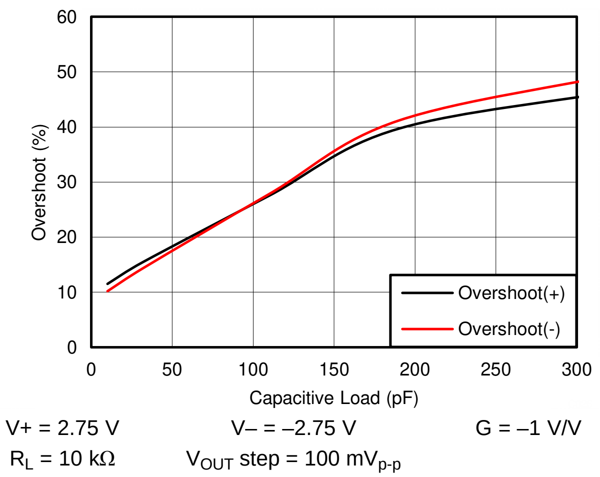


Figure 21. Small-Signal Overshoot vs Load Capacitance

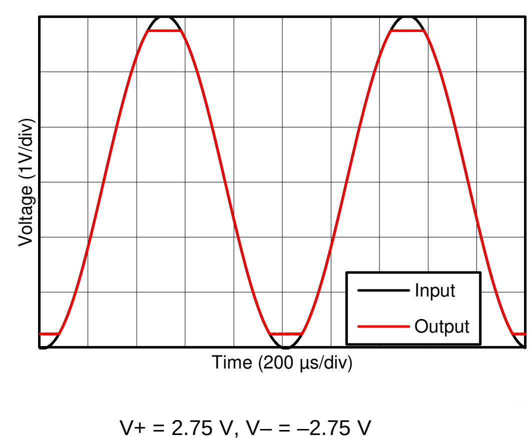


Figure 22. No Phase Reversal

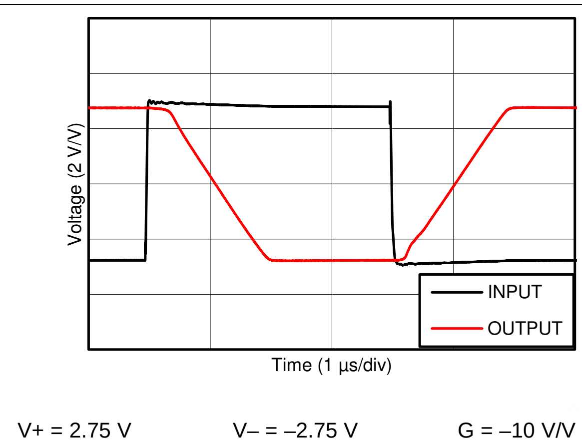


Figure 23. Overload Recovery

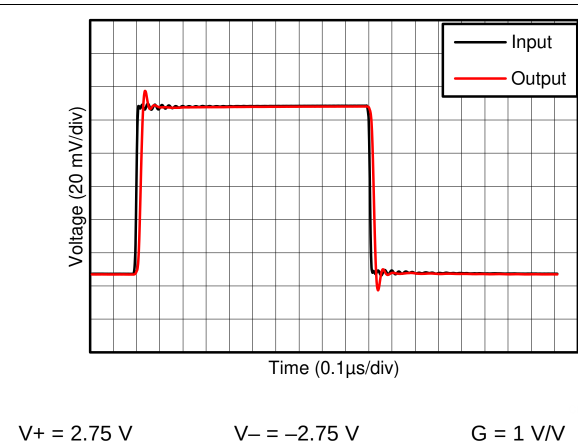
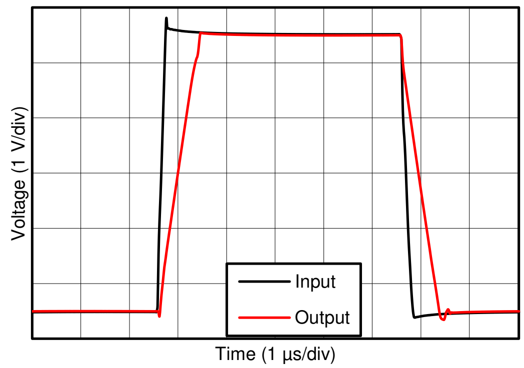


Figure 24. Small-Signal Step Response

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



V+ = 2.75 V V– = –2.75 V C_L = 100 pF
G = 1 V/V

Figure 25. Large-Signal Step Response

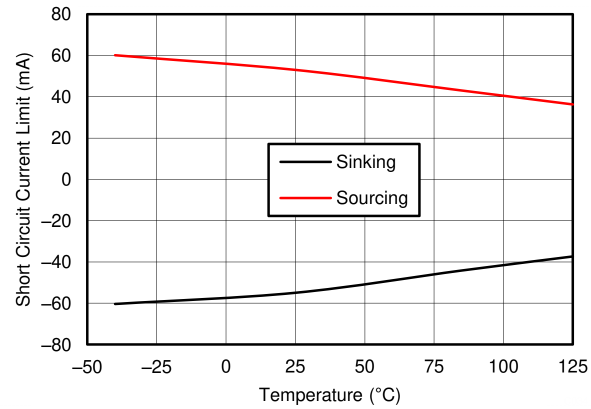
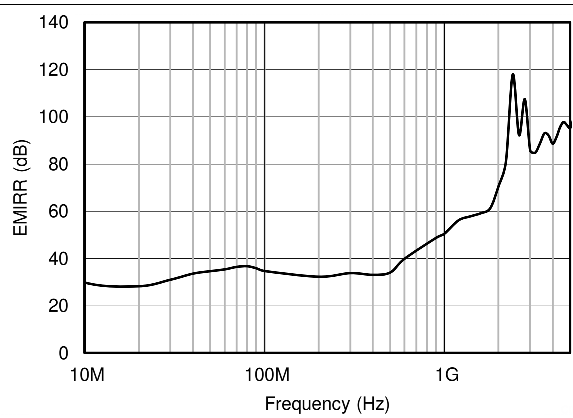
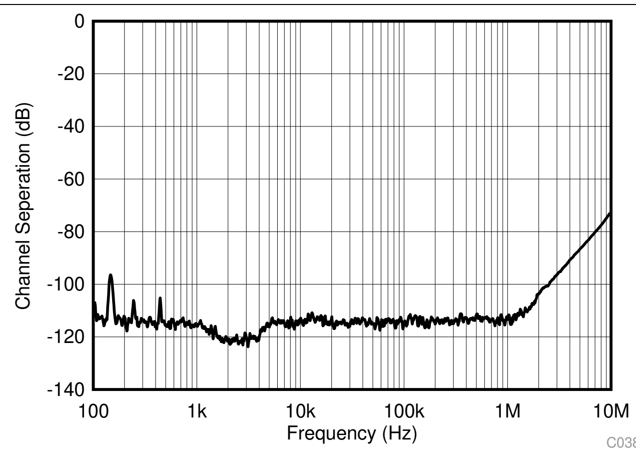


Figure 26. Short-Circuit Current vs Temperature



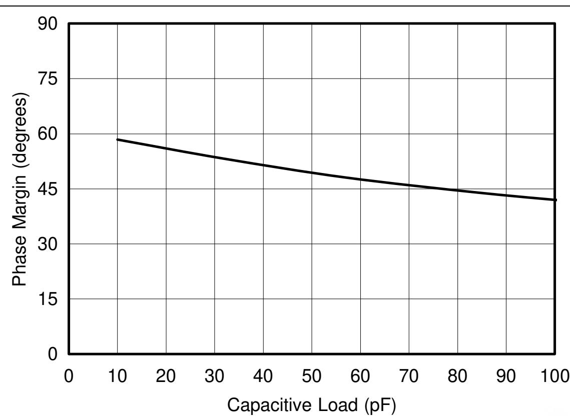
P_{RF} = –10 dBm

Figure 27. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency



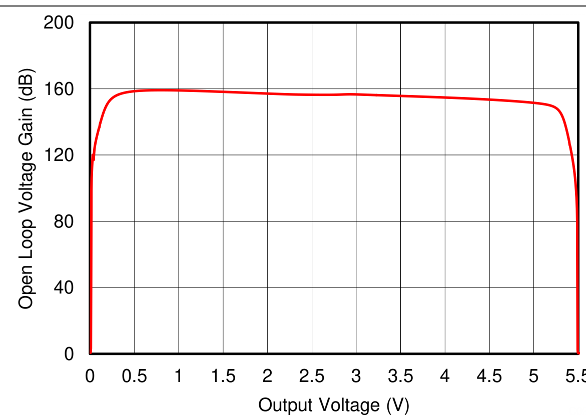
V+ = 2.75 V, V– = –2.75 V

Figure 28. Channel Separation vs Frequency



V_S = 5.5 V

Figure 29. Phase Margin vs Capacitive Load



V_S = 5.5 V

Figure 30. Open Loop Voltage Gain vs Output Voltage

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

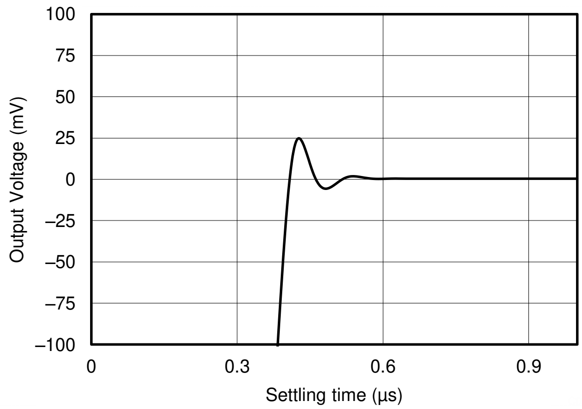


Figure 31. Large Signal Settling Time (Positive)

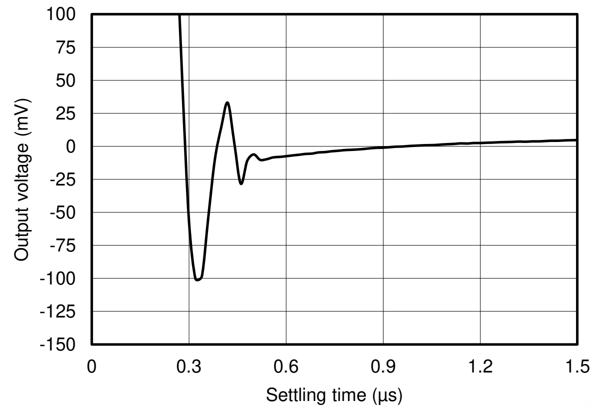


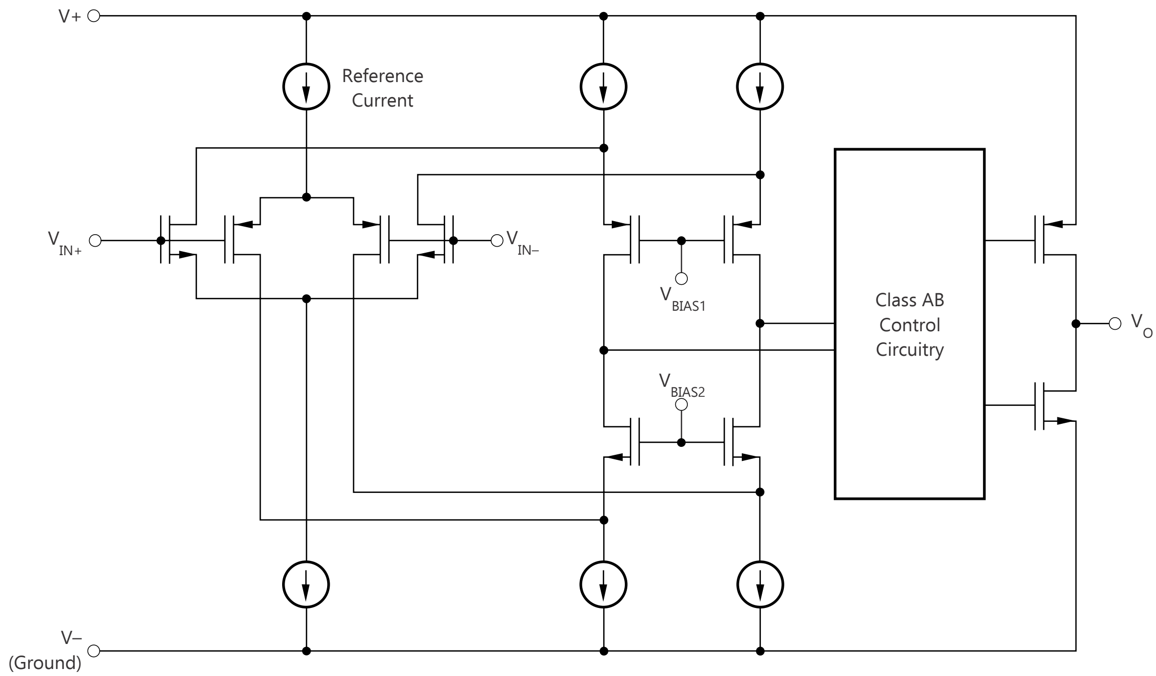
Figure 32. Large Signal Settling Time (Negative)

8 Detailed Description

8.1 Overview

The MCP629x series is a family of low-power, rail-to-rail input and output op amps. These devices operate from 2.4 V to 5.5 V, are unity-gain stable, and are designed for a wide range of general-purpose applications. The input common-mode voltage range includes both rails and allows the MCP629x series to be used in any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range in low-supply applications and are designed for driving sampling analog-to-digital converters (ADCs).

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Rail-to-Rail Input

The input common-mode voltage range of the MCP629x family extends 100 mV beyond the supply rails for the full supply voltage range of 2.4 V to 5.5 V. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as the *Functional Block Diagram* shows. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.4 V to 100 mV above the positive supply, whereas the P-channel pair is active for inputs from 100 mV below the negative supply to approximately (V+) – 1.4 V. There is a small transition region, typically (V+) – 1.2 V to (V+) – 1 V, in which both pairs are on. This 200-mV transition region can vary up to 200 mV with process variation. Thus, the transition region (with both stages on) can range from (V+) – 1.4 V to (V+) – 1.2 V on the low end, and up to (V+) – 1 V to (V+) – 0.8 V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can degrade compared to device operation outside this region.

8.3.2 Rail-to-Rail Output

Designed as a low-power, low-voltage operational amplifier, the MCP629x series delivers a robust output drive capability. A class AB output stage with common-source transistors achieves full rail-to-rail output swing capability. For resistive loads of 10 kΩ, the output swings to within 15 mV of either supply rail, regardless of the applied power-supply voltage. Different load conditions change the ability of the amplifier to swing close to the rails.

8.3.3 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, because of the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return to the linear state. After the charge carriers return to the linear state, the device begins to slew at the specified slew rate. Therefore, the propagation delay (in case of an overload condition) is the sum of the overload recovery time and the slew time. The overload recovery time for the MCP629x series is approximately 200 ns.

8.4 Device Functional Modes

The MCP629x family has a single functional mode. These devices are powered on as long as the power-supply voltage is between 2.4 V (±1.2 V) and 5.5 V (±2.75 V).

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The MCP629x series features 10-MHz bandwidth and 6.5-V/µs slew rate with only 600µA of supply current per channel, providing good AC performance at low power consumption. DC applications are well served with a low input noise voltage of 8.7 nV / $\sqrt{Hz}$ at 10 kHz, low input bias current, and a typical input offset voltage of 0.3 mV.

9.2 Typical Application

Figure 33 shows the MCP629x configured in a low-side, motor-control application.

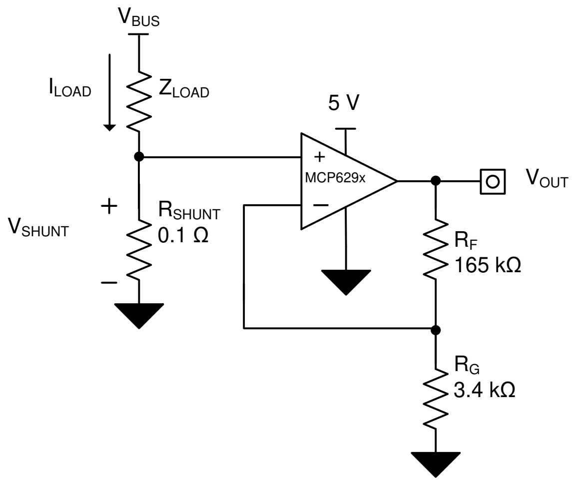


Figure 33. MCP629x in a Low-Side, Motor-Control Application

9.2.1 Design Requirements

The design requirements for this design are:

- Load current: 0 A to 1 A
- Output voltage: 4.95 V
- Maximum shunt voltage: 100 mV

Typical Application (continued)

9.2.2 Detailed Design Procedure

The transfer function of the circuit in Figure 33 is shown in Equation 1.

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times Gain \tag{1}$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0 A to 1 A. To keep the shunt voltage below 100 mV at maximum load current, the largest shunt resistor is defined using Equation 2.

$$R_{SHUNT} = \frac{V_{SHUNT\_MAX}}{I_{LOAD\_MAX}} = \frac{100mV}{1A} = 100m\Omega \tag{2}$$

Using Equation 2, R_{SHUNT} is 100 mΩ. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the MCP629x to produce an output voltage of roughly 0 V to 4.95 V. The gain needed by the MCP629x to produce the necessary output voltage is calculated using Equation 3:

$$Gain = \frac{\left(V_{OUT\_MAX} - V_{OUT\_MIN}\right)}{\left(V_{IN\_MAX} - V_{IN\_MIN}\right)} \tag{3}$$

Using Equation 3, the required gain is calculated to be 49.5 V/V, which is set with resistors R_F and R_G. Equation 4 is used to size the resistors, R_F and R_G, to set the gain of the MCP629x to 49.5 V/V.

$$Gain = 1 + \frac{(R_F)}{(R_G)} \tag{4}$$

Choosing R_F as 165 kΩ and R_G as 3.4 kΩ provides a combination that equals roughly 49.5 V/V. Figure 34 shows the measured transfer function of the circuit shown in Figure 33.

9.2.3 Application Curve

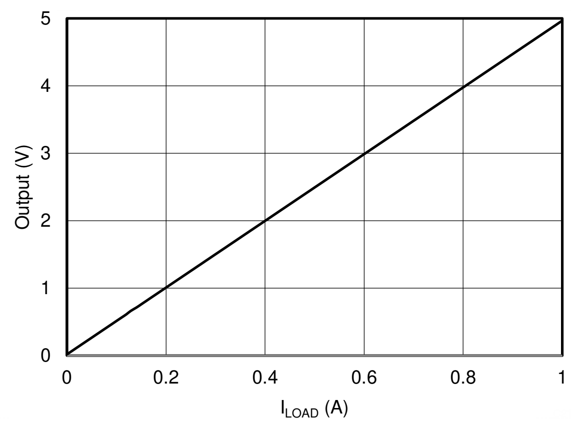


Figure 34. Low-Side, Current-Sense Transfer Function

10 Power Supply Recommendations

The MCP629x series is specified for operation from 2.4 V to 5.5 V (±1.2 V to ±2.75 V); many specifications apply from –40°C to 125°C. The *Typical Characteristics* section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 6 V can permanently damage the device; see the *Absolute Maximum Ratings* table.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout Example* section.

10.1 Input and ESD Protection

The MCP629x series incorporates internal ESD protection circuits on all pins. For input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10-mA, as stated in the *Absolute Maximum Ratings* table. Figure 35 shows how a series input resistor is added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

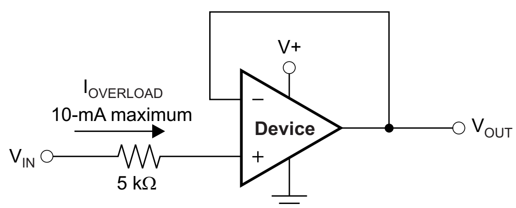


Figure 35. Input Current Protection

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good printed-circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of op amp itself. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see *Circuit Board Layout Techniques*.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in Figure 37, keeping RF and RG close to the inverting input minimizes parasitic capacitance on the inverting input.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

11.2 Layout Example

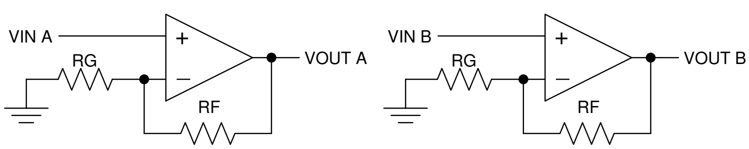


Figure 36. Schematic Representation for Figure 37

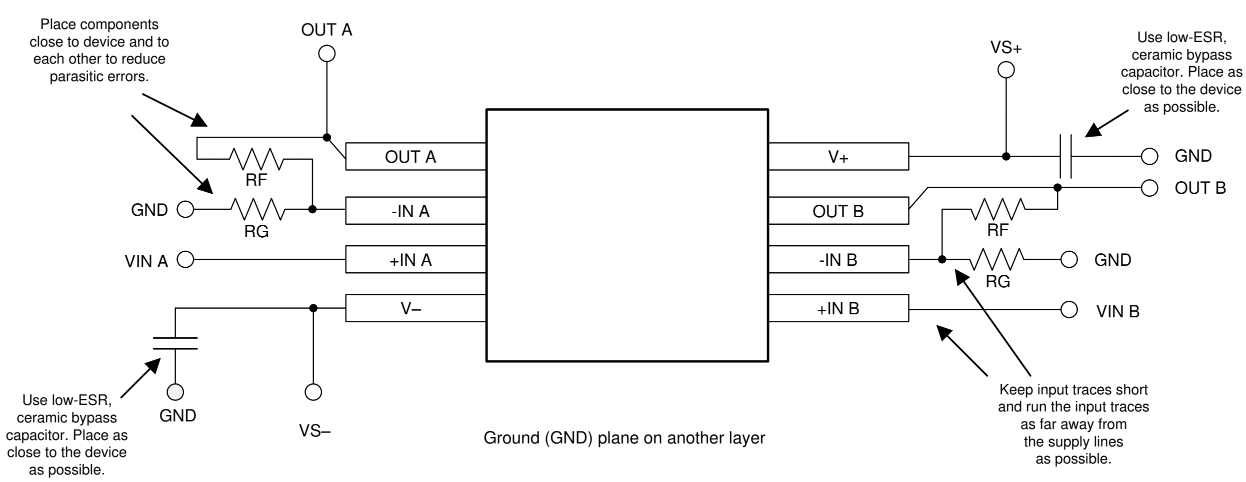


Figure 37. Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

Circuit Board Layout Techniques, SLOA089

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
MCP6291	Click here	Click here	Click here	Click here	Click here
MCP6292	Click here	Click here	Click here	Click here	Click here
MCP6294	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MCP6291IDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1U3F
MCP6291IDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1U3F
MCP6291IDBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1U3F
MCP6291IDBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1U3F
MCP6291IDBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1U3F
MCP6291IDCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1EL
MCP6291IDCKR.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1EL
MCP6292IDDFR	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	M292
MCP6292IDDFR.A	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	M292
MCP6292IDDFR.B	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 125	M292
MCP6292IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	M292
MCP6292IDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M292
MCP6292IDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	M292
MCP6292IDGKT.A	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M292
MCP6292IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MC6292
MCP6292IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MC6292
MCP6294IDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MCP6294D
MCP6294IDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MCP6294D
MCP6294IPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	MCP6294
MCP6294IPWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	MCP6294
MCP6294IPWT	Active	Production	TSSOP (PW) | 14	250 | SMALL T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	MCP6294
MCP6294IPWT.A	Active	Production	TSSOP (PW) | 14	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	MCP6294

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

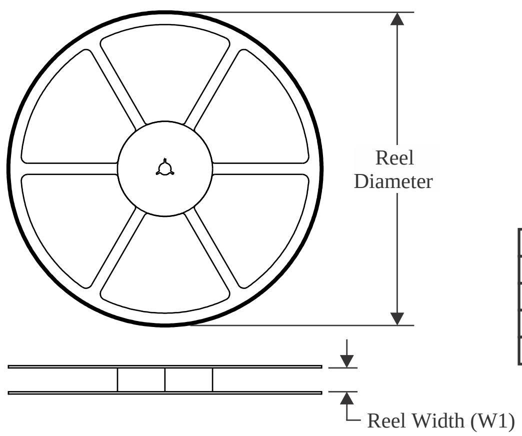
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

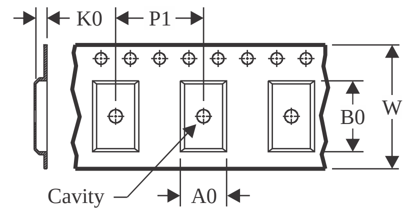
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

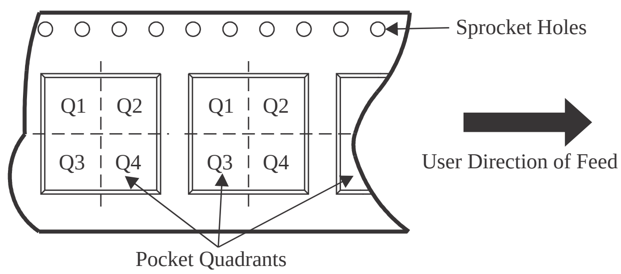


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

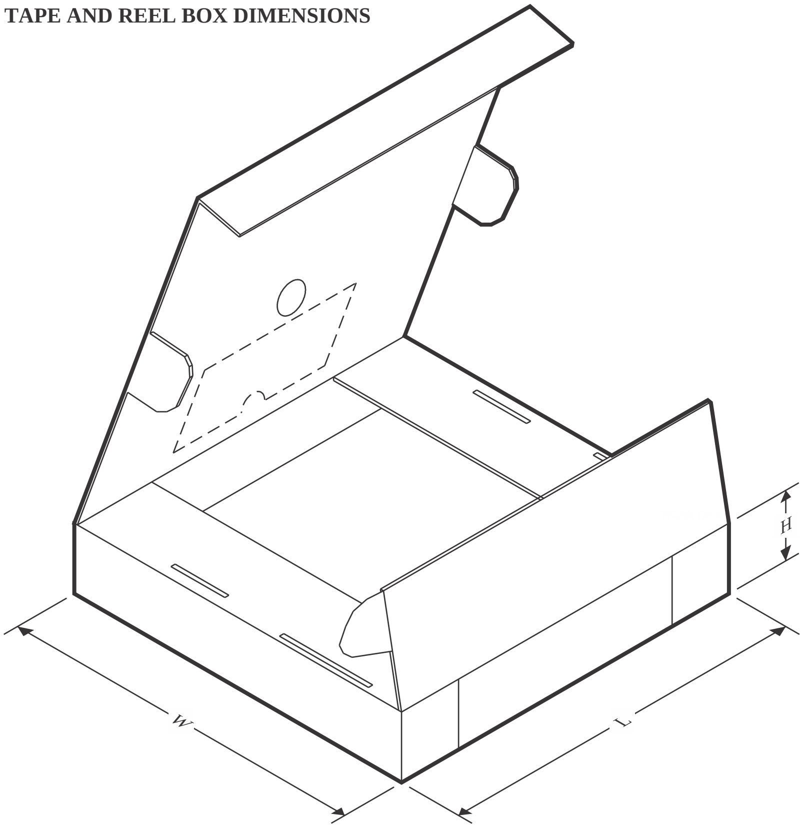
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

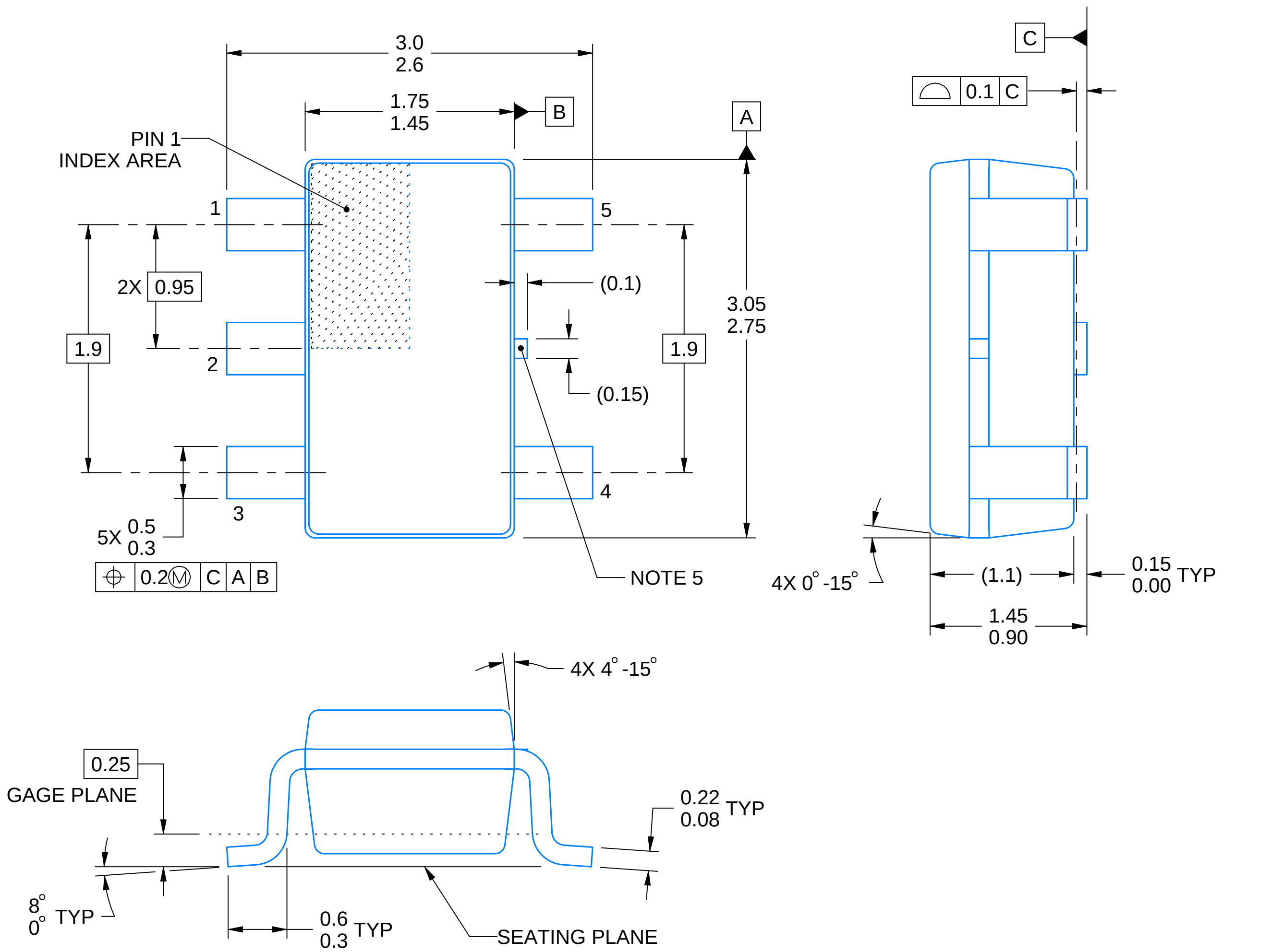
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MCP6291IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
MCP6291IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
MCP6291IDBVRG4	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
MCP6291IDCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
MCP6292IDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
MCP6292IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
MCP6292IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
MCP6292IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
MCP6292IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
MCP6294IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
MCP6294IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MCP6294IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MCP6294IPWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

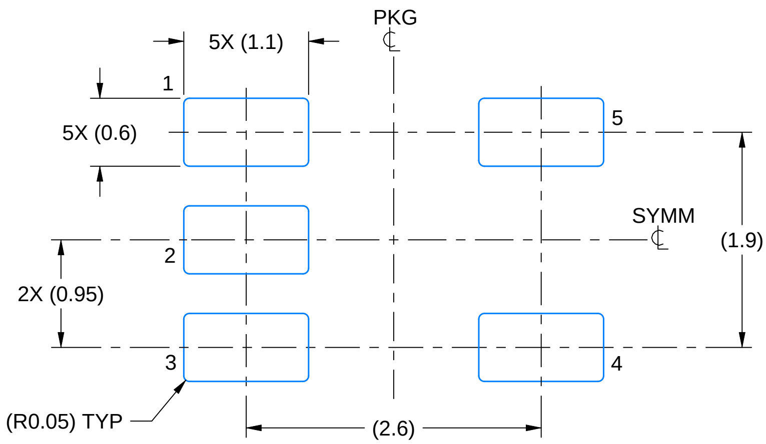
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MCP6291IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
MCP6291IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
MCP6291IDBVRG4	SOT-23	DBV	5	3000	210.0	185.0	35.0
MCP6291IDCKR	SC70	DCK	5	3000	210.0	185.0	35.0
MCP6292IDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
MCP6292IDGKR	VSSOP	DGK	8	2500	356.0	356.0	36.0
MCP6292IDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
MCP6292IDGKT	VSSOP	DGK	8	250	353.0	353.0	32.0
MCP6292IDR	SOIC	D	8	2500	353.0	353.0	32.0
MCP6294IDR	SOIC	D	14	2500	353.0	353.0	32.0
MCP6294IPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
MCP6294IPWR	TSSOP	PW	14	2000	366.0	364.0	50.0
MCP6294IPWT	TSSOP	PW	14	250	353.0	353.0	32.0



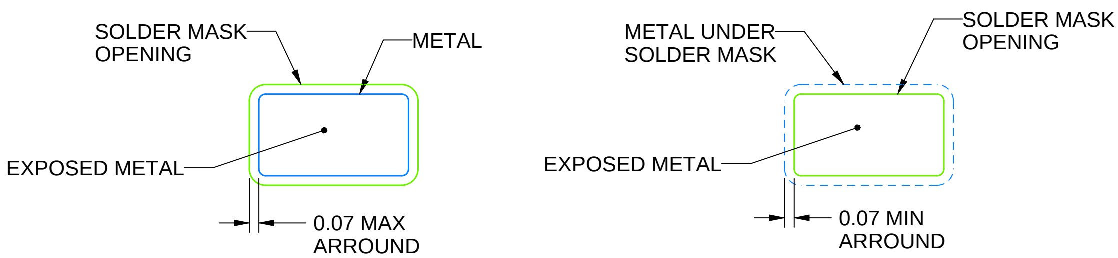
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK DEFINED (PREFERRED)

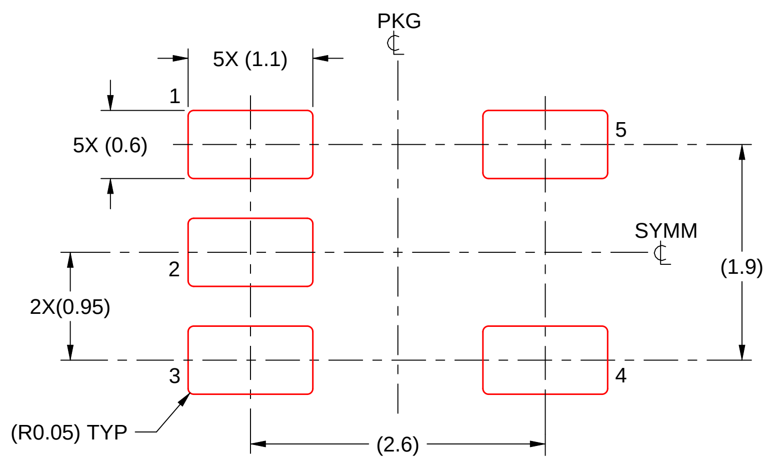
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

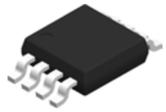
4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

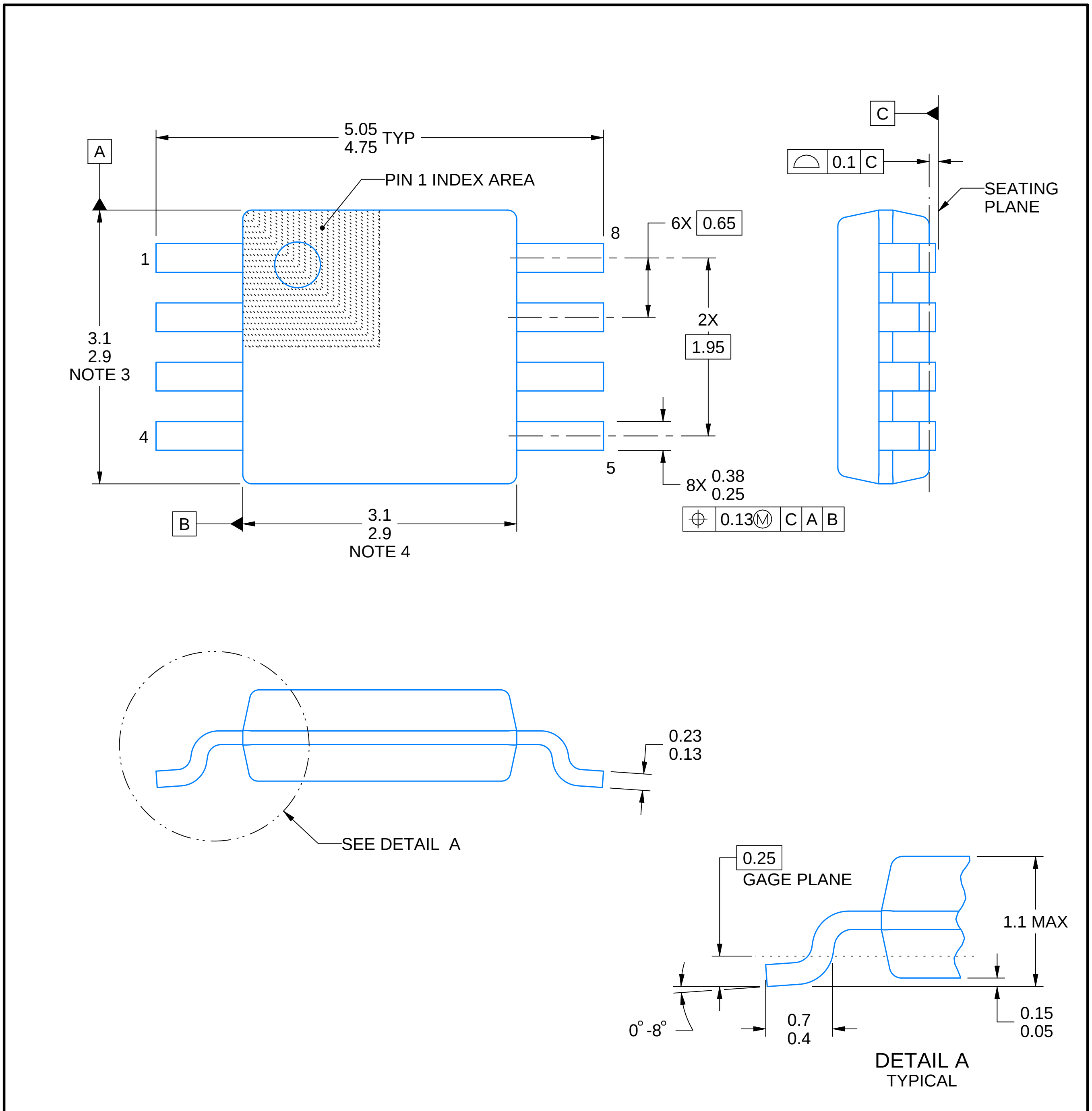
PACKAGE OUTLINE

DGK0008A



VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

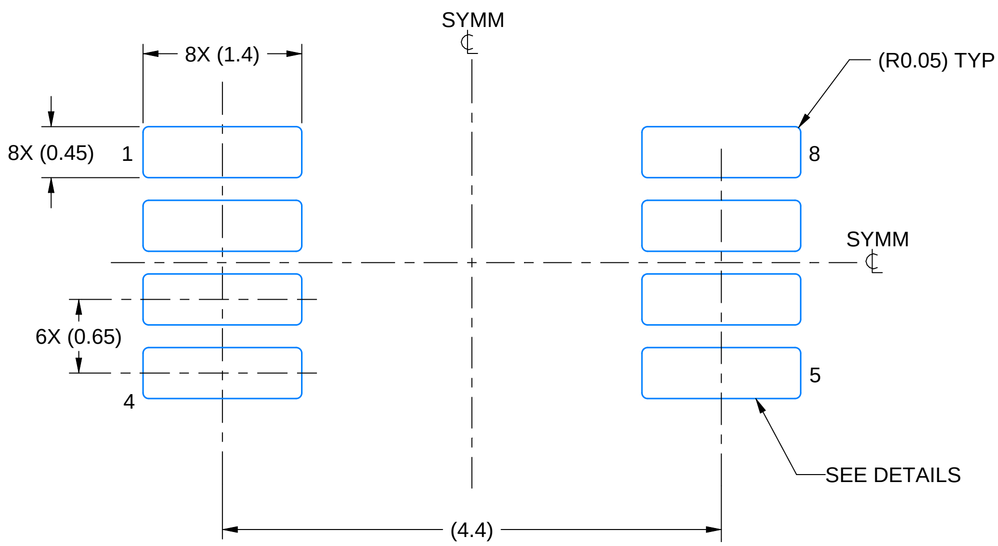


4214862/A 04/2023

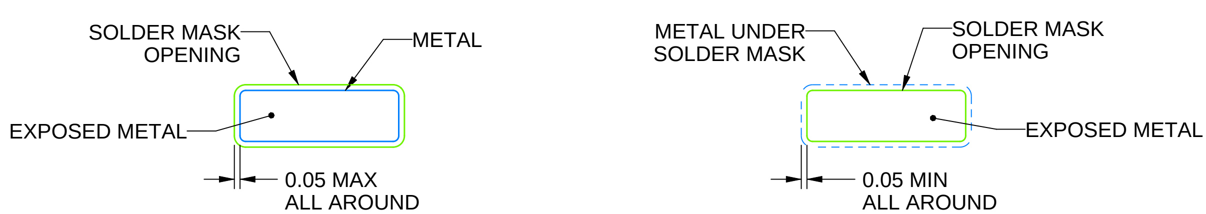
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

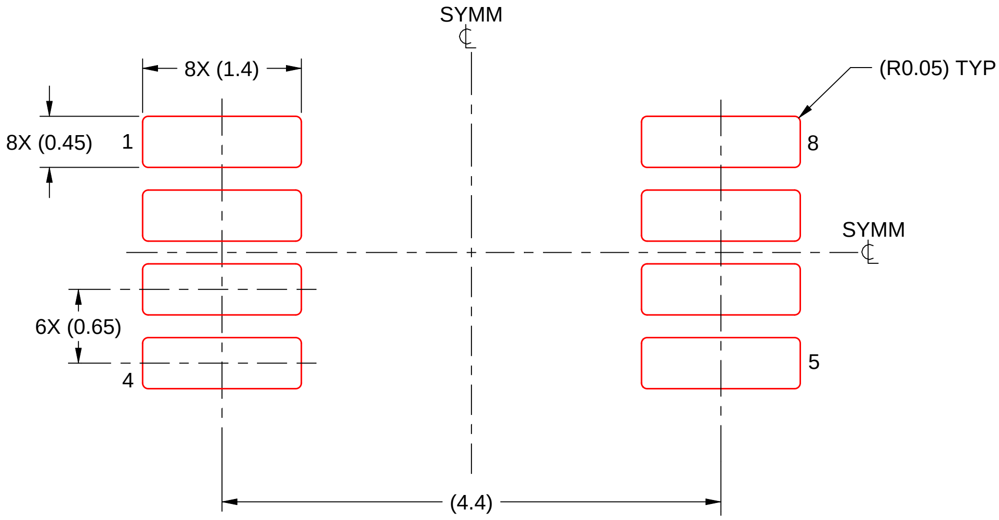


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

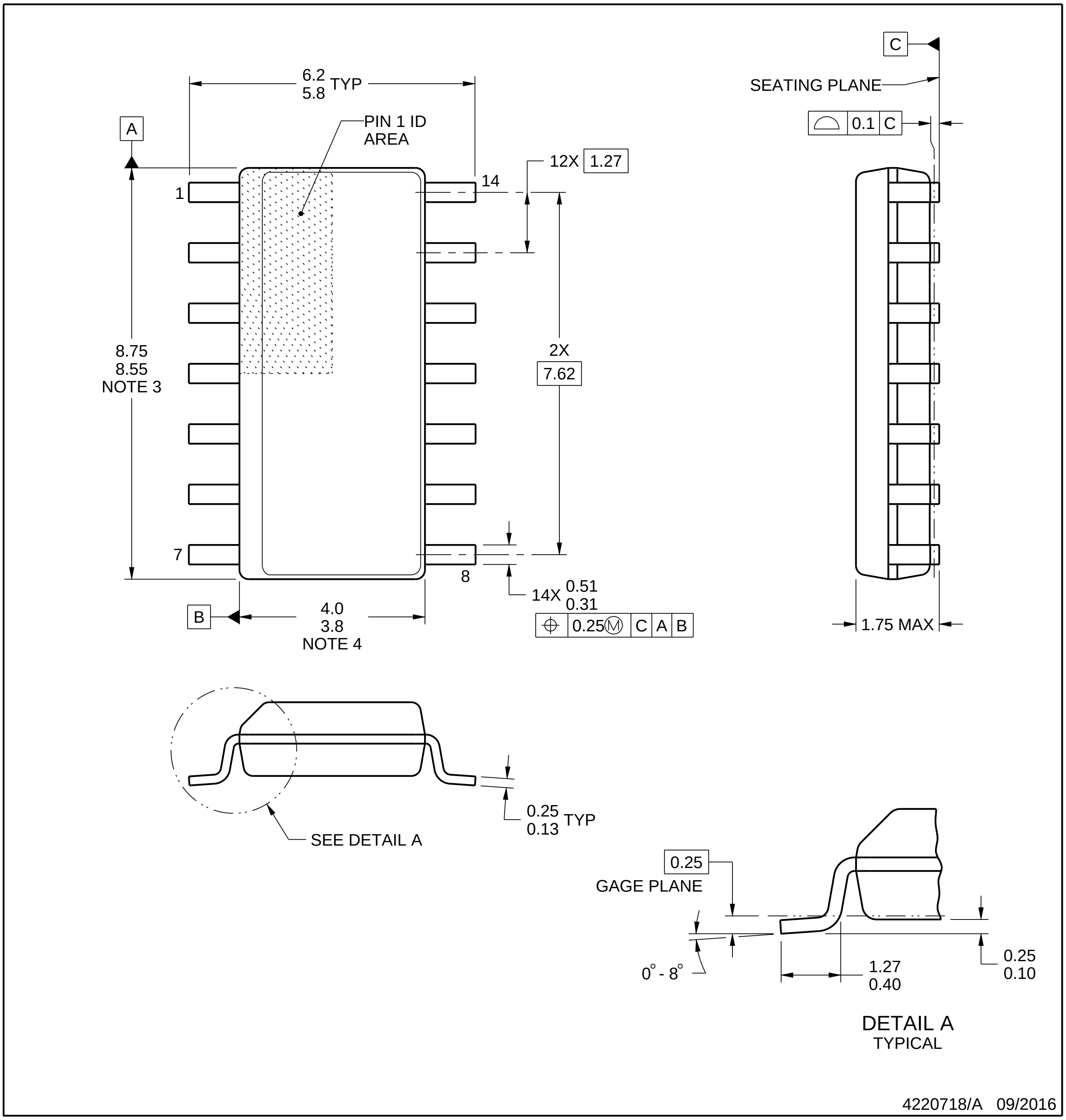


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

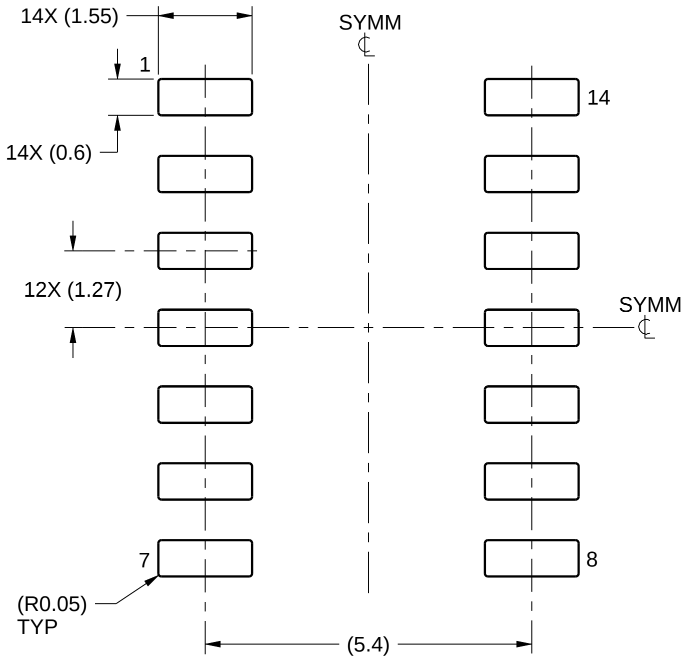
NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

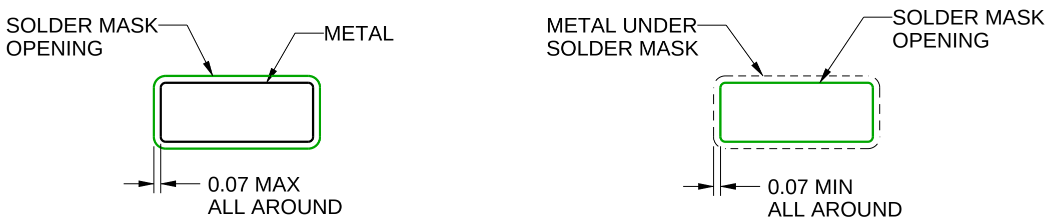


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



NON SOLDER MASK
DEFINED

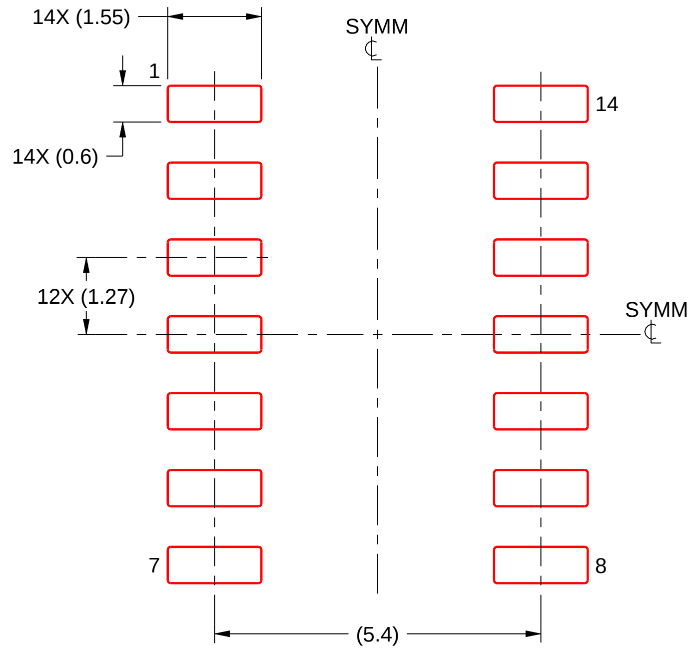
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

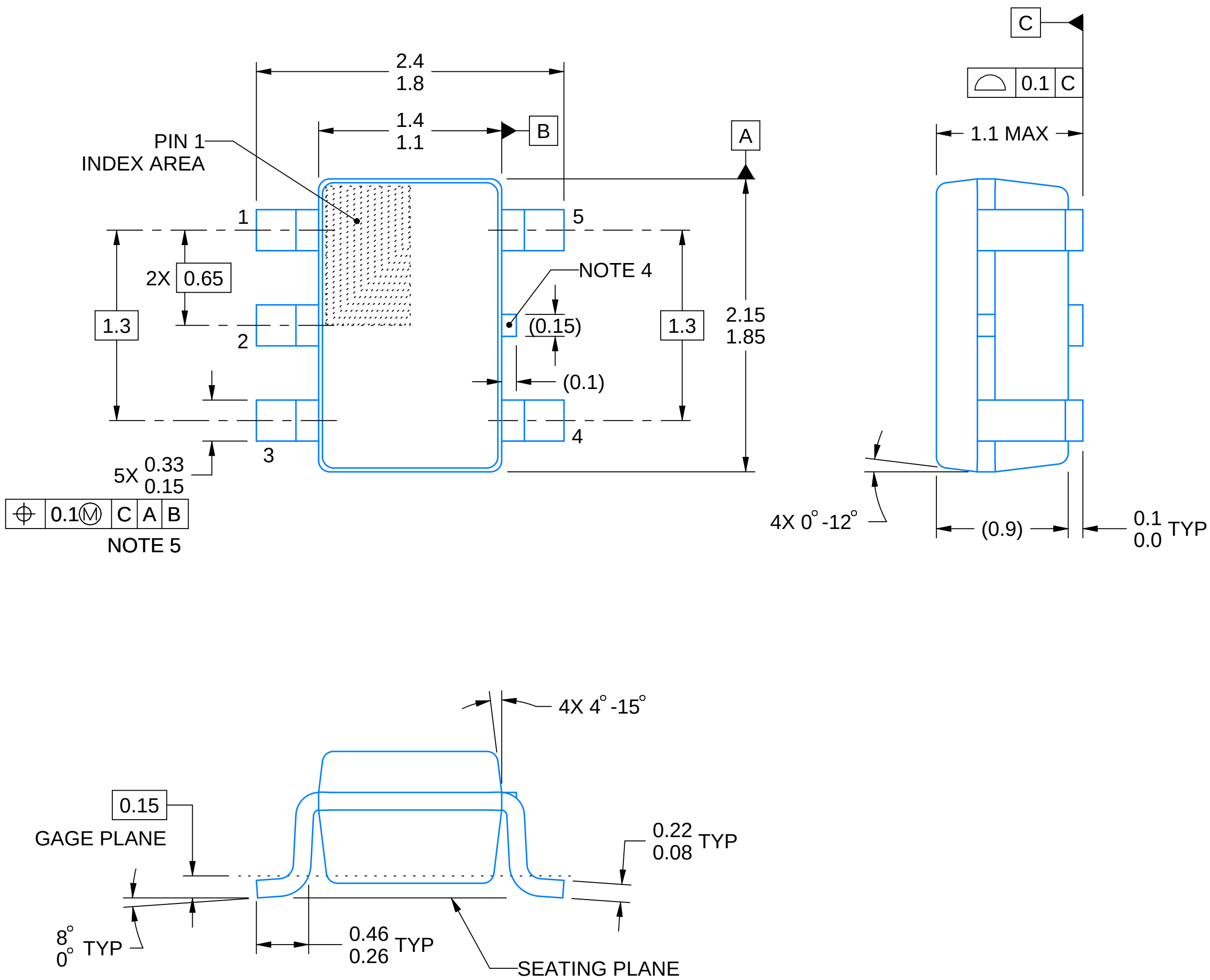
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

SOT - 1.1 max height

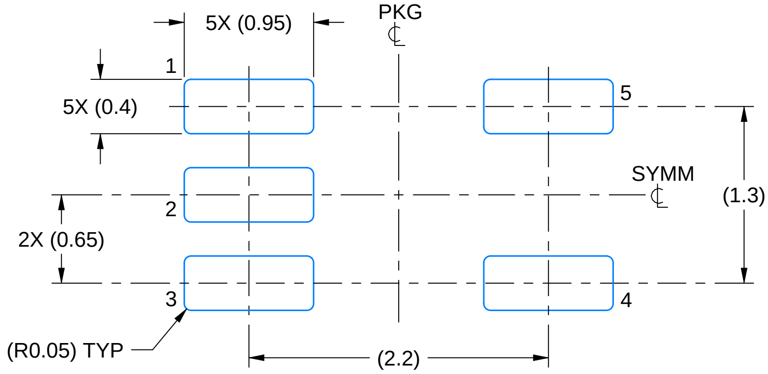
SMALL OUTLINE TRANSISTOR



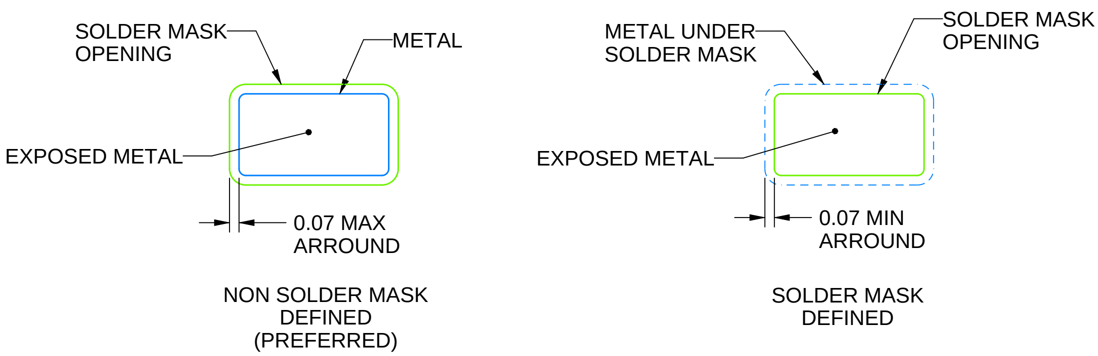
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

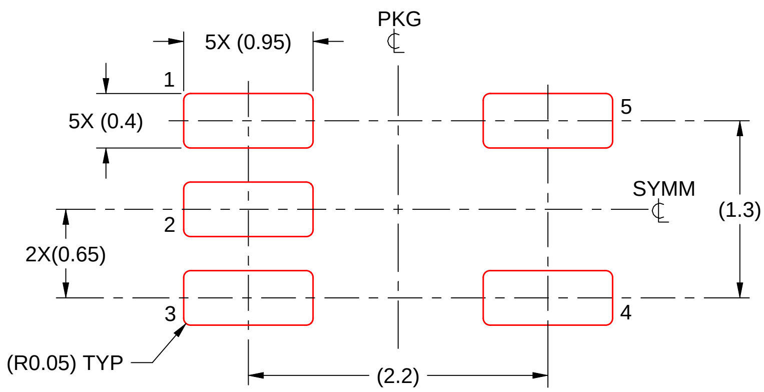


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

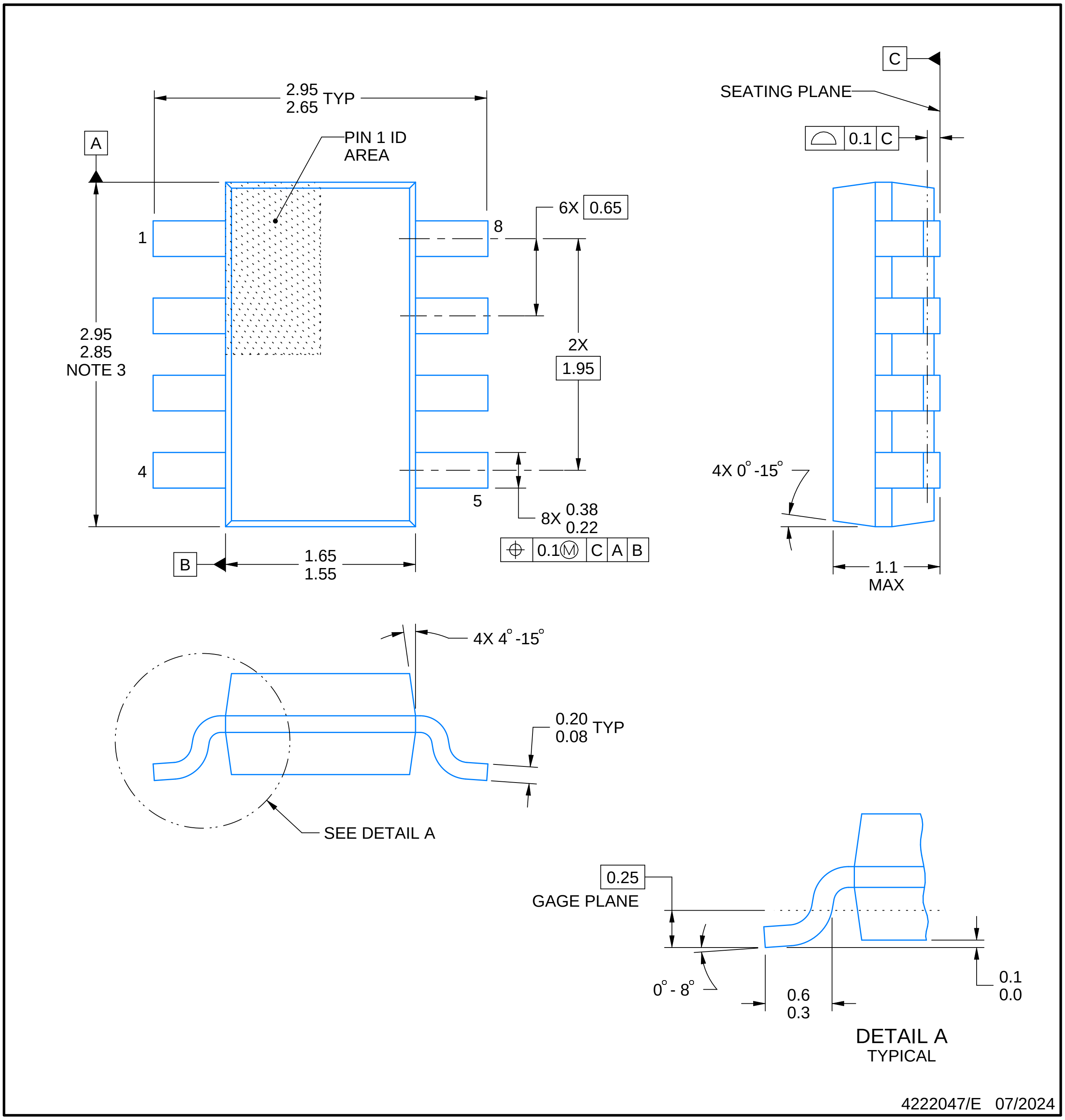


SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

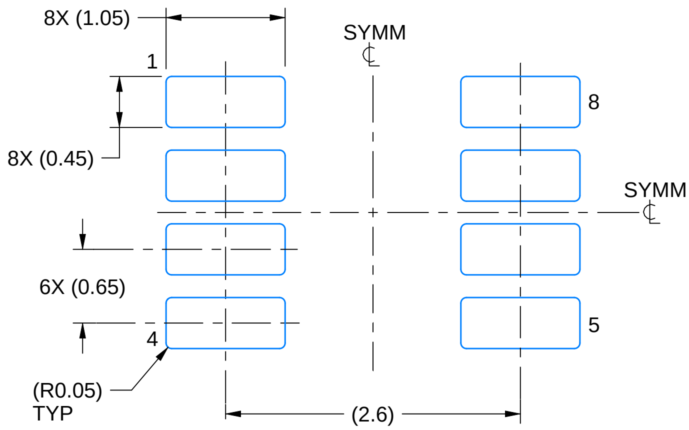
NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

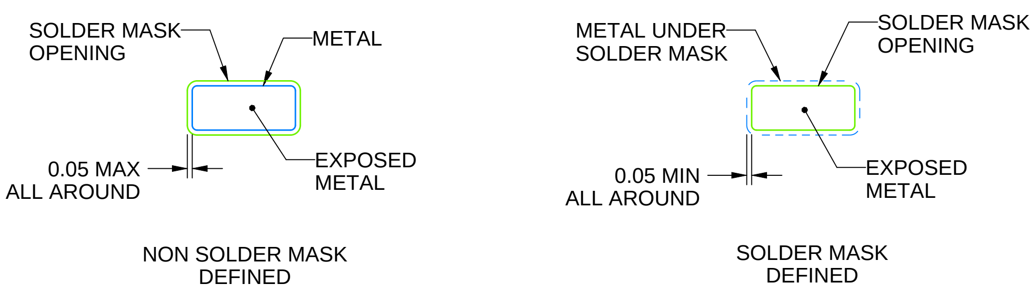


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

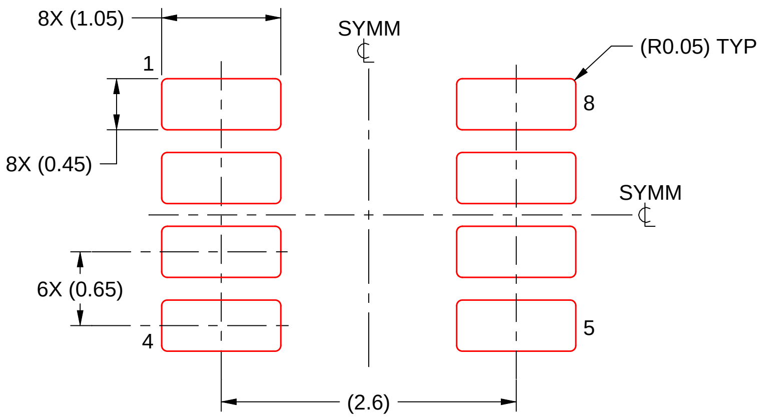


SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

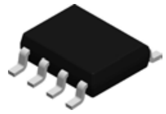


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

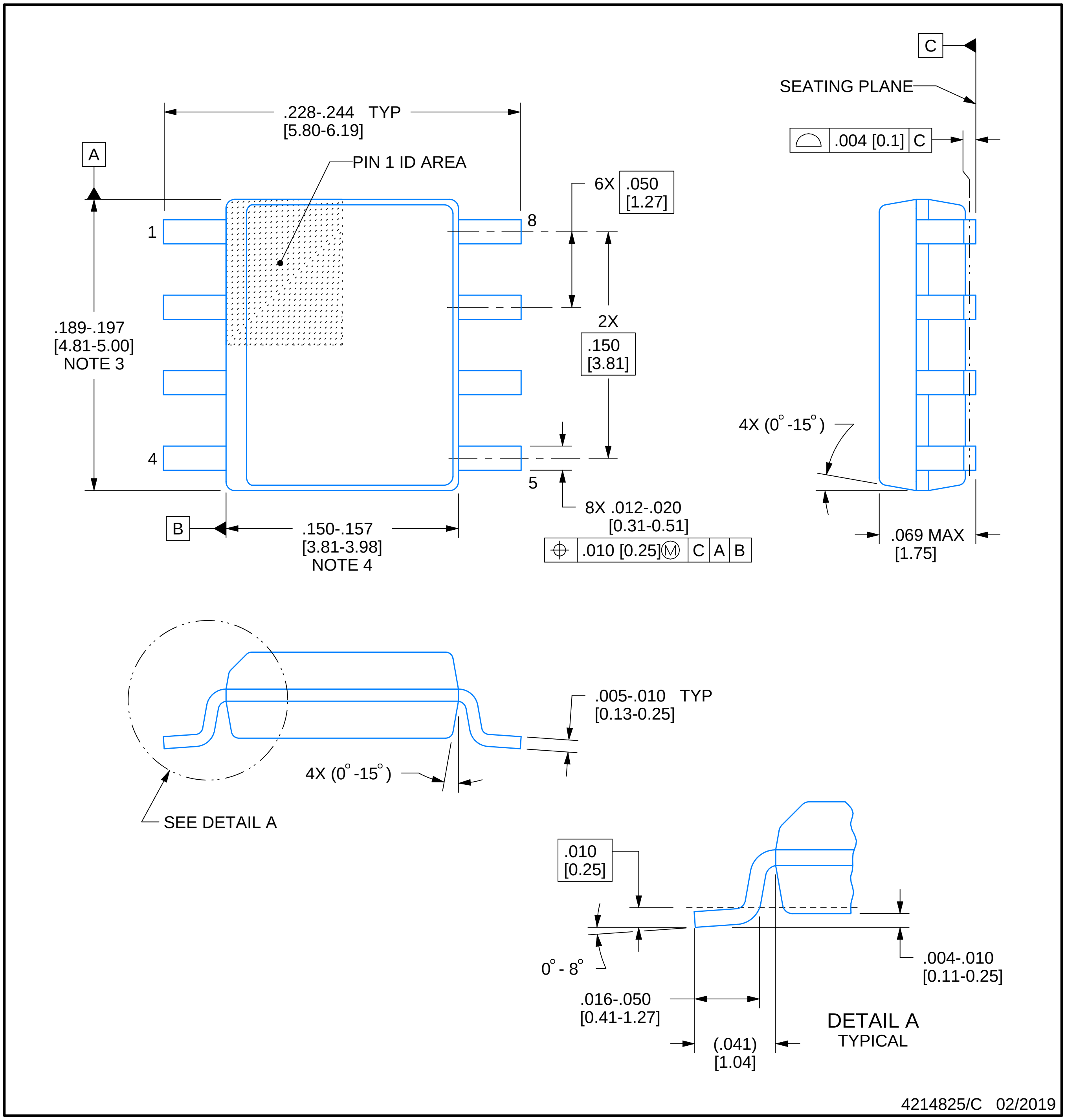
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.



PACKAGE OUTLINE

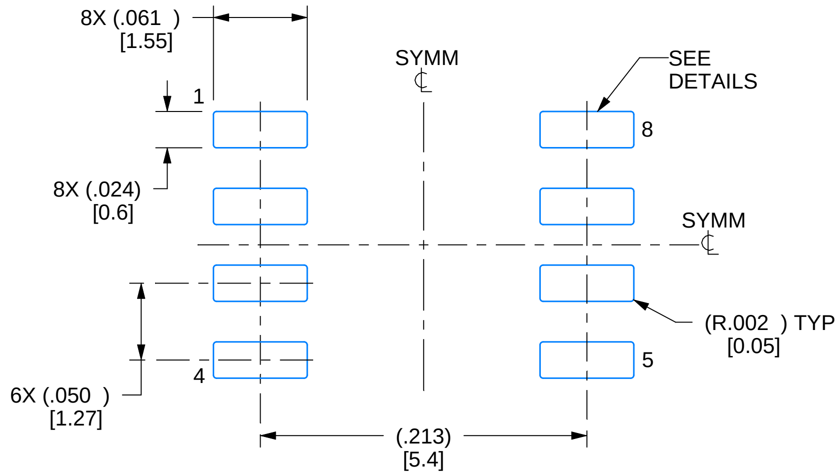
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

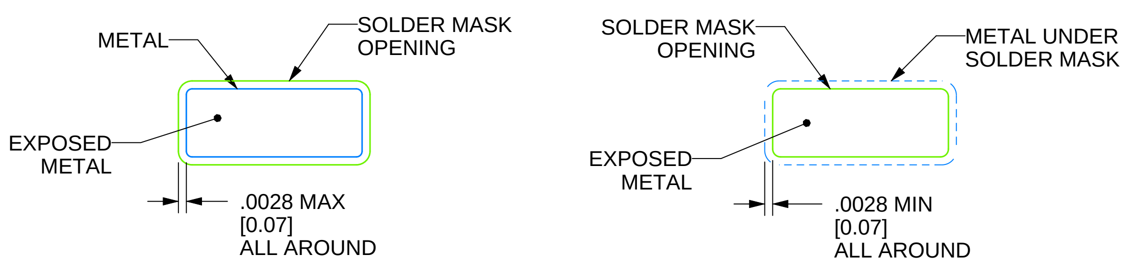


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK DEFINED

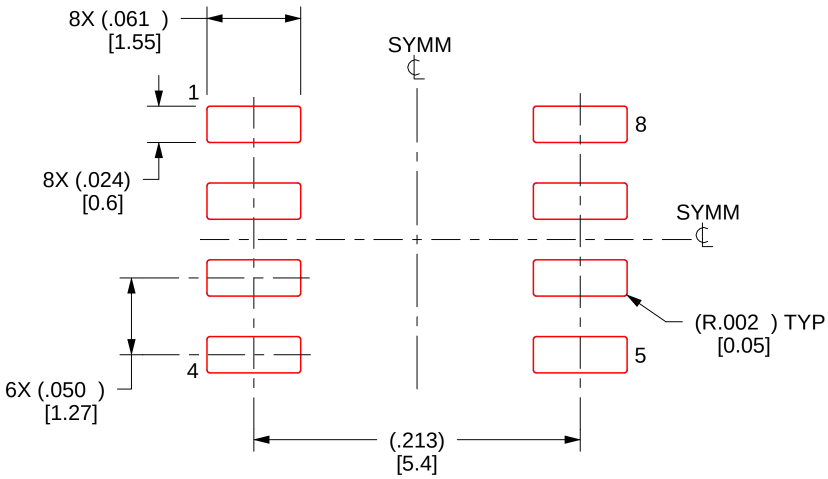
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

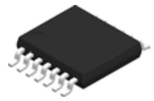


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

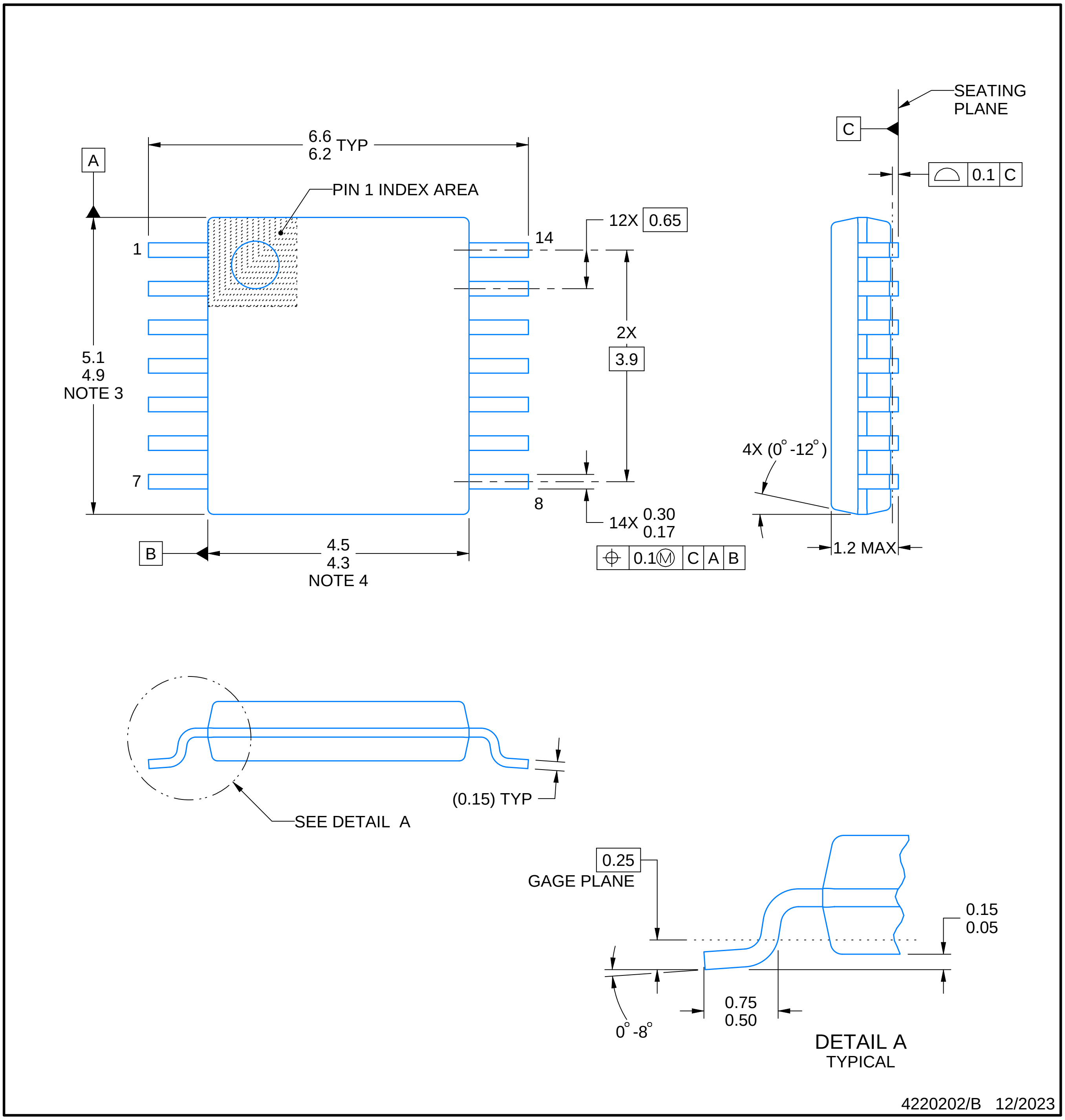


PACKAGE OUTLINE

PW0014A

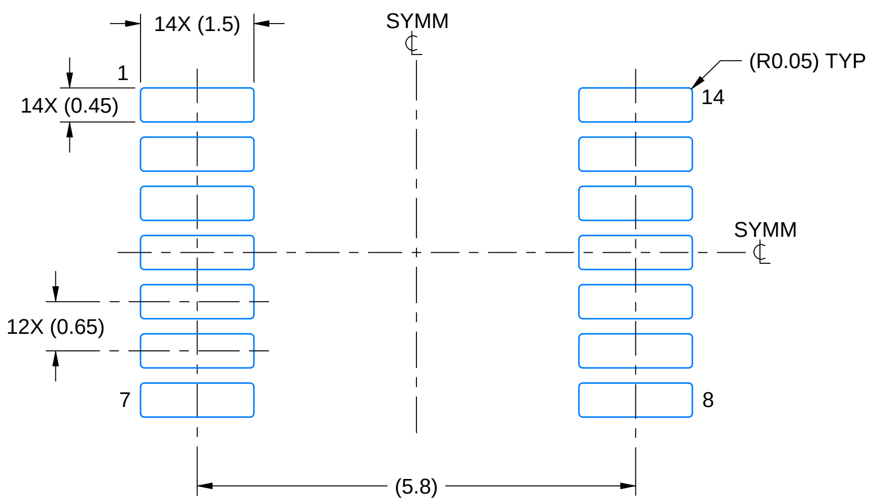
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

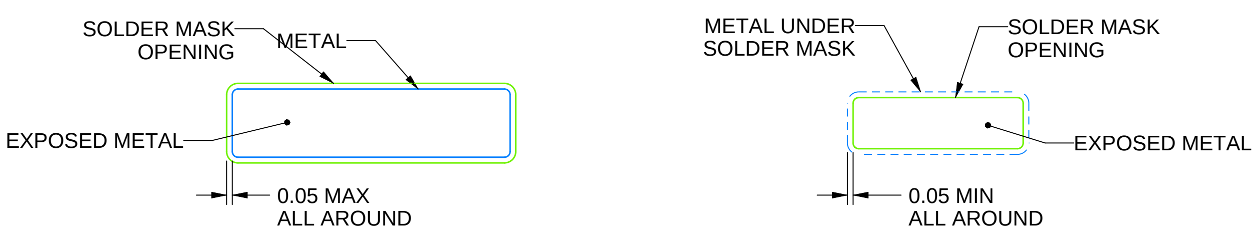


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



NON-SOLDER MASK
DEFINED
(PREFERRED)

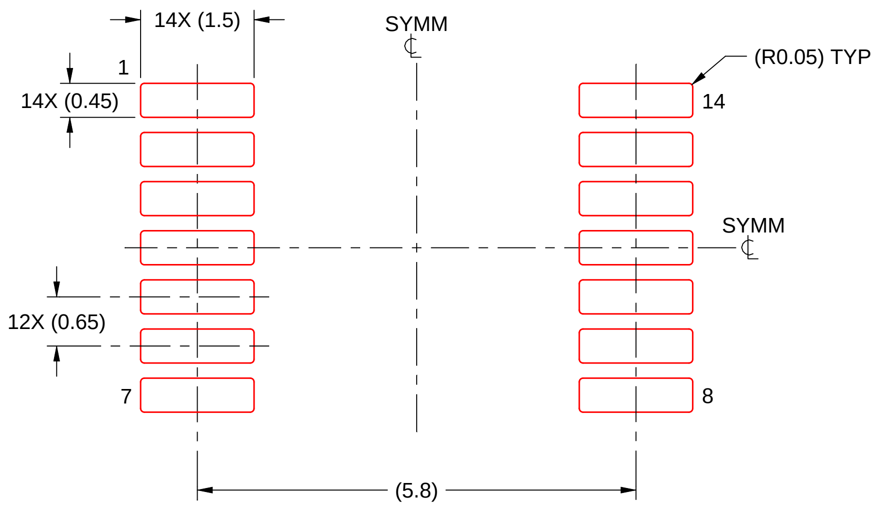
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER