

MAX3221E 3V to 5.5V Single-Channel RS-232 Line Driver and Receiver With ±15kV **IEC ESD Protection**

1 Features

- ESD protection for RS-232 pins
 - ±15kV Human-body model (HBM)
 - ±8kV (IEC 61000-4-2, Contact discharge)
 - ±15kV (IEC 61000-4-2, Air-gap discharge)
- Meets or exceeds the requirements of TIA/ EIA-232-F and ITU v.28 standards
- Operates with 3V to 5.5V V_{CC} supply
- Operates up to 250kbit/s
- One driver and one receiver
- Low standby current: 1µA typical
- Accepts 5V logic input with 3.3V supply
- Auto-power-down feature automatically disables drivers for power savings
- Alternative high-speed device (1Mbit/s)
 - SN75C3221E and SN65C3221E

2 Applications

- **Industrial PCs**
- Wired networking
- Data center and enterprise computing
- Battery-powered systems
- **PDAs**
- **Notebooks**
- Laptops
- Palmtop PCs
- Hand-held equipment

3 Description

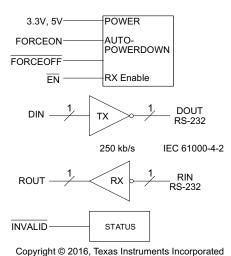
The MAX3221E is a single driver, single receiver RS-232 solution operating from a single V_{CC} supply. The RS-232 pins provide IEC 61000-4-2 ESD protection. The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3V to 5.5V supply. These devices operate at data signaling rates up to 250kbit/s and a maximum of 30V/µs driver output slew rate.

Flexible control options for power management are available. Auto-power down disables driver and charge pump when the receiver is disconnected or the remote driver is power down. The drivers can be manually enabled or disabled. INVALID output goes low when receiver input is unconnected or power off.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
	SSOP (DB, 16)	6.2mm × 7.8mm
MAX3221E	TSSOP (PW, 16)	5mm × 6.4mm
	SOT-23-THN (DYY, 16)	4.2mm × 2mm

- For more information, see Section 11.
- The package size (length × width) is a nominal value and (2)includes pins, where applicable.



Block Diagram



Table of Contents

1 Features1	7 Detailed Description12
2 Applications1	7.1 Overview12
3 Description1	7.2 Functional Block Diagram12
4 Pin Configuration and Functions3	7.3 Feature Description12
5 Specifications4	7.4 Device Functional Modes13
5.1 Absolute Maximum Ratings4	8 Application and Implementation14
5.2 ESD Ratings4	8.1 Application Information14
5.3 ESD Ratings - IEC Specifications4	8.2 Typical Application14
5.4 Recommended Operating Conditions5	8.3 Power Supply Recommendations15
5.5 Thermal Information5	8.4 Layout16
5.6 Electrical Characteristics5	9 Device and Documentation Support17
5.7 Electrical Characteristics: Driver6	9.1 Receiving Notification of Documentation Updates17
5.8 Electrical Characteristics: Receiver6	9.2 Support Resources17
5.9 Electrical Characteristics: Auto-Power Down6	9.3 Trademarks17
5.10 Switching Characteristics: Driver7	9.4 Electrostatic Discharge Caution17
5.11 Switching Characteristics: Receiver7	9.5 Glossary17
5.12 Switching Characteristics: Auto-Power Down7	10 Revision History17
5.13 Typical Characteristics8	11 Mechanical, Packaging, and Orderable
6 Parameter Measurement Information9	Information18



4 Pin Configuration and Functions

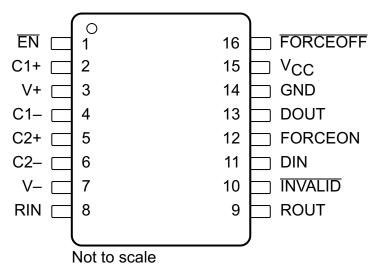


Figure 4-1. DB, PW or DYY Package 16-Pin SSOP, TSSOP, or SOT-23-THN (Top View)

Table 4-1. Pin Functions

P	IN	TYPE	DESCRIPTION
NAME	NO.	1176	DESCRIPTION
C1+	2		Positive terminals of the voltage-doubler charge pump capacitors
C2+	5	T -	Positive terminals of the voltage-doubler charge pump capacitors
C1-	4		Negative terminals of the voltage doubler charge nump agreeiters
C2-	6	Ī —	Negative terminals of the voltage-doubler charge pump capacitors
DIN	11	I	Driver input
DOUT	13	0	RS-232 driver output
EN	1	1	Low input enables receiver ROUT output. High input sets ROUT to high impedance.
FORCEOFF	16	I	Automatic power-down control input
FORCEON	12	I	Automatic power-down control input
GND	14	_	Ground
INVALID	10	0	Invalid output pin. Output low when RIN input is unpowered.
RIN	8	I	RS-232 receiver input
ROUT	9	0	Receiver output
V _{CC}	15	_	3V to 5.5V supply voltage
V+	3	0	5.5V supply generated by the charge pump
V-	7	0	-5.5V supply generated by the charge pump



5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	5 1 3 (MIN	MAX	UNIT
V _{CC}	Supply voltage ⁽²⁾		-0.3	6	V
V+	Positive output supply voltage ⁽²⁾		-0.3	7	V
V-	Negative output supply voltage ⁽²⁾		0.3	- 7	V
V+ – V–	Supply voltage difference ⁽²⁾			13	V
V	Input voltage	DIN, FORCEOFF, FORCEON, EN	-0.3	6	V
V _I	Input voltage	RIN	-25	25	V
V	Output valtage	DOUT	-13.2	13.2	V
Vo	Output voltage	-0.3	V _{CC} + 0.3	V	
TJ	Operating virtual junction temperature			150	°C
T _{stg}	Storage temperature			150	°C

⁽¹⁾ Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

				VALUE	UNIT
	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	Pins 8 and 13	±15000		
V _{(ESD}	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC 35-00 NV	All other pins	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	All pins	±1500	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 ESD Ratings - IEC Specifications

				VALUE	UNIT
V	Electrostatio discharge	IEC 61000-4-2 Contact Discharge, DOUT and RIN (1) (2)	- Pins 8 and 13	±8000	V
V _(ESD)	Electrostatic discharge	IEC 61000-4-2 Air-Gap Discharge, DOUT and RIN ⁽¹⁾ ⁽²⁾	TIIIS O AIIU 13	±15000	V

- (1) A minimum of 1µF capacitor is required between VCC and GND to meet the specified IEC-ESD level.
- (2) For optimized IEC ESD performance for DYY package, the recommendation is to have series resistor (≥ 50Ω), on all logic inputs directly connected to power or ground, to minimize the transient currents going into or out of the logic pins.

Product Folder Links: MAX3221E

⁽²⁾ All voltages are with respect to network GND.

5.4 Recommended Operating Conditions

See Figure 8-1 (1)

	-			MIN	NOM	MAX	UNIT
	Supply voltage	V _{CC} = 3.3V	3	3.3	3.6	V	
	Supply voltage			4.5	5	5.5	V
V _{IH} Driver and control high-level input voltag	DIN, FORCEOFF, FORCEON, EN	V _{CC} = 3.3V	2			V	
	Driver and control high-level input voltage	DIN, FORCEOFF, FORCEON, EN	V _{CC} = 5V	2.4			V
V_{IL}	Driver and control low-level input voltage	DIN, FORCEOFF, FORCEON, EN	•			0.8	V
VI	Driver and control input voltage	DIN, FORCEOFF, FORCEON		0		5.5	V
VI	Receiver input voltage			-25		25	V
T _A	Operating free air temperature	MAX3221EC		0		70	°C
	Operating free-air temperature	MAX3221EI		-40		85	C

⁽¹⁾ Test conditions are C1–C4 = $0.1\mu F$ at V_{CC} = $3.3V \pm 0.3V$; C1 = $0.047\mu F$, C2–C4 = $0.33\mu F$ at V_{CC} = $5V \pm 0.5V$.

5.5 Thermal Information

			MAX3221E				
THERMAL METRIC ⁽¹⁾		DB (SSOP)	PW (TSSOP)	DYY (SOT-23-THN)	UNIT		
		16 PINS	16 PINS	16 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	105.8	110.9	120.0	°C/W		
R _{θJC(top)}	Junction-to-case (top) thermal resistance	51.9	41.7	56.8	°C/W		
R _{θJB}	Junction-to-board thermal resistance	57.6	57.2	51.3	°C/W		
Ψ_{JT}	Junction-to-top characterization parameter	14.1	4.2	2.6	°C/W		
ΨЈВ	Junction-to-board characterization parameter	56.8	56.6	50.9	°C/W		

For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.6 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(2)

	PARAMETE	R	TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
II	Input leakage current	FORCEOFF, FORCEON, EN				±0.01	±1	μΑ
		Auto-power down disabled		No load, FORCEOFF and FORCEON at V _{CC}		0.3	1	mA
I _{CC}	Supply current	Powered off	Powered off	No load, FORCEOFF at GND		1	10	
	Auto-power enabled	Auto-power down enabled		No load, FORCEOFF at V _{CC} , FORCEON at GND, All RIN are open or grounded		1	10	μΑ

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⁽¹⁾ All typical values are at V_{CC} = 3.3V or V_{CC} = 5V, and T_A = 25°C. (2) Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3V \pm 0.3V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5V \pm 0.5V.



5.7 Electrical Characteristics: Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(3)

	PARAMETER	TEST	TEST CONDITIONS			TYP ⁽¹⁾	MAX	UNIT
V _{OH}	High-level output voltage	DOUT at $R_L = 3k\Omega$ to GND,	DIN = GND		5	5.4		V
V _{OL}	Low-level output voltage	DOUT at $R_L = 3k\Omega$ to GND,	DIN = V _{CC}		- 5	-5.4		V
I _{IH}	High-level input current	V _I = V _{CC}	$V_I = V_{CC}$			±0.01	±1	μA
I _{IL}	Low-level input current	V _I = GND				±0.01	±1	μA
	Short-circuit	V _{CC} = 3.6V,	V _O = 0V			±35	±60	mA
los	output current ⁽²⁾	V _{CC} = 5.5V,	V _O = 0V			±35	±60	ША
r _o	Output resistance	V _{CC} , V+, and V- = 0V,	V _O = ±2V		300	10M		Ω
	Output leakage current	FORCEOFF = GND	$V_{O} = \pm 12V$,	V _{CC} = 3V to 3.6V			±25	^
I _{off}		FORCEOTT - GND	$V_O = \pm 10V$,	V _{CC} = 4.5V to 5.5V			±25	μA

- All typical values are at V_{CC} = 3.3V or V_{CC} = 5V, and T_A = 25°C.
- Short-circuit durations should be controlled to prevent exceeding the device absolute power-dissipation ratings, and not more than one output should be shorted at a time.
- Test conditions are C1–C4 = $0.1\mu F$ at V_{CC} = $3.3V \pm 0.3V$; C1 = $0.047\mu F$, C2–C4 = $0.33\mu F$ at V_{CC} = $5V \pm 0.5V$.

5.8 Electrical Characteristics: Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(2)

	PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}	High-level output voltage	I _{OH} = -1mA	V _{CC} - 0.6	V _{CC} - 0.1		V
V _{OL}	Low-level output voltage	I _{OL} = 1.6mA			0.4	V
V _{IT+}	Positive-going input threshold voltage	V _{CC} = 3.3V		1.6	2.4	V
	Positive-going input threshold voltage	V _{CC} = 5V		1.9	2.4	V
\/	Negative going input threshold voltage	V _{CC} = 3.3V	0.6	1.1		V
V_{IT-}	Negative-going input threshold voltage	V _{CC} = 5V	0.8	1.4		V
V _{hys}	Input hysteresis (V _{IT+} - V _{IT-})			0.5		V
I _{off}	Output leakage current	EN = V _{CC}		±0.05	±10	μA
r _i	Input resistance	V _I = ±3V to ±25V	3	5	7	kΩ

- All typical values are at V_{CC} = 3.3V or V_{CC} = 5V, and T_A = 25°C. Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3V \pm 0.3V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5V \pm 0.5V.

5.9 Electrical Characteristics: Auto-Power Down

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V _{T+(valid)}	Receiver input threshold for INVALID high-level output voltage	FORCEON = GND, FOR	RCEOFF = V _{CC}		2.7	V
V _{T-(valid)}	Receiver input threshold for INVALID high-level output voltage	FORCEON = GND, FOR	RCEOFF = V _{CC}	-2.7		V
V _{T(invalid)}	Receiver input threshold for I NVALID low-level output voltage	FORCEON = GND, FOR	RCEOFF = V _{CC}	-0.3	0.3	V
V _{OH}	INVALID high-level output voltage	I_{OH} = -1mA, FORCEON = GN FORCEOFF = V_{CC}	ID,	V _{CC} -0.6		٧
V _{OL}	INVALID low-level output voltage	I_{OL} = 1.6mA, FORCEON = GN FORCEOFF = V_{CC}	ND,		0.4	V

Product Folder Links: MAX3221E

5.10 Switching Characteristics: Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(3)

	PARAMETER	TE	MIN	TYP ⁽¹⁾	MAX	UNIT	
	Maximum data rate	C _L = 1000pF,	$R_L = 3k\Omega$,	150	250		kbit/s
t _{sk(p)}	Pulse skew ⁽²⁾	C _L = 150pF to 2500pF,	R_L = 3kΩ to 7kΩ, See Figure 6-2		100		ns
25"	Slew rate,	V _{CC} = 3.3V,	C _L = 150pF to 1000pF	6		30	
SR(tr)	transition region (see Figure 6-1)	D 0101 710	C _L = 150pF to 2500pF	4		30	V/µs

- (1) All typical values are at V_{CC} = 3.3V or V_{CC} = 5V, and T_A = 25°C.
- Pulse skew is defined as $|t_{PLH}-t_{PHL}|$ of each channel of the same device. Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3V \pm 0.3V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5V \pm 0.5V.

5.11 Switching Characteristics: Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽³⁾

	PARAMETER	TEST CONDITIONS	TYP ⁽¹⁾	UNIT
t _{PLH}	Propagation delay time, low- to high-level output	C _L = 150pF, See Figure 6-3	150	ns
t _{PHL}	Propagation delay time, high- to low-level output	C _L = 150pF, See Figure 6-3	150	ns
t _{en}	Output enable time	$C_L = 150 \text{pF}, R_L = 3 \text{k}\Omega, \text{ See Figure 6-4}$	200	ns
t _{dis}	Output disable time	C_L = 150pF, R_L = 3k Ω , See Figure 6-4	200	ns
t _{sk(p)}	Pulse skew ⁽²⁾	See Figure 6-3	50	ns

- All typical values are at V_{CC} = 3.3V or V_{CC} = 5V, and T_A = 25°C.
- (2) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
- Test conditions are C1–C4 = $0.1\mu F$ at $V_{CC} = 3.3V \pm 0.3V$; C1 = $0.047\mu F$, C2–C4 = $0.33\mu F$ at $V_{CC} = 5V \pm 0.5V$.

5.12 Switching Characteristics: Auto-Power Down

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

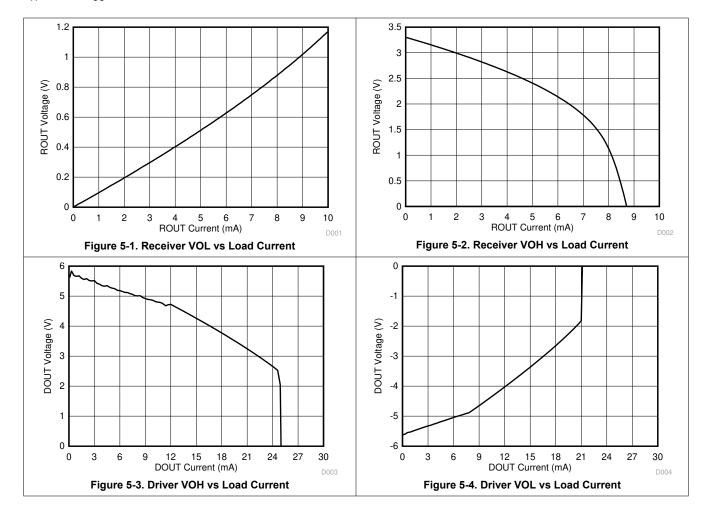
	PARAMETER						
t _{valid}	Propagation delay time, low- to high-level output	1	μs				
t _{invalid}	Propagation delay time, high- to low-level output	30	μs				
t _{en}	Supply enable time	100	μs				

All typical values are at V_{CC} = 3.3V or V_{CC} = 5V, and T_A = 25°C.

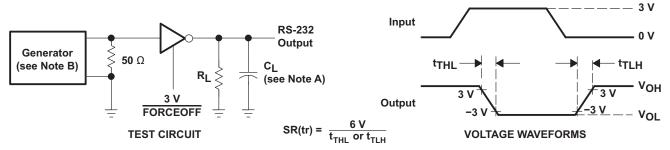


5.13 Typical Characteristics

 $T_A = 25^{\circ}C; V_{CC} = 3.3V$

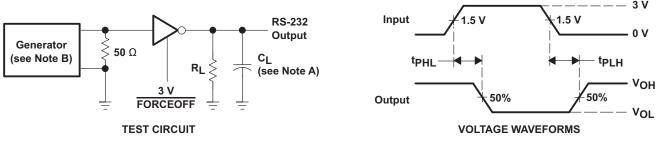


6 Parameter Measurement Information



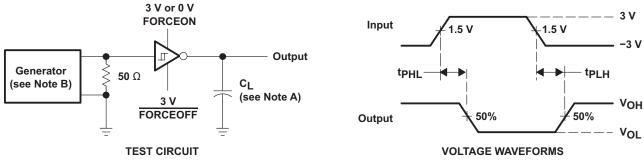
- C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 250kbps, $Z_0 = 50\Omega$, 50% duty cycle, $t_f \le 10$ ns, $t_f \le 10$ ns.

Figure 6-1. Driver Slew Rate



- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 250kbps, $Z_0 = 50\Omega$, 50% duty cycle, $t_f \le 10$ ns, $t_f \le 10$ ns.

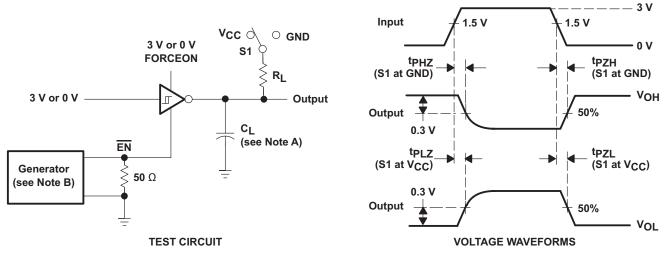
Figure 6-2. Driver Pulse Skew



- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: $Z_0 = 50\Omega$, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

Figure 6-3. Receiver Propagation Delay Times





- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: $Z_0 = 50\Omega$, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.
- C. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- D. t_{PZL} and t_{PZH} are the same as t_{en} .

Figure 6-4. Receiver Enable and Disable Times

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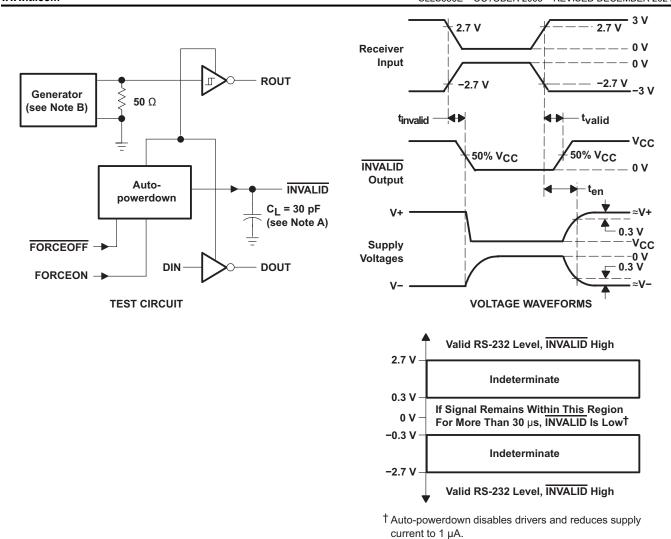


Figure 6-5. INVALID Propagation Delay Times and Driver Enabling Time



7 Detailed Description

7.1 Overview

The MAX3221E is a single driver, single receiver RS-232 solution operating from a single V_{CC} supply. The RS-232 pins provide IEC 61000-4-2 ESD protection. The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3V to 5.5V supply. These devices operate at data signaling rates up to 250kbit/s and a maximum of 30V/ μ s driver output slew rate.

Flexible control options for power management are available when the serial port is inactive. The auto-power-down feature functions when FORCEON is low and $\overline{FORCEOFF}$ is high. During this mode of operation, if the device does not sense a valid RS-232 signal on the receiver input, the driver output is disabled. If $\overline{FORCEOFF}$ is set low and \overline{EN} is high, both the driver and receiver are shut off, and the supply current is reduced to 1 μ A. Disconnecting the serial port or turning off the peripheral drivers causes the auto-power-down condition to occur. Auto-power down can be disabled when FORCEON and $\overline{FORCEOFF}$ are high. With auto-power down enabled, the device is activated automatically when a valid signal is applied to the receiver input. The $\overline{INVALID}$ output notifies the user if an RS-232 signal is present at the receiver input. $\overline{INVALID}$ is high (valid data) if the receiver input voltage is greater than 2.7V or less than -2.7V, or has been between -0.3V and 0.3V for less than 30 μ s. See Figure 6-1 for receiver input levels.

7.2 Functional Block Diagram

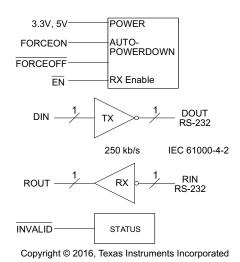


Figure 7-1. Logic Diagram (Positive Logic)

7.3 Feature Description

7.3.1 Power

The power block increases, inverts, and regulates voltage at V+ and V- pins using a charge pump that requires four external capacitors. Auto-power-down feature for driver is controlled by FORCEON and $\overline{\text{FORCEOFF}}$ inputs. Receiver is controlled by $\overline{\text{EN}}$ input. When unpowered, the MAX3221E can be safely connected to an active remote RS-232 device.

7.3.2 RS-232 Driver

One driver interfaces standard logic levels to RS-232 levels. DIN input must be valid high or low.

Product Folder Links: MAX3221E

7.3.3 RS-232 Receiver

One receiver interfaces RS-232 levels to standard logic levels. An open input results in a high output on ROUT. RIN input includes an internal standard RS-232 load. A logic high input on the $\overline{\text{EN}}$ pin shuts down the receiver output.

7.3.4 RS-232 Status

The $\overline{\text{INVALID}}$ output goes low when RIN input is unpowered for more than 30µs. The $\overline{\text{INVALID}}$ output goes high when receiver has a valid input. The $\overline{\text{INVALID}}$ output is active when V_{CC} is powered irregardless of FORCEON and $\overline{\text{FORCEOFF}}$ inputs (see Table 7-3).

7.4 Device Functional Modes

Table 7-1, Table 7-2, and Table 7-3 show the behavior of the driver, receiver, and INVALID features under all possible relevant combinations of inputs.

Table 7-1. Function Tables Each Driver (1)

		INPUTS	OUTPUT		
DIN	FORCEON	FORCEOFF	VALID RIN RS-232 LEVEL	DOUT	DRIVER STATUS
Х	X	L	Х	Z	Powered off
L	Н	Н	X	Н	Normal operation with
Н	Н	Н	X	L	auto-power down disabled
L	L	Н	Yes	Н	Normal operation with
Н	L	Н	Yes	L	auto-power down enabled
L	L	Н	No	Z	Powered off by
Н	L	Н	No	Z	auto-power down feature

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

Table 7-2. Each Receiver (1)

	OUTPUT		
RIN	ĒN	VALID RIN RS-232 LEVEL	ROUT
L	L	Х	Н
Н	L	Х	L
X	Н	Х	Z
Open	L	No	Н

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = disconnected input or connected driver off

Table 7-3. INVALID (1)

INPUTS	OUTPUT			
RIN	FORCEON	FORCEOFF	EN	INVALID
L	X	X	X	Н
Н	X	X	X	Н
Open	X	X	X	L

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

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8 Application and Implementation

Note

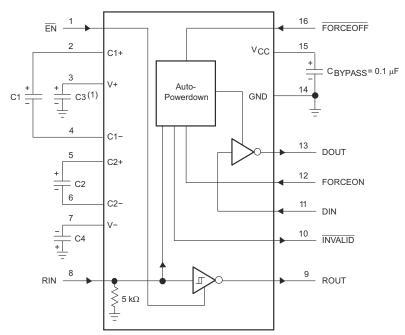
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The MAX3221E line driver and receiver is a specialized device for 3V to 5.5V RS-232 communication applications. This application is a generic implementation of this device with all required external components. For proper operation, add capacitors as shown in Figure 8-1.

8.2 Typical Application

ROUT and DIN connect to UART or general purpose logic lines. FORCEON and $\overline{FORCEOFF}$ may be connected general purpose logic lines or tied to ground or V_{CC} . $\overline{INVALID}$ may be connected to a general purpose logic line or left unconnected. RIN and DOUT lines connect to a RS-232 connector or cable. DIN, FORCEON, and $\overline{FORCEOFF}$ inputs must not be left unconnected.



(1) C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown

V_{CC} vs CAPACITOR VALUES

V _{CC}	C1	C2, C3, and C4				
3.3 V ± 0.3 V	0.1 μF	0.1 μF				
5 V ± 0.5 V	0.047 μF	0.33 μF				
3 V to 5.5 V	0.1 μF	0.47 μF				

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Figure 8-1. Typical Operating Circuit and Capacitor Values

Product Folder Links: MAX3221E

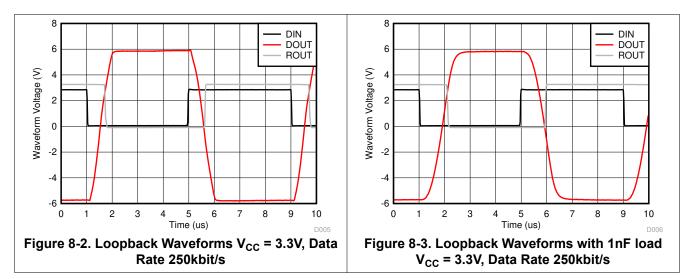
8.2.1 Design Requirements

- Recommended V_{CC} is 3.3V or 5V.
 - 3V to 5.5V is also possible
- Maximum recommended bit rate is 250kbps.
- Use capacitors as shown in Figure 8-1.

8.2.2 Detailed Design Procedure

- DIN, FORCEOFF and FORCEON inputs must be connected to valid low or high logic levels.
- · Select capacitor values based on VCC level for best performance.

8.2.3 Application Curves



8.3 Power Supply Recommendations

TI recommends a $0.1\mu\text{F}$ capacitor to filter noise on the power supply pin. For additional filter capability, a $0.01\mu\text{F}$ capacitor may be added in parallel as well. Power supply input voltage is recommended to be any valid level in Section 5.4.



8.4 Layout

8.4.1 Layout Guidelines

Keep the external capacitor traces short. This is more important on C1 and C2 nodes that have the fastest rise and fall times. Make the impedance from MAX3221E ground pin and the circuit board ground plane as low as possible for best ESD performance. Use wide metal and multiple vias on both sides of ground pin.

8.4.2 Layout Example

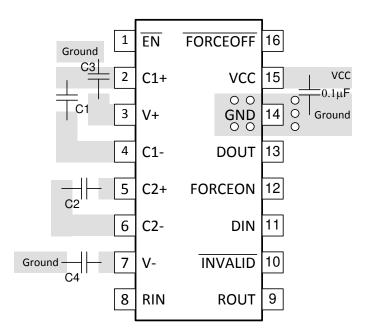


Figure 8-4. MAX3221E Layout Example

Submit Document Feedback



9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

TI E2E[™] is a trademark of Texas Instruments.

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9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (July 2024) to Revision E (December 2024)	Page
Added the SOT-23-THN (DYY) package to the data sheet	1
Added Note 2 to the ESD ratings - IEC Specifications	
Changes from Revision C (July 2021) to Revision D (July 2024)	Page
Changed the Device Information table to the Package Information table	1
Changed Pins 8 and 11 to Pins 8 and 13 in the ESD Ratings	4
Changed Pins 8 and 11 to Pins 8 and 13 in the ESD ratings - IEC Specifications	4
Changes from Revision B (March 2016) to Revision C (July 2021)	Page
Changed the Applications list	1
Added ESD ratings IEC Specifications table and added a table note for the minimum re- IEC ESD level	equirement to meet the
Changed values in the <i>Thermal Information</i> table for DB and PW packages	5

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C	changes from Revision A (May 2006) to Revision B (March 2016)	Page
•	Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and	
	Implementation section, Power Supply Recommendations section, Layout section, Device and	
	Documentation Support section, and Mechanical, Packaging, and Orderable Information section	<u>1</u>
•	Deleted Ordering Information table; see the POA at the end of the data sheet	1
•	Changed R _{0.IA} thermal values: 82 to 92 for DB package and 108 to 100.3 for PW Package	5

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: MAX3221E

www.ti.com 7-Oct-2025

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
MAX3221ECDBR	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	(4) NIPDAU	(5) Level-1-260C-UNLIM	0 to 70	MP221EC
MAX3221ECDBR.A	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MP221EC
MAX3221ECDBR:A	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MP221EC
MAX3221ECDBRG4 MAX3221ECPWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	0 to 70	MP221EC
			` , ,	·		·			
MAX3221ECPWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MP221EC
MAX3221ECPWRG4	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP221EC
MAX3221ECPWRG4.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP221EC
MAX3221EIDBR	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP221EI
MAX3221EIDBR.A	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP221EI
MAX3221EIDBRG4	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP221EI
MAX3221EIDYYR	Active	Production	SOT-23-THIN (DYY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP221EI
MAX3221EIDYYR.A	Active	Production	SOT-23-THIN (DYY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP221EI
MAX3221EIPW	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-40 to 85	MP221EI
MAX3221EIPWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	MP221EI
MAX3221EIPWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP221EI
MAX3221EIPWRG4	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP221EI
MAX3221EIPWRG4.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP221EI

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



PACKAGE OPTION ADDENDUM

www.ti.com 7-Oct-2025

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION



TAPE DIMENSIONS + K0 - P1 - B0 W Cavity - A0 -

A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX3221ECDBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
MAX3221ECPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MAX3221ECPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MAX3221EIDBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
MAX3221EIDYYR	SOT-23- THIN	DYY	16	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
MAX3221EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MAX3221EIPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1



www.ti.com 24-Jul-2025



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MAX3221ECDBR	SSOP	DB	16	2000	353.0	353.0	32.0
MAX3221ECPWR	TSSOP	PW	16	2000	353.0	353.0	32.0
MAX3221ECPWRG4	TSSOP	PW	16	2000	353.0	353.0	32.0
MAX3221EIDBR	SSOP	DB	16	2000	353.0	353.0	32.0
MAX3221EIDYYR	SOT-23-THIN	DYY	16	3000	336.6	336.6	31.8
MAX3221EIPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
MAX3221EIPWRG4	TSSOP	PW	16	2000	353.0	353.0	32.0





NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-150.





NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



PLASTIC SMALL OUTLINE



NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- 5. Reference JEDEC Registration MO-345, Variation AA



PLASTIC SMALL OUTLINE



NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



PLASTIC SMALL OUTLINE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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