LSF0108 Channel Auto-Bidirectional Multi-Voltage Level Translator for Open-Drain and Push-Pull Applications

1 Features

- Provides bidirectional voltage translation with no direction pin
- Supports up to 100-MHz up translation and greater than 100-MHz down translation at ≤ 30 pF capacitive load and up To 40-MHz up or down translation at 50 pF capacitive load
- Allows bidirectional voltage-level translation between
  - 0.65 V ↔ 1.8/2.5/3.3/5 V
  - 0.95 V ↔ 1.8/2.5/3.3/5 V
  - 1.2 V ↔ 1.8/2.5/3.3/5 V
  - 1.8 V ↔ 2.5/3.3/5 V
  - 2.5 V ↔ 3.3/5 V
  - 3.3 V ↔ 5 V
- Low standby current
- 5-V tolerance I/O port to support TTL
- Low R_{ON} provides less signal distortion
- High-impedance I/O pins for EN = Low
- Flow-through pinout for easy PCB trace routing
- Latch-up performance >100 mA per JESD 17
- –40°C to 125°C operating temperature range

2 Applications

- GPIO, MDIO, PMBus, SMBus, SDIO, UART, I^2C, and other interfaces in telecom infrastructure
- Enterprise systems
- Communications equipment
- Personal electronics
- Industrial applications

3 Description

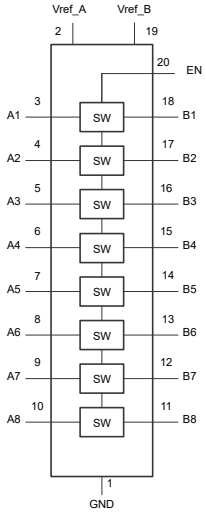
The LSF family of devices supports bidirectional voltage translation without the need for DIR pin which minimizes system effort (for PMBus, I^2C, SMBus, and so forth). The LSF family of devices supports up to 100-MHz up translation and greater than 100-MHz down translation at ≤ 30 pF capacitive load and up to 40-MHz up or down translation at 50 pF capacitive load which allows the LSF family to support more consumer or telecom interfaces (MDIO or SDIO).

LSF family supports 5-V tolerance on I/O port which makes it compatible with TTL levels in industrial and telecom applications. The LSF family is able to set up different voltage translation levels on each channel which makes it very flexible.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
LSF0108	RKS (VQFN, 20)	4.50 mm × 2.50 mm
	PW (TSSOP, 20)	4.40 mm × 6.50 mm
	DGS (VSSOP, 20)	3.00 mm × 5.10 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Functional Block Diagram

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision L (November 2022) to Revision M (May 2023)	Page
• Removed the *LSF0101* and *LSF0102* device from the data sheet	1
• Added 0.65 V voltage range capability to the *Features* section and throughout data sheet	1
• Changed the input-output and reference voltage in the *Recommended Operating Conditions* section	5
• Changed *Thermal Information* section	6
• Updated on-state resistance with 0.65 V specifications in the *Electrical Characteristics* section	6
• Changed all *Switching Characteristics* test conditions	7
• Moved formula to Up Translation in the *Up and Down Translation* sections	12
• Changed *pull up resistor* to *bias resistor* in *Enable, Disable, and Reference Voltage Guidelines* section	14

Changes from Revision K (May 2021) to Revision L (November 2022)	Page
• Updated the *Applications* section	1
• Updated the *Description* section	1
• Updated the *Pin Configuration and Functions* section	4
• Added DDF and DGS packages.	4
• Changed *Thermal Information* section	6
• Updated *Electrical Characteristics* section	6
• Updated the *Functional Block Diagram* section	10
• Updated the *Auto Bidirectional Voltage Translation* section	10
• Updated the *Output Enable* section	11
• Updated the *Device Functional Modes* section	11
• Added the *Up and Down Translation* section	12
• Updated the *Application Information* section	13
• Updated the *Enable, Disable, and Reference Voltage Guidelines* section	14
• Added the *Bias Circuitry* section	14
• Added the *Single Supply Translation* section	17

Changes from Revision J (April 2020) to Revision K (May 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1

- Updated the *Bidirectional Translation* section to include inclusive terminology 15

Changes from Revision I (June 2019) to Revision J (April 2020) **Page**

- Added section *Voltage Translation for Vref_B < Vref_A + 0.8 V* 19

Changes from Revision H (June 2019) to Revision I (July 2019) **Page**

- Changed product status from Advance Information mix to Production Data 1
- Deleted Advance Information note from the DTQ package in the Device Information table. 1
- Deleted Advance Information note from DTQ Package, in the Pin Configuration and Functions section. 4
- Deleted Advance Information note for the DTQ package in the Thermal Information table 6

Changes from Revision G (February 2016) to Revision H (June 2019) **Page**

- Added Advance Information note to Device Information table for DTQ package 1
- Added DTQ6 pinout drawing to *Pin Configurations and Functions* section (Advance Information) 4
- Added Advance Information note to LSF0101 Thermal Information table 6
- General improvements to Application and Implementation section for clarity. 13

Changes from Revision F (October 2015) to Revision G (October 2015) **Page**

- Added all available package dimensions in Device Information and changed the pin diagram description 1

Changes from Revision E (July 2015) to Revision F (October 2015) **Page**

- Changed Features from "Supports High Speed Translation, Greater Than 100 MHz" to "Supports Up to 100 MHz Up Translation and Greater Than 100 MHz Down Translation at ≤ 30pF Cap Load and Up To 40 MHz Up/Down Translation at 50 pF Cap Load." 1
- Updated all propagation delay tables changed from generic to specific LSF devices 7

Changes from Revision D (October 2014) to Revision E (July 2015) **Page**

- Deleted "Less Than 1.5 ns Max Propagation Delay" from Features. 1
- Updated ESD Ratings table 5
- Increased MAX value for TA, Operating free-air temperature, from 85°C to 125°C 5
- Updated the *Device Functional Modes* section 11
- Updated the *Pull-Up Resistor Sizing* section 15

Changes from Revision C (May 2014) to Revision D (August 2014) **Page**

- Changed bidirectional voltage level translation from 1.0 to 0.95 1
- Changed YZT package to fix view error 1
- Changed YZT Package, to fix view error. 4
- Added Vref_A footnote 14

Changes from Revision B (May 2014) to Revision C (May 2014) **Page**

- Changed LSF0108 status from preview to production 1
- Updated document title. 1
- Updated Handling Ratings table 5

Changes from Revision A (January 2014) to Revision B (February 2014) **Page**

- Added LSF0108 to data sheet 1

Changes from Revision * (December 2013) to Revision A (January 2014) **Page**

- Updated part number 1
- Updated *Electrical Characteristics* section 6

5 Pin Configuration and Functions

Pinout drawings are not to scale

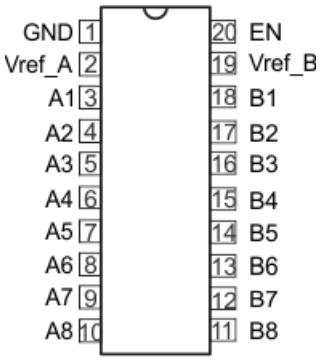


Figure 5-1. LSF0108 PW or DGS Package, 20-Pin TSSOP or VSSOP (Top View)

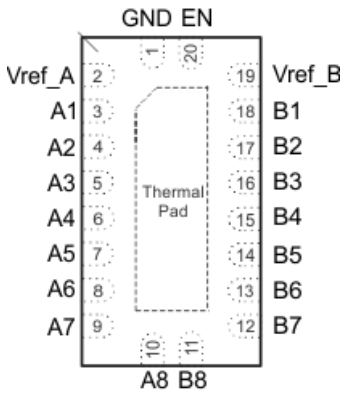


Figure 5-2. LSF0108 RKS Package, 20-Pin VQFN (Transparent Top View)

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
An	3 to 10	I/O	Auto-Bidirectional Data port
Bn	18 to 11	I/O	
EN	20	I	Enable input; connect to Vref_B and pull-up through a high resistor (200 kΩ). See Using the Enable Pin with the LSF Family
GND	1	—	Ground
Vref_A	2	—	Reference supply voltage. For proper device biasing, see *Section 9* and Understanding the Bias Circuit for the LSF Family.
Vref_B	19	—	

(1) I= input, O = output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_I	Input voltage range (2)	–0.5	7	V
$V_{I/O}$	Input-output voltage range (2)	–0.5	7	V
	Continuous channel current		128	mA
I_{IK}	Input Clamp Current (V_I < 0)		–50	mA
$T_{J(Max)}$	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) *Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.*
(2) The input and input-output negative voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/ JEDEC JS-002 (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{I/O}$	Input-output voltage	A1, A2 - An, B2 - Bn	0	5.5	V
$V_{ref\_A/B/EN}$ (1)	Reference Voltage		0	5.5	V
EN-Switch(2)	Switch mode enable voltage (Switch mode enable voltage)		1.5	5.5	V
I_{PASS}	Pass switch current			64	mA
T_A	Ambient temperature		–40	125	°C

(1) To support translation, V_{REF1} supports 0.65 V to V_{REF2} - 0.6 V. V_{REF2} must be between V_{REF1} + 0.6 V to 5.5 V. See Typical Application for more information.
(2) To support switching, V_{REF1} and V_{REF2} Do not need to be connected. EN pin should use a voltage not less than 1.5V when the switch mode is to be enabled. Enabled voltage on this pin should be equal to 1.5V or I/O supply voltage, whichever is higher.

6.4 Thermal Information

THERMAL METRIC(1)		LSF0108			UNIT
		PW (TSSOP)	RKS (VQFN)	DGS (VSSOP)	
		20 PINS	20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	108.8	74.3	123	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.7	76.6	62.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61.8	46.6	77.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	10.4	13.9	8.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	61.1	46.5	77.0	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP (1)	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = -18 mA	V_{EN} = 0 V		-1.2		0	V
I_{IH}	Input leakage current	V_I = 5 V, V_O = 0 V	V_{EN} = 0 V		.001	0.5	3	µA
I_{CC}	Supply current	V_{ref_B} = V_{EN} = 5.5 V, V_{ref_A} = 4.5 V, I_O = 0, V_I = V_{CC} or GND			.002	.05	1.5	µA
$C_{I(EN)}$	Input capacitance	V_I = 3 V or 0 V				40		pF
$C_{IO(off)}$	Off capacitance	V_O = 3 V or 0 V	V_{EN} = 0 V			4	6	pF
$C_{IO(on)}$	On capacitance	V_O = 3 V or 0 V	V_{EN} = 3 V			10.5	12.5	pF
R_{ON} (2)	On-state resistance	V_I = 0 V, V_{ref_B} = 5 V(3)	I_O = 64 mA	V_{ref_A} = 1 V		5		Ω
				V_{ref_A} = 1.8 V		4		
				V_{ref_A} = 2.5 V		3		
				V_{ref_A} = 3.3 V		3		
			I_O = 20 mA	V_{ref_A} = 0.65 V		15		
			I_O = 32 mA	V_{ref_A} = 1 V		5		
				V_{ref_A} = 1.8 V		4		
				V_{ref_A} = 2.5 V		3		
				V_{ref_A} = 3.3 V		3		
		V_I = 1.8 V, V_{ref_B} = 5 V(3)	I_O = 15 mA	V_{ref_A} = 3.3 V		4		
		V_I = 1 V, V_{ref_B} = 3.3 V(3)	I_O = 10 mA	V_{ref_A} = 1.8 V		7		
		V_I = 0 V, V_{ref_B} = 3.3 V(3)	I_O = 10 mA	V_{ref_A} = 0.65 V		15		
				V_{ref_A} = 1 V		5		
		V_I = 0 V, V_{ref_B} = 1.8 V(3)	I_O = 10 mA	V_{ref_A} = 0.65 V		15		
				V_{ref_A} = 1 V		6		

(1) All typical values are at T_A = 25°C.
(2) Measured by the voltage drop between the A and B pins at the indicated current through the switch. Minimum ON-state resistance is determined by the lowest voltage of the two (A or B) pins.
(3) Measured in application connected current source configuration only. See Section 7

6.6 Switching Characteristics (Translating Down)

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
T_{PLH}	Low-to-high propagation delay	V_{CCB} = 3.3 V, V_{CCB} = V_{IH} = V_{ref_A} + 1, V_{IL} = 0, V_M = 0.5V_{ref_A} (2)	C_L = 15 pF		0.75		ns
			C_L = 30 pF		1.4		
			C_L = 50 pF		1.9		
T_{PHL}	High to low propagation delay		C_L = 15 pF		0.85		ns
			C_L = 30 pF		1.5		
			C_L = 50 pF		2		
T_{PLH}	Low-to-high propagation delay	V_{CCB} = 2.5 V, V_{CCB} = V_{IH} = V_{ref_A} + 1, V_{IL} = 0, V_M = 0.5V_{ref_A} (2)	C_L = 15 pF		0.8		ns
			C_L = 30 pF		1.45		
			C_L = 50 pF		2		
T_{PHL}	High to low propagation delay		C_L = 15 pF		0.9		ns
			C_L = 30 pF		1.55		
			C_L = 50 pF		2.1		

(1) Specified by simulation, not tested in production
(2) Translating Down: the high-voltage side driving toward the low-voltage side. See Fig 7.2 *Direct Propagation Measurement*

6.7 Switching Characteristics (Translating Up)

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
T_{PLH}	Low-to-high propagation delay	V_{CCB} = 3.3 V, V_{CCB} = V_T = V_{ref_A} + 1, V_{ref_A} = V_{IH}, V_{IL} = 0, V_M = 0.5V_{ref_A} and R_L = 300 Ω(2)	C_L = 15 pF		0.9		ns
			C_L = 30 pF		1.55		
			C_L = 50 pF		2.1		
T_{PHL}	High to low propagation delay		C_L = 15 pF		1		ns
			C_L = 30 pF		1.65		
			C_L = 50 pF		2.2		
T_{PLH}	Low-to-high propagation delay	V_{CCB} = 2.5 V, V_{CCB} = V_T = V_{ref_A} + 1, V_{ref_A} = V_{IH}, V_{IL} = 0, V_M = 0.5V_{ref_A} and R_L = 300 Ω(2)	C_L = 15 pF		0.8		ns
			C_L = 30 pF		1.35		
			C_L = 50 pF		1.8		
T_{PHL}	High to low propagation delay		C_L = 15 pF		0.9		ns
			C_L = 30 pF		1.45		
			C_L = 50 pF		1.9		

(1) Specified by simulation, not tested in production
(2) Translating up: the low-voltage side driving toward the high-voltage side. See Fig 7.2 *Direct Propagation Measurement*

6.8 Typical Characteristics

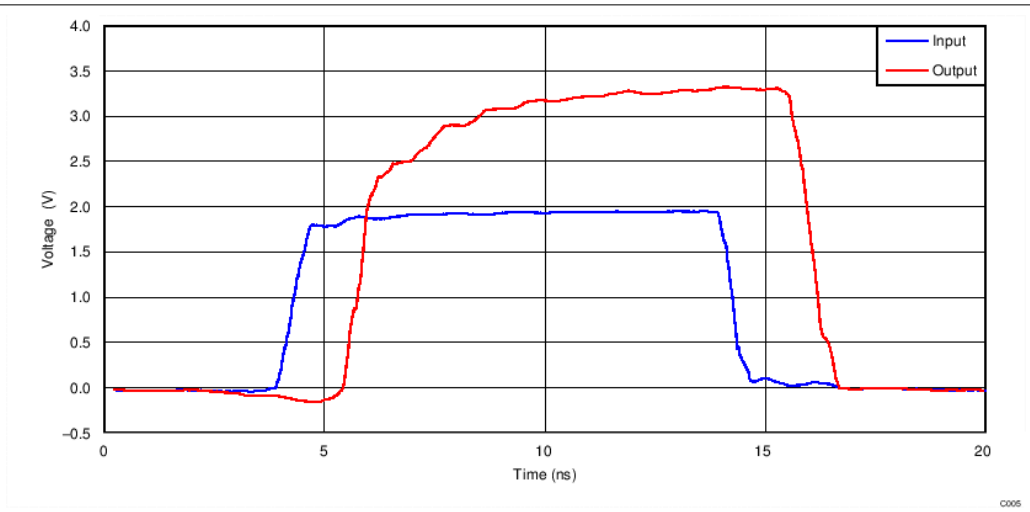
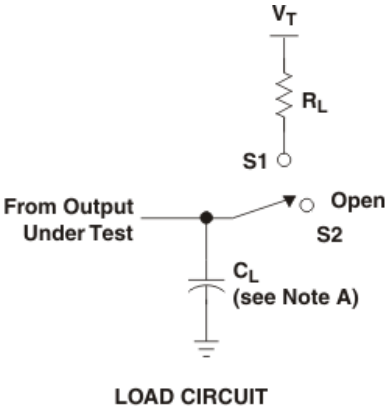


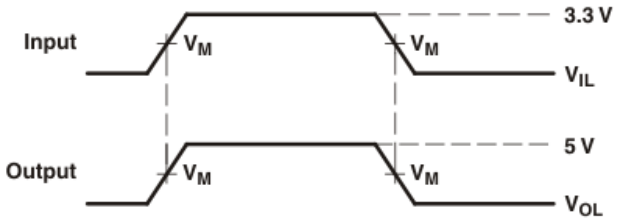
Figure 6-1. Signal Integrity (1.8 to 3.3 V Up Translation at 50 MHz)

7 Parameter Measurement Information

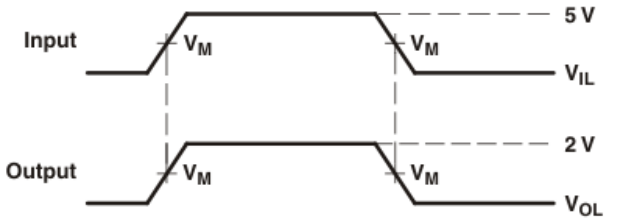


LOAD CIRCUIT

USAGE	SWITCH
Translating up	S1
Translating down	S2



TRANSLATING UP



TRANSLATING DOWN

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
C. The outputs are measured one at a time, with one transition per measurement.

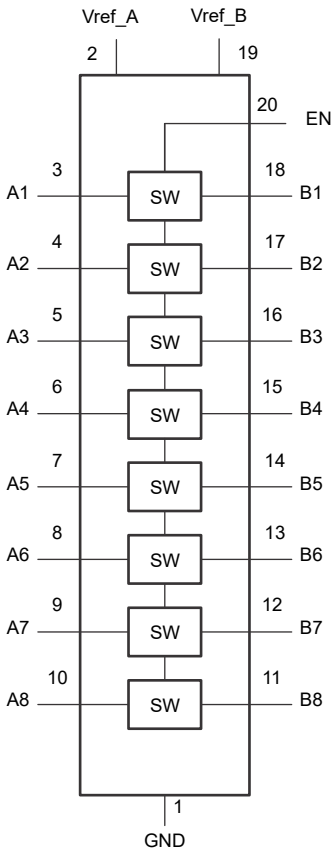
Figure 7-1. Load Circuit for Outputs

8 Detailed Description

8.1 Overview

The LSF family can be used in level-translation applications for interfacing devices or systems operating with one another that operate at different interface voltages. The LSF family is ideal for use in applications where an open-drain driver is connected to the data I/Os. With appropriate pull-up resistors and layout, LSF can achieve 100 MHz. The LSF family can also be used in applications where a push-pull driver is connected to the data I/Os. For an overview of device setup and operation, see *The Logic Minute* training series on *Understanding the LSF Family of Bidirectional, Multi-Voltage Level Translators*.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Auto Bidirectional Voltage Translation

The LSF0108 device is an auto bidirectional voltage level translator that is operational from 0.95 to 5.5 V on V_{ref_A} and 1.8 to 5.5 V on V_{ref_B}. This allows bidirectional voltage translation between 0.95 V and 5.5 V without the need for a direction pin in open-drain or push-pull applications. The LSF family supports level translation applications with transmission speeds greater than 100 Mbps for open-drain systems using a 30-pF capacitance and 250-Ω pullup resistor. Both the output driver of the controller and the peripheral device output can be push-pull or open-drain (pull-up resistors may be required). In both up and down translation, the B-side is often referred to as the high side and refers to devices connected to the B ports. The A-side can be referred to as the low side.

8.3.2 Output Enable

To enable the I/O pins, the EN input should be tied directly to V_{ref_B} during operation and both pins must be pulled up to the HIGH side (V_{CCB}) through a bias resistor (typically 200 kΩ). To ensure the high impedance state during power-up, power-down, or during operation, the EN pin must be LOW. The EN pin should always be tied directly to the V_{ref_B} pin and is recommended to be disabled by an open-drain driver without a pullup resistor. This allows V_{ref_B} to regulate the EN input and bias the channels for proper translation. A filter capacitor on V_{ref_B} is recommended for a stable supply at the device.

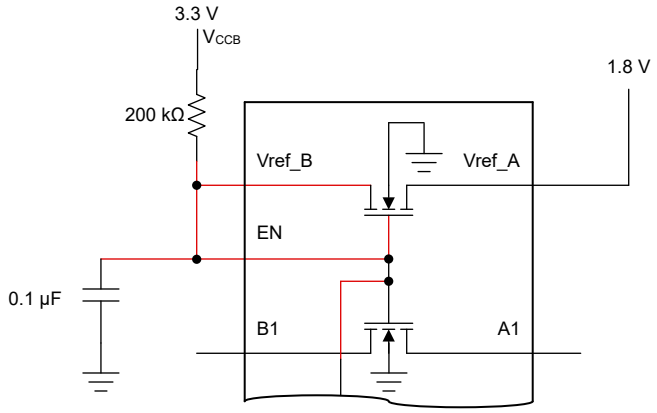


Figure 8-1. Enable Pin Tied to V_{ref_B} Directly and to V_{CCB} Through a Bias Resistor

The supply voltage of open drain I/O devices can be completely different from the supplies used for the LSF and has no impact on the operation. For additional details on how to use the enable pin, see the *Using the Enable Pin with the LSF Family video.*

Table 8-1. Enable Pin Function Table

INPUT EN(1) PIN	Data Port State
Tied directly to V_{ref_B}	An = Bn
L	Hi-Z

(1) EN is controlled by V_{ref_B} logic levels.

8.4 Device Functional Modes

For each channel (n), when either the An or Bn port is LOW, the switch provides a low impedance path between the An and Bn ports; the corresponding Bn or An port will be pulled LOW. The low R_{ON} of the switch allows connections to be made with minimal propagation delay and signal distortion.

Table 8-1 provides a summary of device operation. For additional details on the functional operation of the LSF family of devices, see the *Down Translation with the LSF Family* and *Up Translation with the LSF Family* videos.

Table 8-2. Device Functionality

Signal Direction(1)	Input State	Switch State	Functionality
B to A (Down Translation)	B = LOW	ON (Low Impedance)	A-side voltage is pulled low through the switch to the B-side voltage
	B = HIGH	OFF (High Impedance)	A-side voltage is clamped at V_{ref_A} (2)
A to B (Up Translation)	A = LOW	ON (Low Impedance)	B-side voltage is pulled low through the switch to the A-side voltage
	A = HIGH	OFF (High Impedance)	B-side voltage is clamped at V_{ref_A} and then pulled up to the V_{PU} supply voltage

(1) The downstream channel should not be actively driven through a low impedance driver, or else bus contention may occur.
(2) The A-side can have a pullup to V_{ref_A} for additional current drive capability or may also be pulled above V_{ref_A} with a pullup resistor. Specifications in the *Recommended Operating Conditions* section should always be followed.

8.4.1 Up and Down Translation

8.4.1.1 Up Translation

When the signal is being driven from A to B and the An port is HIGH, the switch will be OFF and the Bn port will then be driven to a voltage higher than V_{ref_A} by the pull-up resistor that is connected to the pull-up supply voltage (V_{PU}). This functionality allows seamless translation between higher and lower voltages selected by the user, without the need for directional control. Pull-up resistors are always required on the high side, and pull-ups are only required on the low side, if the low side of the device's output is open drain or its input has a leakage greater than 1 µA.

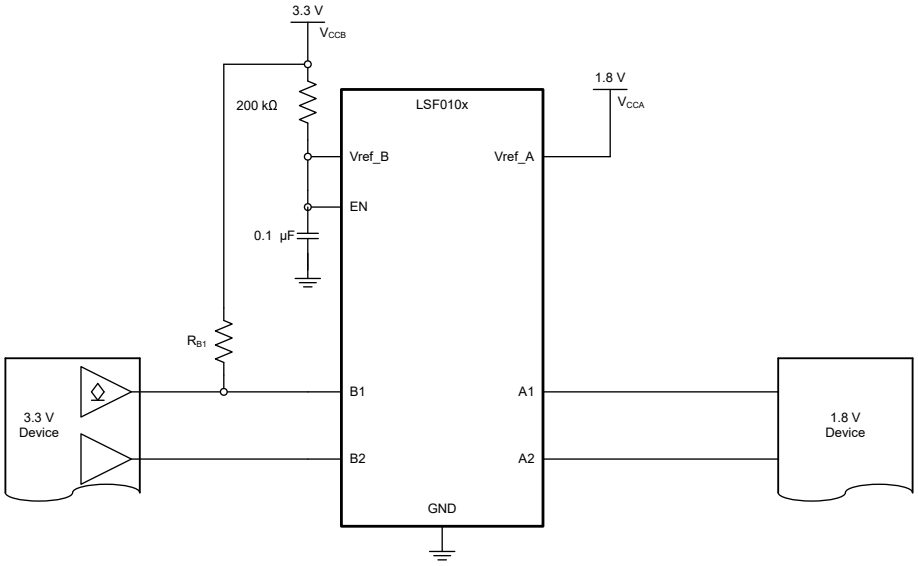


Figure 8-2. Up Translation Example Schematic with Push-Pull and Open Drain Configuration

Up translation with the LSF requires attention to two important factors: maximum data rate and sink current. Maximum data rate is directly related to the rising edge of the output signal. Sink current depends on supply values and the chosen pull-up resistor values. Equation 1 shows the maximum data rate formula and Equation 2 shows the maximum sink current formula, both of which are estimations. A low RC value is needed to reach high speeds, which also require strong drivers. Please see the *Up Translation with the LSF Family* video for estimated data rate and sink current calculations based on circuit components.

$$\frac{1}{3 \times 2R_{B1}C_{B1}} = \frac{1}{6R_{B1}C_{B1}}\left(\frac{bits}{second}\right) \quad (1)$$

$$I_{OL} \cong \frac{V_{CCA}}{R_{A1}} + \frac{V_{CCB}}{R_{B1}}\left(A\right) \quad (2)$$

8.4.1.2 Down Translation

When the signal is being driven HIGH from the Bn port to An port, the switch will be OFF, clamping the voltage on the An port to the voltage set by V_{ref_A}. A pull-up resistor can be added on either side of the device. There are special circumstances that allow the removal of one or both of the pull-up resistors. If the signal is always going to be down translated from a push-pull transmitter, then the resistor on the B-side can be removed. If the leakage current into the receiver on the A-side is less than 1 µA, then the resistor on the A-side can also be removed. This arrangement with no external pull-up resistors can be used when down translating from a push-pull output to a low-leakage input. For an open drain transmitter, the pull-up resistor on the B-side is necessary because an open drain output can't drive high by itself. For a summary of device operation, refer to Section 8.4. For additional details on the functional operation of the LSF family of devices, see the *Up Translation with the LSF Family* and *Down Translation with the LSF Family* videos.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The LSF devices can perform voltage translation for open-drain or push-pull interfaces. Table 9-1 provides common interfaces and the corresponding device recommendation from the LSF family which supports the corresponding bit count.

Table 9-1. Voltage Translator for Common Interfaces

Part Name	Channel Number	Interface
LSF0108	8	GPIO, MDIO, SDIO, SVID, UART, SMBus, PMBus, I^2C, and SPI

Some important reminders regarding the LSF family of devices are as follows:

- LSF devices are switch-based, not buffer-based (for more information, see the TXB family for buffer-based devices).
- Specific data rates cannot be calculated by using 1/Tpd.
- V_{CCB}/V_{CCA} are not the same as V_{ref_B} or V_{ref_A}: V_{CCB} refers to the B-side supply voltage supplied to the LSF device, while V_{ref_B} refers to the voltage at the V_{ref_B} pin (pin 7 of Figure 9-1) on the other side of the 200k resistor.

9.2 Typical Applications

9.2.1 Open-Drain Interface (I^2C, PMBus, SMBus, and GPIO)

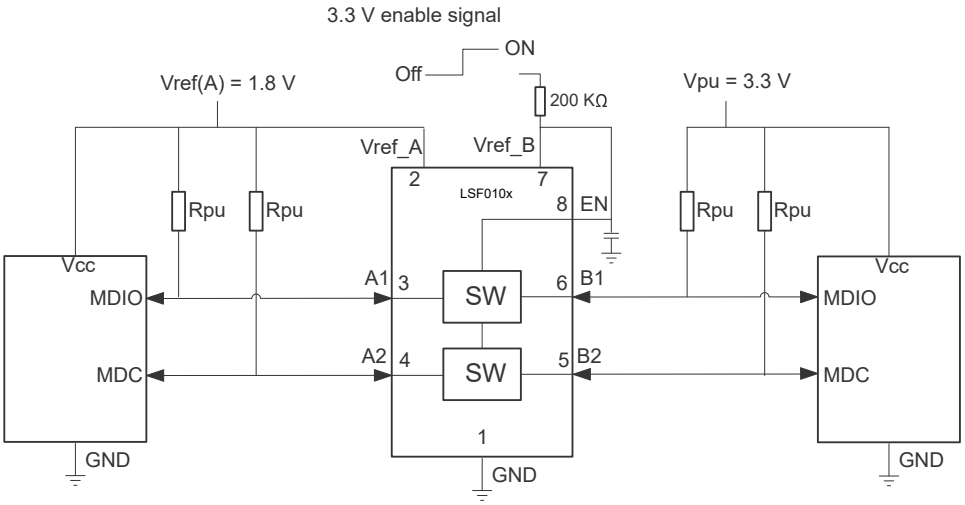


Figure 9-1. Typical Application Circuit for Open-Drain Translation (MDIO Shown as an Example)

9.2.1.1 Design Requirements

9.2.1.1.1 Enable, Disable, and Reference Voltage Guidelines

In the previous figure, V_{ref_B} is connected through a 200-kΩ resistor to a 3.3 V power supply and V_{ref_A} is set to 1.8 V. The A1 and A2 channels have a maximum output voltage equal to V_{ref_A} and the B1 and B2 channels have has a maximum output voltage equal to V_{PU}.

The LSF family has an EN input that is used to disable the device by setting EN LOW, placing all I/Os in the high-impedance state. Since the LSF family of devices are switch-type voltage translators, the power consumption is very low. TI recommends always enabling the LSF family for bidirectional applications (I^2C, SMBus, PMBus, or MDIO).

Table 9-2. Application Operating Condition

PARAMETER		MIN	TYP	MAX	UNIT
V_{ref_A} (1)	reference voltage (A)	0.65		5.5	V
V_{ref_B}	reference voltage (B)	V_{ref_A} + 0.8		5.5	V
$V_{I(EN)}$	input voltage on EN pin	V_{ref_A} + 0.8		5.5	V
V_{PU}	pull-up supply voltage	0		V_{ref_B}	V

(1) V_{ref_A} is required to be the lowest voltage level across all inputs and outputs.

Note

The 200 kΩ, bias resistor is required to allow V_{ref_B} to regulate the EN input and properly bias the device for translation.

9.2.1.1.2 Bias Circuitry

For proper operation, V_{CCA} must always be at least 0.8 V less than V_{CCB} (V_{CCA} + 0.8 ≦ V_{CCB}). The 200 kΩ bias resistor is required to allow V_{ref_B} to regulate the EN input and properly bias the device for translation. A 0.1 µF capacitor is recommended for providing a path from V_{ref_B} to ground for high frequency noise. V_{ref_B} and $V_{I(EN)}$ are recommended to be 1.0 V higher than V_{ref_A} for best signal integrity.

Attempting to drive the EN pin directly with a push-pull output device is a very common design error with the LSF0108 series of devices. It is also very important to note that current does flow into the A-side voltage supply during normal operation. Not all voltage sources can sink current, so be sure that applicable designs can handle this current. For more design details, see the *Understanding the Bias Circuit for the LSF Family* video.

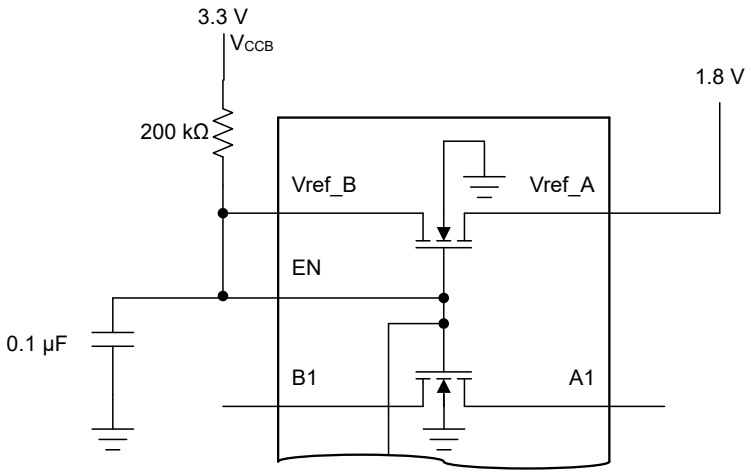


Figure 9-2. Bias Circuitry Inside the LSF010x-Q1 Device

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Bidirectional Translation

For the bidirectional translation configuration (higher voltage to lower voltage or lower voltage to higher voltage), the EN input must be connected to V_{ref_B} and both pins must be pulled up to the HIGH side V_{CCB} through a bias resistor (typically 200 kΩ). This allows V_{ref_B} to regulate the EN input and bias the channels for proper translation. A filter capacitor on V_{ref_B} is recommended for a stable supply at the device. The controller output driver can be push-pull or open-drain (pull-up resistors may be required) and the peripheral device output can be push-pull or open-drain (pull-up resistors are required to pull the Bn outputs to V_{PU}).

Note

If either output is push-pull, data must be unidirectional or the outputs must be tri-state and be controlled by some direction-control mechanism to prevent HIGH-to-LOW bus contention in either direction. If both outputs are open-drain, no direction control is needed.

9.2.1.2.2 Pull-Up Resistor Sizing

The pull-up resistor value needs to limit the current through the pass transistor when it is in the ON state to about 15 mA. This ensures a voltage drop of 260 mV to 350 mV to have a valid LOW signal on the downstream channel. If the current through the pass transistor is higher than 15 mA, the voltage drop is also higher in the ON state. To set the current through each pass transistor at 15 mA, calculate the pull-up resistor value using the following equation:

$$Rpu = \frac{(\text{Vpu} - 0.35\ \text{V})}{0.015\ A} \quad (3)$$

Table 9-3 provides resistor values, reference voltages, and currents at 8 mA, 5 mA, and 3 mA. The resistor value shown in the +10% column (or a larger value) should be used to ensure that the voltage drop across the transistor is 350 mV or less. The external driver must be able to sink the total current from the resistors on both sides of the LSF family device at 0.175 V, although the 15 mA applies only to current flowing through the LSF family device. The device driving the low state at 0.175 V must sink current from one or more of the pull-up resistors and maintain V_{OL}. A decrease in resistance will increase current, and thus result in increased V_{OL}.

Table 9-3. Pull-Up Resistor Values

V_{PU} (1) (2)	8 mA		5 mA		3 mA	
	NOMINAL (Ω)	+10%(3) (Ω)	NOMINAL (Ω)	+10%(3) (Ω)	NOMINAL (Ω)	+10%(3) (Ω)
5 V	581	639	930	1023	1550	1705
3.3 V	369	406	590	649	983	1082
2.5 V	269	296	430	473	717	788
1.8 V	181	199	290	319	483	532
1.5 V	144	158	230	253	383	422
1.2 V	106	117	170	187	283	312

(1) Calculated for V_{OL} = 0.35 V
(2) Assumes output driver V_{OL} = 0.175 V at stated current
(3) +10% to compensate for V_{DD} range and resistor tolerance

9.2.1.3 Application Curve

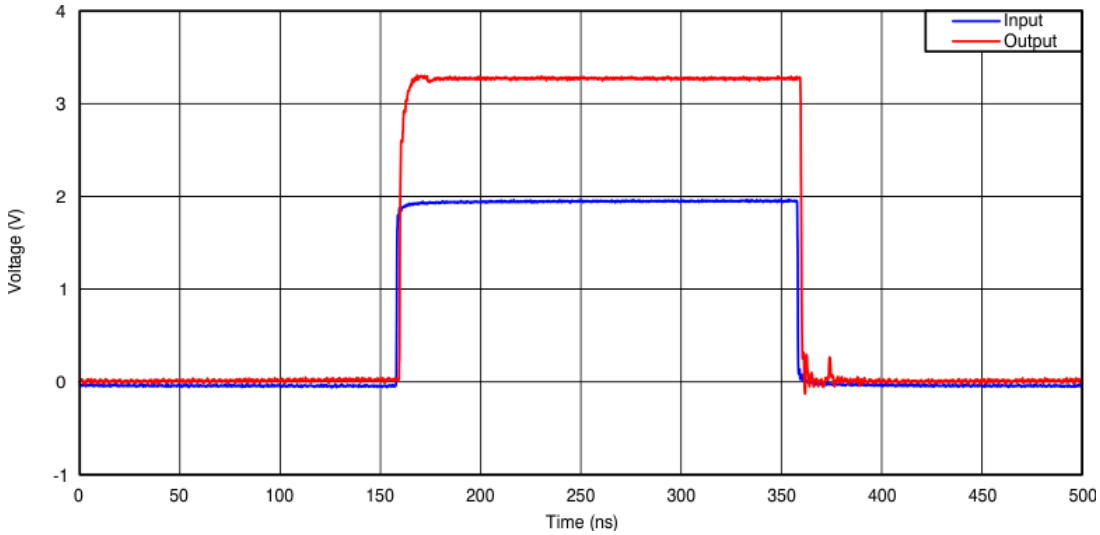


Figure 9-3. Open Drain Translation (1.8 V to 3.3 V at 2.5 MHz)

9.2.2 Mixed-Mode Voltage Translation

The supply voltage (V_{PU}) for each channel can be individually set with a pull-up resistor. Figure 9-4 shows an example of this mixed-mode multi-voltage translation. For additional details on multi-voltage translation, see the *Multi-voltage Translation with the LSF Family* video.

With the V_{ref_B} pulled up to 5 V and V_{ref_A} connected to 1.8 V, all channels will be clamped to 1.8 V at which point a pullup can be used to define the high level voltage for a given channel.

- **Push-Pull Down Translation (5 V to 1.8 V):** Channel 1 is an example of this setup. When B1 is 5 V, A1 is clamped to 1.8 V, and when B1 is LOW, A1 is driven LOW through the switch.
- **Push-Pull Up Translation (1.8 V to 5 V)**: Channel 2 is an example of this setup. When A2 is 1.8 V, the switch is high impedance and the B2 channel is pulled up to 5 V. When A2 is LOW, B2 is driven LOW through the switch.
- **Push-Pull Down Translation (3.3 V to 1.8 V):** Channels 3 and 4 are examples of this setup. When either B3 or B4 are driven to 3.3 V, A3 or A4 are clamped to 1.8 V, and when either B3 or B4 are LOW, A3 or A4 are driven LOW through the switch.
- **Open-Drain Bidirectional Translation (3.3 V ↔ 1.8 V):** Channels 5 through 8 are examples of this setup. These channels are for bidirectional operation for I^2C and MDIO to translate between 1.8 V and 3.3 V with open-drain drivers.

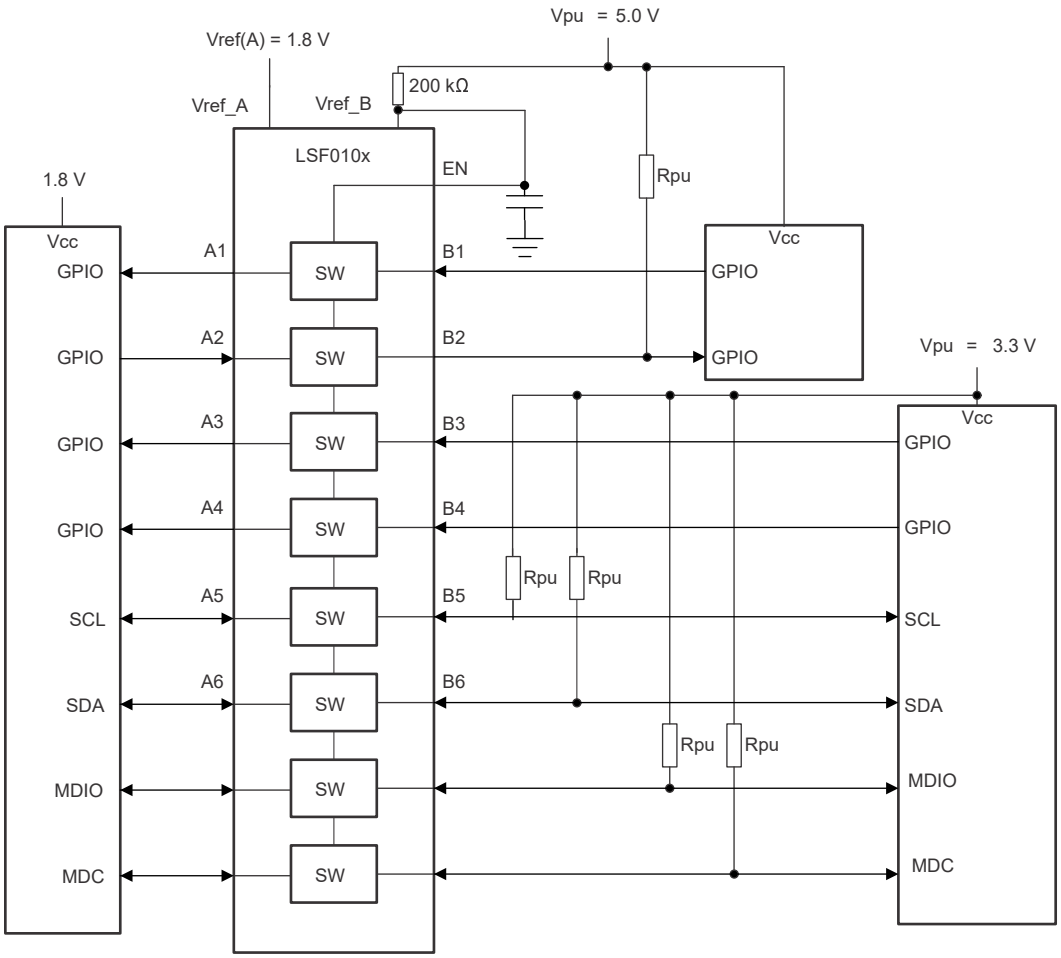


Figure 9-4. Multi-Voltage Translation with the LSF010x-Q1

9.2.3 Single Supply Translation

Sometimes, an external device will have an unknown voltage that could be above or below the desired translation voltage, preventing a normal connection of the LSF. Resistors are added on the A side in place of the second supply in this case – this is an example of when LSF single supply operation is utilized, shown in Figure 9-5. In the following figure, a single 3.3 V supply is used to translate between a 3.3 V device and a device that can change between 1.8 V and 5.0 V. R1 and R2 are added in place of the second supply. Note that due to some current coming out of the V_{ref_A} pin, this cannot be treated as a simple voltage divider.

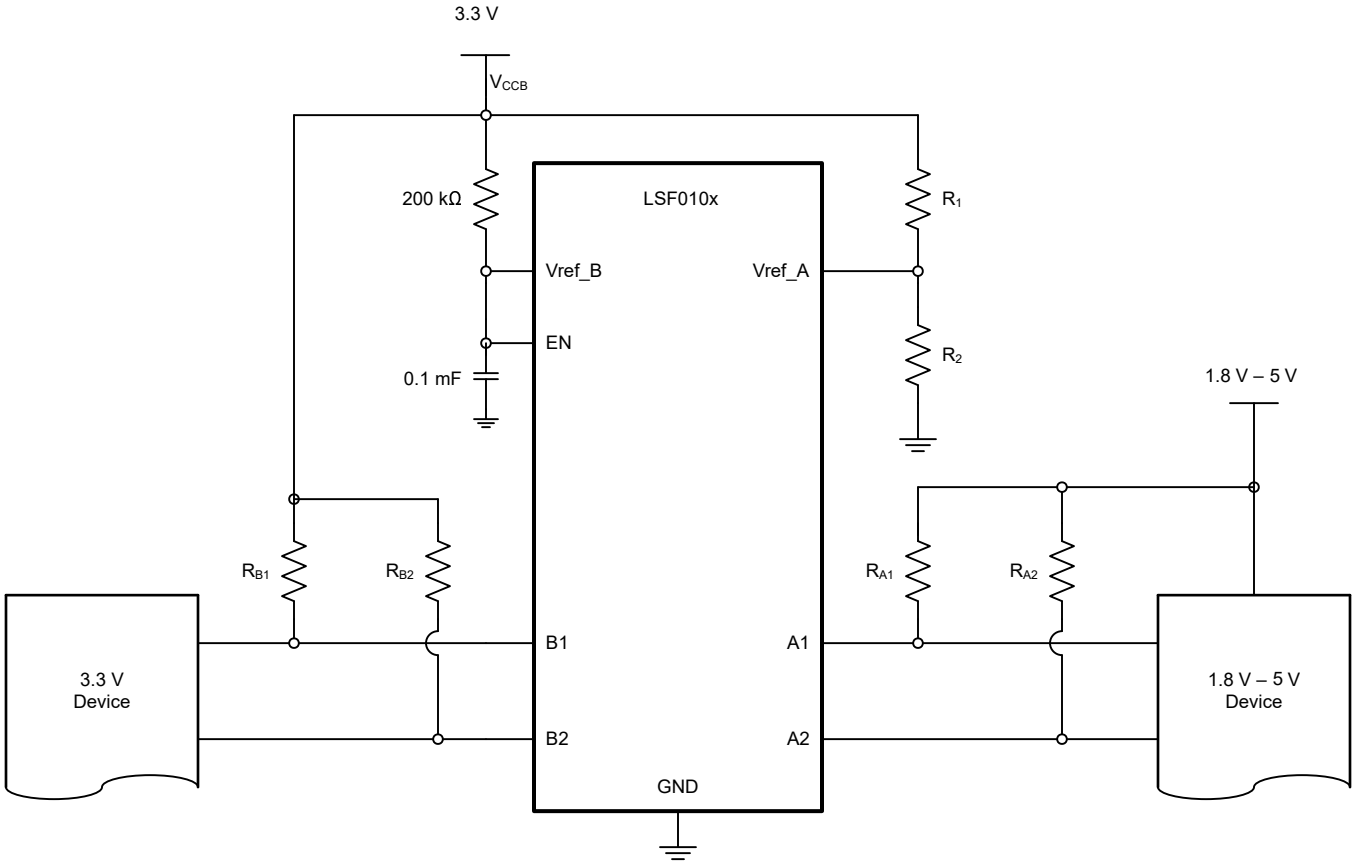


Figure 9-5. Single Supply Translation with 3.3 V Supply

The steps to select the resistor values for R1 and R2 are as follows:

1. Select a value for R1. Typically, 1 MΩ is used to reduce current consumption.
2. Plug in values for your system into the following equation. Note that V_{ref_A} is the lowest voltage in the system. V_{CCB} is the primary supply and R1 is the selected value from step 1.

$$R_2 = \frac{200\left(10^3\right) \times R_1 \times V_{REFA}}{\left(200\left(10^3\right) + R_1\right)\left(V_{CCB} - V_{REFA}\right) - 0.85 \times R_1} \quad (4)$$

The single supply used must be at least 0.8 V larger than the lowest desired translation voltage. The voltage at V_{ref_A} must be selected as the lowest voltage to be used in the system. The LSF evaluation module (LSF-EVM) contains unpopulated pads to place R1 and R2 for single supply operation testing. For an example single supply translation schematic and details, see the *Single Supply Translation with the LSF Family* video.

9.2.4 Voltage Translation for $V_{ref\_B} < V_{ref\_A} + 0.8$ V

As described in the *Enable, Disable, and Reference Voltage Guidelines* section, it is generally recommended that $V_{ref\_B} > V_{ref\_A} + 0.8$ V; however, the device can still operate in the condition where $V_{ref\_B} < V_{ref\_A} + 0.8$ V as long as additional considerations are made for the design.

Typical Operation ($V_{ref\_B} > V_{ref\_A} + 0.8$ V): in this scenario, pullup resistors are not required on the A-side for proper down-translation as is shown for channels 1 and 2 of Figure 9-4. The typical operating mode of the device ensures that when down translating from B to A, the A-side I/O ports will clamp at V_{ref_A} to provide proper voltage translation. For further explanation of device operation, see the *Down Translation with the LSF Family* video.

Requirements for $V_{ref\_B} < V_{ref\_A} + 0.8$ V Operation: in this scenario, there is not a large enough voltage difference between V_{ref_A} and V_{ref_B} to ensure that the A side I/O ports will be clamped at V_{ref_A}, but rather at a voltage approximately equal to V_{ref_B} – 0.8 V. For example, if V_{ref_B} = 1.8 V and V_{ref_A} = 1.2 V, the A-side I/Os will clamp to a voltage around 1.0 V. Therefore, to operate in such a condition, the following additional design considerations must be met:

- V_{ref_B} must be greater than V_{Ref_A} during operation ($V_{ref\_B} > V_{ref\_A}$)
- Pullup resistors should be populated on A-side I/O ports to ensure the line will be fully pulled up to the desired voltage.

Figure 9-6 shows an example of this setup, where 1.2 V ↔ 1.8 V translation is achieved with the LSF0108. This type of setup also applies for other voltage nodes such as 1.8 V ↔ 2.5 V, 1.05 V ↔ 1.5 V, and others as long as the *Recommended Operating Conditions* table is followed.

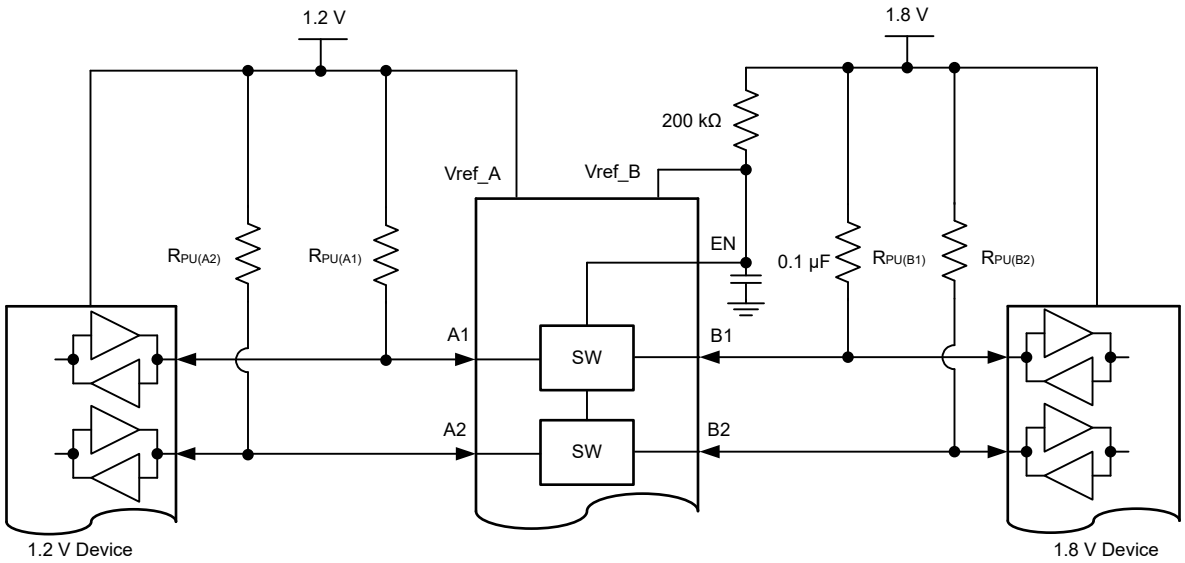


Figure 9-6. 1.2 V to 1.8 V Level Translation with LSF010x

10 Power Supply Recommendations

There are no power sequence requirements for the LSF family. Table 10-1 provides recommended operating voltages for all supply and input pins.

Table 10-1. Recommended Operating Voltages

PARAMETER		MIN	TYP	MAX	UNIT
V_{ref_A} (1)	reference voltage (A)	0.65		5.5	V
V_{ref_B}	reference voltage (B)	V_{ref_A} + 0.8		5.5	V
$V_{I(EN)}$	input voltage on EN pin	V_{ref_A} + 0.8		5.5	V
V_{PU}	pull-up supply voltage	0		V_{ref_B}	V

(1) V_{ref_A} is required to be the lowest voltage level across all inputs and outputs.

11 Layout

11.1 Layout Guidelines

Because the LSF family is a switch-type level translator, the signal integrity is highly related with a pull-up resistor and PCB capacitance condition.

- Short signal trace as possible to reduce capacitance and minimize stub from pull-up resistor.
- Place LSF device close to the high voltage side.
- Select the appropriate pull-up resistor that applies to translation levels and driving capability of the transmitter.

11.2 Layout Example

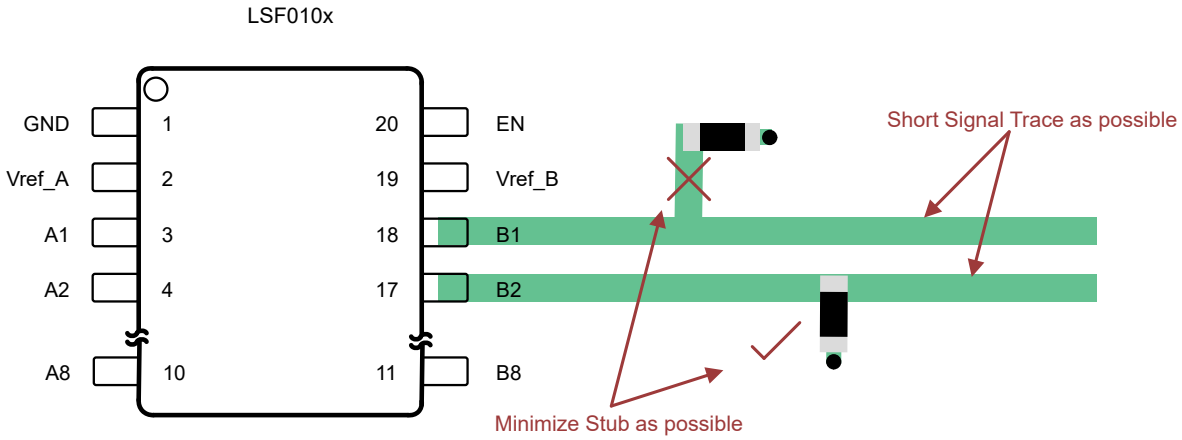


Figure 11-1. Short Trace Layout

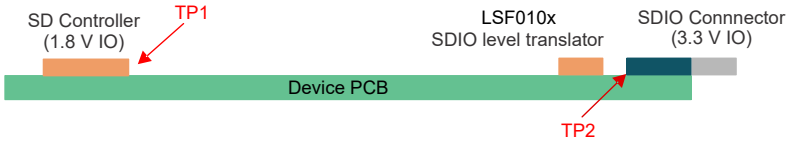


Figure 11-2. Device Placement

12 Device and Documentation Support

12.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *LSF Translator Family Evaluation Module* user's guide
- Texas Instruments, *Biasing Requirements for TXS, TXB, and LSF Auto-Bidirectional Translators* application note
- Texas Instruments, *Voltage Level Translation with the LSF Family* application note
- The Logic Minute Video Training Series on Understanding the LSF Family of Devices:
  - Texas Instruments, *Introduction - Voltage Level Translation with the LSF Family*
  - Texas Instruments, *Understanding the Bias Circuit for the LSF Family*
  - Texas Instruments, *Using the Enable Pin with the LSF Family*
  - Texas Instruments, *Translation Basics with the LSF Family*
  - Texas Instruments, *Down Translation with the LSF Family*
  - Texas Instruments, *Up Translation with the LSF Family*
  - Texas Instruments, *Multi-Voltage Translation with the LSF Family*
  - Texas Instruments, *Single Supply Translation with the LSF Family*

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LSF0108DGSR	Active	Production	VSSOP (DGS) | 20	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LSF08
LSF0108DGSR.A	Active	Production	VSSOP (DGS) | 20	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LSF08
LSF0108PWR	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LSF0108
LSF0108PWR.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LSF0108
LSF0108RKSR	Active	Production	VQFN (RKS) | 20	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	LSF0108
LSF0108RKSR.A	Active	Production	VQFN (RKS) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LSF0108

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF LSF0108 :

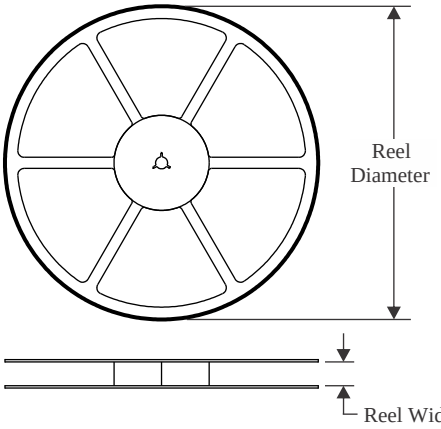
- Automotive : LSF0108-Q1

NOTE: Qualified Version Definitions:

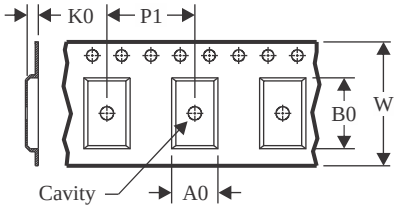
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

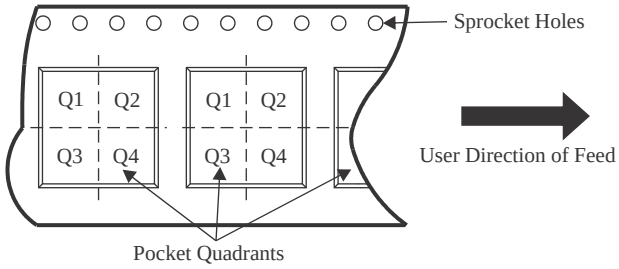


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

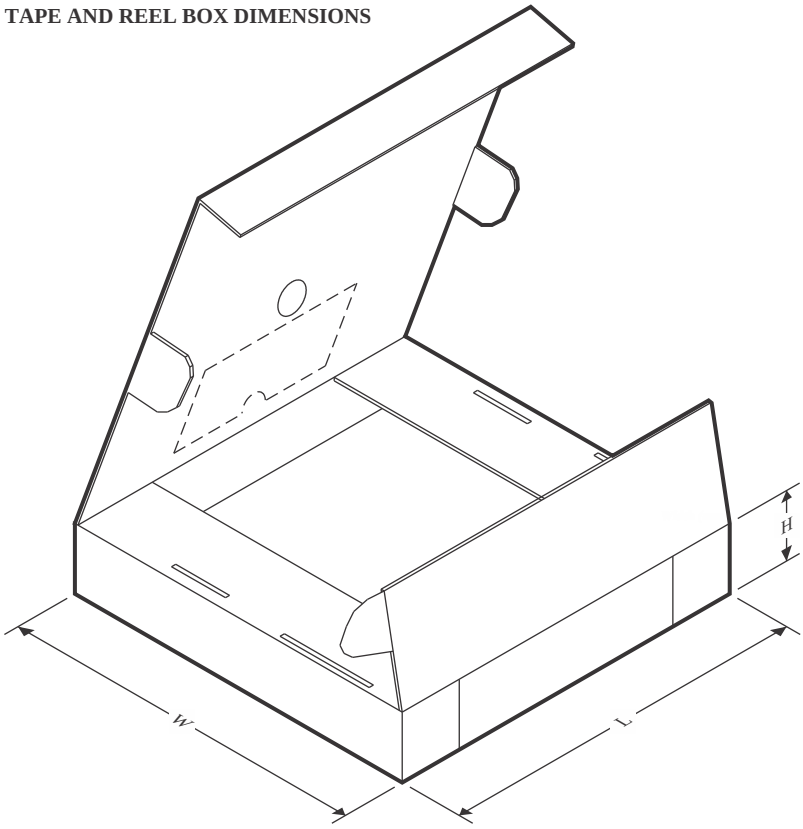
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LSF0108DGSR	VSSOP	DGS	20	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
LSF0108PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
LSF0108RKSR	VQFN	RKS	20	3000	180.0	12.5	2.8	4.8	1.2	4.0	12.0	Q1
LSF0108RKSR	VQFN	RKS	20	3000	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LSF0108DGSR	VSSOP	DGS	20	5000	356.0	356.0	35.0
LSF0108PWR	TSSOP	PW	20	2000	353.0	353.0	32.0
LSF0108RKSR	VQFN	RKS	20	3000	205.0	200.0	33.0
LSF0108RKSR	VQFN	RKS	20	3000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

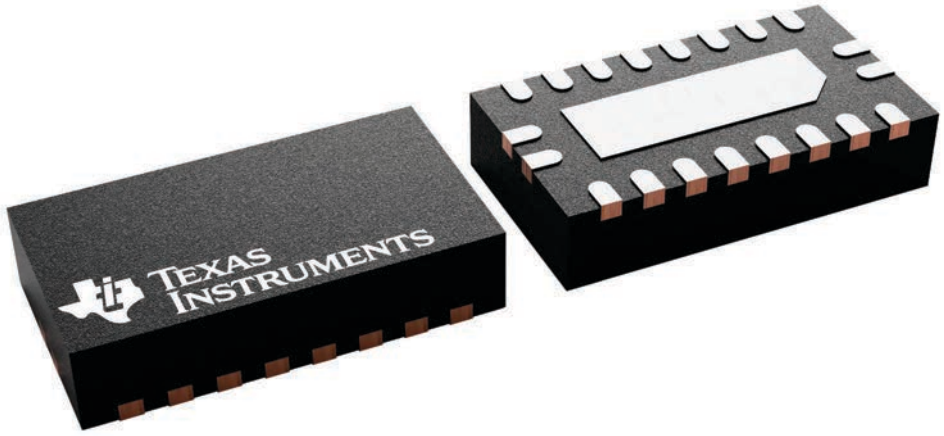
RKS 20

VQFN - 1 mm max height

2.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

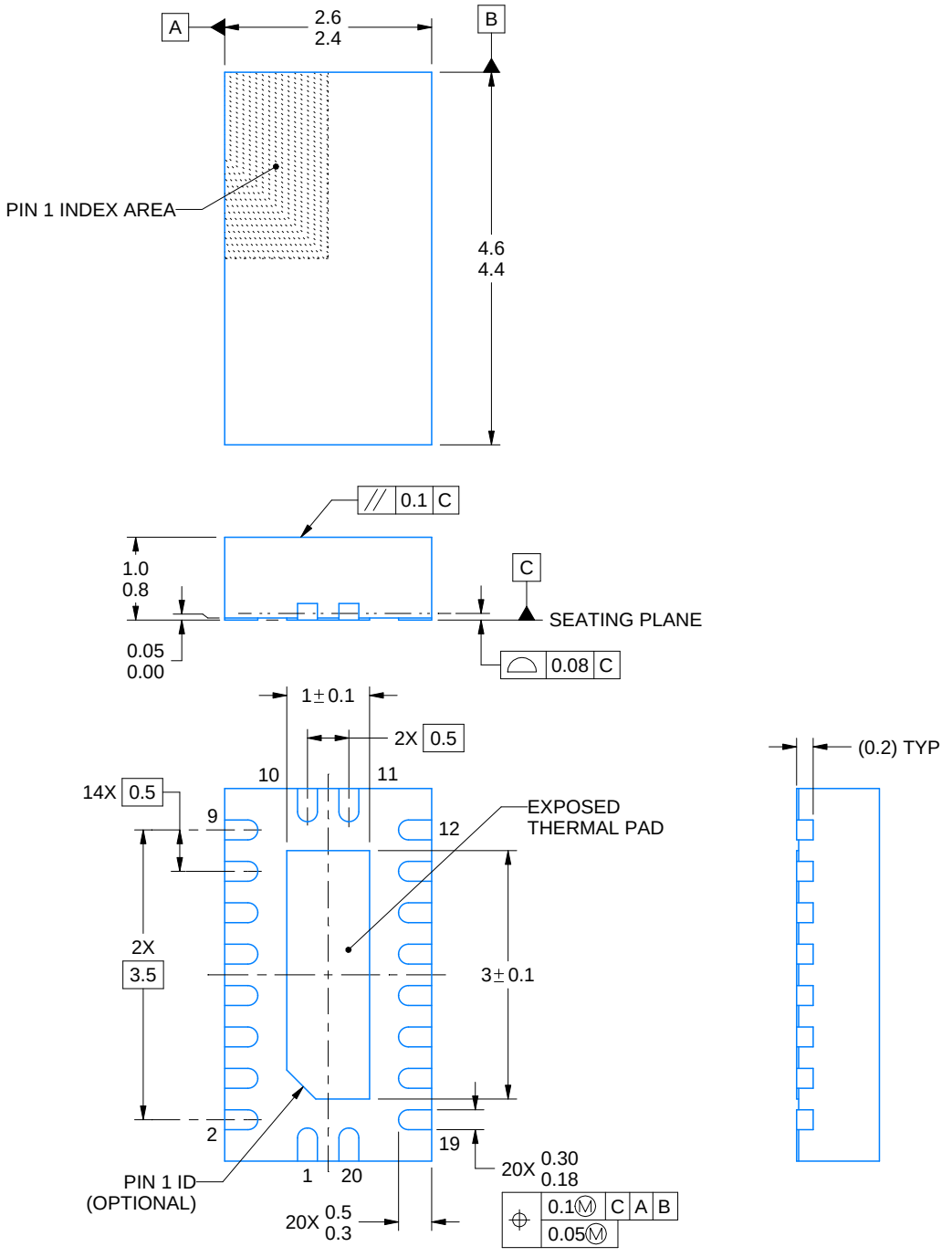


PACKAGE OUTLINE

RKS0020A

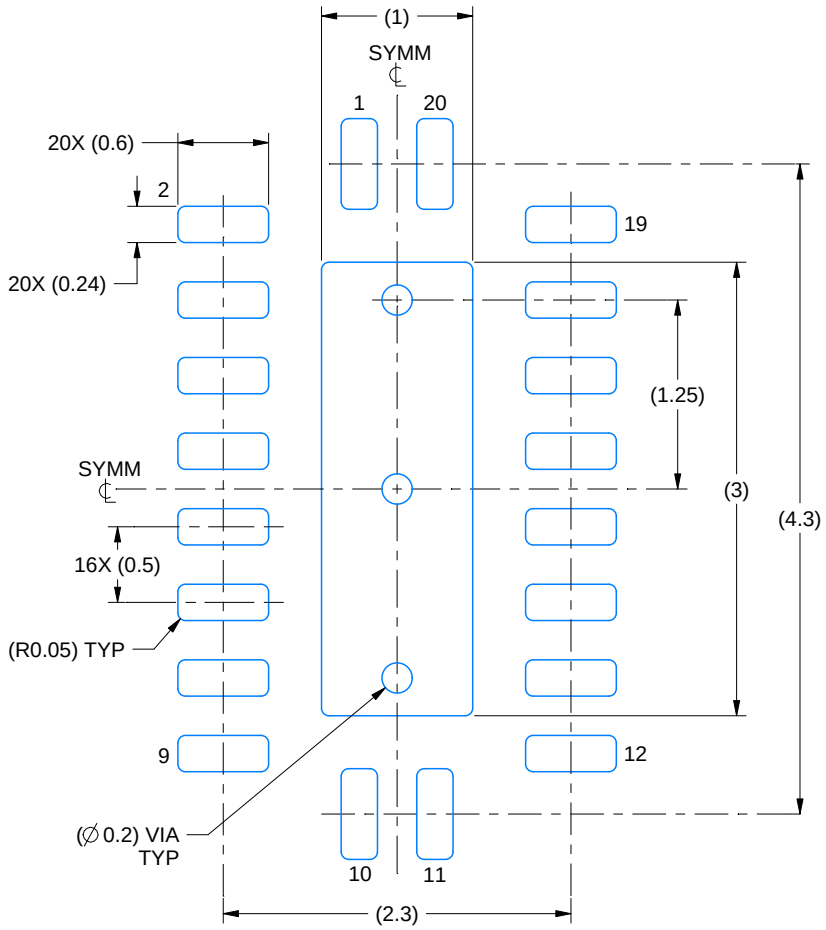
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

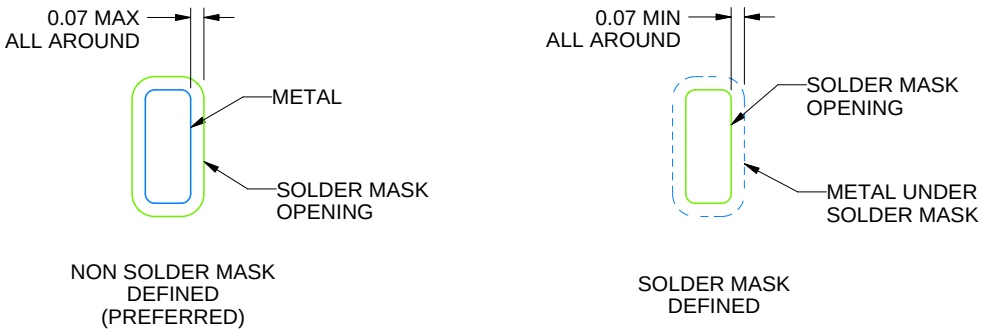


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

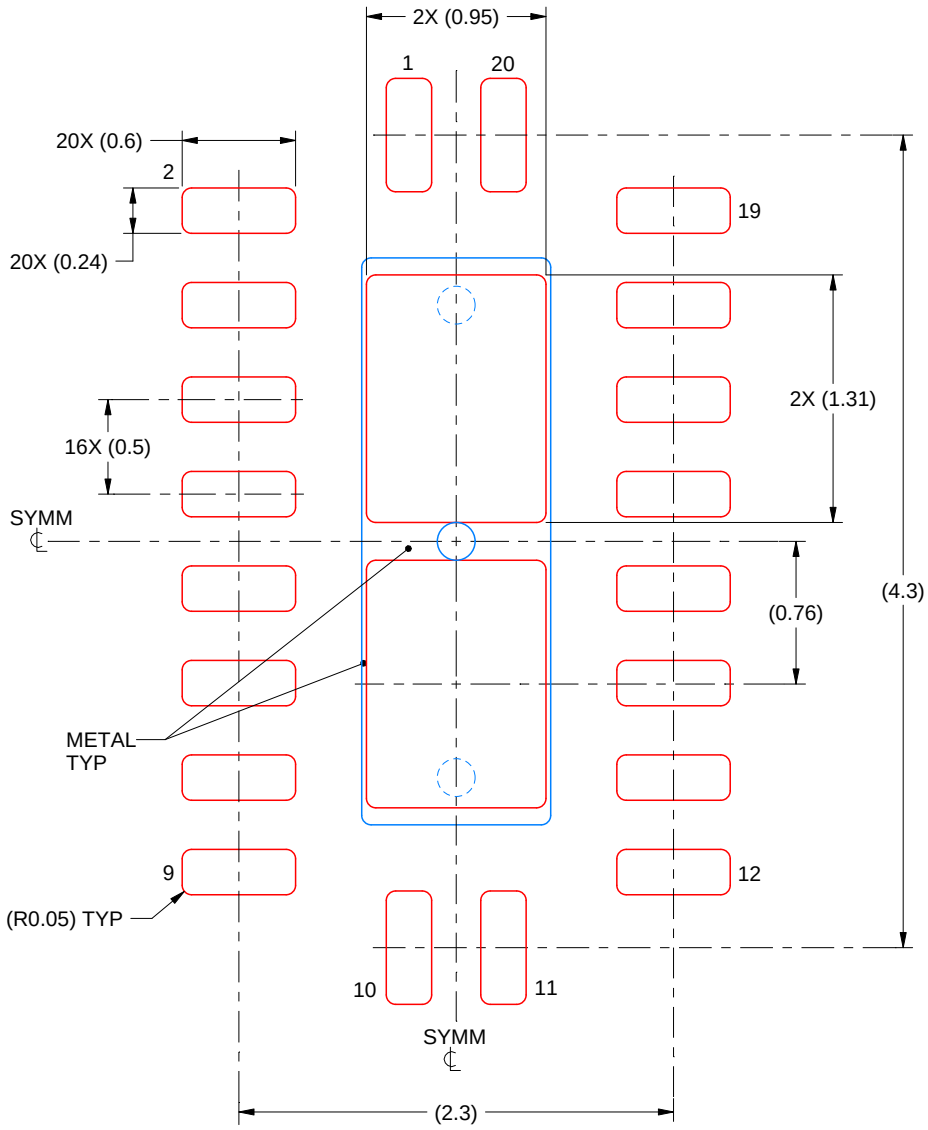


SOLDER MASK DETAILS

4222490/B 02/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
83% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4222490/B 02/2021

NOTES: (continued)

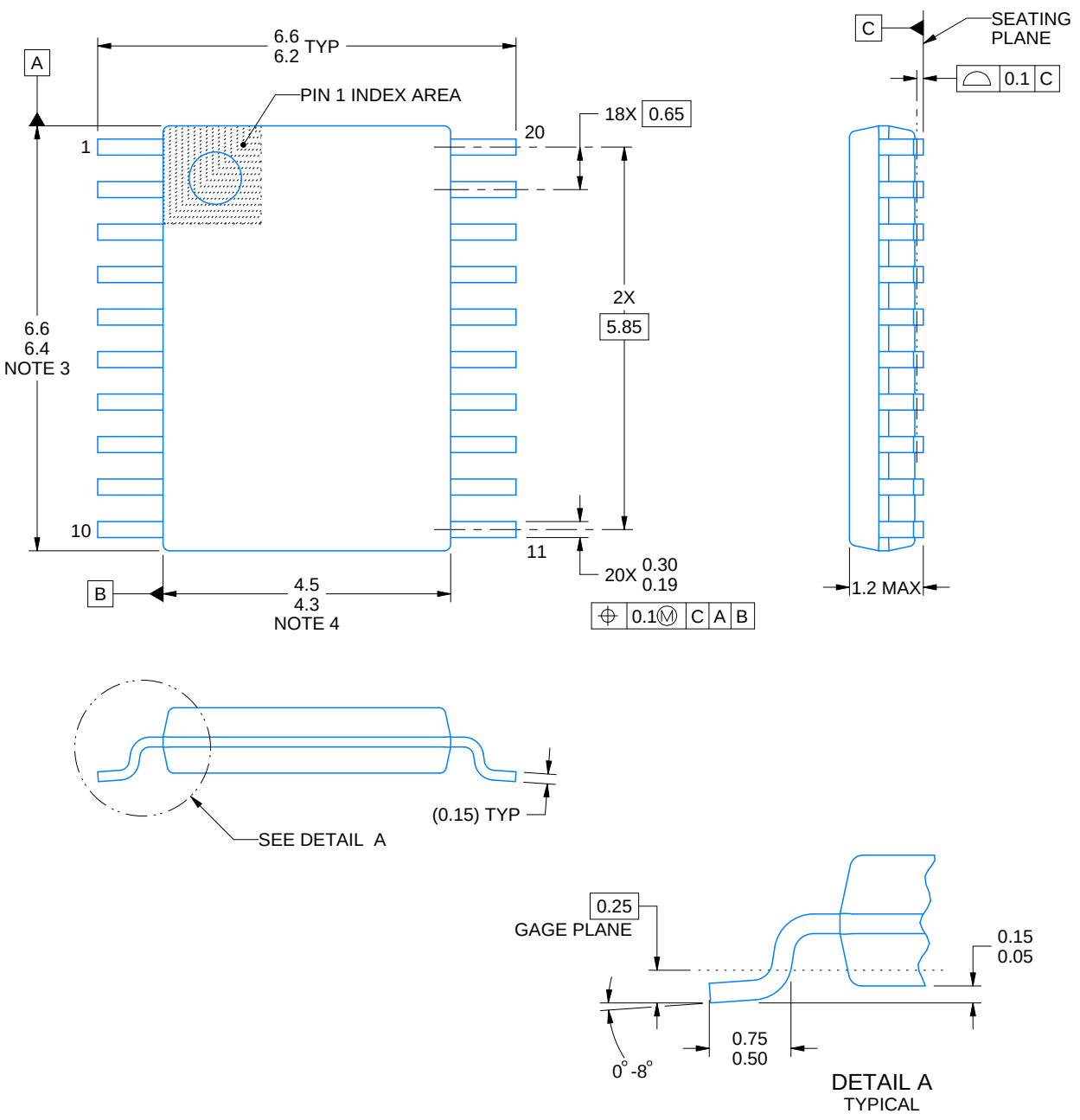
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PW0020A

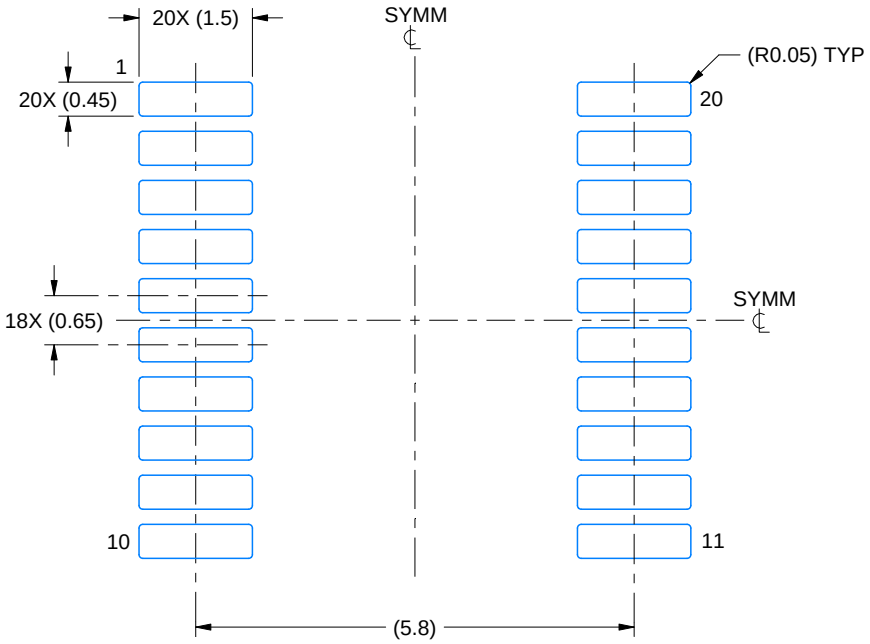
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



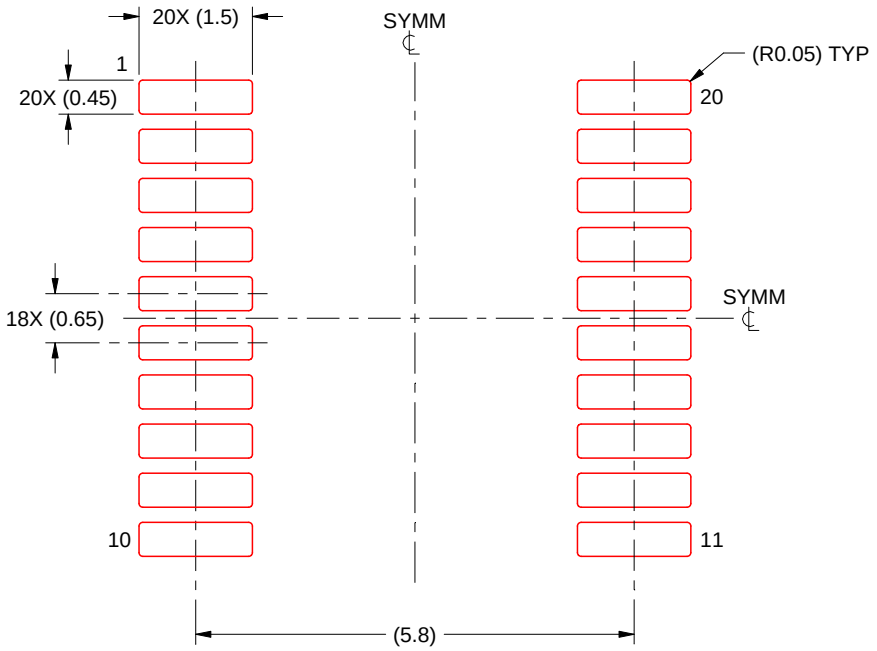
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

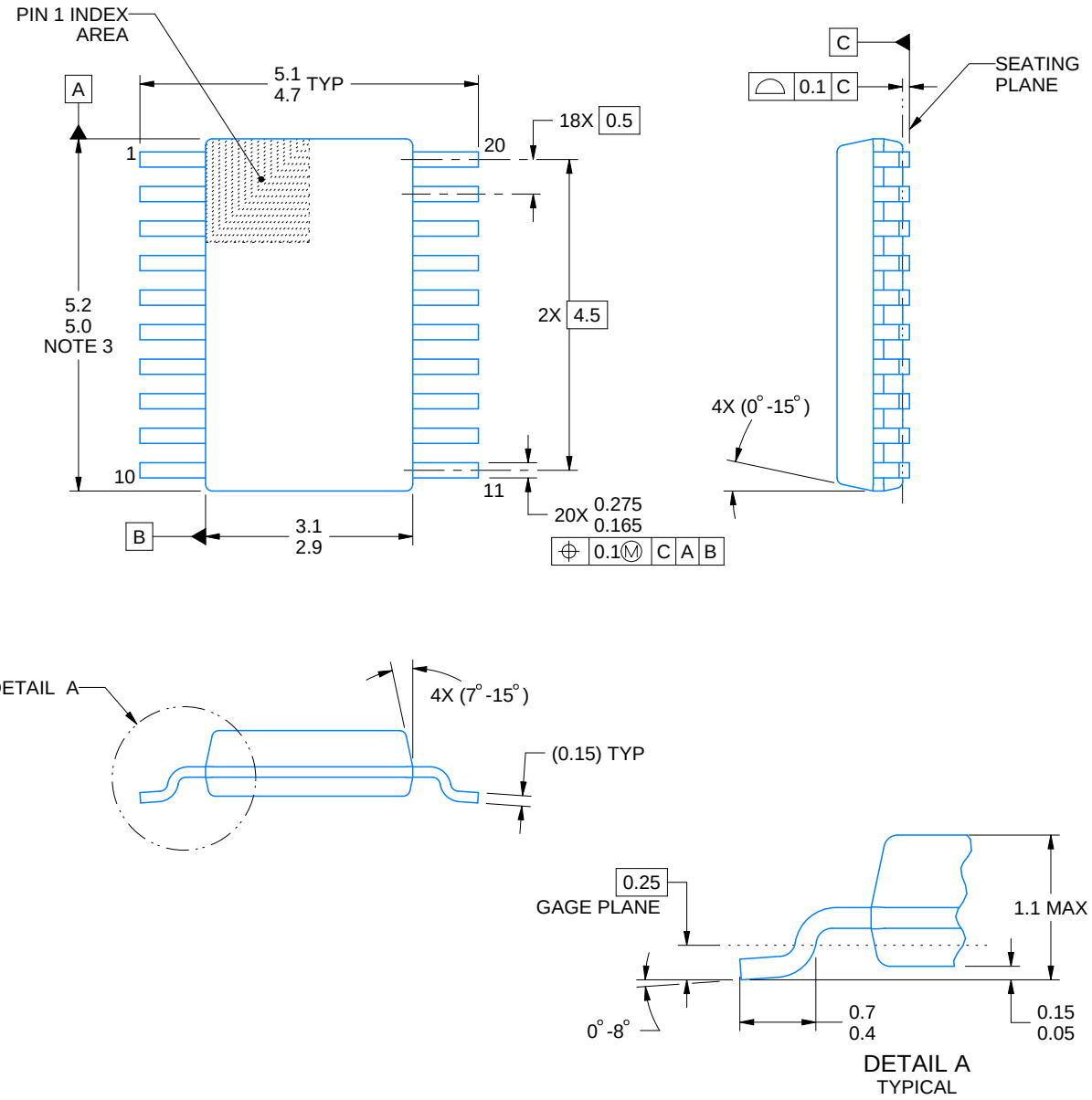
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGS0020A

VSSOP - 1.1 mm max height

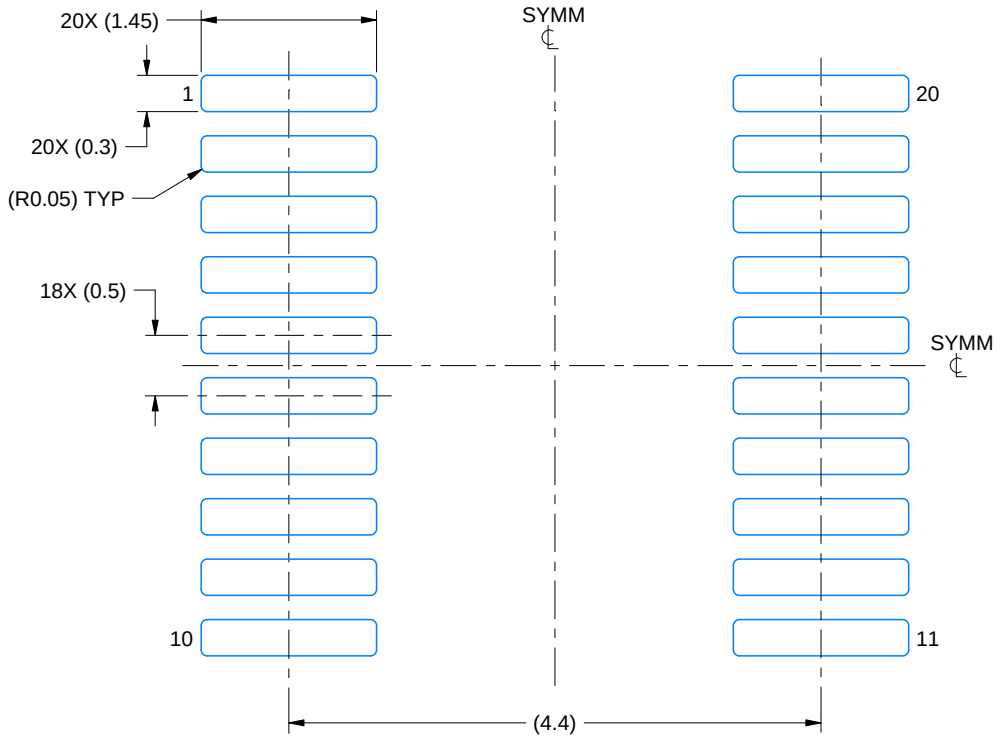
SMALL OUTLINE PACKAGE



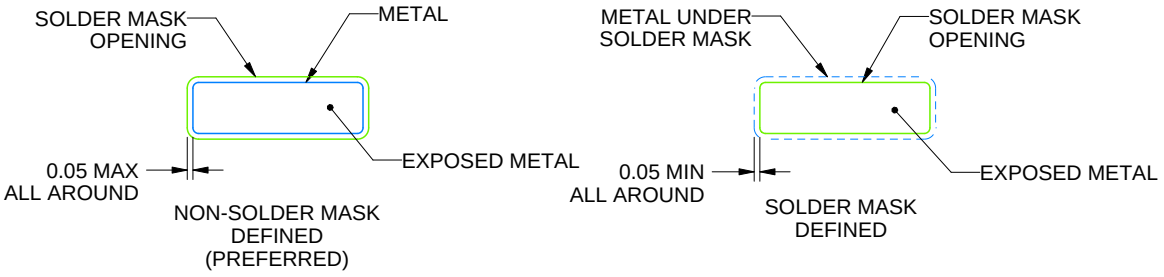
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
SCALE: 16X

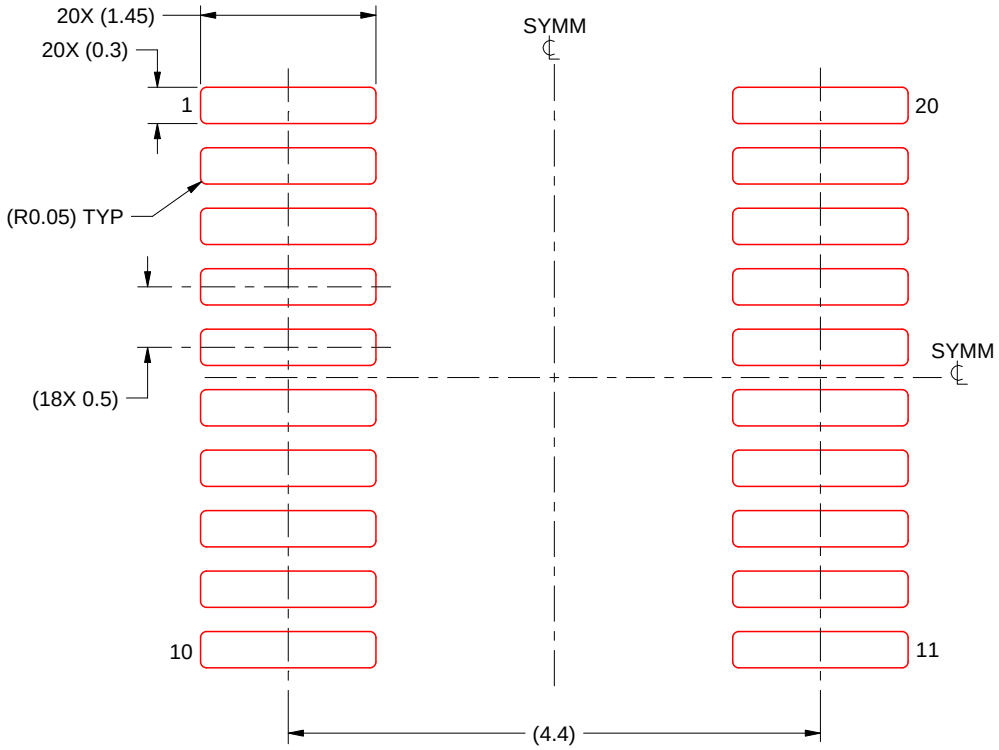


SOLDER MASK DETAILS

4226367/A 10/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 16X

4226367/A 10/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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