

LPC660 Low Power CMOS Quad Operational Amplifier

Check for Samples: LPC660

FEATURES

Rail-to-rail output swing

Micropower operation: (1 mW)

Specified for 100 kΩ and 5 kΩ loads

• High voltage gain: 120 dB

Low input offset voltage: 3 mV

Low offset voltage drift: 1.3 μV/°C

Ultra low input bias current: 2 fA

Input common-mode includes V⁻

Operation range from +5V to +15V

Low distortion: 0.01% at 1 kHz

• Slew rate: 0.11 V/μs

Full military temp. range available

APPLICATIONS

- High-impedance buffer
- Precision current-to-voltage converter
- · Long-term integrator
- High-impedance preamplifier
- Active filter
- Sample-and-Hold circuit
- Peak detector

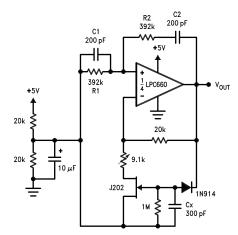
Application Circuit

DESCRIPTION

The LPC660 CMOS Quad operational amplifier is ideal for operation from a single supply. It features a wide range of operating voltages from +5V to +15V and features rail-to-rail output swing in addition to an input common-mode range that includes ground. Performance limitations that have plagued CMOS amplifiers in the past are not a problem with this design. Input $V_{OS},$ drift, and broadband noise as well as voltage gain (into 100 k Ω and 5 k Ω) are all equal to or better than widely accepted bipolar equivalents, while the power supply requirement is typically less than 1 mW.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LPC662 datasheet for a Dual CMOS operational amplifier and LPC661 datasheet for a single CMOS operational amplifier with these same features.



Oscillator frequency is determined by R1, R2, C1, and C2:

 $f_{OSC}=1/2\pi RC$

where R = R1 = R2 and C = C1 = C2.

Figure 1. Sine-Wave Oscillator

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

Abootato maximum ratingo	
Differential Input Voltage	±Supply Voltage
Supply Voltage (V ⁺ - V ⁻)	16V
Output Short Circuit to V ⁺	(2)
Output Short Circuit to V	(3)
Lead Temperature	
(Soldering, 10 sec.)	260°C
Storage Temp. Range	−65°C to +150°C
Junction Temperature (4)	150°C
ESD Rating	
(C = 100 pF, R = 1.5 kΩ)	1000V
Power Dissipation	(4)
Current at Input Pin	±5 mA
Current at Output Pin	±18 mA
Voltage at Input/Output Pin	$(V^+) + 0.3V, (V^-) - 0.3V$
Current at Power Supply Pin	35 mA

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.
- Do not connect output to V⁺when V⁺ is greater than 13V or reliability may be adversely affected.
- Applies to both single supply and split supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.
- The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)\theta_{JA}$.

Operating Ratings (1)

Temperature Range	
LPC660AM	-55°C ≤ T _J ≤ +125°C
LPC660AI	-40°C ≤ T _J ≤ +85°C
LPC660I	-40°C ≤ T _J ≤ +85°C
Supply Range	4.75V to 15.5V
Power Dissipation	(2)
Thermal Resistance (θ _{JA}), ⁽³⁾	
14-Pin Ceramic DIP	90°C/W
14-Pin Molded DIP	85°C/W
14-Pin SOIC	115°C/W
14-Pin Side Brazed Ceramic DIP	90°C/W

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. For operating at elevated temperatures, the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.
- All numbers apply for packages soldered directly into a PC board.

Submit Documentation Feedback

Copyright © 1998-2013, Texas Instruments Incorporated



DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^{\circ}C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$, and $R_L > 1M$ unless otherwise specified.

			LPC660AM	1.0000041	I BOSSOI	Units	
Parameter	Conditions	Тур	LPC660AMJ/883	LPC660AI	LPC660I		
			Limit (1) (2)	Limit (1)	Limit (1)	1	
Input Offset Voltage		1	3	3	6	mV	
			3.5	3.3	6.3	max	
Input Offset Voltage Average Drift		1.3				μV/°C	
Input Bias Current		0.002	20			pА	
			100	4	4	max	
Input Offset Current		0.001	20			pА	
			100	2	2	max	
Input Resistance		>1				Tera Ω	
Common Mode Rejection	0V ≤ V _{CM} ≤ 12.0V	83	70	70	63	dB	
Ratio	V ⁺ = 15V		68	68	61	min	
Positive Power Supply	5V ≤ V ⁺ ≤ 15V	83	70	70	63	dB	
Rejection Ratio			68	68	61	min	
Negative Power Supply	0V ≤ V ⁻ ≤ −10V	94	84	84	74	dB	
Rejection Ratio			82	83	73	min	
Input Common Mode	V ⁺ = 5V & 15V	-0.4	-0.1	-0.1	-0.1	V	
Voltage Range	For CMRR > 50 dB		0	0	0	max	
		V ⁺ - 1.9	V ⁺ - 2.3	V ⁺ - 2.3	V ⁺ - 2.3	V	
			V ⁺ - 2.6	V+ - 2.5	V ⁺ - 2.5	min	
Large Signal	$R_L = 100 \text{ k}\Omega^{(3)}$	1000	400	400	300	V/mV	
Voltage Gain	Sourcing		250	300	200	min	
	Sinking	500	180	180	90	V/mV	
			70	120	70	min	
	$R_L = 5 k\Omega^{(3)}$	1000	200	200	100	V/mV	
	Sourcing		150	160	80	min	
	Sinking	250	100	100	50	V/mV	
			35	60	40	min	

Copyright © 1998–2013, Texas Instruments Incorporated

⁽¹⁾ Limits are guaranteed by testing or correlation.

⁽²⁾ A military RETS electrical test specification is available on request. At the time of printing, the LPC660AMJ/883 RETS specification complied fully with the **boldface** limits in this column. The LPC660AMJ/883 may also be procured to a Standard Military Drawing specification.

⁽³⁾ $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V \le V_O \le 11.5V$. For Sinking tests, $2.5V \le V_O \le 7.5V$.



DC Electrical Characteristics (continued)

Unless otherwise specified, all limits guaranteed for $T_J = 25^{\circ}C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$, and $R_L > 1M$ unless otherwise specified.

Parameter	Conditions	Тур	LPC660AM LPC660AMJ/883	LPC660AI	LPC660I	Units	
			Limit (1) (2)	Limit (1)	Limit (1)		
Output Swing	V ⁺ = 5V	4.987	4.970	4.970	4.940	V	
	$R_L = 100 \text{ k}\Omega \text{ to V}^+/2$		4.950	4.950	4.910	min	
		0.004	0.030	0.030	0.060	V	
			0.050	0.050	0.090	max	
	V ⁺ = 5V	4.940	4.850	4.850	4.750	V	
	$R_L = 5 k\Omega \text{ to } V^+/2$		4.750	4.750	4.650	min	
		0.040	0.150	0.150	0.250	V	
			0.250	0.250	0.350	max	
	V ⁺ = 15V	14.970	14.920	14.920	14.880	V	
	$R_L = 100 \text{ k}\Omega \text{ to V}^+/2$		14.880	14.880	14.820	min	
		0.007	0.030	0.030	0.060	V	
			0.050	0.050	0.090	max	
	V ⁺ = 15V	14.840	14.680	14.680	14.580	V	
	$R_L = 5 k\Omega \text{ to } V^+/2$		14.600	14.600	14.480	min	
		0.110	0.220	0.220	0.320	V	
			0.300	0.300	0.400	max	
Output Current	Sourcing, V _O = 0V	22	16	16	13	mA	
$V^{+} = 5V$			12	14	11	min	
	Sinking, $V_O = 5V$	21	16	16	13	mA	
			12	14	11	min	
Output Current	Sourcing, V _O = 0V	40	19	28	23	mA	
V ⁺ = 15V			19	25	20	min	
	Sinking, V _O = 13V	39	19	28	23	mA	
	(4)		19	24	19	min	
Supply Current	All Four Amplifiers	160	200	200	240	μΑ	
	V _O = 1.5V		250	230	270	max	

⁽⁴⁾ Do not connect output to V⁺when V⁺ is greater than 13V or reliability may be adversely affected.



AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^{\circ}C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5$, and $R_L > 1M$ unless otherwise specified.

Parameter	Conditions	Тур	LPC660AM LPC660AMJ/883	LPC660AI	LPC660I	Units
			Limit (1) (2)	Limit (1)	Limit (1)	
Slew Rate	(3)	0.11	0.07	0.07	0.05	V/µs
			0.04	0.05	0.03	min
Gain-Bandwidth Product		0.35				MHz
Phase Margin		50				Deg
Gain Margin		17				dB
Amp-to-Amp Isolation	(4)	130				dB
Input Referred Voltage Noise	F = 1 kHz	42				nV/√ Hz
Input Referred Current Noise	F = 1 kHz	0.0002				pA/√ Hz
Total Harmonic Distortion	$F = 1 \text{ kHz}, A_V = -10$ $R_L = 100 \text{ k}Ω, V_O = 8 \text{ V}_{PP}$	0.01				%

Limits are guaranteed by testing or correlation.

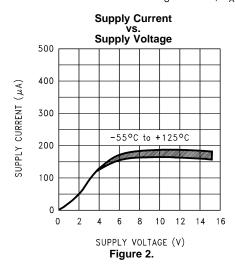
Submit Documentation Feedback Product Folder Links: LPC660

A military RETS electrical test specification is available on request. At the time of printing, the LPC660AMJ/883 RETS specification complied fully with the **boldface** limits in this column. The LPC660AMJ/883 may also be procured to a Standard Military Drawing (3) V⁺ = 15V. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.
 (4) Input referred. V⁺ = 15V and R_L = 100 kΩ connected to V⁺/2. Each amp excited in turn with 1 kHz to produce V_O = 13 V_{PP}.



Typical Performance Characteristics

 $V_S = \pm 7.5 V$, $T_A = 25$ °C unless otherwise specified



Common-Mode Voltage Range

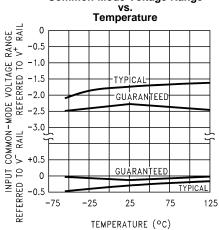
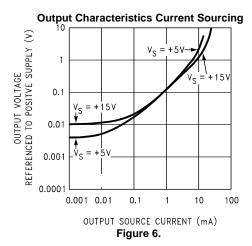
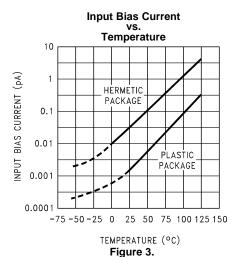


Figure 4.





Output Characteristics Current Sinking

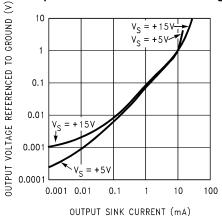
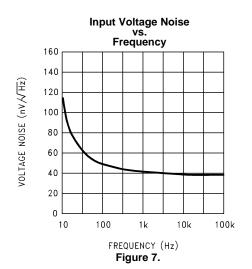


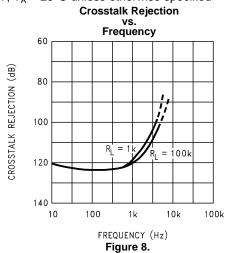
Figure 5.

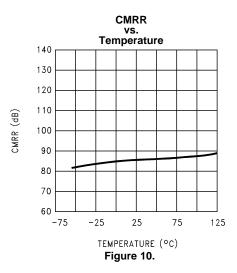


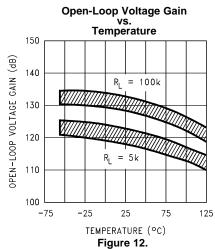


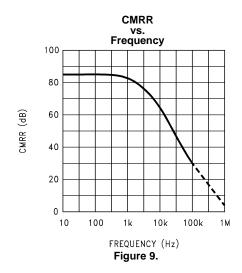
Typical Performance Characteristics (continued)

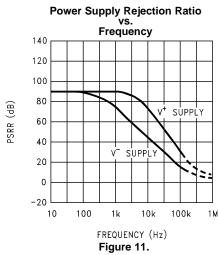
 $V_S = \pm 7.5V$, $T_A = 25$ °C unless otherwise specified

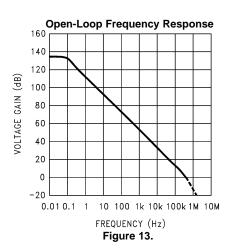








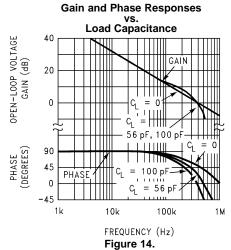


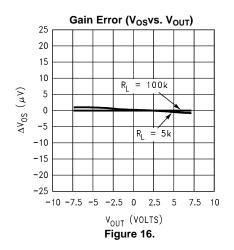




Typical Performance Characteristics (continued)

 $V_S = \pm 7.5V$, $T_A = 25$ °C unless otherwise specified





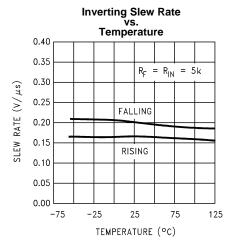
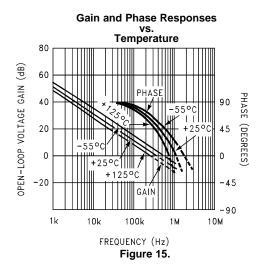
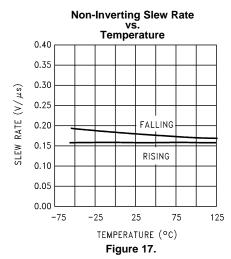


Figure 18.





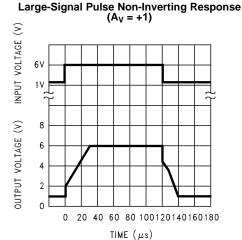


Figure 19.

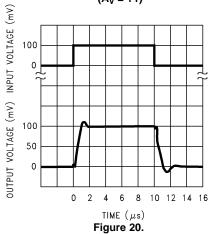
В.



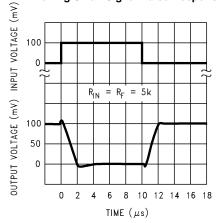
Typical Performance Characteristics (continued)

 $V_S = \pm 7.5V$, $T_A = 25$ °C unless otherwise specified

Non-Inverting Small Signal Pulse Response (A_V = +1)



Inverting Small-Signal Pulse Response



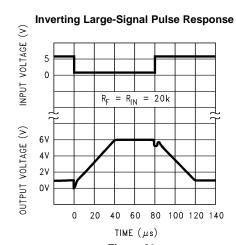
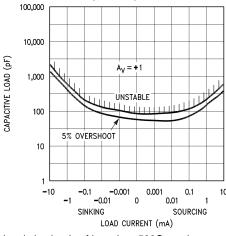


Figure 21.

Stability vs. Capacitive Load



Note: Avoid resistive loads of less than 500Ω , as they may cause instability.

Figure 22.

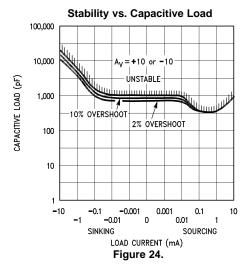


Figure 23.



Application Hints

AMPLIFIER TOPOLOGY

The topology chosen for the LPC660 is unconventional (compared to general-purpose op amps) in that the traditional unity-gain buffer output stage is not used; instead, the output is taken directly from the output of the integrator, to allow rail-to-rail output swing. Since the buffer traditionally delivers the power to the load, while maintaining high op amp gain and stability, and must withstand shorts to either rail, these tasks now fall to the integrator.

As a result of these demands, the integrator is a compound affair with an embedded gain stage that is doubly fed forward (via C_f and C_{ff}) by a dedicated unity-gain compensation driver. In addition, the output portion of the integrator is a push-pull configuration for delivering heavy loads. While sinking current the whole amplifier path consists of three gain stages with one stage fed forward, whereas while sourcing the path contains four gain stages with two fed forward.

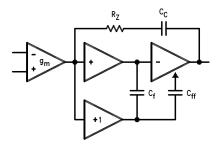


Figure 25. LPC660 Circuit Topology (Each Amplifier)

The large signal voltage gain while sourcing is comparable to traditional bipolar op amps, for load resistance of at least 5 k Ω . The gain while sinking is higher than most CMOS op amps, due to the additional gain stage; however, when driving load resistance of 5 k Ω or less, the gain will be reduced as indicated in the Electrical Characteristics. The op amp can drive load resistance as low as 500 Ω without instability.

COMPENSATING INPUT CAPACITANCE

Refer to the LMC660 or LMC662 datasheets to determine whether or not a feedback capacitor will be necessary for compensation and what the value of that capacitor would be.

CAPACITIVE LOAD TOLERANCE

Like many other op amps, the LPC660 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See the Typical Performance Characteristics.

The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. The addition of a small resistor (50Ω to 100Ω) in series with the op amp's output, and a capacitor (5 pF to 10 pF) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit operation. Thus, larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.

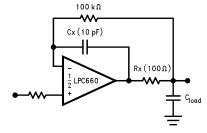


Figure 26. Rx, Cx Improve Capacitive Load Tolerance

0



Capacitive load driving capability is enhanced by using a pull up resistor to V $^+$ (Figure 27). Typically a pull up resistor conducting 50 μ A or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).

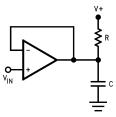


Figure 27. Compensating for LargeCapacitive Loads with A Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LPC660, typically less than 0.04 pA, it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LPC660's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs. See Figure 28. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of 10¹² ohms, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of an input. This would cause a 100 times degradation from the LPC660's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of 10¹¹ ohms would cause only 0.05 pA of leakage current, or perhaps a minor (2:1) degradation of the amplifier's performance. See Figure 29a, Figure 30b, Figure 31c for typical connections of guard rings for standard op-amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see Figure 32d.

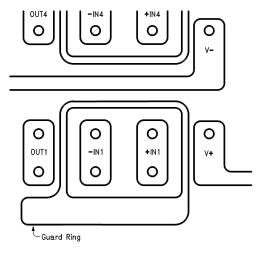


Figure 28. Example of Guard Ring in P.C. Board Layout using the LPC660



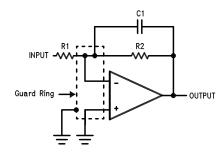


Figure 29. (a) Inverting Amplifier

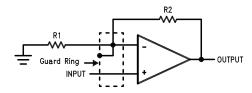


Figure 30. (b) Non-Inverting Amplifier

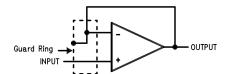


Figure 31. (c) Follower

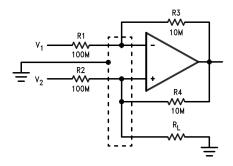
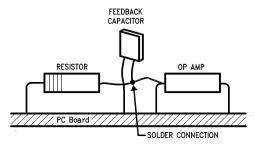


Figure 32. (d) Howland Current Pump

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 33.





(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

Figure 33. Air Wiring

BIAS CURRENT TESTING

The test method of Figure 34 is appropriate for bench-testing bias current with reasonable accuracy. To understand its operation, first close switch S2 momentarily. When S2 is opened, then

$$I^{-} = \frac{dV_{OUT}}{dt} \times C2. \tag{1}$$

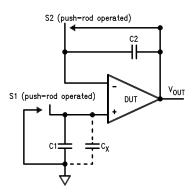


Figure 34. Simple Input Bias Current Test Circuit

A suitable capacitor for C2 would be a 5 pF or 10 pF silver mica, NPO ceramic, or air-dielectric. When determining the magnitude of I⁻, the leakage of the capacitor and socket must be taken into account. Switch S2 should be left shorted most of the time, or else the dielectric absorption of the capacitor C2 could cause errors.

Similarly, if S1 is shorted momentarily (while leaving S2 shorted)

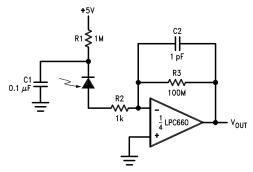
$$I^{+} = \frac{dV_{OUT}}{dt} \times (C1 + C_{\chi}) \tag{2}$$

where C_x is the stray capacitance at the + input.



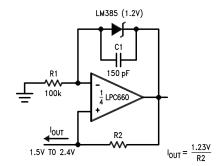
Typical Single-Supply Applications — $(V^+ = 5.0 V_{DC})$

Figure 35. Photodiode Current-to-Voltage Converter



Note: A 5V bias on the photodiode can cut its capacitance by a factor of 2 or 3, leading to improved response and lower noise. However, this bias on the photodiode will cause photodiode leakage (also known as its dark current).

Figure 36. Micropower Current Source



Note: (Upper limit of output range dictated by input common-mode range; lower limit dictated by minimum current requirement of LM385.)

Figure 37. Low-Leakage Sample-and-Hold

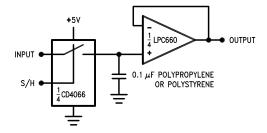
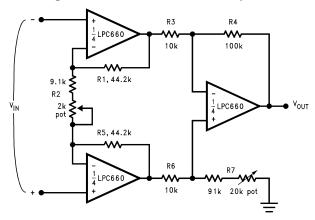




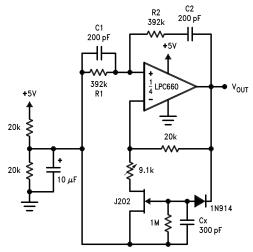
Figure 38. Instrumentation Amplifier



$$\begin{split} &\text{If R1} = \text{R5, R3} = \text{R6, and R4} = \text{R7;} \\ &\text{then } \frac{V_{OUT}}{V_{IN}} = \frac{\text{R2} + 2\text{R1}}{\text{R1}} \times \frac{\text{R4}}{\text{R3}} \\ &\therefore \text{A}_{V} \approx \text{100 for circuits shown.} \end{split}$$

For good CMRR over temperature, low drift resistors should be used. Matching of R3 to R6 and R4 to R7 affects CMRR. Gain may be adjusted through R2. CMRR may be adjusted through R7.

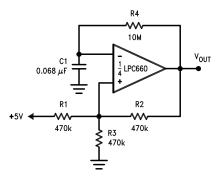
Figure 39. Sine-Wave Oscillator



Oscillator frequency is determined by R1, R2, C1, and C2: f_{OSC} = $1/2\pi RC$

where R = R1 = R2 and C = C1 = C2.

Figure 40. 1 Hz Square-Wave Oscillator





This circuit, as shown, oscillates at 2.0 kHz with a peak-to-peak output swing of 4.5V

Figure 41. Power Amplifier

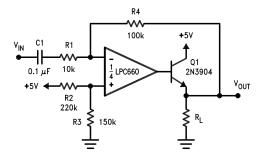
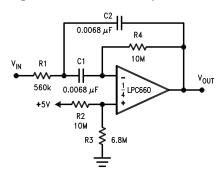
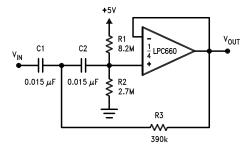


Figure 42. 10 Hz Bandpass Filter



 $f_O = 10 \text{ Hz}$ Q = 2.1Gain = -8.8

Figure 43. 10 Hz High-Pass Filter (2 dB Dip)



 $f_c = 10 \text{ Hz}$ d = 0.895Gain = 1

Figure 44. 1 Hz Low-Pass Filter (Maximally Flat, Dual Supply Only)

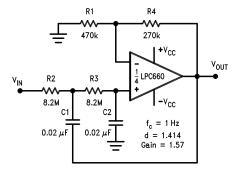
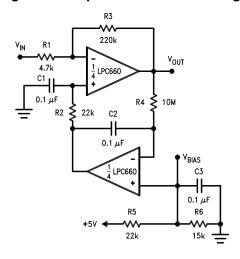




Figure 45. High Gain Amplifier with Offset Voltage Reduction



Gain = -46.8

Output offset voltage reduced to the level of the input offset voltage of the bottom amplifier (typically 1 mV), referred to V_{BIAS} .

Connection Diagram

Figure 46. 14-Pin SOIC Package See Package Number D0014A

SNOS554D -MAY 1998-REVISED MARCH 2013



REVISION HISTORY

Cr	nanges from Revision C (March 2013) to Revision D	Pa	ıg
•	Changed layout of National Data Sheet to TI format		17

www.ti.com

11-Nov-2025

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
LPC660AIM/NOPB	Active	Production	SOIC (D) 14	55 TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LPC660AIM
LPC660AIM/NOPB.A	Active	Production	SOIC (D) 14	55 TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LPC660AIM
LPC660AIM/NOPB.B	Active	Production	SOIC (D) 14	55 TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LPC660AIM
LPC660AIMX/NOPB	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LPC660AIM
LPC660AIMX/NOPB.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LPC660AIM
LPC660AIMX/NOPB.B	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LPC660AIM
LPC660IM/NOPB	Active	Production	SOIC (D) 14	55 TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LPC660IM
LPC660IM/NOPB.A	Active	Production	SOIC (D) 14	55 TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LPC660IM
LPC660IM/NOPB.B	Active	Production	SOIC (D) 14	55 TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LPC660IM
LPC660IMX/NOPB	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LPC660IM
LPC660IMX/NOPB.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LPC660IM
LPC660IMX/NOPB.B	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LPC660IM

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No. RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

www.ti.com 11-Nov-2025

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

www.ti.com 23-May-2025

TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LPC660AIMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LPC660IMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1



www.ti.com 23-May-2025



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LPC660AIMX/NOPB	SOIC	D	14	2500	356.0	356.0	35.0
LPC660IMX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0

PACKAGE MATERIALS INFORMATION

www.ti.com 23-May-2025

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LPC660AIM/NOPB	D	SOIC	14	55	495	8	4064	3.05
LPC660AIM/NOPB.A	D	SOIC	14	55	495	8	4064	3.05
LPC660AIM/NOPB.B	D	SOIC	14	55	495	8	4064	3.05
LPC660IM/NOPB	D	SOIC	14	55	495	8	4064	3.05
LPC660IM/NOPB.A	D	SOIC	14	55	495	8	4064	3.05
LPC660IM/NOPB.B	D	SOIC	14	55	495	8	4064	3.05



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale, TI's General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025