LP5862 2 × 18 LED Matrix Driver with 8-Bit Analog and 8-/16-Bit PWM Dimming

1 Features

- LED matrix topology:
  - 18 constant current sinks with 2 scan switches for 36 LED dots
  - Configurable for 1 to 2 scan switches
- Operating voltage range:
  - V_{CC}/V_{LED} range: 2.7V to 5.5V
  - Logic pins compatible with 1.8V, 3.3V, and 5V
- 18 constant current sinks with high precision:
  - 50mA per current sink when V_{CC} ≥ 3.3V
  - Device-to-device error: ±5%
  - Channel-to-channel error: ±5%
  - Phase-shift for balanced transient power
- Ultra-low power consumption:
  - Shutdown mode: I_{CC} ≤ 2μA when EN = Low
  - Standby mode: I_{CC} ≤ 10μA when EN = High and CHIP_EN = 0 (data retained)
  - Active mode: I_{CC} = 3mA (typ.) when channel current = 5mA
- Flexible dimming options:
  - Individual ON, OFF control for each LED dot
  - Analog dimming (current gain control)
    - Global 3-bit Maximum Current (MC) setting for all LED dots
    - 3 groups of 7-bit Color Current (CC) setting for red, green, and blue
    - Individual 8-bit Dot Current (DC) setting for each LED dot
  - PWM dimming with audible-noise-free frequency
    - Global 8-bit PWM dimming for all LED dots
    - 3 programmable groups of 8-bit PWM dimming for LED dot arbitrary mapping
    - Individual 8-bit or 16-bit PWM dimming for each LED dot
- Full addressable SRAM to minimize data traffic
- Individual LED dot open and short detection
- Deghosting and low brightness compensation
- Interface options:
  - 1MHz (max.) I^2C interface when IFS = Low
  - 12MHz (max.) SPI interface when IFS = High

2 Applications

- LED animation and indication for:
  - Keyboard, mouse, and gaming accessories
  - Major and smart home appliances
  - Smart speaker, wired and wireless speaker
  - Audio mixer, DJ equipment, and broadcast
  - Access equipment, switches, and servers
- Constant current sinks for optical module

3 Description

Electronic devices are becoming smarter, requiring larger quantity of LEDs for animation and indication purposes. A high-performance LED matrix driver is required to improve user experience with small solution size.

The LP586x devices are a family of high performance LED matrix drivers. The device integrates 18 constant current sinks with N (N = 1/2/4/6/8/11) switching MOSFETs to support N × 18 LED dots or N × 6 RGB LEDs. The LP5862 integrates two MOSFETs for up to 36 LED dots or 12 RGB LEDs.

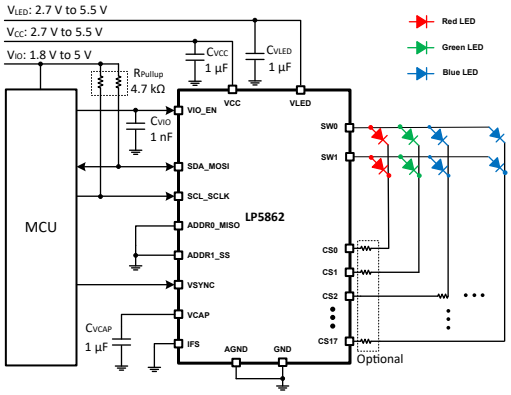
The LP5862 supports both analog dimming and PWM dimming methods. For analog dimming, each LED dot can be adjusted with 256 steps. For PWM dimming, the integrated 8-bit or 16-bit configurable PWM generators enable smooth and audible-noise-free dimming control. Each LED dot can also be arbitrarily mapped into 8-bit Group PWM to achieve dimming control together.

The LP5862 device implements full addressable SRAM to minimize the data traffic. The ghost-cancellation circuitry is integrated to eliminate both upside and downside ghosting. The LP5862 also supports LED open and short detection functions. Both 1-MHz (maximum) I^2C and 12-MHz (maximum) SPI are available in LP5862.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
LP5862	VQFN (32)	4.00mm × 4.00mm
	TSSOP (38)	9.70mm × 4.40mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

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4 Device Comparison

PART NUMBER	MATERIAL	LED DOT NUMBER	PACKAGE(2)	SOFTWARE COMPATIBLE
LP5861	LP5861RSMR	18 × 1 = 18	VQFN-32	Yes
LP5862	LP5862RSMR	18 × 2 = 36	VQFN-32	
	LP5862DBTR		TSSOP-38	
LP5864	LP5864RSMR	18 × 4 = 72	VQFN-32	
	LP5864MRSMR(1)			
LP5866	LP5866RKPR	18 × 6 = 108	VQFN-40	
	LP5866DBTR		TSSOP-38	
	LP5866MDBTR(1)			
LP5868	LP5868RKPR	18 × 8 = 144	VQFN-40	
LP5860	LP5862RKPR	18 × 11 = 198	VQFN-40	
	LP5862MRKPR(1)			

(1) Extended Temperature devices, supporting –55°C to approximately 125°C operating ambient temperature.
(2) The same packages are hardware compatible.

5 Pin Configuration and Functions

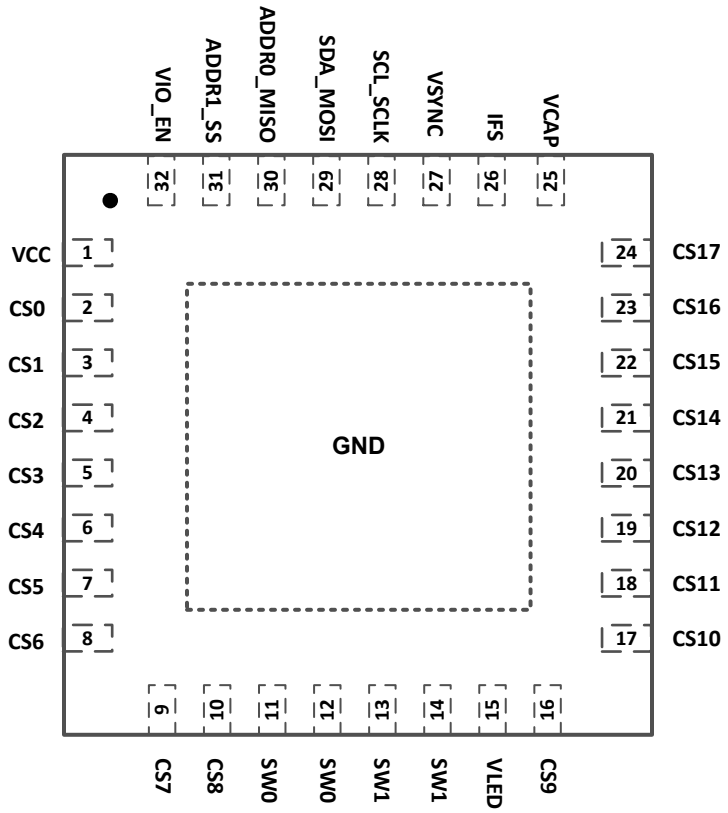


Figure 5-1. LP5862 RSM Package 32-Pin VQFN with Exposed Thermal Pad Top View

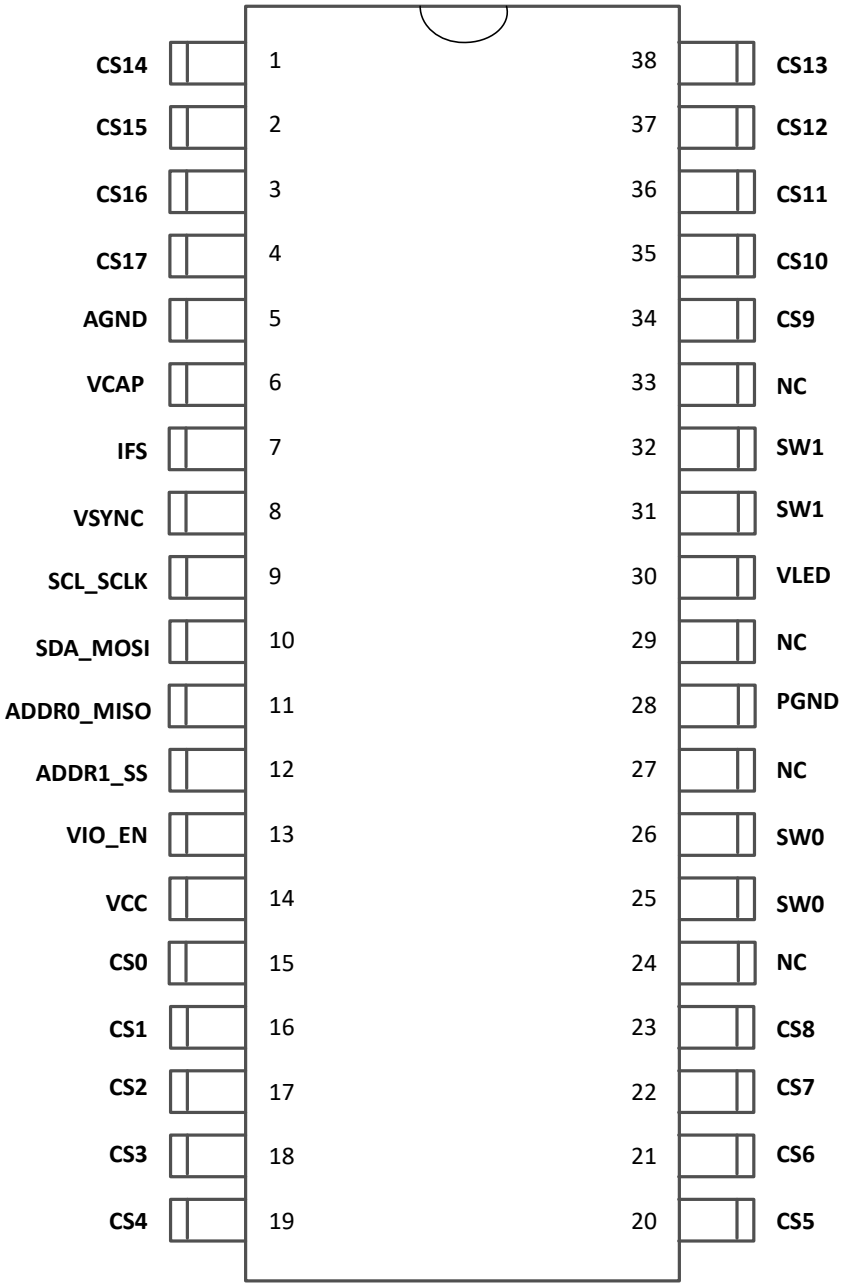


Figure 5-2. LP5862 DBT Package 38-Pin TSSOP Top View

Table 5-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	RSM NO.	DBT NO.		
VCC	1	14	Power	Power supply for device. A 1-µF capacitor must be connected between this pin with GND and be placed as close to the device as possible.
CS0	2	15	O	Current sink 0. If not used, this pin must be left floating.
CS1	3	16	O	Current sink 1. If not used, this pin must be left floating.
CS2	4	17	O	Current sink 2. If not used, this pin must be left floating.
CS3	5	18	O	Current sink 3. If not used, this pin must be left floating.
CS4	6	19	O	Current sink 4. If not used, this pin must be left floating.
CS5	7	20	O	Current sink 5. If not used, this pin must be left floating.

Table 5-1. Pin Functions (continued)

PIN			I/O	DESCRIPTION
NAME	RSM NO.	DBT NO.		
CS6	8	21	O	Current sink 6. If not used, this pin must be left floating.
CS7	9	22	O	Current sink 7. If not used, this pin must be left floating.
CS8	10	23	O	Current sink 8. If not used, this pin must be left floating.
SW0	11/12	25/26	O	High-side PMOS switch output 0. Both 2 pins must be tied together. If not used, this pin must be left floating.
SW1	13/14	31/32	O	High-side PMOS switch output 1. Both 2 pins must be tied together. If not used, this pin must be left floating.
VLED	15	30	Power	Power input for high-side switches.
CS9	16	34	O	Current sink 9. If not used, this pin must be left floating.
CS10	17	35	O	Current sink 10. If not used, this pin must be left floating.
CS11	18	36	O	Current sink 11. If not used, this pin must be left floating.
CS12	19	37	O	Current sink 12. If not used, this pin must be left floating.
CS13	20	38	O	Current sink 13. If not used, this pin must be left floating.
CS14	21	1	O	Current sink 14. If not used, this pin must be left floating.
CS15	22	2	O	Current sink 15. If not used, this pin must be left floating.
CS16	23	3	O	Current sink 16. If not used, this pin must be left floating.
CS17	24	4	O	Current sink 17. If not used, this pin must be left floating.
VCAP	25	6	O	Internal LDO output. An 1-µF capacitor must be connected between this pin with GND. Place the capacitor as close to the device as possible.
IFS	26	7	I	Interface type select. I^2C is selected when IFS is low. SPI is selected when IFS is high. A resistor must be connected between VIO and this pin.
VSYNC	27	8	I	External synchronize signal for display mode 2 and mode 3.
SCL_SCLK	28	9	I	I^2C clock input or SPI clock input. Pull up to VIO when configured as I^2C.
SDA_MOSI	29	10	I/O	I^2C data input or SPI leader output follower input. Pull up to VIO when configured as I^2C.
ADDR0_MISO	30	11	I/O	I^2C address select 0 or SPI leader input follower output.
ADDR1_SS	31	12	I	I^2C address select 1 or SPI follower select.
VIO_EN	32	13	Power,I	Power supply for digital circuits and chip enable. A 1-nF capacitor must be connected between this pin with GND and be placed as close to the device as possible.
GND	Exposed Thermal Pad	5/28	Ground	Common ground plane.
NC	-	24/27/29/33	-	No connection.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage on V_{CC} / V_{LED} / VIO / EN / CS / SW / SDA / SCL / SCLK / MOSI / MISO / SS / ADDR0 / ADDR1 / VSYNC / IFS		–0.3	6	V
Voltage on VCAP		–0.3	2	V
T_J	Junction temperature	–55	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±3000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage on V_{CC}	Supply voltage	2.7		5.5	V
Input voltage on V_{LED}	LED supply voltage	2.7		5.5	V
Input voltage on VIO_EN		1.65		5.5	V
Voltage on SDA / SCL / SCLK / MOSI / MISO / SS / ADDRx / VSYNC / IFS				VIO	V
T_A	Operating ambient temperature	–40		85	°C

6.4 Thermal Information

THERMAL METRIC (1)		LP5862		UNIT
		RSM (VQFN)	DBT (TSSOP)	
		32 Pins	38 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32,9	67.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.2	20.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.3	27.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.4	1.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	12.3	27.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.7	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

V_{CC} = 3.3 V, V_{LED} = 3.8 V, VIO = 1.8 V and T_A = –40 °C to +85 °C; Typical values are at T_A = 25 °C (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power supplies						
V_{CC}	Device supply voltage		2.7		5.5	V
V_{UVR}	Undervoltage restart	V_{CC} rising, Test mode			2.5	V
V_{UVF}	Undervoltage shutdown	V_{CC} falling, Test mode	1.9			V
V_{UV_HYS}	Undervoltage shutdown hysteresis			0.3		V
V_{CAP}	Internal LDO output	V_{CC} = 2.7 V to 5.5 V		1.78		V
I_{CC}	Shutdown supply current $I_{SHUTDOWN}$	V_{EN} = 0 V, CHIP_EN = 0 (bit), measure the total current from V_{CC} and V_{LED}		0.1	1	µA
	Standby supply current $I_{STANDBY}$	V_{EN} = 3.3 V, CHIP_EN = 0 (bit), measure the total current from V_{CC} and V_{LED}		5.5	10	µA
	Active mode supply current I_{NORMAL}	V_{EN} = 3.3 V, CHIP_EN = 1 (bit), all channels I_{OUT} = 5 mA (MC = 1, CC = 127, DC = 256), measure the current from V_{CC}		4.3	6	mA
V_{LED}	LED supply voltage		2.7		5.5	V
V_{VIO}	VIO supply voltage		1.65		5.5	V
I_{VIO}	VIO supply current	Interface idle			5	µA
Output Stages						
I_{CS}	Constant current sink output range (CS0 – CS17)	2.7 <= V_{CC} < 3.3 V, PWM = 100%	0.1		40	mA
		V_{CC} >= 3.3 V PWM = 100%	0.1		50	mA
I_{LKG}	Leakage current (CS0 – CS17)	channels off, up_deghost = 0, V_{CS} = 5 V		0.1	1	µA
I_{ERR_DD}	Device to device current error, I_{ERR_DD} = (I_{AVE} - I_{SET}) / I_{SET} × 100%	All channels ON. Current set to 0.1 mA. MC = 0 CC = 42 DC = 25 PWM = 100%	–7		7	%
		All channels ON. Current set to 1 mA. MC = 2 CC = 127 DC = 25 PWM = 100%	–5		5	%
		All channels ON. Current set to 10 mA. MC = 2 CC = 127 DC = 255 PWM = 100%	–3.5		3.5	%
		All channels ON. Current set to 25 mA. MC = 7 CC = 64 DC = 255 PWM = 100%	–3.5		3.5	%
		All channels ON. Current set to 50 mA. MC = 7 CC = 127 DC = 255 PWM = 100%	–3		3	%
I_{ERR_CC}	Channel to channel current error, I_{ERR_CC} = (I_{OUTX} - I_{AVE}) / I_{AVE} × 100%	All channels ON. Current set to 0.1 mA. MC = 0 CC = 42 DC = 25 PWM = 100%	–5.5		5.5	%
		All channels ON. Current set to 1 mA. MC = 2 CC = 127 DC = 25 PWM = 100%	–5		5	%
		All channels ON. Current set to 10 mA. MC = 2 CC = 127 DC = 255 PWM = 100%	–4		4	%
		All channels ON. Current set to 25 mA. MC = 7 CC = 64 DC = 255 PWM = 100%	–3.5		3.5	%
		All channels ON. Current set to 50 mA. MC = 7 CC = 127 DC = 255 PWM = 100%	–3		3	%
f_{PWM}	LED PWM frequency	PWM_Fre = 1, PWM = 100%		62.5		KHz
		PWM_Fre = 0, PWM = 100%		125		KHz

6.5 Electrical Characteristics (continued)

V_{CC} = 3.3 V, V_{LED} = 3.8 V, VIO = 1.8 V and T_A = –40 °C to +85 °C; Typical values are at T_A = 25 °C (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SAT}	Output saturation voltage	I_{OUT} = 50 mA, decreasing output voltage, when the LED current has dropped 5%			0.45	V
		I_{OUT} = 30 mA, decreasing output voltage, when the LED current has dropped 5%			0.4	V
		I_{OUT} = 10 mA, decreasing output voltage, when the LED current has dropped 5%			0.35	V
R_{SW}	High-side PMOS ON resistance	V_{LED} = 2.7 V, I_{SW} = 200 mA		450		mΩ
		V_{LED} = 3.8 V, I_{SW} = 200 mA		380		mΩ
		V_{LED} = 5 V, I_{SW} = 200 mA		310		mΩ
Logic Interfaces						
V_{LOGIC_IL}	Low-level input voltage, SDA, SCL, SCLK, MOSI, SS, ADDRx, VSYNC, IFS				0.3 × VIO	V
V_{LOGIC_IH}	High-level input voltage, SDA, SCL, SCLK, MOSI, SS, ADDRx, VSYNC, IFS		0.7 × VIO			V
V_{EN_IL}	Low-level input voltage of EN				0.4	V
V_{EN_IH}	High-level input voltage of EN	When V_{CAP} powered up	1.4			V
I_{LOGIC_I}	Input current, SDA, SCL, SCLK, MOSI, SS, ADDRx		–1		1	µA
V_{LOGIC_OL}	Low-level output voltage, SDA, MISO	I_{PULLUP} = 3 mA			0.4	V
V_{LOGIC_OH}	High-level output voltage, MISO	I_{PULLUP} = –3 mA	0.7 × VIO			V
Protection Circuits						
V_{LOD_TH}	Thershold for channel open detection			0.25		V
V_{LSD_TH}	Thershold for channel short detection			V_{LED} – 1		V
T_{TSD}	Thermal-shutdown junction temperature			150		°C
T_{HYS}	Thermal shutdown temperature hysteresis			15		°C

6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
MISC. Timming Requirements					
f_{OSC}	Internal oscillator frequency		31.2		MHz
f_{OSC_ERR}	Device to device oscillator frequency error	–3%		3%	
t_{POR_H}	Wait time from UVLO disactive to device NORMAL			500	µs
t_{CHIP_EN}	Wait time from setting Chip_EN (Register) =1 to device NORMAL			100	µs
t_{RISE}	LED output rise time		10		ns
t_{FALL}	LED output fall time		15		ns
t_{VSYNC_H}	The minimum high-level pulse width of VSYNC	200			µs
SPI timing requirements					
f_{SCLK}	SPI Clock frequency			12	MHz
1	Cycle time	83.3			ns
2	SS active lead-time	50			ns
3	SS active leg time	50			ns
4	SCLK low time	36			ns

6.6 Timing Requirements (continued)

		MIN	NOM	MAX	UNIT
5	SCLK high time	36			ns
6	MOSI set-up time	20			ns
7	MOSI hold time	20			ns
8	MISO disable time			30	ns
9	MISO data valid time			35	ns
10	SS inactive time	50			ns
C_b	Bus capacitance	5		40	pF
I²C standard mode timing requirements					
f_{SCL}	I²C clock frequency	0		100	KHz
1	Hold time (repeated) START condition	4			µs
2	Clock low time	4.7			µs
3	Clock high time	4			µs
4	Setup time for a repeated START condition	4.7			µs
5	Data hold time	0			µs
6	Data setup time	250			ns
7	Rise time of SDA and SCL			1000	ns
8	Fall time of SDA and SCL			300	ns
9	Setup time for STOP condition	4			µs
10	Bus free time between a STOP and a START condition	4.7			µs
I²C fast mode timing requirements					
f_{SCL}	I²C clock frequency	0		400	KHz
1	Hold time (repeated) START condition	0.6			µs
2	Clock low time	1.3			µs
3	Clock high time	0.6			µs
4	Setup time for a repeated START condition	0.6			µs
5	Data hold time	0			µs
6	Data setup time	100			ns
7	Rise time of SDA and SCL			300	ns
8	Fall time of SDA and SCL			300	ns
9	Setup time for STOP condition	0.6			µs
10	Bus free time between a STOP and a START condition	1.3			µs
I²C fast mode plus timing requirements					
f_{SCL}	I²C clock frequency	0		1000	KHz
1	Hold time (repeated) START condition	0.26			µs
2	Clock low time	0.5			µs
3	Clock high time	0.26			µs
4	Setup time for a repeated START condition	0.26			µs
5	Data hold time	0			µs
6	Data setup time	50			ns
7	Rise time of SDA and SCL			120	ns
8	Fall time of SDA and SCL			120	ns
9	Setup time for STOP condition	0.26			µs
10	Bus free time between a STOP and a START condition	0.5			µs

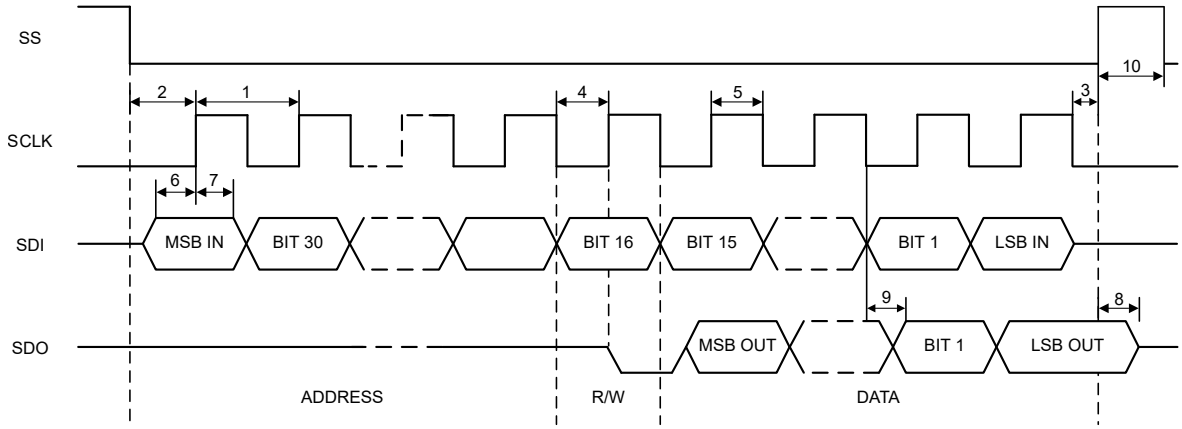


Figure 6-1. SPI Timing Parameters

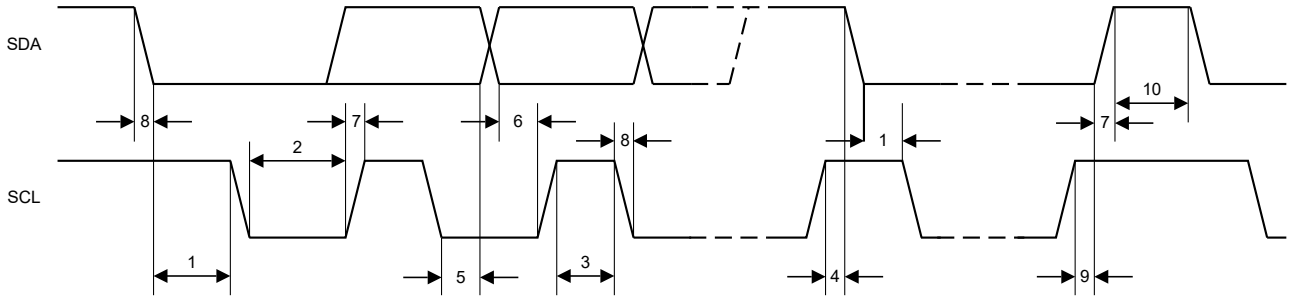


Figure 6-2. I^2C Timing Parameters

6.7 Typical Characteristics

Unless specified otherwise, typical characteristics apply over the full ambient temperature range (–55°C < T_A < +125°C for LP5860MRKPR, LP5864MRSMR, and LP5866MDBTR while –40°C < T_A < +85°C for the other devices), V_{CC} = 3.3 V, V_{IO} = 3.3 V, V_{LED} = 5 V, I_{LED_Peak} = 50 mA, C_{VLED} = 1 µF, C_{VCC} = 1 µF.

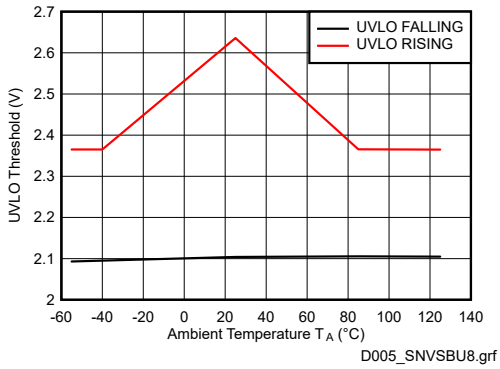


Figure 6-3. V_{CC} UVLO Rising and Falling Thresholds

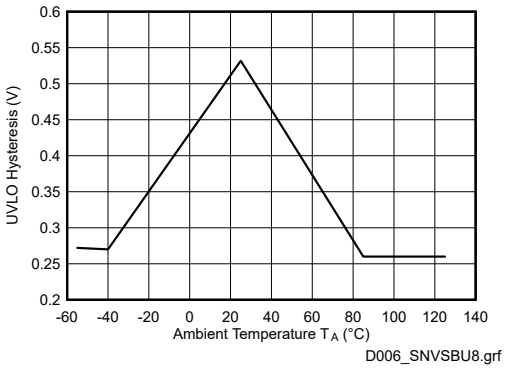


Figure 6-4. V_{CC} UVLO Hysteresis

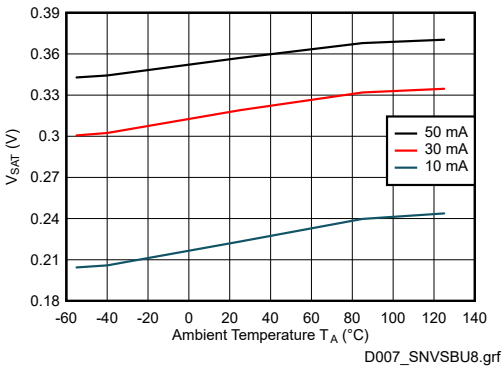


Figure 6-5. V_{SAT} vs Temperature

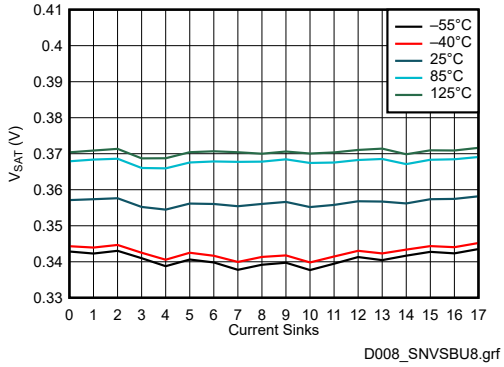


Figure 6-6. V_{SAT} vs Current Sinks (50 mA)

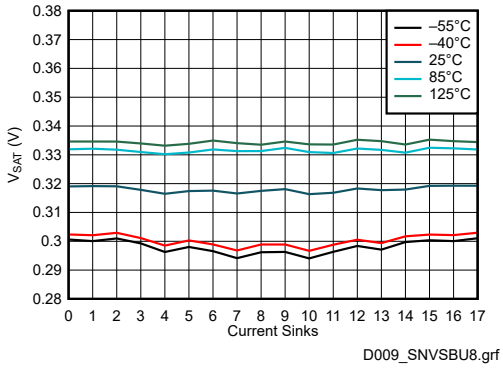


Figure 6-7. V_{SAT} vs Current Sinks (30 mA)

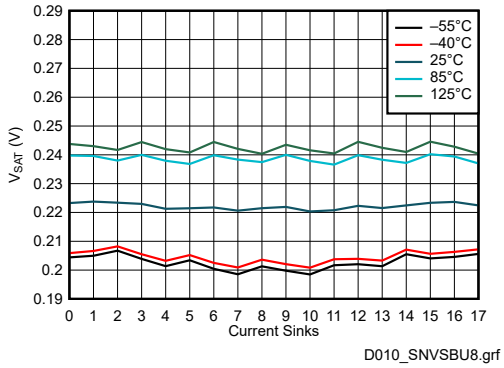
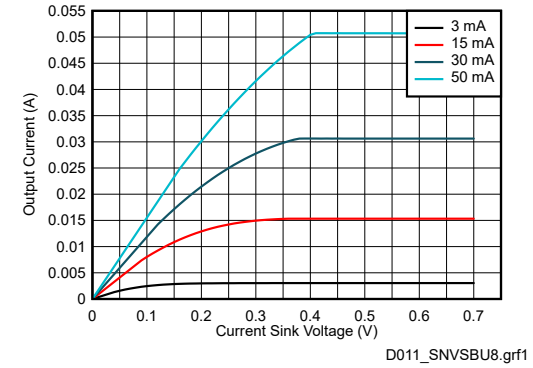


Figure 6-8. V_{SAT} vs Current Sinks (10 mA)

6.7 Typical Characteristics (continued)

Unless specified otherwise, typical characteristics apply over the full ambient temperature range (–55°C < T_A < +125°C for LP5860MRKPR, LP5864MRSMR, and LP5866MDBTR while –40°C < T_A < +85°C for the other devices), V_{CC} = 3.3 V, V_{IO} = 3.3 V, V_{LED} = 5 V, I_{LED_Peak} = 50 mA, C_{VLED} = 1 µF, C_{VCC} = 1 µF.



T_A = 25°C

Figure 6-9. Current Sinks Voltage vs Current

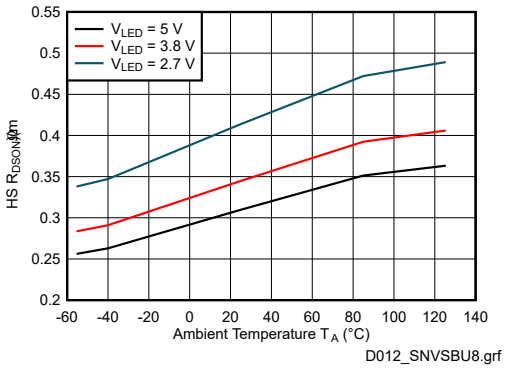


Figure 6-10. High-Side Switch R_{DSON}

7 Detailed Description

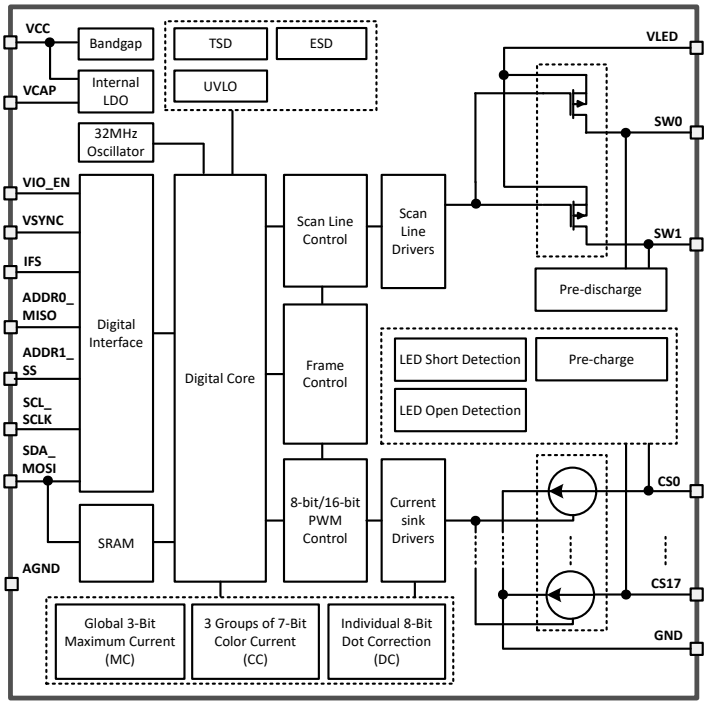
7.1 Overview

The LP5862 is an 2 × 18 LED matrix driver. The device integrates 2 switching FETs with 18 constant current sinks. One LP5862 device can drive up to 36 LED dots or 12 RGB pixels by using time-multiplexing matrix scheme.

The LP5862 supports both analog dimming and PWM dimming methods. For analog dimming, the current gain of each individual LED dot can be adjusted with 256 steps through 8-bits dot correction. For PWM dimming, the integrated 8-bits or 16-bits configurable, > 20KHz PWM generators for each LED dot enable smooth, vivid animation effects without audible noise. Each LED can also be mapped into a 8-bits group PWM to achieve the group control with minimum data traffic.

The LP5862 device implements full addressable SRAM. The device supports entire SRAM data refresh and partial SRAM data update on demand to minimize the data traffic. The LP5862 implements the ghost cancellation circuit to eliminate both upside and downside ghosting. The LP5862 also uses low brightness compensation technology to support high density LED pixels. Both 1MHz (maximum) I^2C and 12MHz (maximum) SPI interfaces are available in the LP5862.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Time-Multiplexing Matrix

The LP5862 device uses time-multiplexing matrix scheme to support up to 36 LED dots with one chip. The device integrates 18 current sinks with 2 scan lines to drive 18 × 2 = 36 LED dots or 6 × 2 = 12 RGB pixels. In matrix control scheme, the device scans from Line 0 to Line 1 sequentially as shown in Figure 7-1. Current gain and PWM duty registers are programmable for each LED dot to support individual analog and PWM dimming.

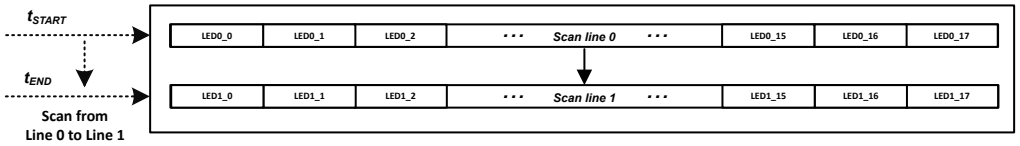


Figure 7-1. Scan Line Control Scheme

There are two high-side p-channel MOSFETs (PMOS) integrated in LP5862 device. Users can flexibly set the active scan numbers from 1 to 2 by configuring the 'Max_Line_Num' in Dev_initial register. The time-multiplexing matrix timing sequence follows the Figure 7-2.

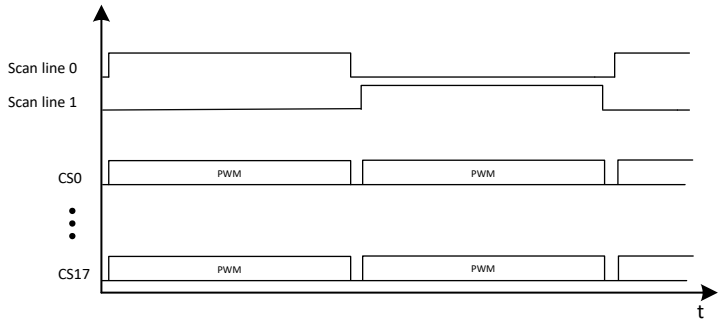


Figure 7-2. Time-Multiplexing Matrix Timing Sequence

One cycle time of the line switching can be calculated as below:

$$t_{line\_switch} = t_{PWM} + t_{SW\_BLK} + 2 \times t_{phase\_shift} \quad (1)$$

- t_{PWM} is the current sink active time, which equals to 8μs (PWM frequency set at 125kHz) or 16μs (PWM frequency set at 62.5kHz) by configuring 'PWM_Fre' in Dev_initial register.
- t_{SW_BLK} is the switch blank time, which equals to 1 us or 0.5μs by configuring 'SW_BLK' in Dev_config1 register.
- t_{phase_shift} is the PWM phase shift time, which equals to 0 or 125ns by configuring 'PWM_Phase_Shift' in Dev_config1 register.

Total display time for one complete sub-period is t_{sub_period} and it can be calculated by the following equation:

$$t_{sub\_period} = t_{line\_switch} \times Scan\_line\# \quad (2)$$

- Scan_line# is the scan line number determined by 'Max_Line_Num' in Dev_initial register.

The time-multiplexing matrix scheme time diagram is shown in Figure 7-3. The $t_{CS\_ON\_Shift}$ is the current sink turning on shift by configuring 'CS_ON_Shift' bit in Dev_config1 register.

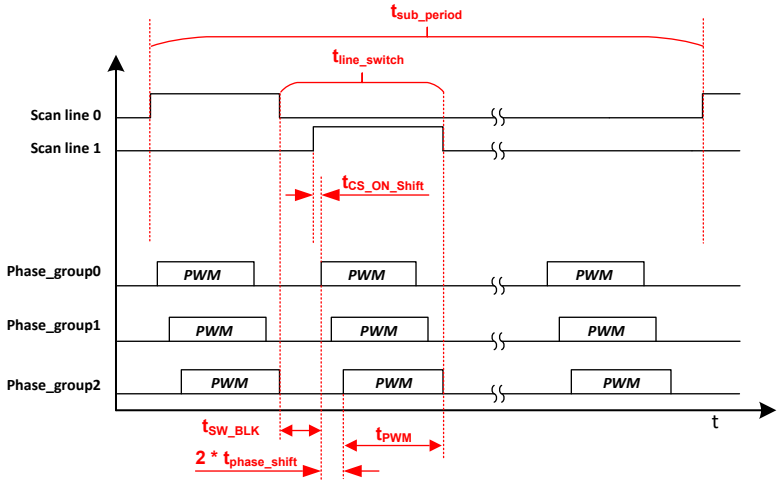


Figure 7-3. Time-Multiplexing Matrix Timing Diagram

The LP5862 device implements deghosting and low brightness compensation to remove the side effects of matrix topology:

- **Deghosting**: both upside deghosting and downside deghosting are implemented to eliminate the LED unexpected weak turn-on.
  - Upside_deghosting: discharge each scan line during its off state. By configuring the 'Up_Deghost' in Dev_config3 register, the LP5862 discharges and clamps the scan line switch to a certain voltage.
  - Downside_deghosting: pre-charge each current sink voltage during its off state. The deghosting capability can be adjusted through the 'Down_Deghost' in Dev_config3 register.
- **Low Brightness Compensation**: three groups compensation are implemented to overcome the color-shift and non-uniformity in low brightness conditions. The compensation capability can be through 'Comp_Group1', 'Comp_Group2', and 'Comp_Group3' in Dev_config2 register.
  - Compensation_group 1: CS0, CS3, CS6, CS9, CS12, CS15
  - Compensation_group 2: CS1, CS4, CS7, CS10, CS13, CS16
  - Compensation_group 3: CS2, CS5, CS8, CS11, CS14, CS17

7.3.2 Analog Dimming (Current Gain Control)

Analog dimming of LP5862 is achieved by configuring the current gain control. There are several methods to control the current gain of each LED.

- Global 3-bits Maximum Current (MC) setting without external resistor
- 3 Groups of 7-bits Color Current (CC) setting
- Individual 8-bit Dot Current (DC) setting

Global 3-Bits Maximum Current (MC) Setting

The MC is used to set the maximum current, I_{OUT_MAX}, for each current sink, and this current is the maximum peak current for each LED dot. The MC can be set with 3 bits (8 steps) from 3mA to 50mA. When the device is powered on, the MC data is set to default value, which is 15mA.

For data refresh Mode 1, MC data is effective immediately after new data updated. For Mode 2 and Mode 3, to avoid unexpected MC data change during high speed data refreshing, MC data must be changed when all channels are off and new MC data is only be updated when the 'Chip_EN' bit in Chip_en register is set to 0, and after the 'Chip_EN' returns to 1, the new MC data is effective. 'Down_Deghost' and 'Up_Deghost' in Dev_config3 work in the similar way with MC.

Table 7-1. Maximum Current (MC) Register Setting

3-BITS MAXIMUM_CURRENT REGISTER		I_{OUT_MAX}
Binary	Decimal	mA
000	0	3
001	1	5
010	2	10
011 (default)	3 (default)	15 (default)
100	4	20
101	5	30
110	6	40
111	7	50

3 Groups of 7-Bits Color Current (CC) Setting

The LP5862 device can adjust the output current of three color groups separately. For each color, it has 7-bits data in 'CC_Group1', 'CC_Group2', and 'CC_Group3'. Thus, all color group currents can be adjusted in 128 steps from 0% to 100% of the maximum output current, I_{OUT_MAX}.

The 18 current sinks have fixed mapping to the three color groups:

- CC-Group 1: CS0, CS3, CS6, CS9, CS12, CS15
- CC-Group 2: CS1, CS4, CS7, CS10, CS13, CS16
- CC-Group 3: CS2, CS5, CS8, CS11, CS14, CS17

Table 7-2. 3 Groups of 7-bits Color Current (CC) Setting

7-BITS CC_GROUP1/CC_GROUP2/CC_GROUP3 REGISTER		RATIO OF OUTPUT CURRENT TO I_{OUT_MAX}
Binary	Decimal	%
000 0000	0	0
000 0001	1	0.79
000 0010	2	1.57
- - -	- - -	- - -
100 0000 (default)	64 (default)	50.4 (default)
- - -	- - -	- - -
111 1101	125	98.4
111 1110	126	99.2
111 1111	127	100

Individual 8-bit Dot Current (DC) Setting

The LP5862 can individually adjust the output current of each LED by using dot current function through DC setting. The device allows the brightness deviations of the LEDs to adjusted be individually. Each output DC is programmed with a 8-bit depth, so the value can be adjusted with 256 steps within the range from 0% to 100% of (I_{OUT_MAX} × CC/127).

Table 7-3. Individual 8-bit Dot Current (DC) Setting

8-BIT DC REGISTER		RATIO OF OUTPUT CURRENT TO I_{OUT_MAX} × CC/127
Binary	Decimal	%
0000 0000	0	0
0000 0001	1	0.39
0000 0010	2	0.78
- - -	- - -	- - -
1000 0000 (default)	128 (default)	50.2 (default)

Table 7-3. Individual 8-bit Dot Current (DC) Setting (continued)

8-BIT DC REGISTER		RATIO OF OUTPUT CURRENT TO I_{OUT_MAX} × CC/127
Binary	Decimal	%
- - -	- - -	- - -
1111 1101	253	99.2
1111 1110	254	99.6
1111 1111	255	100

In summary, the current gain of each current sink can be calculated as below:

$$I_{OUT}\ (mA) = I_{OUT\_MAX} \times (CC/127) \times (DC/255) \quad (3)$$

For time-multiplexing scan scheme, if the scan number is N, each LED dot average current I_{AVG} is shown as below:

$$I_{AVG}\ (mA) = I_{OUT} / N = I_{OUT\_MAX} \times (CC/127) \times (DC/255)/N \quad (4)$$

7.3.3 PWM Dimming

There are several methods to control the PWM duty cycle of each LED dot.

- ***Individual 8-bit / 16-bit PWM for Each LED Dot***

  Every LED has an individual 8-bit or 16-bit PWM register that is used to change the LED brightness by PWM duty. The LP5862 uses an enhanced spectrum PWM (ES-PWM) algorithm to achieve 16-bit depth with high refresh rate and this can avoid flicker under high speed camera. Comparing with conventional 8-bit PWM, 16-bit PWM can help to achieve ultimate high dimming resolution in LED animation applications.
- ***3 Programmable Groups of 8-bit PWM Dimming***

  The group PWM Control is used to select LEDs into 1 to 3 groups where each group has a separate register for duty cycle control. Every LED has 2-bit selection in LED_DOT_GROUP Registers (x = 0, 1, … , 9) to select whether it belongs to one of the three groups or not:
  - 00: not a member of any group
  - 01: member of group 1
  - 10: member of group 2
  - 11: member of group 3
- ***8-bit PWM for Global Dimming***

  The Global PWM Control function affects all LEDs simultaneously.

The final PWM duty cycle can be calculated as below:

$$PWM\_Final(8\ bit) = PWM\_Individual(8\ bit) \times PWM\_Group(8\ bit) \times PWM\_\ Global(\ -bit) \quad (5)$$

$$PWM\_Final(16\ bit) = PWM\_Individual(16\ bit) \times PWM\_Group(8\ bit) \times PWM\_\ Global(8\ bit) \quad (6)$$

The LP5862 supports 125kHz or 62.5kHz PWM output frequency. The PWM frequency is selected by configuring the 'PWM_Fre' in Dev_initial register. An internal 32MHz oscillator is used for generating PWM outputs. The oscillator's high accuracy design (f_{OSC_ERR} ≤ ± 2%) enables a better synchronization if multiple LP5862 devices are connected together.

A PWM phase-shifting scheme is implemented in each current sink to avoid the current overshot when turning on simultaneously. As the LED drivers are not activated simultaneously, the peak load current from the pre-stage power supply is significantly decreased. This scheme also reduces input-current ripple and ceramic-capacitor audible ringing. LED drivers are grouped into three different phases. By configuring the 'PWM_Phase_Shift' in

Dev_config1 register, which is default off, the LP5862 supports t_{phase_shift} = 125ns shifting time shown in Figure 7-4.

- Phase 1: CS0, CS3, CS6, CS9, CS12, CS15
- Phase 2: CS1, CS4, CS7, CS10, CS13, CS16
- Phase 3: CS2, CS5, CS8, CS11, CS14, CS17

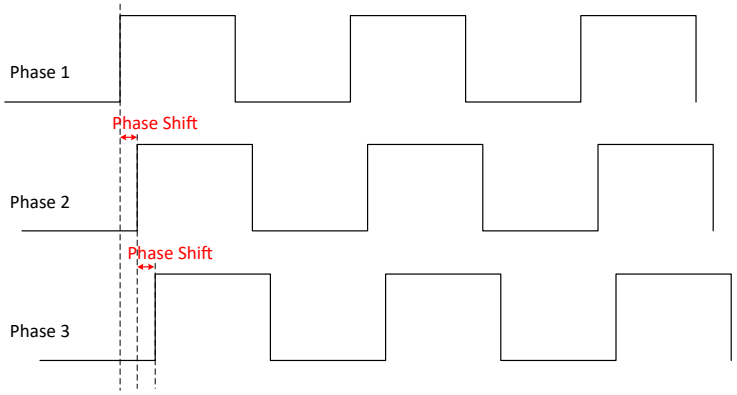


Figure 7-4. Phase Shift

To avoid high current sinks output ripple during line switching, current sinks can be configured to turn on with 1 clock delay (62.5ns or 31.25ns according to the PWM frequency) after lines turn on, as shown in Figure 7-3. This function an be configured by 'CS_ON_Shift' in Dev_config1 register.

The LP5862 allows users to configure the dimming scale either exponentially (Gamma Correction) or linearly through the 'PWM_Scale_Mode' in Dev_config1 register. If a human-eye-friendly dimming curve is desired, using the internal fixed exponential scale is an easy approach. If a special dimming curve is desired, using the linear scale with software correction is recommended. The LP5862 supports both linear and exponential dimming curves under 8-bit and 16-bit PWM depth. Figure 7-5 is an example of 8-bit PWM depth.

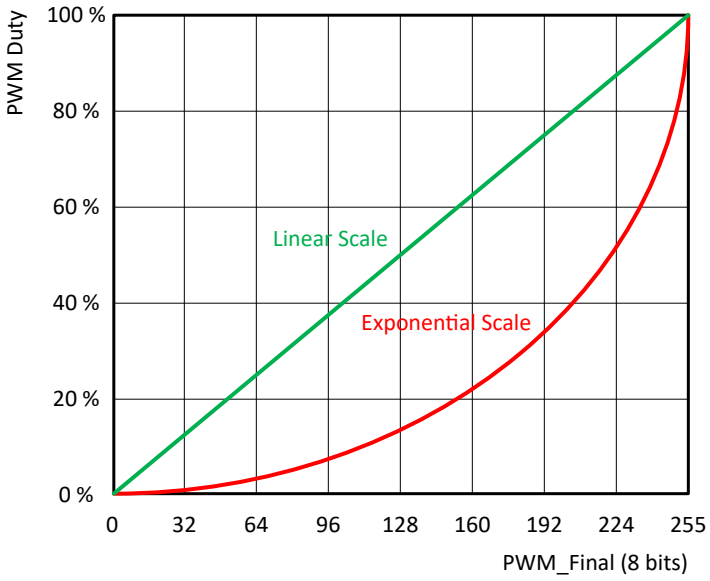


Figure 7-5. Linear and Exponential Dimming Curves

In summary, the PWM control method is illustrated as Figure 7-6:

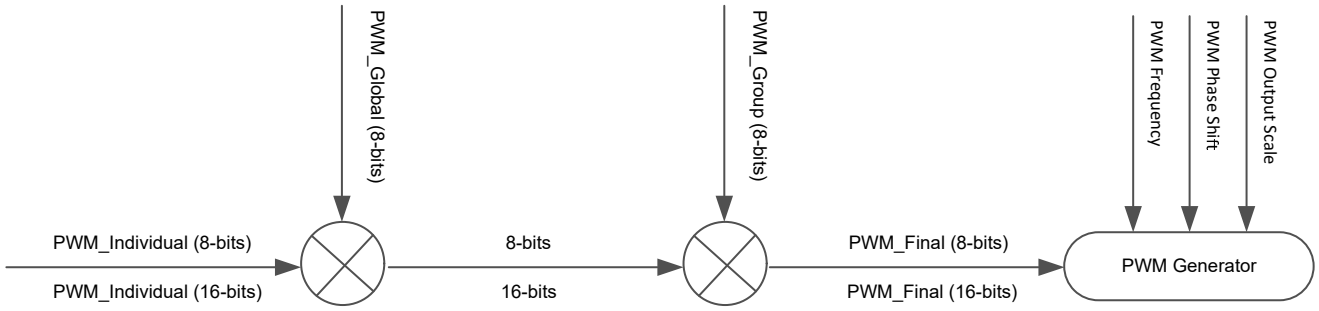


Figure 7-6. PWM Control Scheme

7.3.4 ON and OFF Control

The LP5862 device supports the individual ON and OFF control of each LED. For indication purpose, users can turn on and off the LED directly by writing 1-bit ON and OFF data to the corresponding Dot_onoffx (x = 0, 1, … , 5) register.

7.3.5 Data Refresh Mode

The LP5862 supports three data refresh modes: Mode 1, Mode 2, and Mode 3, by configuring 'Data_Ref_Mode' in Dev_initial register.

Mode 1: 8-bit PWM data without VSYNC command. Data is sent out for display instantly after received. With Mode 1, users can refresh the corresponding dots' data only instead of updating the whole SRAM. It is called ‘on demand data refresh’, which can save the total data volume effectively. As shown in Figure 7-7, the red LED dots can be refreshed after sending the corresponding data while the others kept the same with last frame.

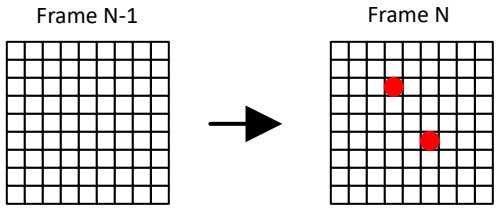


Figure 7-7. On Demand Data Refresh – Mode 1

Mode 2: 8-bit PWM data with VSYNC command. Data is held and sent out simultaneously by frame after receiving the VSYNC command.

Mode 3: 16-bit PWM data with VSYNC command. Data is held and sent out simultaneously by frame after receiving the VSYNC command.

Frame control is implemented in Mode 2 and Mode 3. Instead of refreshing the output instantly after data is received (Mode 1), the device holds the data and refreshes the whole frame data by a fixed frame rate, f_{VSYNC}. Usually, 24Hz, 50Hz, 60Hz, 120Hz or even higher frame rate is selected to achieve vivid animation effects. Whole SRAM Data Refresh is shown in Figure 7-8, a new frame is updated after receiving the VSYNC command.

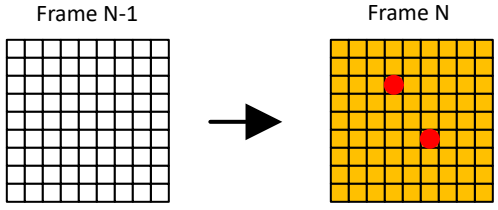


Figure 7-8. Whole SRAM Data Refresh

Comparing with Mode 1, Mode 2 and Mode 3 provide a better synchronization when multiple LP5862 devices used together. A high-level pulse width longer than t_{SYNC_H} is required at the beginning of each VSYNC frame. Figure 7-9 shows the VSYNC connections and Figure 7-10 shows the timing requirements.

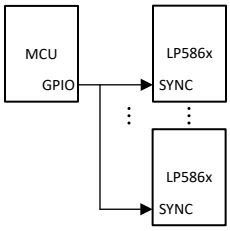


Figure 7-9. Multiple Devices Sync

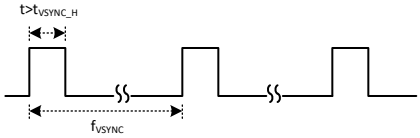


Figure 7-10. VSYNC Timing

Table 8-4 is the summary of the three data refresh modes.

Table 7-4. Data Refresh Mode

MODE TYPE	PWM RESOLUTION	PWM OUTPUT	EXTERNAL VSYNC
Mode 1	8 bits	Data update instantly	No
Mode 2	8 bits	Data update by frame	Yes
Mode 3	16 bits		

7.3.6 Full Addressable SRAM

SRAM is implemented inside the LP5862 device to support data writing and reading at the same time.

Although data refresh mechanisms are not the same for Mode 1 and Mode 2 and 3, the data writing and reading follow the same method. Uses can update partial of the SRAM data only or the whole SRAM page simultaneously. The LP5862 supports auto-increment function to minimize data traffic and increase data transfer efficiency.

Please be noted that 16-bit PWM (Mode 3) and 8-bit PWM (Mode 1 and Mode 2) are assigned with different SRAM addresses.

7.3.7 Protections and Diagnostics

LED Open Detection

The LP5862 includes LED open detection (LOD) for the fault caused by any opened LED dot. The threshold for LED open is 0.25V typical. LED open detection is only performed when PWM ≥ 25 (Mode 1 and Mode 2) or PWM ≥ 6400 (Mode 3) and voltage on CSn is detected lower than open threshold for continuously 4 sub-periods.

Figure 7-11 shows the detection circuit of LOD function. When open fault is detected, 'Global_LOD' bit in Fault_state register is set to 1 and detailed fault state for each LED is also monitored in register Dot_lodx (x = 0, 1, … , 5). All open fault indicator bits can be cleared by setting LOD_clear = 0Fh after the open condition is removed.

LOD removal function can be enabled by setting 'LOD_removal' bit in Dev_config2 register to 1. This function turns off the current sink of the open channel when scanning to the line where the opened LED is included.

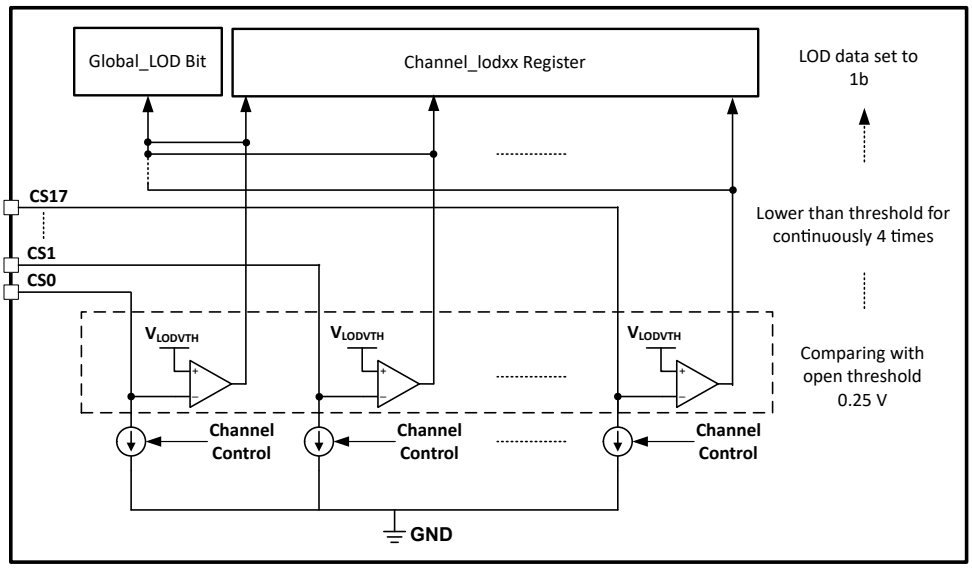


Figure 7-11. LOD Circuits

LED Short Detection

The LP5862 includes LED short detection (LSD) for the fault caused by any shorted LED. Threshold for channel short is (VLED – 1) V typical. LED short detection only performed when PWM ≥ 25 (Mode 1 and Mode 2)

or PWM ≥ 6400 (Mode 3) and voltage on CSn is detected higher than short threshold for continuously 4 sub-periods. As there is parasitic capacitance for the current sink, to make sure the LSD result is correct, TI recommends to set the LED current higher than 0.5mA.

Figure 7-12 shows the detection circuit of LSD function. When short fault is detected, 'Global_LSD bit' in Fault_state register is set to 1 and detailed fault state for every channel is also monitored in register Dot_lsdx (x = 0, 1, … , 5). All short fault indicator bits can be cleared by setting LSD_clear = 0Fh after the short condition is removed.

LSD removal function can be enabled by setting 'LSD_removal' bit in Dev_config2 register to 1. This function turns off the upside deghosting function of the scan line where short LED is included.

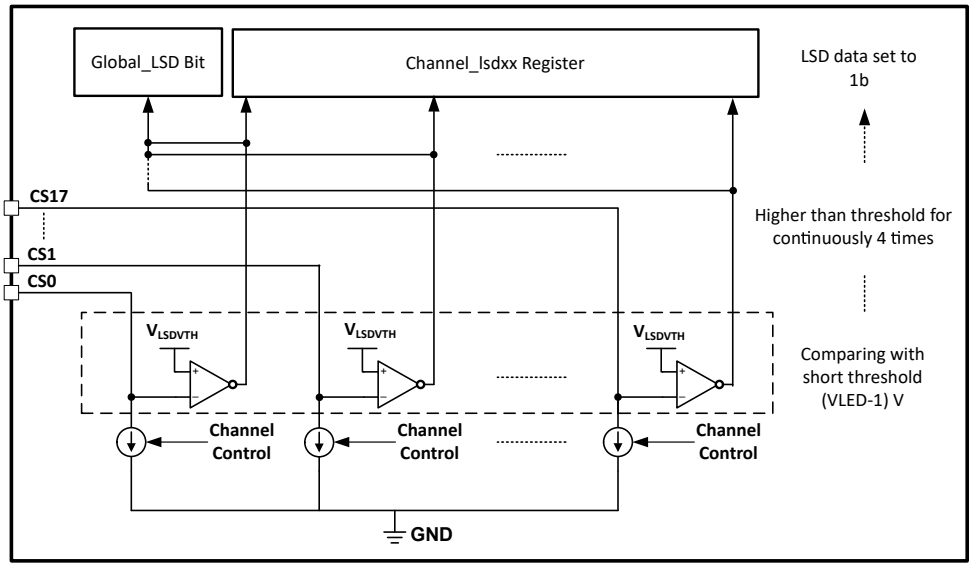


Figure 7-12. LSD Circuit

Thermal Shutdown

The LP5862 device implements thermal shutdown mechanism to protect the device from damage due to overheating. When the junction temperature rises to 160°C (typical) and above, the device switches into shutdown mode. The LP5862 exits thermal shutdown when the junction temperature of the device drops to 145°C (typical) and below.

UVLO (Undervoltage Lock Out)

The LP5862 has an internal comparator that monitors the voltage at VCC. When VCC is below V_{UVF}, reset is active and the LP5862 enters INITIALIZATION state.

7.4 Device Functional Modes

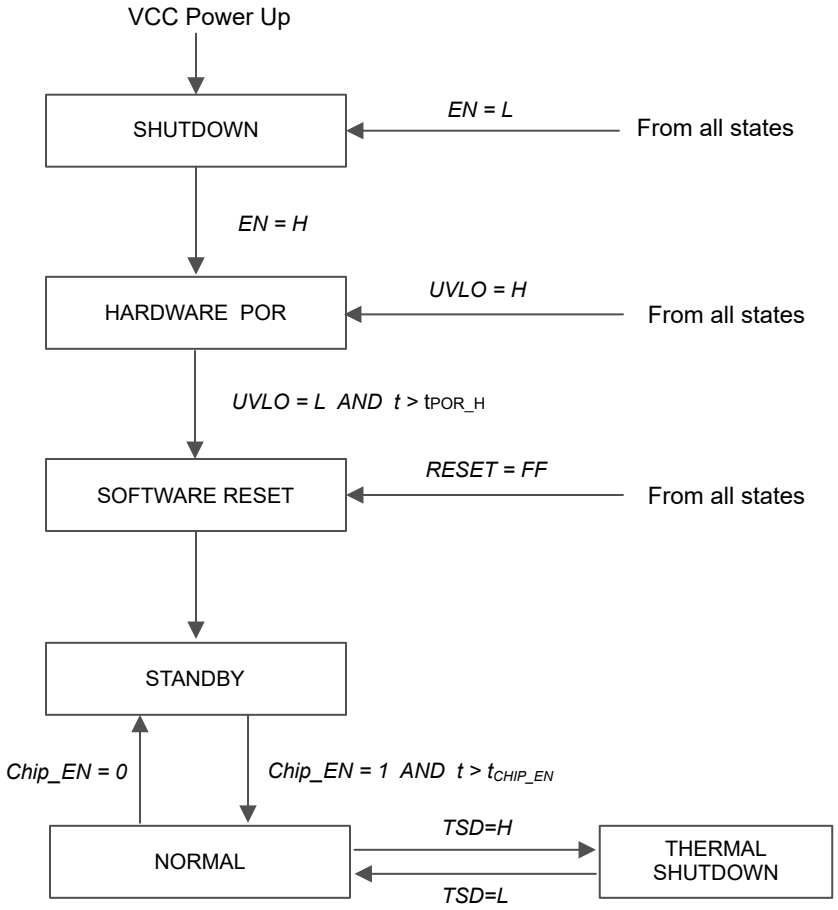


Figure 7-13. Device Functional Modes

- Shutdown: The device enters into shutdown mode from all states on VCC power up or EN pin is low.
- Hardware POR: The device enters into hardware POR when Enable pin is high or VCC fall under V_{UVF} causing UVLO = H from all states.
- Software reset: The device enters into software reset mode when VCC rise higher than V_{UVR} with the time t > t_{POR_H}. In this mode, all the registers are reset. Entry can also be from any state when the RESET (register) = FFh or UVLO is low.
- Standby: The device enters the standby mode when Chip_EN (register) = 0. In this mode, the device enters into low power mode, but the I^2C/SPI are still available for Chip_EN only and the register data is retained.
- Normal: The device enters the normal mode when 'Chip_EN' = 1 with the time t > t_{CHIP_EN}.
- Thermal shutdown: The device automatically enters the thermal shutdown mode when the junction temperature exceeds 160°C (typical). If the junction temperature decreases below 145°C (typical), the device returns to the normal mode.

7.5 Programming

Interface Selection

The LP5862 supports two communication interfaces: I²C and SPI. If IFS is high, the device enters into SPI mode. If IFS is low, the device enters into I²C mode.

Table 7-5. Interface Selection

INTERFACE TYPE	ENTRY CONDITION
I²C	IFS = Low
SPI	IFS = High

I²C Interface

The LP5862 is compatible with I²C standard specification. The device supports both fast mode (400-KHz maximum) and fast plus mode (1-MHz maximum).

I²C Data Transactions

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when clock signal is LOW. START and STOP conditions classify the beginning and the end of the data transfer session. A START condition is defined as the SDA signal transitioning from HIGH to LOW while SCL line is HIGH. A STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The bus leader always generates START and STOP conditions. The bus is considered to be busy after a START condition and free after a STOP condition. During data transmission, the bus leader can generate repeated START conditions. First START and repeated START conditions are functionally equivalent.

Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the leader. The leader releases the SDA line (HIGH) during the acknowledge clock pulse. The device pulls down the SDA line during the 9th clock pulse, signifying an acknowledge. The device generates an acknowledge after each byte has been received.

There is one exception to the acknowledge after every byte rule. When the leader is the receiver, it must indicate to the transmitter an end of data by not acknowledging (*negative acknowledge*) the last byte clocked out of the follower. This negative acknowledge still includes the acknowledge clock pulse (generated by the leader), but the SDA line is not pulled down.

I²C Data Format

The address and data bits are transmitted MSB first with 8-bits length format in each cycle. Each transmission is started with Address Byte 1, which are divided into 5-bits of the chip address, 2 higher bits of the register address, and 1 read and write bit. The other 8 lower bits of register address are put in Address Byte 2.The device supports both independent mode and broadcast mode. The auto-increment feature allows writing and reading several consecutive registers within one transmission. If not consecutive, a new transmission must be started.

Table 7-6. I²C Data Format

Address Byte 1	Chip Address					Register Address		R/W
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Independent	1	0	0	ADDR1	ADDR0	9th bit	8th bit	R: 1 W: 0
Broadcast	1	0	1	0	1			
Address Byte 2	Register Address							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	7th bit	6th bit	5th bit	4th bit	3th bit	2th bit	1th bit	0th bit

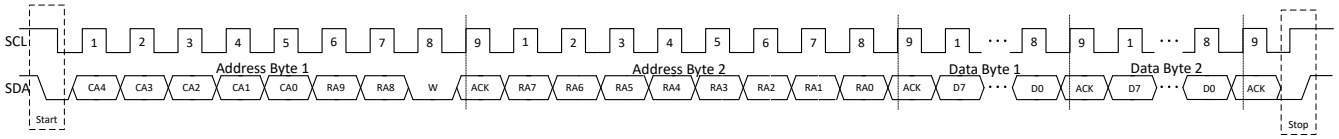


Figure 7-14. I²C Write Timming

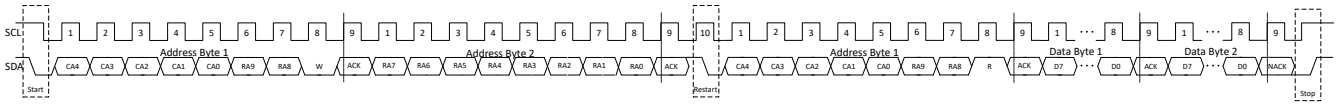


Figure 7-15. I²C Read Timing

Multiple Devices Connection

The LP5862 enters into I²C mode if IFS is connected to GND. The ADDR0/1 pin is used to select the unique I²C follower address for each device. The SCL and SDA lines must each have a pullup resistor (4.7 KΩ for 400 KHz, 2 KΩ for 1 MHz) placed somewhere on the line and remain HIGH even when the bus is idle. VIO_EN can either be connected with VIO power supply or GPIO. TI suggests to put one 1-nF cap as closer to VIO_EN pin as possible. Up to four LP5862 follower devices can share the same I²C bus by the different ADDR configurations.

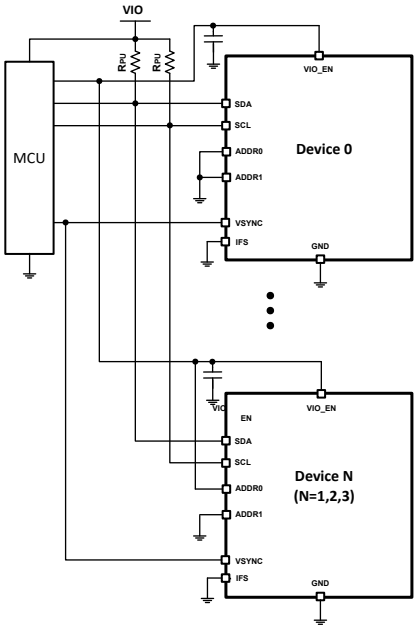


Figure 7-16. I²C Multiple Devices Connection

SPI Interface

The LP5862 is compatible with SPI serial-bus specification, and it operates as a follower. The maximum frequency supported by LP5862 is 12 MHz.

SPI Data Transactions

MISO output is normally in a high impedance state. When the follower-select pin SS for the device is active (low) the MISO output is pulled low for read only. During write cycle MISO stays in high-impedance state. The follower-select signal SS must be low during the cycle transmission. SS resets the interface when high. Data is clocked in on the rising edge of the SCLK clock signal, while data is clocked out on the falling edge of SCLK.

SPI Data Format

The address and data bits are transmitted MSB first with 8-bits length format in each cycle. Each transmission is started with Address Byte 1, which contains 8 higher bits of the register address. The Address Byte 2 is started with 2 lower bits of the register address and 1 read and write bit. The auto-increment feature allows writing and reading several consecutive registers within one transmission. If not consecutive, a new transmission must be started.

Table 7-7. SPI Data Format

Address Byte 1	**Register Address**							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
	9^{th} bit	8^{th} bit	7^{th} bit	6^{th} bit	5^{th} bit	4^{th} bit	3^{th} bit	2^{th} bit
Address Byte 2	**Register Address**							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
	1^{th} bit	0^{th} bit	R: 0 W: 1	Do not care				

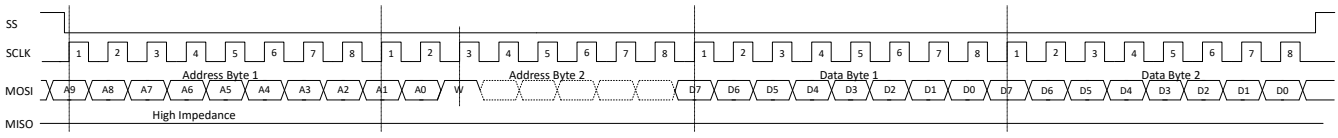


Figure 7-17. SPI Write Timing

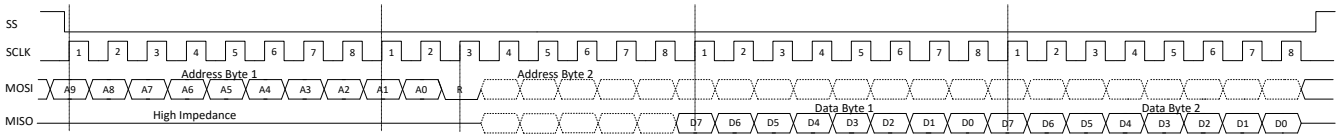


Figure 7-18. SPI Read Timing

Multiple Devices Connection

The device enters into SPI mode if IFS is pulled high to VIO through a pullup resistor (4.7 KΩ recommended). VIO_EN can either be connected with VIO power supply or GPIO. TI suggests to put one 1-nF cap as closer to VIO_EN pin as possible. In SPI mode host can address as many devices as there are follower select pins on host.

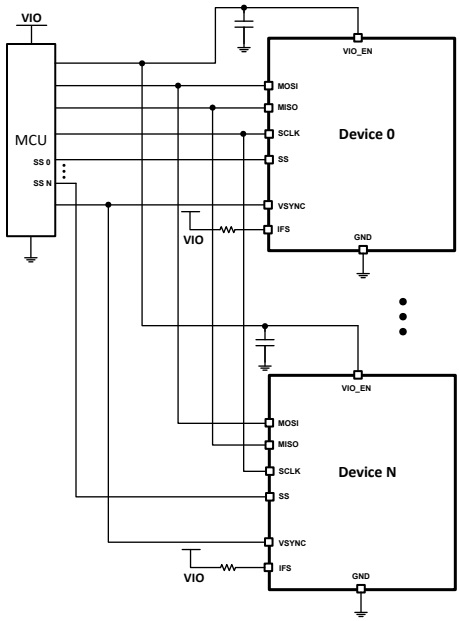


Figure 7-19. SPI Multiple Devices Connection

7.6 Register Maps

This section provides a summary of the register maps. For detailed register functions and descriptions, please refer to *LP5860 11x18 LED Matrix Driver Register Maps*.

Table 7-8. Register Section/Block Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
W0CP	W 0C P	W 0 to clear Requires privileged access
Reset or Default Value		
-n		Value after reset or the default value

Register Acronym	Address	Type	D7	D6	D5	D4	D3	D2	D1	D0	Default
Chip_en	000h	R/W	Reserved							Chip_EN	00h
Dev_initial	001h	R/W	Reserved	Max_Line_Num				Data_Ref_Mode		PWM_Fre	5Eh
Dev_config1	002h	R/W	Reserved	Reserved	Reserved	Reserved	SW_BLK	PWM_Scale_Mode	PWM_Phase_Shift	CS_ON_Shift	00h
Dev_config2	003h	R/W	Comp_Group3		Comp_Group2		Comp_Group1		LOD_removal	LSD_removal	00h
Dev_config3	004h	R/W	Down_Deghost		Up_Deghost		Maximum_Current			Up_Deghost_enable	47h

Global_bri	005h	R/W	PWM_Global							FFh
Group0_bri	006h	R/W	PWM_Group1							FFh
Group1_bri	007h	R/W	PWM_Group2							FFh
Group2_bri	008h	R/W	PWM_Group3							FFh
R_current_set	009h	R/W	Reserved	CC_Group1						40h
G_current_set	00Ah	R/W	Reserved	CC_Group2						40h
B_current_set	00Bh	R/W	Reserved	CC_Group3						40h
Dot_grp_sel0	00Ch	R/W	Dot L0-CS3 group		Dot L0-CS2 group		Dot L0-CS1 group		Dot L0-CS0 group	00h
Dot_grp_sel1	00Dh	R/W	Dot L0-CS7 group		Dot L0-CS6 group		Dot L0-CS5 group		Dot L0-CS4 group	00h
Dot_grp_sel2	00Eh	R/W	Dot L0-CS11 group		Dot L0-CS10 group		Dot L0-CS9 group		Dot L0-CS8 group	00h
Dot_grp_sel3	00Fh	R/W	Dot L0-CS15 group		Dot L0-CS14 group		Dot L0-CS13 group		Dot L0-CS12 group	00h
Dot_grp_sel4	010h	R/W	Reserved				Dot L0-CS17 group		Dot L0-CS16 group	00h
Dot_grp_sel5	011h	R/W	Dot L1-CS3 group		Dot L1-CS2 group		Dot L1-CS1 group		Dot L1-CS0 group	00h
Dot_grp_sel6	012h	R/W	Dot L1-CS7 group		Dot L1-CS6 group		Dot L1-CS5 group		Dot L1-CS4 group	00h
Dot_grp_sel7	013h	R/W	Dot L1-CS11 group		Dot L1-CS10 group		Dot L1-CS9 group		Dot L1-CS8 group	00h
Dot_grp_sel8	014h	R/W	Dot L1-CS15 group		Dot L1-CS14 group		Dot L1-CS13 group		Dot L1-CS12 group	00h
Dot_grp_sel9	015h	R/W	Reserved				Dot L1-CS17 group		Dot L1-CS16 group	00h
Dot_onoff0	043h	R/W	Dot L0-CS7 onoff	Dot L0-CS6 onoff	Dot L0-CS5 onoff	Dot L0-CS4 onoff	Dot L0-CS3 onoff	Dot L0-CS2 onoff	Dot L0-CS1 onoff	Dot L0-CS0 onoff	FFh
Dot_onoff1	044h	R/W	Dot L0-CS15onoff	Dot L0-CS14 onoff	Dot L0-CS13 onoff	Dot L0-CS12 onoff	Dot L0-CS11 onoff	Dot L0-CS10 onoff	Dot L0-CS9 onoff	Dot L0-CS8 onoff	FFh
Dot_onoff2	045h	R/W	Reserved						Dot L0-CS17 onoff	Dot L0-CS16 onoff	03h
Dot_onoff3	046h	R/W	Dot L1-CS7 onoff	Dot L1-CS6 onoff	Dot L1-CS5 onoff	Dot L1-CS4 onoff	Dot L1-CS3 onoff	Dot L1-CS2 onoff	Dot L1-CS1 onoff	Dot L1-CS0 onoff	FFh
Dot_onoff4	047h	R/W	Dot L1-CS15 onoff	Dot L1-CS14 onoff	Dot L1-CS13 onoff	Dot L1-CS12 onoff	Dot L1-CS11 onoff	Dot L1-CS10 onoff	Dot L1-CS9 onoff	Dot L1-CS8 onoff	FFh
Dot_onoff5	048h	R/W	Reserved						Dot L1-CS17 onoff	Dot L1-CS16 onoff	03h
Fault_state	064h	R	Reserved						Global_LOD	Global_LSD	00h
Dot_lod0	065h	R	Dot L0-CS7 LOD	Dot L0-CS6 LOD	Dot L0-CS5 LOD	Dot L0-CS4 LOD	Dot L0-CS3 LOD	Dot L0-CS2 LOD	Dot L0-CS1 LOD	Dot L0-CS0 LOD	00h
Dot_lod1	066h	R	Dot L0-CS15 LOD	Dot L0-CS14 LOD	Dot L0-CS13 LOD	Dot L0-CS12 LOD	Dot L0-CS11 LOD	Dot L0-CS10 LOD	Dot L0-CS9 LOD	Dot L0-CS8 LOD	00h
Dot_lod2	067h	R	Reserved						Dot L0-CS17 LOD	Dot L0-CS16 LOD	00h
Dot_lod3	068h	R	Dot L1-CS7 LOD	Dot L1-CS6 LOD	Dot L1-CS5 LOD	Dot L1-CS4 LOD	Dot L1-CS3 LOD	Dot L1-CS2 LOD	Dot L1-CS1 LOD	Dot L1-CS0 LOD	00h
Dot_lod4	069h	R	Dot L1-CS15 LOD	Dot L1-CS14 LOD	Dot L1-CS13 LOD	Dot L1-CS12 LOD	Dot L1-CS11 LOD	Dot L1-CS10 LOD	Dot L1-CS9 LOD	Dot L1-CS8 LOD	00h
Dot_lod5	06Ah	R	Reserved						Dot L1-CS17 LOD	Dot L1-CS16 LOD	00h
Dot_lsd0	086h	R	Dot L0-CS7 LSD	Dot L0-CS6 LSD	Dot L0-CS5 LSD	Dot L0-CS4 LSD	Dot L0-CS3 LSD	Dot L0-CS2 LSD	Dot L0-CS1 LSD	Dot L0-CS0 LSD	00h

Dot_lsd1	087h	R	Dot L0-CS15 LSD	Dot L0-CS14 LSD	Dot L0-CS13 LSD	Dot L0-CS12 LSD	Dot L0-CS11 LSD	Dot L0-CS10 LSD	Dot L0-CS9 LSD	Dot L0-CS8 LSD	00h
Dot_lsd2	088h	R	Reserved						Dot L0-CS17 LSD	Dot L0-CS16 LSD	00h
Dot_lsd3	089h	R	Dot L1-CS7 LSD	Dot L1-CS6 LSD	Dot L1-CS5 LSD	Dot L1-CS4 LSD	Dot L1-CS3 LSD	Dot L1-CS2 LSD	Dot L1-CS1 LSD	Dot L1-CS0 LSD	00h
Dot_lsd4	08Ah	R	Dot L1-CS15 LSD	Dot L1-CS14 LSD	Dot L1-CS13 LSD	Dot L1-CS12 LSD	Dot L1-CS11 LSD	Dot L1-CS10 LSD	Dot L1-CS9 LSD	Dot L1-CS8 LSD	00h
Dot_lsd5	08Bh	R	Reserved						Dot L1-CS17 LSD	Dot L1-CS16 LSD	00h
LOD_clear	0A7h	W	Reserved				LOD_Clear				00h
LSD_clear	0A8h	W	Reserved				LSD_Clear				00h
Reset	0A9h	W	Reset								00h
DC0	100h	R/W	LED dot current setting for Dot L0-CS0								80h
DC1	101h	R/W	LED dot current setting for Dot L0-CS1								80h
DC2	102h	R/W	LED dot current setting for Dot L0-CS2								80h
DC3	103h	R/W	LED dot current setting for Dot L0-CS3								80h
DC4	104h	R/W	LED dot current setting for Dot L0-CS4								80h
DC5	105h	R/W	LED dot current setting for Dot L0-CS5								80h
DC6	106h	R/W	LED dot current setting for Dot L0-CS6								80h
DC7	107h	R/W	LED dot current setting for Dot L0-CS7								80h
DC8	108h	R/W	LED dot current setting for Dot L0-CS8								80h
DC9	109h	R/W	LED dot current setting for Dot L0-CS9								80h
DC10	10Ah	R/W	LED dot current setting for Dot L0-CS10								80h
DC11	10Bh	R/W	LED dot current setting for Dot L0-CS11								80h
DC12	10Ch	R/W	LED dot current setting for Dot L0-CS12								80h
DC13	10Dh	R/W	LED dot current setting for Dot L0-CS13								80h
DC14	10Eh	R/W	LED dot current setting for Dot L0-CS14								80h
DC15	10Fh	R/W	LED dot current setting for Dot L0-CS15								80h
DC16	110h	R/W	LED dot current setting for Dot L0-CS16								80h
DC17	111h	R/W	LED dot current setting for Dot L0-CS17								80h
DC18	112h	R/W	LED dot current setting for Dot L1-CS0								80h
DC19	113h	R/W	LED dot current setting for Dot L1-CS1								80h
DC20	114h	R/W	LED dot current setting for Dot L1-CS2								80h
DC21	115h	R/W	LED dot current setting for Dot L1-CS3								80h
DC22	116h	R/W	LED dot current setting for Dot L1-CS4								80h
DC23	117h	R/W	LED dot current setting for Dot L1-CS5								80h
DC24	118h	R/W	LED dot current setting for Dot L1-CS6								80h
DC25	119h	R/W	LED dot current setting for Dot L1-CS7								80h
DC26	11Ah	R/W	LED dot current setting for Dot L1-CS8								80h
DC27	11Bh	R/W	LED dot current setting for Dot L1-CS9								80h
DC28	11Ch	R/W	LED dot current setting for Dot L1-CS10								80h
DC29	11Dh	R/W	LED dot current setting for Dot L1-CS11								80h
DC30	11Eh	R/W	LED dot current setting for Dot L1-CS12								80h
DC31	11Fh	R/W	LED dot current setting for Dot L1-CS13								80h
DC32	120h	R/W	LED dot current setting for Dot L1-CS14								80h

DC33	121h	R/W	LED dot current setting for Dot L1-CS15	80h
DC34	122h	R/W	LED dot current setting for Dot L1-CS16	80h
DC35	123h	R/W	LED dot current setting for Dot L1-CS17	80h
pwm_bri0	200h	R/W	8-bits PWM for Dot L0-CS0 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS0	00h
pwm_bri1	201h	R/W	8-bits PWM for Dot L0-CS1 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS0	00h
pwm_bri2	202h	R/W	8-bits PWM for Dot L0-CS2 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS1	00h
pwm_bri3	203h	R/W	8-bits PWM for Dot L0-CS3 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS1	00h
pwm_bri4	204h	R/W	8-bits PWM for Dot L0-CS4 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS2	00h
pwm_bri5	205h	R/W	8-bits PWM for Dot L0-CS5 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS2	00h
pwm_bri6	206h	R/W	8-bits PWM for Dot L0-CS6 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS3	00h
pwm_bri7	207h	R/W	8-bits PWM for Dot L0-CS7 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS3	00h
pwm_bri8	208h	R/W	8-bits PWM for Dot L0-CS8 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS4	00h
pwm_bri9	209h	R/W	8-bits PWM for Dot L0-CS9 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS4	00h
pwm_bri10	20Ah	R/W	8-bits PWM for Dot L0-CS10 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS5	00h
pwm_bri11	20Bh	R/W	8-bits PWM for Dot L0-CS11 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS5	00h
pwm_bri12	20Ch	R/W	8-bits PWM for Dot L0-CS12 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS6	00h
pwm_bri13	20Dh	R/W	8-bits PWM for Dot L0-CS13 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS6	00h
pwm_bri14	20Eh	R/W	8-bits PWM for Dot L0-CS14 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS7	00h
pwm_bri15	20Fh	R/W	8-bits PWM for Dot L0-CS15 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS7	00h
pwm_bri16	210h	R/W	8-bits PWM for Dot L0-CS16 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS8	00h
pwm_bri17	211h	R/W	8-bits PWM for Dot L0-CS17 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS8	00h
pwm_bri18	212h	R/W	8-bits PWM for Dot L1-CS0 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS9	00h
pwm_bri19	213h	R/W	8-bits PWM for Dot L1-CS1 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS9	00h
pwm_bri20	214h	R/W	8-bits PWM for Dot L1-CS2 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS10	00h
pwm_bri21	215h	R/W	8-bits PWM for Dot L1-CS3 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS10	00h
pwm_bri22	216h	R/W	8-bits PWM for Dot L1-CS4 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS11	00h
pwm_bri23	217h	R/W	8-bits PWM for Dot L1-CS5 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS11	00h
pwm_bri24	218h	R/W	8-bits PWM for Dot L1-CS6 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS12	00h
pwm_bri25	219h	R/W	8-bits PWM for Dot L1-CS7 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS12	00h
pwm_bri26	21Ah	R/W	8-bits PWM for Dot L1-CS8 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS13	00h
pwm_bri27	21Bh	R/W	8-bits PWM for Dot L1-CS9 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS13	00h
pwm_bri28	21Ch	R/W	8-bits PWM for Dot L1-CS10 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS14	00h
pwm_bri29	21Dh	R/W	8-bits PWM for Dot L1-CS11 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS14	00h
pwm_bri30	21Eh	R/W	8-bits PWM for Dot L1-CS12 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS15	00h
pwm_bri31	21Fh	R/W	8-bits PWM for Dot L1-CS13 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS15	00h
pwm_bri32	220h	R/W	8-bits PWM for Dot L1-CS14 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS16	00h
pwm_bri33	221h	R/W	8-bits PWM for Dot L1-CS15 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS16	00h
pwm_bri34	222h	R/W	8-bits PWM for Dot L1-CS16 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS17	00h
pwm_bri35	223h	R/W	8-bits PWM for Dot L1-CS17 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS17	00h
pwm_bri36	224h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L1-CS0	00h
pwm_bri37	225h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L1-CS0	00h
pwm_bri38	226h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L1-CS1	00h
pwm_bri39	227h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L1-CS1	00h
pwm_bri40	228h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L1-CS2	00h
pwm_bri41	229h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L1-CS2	00h
pwm_bri42	22Ah	R/W	16-bits PWM lower 8 bits [7:0] for Dot L1-CS3	00h
pwm_bri43	22Bh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L1-CS3	00h

pwm_bri44	22Ch	R/W	16-bits PWM lower 8 bits [7:0] for Dot L1-CS4	00h
pwm_bri45	22Dh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L1-CS4	00h
pwm_bri46	22Eh	R/W	16-bits PWM lower 8 bits [7:0] for Dot L1-CS5	00h
pwm_bri47	22Fh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L1-CS5	00h
pwm_bri48	230h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L1-CS6	00h
pwm_bri49	231h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L1-CS6	00h
pwm_bri50	232h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L1-CS7	00h
pwm_bri51	233h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L1-CS7	00h
pwm_bri52	234h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L1-CS8	00h
pwm_bri53	235h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L1-CS8	00h
pwm_bri54	236h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L1-CS9	00h
pwm_bri55	237h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L1-CS9	00h
pwm_bri56	238h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L1-CS10	00h
pwm_bri57	239h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L1-CS10	00h
pwm_bri58	23Ah	R/W	16-bits PWM lower 8 bits [7:0] for Dot L1-CS11	00h
pwm_bri59	23Bh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L1-CS11	00h
pwm_bri60	23Ch	R/W	16-bits PWM lower 8 bits [7:0] for Dot L1-CS12	00h
pwm_bri61	23Dh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L1-CS12	00h
pwm_bri62	23Eh	R/W	16-bits PWM lower 8 bits [7:0] for Dot L1-CS13	00h
pwm_bri63	23Fh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L1-CS13	00h
pwm_bri64	240h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L1-CS14	00h
pwm_bri65	241h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L1-CS14	00h
pwm_bri66	242h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L1-CS15	00h
pwm_bri67	243h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L1-CS15	00h
pwm_bri68	244h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L1-CS16	00h
pwm_bri69	245h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L1-CS16	00h
pwm_bri70	246h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L1-CS17	00h
pwm_bri71	247h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L1-CS17	00h

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LP5862 integrates 18 constant current sinks with 2 switching FETs and one LP5862 can drive up to 36 LED dots or 12 RGB pixels and achieve great dimming effect. In smart home, gaming keyboards, and other human-machine interaction applications, the device can greatly improve user experience with small amount of components.

8.2 Typical Application

8.2.1 Application

Figure 8-1 shows an example of typical application, which uses one LP5862 to drive 12 common-anode RGB LEDs through I^2C communication.

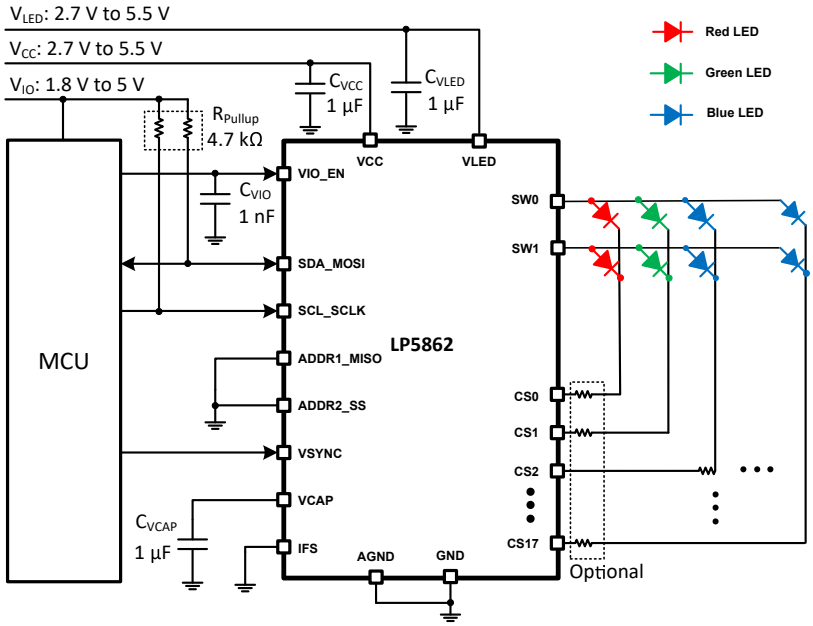


Figure 8-1. Typical Application - LP5862 Driving 36 RGB LEDs (12 LED Dots)

8.2.2 Design Requirements

Table 8-1. Design Parameters

PARAMETER	VALUE
VCC / VIO	3.3V
VLED	5V
RGB LED count	12
Scan number	2
Interface	I^2C
LED maximum average current (red, green, blue)	22mA, 16.5mA, 11mA
LED maximum peak current (red, green, blue)	44mA, 33mA, 22mA

8.2.3 Detailed Design Procedure

LP5862 requires an external capacitor C_{VCAP}, whose value is 1μF connected from V_{CAP} to GND for proper operation of internal LDO. The external capacitor must be placed as close to the device as possible.

TI recommends 1μF capacitors be placed between VCC/VLED with GND, and 1nF capacitor placed between VIO with GND. Place the capacitors as close to the device as possible.

Pullup resistors $R_{pull-up}$ are requirement for SCL and SDA when using I^2C as communication method. In typical applications, TI recommends 1.8kΩ to 4.7kΩ resistors.

To decrease thermal dissipation from device to ambient, resistors R_{CS} can optionally be placed in serial with the LED. Voltage drop on these resistors must leave enough margins for VSAT to ensure the device works normally.

8.2.3.1 Program Procedure

When selecting data refresh Mode 1, outputs are refreshed instantly after data is received.

When selecting data refresh Mode 2 and 3, VSYNC signal is required for synchronized display. Programming flow is showed as Figure 8-2. To display full pixel of last frame, VSYNC pulse must be sent to the device after the end of last PWM. Time between two pulses t_{SYNC} must be larger than the whole PWM time of all Dots t_{frame}. Common selection like 60Hz, 90Hz, 120Hz or even higher refresh frequency an be supported. High pulse width longer than t_{SYNC_H} is required at the beginning of each VSYNC frame, and data must not be write to PWM registers during high pulse width.

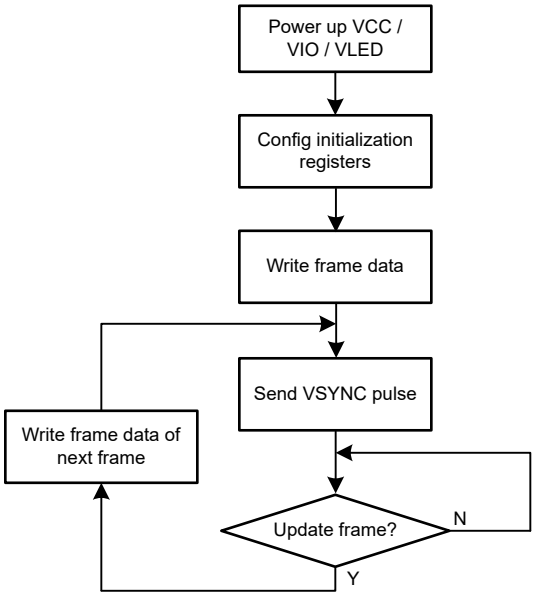


Figure 8-2. Program Procedure

9 Power Supply Recommendations

VDD Input Supply Recommendations

LP5862 is designed to operate from a 2.7V to 5.5V VDD voltage supply. This input supply must be well regulated and be able to provide the peak current required by the LED matrix. The resistance of the VDD supply rail must be low enough such that the input current transient does not cause the LP5862 VDD supply voltage to drop below the maximum POR voltage.

VLED Input Supply Recommendations

LP5862 is designed to operate with a 2.7V to 5.5V VLED voltage supply. The VLED supply must be well regulated and able to provide the peak current required by the LED configuration without voltage drop, under load transients like start-up or rapid brightness change. The resistance of the input supply rail must be low enough so that the input current transient does not cause the VLED supply voltage to drop below LED V_f + VSAT voltage.

VIO Input Supply Recommendations

LP5862 is designed to operate with a 1.65V to 5.5V VIO_EN voltage supply. The VIO_EN supply must be well regulated and able to provide the peak current required by the LED configuration without voltage drop under load transients like start-up or rapid brightness change.

10 Layout

10.1 Layout Guidelines

the below guidelines for layout design can help to get a better on-board performance.

- The decoupling capacitors C_{VCC} and C_{VLED} for power supply must be close to the chip to have minimized the impact of high-frequency noise and ripple from power. C_{VCAP} for internal LDO must be put as close to chip as possible. GND plane connections to C_{VLED} and GND pins must be on TOP layer copper with multiple vias connecting to system ground plane. C_{VIO} for internal enable block also must be put as close to chip as possible.
- The exposed thermal pad must be well soldered to the board, which can have better mechanical reliability. This action can optimize heat transfer so that increasing thermal performance. AGND pin must be connected to thermal pad and system ground.
- The major heat flow path from the package to the ambient is through copper on the PCB. Several methods can help thermal performance. Below exposed thermal pad of IC, putting much vias through the PCB to other ground layer can dissipate more heat. Maximizing the copper coverage on the PCB can increase the thermal conductivity of the board.
- Low inductive and resistive path of switch load loop can help to provide a high slew rate. Therefore, path of VLED – SWx must be short and wide and avoid parallel wiring and narrow trace. Transient current in SWx pins is much larger than CSy pins, so that trace for SWx must be wider than CSy.

10.2 Layout Example

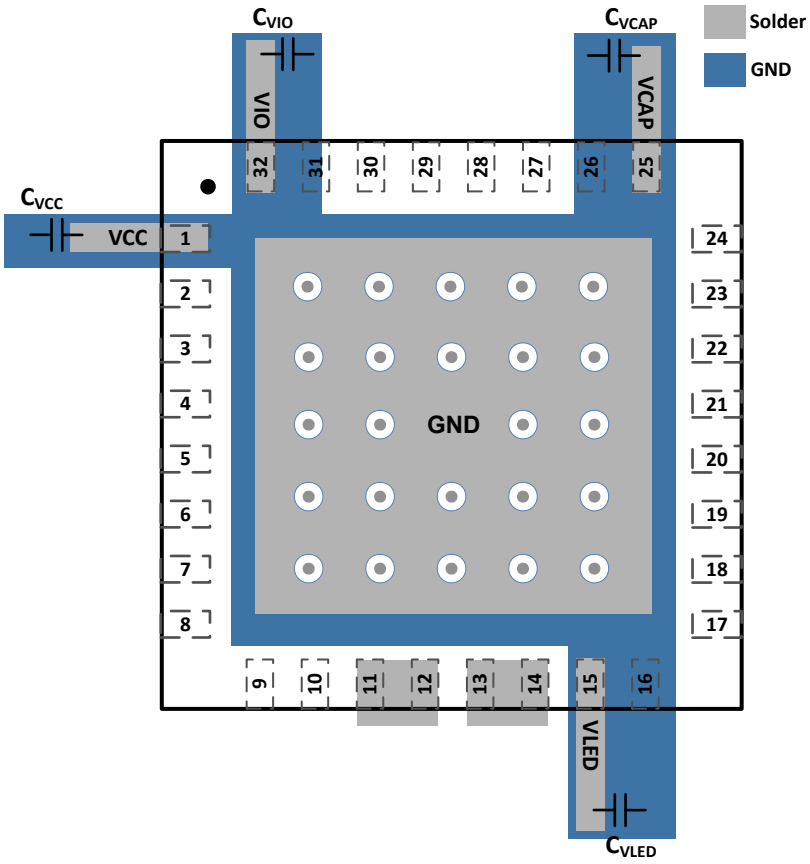


Figure 10-1. LP5862RSMR Layout Example

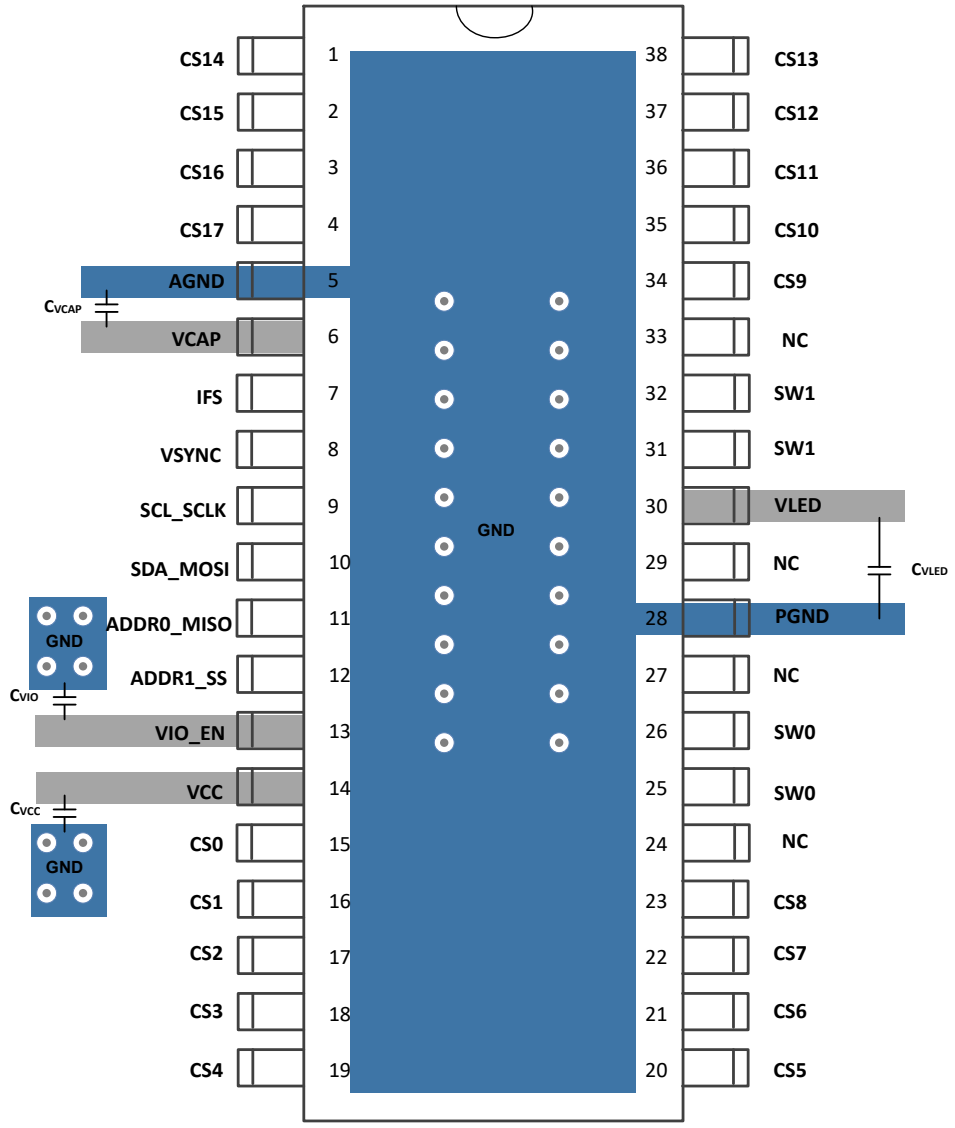


Figure 10-2. LP5862DBTR Layout Example

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 Trademarks

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All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2021) to Revision A (June 2025)	Page
• Added DBT package information in the *Device Information* table	1
• Added DBT package information	4
• Corrected pin name and count in Figure 5-1	4
• Added thermal information of DBT package	7
• Modified I^2C timing requirements	7

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP5862DBTR	Active	Production	TSSOP (DBT) | 38	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LP5862DBTR
LP5862DBTR.A	Active	Production	TSSOP (DBT) | 38	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LP5862DBTR
LP5862RSMR	Active	Production	VQFN (RSM) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LP5862
LP5862RSMR.A	Active	Production	VQFN (RSM) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LP5862

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

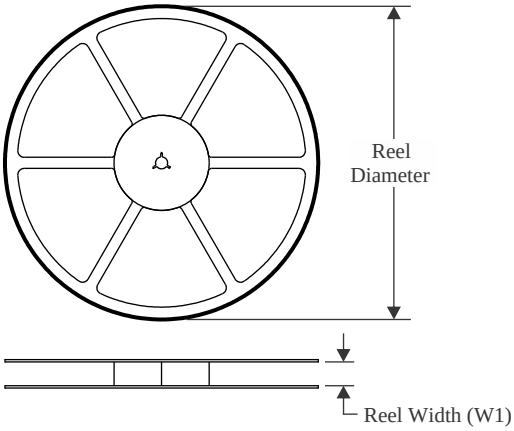
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

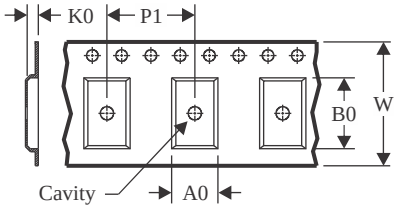
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

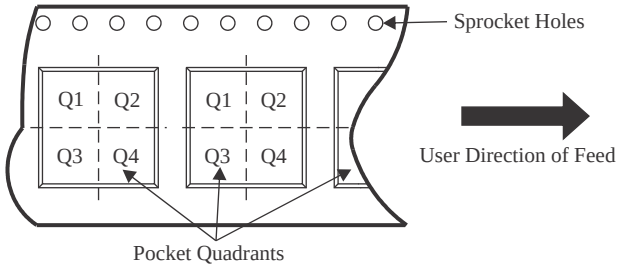


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

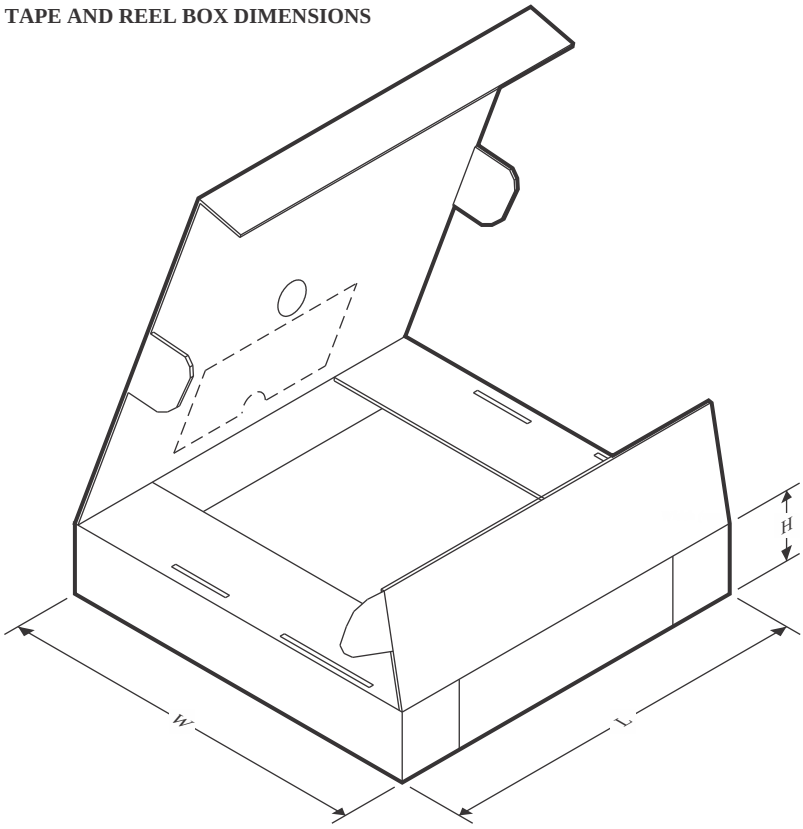
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5862DBTR	TSSOP	DBT	38	2000	330.0	16.4	6.75	10.1	1.8	12.0	16.0	Q1
LP5862RSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5862DBTR	TSSOP	DBT	38	2000	353.0	353.0	32.0
LP5862RSMR	VQFN	RSM	32	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

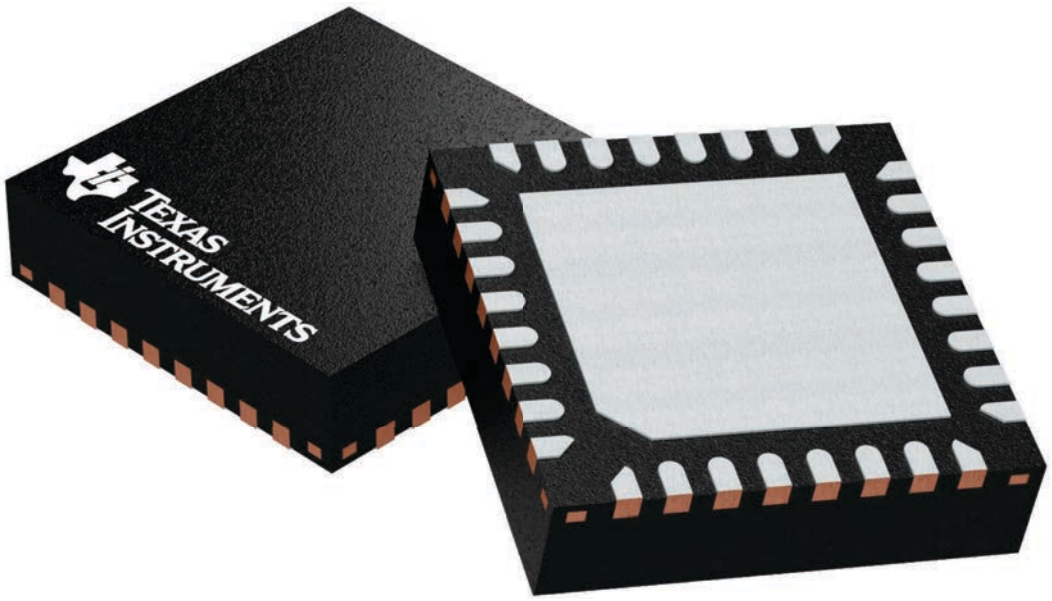
RSM 32

VQFN - 1 mm max height

4 x 4, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



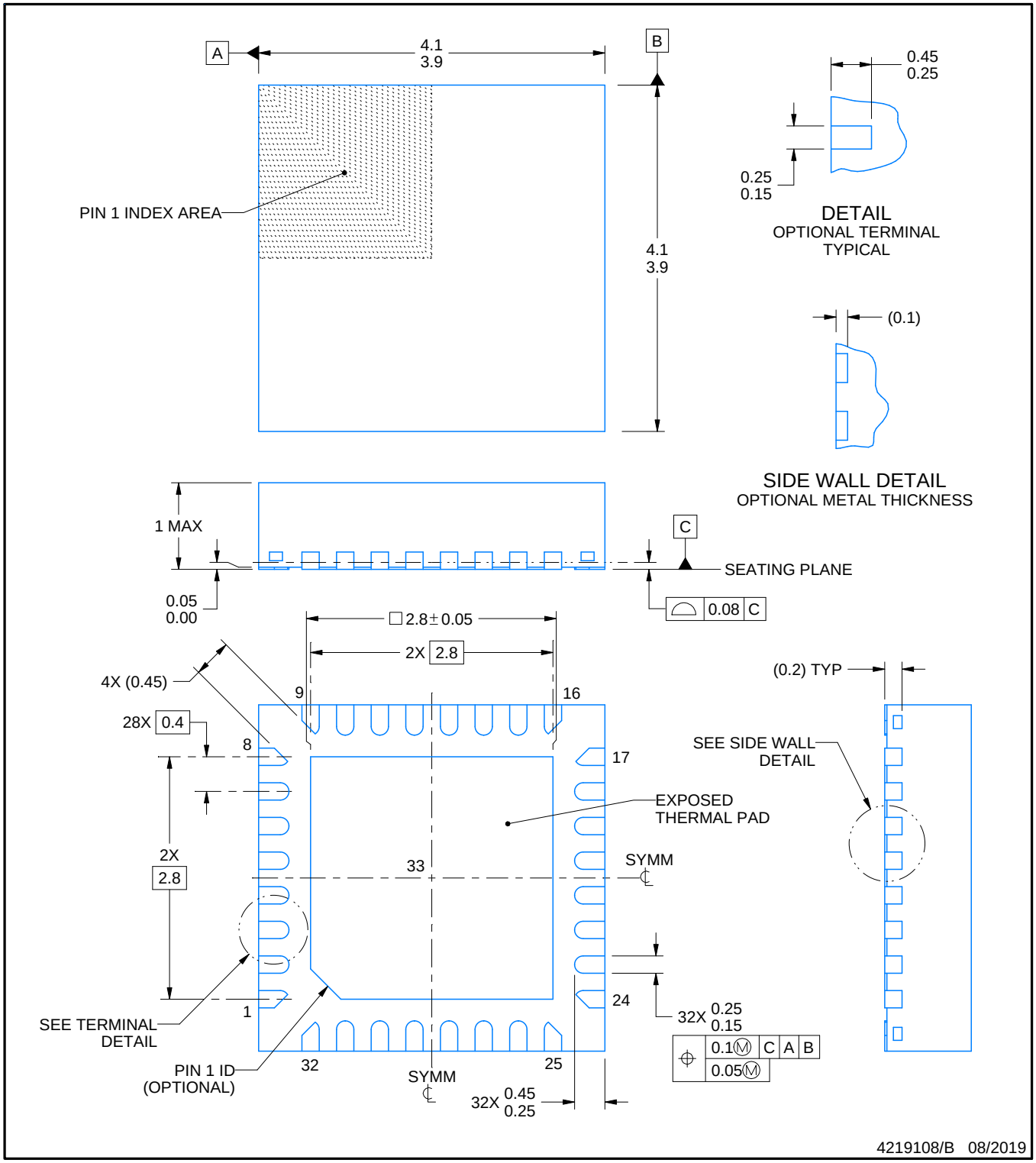
4224982/A

PACKAGE OUTLINE

RSM0032B

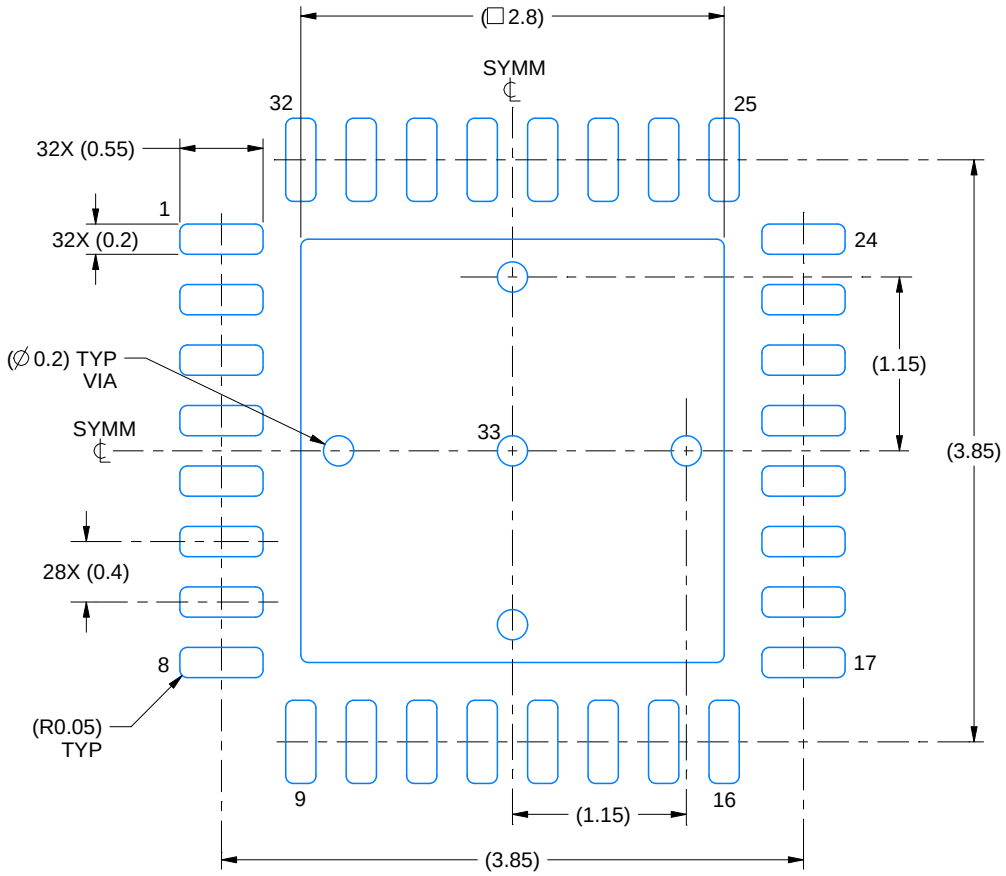
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

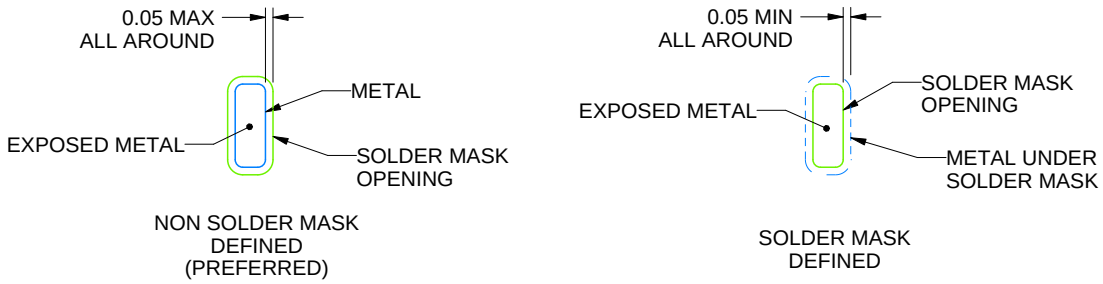


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

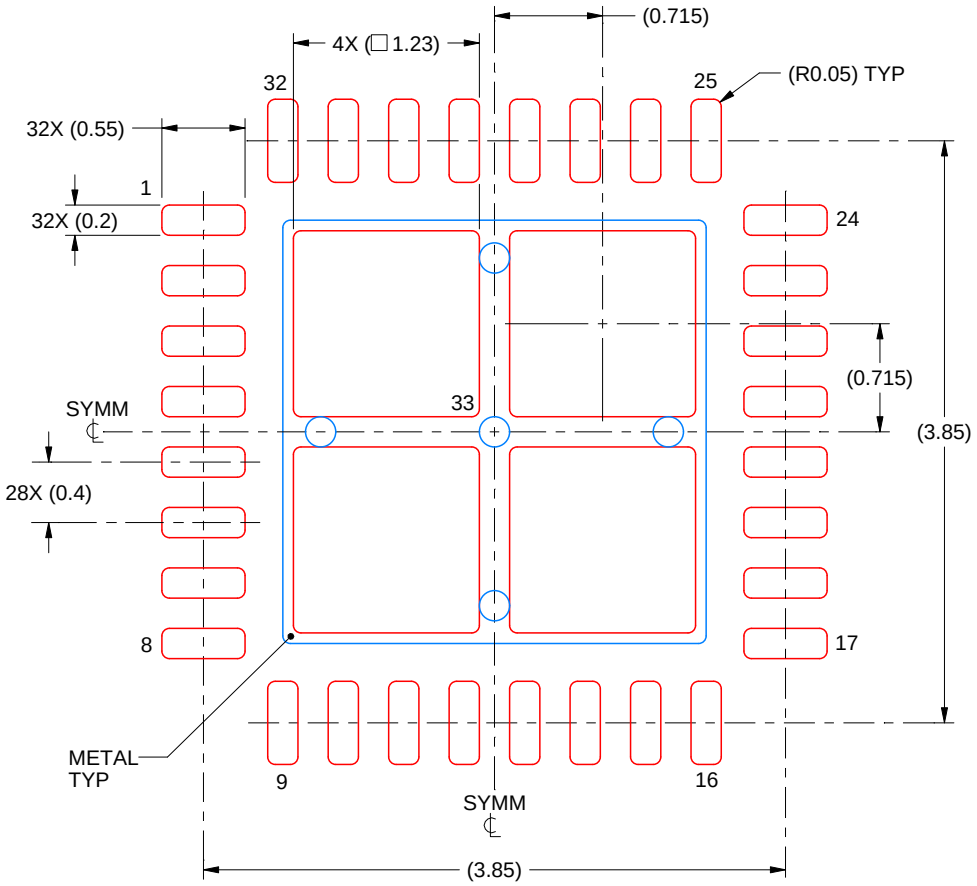


SOLDER MASK DETAILS

4219108/B 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 33:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219108/B 08/2019

NOTES: (continued)

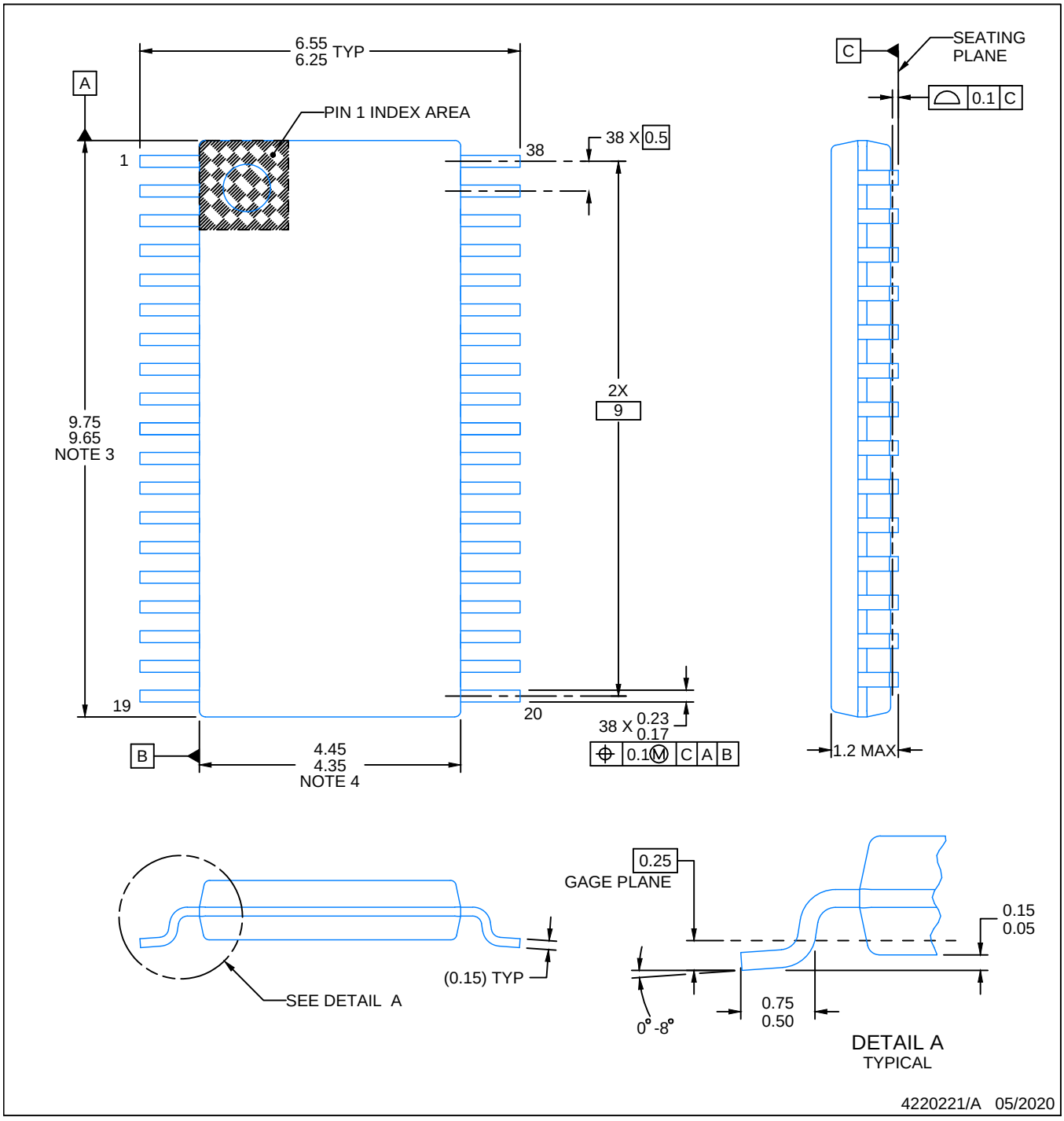
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DBT0038A

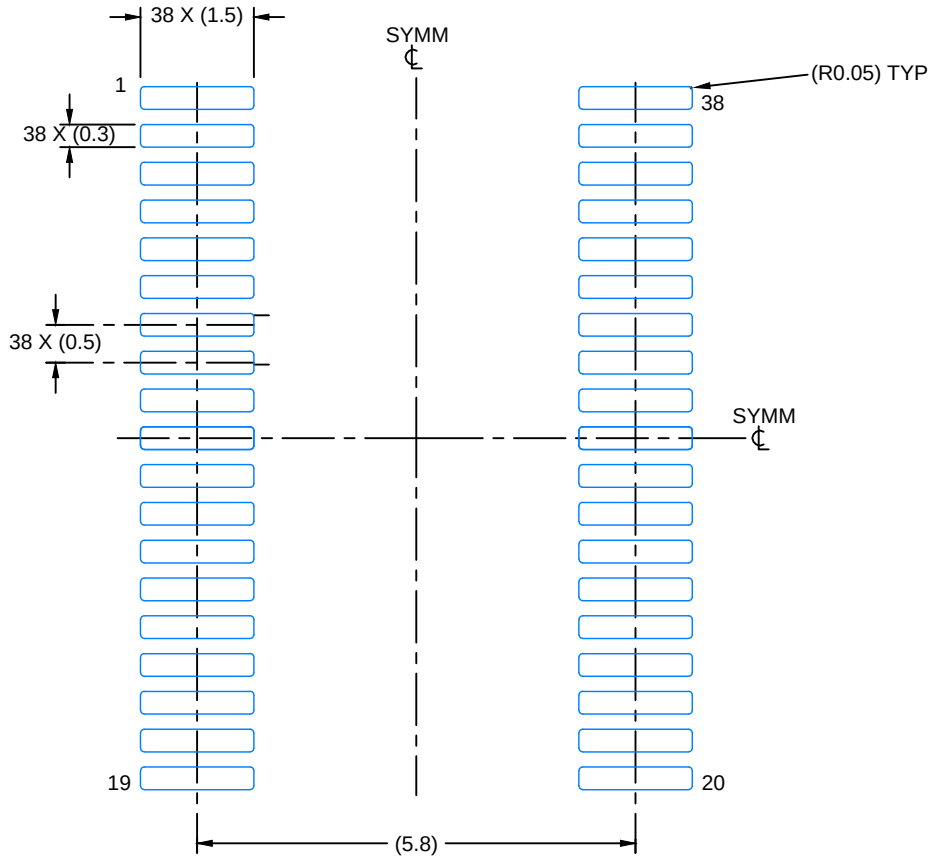
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

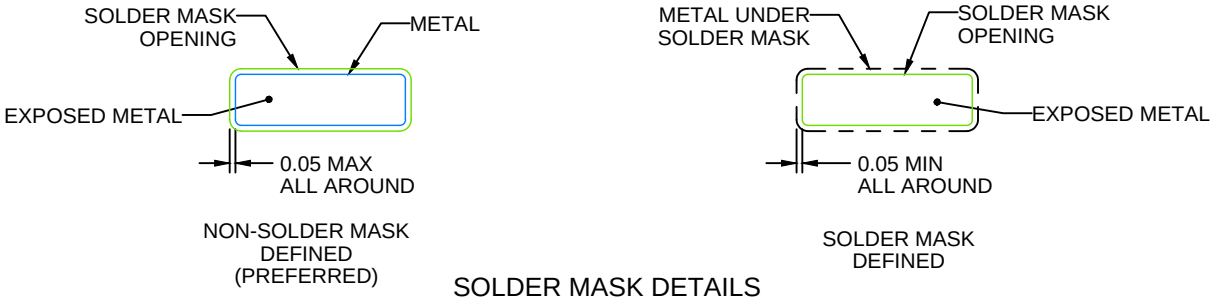


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

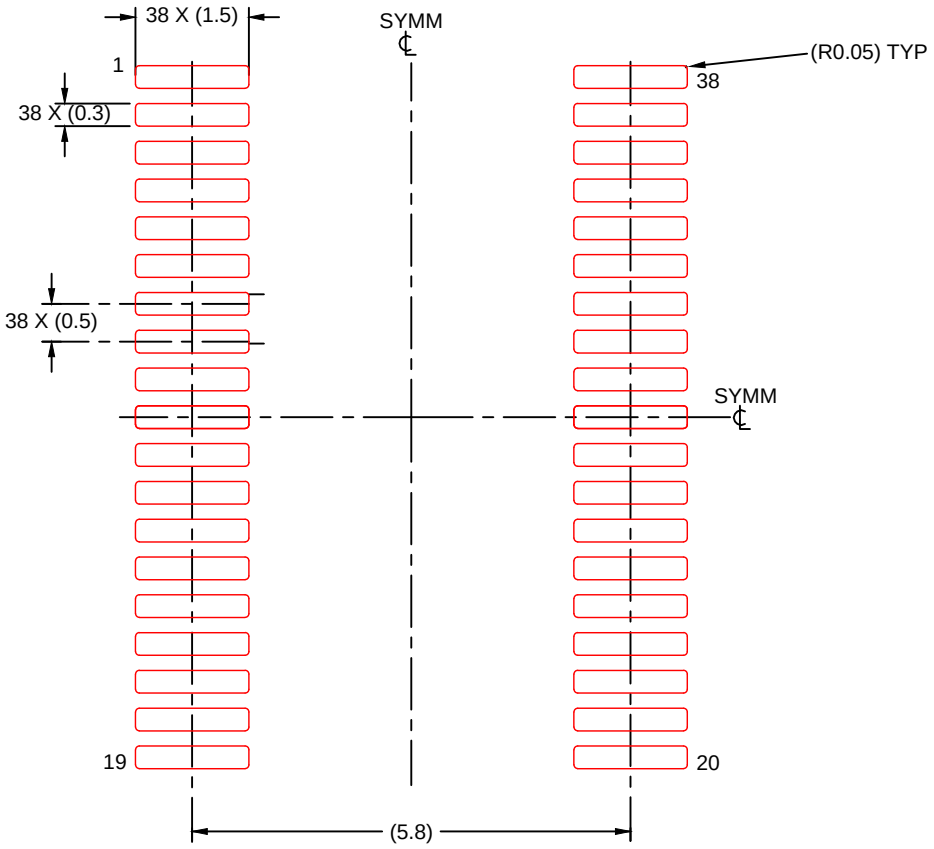


SOLDER MASK DETAILS

4220221/A 05/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220221/A 05/2020

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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