LP38513 3-A Fast Response Ultra-Low Dropout Linear Regulator

1 Features

- Input Supply Voltage 2.25 V to 5.5 V
- Conversions from 2.5-V Rail to 1.8-V Rail
- Stable with Ceramic Capacitors
- Low Ground Pin Current
- Load Regulation of 0.1% for 10 mA to 3-A Load Current
- 60-µA Typical Quiescent Current in Shutdown Mode
- Specified Output Current of 3 A
- Specified V_{OUT} Accuracy of ±2.6% With T_J from 0°C to +125°C
- $\overline{\text{ERROR}}$ Flag Indicates V_{OUT} Status
- Overtemperature and Overcurrent Protection
- −40°C to +125°C Operating T_J Range

2 Applications

- Microprocessor Power Supplies
- GTL, GTL+, BTL, and SSTL Bus Terminators
- Power Supplies for DSPs
- SCSI Terminator
- Post Regulators
- Battery Chargers
- Other Battery Powered Applications

3 Description

The LP38513 fast-response ultra-low dropout linear regulator operates from a 2.25-V to 5.5-V input supply. This device responds very quickly to step changes in line or load conditions, making it suitable for low-voltage microprocessor applications. Developed on a CMOS process, with a PMOS pass transistor, the LP38513 has low quiescent-current operation independent of the output load current.

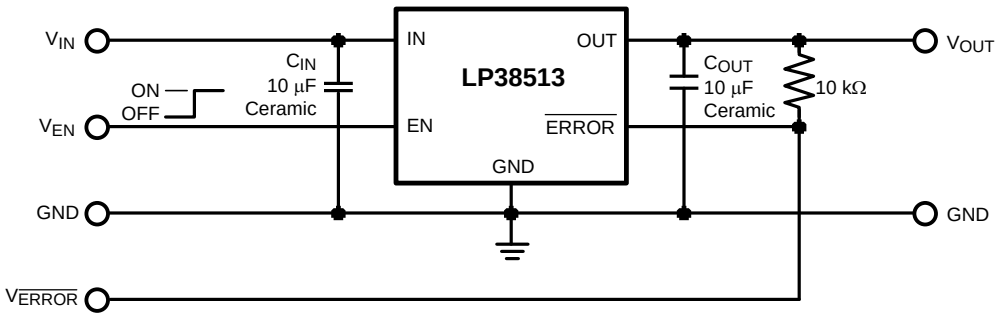
- Ground Pin Current: Typically 12 mA at 3-A load current.
- Disable Mode: Typically 60 µA quiescent current when the enable (EN) pin is pulled low.
- $\overline{\text{ERROR}}$ Flag: The $\overline{\text{ERROR}}$ flag goes low if V_{OUT} falls more than typically 15% below the nominal value.
- Precision Output Voltage: A specified V_{OUT} accuracy of ±2.6% with T_J from 0°C to 125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP38513	TO-220 (5)	14.986 mm × 10.16 mm
	DDPAK/TO-263 (5)	10.16 mm × 8.42 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (April 2013) to Revision E — **Page**

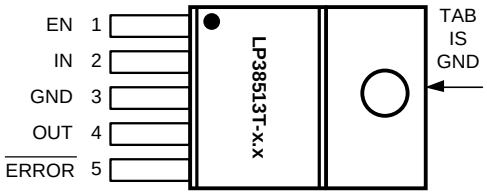
- Added *Device Information* and *Pin Configuration and Functions* sections, *ESD Ratings* table, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections ... 1
- Deleted lead temp from Abs Max - it is in POA ... 4
- Added updated thermal information ... 4
- Deleted out-of-date heat sinking subsection ... 14

Changes from Revision C (April 2013) to Revision D — **Page**

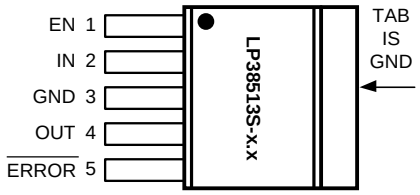
- Changed layout of National Data Sheet to TI format ... 14

5 Pin Configuration and Functions

NDH Package
5-Pin TO-220
Top View



KTT Package
5-Pin DDPAK/TO-263
Top View



Pin Functions for TO-220 and DDPAK/TO-263 Packages

PIN		TYPE	DESCRIPTION
NUMBER	NAME		
1	EN	I	Enable. Pull high to enable the output, low to disable the output. This pin has no internal bias and must be tied to the input voltage, or actively driven.
2	IN	I	Input supply pin
3	GND	G	Ground
4	OUT	O	Regulated output voltage pin
5	$\overline{\text{ERROR}}$	O	$\overline{\text{ERROR}}$ flag. A high level indicates that V_{OUT} is within 15% of the nominal regulated voltage.
TAB	TAB	G	The TO-220 and DDPAK/TO-263 TAB is used as a thermal connection to remove heat from the device to an external heat sink. The TAB is internally connected to device pin 3.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
IN pin voltage (survival)	−0.3	6	V
EN pin voltage (survival)	−0.3	6	V
OUT pin Voltage (survival)	−0.3	6	V
$\overline{\text{ERROR}}$ pin voltage (survival)	−0.3	6	V
I_{OUT} (Survival)	Internally limited		
Power dissipation(3)	Internally limited		
Storage temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, contact the TI Sales Office/ Distributors for availability and specifications.
(3) Device operation must be evaluated, and derated as needed, based on ambient temperature (T_A), power dissipation (P_D), maximum allowable operating junction temperature ($T_{J(MAX)}$), and package thermal resistance ($R_{\theta JA}$).

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	NOM	MAX	UNIT
Input supply voltage, V_{IN}	2.25		5.5	V
Enable input voltage, V_{EN}	0		5.5	V
$\overline{\text{ERROR}}$ pin voltage	0		V_{IN}	V
Output current (DC)	0		3	mA/A
Junction temperature(2)	−40		125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Device operation must be evaluated, and derated as needed, based on ambient temperature (T_A), power dissipation (P_D), maximum allowable operating junction temperature ($T_{J(MAX)}$), and package thermal resistance ($R_{\theta JA}$).

6.4 Thermal Information

THERMAL METRIC(1)		LP38513		UNIT
		NDH (TO-220)	KTT (DDPAK/TO-263)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.9	32.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.7	37.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.4	18.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.3	5.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	16.4	17.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.2	1.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Unless otherwise specified: V_{IN} = 2.5 V, I_{OUT} = 10 mA, C_{IN} = 10 µF, C_{OUT} = 10 µF, V_{EN} = 2 V, and limits apply for T_J = 25°C. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Output voltage tolerance(1)	2.25 V ≤ V_{IN} ≤ 5.5 V 10 mA ≤ I_{OUT} ≤ 3 A	–1.6%	0%	1.6%	
		2.25 V ≤ V_{IN} ≤ 5.5 V 10 mA ≤ I_{OUT} ≤ 3 A T_J = –40°C to +125°C	–4.1%		2.6%	
		2.25V ≤ V_{IN} ≤ 5.5V 10 mA ≤ I_{OUT} ≤ 3A 0°C ≤ T_J ≤ 125°C	–2.6%	0%	2.6%	
$\Delta V_{OUT}/\Delta V_{IN}$	Output voltage line regulation(1)(2)	2.25 V ≤ V_{IN} ≤ 5.5 V		0.03		%/V
		2.25 V ≤ V_{IN} ≤ 5.5 V T_J = –40°C to +125°C		0.06		
$\Delta V_{OUT}/\Delta I_{OUT}$	Output voltage load regulation(1)(3)	10 mA ≤ I_{OUT} ≤ 3 A		0.1		%/A
		10 mA ≤ I_{OUT} ≤ 3 A T_J = –40°C to +125°C		0.2		
V_{DO}	Dropout voltage(4)	I_{OUT} = 3 A, T_J = –40°C to +125°C			425	mV
I_{GND}	Ground pin current, output enabled	I_{OUT} = 10 mA, $\overline{\text{ERROR}}$ pin = GND		10	12	mA
		I_{OUT} = 10 mA, $\overline{\text{ERROR}}$ pin = GND T_J = –40°C to +125°C			15	
		I_{OUT} = 3 A, $\overline{\text{ERROR}}$ pin = GND		12	15	
		I_{OUT} = 3 A, $\overline{\text{ERROR}}$ pin = GND T_J = –40°C to +125°C			20	
	Ground pin current, output disabled	V_{EN} = 0.5 V, $\overline{\text{ERROR}}$ pin = GND		60	100	µA
		V_{EN} = 0.5 V, $\overline{\text{ERROR}}$ pin = GND T_J = –40°C to +125°C			110	
I_{SC}	Short-circuit current	V_{OUT} = 0 V		5.6		A
ENABLE INPUT						
$V_{EN(TH)}$	Enable on/off threshold	V_{EN} rising from 0 V until the output turns to an ON state, or V_{EN} falling from ≥ 2 V until the output turns to an OFF state	0.74	0.85	0.92	V
		V_{EN} rising from 0 V until the output turns to an ON state, or V_{EN} falling from ≥ 2 V until the output turns to an OFF state T_J = –40°C to +125°C	0.56		1	
$t_{d(OFF)}$	Turnoff delay	Time from V_{EN} < $V_{EN(TH)}$ to V_{OUT} = OFF, I_{LOAD} = 3 A		5		µs
$t_{d(ON)}$	Turnon delay	Time from V_{EN} >$V_{EN(TH)}$ to V_{OUT} = ON, I_{LOAD} = 3 A		5		
I_{EN}	EN pin current	V_{EN} = V_{IN}		1		nA
		V_{EN} = 0 V		–1		

(1) The line and load regulation specification contains only the typical number. However, the limits for line and load regulation are included in the output voltage tolerance specification.
(2) Output voltage line regulation is defined as the change in output voltage from the nominal value due to change in the voltage at the input.
(3) Output voltage load regulation is defined as the change in output voltage from the nominal value due to change in the load current at the output.
(4) Dropout voltage (V_{DO}) is typically defined as the input to output voltage differential (V_{IN} – V_{OUT}) where the input voltage is low enough to cause the output voltage to drop 2% from the nominal value. For the LP38513, the minimum operating voltage of 2.25 V is the limiting factor, and the maximum dropout voltage is defined as: $V_{DO(MAX)}$ = $V_{IN(MIN)}$ – $V_{OUT(MIN)}$ = (2.25 V – (1.8 V × 95.9%) = 524 mV).

Electrical Characteristics (continued)

Unless otherwise specified: V_{IN} = 2.5 V, I_{OUT} = 10 mA, C_{IN} = 10 µF, C_{OUT} = 10 µF, V_{EN} = 2 V, and limits apply for T_J = 25°C. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\overline{\text{ERROR}}$ FLAG						
V_{TH}	$\overline{\text{ERROR}}$ flag threshold(5)	V_{OUT} falling from $V_{OUT(NOM)}$ until $\overline{\text{ERROR}}$ flag goes low		85%		
		V_{OUT} falling from $V_{OUT(NOM)}$ until $\overline{\text{ERROR}}$ flag goes low T_J = –40°C to +125°C	77%		94%	
ΔV_{TH}	$\overline{\text{ERROR}}$ flag threshold hysteresis(5)	V_{OUT} rising from V_{TH} until $\overline{\text{ERROR}}$ flag goes high		4%		
		V_{OUT} rising from V_{TH} until $\overline{\text{ERROR}}$ flag goes high T_J = –40°C to +125°C	2.2%		5.8%	
$V_{ERROR(SAT)}$	$\overline{\text{ERROR}}$ flag saturation voltage	I_{SINK} = 1 mA		20		mV
		I_{SINK} = 1 mA, T_J = –40°C to +125°C			100	
I_{lk}	$\overline{\text{ERROR}}$ flag pin leakage current	$V_{\overline{\text{ERROR}}}$ = 5.5 V		100		nA
t_d	$\overline{\text{ERROR}}$ flag delay time			1		µs
AC PARAMETERS						
PSRR	Ripple rejection	V_{IN} = 2.5 V, f = 120 Hz		73		dB
		V_{IN} = 2.5 V, f = 1 kHz		70		
$\rho_{n(l/f)}$	Output noise density	f = 120 Hz		0.8		µV/√Hz
e_n	Output noise voltage	BW = 100 Hz – 100 kHz, V_{OUT} = 1.8 V		45		μV_{RMS}
THERMAL CHARACTERISTICS						
T_{SD}	Thermal shutdown	T_J rising		165		°C
ΔT_{SD}	Thermal shutdown hysteresis	T_J falling from T_{SD}		10		

(5) The $\overline{\text{ERROR}}$ flag thresholds are specified as percentage of the nominal regulated output voltage. See *Application and Implementation* section.

6.6 Typical Characteristics

Unless otherwise specified: T_J = 25°C, V_{IN} = 2.5V, V_{EN} = 2 V, C_{IN} = 10 µF, C_{OUT} = 10 µF, I_{OUT} = 10 mA.

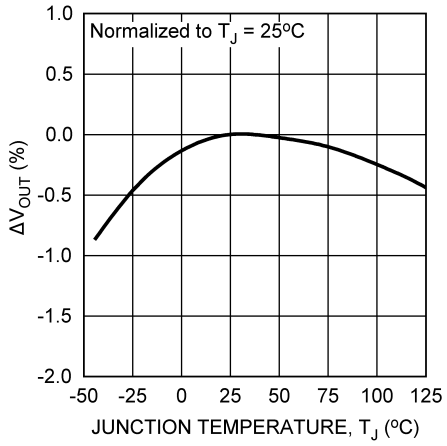


Figure 1. V_{OUT} vs Temperature

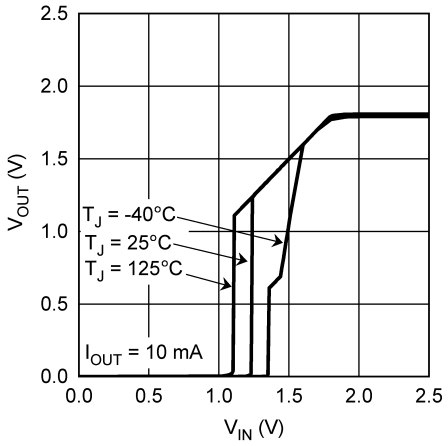


Figure 2. V_{OUT} vs V_{IN}

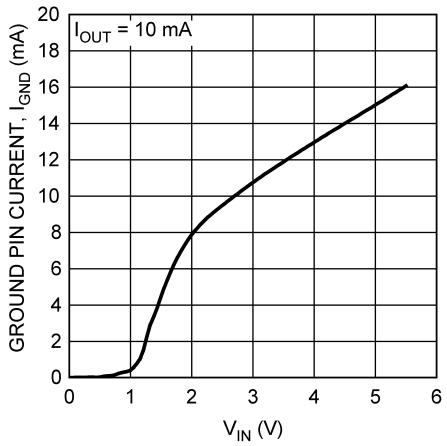


Figure 3. Ground Pin Current (I_{GND}) vs V_{IN}

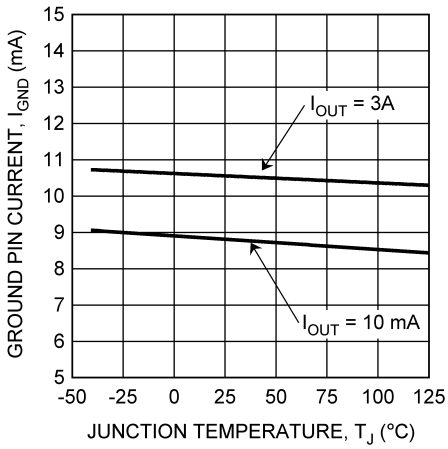


Figure 4. Ground Pin Current (I_{GND}) vs Temperature

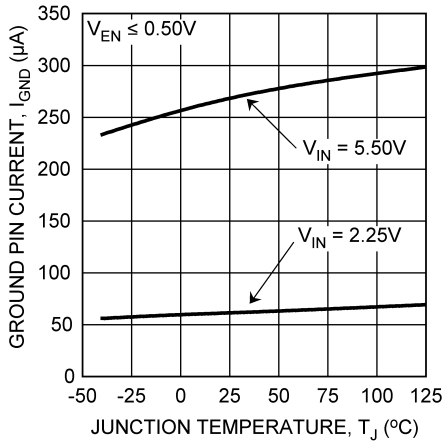


Figure 5. Ground Pin Current (I_{GND}) vs Temperature

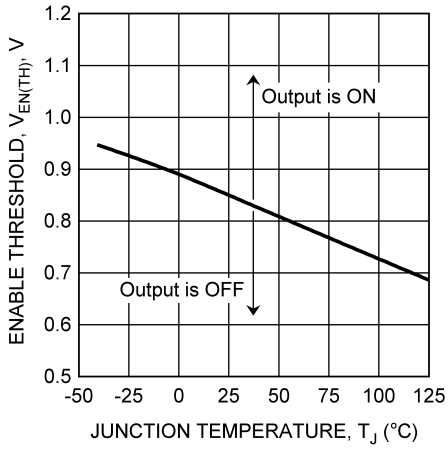


Figure 6. Enable Threshold vs Temperature

Typical Characteristics (continued)

Unless otherwise specified: T_J = 25°C, V_{IN} = 2.5V, V_{EN} = 2 V, C_{IN} = 10 µF, C_{OUT} = 10 µF, I_{OUT} = 10 mA.

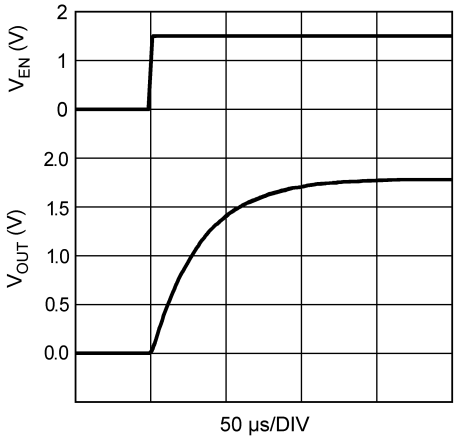


Figure 7. V_{OUT} vs V_{EN}

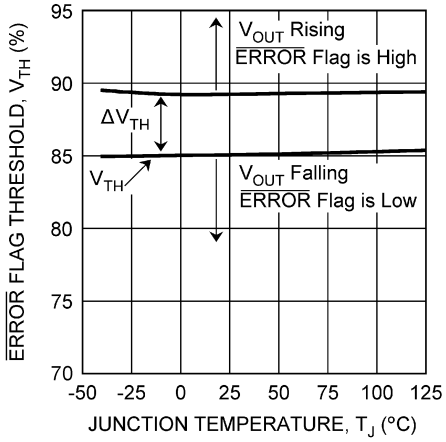


Figure 8. V_{OUT} ERROR Flag Threshold vs Temperature

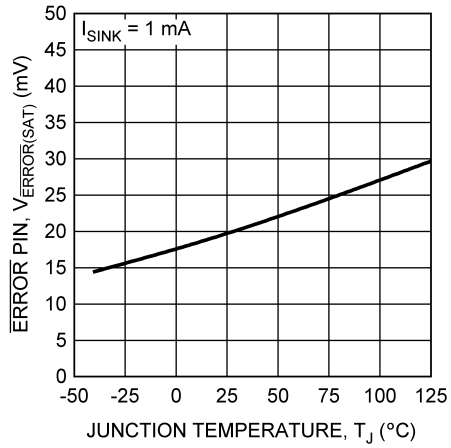


Figure 9. ERROR Flag Low vs Temperature

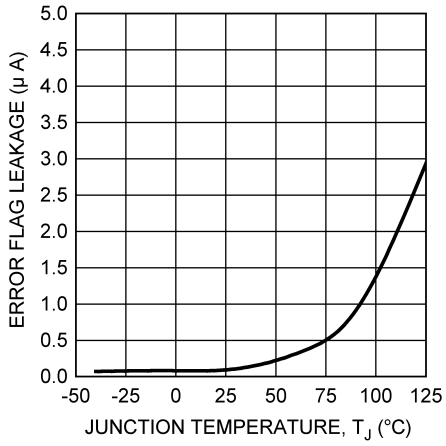


Figure 10. ERROR Flag Leakage vs Temperature

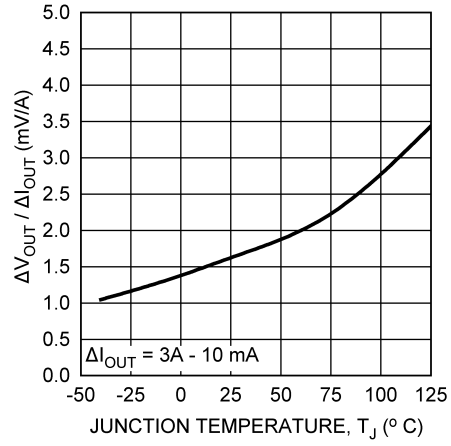


Figure 11. Load Regulation vs Temperature

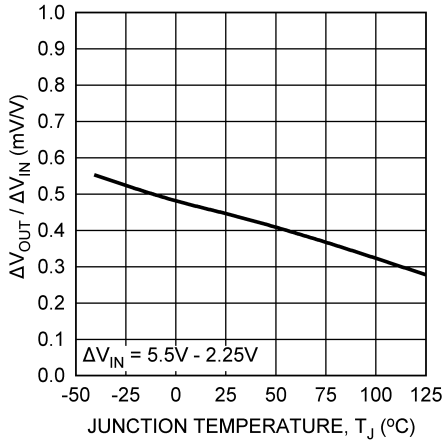


Figure 12. Line Regulation vs Temperature

Typical Characteristics (continued)

Unless otherwise specified: T_J = 25°C, V_{IN} = 2.5V, V_{EN} = 2 V, C_{IN} = 10 µF, C_{OUT} = 10 µF, I_{OUT} = 10 mA.

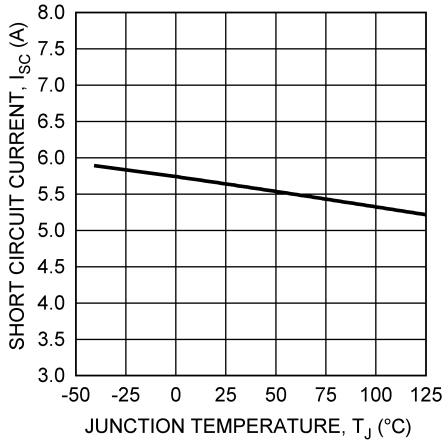


Figure 13. Current Limit vs Temperature

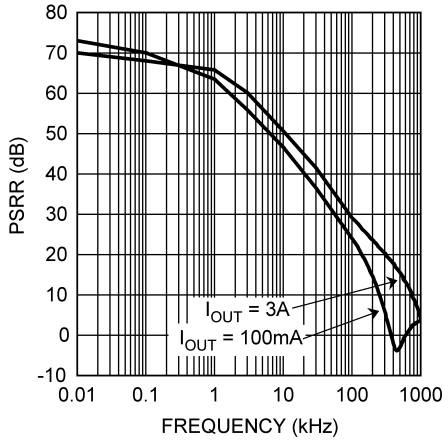


Figure 14. PSRR

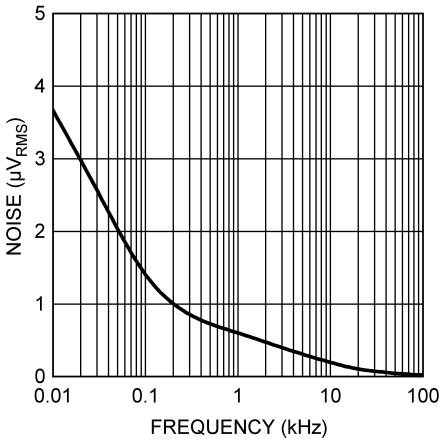


Figure 15. Noise

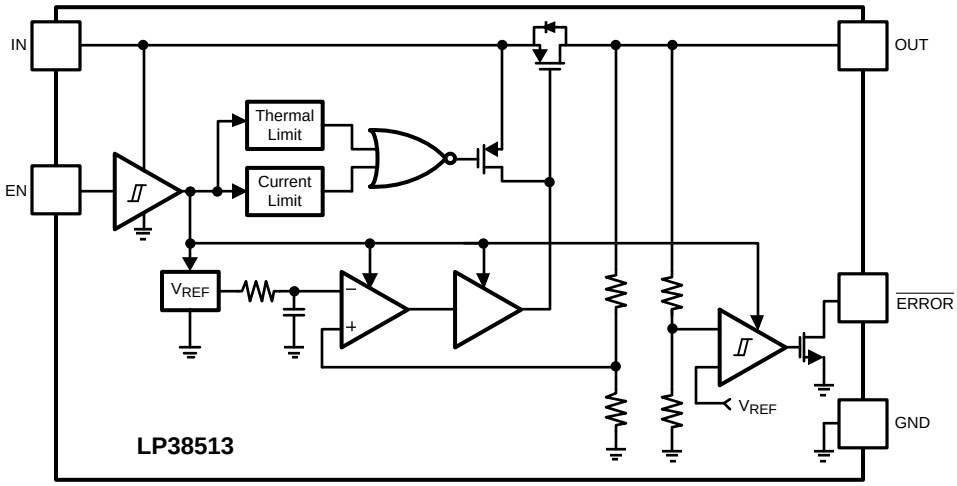
7 Detailed Description

7.1 Overview

The LP38513 is a fast response, ultra-low-dropout linear regulator that operates from a 2.25-V to 5.5-V input supply. This linear regulator responds very quickly to step changes in line or load conditions, making it suitable for low-voltage microprocessor applications. The device has low quiescent current operation that is independent of the output load current, and it has an $\overline{\text{ERROR}}$ flag pin, which can indicate that V_{OUT} is within 15% of the nominal regulated voltage.

The LP38513 is designed to perform with a10-µF (minimum value) input capacitor and a 10-µF (minimum value) output capacitor.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Short-Circuit Protection

The LP38513 is short-circuit protected and, in the event of a peak overcurrent condition, the short-circuit control loop rapidly drives the output PMOS pass element off. Once the power pass element shuts down, the control loop rapidly cycles the output on and off until the average power dissipation causes the thermal shutdown circuit to respond to servo the on/off cycling to a lower frequency. Refer to the *Power Dissipation* section for power dissipation calculations.

7.3.2 Enable

LP38513 has an EN pin to enable/disable the device. If the application does not require the enable function, the pin must be connected directly to the adjacent IN pin.

The status of the EN pin also affects the behavior of the $\overline{\text{ERROR}}$ flag. While the EN pin is high the regulator control loop is active, and the $\overline{\text{ERROR}}$ flag reorts the status of the output voltage. When the EN pin is taken low the regulator control loop is shut down, the output is turned off, and the internal logic immediately forces the $\overline{\text{ERROR}}$ flag pin low.

7.3.3 $\overline{\text{ERROR}}$ Flag

When the LP38513 EN pin is high, the $\overline{\text{ERROR}}$ flag pin produces a logic low signal when the output drops by more than 15% (V_{TH}, typical) from the nominal output voltage. The drop in output voltage may be due to low input voltage, current limiting, or thermal limiting. This flag has a built-in hysteresis. The output voltage must to rise to greater than typically 89% of the nominal output voltage for the $\overline{\text{ERROR}}$ flag to return to a logic high state. Also, if the EN pin is pulled low, the $\overline{\text{ERROR}}$ flag pin is forced to low as well.

7.4 Device Functional Modes

7.4.1 Enable Operation

The Enable on/off threshold is typically 850 mV and has no hysteresis. The voltage signal must rise and fall cleanly, and promptly, through this threshold. The EN pin has no internal pullup or pulldown to establish a default condition and, as a result, this pin must be terminated either actively or passively.

If the EN pin is driven from a single ended device (such as the collector of a discrete transistor) a pullup resistor to V_{IN}, or a pulldown resistor to ground, is required for proper operation. A 1-kΩ to 100-kΩ resistor can be used as the pullup or pulldown resistor to establish default condition for the EN pin. The resistor value selected must be appropriate to swamp out any leakage in the external single-ended device, as well as any stray capacitance.

If the EN pin is driven from a source that actively pulls high and low (such as a CMOS rail-to-rail comparator output), the pullup or pulldown resistor is not required.

If the application does not require the enable function, the EN pin must be connected directly to the adjacent IN pin.

7.4.2 $\overline{\text{ERROR}}$ Flag Operation

The internal $\overline{\text{ERROR}}$ flag comparator has an open-drain output stage. Hence, the $\overline{\text{ERROR}}$ pin requires an external pullup resistor. The value of the pullup resistor must be in the range of 2 kΩ to 20 kΩ and must be connected to the LP38513 OUT pin. The $\overline{\text{ERROR}}$ flag pin must not be pulled up to any voltage source higher than V_{IN} as current flow through an internal parasitic diode may cause unexpected behavior. When the input voltage is less than typically 1.25 V the status of the $\overline{\text{ERROR}}$ flag output is not reliable. The $\overline{\text{ERROR}}$ flag pin must be connected to ground if this function is not used.

The timing diagram in Figure 16 shows the relationship between the $\overline{\text{ERROR}}$ flag and the output voltage when a pullup resistor is connected to the output voltage pin.

The timing diagram in Figure 17 shows the relationship between the $\overline{\text{ERROR}}$ flag and the output voltage when the pullup resistor is connected to the input voltage.

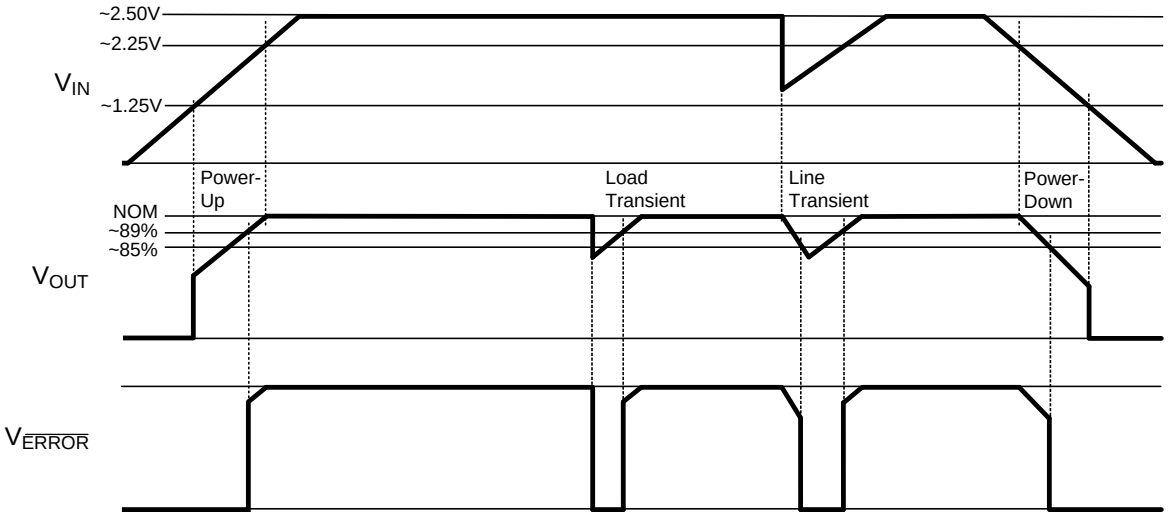


Figure 16. $\overline{\text{ERROR}}$ Flag Operation (see Figure 18)

Device Functional Modes (continued)

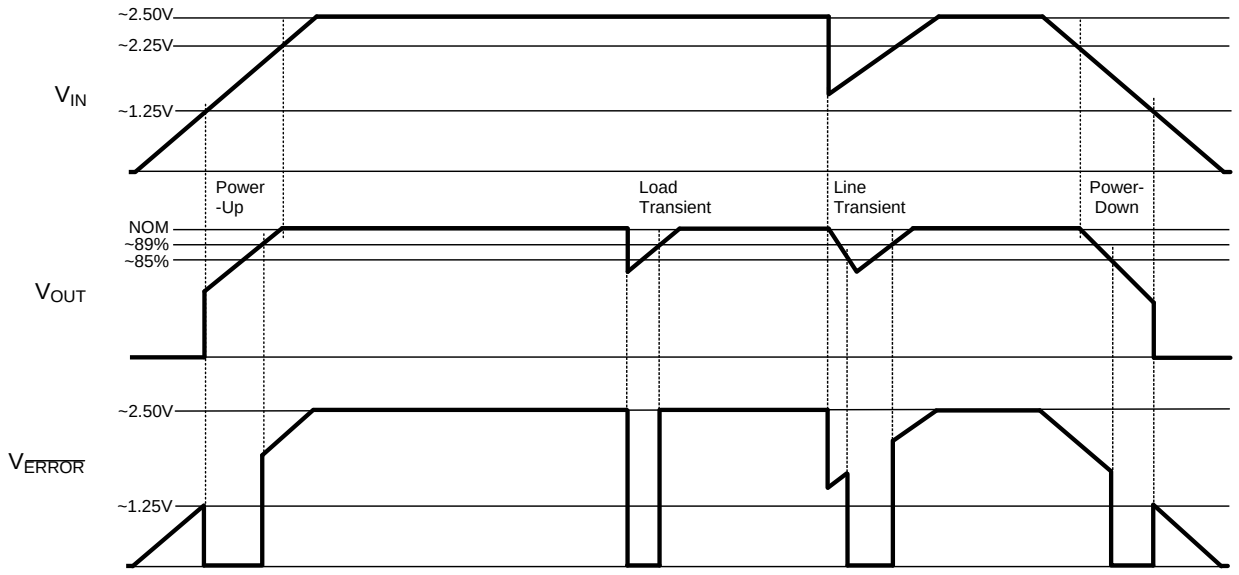


Figure 17. $\overline{\text{ERROR}}$ Flag Operation Biased from V_{IN}

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The typical application of the LP38513 includes microprocessor supplies, bus terminators, post regulators, and battery-powered application. Figure 18 shows the typical application circuit for LP38513. The input and output capacitances may need to be increased above the 10-µF minimum for some applications.

8.2 Typical Application

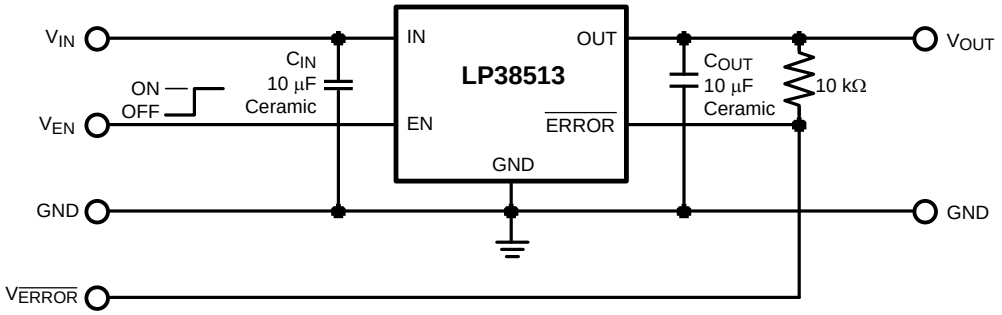


Figure 18. LP38513 Typical Application

8.2.1 Design Requirements

For the typical LP38513 ultra-low-dropout linear regulator applications, use the parameters listed in Table 1.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Minimum input voltage	2.25 V
Output voltage	1.8 V
Output current	0 mA to 3 A

8.2.2 Detailed Design Procedure

8.2.2.1 External Capacitors

Like any low-dropout regulator, external capacitors are required to assure stability. These capacitors must be correctly selected for proper performance.

8.2.2.1.1 Input Capacitor

A ceramic input capacitor of at least 10 µF is required. For general usage across all load currents and operating conditions, a 10-µF ceramic input capacitor provides satisfactory performance.

8.2.2.1.2 Output Capacitor

A ceramic capacitor with a minimum value of 10 µF is required at the output pin for loop stability. It must be located less than 1 cm from the device and connected directly to the OUT and GND pin using traces which have no other currents flowing through them. As long as the minimum of 10 µF ceramic is met, there is no limitation on any additional capacitance.

X7R and X5R dielectric ceramic capacitors are strongly recommended, as they typically maintain a capacitance range within ±20% of nominal over full operating ratings of temperature and voltage; they are typically larger and more costly than Z5U/Y5U types for a given voltage and capacitance.

Z5U and Y5V dielectric ceramics are not recommended as the capacitance will drop severely with applied voltage. A typical Z5U or Y5V capacitor can lose 60% of its rated capacitance with half of the rated voltage applied to it. The Z5U and Y5V also exhibit a severe temperature effect, losing more than 50% of nominal capacitance at high and low limits of the temperature range.

8.2.2.2 Reverse Voltage

A reverse voltage condition will exist when the voltage at the OUT pin is higher than the voltage at the IN pin. Typically this happens when V_{IN} is abruptly taken low and C_{OUT} continues to hold a sufficient charge such that the input to output voltage becomes reversed. A less common condition is when an alternate voltage source is connected to the output.

There are two possible paths for current to flow from the OUT pin back to the input during a reverse voltage condition.

While V_{IN} is high enough to keep the control circuity alive, and the EN pin is above the $V_{EN(ON)}$ threshold, the control circuitry attempts to regulate the output voltage. Because the input voltage is less than the output voltage the control circuit drives the gate of the pass element to the full ON condition when the output voltage begins to fall. In this condition, reverse current will flow from the OUT pin to the IN pin, limited only by the $R_{DS(ON)}$ of the pass element and the output-to-input voltage differential. Discharging an output capacitor up to 1000 µF in this manner does not damage the device as the current rapidly decays. However, continuous reverse current must be avoided.

The internal PFET pass element in the LP38513 has an inherent parasitic diode. During normal operation, the input voltage is higher than the output voltage, and the parasitic diode is reverse biased. However, if the output-voltage-to-input-voltage differential is more than 500 mV (typical), the parasitic diode becomes forward biased, and current flows from the OUT pin to the input through the diode. The current in the parasitic diode must be limited to less than 1-A continuous and 5-A peak.

If used in a dual-supply system where the regulator output load is returned to a negative supply, the OUT pin must be diode clamped to ground. A Schottky diode is recommended for this protective clamp.

8.2.2.3 Power Dissipation

A heat sink may be required depending on the maximum power dissipation ($P_{D(MAX)}$), maximum ambient temperature ($T_{A(MAX)}$)of the application, and the thermal resistance ($R_{\theta JA}$) of the package. Under all possible conditions, the junction temperature (T_J) must be within the range specified in the *Recommended Operating Conditions*. The total power dissipation of the device is given by:

$$P_D = ((V_{IN} - V_{OUT}) \times I_{OUT}) + ((V_{IN}) \times I_{GND})$$

where

- I_{GND} is the operating ground current of the device (specified under *Electrical Characteristics*). (1)

The maximum allowable junction temperature rise (ΔT_J) depends on the maximum expected ambient temperature ($T_{A(MAX)}$) of the application, and the maximum allowable junction temperature ($T_{J(MAX)}$):

$$\Delta T_J = T_{J(MAX)} - T_{A(MAX)} \quad (2)$$

The maximum allowable value for junction-to-ambient thermal resistance, $R_{\theta JA}$, can be calculated using the formula:

$$R_{\theta JA} = \Delta T_J / P_{D(MAX)} \quad (3)$$

Knowing the device power dissipation and proper sizing of the thermal plane connected to the tab or pad is critical to ensuring reliable operation. Device power dissipation depends on input voltage, output voltage, and load conditions and can be calculated with Equation 4.

$$P_{D(MAX)} = (V_{IN(MAX)} - V_{OUT}) \times I_{OUT(MAX)} \quad (4)$$

Power dissipation can be minimized, and greater efficiency can be achieved, by using the lowest available voltage drop option that would still be greater than the dropout voltage (V_{DO}). However, keep in mind that higher voltage drops result in better dynamic (that is, PSRR and transient) performance.

The maximum allowable junction temperature ($T_{J(MAX)}$) determines maximum power dissipation allowed ($P_{D(MAX)}$) for the device package.

Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A), according to Equation 5 or Equation 6:

$$T_{J(MAX)} = T_{A(MAX)} + (R_{\theta JA} \times P_{D(MAX)}) \quad (5)$$

$$P_{D(MAX)} = (T_{J(MAX)} - T_{A(MAX)}) / R_{\theta JA} \quad (6)$$

Unfortunately, this $R_{\theta JA}$ is highly dependent on the heat-spreading capability of the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in *Thermal Information* is determined by the specific EIA/JEDEC JESD51-7 standard for PCB and copper-spreading area, and is to be used only as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the package junction-to-case (bottom) thermal resistance ($R_{\theta JCbot}$) plus the thermal resistance contribution by the PCB copper area acting as a heat sink.

8.2.2.4 Estimating Junction Temperature

The EIA/JEDEC standard recommends the use of psi (Ψ) thermal characteristics to estimate the junction temperatures of surface mount devices on a typical PCB board application. These characteristics are not true thermal resistance values, but rather package specific thermal characteristics that offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of copper-spreading area. The key thermal characteristics (Ψ_{JT} and Ψ_{JB}) are given in *Thermal Information* and are used in accordance with Equation 7 or Equation 8.

$$T_{J(MAX)} = T_{TOP} + (\Psi_{JT} \times P_{D(MAX)})$$

where

- $P_{D(MAX)}$ is explained in Equation 4.
- T_{TOP} is the temperature measured at the center-top of the device package. (7)

$$T_{J(MAX)} = T_{BOARD} + (\Psi_{JB} \times P_{D(MAX)})$$

where

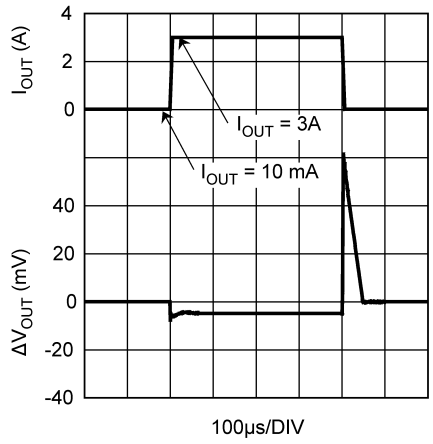
- $P_{D(MAX)}$ is explained in Equation 4.
- T_{BOARD} is the PCB surface temperature measured 1-mm from the device package and centered on the package edge. (8)

For more information about the thermal characteristics Ψ_{JT} and Ψ_{JB}, see the TI Application Report: *Semiconductor and IC Package Thermal Metrics* (SPRA953), available for download at www.ti.com.

For more information about measuring T_{TOP} and T_{BOARD}, see the TI Application Report: *Using New Thermal Metrics* (SBVA025), available for download at www.ti.com.

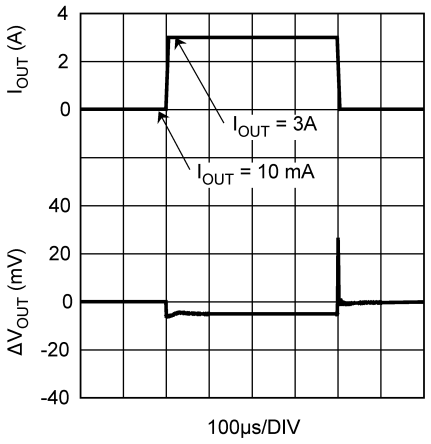
For more information about the EIA/JEDEC JESD51 PCB used for validating $R_{\theta JA}$, see the TI Application Report: *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* (SZZA017), available for download at www.ti.com.

8.2.3 Application Curves



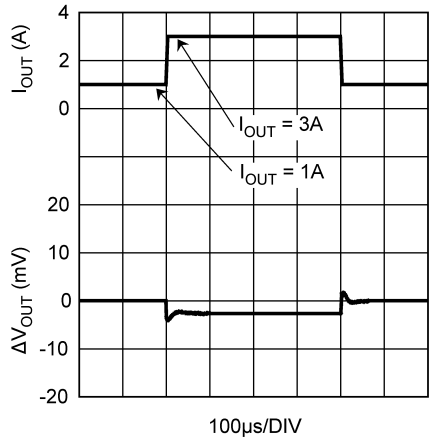
10 mA to 3 A C_{OUT} = 10 µF Ceramic

Figure 19. Load Transient



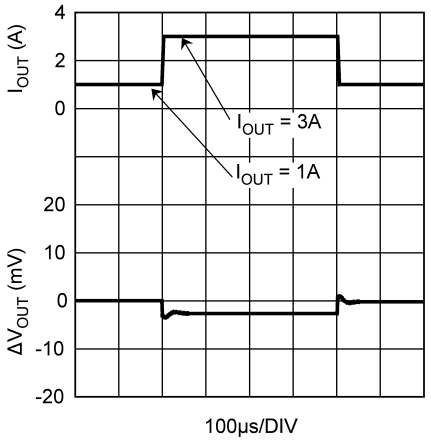
10 mA to 3 A C_{OUT} = 10 µF ceramic + 100 µF aluminum

Figure 20. Load Transient



10 mA to 3 A C_{OUT} = 10 µF Ceramic

Figure 21. Load Transient



10 mA to 3 A C_{OUT} = 10 µF Ceramic + 100 µF Aluminum

Figure 22. Load Transient

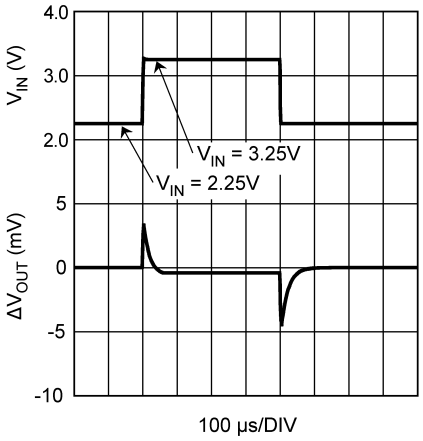


Figure 23. Line Transient

9 Power Supply Recommendations

The LP38513 device is designed to operate from an input supply voltage range of 2.25 V to 5.5 V. The input supply should be well-regulated and free of spurious noise. A minimum capacitor value of 10 µF is required.

10 Layout

10.1 Layout Guidelines

The dynamic performance of the LP38513 is dependent on the layout of the PCB. PCB layout practices that are adequate for typical LDOs may degrade the PSRR, noise, or transient performance of the device. Best performance is achieved by placing C_{IN} and C_{OUT} on the same side of the PCB as the LP38513, and as close to the package as is practical. The ground connections for C_{IN} and C_{OUT} must be back to the LP38513 GND pin using as wide and short of a copper trace as is practical.

Good PC layout practices must be used or instability can be induced because of ground loops and voltage drops. The input and output capacitors must be directly connected to the IN, OUT, and GND pins of the LP38513 using traces which do not have other currents flowing in them (Kelvin connect). The best way to do this is to lay out C_{IN} and C_{OUT} near the device with short traces to the IN, OUT, and GND pins. The regulator ground pin must be connected to the external circuit ground so that the regulator and its capacitors have a single-point ground.

Stability problems have been seen in applications where vias to an internal ground plane were used at the ground points of the LP38513 device and the input and output capacitors. This was caused by varying ground potentials at these nodes resulting from current flowing through the ground plane. Using a single point ground technique for the regulator and its capacitors fixed the problem.

Because high current flows through the traces going into the IN pin and coming from the OUT pin, Kelvin connect the capacitor leads to these pins so there is no voltage drop in series with the input and output capacitors.

10.2 Layout Example

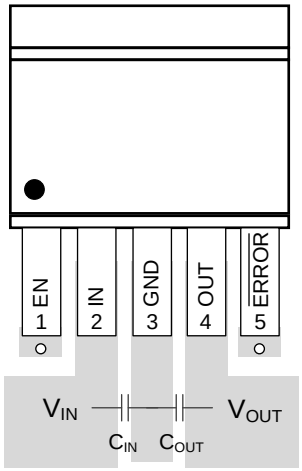


Figure 24. LP38513 Layout

11 Device and Documentation Support

11.1 Related Documentation

For additional information, see the following:

- TI Application Report *Using New Thermal Metrics* (SBVA025)
- TI Application Report *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* (SZZA017)

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
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11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP38513S-1.8/NOPB	Active	Production	DDPAK/ TO-263 (KTT) | 5	45 | TUBE	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP38513S -1.8
LP38513S-1.8/NOPB.A	Active	Production	DDPAK/ TO-263 (KTT) | 5	45 | TUBE	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP38513S -1.8
LP38513SX-1.8/NOPB	Active	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP38513S -1.8
LP38513SX-1.8/NOPB.A	Active	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP38513S -1.8
LP38513T-1.8/NOPB	Active	Production	TO-220 (NDH) | 5	45 | TUBE	Yes	SN	Level-1-NA-UNLIM	-40 to 125	LP38513T -1.8
LP38513T-1.8/NOPB.A	Active	Production	TO-220 (NDH) | 5	45 | TUBE	Yes	SN	Level-1-NA-UNLIM	-40 to 125	LP38513T -1.8

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

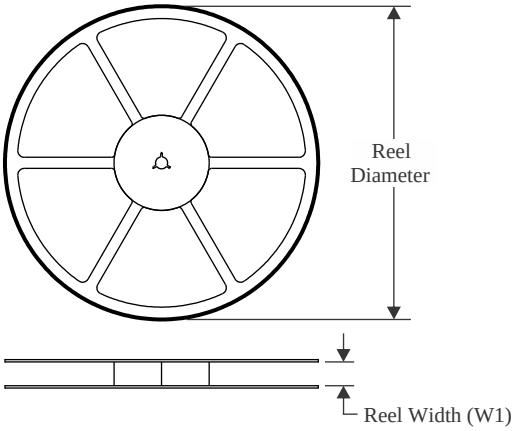
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

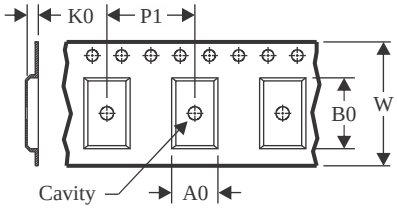
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

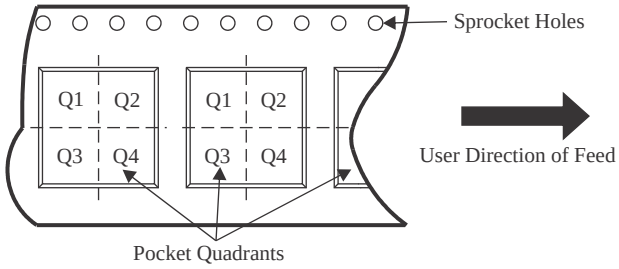


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

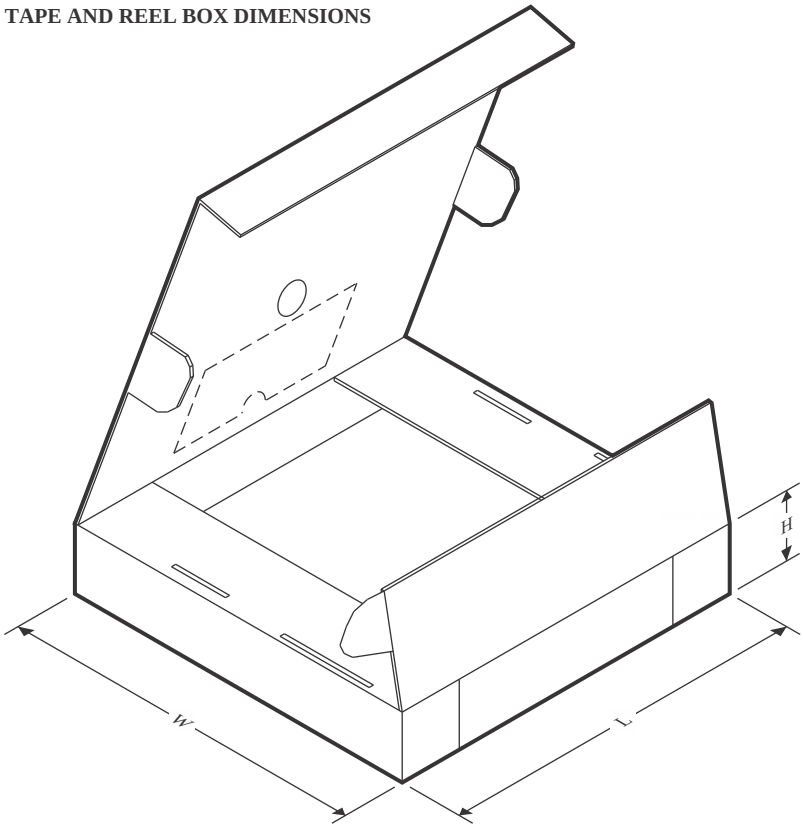
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP38513SX-1.8/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2

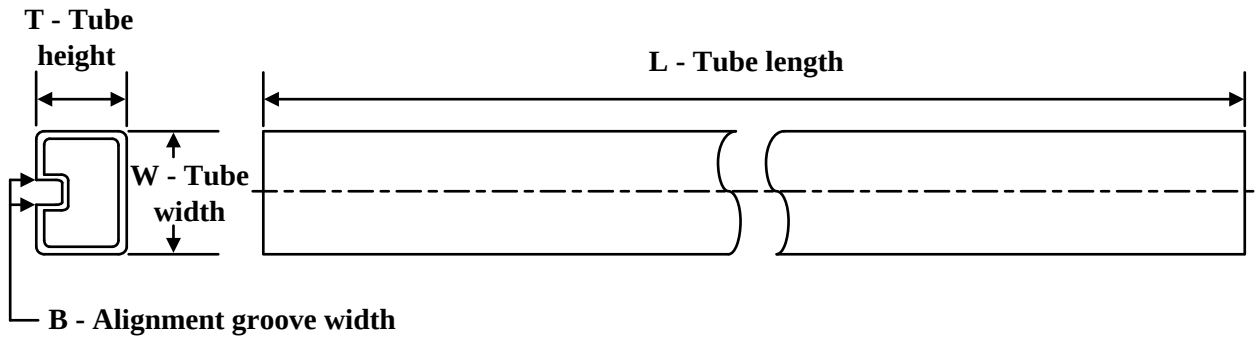
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP38513SX-1.8/NOPB	DDPAK/TO-263	KTT	5	500	356.0	356.0	45.0

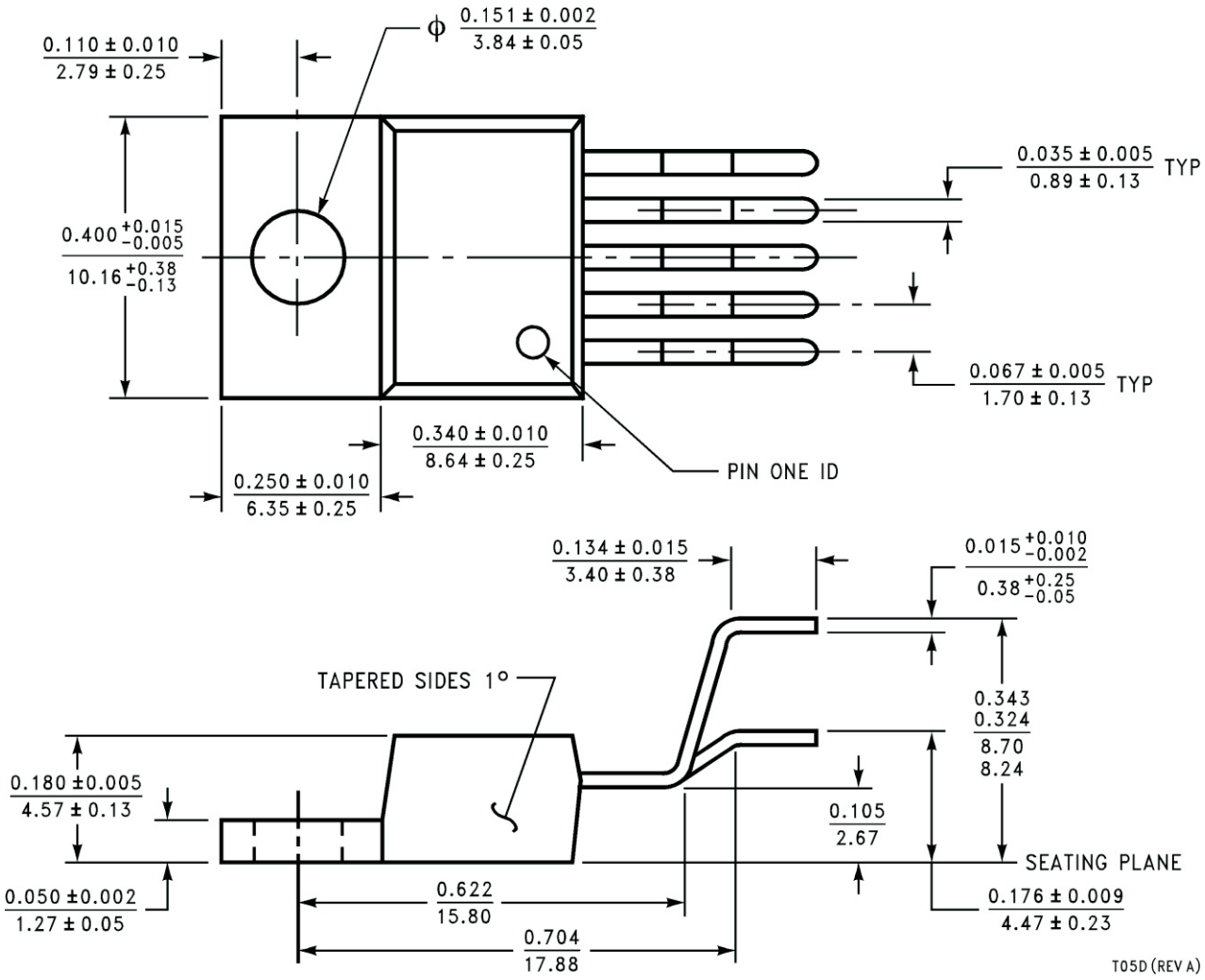
TUBE



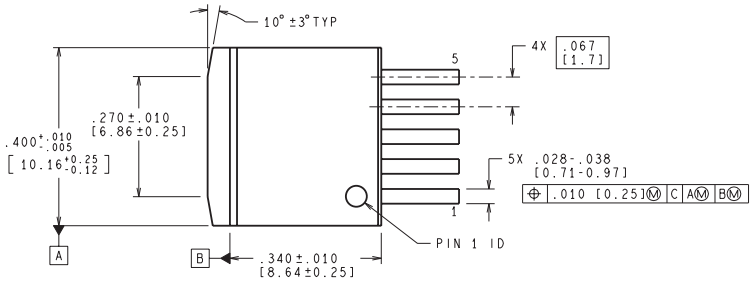
*All dimensions are nominal

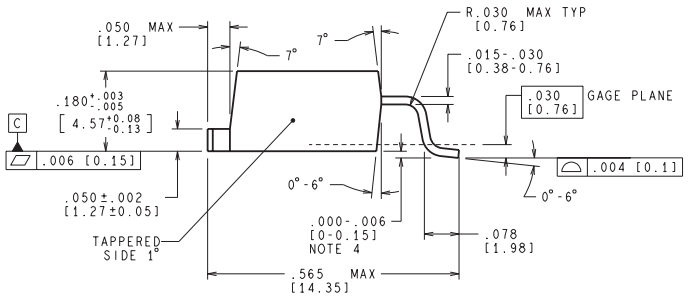
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LP38513S-1.8/NOPB	KTT	TO-263	5	45	502	25	8204.2	9.19
LP38513S-1.8/NOPB.A	KTT	TO-263	5	45	502	25	8204.2	9.19
LP38513T-1.8/NOPB	NDH	TO-220	5	45	502	30	30048.2	10.74
LP38513T-1.8/NOPB.A	NDH	TO-220	5	45	502	30	30048.2	10.74

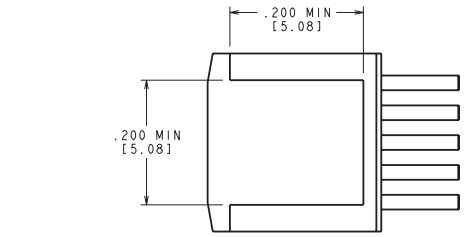
NDH0005D


0.110 ± 0.010
2.79 ± 0.25
ϕ 0.151 ± 0.002
3.84 ± 0.05
0.035 ± 0.005
0.89 ± 0.13
TYP
0.400 +0.015 −0.005
10.16 +0.38 −0.13
0.067 ± 0.005
1.70 ± 0.13
TYP
0.340 ± 0.010
8.64 ± 0.25
PIN ONE ID
0.250 ± 0.010
6.35 ± 0.25
0.134 ± 0.015
3.40 ± 0.38
0.015 +0.010 −0.002
0.38 +0.25 −0.05
TAPERED SIDES 1°
0.343
0.324
8.70
8.24
0.180 ±0.005
4.57 ± 0.13
0.105
2.67
SEATING PLANE
0.050 ±0.002
1.27 ± 0.05
0.622
15.80
0.176 ± 0.009
4.47 ± 0.23
0.704
17.88
T05D (REV A)

KTT0005B







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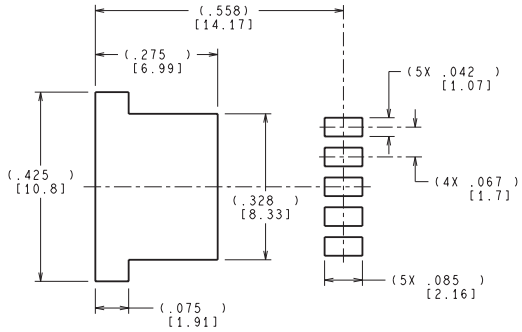

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