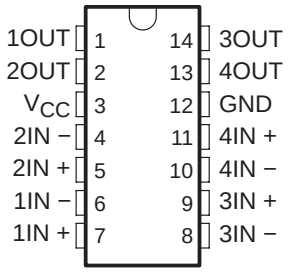
The LP239 is obsolete and is no longer supplied.

SLCS004B − OCTOBER 1987 − REVISED SEPTEMBER 2004

- **Wide Supply-Voltage Range . . . 3 V to 30 V**
- **Ultralow Power Supply Current Drain . . . 60 μA Typ**
- **Low Input Biasing Current . . . 3 nA**
- **Low Input Offset Current . . . ±0.5 nA**
- **Low Input Offset Voltage . . . ±2 mV**
- **Common-Mode Input Voltage Includes Ground**
- **Output Voltage Compatible With MOS and CMOS Logic**
- **High Output Sink-Current Capability (30 mA at V_O = 2V)**
- **Power Supply Input Reverse-Voltage Protected**
- **Single-Power-Supply Operation**
- **Pin-for-Pin Compatible With LM239, LM339, LM2901**

D OR N PACKAGE
(TOP VIEW)



description/ordering information

The LP239, LP339, LP2901 are low-power quadruple differential comparators. Each device consists of four independent voltage comparators designed specifically to operate from a single power supply and typically to draw 60-μA drain current over a wide range of voltages. Operation from split power supplies also is possible and the ultra-low power-supply drain current is independent of the power-supply voltage.

Applications include limit comparators, simple analog-to-digital converters, pulse generators, squarewave generators, time-delay generators, voltage-controlled oscillators, multivibrators, and high-voltage logic gates. The LP239, LP339, LP2901 were designed specifically to interface with the CMOS logic family. The ultra-low power-supply current makes these products desirable in battery-powered applications.

The LP239 is characterized for operation from −25°C to 85°C. The LP339 is characterized for operation from 0°C to 70°C. The LP2901 is characterized for operation from −40°C to 85°C.

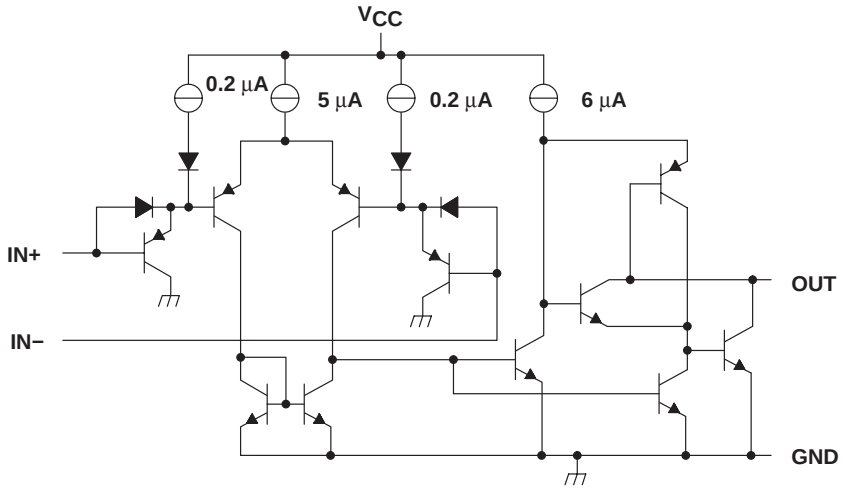
ORDERING INFORMATION

T_A	V_{IO}MAX AT 25°C	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	±5 mV	PDIP (N)	Tube of 25	LP339N	LP339N
		SOIC (D)	Tube of 50	LP339D	LP339
			Reel of 2500	LP339DR	
−40°C to 85°C	±5 mV	PDIP (N)	Tube of 25	LP2901N	LP2901N
		SOIC (D)	Tube of 50	LP2901D	LP2901
			Reel of 2500	LP2901DR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

The LP239 is obsolete and is no longer supplied.

schematic diagram (each comparator)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 36 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±36 V
Input voltage range, V_I (either input) . . . . . −0.3 V to 36 V
Input current, $V_I \le -0.3$ V (see Note 3) . . . . . −50 mA
Duration of output short-circuit to ground (see Note 4) . . . . . Unlimited
Continuous total dissipation (see Note 5) . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: LP239 . . . . . −25°C to 85°C
LP339 . . . . . 0°C to 70°C
LP2901 . . . . . −40°C to 85°C
Package thermal impedance, θ_{JA} (see Notes 6 and 7): D package . . . . . 86°C/W
N package . . . . . 80°C/W
Operating virtual junction temperature, T_J . . . . . 150°C
Lead temperature range 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values, except differential voltages, are with respect to the network ground.
2. Differential voltages are at IN+ with respect to IN −.
3. This input current only exists when the voltage at any of the inputs is driven negative. The current flows through the collector-base junction of the input clamping device. In addition to the clamping device action, there is lateral n-p-n parasitic transistor action. This action is not destructive, and normal output states are reestablished when the input voltage returns to a value more positive than − 0.3 V at T_A = 25°C.
4. Short circuits between outputs to V_{CC} can cause excessive heating and eventual destruction.
5. If the output transistors are allowed to saturate, the low-bias dissipation and the on-off characteristics of the outputs keep the dissipation very small (usually less than 100 mW).
6. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
7. The package thermal impedance is calculated in accordance with JESD 51-7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25$°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
J	1025 mW	8.2 mW/°C	656 mW	533 mW

recommended operating conditions

			LP239		LP339		LP2901		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		3	30	3	30	3	30	V
V_{IC}	Common-mode input voltage	V_{CC} = 5 V	0	3	0	3	0	3	V
		V_{CC} = 30 V	0	28	0	28	0	28	V
V_I	Input voltage	V_{CC} = 5 V	0	3	0	3	0	3	V
		V_{CC} = 30 V	0	28	0	28	0	28	V
T_A	Operating free-air temperature		−25	85	0	70	−40	85	°C

electrical characteristics, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, RS = 0,	V_O = 2 V, See Note 6	25°C		±2	±5	mV
				Full range			±9	
I_{IO}	Input offset current			25°C		±0.5	±5	nA
				Full range		±1	±15	
I_{IB}	Input bias current	See Note 7		25°C		−2.5	−25	nA
				Full range		−4	−40	
V_{ICR}	Common-mode input voltage range	Single supply		25°C	0 to V_{CC} − 1.5			V
				Full range	0 to V_{CC} − 2			
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V,	RL = 15 kΩ			500		V/mV
	Output sink current	$V_{I−}$ = 1 V, V_{I+} = 0	V_O = 2 V, See Note 8	25°C	20	30		mA
				Full range	15			
			V_O = 0.4 V	25°C	0.2	0.7		
	Output leakage current	V_{I+} = 1 V, $V_{I−}$ = 0	V_O = 5 V	25°C		0.1		nA
			V_O = 30 V	Full range			1	µA
V_{ID}	Differential input voltage	V_I ≤ 0 (or V_{CC} − on split supplies)					36	V
I_{CC}	Supply current	R_L = ∞ all comparators				60	100	µA

† Full range is −25°C to 85°C for the LP239, 0°C to 70°C for the LP339, and −40°C to 85°C for the LP2901.

NOTES: 8. V_{IO} is measured over the full common-mode input voltage range.

9. Because of the p-n-p input stage, the direction of the current is out of the device. This current essentially is constant (i.e., independent of the output state). No loading change exists on the reference or input lines as long as the common-mode input voltage range is not exceeded.

10. The output sink current is a function of the output voltage. These devices have a bimodal output section that allows them to sink (via a Darlington connection) large currents at output voltages greater than 1.5 V, and smaller currents at output voltages less than 1.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, R_L connected to 5 V through 5.1 kΩ

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Large-signal response time	TTL logic swing, V_{ref} = 1.4 V		1.3		µs
Response time			8		

APPLICATION INFORMATION

Figure 1 shows the basic configuration for using the LP239, LP339, or LP2901 comparator. Figure 2 shows the diagram for using one of these comparators as a CMOS driver.

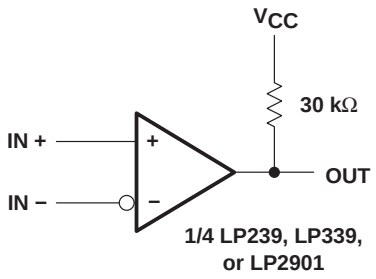


Figure 1. Basic Comparator

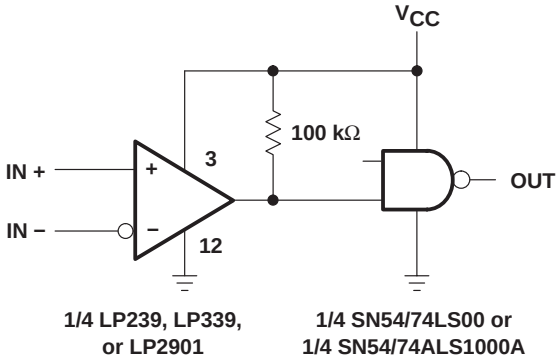


Figure 2. CMOS Driver

All pins of any unused comparators should be grounded. The bias network of the LP239, LP339, and LP2901 establishes a drain current that is independent of the magnitude of the power-supply voltage over the range of 2 V to 30 V. It usually is necessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V_{CC} without damaging the device. Protection should be provided to prevent the input voltages from going negative by more than −0.3 V. The output section has two distinct modes of operation: a Darlington mode and ground-emitter mode. This unique drive circuit permits the device to sink 30 mA at V_O = 2 V in the Darlington mode and 700 μA at V_O = 0.4 V in the ground-emitter mode. Figure 3 is a simplified schematic diagram of the output section. The output section is configured in a Darlington connection (ignoring Q3). If the output voltage is held high enough (above 1 V), Q1 is not saturated and the output current is limited only by the product of the h_{FE} of Q1, the h_{FE} of Q2, and I1 and the 60-Ω saturation resistance of Q2. The devices are capable of driving LEDs, relays, etc. in this mode while maintaining an ultra-low power-supply current of 60 μA, typically.

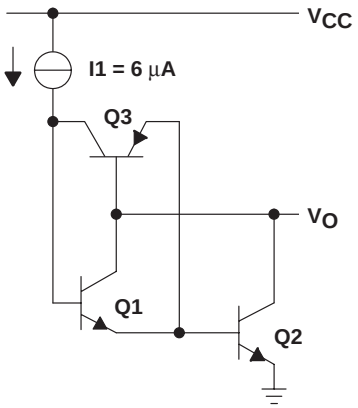


Figure 3. Output-Section Schematic Diagram

APPLICATION INFORMATION

Without transistor Q3, if the output voltage were allowed to drop below 0.8 V, transistor Q1 would saturate, and the output current would drop to zero. The circuit would be unable to pull low current loads down to ground or the negative supply, if used. Transistor Q3 has been included to bypass transistor Q1 under these conditions and apply the current I1 directly to the base of Q2. The output sink current now is approximately I1 times the h_{FE} of Q2 (700 μA at V_O = 0.4 V). The output of the devices exhibits a bimodal characteristic, with a smooth transition between modes.

In both cases, the output is an uncommitted collector. Several outputs can be tied together to provide a dot logic function. An output pullup resistor can be connected to any available power-supply voltage within the permitted power-supply range, and there is no restriction on this voltage, based on the magnitude of the voltage that is supplied to V_{CC} of the package.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP2901D	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 85	LP2901
LP2901DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LP2901
LP2901DR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LP2901
LP2901N	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	LP2901N
LP2901N.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	LP2901N
LP339D	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	0 to 70	LP339
LP339DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LP339
LP339DR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LP339
LP339DRG4	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	0 to 70	LP339
LP339N	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	LP339N
LP339N.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	LP339N

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF LP2901 :

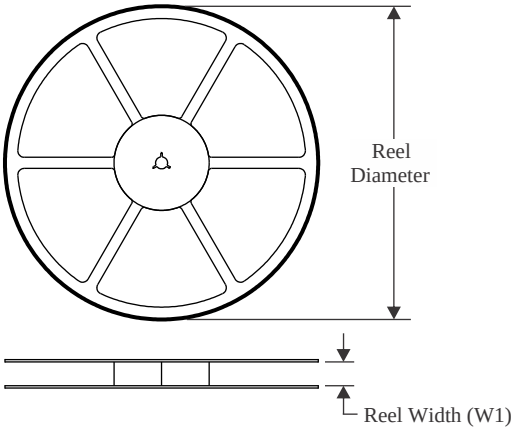
- Automotive : LP2901-Q1

NOTE: Qualified Version Definitions:

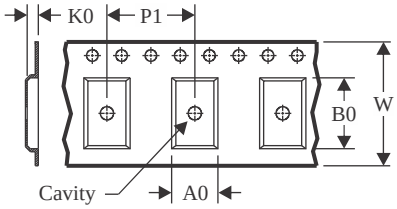
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

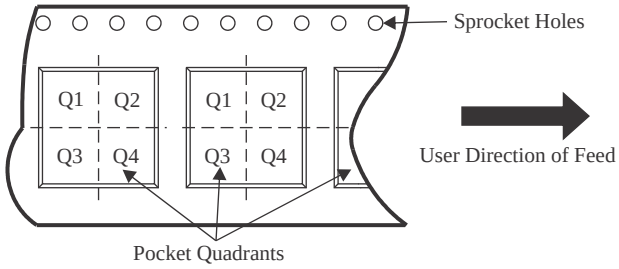


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

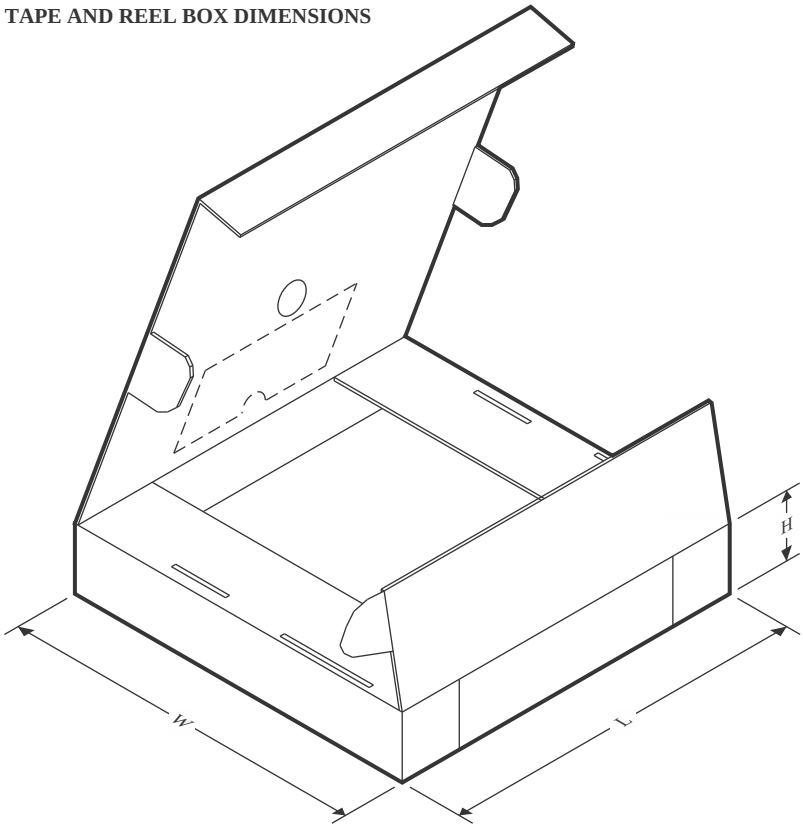
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2901DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LP339DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

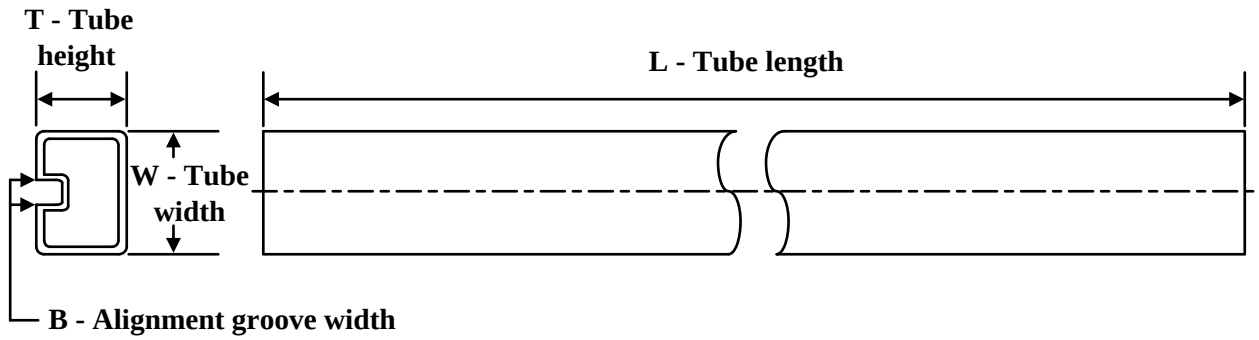
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

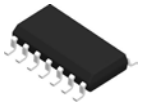
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2901DR	SOIC	D	14	2500	353.0	353.0	32.0
LP339DR	SOIC	D	14	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LP2901N	N	PDIP	14	25	506	13.97	11230	4.32
LP2901N.A	N	PDIP	14	25	506	13.97	11230	4.32
LP339N	N	PDIP	14	25	506	13.97	11230	4.32
LP339N.A	N	PDIP	14	25	506	13.97	11230	4.32

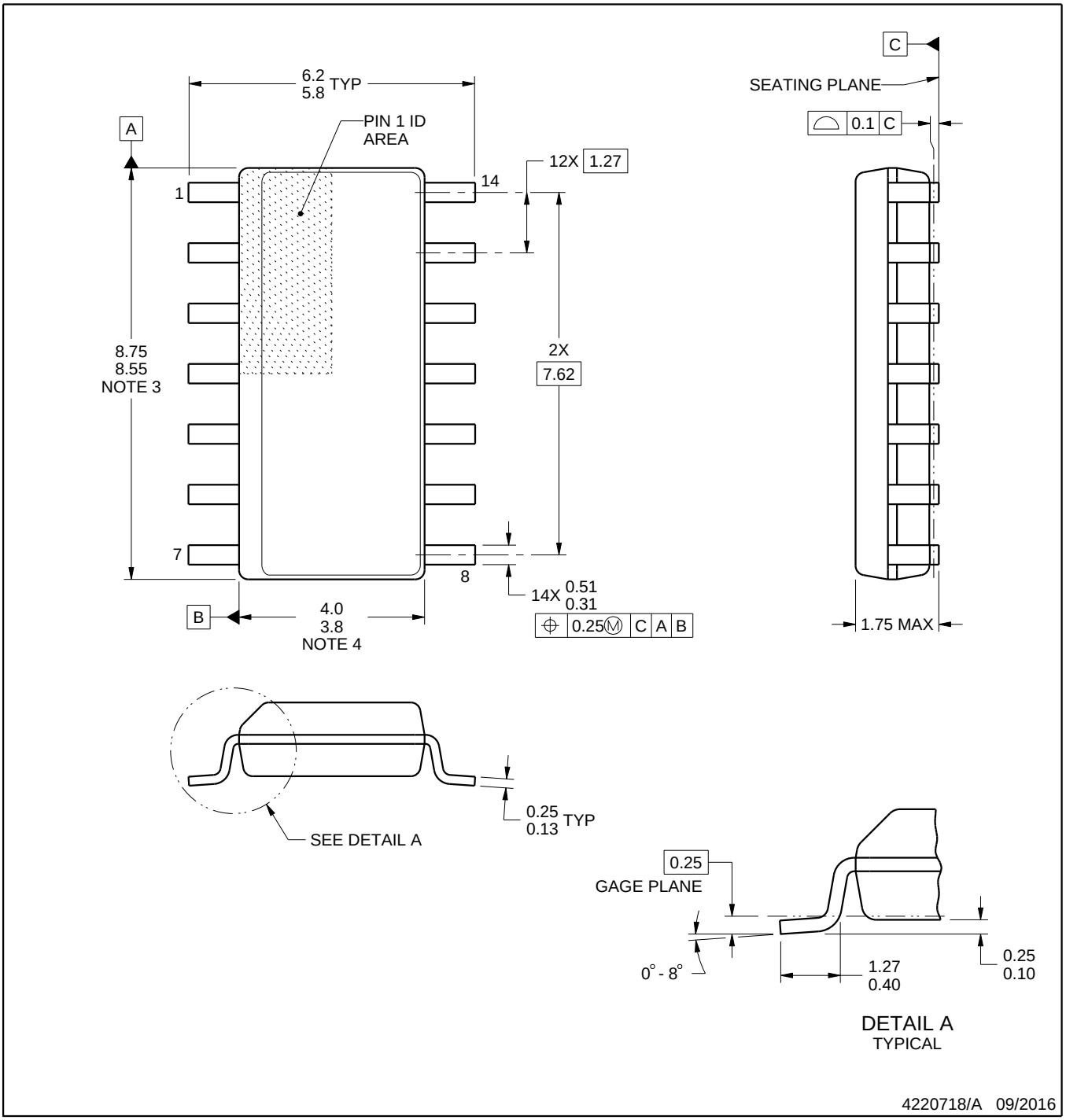


PACKAGE OUTLINE

D0014A

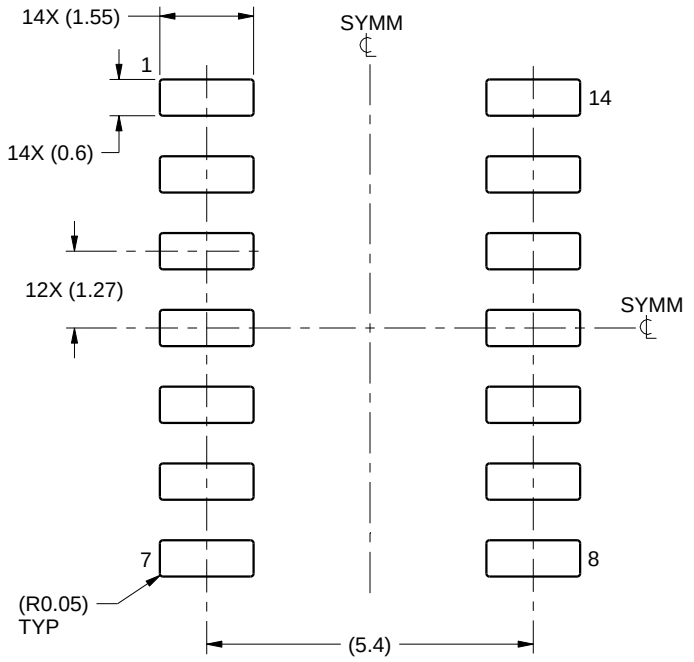
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

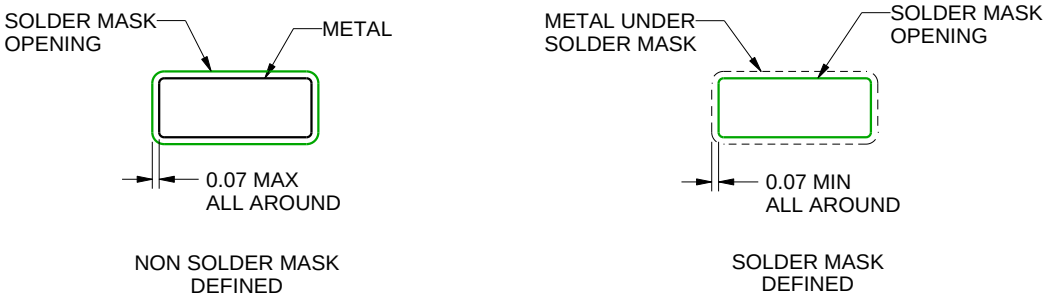


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

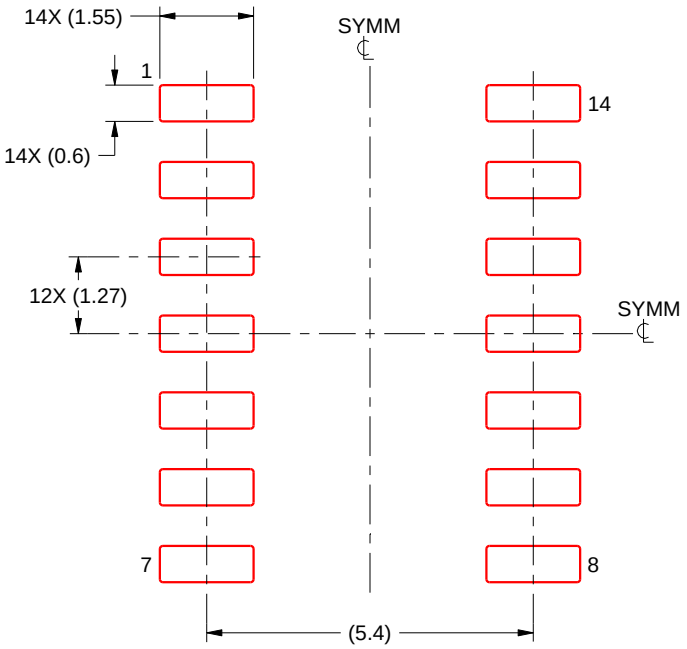
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

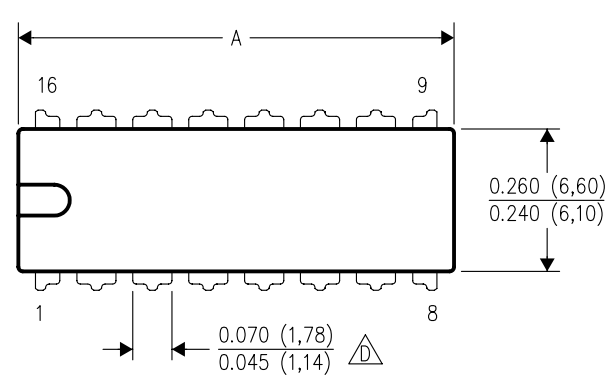
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

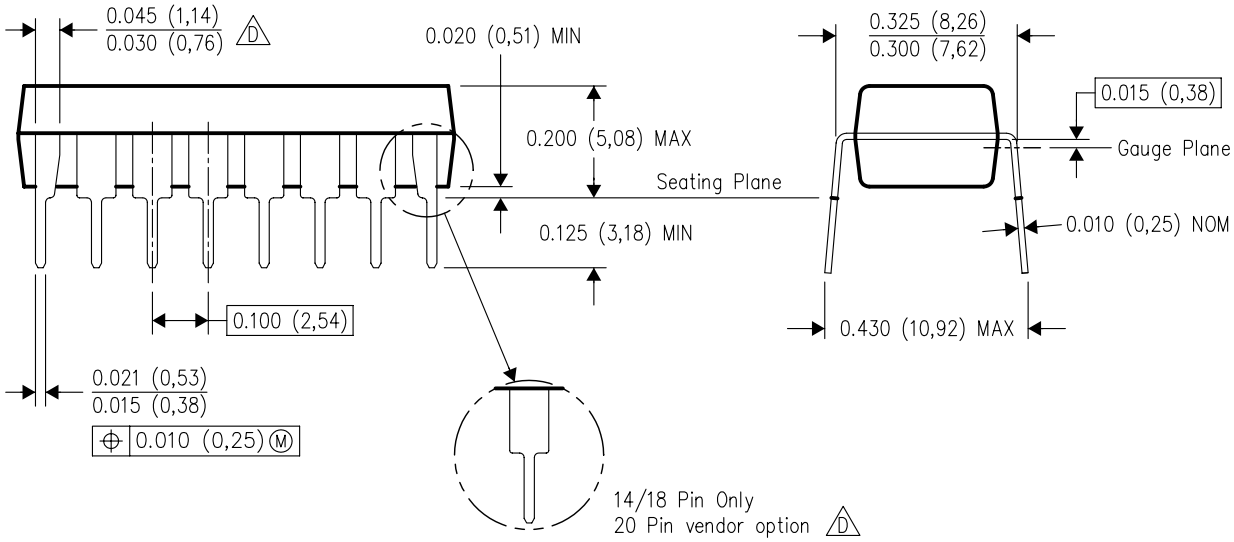
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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