LP2986 Micropower, 200-mA Ultra-Low-Dropout Fixed or Adjustable Voltage Regulator

1 Features

- Wide Supply Voltage Range (16 V Maximum)
- Ultra-Low-Dropout Voltage
- 0.5% Output Voltage Accuracy (A Grade)
- Ensured 200-mA Output Current
- < 1-µA Quiescent Current when Shutdown
- Low GROUND Pin Current at All Loads
- High Peak Current Capability (400 mA Typical)
- Overtemperature/Overcurrent Protection
- −40°C to +125°C Junction Temperature Range

2 Applications

- Cellular Phones
- Palmtop/Laptop Computers
- Camcorders, Personal Stereos, Cameras

3 Description

The LP2986 is a 200-mA high-precision LDO regulator with a wide input voltage supply. The device has two output voltage modes: a fixed-precision output mode and an adjustable output voltage via an external resistive divider.

Using an optimized Vertically Integrated PNP (VIP) process, the LP2986 delivers superior performance:

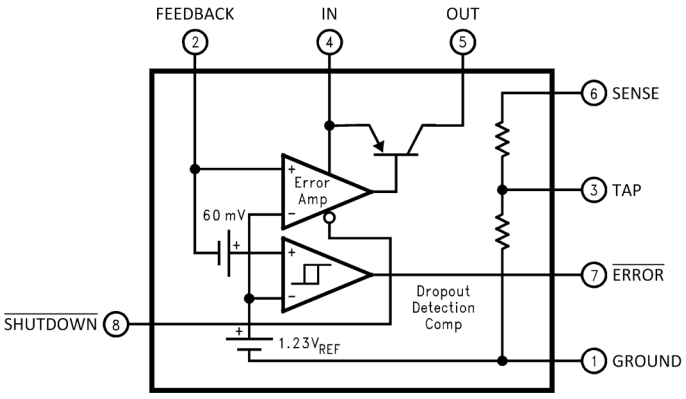
- Dropout Voltage: Typically 180 mV at 200-mA load, and 1 mV at 1-mA load.
- GROUND Pin Current: Typically 1 mA at 200-mA load, and 200 µA at 10-mA load.
- Sleep Mode: The LP2986 draws less than 1 µA quiescent current when $\overline{\text{SHUTDOWN}}$ pin is pulled low.
- $\overline{\text{ERROR}}$ Flag: The built-in $\overline{\text{ERROR}}$ flag goes low when the output drops approximately 5% below nominal.
- Precision Output: The standard product versions available can be pin-strapped (using the internal resistive divider) to provide output voltages of 5 V, 3.3 V, or 3 V with ensured accuracy of 0.5% (A grade) and 1% (standard grade) at room temperature.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP2986	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm
	WSON (8)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (April 2013) to Revision I — **Page**

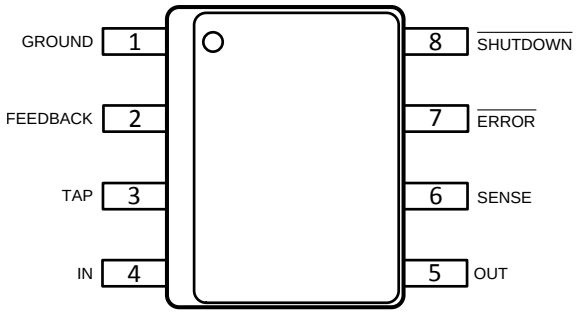
- Added *Device Information* and *Pin Configuration and Functions* sections, *ESD Ratings* table, update *Thermal Values*, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections ... 1
- Deleted Lead Temp from *Abs Max* table (in POA); delete *Heatsinking* sections re: specific packages (outdated info) ... 4

Changes from Revision G (April 2013) to Revision H — **Page**

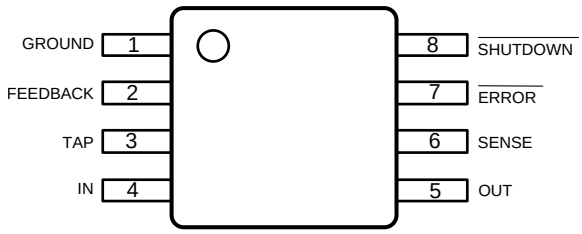
- Changed layout of National Data Sheet to TI format ... 18

5 Pin Configuration and Function

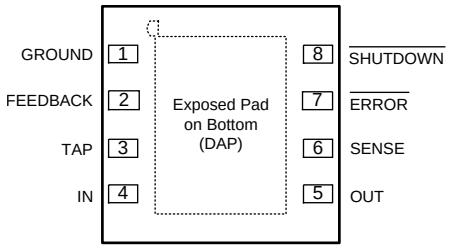
D Package
8-Pin SOIC
Top View



DGK Package
8-Pin VSSOP
Top View



NGN Package
8-Pin WSON
Top View



See *WSON Mounting*.

Pin Functions: All Packages

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{\text{ERROR}}$	7	O	Active-low open-collector error output. Goes low when V_{OUT} drops by 5% of its nominal value.
FEEDBACK	2	I	Determines the output voltage. Connect to TAP (with OUT tied to SENSE) to output the fixed voltage corresponding to the part version, or connect to a resistor divider to adjust the output voltage (see *Typical Applications*).
GROUND	1	—	Ground.
IN	4	I	Input voltage supply.
OUT	5	O	Regulated output.
SENSE	6	I	Connect to OUT (with FEEDBACK tied to TAP) to output the voltage corresponding to the part version (see *Typical Applications*).
$\overline{\text{SHUTDOWN}}$	8	I	Active-high. pull low to showdown the output voltage.
TAP	3	O	Middle tap of the Internal voltage divider. Tie to FEEDBACK (with OUT tied to SENSE) to output the fixed voltage corresponding to the part version (see *Typical Applications*).
DAP (Thermal Pad - WSON only)	√	—	The exposed thermal pad on the bottom of the WSON package should be connected to a copper thermal pad on the PCB under the package. The use of thermal vias to remove heat from the package into the PCB is recommended. Connect the thermal pad to ground potential or leave floating. Do not connect the thermal pad to any potential other than the same ground potential seen at device pin 1. For additional information on using TI's non-pullback WSON package, see Application Note AN-1187 *Leadless Leadframe Package (LLP)* (SNOA401).

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1][2]

	MIN	MAX	UNIT
Input supply voltage (survival)	–0.3	16	V
Input supply voltage (operating)	2.1	16	V
$\overline{\text{SHUTDOWN}}$ pin	–0.3	16	V
FEEDBACK pin	–0.3	5	V
Output voltage (survival)[3]	–0.3	16	V
I_{OUT} (survival)	Short-circuit protected		
Input-output voltage (survival)[4]	–0.3	16	V
Power dissipation[5]	Internally limited		
Storage temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) If used in a dual-supply system where the regulator load is returned to a negative supply, the LM2986 output must be diode-clamped to ground.
(4) The output PNP structure contains a diode between the IN and OUT pins that is normally reverse-biased. Forcing the output above the input will turn on this diode and may induce a latch-up mode which can damage the part (see *Reverse Input-Output Voltage*).
(5) The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction-to-ambient thermal resistance, $R_{\theta JA}$, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{(MAX)} = T_{J(MAX)} – T_A / R_{\theta JA}$
For improved thermal resistance and power dissipation for the WSON package, refer to Texas Instruments Application Note *Leadless Leadframe Package (LLP)* (SNOA401). Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	All pins except FEEDBACK, IN, and TAP	±2000	V
			FEEDBACK pin	±500	
			IN pin	±1000	
			TAP pin	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply input voltage	2.1		16	V
Enable input voltage	0		16	V
Output current			200	mA
Operating junction temperature	−40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		LP2986			UNIT
		D (SOIC)	DGK (VSSOP)	NGN (WSON)	
		8 PINS			
$R_{\theta JA}$[2]	Junction-to-ambient thermal resistance, High-K	114.4	156.5	37.8[3]	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	61.4	51.0	28.58	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	55.5	76.5	15.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.8	4.9	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	54.9	75.2	15.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	4.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Thermal resistance value $R_{\theta JA}$ is based on the EIA/JEDEC High-K printed circuit board defined by: JESD51-7 - *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages.*
(3) The PCB for the NGN (WSON) package $R_{\theta JA}$ includes four (4) thermal vias under the exposed thermal pad per EIA/JEDEC JESD51-5.

6.5 Electrical Characteristics

Unless otherwise specified: T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1 V, I_{OUT} = 1 mA, C_{OUT} = 4.7 µF, C_{IN} = 2.2 µF, $V_{\overline{SD}}$ = 2 V.

PARAMETER		TEST CONDITIONS	LP2986AI-X.X[1]			LP2986I-X.X[1]			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OUT}	Output voltage (5-V version)		4.975	5	5.025	4.95	5	5.05	V
		0.1 mA < I_{OUT} < 200 mA	4.96	5	5.04	4.92	5	5.08	
		0.1 mA < I_{OUT} < 200 mA –40°C ≤ T_J ≤ 125°C	4.91		5.09	4.86		5.14	
	Output voltage (3.3-V version)		3.283	3.3	3.317	3.267	3.3	3.333	V
		0.1 mA < I_{OUT} < 200 mA	3.274	3.3	3.326	3.247	3.3	3.353	
		0.1 mA < I_{OUT} < 200 mA –40°C ≤ T_J ≤ 125°C	3.241		3.359	3.208		3.392	
	Output voltage (3-V version)		2.985	3	3.015	2.97	3	3.03	V
		0.1 mA < I_{OUT} < 200 mA	2.976	3	3.024	2.952	3	3.048	
		0.1 mA < I_{OUT} < 200 mA –40°C ≤ T_J ≤ 125°C	2.946		3.054	2.916		3.084	
$\Delta V_{OUT}/\Delta V_{IN}$	Output voltage line regulation	$V_{OUT(NOM)}$ + 1 V ≤ V_{IN} ≤ 16 V		0.007	0.014		0.007	0.014	%/V
		$V_{OUT(NOM)}$ + 1 V ≤ V_{IN} ≤ 16 V, –40°C ≤ T_J ≤ 125°C			0.032			0.032	
$V_{IN} – V_{OUT}$	Dropout voltage[2]	I_{OUT} = 100 µA		1	2		1	2	mV
		I_{OUT} = 100 µA –40°C ≤ T_J ≤ 125°C			3.5			3.5	
		I_{OUT} = 75 mA		90	120		90	120	
		I_{OUT} = 75 mA –40°C ≤ T_J ≤ 125°C			170			170	
		I_{OUT} = 200 mA		180	230		180	230	
		I_{OUT} = 200 mA –40°C ≤ T_J ≤ 125°C			350			350	

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate TI's Average Outgoing Quality Level (AOQL).
(2) Dropout voltage is defined as the input to output differential at which the output voltage drops 100 mV below the value measured with a 1-V differential.

Electrical Characteristics (continued)

Unless otherwise specified: T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1 V, I_{OUT} = 1 mA, C_{OUT} = 4.7 µF, C_{IN} = 2.2 µF, $V_{\overline{SD}}$ = 2 V.

PARAMETER		TEST CONDITIONS	LP2986AI-X.X(1)			LP2986I-X.X(1)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{GND}	Ground pin current	I_{OUT} = 100 µA		100	120		100	120	µA
		I_{OUT} = 100 µA –40°C ≤ T_J ≤ 125°C			150		110	150	
		I_{OUT} = 75 mA		500	800		500	800	
		I_{OUT} = 75 mA –40°C ≤ T_J ≤ 125°C			1400			1400	
		I_{OUT} = 200 mA		1	2.1		1	2.1	mA
		I_{OUT} = 200 mA –40°C ≤ T_J ≤ 125°C			3.7			3.7	
		$V_{\overline{SD}}$ < 0.3 V		0.05			0.05		µA
		$V_{\overline{SD}}$ < 0.3 V –40°C ≤ T_J ≤ 125°C			1.5			1.5	
$I_{OUT(PK)}$	Peak output current	V_{OUT} ≥ $V_{OUT(NOM)}$ − 5%	250	400		250	400		mA
$I_{OUT(MAX)}$	Short-circuit current	R_L = 0 (steady state)(3)		400			400		mA
e_n	Output noise voltage (RMS)	BW = 300 Hz to 50 kHz, C_{OUT} = 10 µF		160			160		μV_{RMS}
$\Delta V_{OUT}/\Delta V_{IN}$	Ripple rejection	f = 1 kHz, C_{OUT} = 10 µF		65			65		dB
$\Delta V_{OUT}/\Delta T_D$	Output voltage temperature coefficient	See(4)		20			20		ppm/°C
FEEDBACK PIN									
V_{FB}	FEEDBACK pin voltage		1.21	1.23	1.25	1.2	1.23	1.26	V
		–40°C ≤ T_J ≤ 125°C	1.2		1.26	1.19		1.27	
		See(5)	1.19		1.28	1.18		1.29	
$\Delta V_{FB}/\Delta T$	FEEDBACK pin voltage temperature coefficient	See(6)		20			20		ppm/°C
I_{FB}	FEEDBACK pin bias current	I_{OUT} = 200 mA		150	330		150	330	nA
		I_{OUT} = 200 mA –40°C ≤ T_J ≤ 125°C			760			760	
$\Delta I_{FB}/\Delta T$	FEEDBACK pin bias current temperature coefficient	See(6)		0.1			0.1		nA/°C
$\overline{\text{SHUTDOWN}}$ INPUT									
$V_{\overline{SD}}$	$\overline{SD}$ Input voltage(7)	V_H = Output ON		1.4			1.4		V
		V_H = Output ON –40°C ≤ T_J ≤ 125°C	1.6			1.6			
		V_L = Output OFF		0.55			0.55		µA
		V_L = Output OFF –40°C ≤ T_J ≤ 125°C			0.18			0.18	
$I_{\overline{SD}}$	$\overline{SD}$ Input current	$V_{\overline{SD}}$ = 0 V		0			0		V
		$V_{\overline{SD}}$ = 0 V, –40°C ≤ T_J ≤ 125°C			–1			–1	
		$V_{\overline{SD}}$ = 5 V		5			5		µA
		$V_{\overline{SD}}$ = 5 V, –40°C ≤ T_J ≤ 125°C			15			15	

(3) See the *Typical Characteristics* section.
(4) Temperature coefficient is defined as the maximum (worst-case) change divided by the total temperature range.
(5) V_{FB} ≤ V_{OUT} ≤ (V_{IN} − 1), 2.5 V ≤ V_{IN} ≤ 16 V, 100 µA ≤ I_L ≤ 200 mA, T_J ≤ 125°C.
(6) Temperature coefficient is defined as the maximum (worst-case) change divided by the total temperature range.
(7) To prevent mis-operation, the $\overline{\text{SHUTDOWN}}$ pin must be driven by a signal that swings above V_H and below V_L with a slew rate not less than 40 mV/µs (see *Application and Implementation*).

Electrical Characteristics (continued)

Unless otherwise specified: T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1 V, I_{OUT} = 1 mA, C_{OUT} = 4.7 µF, C_{IN} = 2.2 µF, $V_{\overline{SD}}$ = 2 V.

PARAMETER		TEST CONDITIONS	LP2986AI-X.X(1)			LP2986I-X.X(1)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$\overline{\text{ERROR}}$ COMPARATOR									
I_{OH}	Output HIGH leakage	V_{OH} = 16 V		0.01	1		0.001	1	µA
		V_{OH} = 16 V, –40°C ≤ T_J ≤ 125°C			2		0.001	2	
V_{OL}	Output LOW voltage	V_{IN} = $V_{OUT(NOM)}$ − 0.5 V $I_{OUT(COMP)}$ = 300 µA		150	220		150	220	µA
		V_{IN} = $V_{OUT(NOM)}$ − 0.5 V $I_{OUT(COMP)}$ = 300 µA –40°C ≤ T_J ≤ 125°C			350			350	mV
$V_{THR(MAX)}$	Upper threshold voltage		−5.5	−4.6	−3.5	−5.5	−4.6	−3.5	%V_{OUT}
		–40°C ≤ T_J ≤ 125°C	−7.7		−2.5	−7.7		−2.5	
$V_{THR(MIN)}$	Lower threshold voltage		−8.9	−6.6	−4.9	−8.9	−6.6	−4.9	%V_{OUT}
		–40°C ≤ T_J ≤ 125°C	−13		−3.3	−13		−3.3	
HYST	Hysteresis			2			2		

6.6 Typical Characteristics

Unless otherwise specified: T_A = 25°C, C_{OUT} = 4.7 µF, C_{IN} = 2.2 µF, $\overline{SD}$ is tied to V_{IN}, V_{IN} = V_O(NOM) + 1 V, I_L = 1 mA.

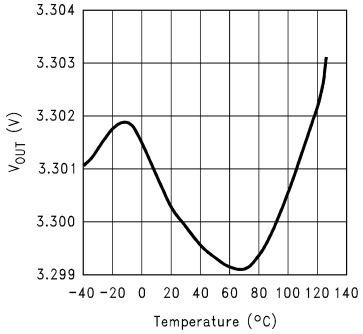


Figure 1. V_{OUT} vs Temperature

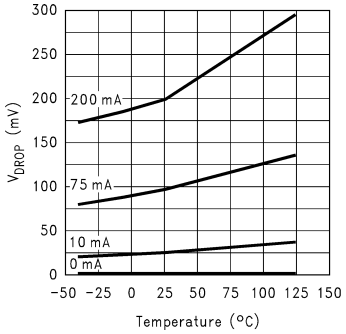


Figure 2. Dropout Voltage vs Temperature

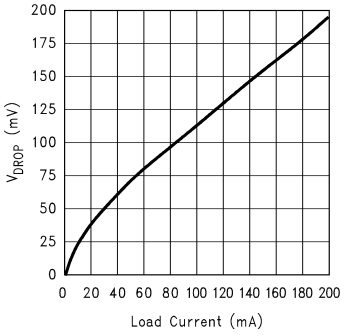


Figure 3. Dropout Voltage vs Load Current

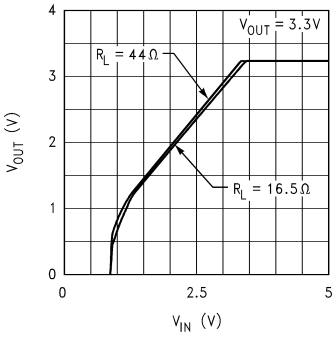


Figure 4. Dropout Characteristics

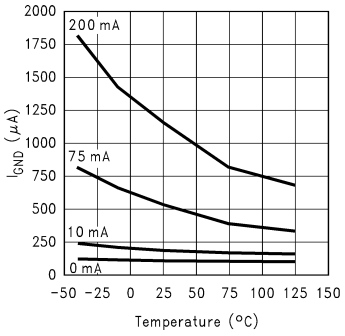


Figure 5. Ground Pin Current vs Temperature And Load

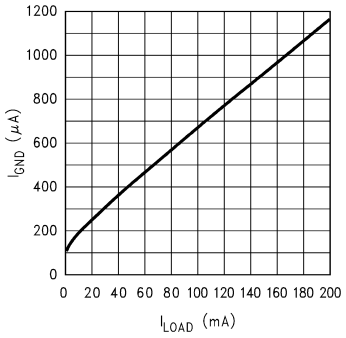


Figure 6. Ground Pin Current vs Load Current

Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C, C_{OUT} = 4.7 µF, C_{IN} = 2.2 µF, $\overline{SD}$ is tied to V_{IN}, V_{IN} = V_O(NOM) + 1 V, I_L = 1 mA.

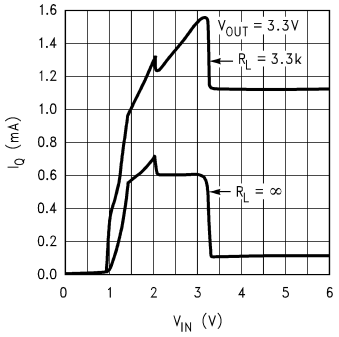


Figure 7. Input Current vs V_{IN}

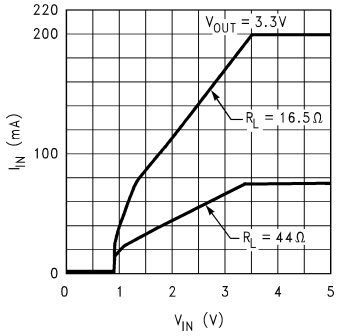


Figure 8. Input Current vs V_{IN}

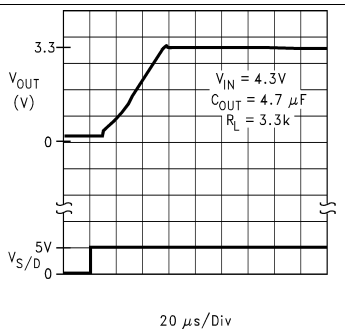


Figure 9. Turnon Waveform

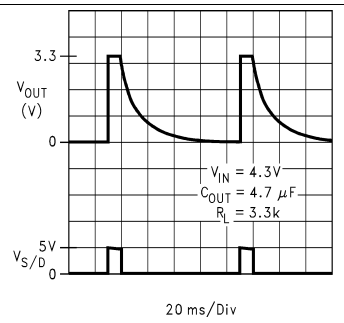


Figure 10. Turnoff Waveform

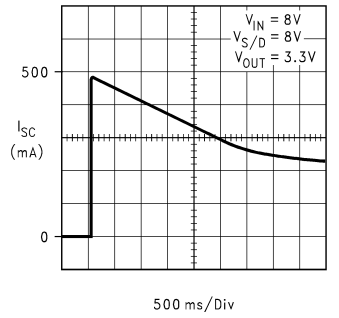


Figure 11. Short-Circuit Current

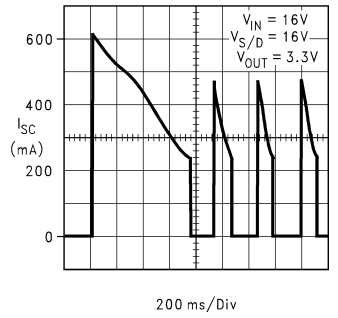


Figure 12. Short-Circuit Current

Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C, C_{OUT} = 4.7 µF, C_{IN} = 2.2 µF, $\overline{SD}$ is tied to V_{IN}, V_{IN} = V_O(NOM) + 1 V, I_L = 1 mA.

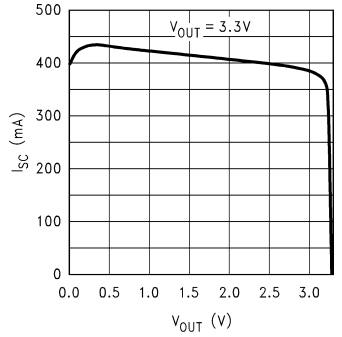


Figure 13. Short-Circuit Current vs Output Voltage

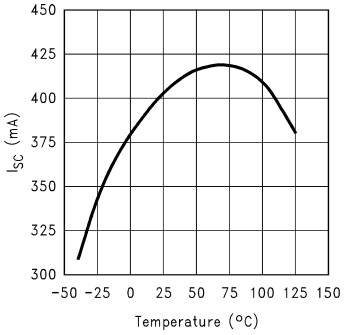


Figure 14. Instantaneous Short-Circuit Current vs Temperature

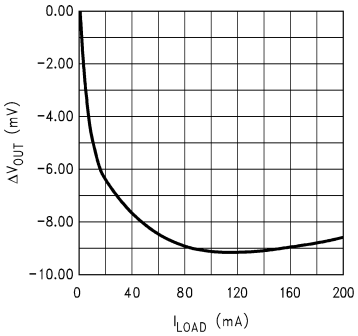


Figure 15. DC Load Regulation

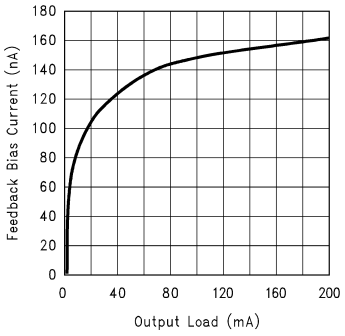


Figure 16. Feedback Bias Current vs Load

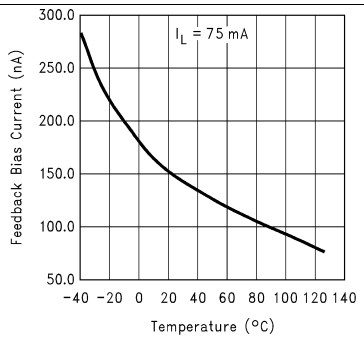


Figure 17. Feedback Bias Current vs Temperature

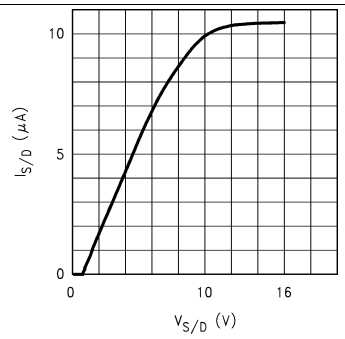


Figure 18. $\overline{SHUTDOWN}$ Pin Current vs $\overline{SHUTDOWN}$ Pin Voltage

Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C, C_{OUT} = 4.7 µF, C_{IN} = 2.2 µF, $\overline{SD}$ is tied to V_{IN}, V_{IN} = V_O(NOM) + 1 V, I_L = 1 mA.

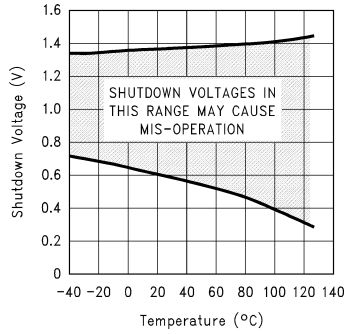


Figure 19. Shutdown Voltage vs Temperature

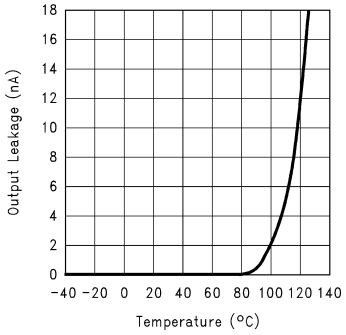


Figure 20. Input-to-Output Leakage vs Temperature

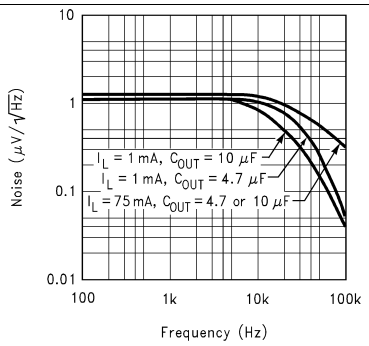


Figure 21. Output Noise Density

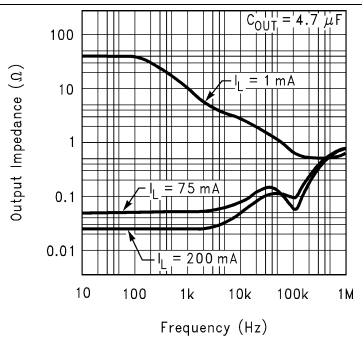


Figure 22. Output Impedance vs Frequency

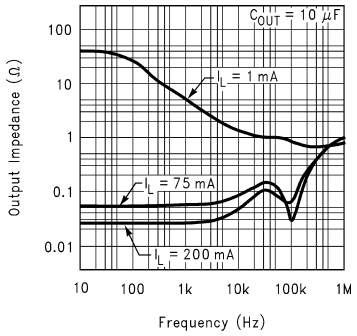


Figure 23. Output Impedance vs Frequency

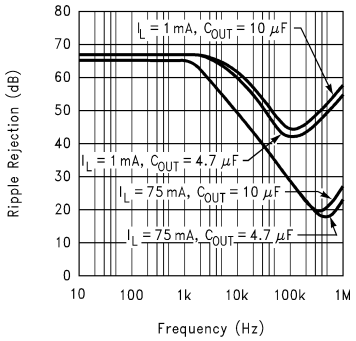


Figure 24. Ripple Rejection

Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C, C_{OUT} = 4.7 µF, C_{IN} = 2.2 µF, $\overline{SD}$ is tied to V_{IN}, V_{IN} = V_O(NOM) + 1 V, I_L = 1 mA.

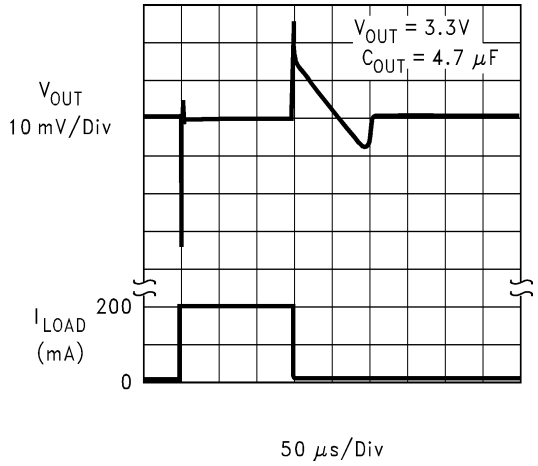


Figure 25. Load Transient Response

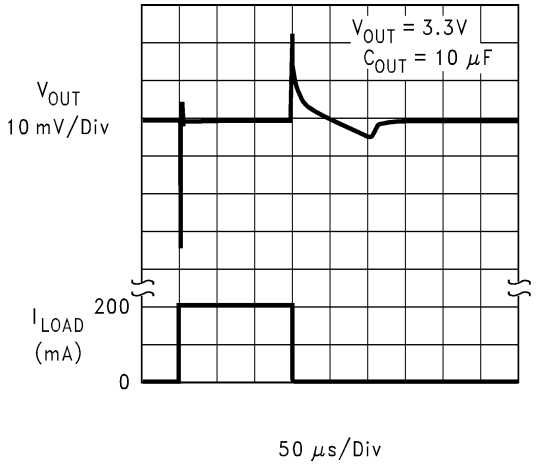


Figure 26. Load Transient Response

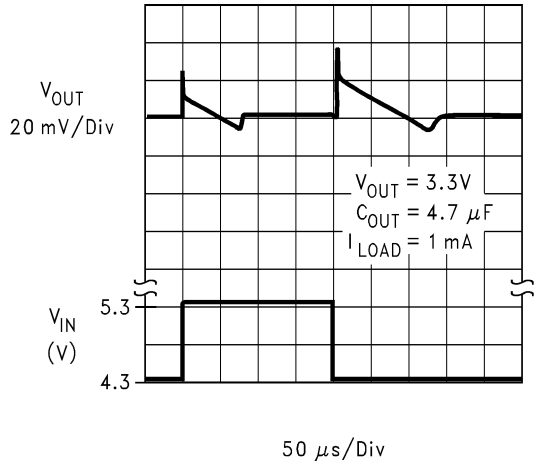


Figure 27. Line Transient Response

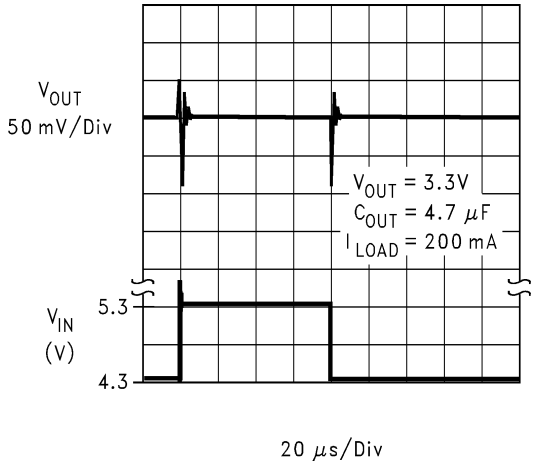


Figure 28. Line Transient Response

7 Detailed Description

7.1 Overview

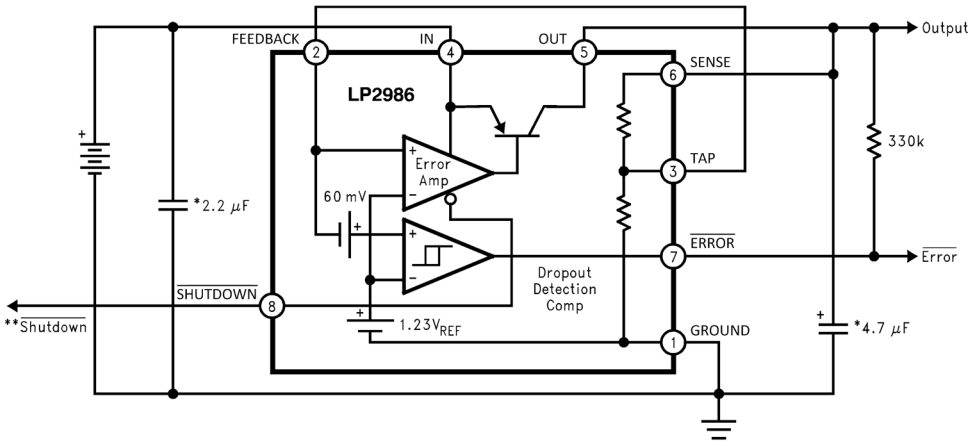
The LP2986 is a bipolar, low-dropout (LDO) voltage regulator that can accommodate a wide input supply-voltage range of up to 16 V. The LP2986 LDO is able to output either a fixed or adjustable output from the same device. By tying the OUT and SENSE pins together, and the FEEDBACK and TAP pins together, the LP2986 device outputs a fixed 5 V, 3.3 V, or 3 V (depending on the version). Alternatively, by leaving the SENSE and TAP pins open and connecting FEEDBACK to an external resistor divider, the output can be set to any value between 2.1 V to 16 V. The LP2986 device also offers additional functionality that makes it particularly suitable for battery-powered applications. For example, a logic-compatible shutdown feature allows the regulator to be put in standby mode for power savings. In addition, there is a built-in supervisor reset function in which the ERROR output goes low when V_{OUT} drops by 5% of its nominal value for whatever reasons – due to a drop in V_{IN}, current limiting, or thermal shutdown.

The LP2986 devices are designed to minimize all error contributions to the output voltage. With a tight output tolerance (0.5% at 25°C), a very low output voltage temperature coefficient (20 ppm typical), extremely good line and load regulation and remote sensing capability, the part can be used as either low-power voltage reference or 200-mA regulator.

Multiple features of the device include:

- Very high-accuracy 1.23-V reference
- Sleep mode
- Error flag output
- Internal protection circuitry, such as overcurrent limit, and thermal shutdown.

7.2 Functional Block Diagram



* Minimum capacitance shown to assure stability, but may be increased without limit. Larger output capacitor provides improved dynamic response.

** Shutdown input must be actively terminated. Tie to V_{IN} if not used.

7.3 Feature Description

7.3.1 High-Accuracy Output Voltage

With special careful design to minimize all contributions to the output voltage error, the LP2989 distinguishes itself as a very high output-voltage-accuracy micro-power LDO. This includes a tight initial tolerance (0.5% typical, A grade), extremely good line regulation (0.007%/V typical).

Feature Description (continued)

7.3.2 Error Detection Comparator Output

The LP2989 will generate a logic low output whenever its output falls out of regulation by more than approximately 5% below nominal. Because the $\overline{\text{ERROR}}$ comparator has an open-collector output, an external pull-up resistor is required to pull the output up to V_{OUT} or another supply voltage (up to 16 V). The output of the comparator is rated to sink up to 300 µA. If $\overline{\text{ERROR}}$ pin is not used, it can be left open.

Because the $\overline{\text{ERROR}}$ comparator has an open-collector output, an external pull-up resistor is required to pull the output up to VOUT or another supply voltage (up to 16 V). The output of the comparator is rated to sink up to 300 µA. If $\overline{\text{ERROR}}$ pin is not used, it can be left open.

7.3.3 Thermal Protection

The device contains a thermal shutdown protection circuit to turn off the output current when excessive heat is dissipated in the LDO. The circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown degrades its reliability.

7.3.4 Short-Circuit Protection (Current Limit)

The internal current limit circuit is used to protect the LDO against high-load current faults or shorting events. The LDO is not designed to operate in a steady-state current limit. During a current-limit event, the LDO sources constant current. Therefore, the output voltage falls when load impedance decreases. Note also that if a current limit occurs and the resulting output voltage is low, excessive power may be dissipated across the LDO, resulting in a thermal shutdown of the output.

7.4 Device Functional Modes

7.4.1 Shutdown Mode

The LP2986 is shut off by driving the shutdown input low, and turned on by pulling it high. If this feature is not to be used, the $\overline{\text{SHUTDOWN}}$ input should be tied to V_{IN} to keep the regulator output on at all times.

To assure proper operation, the signal source used to drive the $\overline{\text{SHUTDOWN}}$ input must be able to swing above and below the specified turnon/turnoff voltage thresholds listed as V_H and V_L, respectively (see *Typical Characteristics*).

Since the $\overline{\text{SHUTDOWN}}$ input comparator does not have hysteresis, It is also important that the turnon (and turnoff) voltage signals applied to the $\overline{\text{SHUTDOWN}}$ input have a slew rate which is not less than 40 mV/µs when moving between the V_H and V_L thresholds.

CAUTION

The regulator output state (either On or Off) cannot be specified if a slow-moving AC (or DC) signal is applied that is in the range between V_H and V_L.

7.4.2 Fixed or Adjustable Regulated Output

A unique feature of the LP2986 device is its ability to output either a fixed voltage or an adjustable voltage, depending on the external pin connections. To output the internally programmed fixed voltage, tie the SENSE pin to the OUTPUT pin and the FEEDBACK pin to the TAP pin.

Alternatively, a user-programmable voltage ranging from the internal reference to a 16-V maximum can be set by using an external resistor divider pair. The resistor divider is tied to V_{OUT}, and the divided-down voltage is tied directly to FEEDBACK for comparison against the internal voltage reference. To satisfy the steady-state condition in which its two inputs are equal, the error amplifier drives the output to equal to Equation 1. For detailed information see *Application and Implementation*.

8 Application and Implementation

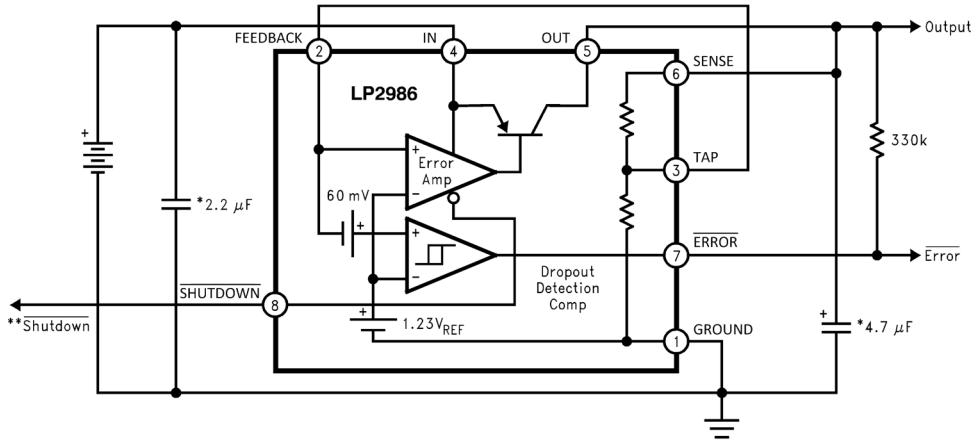
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP2986 can provide 200-mA output current with 2.1-V to 16-V input. It is stable with a minimum of 4.7-µF ceramic output capacitor. An input capacitor of (≥ 2.2 µF) is required. An optional external bypass capacitor reduces the output noise without slowing down the load transient response. Typical output noise is 160 μV_{RMS} at frequencies from 300 Hz to 50 kHz. Typical power supply rejection is 65 dB at 1 kHz.

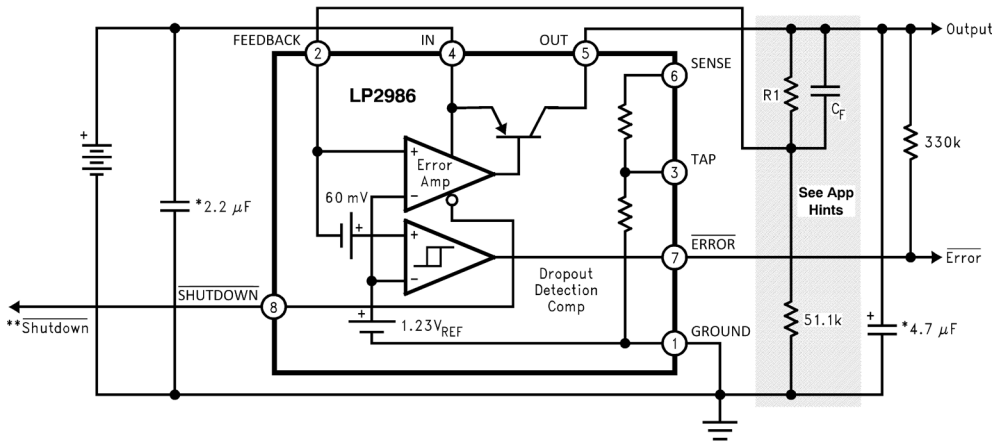
8.2 Typical Applications



* Minimum capacitance shown to assure stability, but may be increased without limit. Larger output capacitor provides improved dynamic response.

** Shutdown input must be actively terminated. Tie to V_{IN} if not used.

Figure 29. Application Using Internal Resistive Divider



* Minimum capacitance shown to assure stability, but may be increased without limit. Larger output capacitor provides improved dynamic response.

** Shutdown input must be actively terminated. Tie to V_{IN} if not used.

Figure 30. Application Using External Divider

Typical Applications (continued)

8.2.1 Design Requirements

For typical ultra-low-dropout linear regulator applications, use the parameters listed in Table 1.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	4.3 V
Output voltage	3.3 V
Output current	200 mA (maximum)
RMS noise, 300 Hz to 50 kHz	150 μV_{RMS} typical
PSRR at 1 kHz	65 dB typical

8.2.2 Detailed Design Procedure

8.2.2.1 Using an External Resistive Divider

The LP2986 output voltage can be programmed using an external resistive divider. Figure 30 shows a typical circuit application using external resistive divider.

The resistor connected between the FEEDBACK pin and ground should be 51.1 kΩ. The value for the other resistor (R1) connected between the FEEDBACK pin and the regulated output is found using the formula:

$$V_{OUT} = V_{FB} \times (1 + (R1 / 51.1k)) \quad (1)$$

It should be noted that the 25 µA of current flowing through the external divider is approximately equal to the current saved by not connecting the internal divider, which means the quiescent current is not increased by using external resistors.

A lead compensation capacitor (C_F) must also be used to place a zero in the loop response at about 50 kHz. The value for C_F can be found using:

$$C_F = 1/(2\pi \times R1 \times 50k) \quad (2)$$

A good quality capacitor must be used for C_F to ensure that the value is accurate and does not change significantly over temperature. Mica or ceramic capacitors can be used, assuming a tolerance of ±20% or better is selected.

If a ceramic is used, select one with a temperature coefficient of NPO, COG, Y5P, or X7R. Capacitor types Z5U, Y5V, and Z4V can not be used because their value varies more that 50% over the −25°C to +85°C temperature range.

8.2.2.2 External Capacitors

Like any low-dropout regulator, external capacitors are required to assure stability. These capacitors must be correctly selected for proper performance.

8.2.2.2.1 Input Capacitor

An input capacitor (≥ 2.2 µF) is required between the LP2986 input and ground (amount of capacitance may be increased without limit).

This capacitor must be located a distance of not more than 0.5 inches from the input pin and returned to a clean analog ground. Any good quality ceramic or tantalum may be used for this capacitor.

8.2.2.2.2 Output Capacitor

The output capacitor must meet the requirement for minimum amount of capacitance and also have an appropriate equivalent series resistance (ESR) value.

Curves are provided which show the allowable ESR range as a function of load current for various output voltages and capacitor values (see Figure 31 and Figure 32).

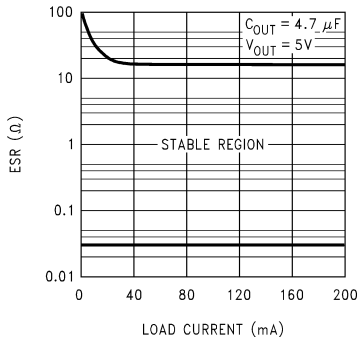


Figure 31. ESR Curves For 5-V Output

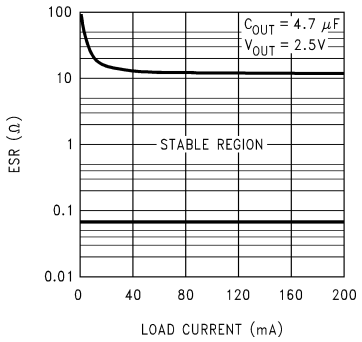


Figure 32. ESR Curves for 2.5-V Output

NOTE

The output capacitor must maintain its ESR in the stable region *over the full operating temperature range of the application* to assure stability.

The minimum required amount of output capacitance is 4.7 µF. Output capacitor size can be increased without limit.

It is important to remember that capacitor tolerance and variation with temperature must be taken into consideration when selecting an output capacitor so that the minimum required amount of output capacitance is provided over the full operating temperature range. A good tantalum capacitor will show very little variation with temperature, but a ceramic may not be as good (see *Capacitor Characteristics*).

8.2.2.3 Capacitor Characteristics

8.2.2.3.1 Tantalum

The best choice for size, cost, and performance are solid tantalum capacitors. Available from many sources, their typical ESR is very close to the ideal value required on the output of many LDO regulators.

Tantalums also have good temperature stability: a 4.7 µF was tested and showed only a 10% decline in capacitance as the temperature was decreased from +125°C to −40°C. The ESR increased only about 2:1 over the same range of temperature.

However, it should be noted that the increasing ESR at lower temperatures present in all tantalums can cause oscillations when marginal quality capacitors are used (where the ESR of the capacitor is near the upper limit of the stability range at room temperature).

8.2.2.3.2 Ceramic

For a given amount of a capacitance, ceramics are usually larger and more costly than tantalums.

Be warned that the ESR of a ceramic capacitor can be low enough to cause instability: a 2.2-µF ceramic capacitor was measured and found to have an ESR of about 15 mΩ.

If a ceramic capacitor is to be used on the LP2986 output, a 1-Ω resistor should be placed in series with the capacitor to provide a minimum ESR for the regulator.

Another disadvantage of ceramic capacitors is that their capacitance varies a lot with temperature:

Large ceramic capacitors are typically manufactured with the Z5U temperature characteristic, which results in the capacitance dropping by a 50% as the temperature goes from +25°C to 80°C.

This means you have to buy a capacitor with twice the minimum C_{OUT} to assure stable operation up to 80°C.

8.2.2.3.3 Aluminum

The large physical size of aluminum electrolytics makes them unattractive for use with the LP2986. Their ESR characteristics are also not well suited to the requirements of LDO regulators.

The ESR of an aluminum electrolytic is higher than a tantalum, and it also varies greatly with temperature.

A typical aluminum electrolytic can exhibit an ESR increase of 50× when going from +20°C to −40°C. Also, some aluminum electrolytics can not be used below −25°C because the electrolyte will freeze.

8.2.2.4 Reverse Input-Output Voltage

The PNP power transistor used as the pass element in the LP2986 has an inherent diode connected between the regulator output and input.

During normal operation (where the input voltage is higher than the output) this diode is reverse-biased.

However, if the output voltage is pulled above the input, or the input voltage is pulled below the output, this diode will turn ON and current will flow into the regulator OUT pin.

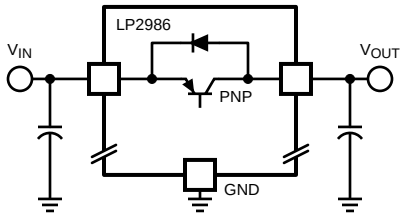


Figure 33. Inherent Diode

In such cases, a parasitic SCR can latch which will allow a high current to flow into V_{IN} (and out the GROUND pin), which can damage the part.

In any application where the output voltage may be higher than the input, an external Schottky diode must be connected from V_{IN} to V_{OUT} (cathode on V_{IN}, anode on V_{OUT}), to limit the reverse voltage across the LP2986 to 0.3 V (see *Absolute Maximum Ratings*).

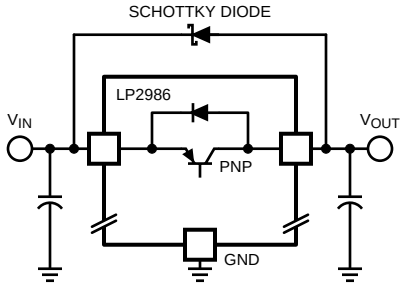


Figure 34. Inherent and External Schottky Diodes

8.2.2.5 WSON Package Devices

The LP2986 is offered in the 8-pin WSON surface mount package to allow for increased power dissipation compared to the 8-pin SOIC-8 and 8-pin VSSOP. For details on WSON thermal performance as well as mounting and soldering specifications, refer to *WSON Mounting*.

8.2.3 Application Curves

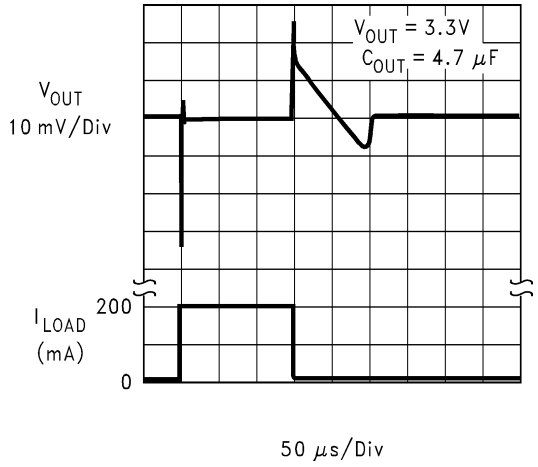


Figure 35. Load Transient Response

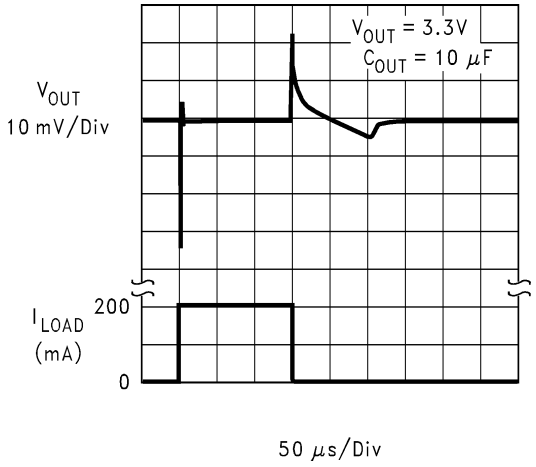


Figure 36. Load Transient Response

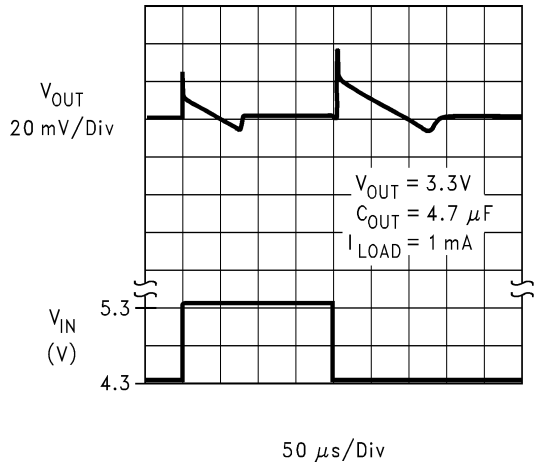


Figure 37. Line Transient Response

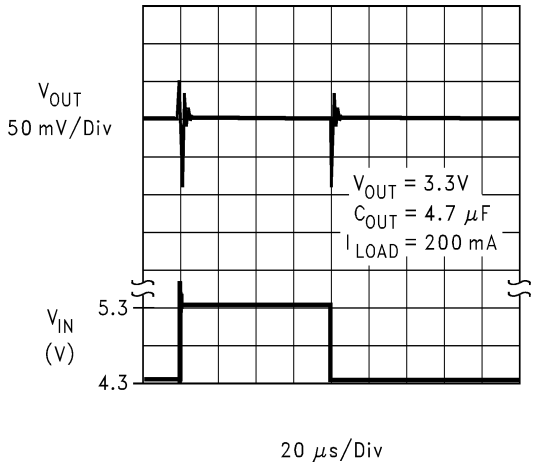


Figure 38. Line Transient Response

9 Power Supply Recommendations

The LP2986 is designed to operate from an input voltage supply range from 2.1 V to 16 V. The input voltage range provides adequate headroom for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO circuit connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability. A ground reference plane is also recommended and is either embedded in the PCB itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device. In most applications, this ground plane is necessary to meet thermal requirements.

10.2 Layout Examples

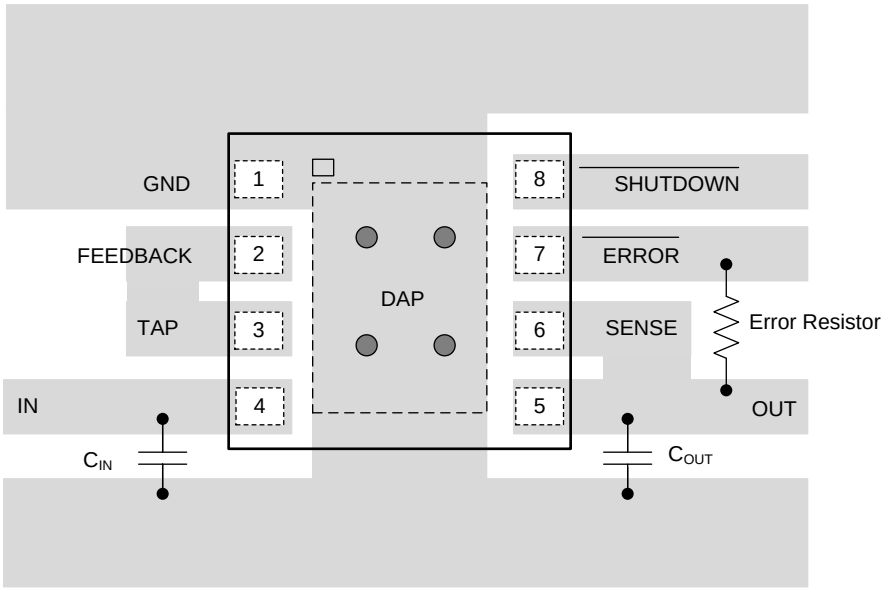


Figure 39. WSON Layout with Internal Resistor Divider

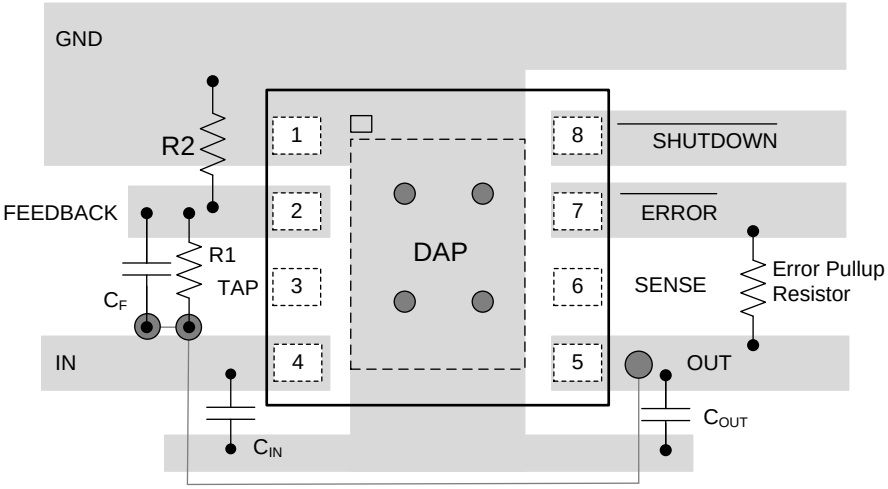


Figure 40. WSON Layout with External Resistor Divider

10.3 WSON Mounting

The LDC08A (pullback) 8-pin WSON package requires specific mounting techniques which are detailed in Texas Instruments Application Note *Leadless Leadframe Package (LLP)* (SNOA401). Referring to the section *PCB Design Recommendations* in SNOA401, the pad style which should be used with this WSON package is the NSMD (non-solder mask defined) type. Additionally, for optimal reliability, there is a recommended 1:1 ratio between the package pad and the PCB pad for the pullback WSON.

The thermal dissipation of the WSON package is directly related to the printed circuit board construction and the amount of additional copper area connected to the DAP.

The DAP (exposed pad) on the bottom of the WSON package is connected to the die substrate with a conductive die attach adhesive. The DAP has no direct electrical (wire) connection to any of the eight pins. There is a parasitic PN junction between the die substrate and the device ground. As such, it is strongly recommend that the DAP be connected directly to the ground at device pin 1 (GROUND). Alternately, but not recommended, the DAP may be left floating (that is, no electrical connection). The DAP must not be connected to any potential other than ground.

For the LP2986 in the NGN 8-pin WSON package, the junction-to-case thermal rating ($R_{\theta JC}$) is 4.4°C/W, where the case is on the bottom of the package at the center of the DAP.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For additional information, see the following:

Texas Instruments Application Note *Leadless Leadframe Package (LLP)* (SNOA401).

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP2986AILD-3.3/NO.A	Active	Production	WSON (NGN) | 8	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	L005A
LP2986AILD-3.3/NOPB	Active	Production	WSON (NGN) | 8	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	L005A
LP2986AILDX-3.3/NO.A	Active	Production	WSON (NGN) | 8	4500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	L005A
LP2986AILDX-3.3/NOPB	Active	Production	WSON (NGN) | 8	4500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	L005A
LP2986AIM-3.0/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2986A IM3.0
LP2986AIM-3.0/NOPB.A	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2986A IM3.0
LP2986AIM-3.0/NOPB.B	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2986A IM3.0
LP2986AIM-3.3/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2986A IM3.3
LP2986AIM-3.3/NOPB.A	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2986A IM3.3
LP2986AIM-3.3/NOPB.B	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2986A IM3.3
LP2986AIM-5.0/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2986A IM5.0
LP2986AIM-5.0/NOPB.A	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2986A IM5.0
LP2986AIM-5.0/NOPB.B	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2986A IM5.0
LP2986AIMM-3.0/NO.A	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L39A
LP2986AIMM-3.0/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L39A
LP2986AIMM-3.3/NO.A	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L40A
LP2986AIMM-3.3/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L40A
LP2986AIMM-5.0/NO.A	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L41A
LP2986AIMM-5.0/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L41A
LP2986AIMMX-3.0/NO.A	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L39A
LP2986AIMMX-3.0/NOPB	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L39A
LP2986AIMMX-5.0/NO.A	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L41A

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP2986AIMMX-5.0/NOPB	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L41A
LP2986AIMX-3.3/NO.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2986A IM3.3
LP2986AIMX-3.3/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2986A IM3.3
LP2986AIMX-5.0/NO.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2986A IM5.0
LP2986AIMX-5.0/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2986A IM5.0
LP2986ILD-3.3/NOPB	Active	Production	WSON (NGN) | 8	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	L005A B
LP2986ILD-3.3/NOPB.A	Active	Production	WSON (NGN) | 8	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	L005A B
LP2986ILD-3.3/NOPB.B	Active	Production	WSON (NGN) | 8	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	L005A B
LP2986IM-3.0/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2986I M3.0
LP2986IM-3.0/NOPB.A	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2986I M3.0
LP2986IM-3.0/NOPB.B	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2986I M3.0
LP2986IM-3.3/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2986I M3.3
LP2986IM-3.3/NOPB.A	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2986I M3.3
LP2986IM-3.3/NOPB.B	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2986I M3.3
LP2986IM-5.0/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2986I M5.0
LP2986IM-5.0/NOPB.A	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2986I M5.0
LP2986IM-5.0/NOPB.B	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2986I M5.0
LP2986IMM-3.0/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L39B
LP2986IMM-3.0/NOPB.A	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L39B

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP2986IMM-3.0/NOPB.B	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L39B
LP2986IMM-3.3/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L40B
LP2986IMM-3.3/NOPB.A	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L40B
LP2986IMM-3.3/NOPB.B	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L40B
LP2986IMM-5.0/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L41B
LP2986IMM-5.0/NOPB.A	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L41B
LP2986IMM-5.0/NOPB.B	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L41B
LP2986IMMX-5.0/NO.A	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L41B
LP2986IMMX-5.0/NOPB	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L41B
LP2986IMX-3.3/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2986I M3.3
LP2986IMX-3.3/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2986I M3.3
LP2986IMX-3.3/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2986I M3.3
LP2986IMX-5.0	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	2986I M5.0
LP2986IMX-5.0/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2986I M5.0
LP2986IMX-5.0/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2986I M5.0
LP2986IMX-5.0/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2986I M5.0

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

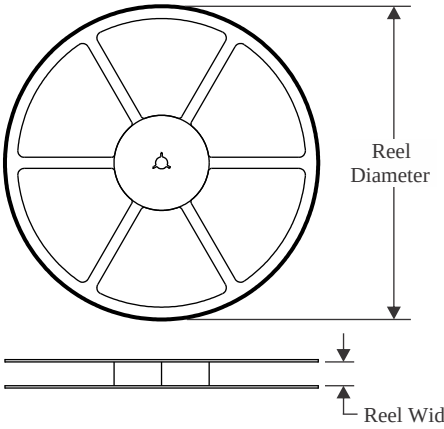
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

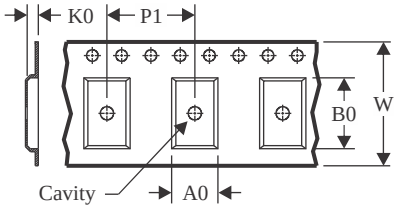
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

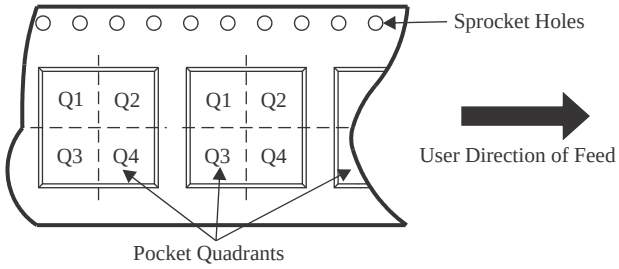


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

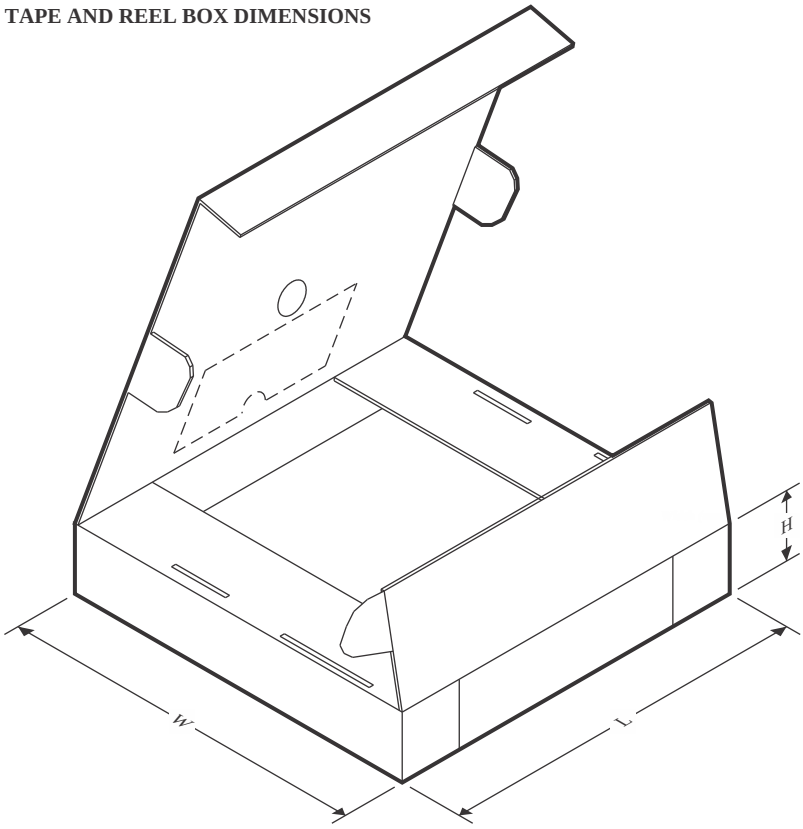
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2986AILD-3.3/NOPB	WSON	NGN	8	1000	177.8	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP2986AILDX-3.3/NOPB	WSON	NGN	8	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP2986AIMM-3.0/NOPB	VSSOP	DGK	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2986AIMM-3.3/NOPB	VSSOP	DGK	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2986AIMM-5.0/NOPB	VSSOP	DGK	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2986AIMMX-3.0/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2986AIMMX-5.0/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2986AIMX-3.3/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP2986AIMX-5.0/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP2986ILD-3.3/NOPB	WSON	NGN	8	1000	177.8	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP2986IMM-3.0/NOPB	VSSOP	DGK	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2986IMM-3.3/NOPB	VSSOP	DGK	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2986IMM-5.0/NOPB	VSSOP	DGK	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2986IMMX-5.0/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2986IMX-3.3/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP2986IMX-5.0/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

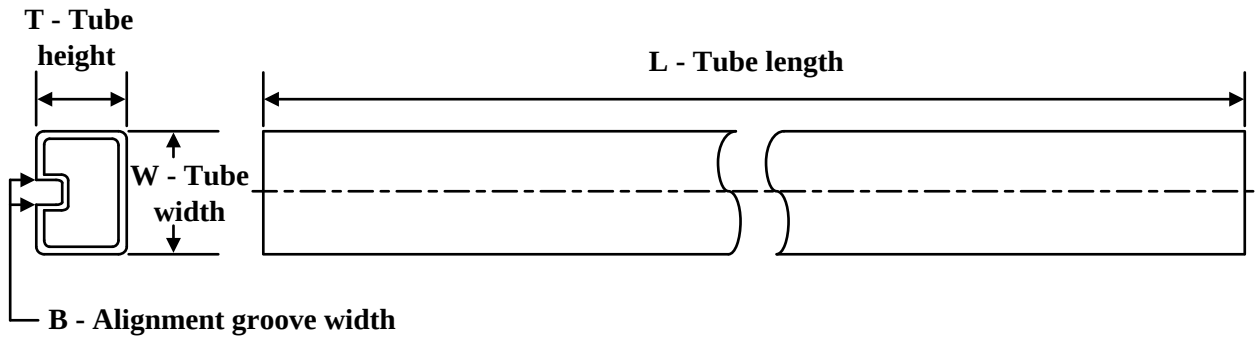
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2986AILD-3.3/NOPB	WSON	NGN	8	1000	208.0	191.0	35.0
LP2986AILDX-3.3/NOPB	WSON	NGN	8	4500	356.0	356.0	36.0
LP2986AIMM-3.0/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LP2986AIMM-3.3/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LP2986AIMM-5.0/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LP2986AIMMX-3.0/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LP2986AIMMX-5.0/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LP2986AIMX-3.3/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LP2986AIMX-5.0/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LP2986ILD-3.3/NOPB	WSON	NGN	8	1000	208.0	191.0	35.0
LP2986IMM-3.0/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LP2986IMM-3.3/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LP2986IMM-5.0/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LP2986IMMX-5.0/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LP2986IMX-3.3/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LP2986IMX-5.0/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

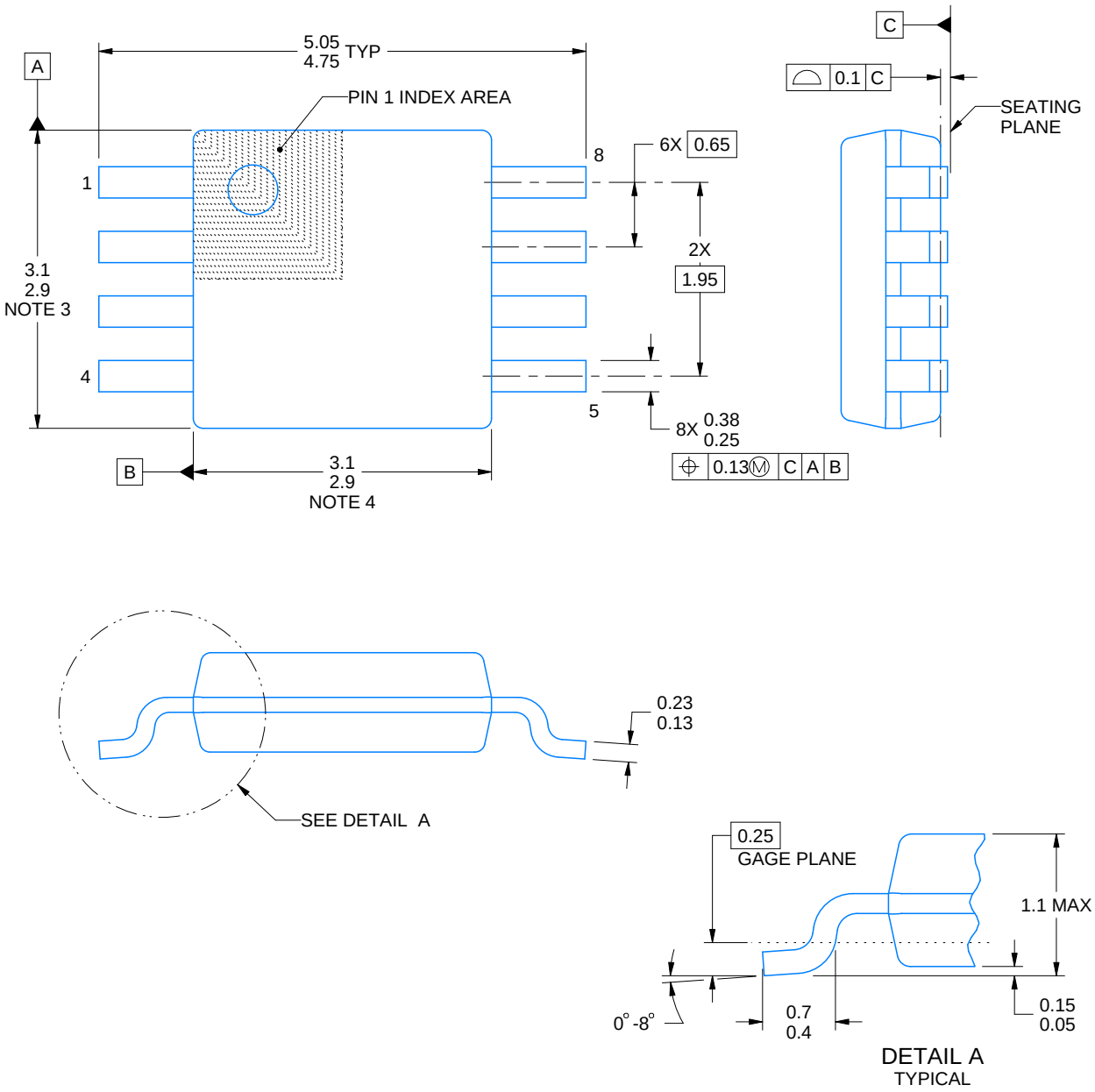
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LP2986AIM-3.0/NOPB	D	SOIC	8	95	495	8	4064	3.05
LP2986AIM-3.0/NOPB.A	D	SOIC	8	95	495	8	4064	3.05
LP2986AIM-3.0/NOPB.B	D	SOIC	8	95	495	8	4064	3.05
LP2986AIM-3.3/NOPB	D	SOIC	8	95	495	8	4064	3.05
LP2986AIM-3.3/NOPB.A	D	SOIC	8	95	495	8	4064	3.05
LP2986AIM-3.3/NOPB.B	D	SOIC	8	95	495	8	4064	3.05
LP2986AIM-5.0/NOPB	D	SOIC	8	95	495	8	4064	3.05
LP2986AIM-5.0/NOPB.A	D	SOIC	8	95	495	8	4064	3.05
LP2986AIM-5.0/NOPB.B	D	SOIC	8	95	495	8	4064	3.05
LP2986IM-3.0/NOPB	D	SOIC	8	95	495	8	4064	3.05
LP2986IM-3.0/NOPB.A	D	SOIC	8	95	495	8	4064	3.05
LP2986IM-3.0/NOPB.B	D	SOIC	8	95	495	8	4064	3.05
LP2986IM-3.3/NOPB	D	SOIC	8	95	495	8	4064	3.05
LP2986IM-3.3/NOPB.A	D	SOIC	8	95	495	8	4064	3.05
LP2986IM-3.3/NOPB.B	D	SOIC	8	95	495	8	4064	3.05
LP2986IM-5.0/NOPB	D	SOIC	8	95	495	8	4064	3.05
LP2986IM-5.0/NOPB.A	D	SOIC	8	95	495	8	4064	3.05
LP2986IM-5.0/NOPB.B	D	SOIC	8	95	495	8	4064	3.05

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

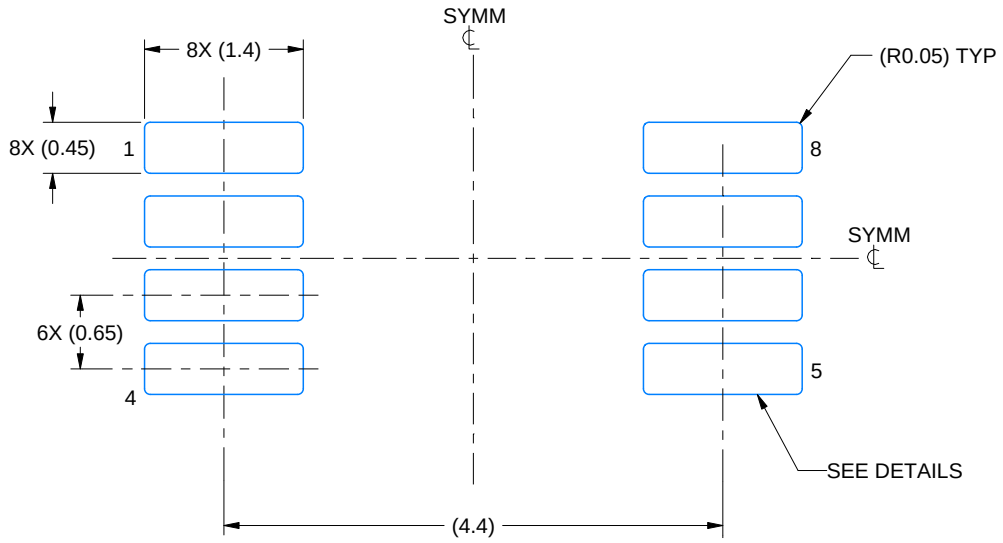
SMALL OUTLINE PACKAGE



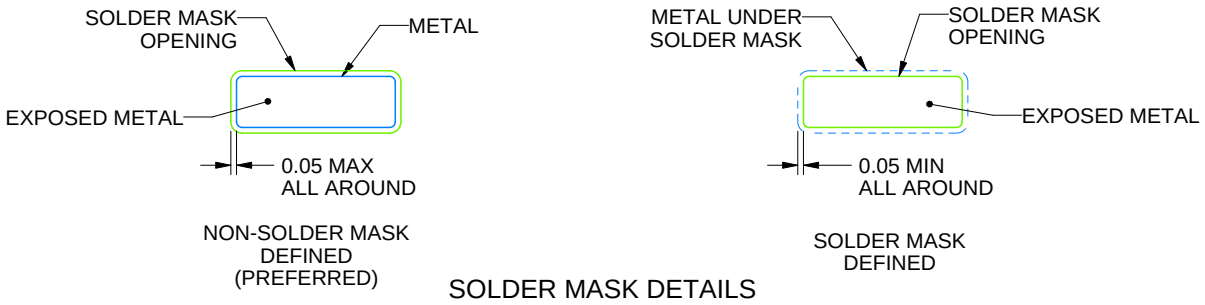
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

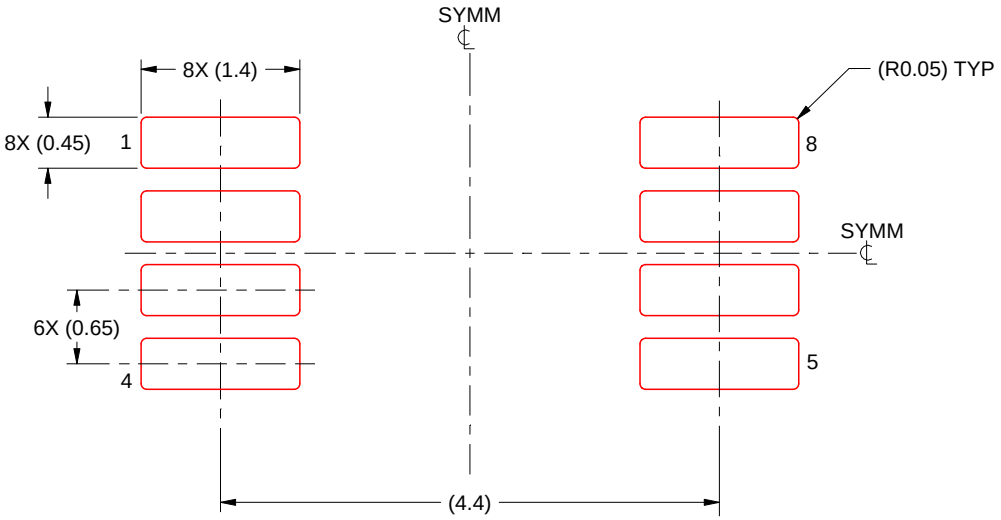


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

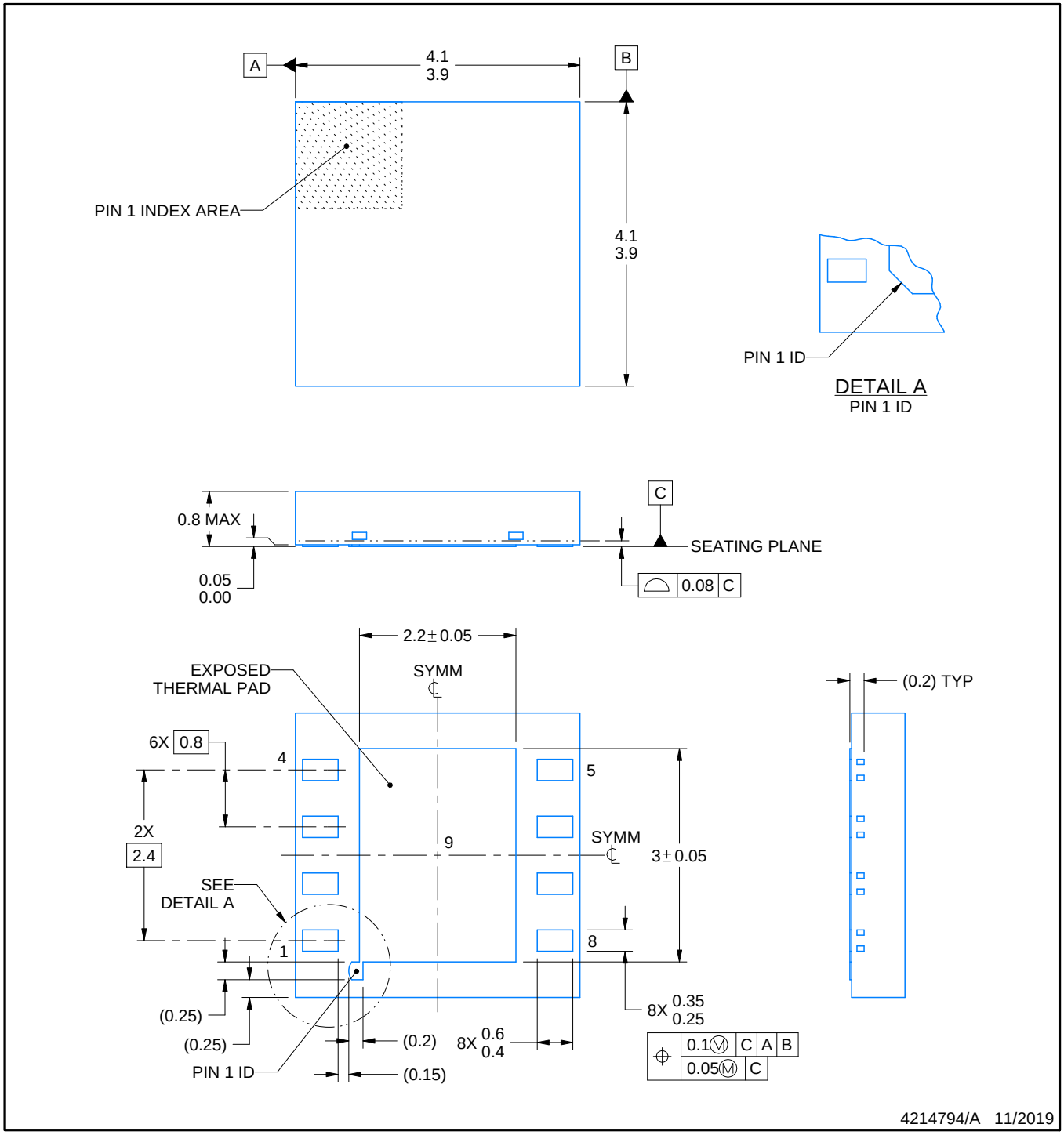
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

NGN0008A

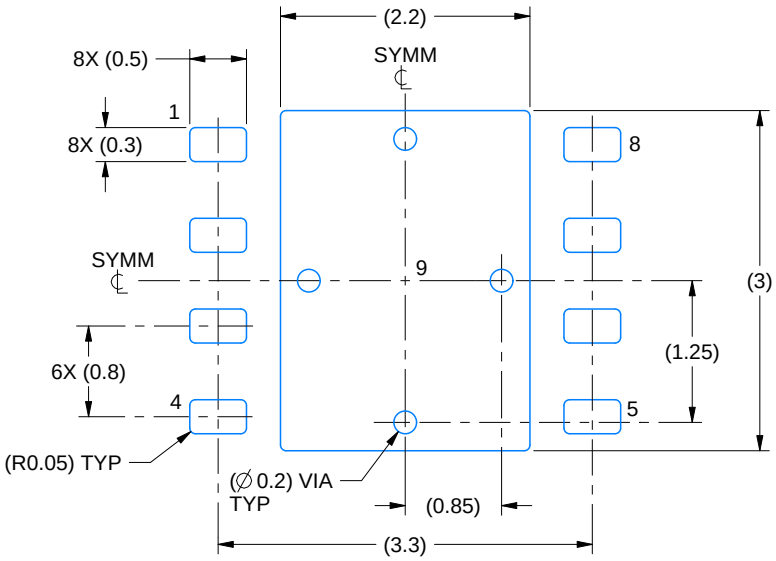
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

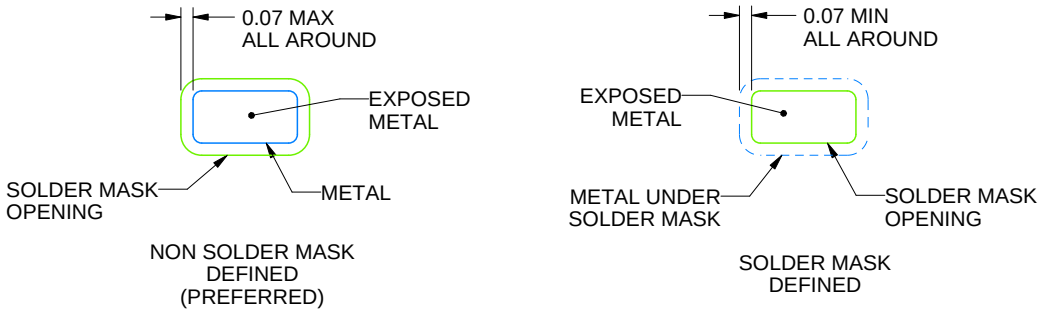


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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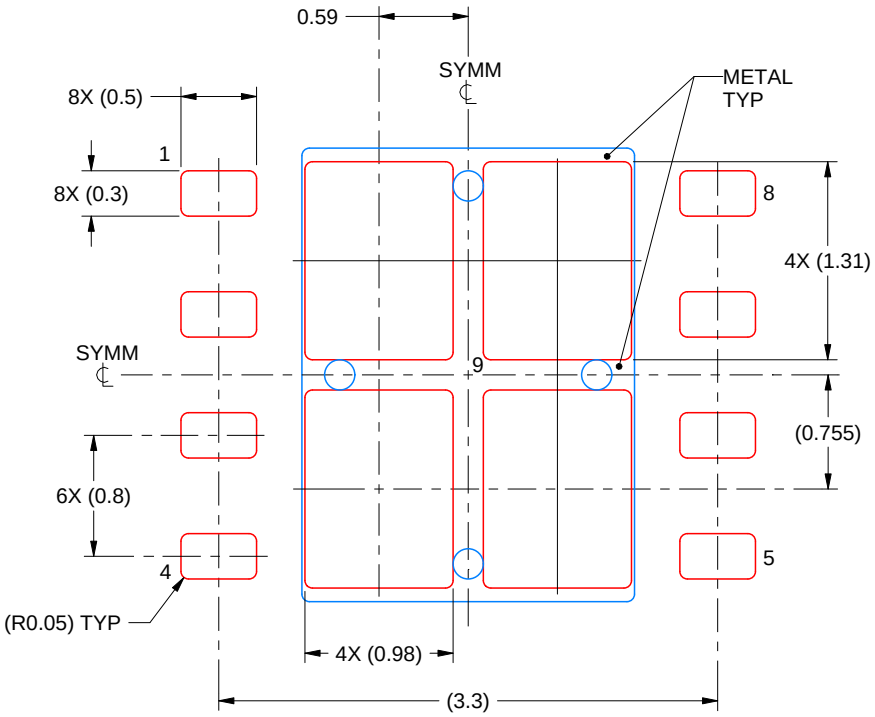
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



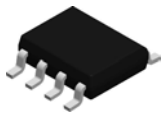
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4214794/A 11/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

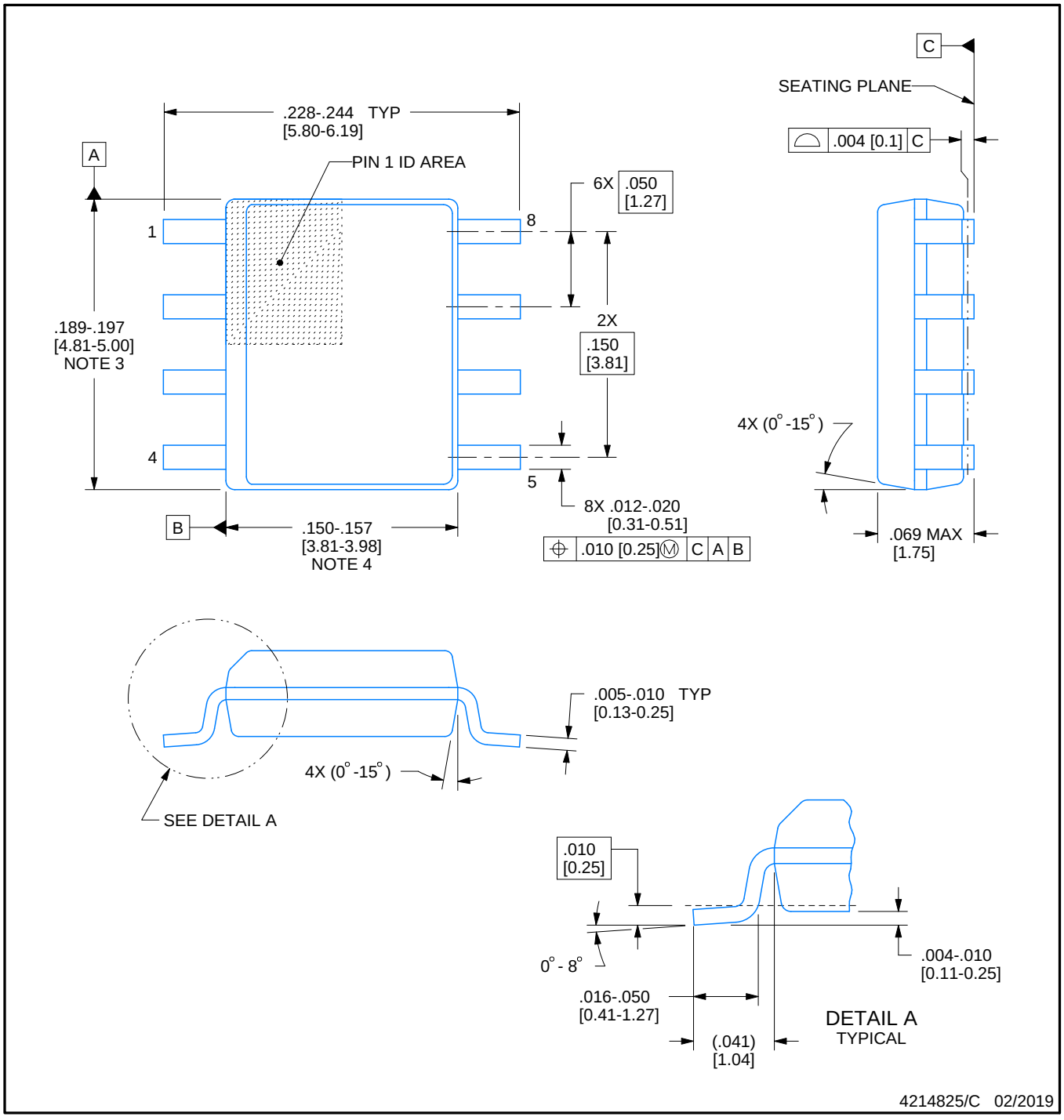


PACKAGE OUTLINE

D0008A

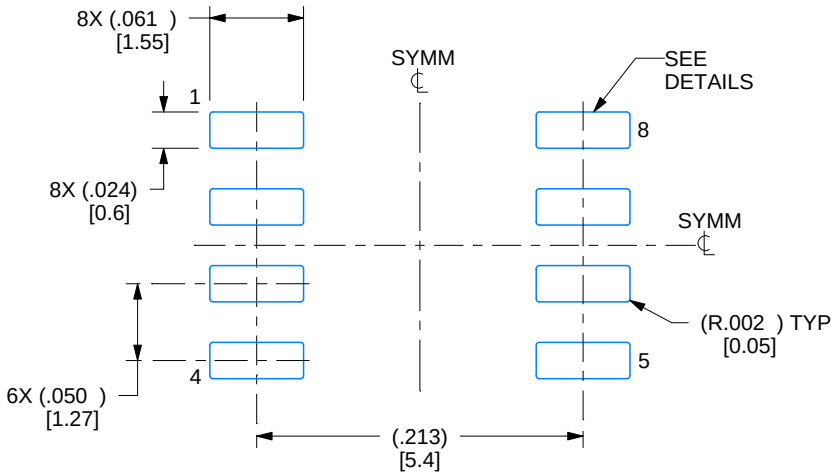
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

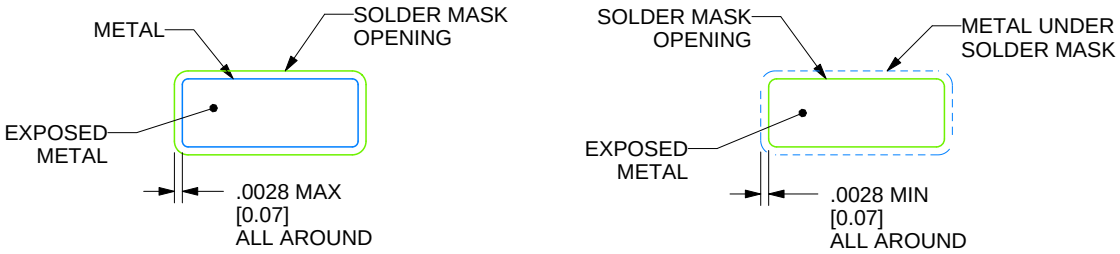


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

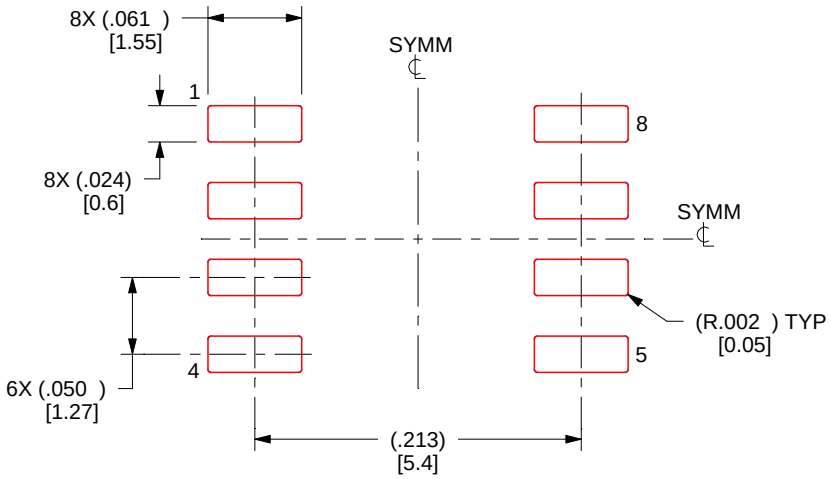
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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