LP2985 150mA, Low-Noise, Low-Dropout Regulator With Shutdown

1 Features

- V_{IN} range (new chip): 2.5V to 16V
- V_{OUT} range (new chip):
  - 1.2V to 5.0V (fixed, 100mV steps)
- V_{OUT} accuracy:
  - ±1% for A-grade (legacy chip)
  - ±1.5% for standard-grade (legacy chip)
  - ±0.5% (new chip)
- ±1% output accuracy over load and temperature (new chip)
- Output current: Up to 150mA
- Low I_Q (new chip): 71µA at I_{LOAD} = 0mA
- Low I_Q (new chip): 750µA at I_{LOAD} = 150mA
- Shutdown current:
  - 0.01µA (typ, legacy chip)
  - 1.12µA (typ, new chip)
- Low noise: 30µV_{RMS} with 10nF bypass capacitor
- Output current limiting and thermal protection
- Stable with 2.2µF ceramic capacitors (new chip)
- High PSRR: 70dB at 1kHz, 40dB at 1MHz (new chip)
- Operating junction temperature: –40°C to +125°C
- Package: 5-pin SOT-23 (DBV)

2 Applications

- Washer and dryer
- Land mobile radio
- Active antenna system mMIMO
- Cordless power tool
- Motor drives and control boards

3 Description

The LP2985 is a fixed-output, wide-input, low-noise, low-dropout voltage regulator supporting an input voltage range from 2.5V to 16V (for new chip) and up to 150mA of load current. The LP2985 supports an output range of 1.2V to 5.0V (for new chip).

Additionally, the LP2985 (new chip) has a ±1% output accuracy across load, and temperature that can meet the needs of low-voltage microcontrollers (MCUs) and processors.

Low output noise of 30µV_{RMS} (with 10nF bypass capacitors) and wide bandwidth PSRR performance of greater than 70dB at 1kHz and 40dB at 1MHz help attenuate the switching frequency of an upstream DC/DC converter and minimize post regulator filtering.

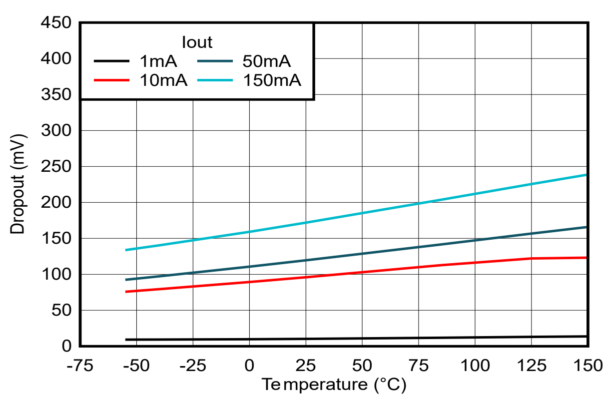
The new chip provides internal soft-start mechanism to reduce inrush current during start up, thus minimizing input capacitance. Standard protection features, such as overcurrent and overtemperature protection, are also included.

The LP2985 is available in a 5-pin 2.9mm × 2.8mm SOT-23 (DBV) package.

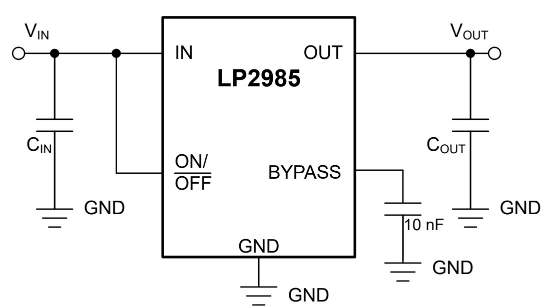
Package Information

PART NUMBER	PACKAGE(1)	PACKAGING SIZE(2)
LP2985	DBV (SOT-23, 5)	2.9mm × 2.8mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Dropout Voltage vs Temperature (New Chip)



Typical Application Circuit

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4 Pin Configuration and Functions

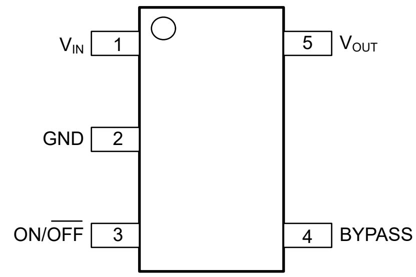


Figure 4-1. DBV Package, 5-Pin SOT-23 (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
BYPASS	4	I/O	BYPASS pin to achieve low noise performance. Connecting an external capacitor between BYPASS pin and ground reduces reference voltage noise. See the *Recommended Operating Conditions* section for more information.
GND	2	—	Ground
ON/$\overline{OFF}$	3	I	Enable pin for the LDO. Driving the ON/$\overline{OFF}$ pin high enables the device. Driving this pin low disables the device. High and low thresholds are listed in the *Electrical Characteristics* table. Tie this pin to V_{IN} if unused.
V_{IN}	1	I	Input supply pin. Use a capacitor with a value of 1 µF or larger from this pin to ground. See the *Input and Output Capacitor Requirements* section for more information.
V_{OUT}	5	O	Output of the regulator. Use a capacitor with a value of 2.2 µF or larger from this pin to ground.(1) See the *Input and Output Capacitor Requirements* section for more information.

(1) The nominal output capacitance must be greater than 1 µF. Throughout this document, the nominal derating on these capacitors is 50%. Make sure that the effective capacitance at the pin is greater than 1 µF.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)] [(2)]

		MIN	MAX	UNIT
V_{IN}	Continuous input voltage range (for legacy chip)	–0.3	16	V
	Continuous input voltage range (for new chip)	–0.3	18	
V_{OUT}	Output voltage range (for legacy chip)	–0.3	9	
	Output voltage range (for new chip)	–0.3	V_{IN} + 0.3 or 9 (whichever is smaller)	
V_{BYPASS}	BYPASS pin voltage range (for new chip)	–0.3	3	
$V_{ON/\overline{OFF}}$	ON/$\overline{\text{OFF}}$ pin voltage range (for legacy chip)	–0.3	16	
	ON/$\overline{\text{OFF}}$ pin voltage range (for new chip)	–0.3	18	
Current	Maximum output	Internally limited		A
Temperature	Operating junction, T_J	–55	150	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages with respect to GND.

5.2 ESD Ratings

			VALUE (Legacy Chip)	VALUE (New Chip)	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	±3000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[(2)]	±500	±1000	

(1) JEDEC document JEP155 states that 2-kV HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 500-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Supply input voltage (for legacy chip)	2.2		16	V
	Supply input voltage (for new chip)	2.5		16	
V_{OUT}	Output voltage (for legacy chip)	1.2		10.0	V
	Output voltage (for new chip)	1.2		5.0	
V_{BYPASS}	Bypass voltage		1.2		V
$V_{ON/\overline{OFF}}$	Enable voltage (for legacy chip)	0		V_{IN}	V
	Enable voltage (for new chip)	0		16	
I_{OUT}	Output current	0		150	mA
C_{IN} [(1)]	Input capacitor		1		µF
C_{OUT}	Output capacitance (for legacy chip)	2.2	4.7		µF
	Output capacitance (for new chip) [(1)]	1	2.2	200	
C_{OUT} ESR[(3)]	Output capacitor ESR (for new chip)[(2)]	0		1	Ω
T_J	Operating junction temperature	–40		125	°C

(1) All capacitor values are assumed to derate to 50% of the nominal capacitor value. Maintain an effective output capacitance of 1 µF minimum for stability.
(2) Details related to supported ESR range for the legacy chip are available in *Recommended Capacitors for the Legacy Chip*
(3) Maximum supported ESR range for new chip is 1Ω. For output capacitor with higher ESR values, place a low ESR MLCC capacitor with value of 100nF, close to the output pin of the LDO.

5.4 Thermal Information

THERMAL METRIC (2) (1)		Legacy Chip DBV (SOT23-5) 5 PINS	New Chip DBV (SOT23-5) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	205.4	178.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78.8	77.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.7	47.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.3	15.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	46.3	46.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.
(2) Thermal performance results are based on the JEDEC standard of 2s2p PCB configuration. These thermal metric parameters can be further improved by 35-55% based on thermally optimized PCB layout designs. See the analysis of the Impact of board layout on LDO thermal performance application note.

5.5 Electrical Characteristics

specified at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 1.0 V or V_{IN} = 2.5 V (whichever is greater), I_{OUT} = 1 mA, $V_{ON/OFF}$ = 2 V, C_{IN} = 1.0 µF, and C_{OUT} = 2.2 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ΔV_{OUT}	Output voltage tolerance	I_L = 1 mA	Legacy chip (standard grade)	–1.5		1.5	%
			Legacy chip (A grade)	–1.0		1.0	
			New chip	–0.5		0.5	
		1 mA ≤ I_L ≤ 50 mA	Legacy chip (standard grade)	–2.5		2.5	
			Legacy chip (A grade)	–1.5		1.5	
			New chip	–0.5		0.5	
		1 mA ≤ I_L ≤ 150 mA	Legacy chip (standard grade)	–3.0		3.0	
			Legacy chip (A grade)	–2.5		2.5	
			New chip	–0.5		0.5	
		1 mA ≤ I_L ≤ 50 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip (standard grade)	–3.5		3.5	
			Legacy chip (A grade)	–2.5		2.5	
			New chip	–1		1	
		1 mA ≤ I_L ≤ 150 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip (standard grade)	–4.0		4.0	
			Legacy chip (A grade)	–3.5		3.5	
			New chip	–1		1	
$\Delta V_{OUT(\Delta VIN)}$	Line regulation	$V_{O(NOM)}$ + 1 V ≤ V_{IN} ≤ 16 V	Legacy chip		0.007	0.014	%/V
			New chip		0.002	0.014	
		$V_{O(NOM)}$ + 1 V ≤ V_{IN} ≤ 16 V, –40°C ≤ T_J ≤ 125°C	Legacy chip		0.007	0.032	
			New chip		0.002	0.032	

5.5 Electrical Characteristics (continued)

specified at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 1.0 V or V_{IN} = 2.5 V (whichever is greater), I_{OUT} = 1 mA, $V_{ON/OFF}$ = 2 V, C_{IN} = 1.0 µF, and C_{OUT} = 2.2 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN} - V_{OUT}	Dropout voltage[(1)]	I_{OUT} = 0 mA	Legacy chip		1	3	mV
			New chip		1	2.75	
		I_{OUT} = 0 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			5	
			New chip			3	
		I_{OUT} = 1 mA	Legacy chip		7	10	
			New chip		11.5	14	
		I_{OUT} = 1 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			15	
			New chip			17	
		I_{OUT} = 10 mA	Legacy chip		40	60	
			New chip		98	115	
		I_{OUT} = 10 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			90	
			New chip			148	
		I_{OUT} = 50 mA	Legacy chip		120	150	
			New chip		120	145	
		I_{OUT} = 50 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			225	
			New chip			184	
		I_{OUT} = 150 mA	Legacy chip		280	350	
			New chip		180	198	
		I_{OUT} = 150 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			575	
			New chip			254	
I_{GND}	GND pin current	I_{OUT} = 0 mA	Legacy chip		65	95	µA
			New chip		69	95	
		I_{OUT} = 0 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			125	
			New chip			123	
		I_{OUT} = 1 mA	Legacy chip		75	110	
			New chip		78	110	
		I_{OUT} = 1 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			170	
			New chip			140	
I_{GND}	GND pin current	I_{OUT} = 10 mA	Legacy chip		120	220	µA
			New chip		175	210	
		I_{OUT} = 10 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			400	
			New chip			250	
I_{GND}	GND pin current	I_{OUT} = 50 mA	Legacy chip		350	600	µA
			New chip		380	440	
I_{GND}	GND pin current	I_{OUT} = 50 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			900	µA
I_{GND}	GND pin current	I_{OUT} = 50 mA, –40°C ≤ T_J ≤ 125°C	New chip			650	µA
I_{GND}	GND pin current	I_{OUT} = 150 mA	Legacy chip		850	1200	µA
I_{GND}	GND pin current	I_{OUT} = 150 mA	New chip		765	890	µA
I_{GND}	GND pin current	I_{OUT} = 150 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			2000	µA
I_{GND}	GND pin current	I_{OUT} = 150 mA, –40°C ≤ T_J ≤ 125°C	New chip			1060	µA
I_{GND}	GND pin current	$V_{ON/OFF}$ < 0.3 V, V_{IN} = 16 V	Legacy chip		0.01	0.08	µA
I_{GND}	GND pin current	$V_{ON/OFF}$ < 0.3 V, V_{IN} = 16 V	New chip		1.25	1.75	µA
I_{GND}	GND pin current	$V_{ON/OFF}$ < 0.15 V, V_{IN} = 16 V, –40°C ≤ T_J ≤ 85°C	Legacy chip		0	1	µA

5.5 Electrical Characteristics (continued)

specified at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 1.0 V or V_{IN} = 2.5 V (whichever is greater), I_{OUT} = 1 mA, $V_{ON/OFF}$ = 2 V, C_{IN} = 1.0 μF, and C_{OUT} = 2.2 μF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{GND}	GND pin current	$V_{ON/OFF}$ < 0.15 V, V_{IN} = 16 V, –40°C ≤ T_J ≤ 85°C	New chip		1.12	2.25	μA
I_{GND}	GND pin current	$V_{ON/OFF}$ < 0.15 V, V_{IN} = 16 V, –40°C ≤ T_J ≤ 125°C	Legacy chip		0.01	2	μA
I_{GND}	GND pin current	$V_{ON/OFF}$ < 0.15 V, V_{IN} = 16 V, –40°C ≤ T_J ≤ 125°C	New chip		1.12	2.75	μA
V_{UVLO+}	Rising bias supply UVLO	V_{IN} rising, –40°C ≤ T_J ≤ 125°C	New chip		2.2	2.4	V
V_{UVLO-}	Falling bias supply UVLO	V_{IN} falling, –40°C ≤ T_J ≤ 125°C		1.9			V
$V_{UVLO(HYST)}$	UVLO hysteresis	–40°C ≤ T_J ≤ 125°C			0.130		V
$V_{ON/\overline{OFF}}$	ON/$\overline{\text{OFF}}$ input voltage	Low = Output OFF	Legacy chip		0.55		V
			New chip		0.72		
		Low = Output OFF, V_{OUT} + 1 ≤ V_{IN} ≤ 16 V, –40°C ≤ T_J ≤ 125°C	Legacy chip			0.15	
			New chip			0.15	
		High = Output ON	Legacy chip		1.4		
			New chip		0.85		
		High = Output ON, V_{OUT} + 1 ≤ V_{IN} ≤ 16 V, –40°C ≤ T_J ≤ 125°C	Legacy chip	1.6			
			New chip	1.6			
$I_{ON/\overline{OFF}}$	ON/OFF input current	$V_{ON/OFF}$ = 0 V	Legacy chip		0.01		μA
			New chip		0.42		
$I_{ON/\overline{OFF}}$	ON/OFF input current	$V_{ON/OFF}$ = 0 V, V_{OUT} + 1 ≤ V_{IN} ≤ 16 V, –40°C ≤ T_J ≤ 125°C	Legacy chip			-1	μA
			New chip			-0.9	μA
		$V_{ON/OFF}$ = 5 V	Legacy chip		5		μA
			New chip		0.011		μA
		$V_{ON/OFF}$ = 5 V, V_{OUT} + 1 ≤ V_{IN} ≤ 16 V, –40°C ≤ T_J ≤ 125°C	Legacy chip			15	μA
			New chip			2.20	μA
IO(PK)	Peak output current	V_{OUT} ≥ $V_{O(NOM)}$ –5% (steady state)	Legacy chip	300	350		mA
			New chip	300	350		
$I_{O(SC)}$	Short output current	R_L = 0 Ω (steady state)	Legacy chip		400		
			New chip		375		
$ΔV_O/ΔV_{IN}$	Ripple rejection	f = 1 kHz, C_{BYPASS} = 10 nF, C_{OUT} = 10 μF	Legacy chip		45		dB
			New chip		78		
V_n	Output noise voltage	Bandwidth = 300 Hz to 50 kHz, C_{BYPASS} = 10 nF, C_{OUT} = 2.2 μF, V_{OUT} = 3.3 V, I_{LOAD} = 150 mA	Legacy chip		30		μVRMS
		Bandwidth = 300 Hz to 50 kHz, C_{BYPASS} = 10 nF, C_{OUT} = 2.2 μF, V_{OUT} = 3.3 V, I_{LOAD} = 150 mA	New chip		30		
T_{sd+}	Thermal shutdown threshold	Shutdown, temperature increasing	New chip		170		°C
T_{sd-}		Reset, temperature decreasing			150		

(1) Dropout voltage (V_{DO}) is defined as the input-to-output differential at which the output voltage drops 100 mV below the value measured with a 1 V differential. V_{DO} is measured with V_{IN} = $V_{OUT(nom)}$ – 100 mV for fixed output devices.

5.6 Typical Characteristics

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, ON/$\overline{OFF}$ pin tied to V_{IN}, C_{IN} = 1.0 µF, and C_{OUT} = 4.7 µF (unless otherwise noted)

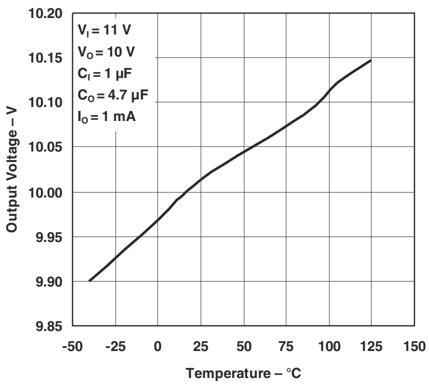


Figure 5-1. Output Voltage vs Temperature for Legacy Chip

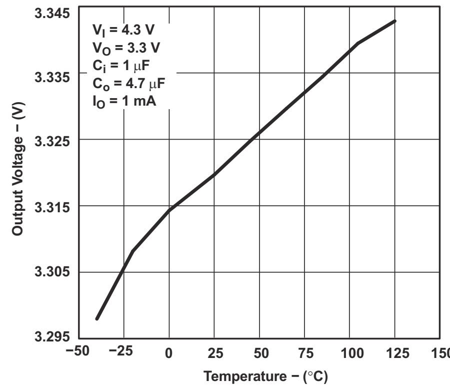
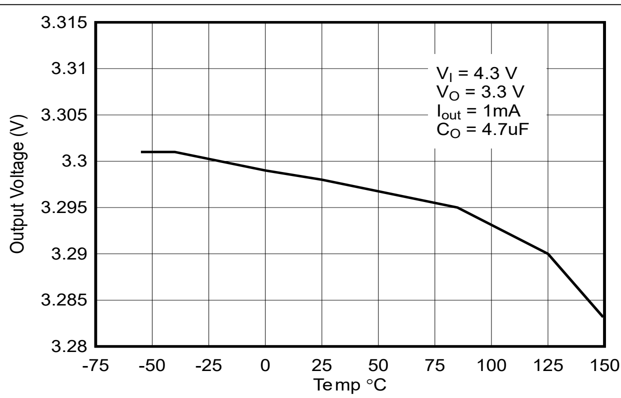


Figure 5-2. Output Voltage vs Temperature for Legacy Chip



V_{IN} = 4.3 V, V_{OUT} = 3.3 V (for new chip)

Figure 5-3. Output Voltage vs Temperature for New Chip

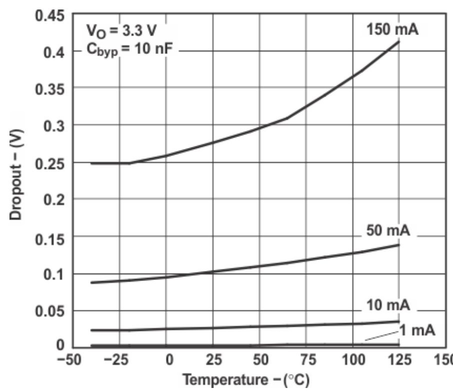


Figure 5-4. Dropout Voltage vs Temperature for Legacy Chip

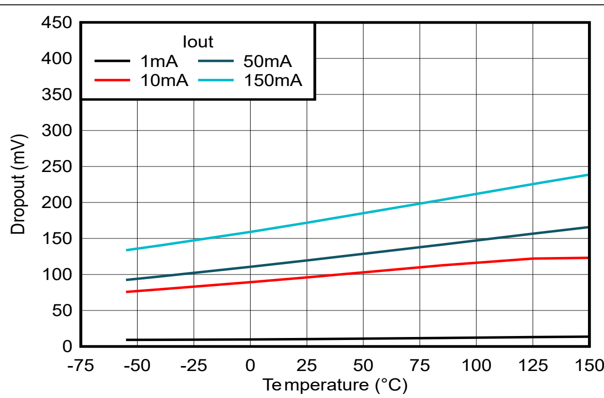


Figure 5-5. Dropout Voltage vs Temperature for New Chip

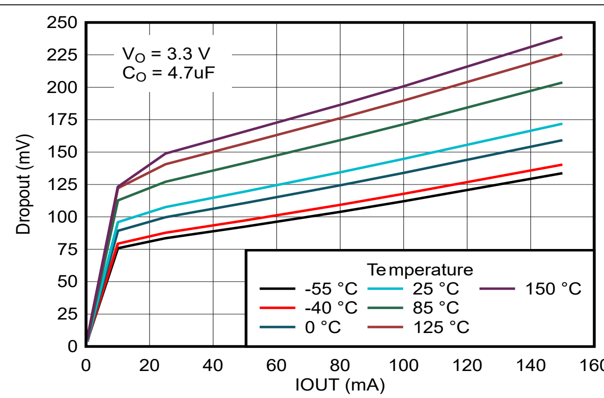


Figure 5-6. Dropout Voltage vs Load Current for New Chip

5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, ON/$\overline{\text{OFF}}$ pin tied to V_{IN}, C_{IN} = 1.0 µF, and C_{OUT} = 4.7 µF (unless otherwise noted)

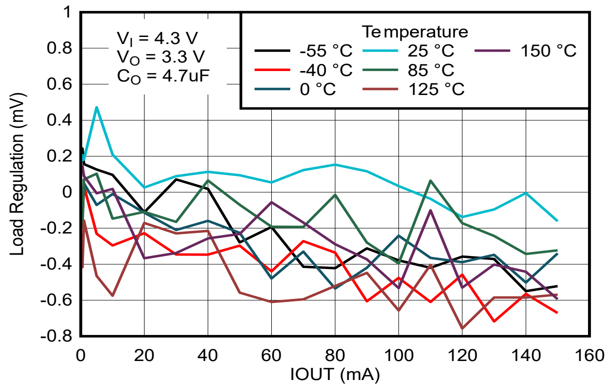


Figure 5-7. Output Regulation vs Load Current for New Chip

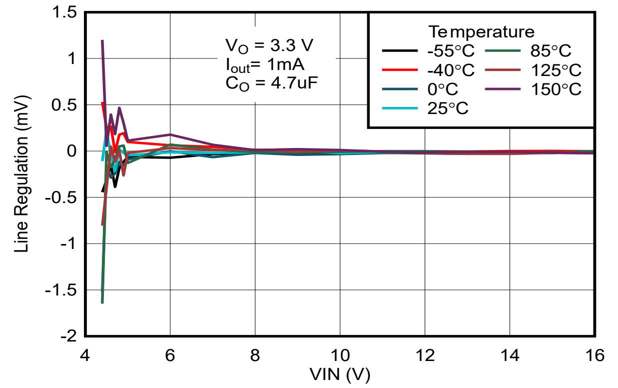


Figure 5-8. Output Regulation vs Input Voltage for New Chip

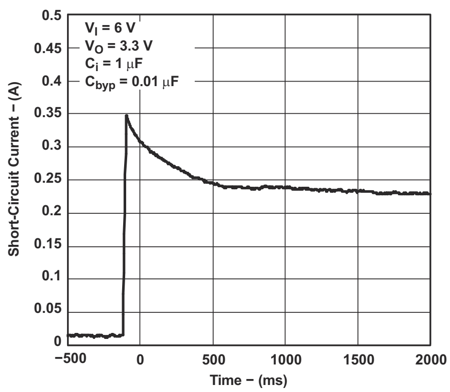
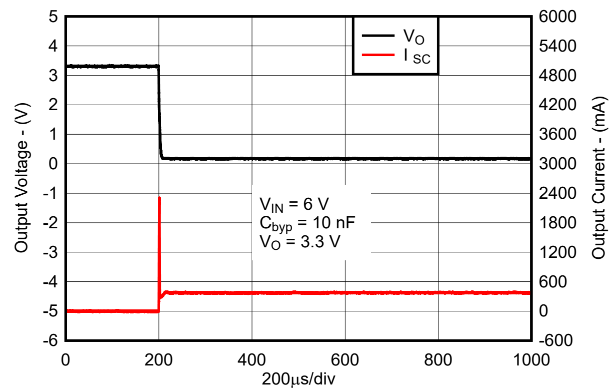


Figure 5-9. Short-Circuit Current vs Time for Legacy Chip



V_{IN} = 6 V

Figure 5-10. Short-Circuit Current vs Time for New Chip

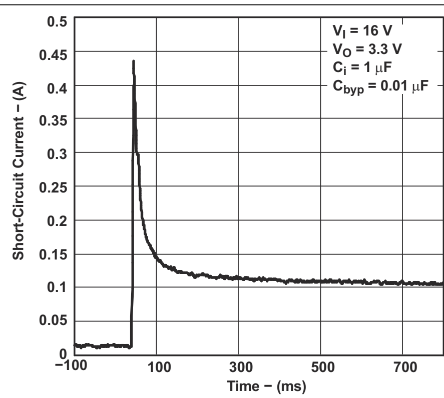


Figure 5-11. Short-Circuit Current vs Time for Legacy Chip

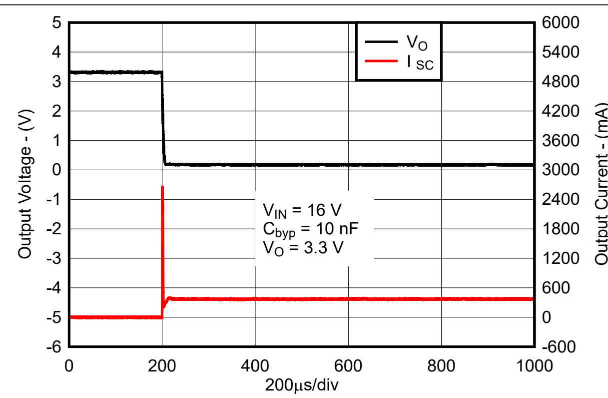


Figure 5-12. Short-Circuit Current vs Time for New Chip

5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, ON/$\overline{\text{OFF}}$ pin tied to V_{IN}, C_{IN} = 1.0 µF, and C_{OUT} = 4.7 µF (unless otherwise noted)

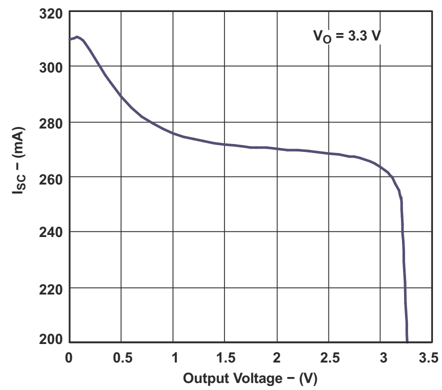


Figure 5-13. Short-Circuit Current vs Output Voltage for Legacy Chip

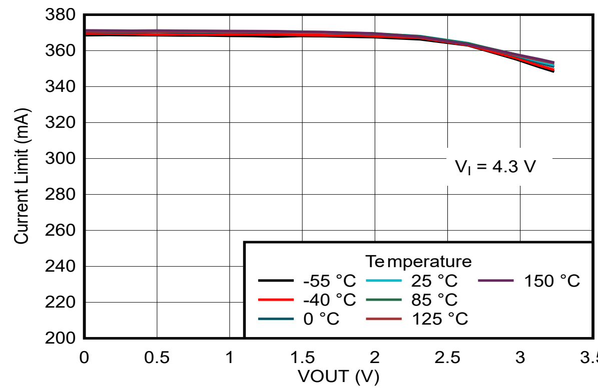


Figure 5-14. Short-Circuit Current vs Output Voltage for New Chip

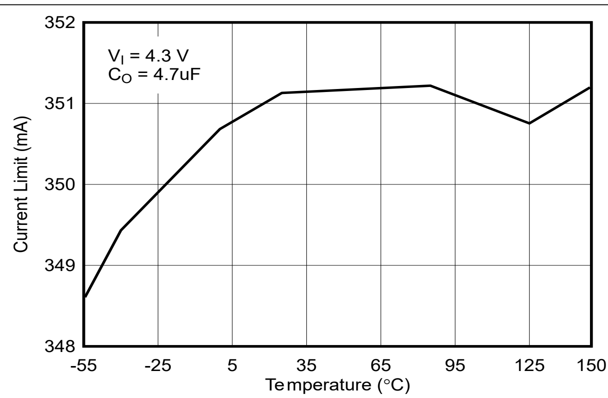


Figure 5-15. Short-Circuit Current vs Temperature for New Chip

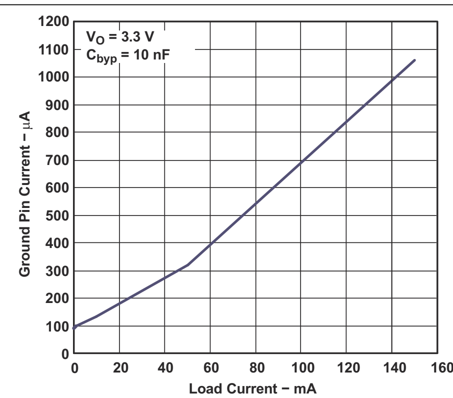


Figure 5-16. Ground Pin Current vs Load Current for Legacy Chip

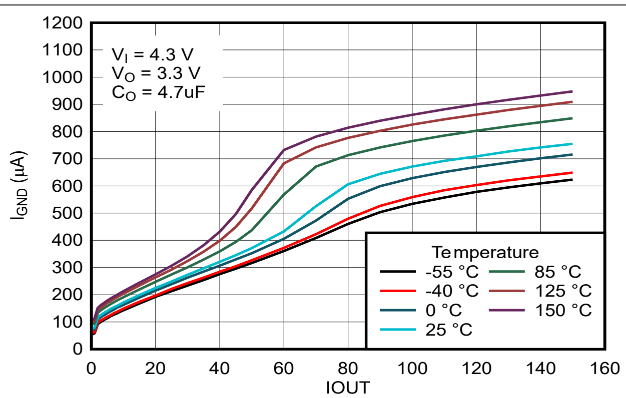


Figure 5-17. Ground Pin Current vs Load Current for New Chip

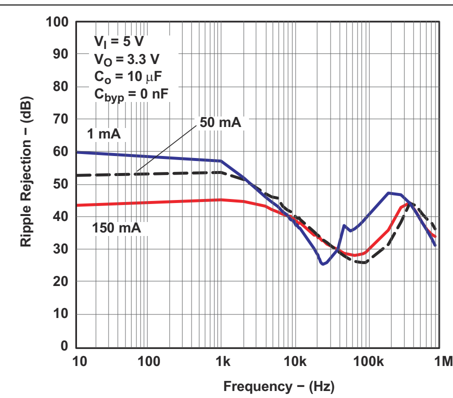
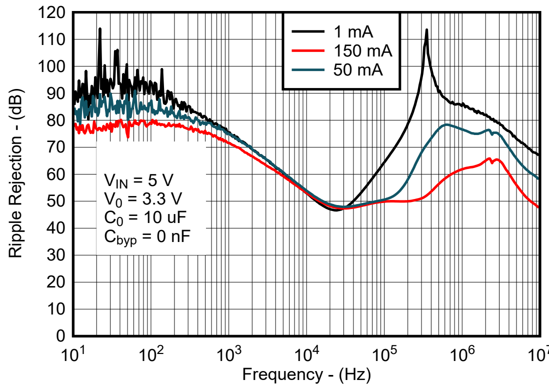


Figure 5-18. Ripple Rejection vs Frequency for Legacy Chip

5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, ON/$\overline{\text{OFF}}$ pin tied to V_{IN}, C_{IN} = 1.0 µF, and C_{OUT} = 4.7 µF (unless otherwise noted)



V_{IN} = 5 V, V_{OUT} = 3.3 V, C_{OUT} = 10 µF, C_{BYP} = 0 nF

Figure 5-19. Ripple Rejection vs Frequency for New Chip

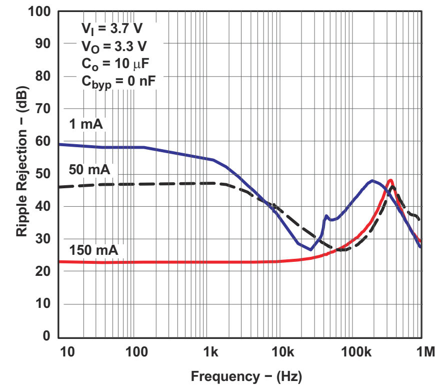
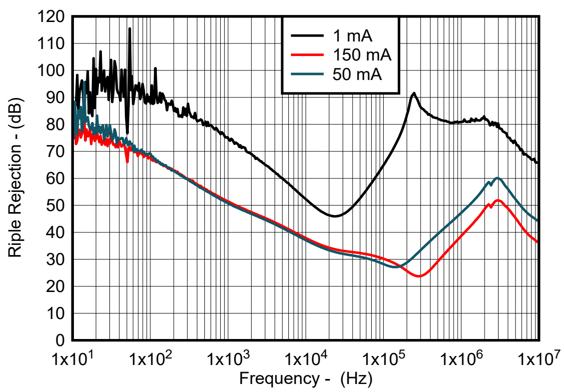


Figure 5-20. Ripple Rejection vs Frequency for Legacy Chip



V_{IN} = 3.7 V, V_{OUT} = 3.3 V, C_{OUT} = 10 µF, C_{BYP} = 0 nF

Figure 5-21. Ripple Rejection vs Frequency for New Chip

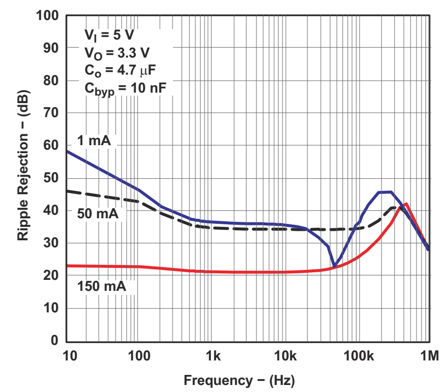


Figure 5-22. Ripple Rejection vs Frequency for Legacy Chip

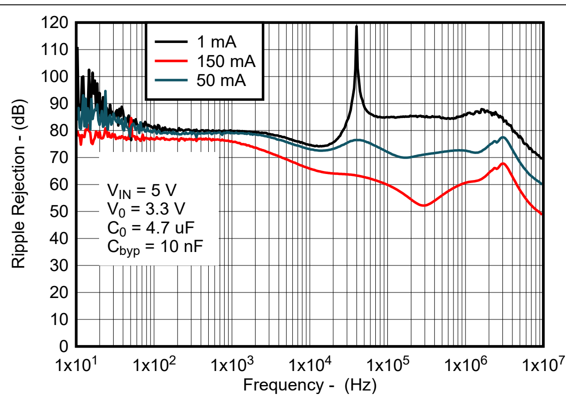


Figure 5-23. Ripple Rejection vs Frequency for New Chip

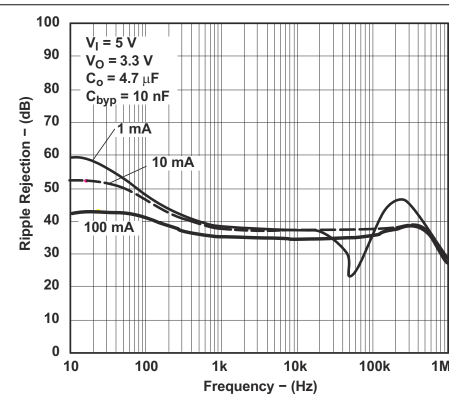


Figure 5-24. Ripple Rejection vs Frequency for Legacy Chip

5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, ON/$\overline{OFF}$ pin tied to V_{IN}, C_{IN} = 1.0 µF, and C_{OUT} = 4.7 µF (unless otherwise noted)

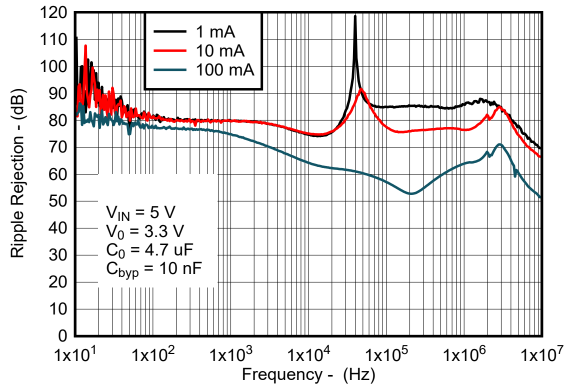


Figure 5-25. Ripple Rejection vs Frequency for New Chip

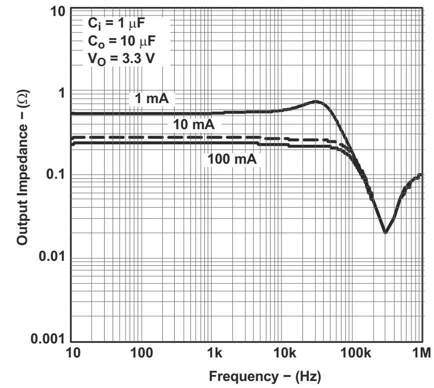


Figure 5-26. Output Impedance vs Frequency for Legacy Chip

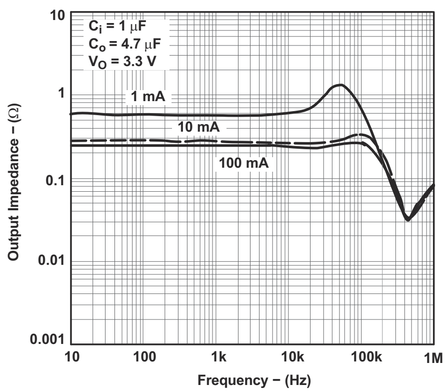


Figure 5-27. Output Impedance vs Frequency for Legacy Chip

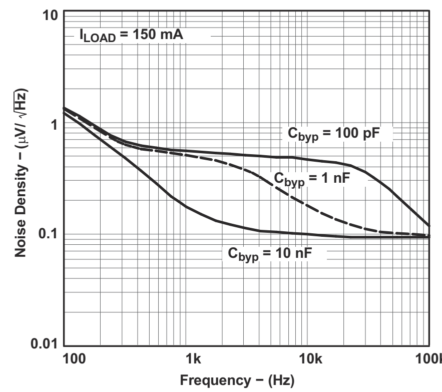


Figure 5-28. Output Noise Density vs Frequency for Legacy Chip

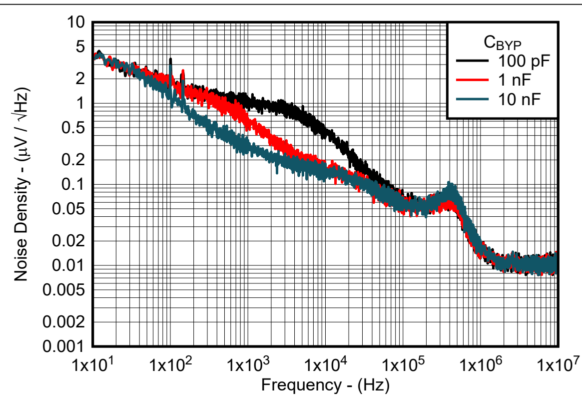


Figure 5-29. Output Noise Density vs Frequency for New Chip

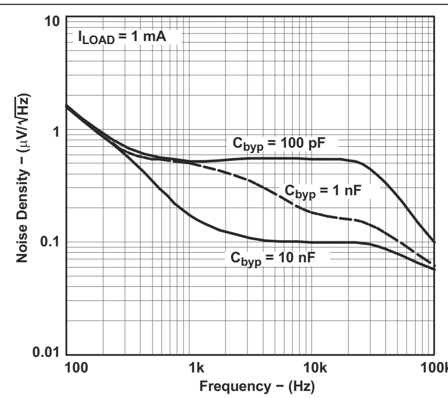


Figure 5-30. Output Noise Density vs Frequency for Legacy Chip

5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, ON/$\overline{\text{OFF}}$ pin tied to V_{IN}, C_{IN} = 1.0 μF, and C_{OUT} = 4.7 μF (unless otherwise noted)

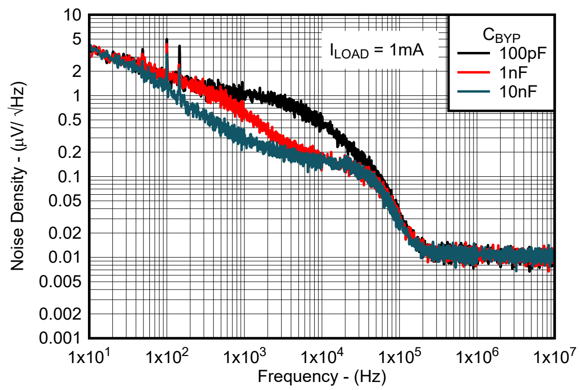


Figure 5-31. Output Noise Density vs Frequency for New Chip

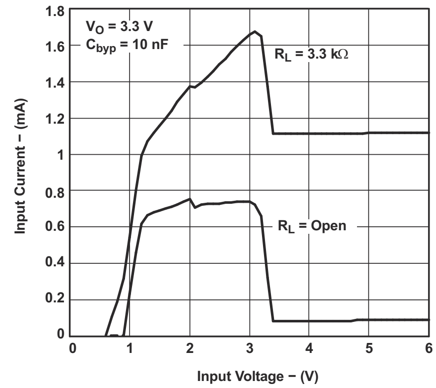


Figure 5-32. Input Current vs Input Voltage for Legacy Chip

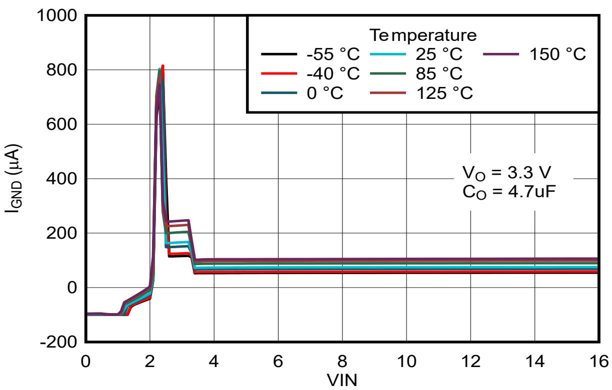


Figure 5-33. Input Current vs Input Voltage for New Chip

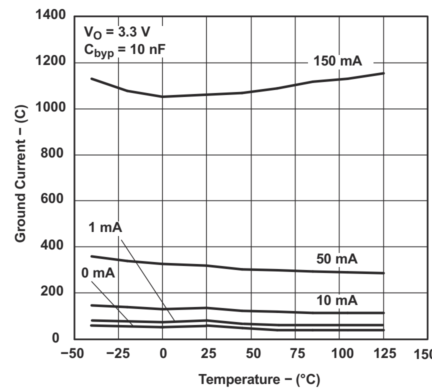


Figure 5-34. Ground-Pin Current vs Temperature for Legacy Chip

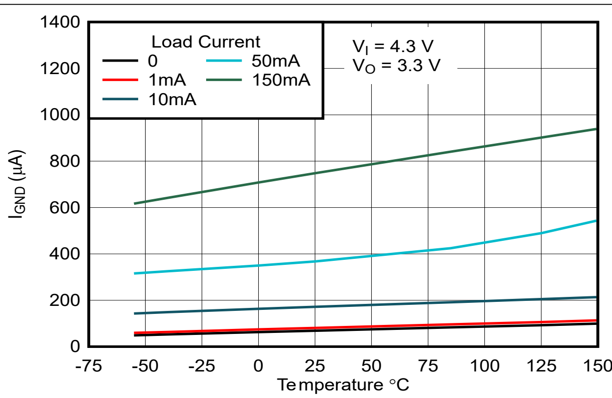


Figure 5-35. Ground-Pin Current vs Temperature for New Chip

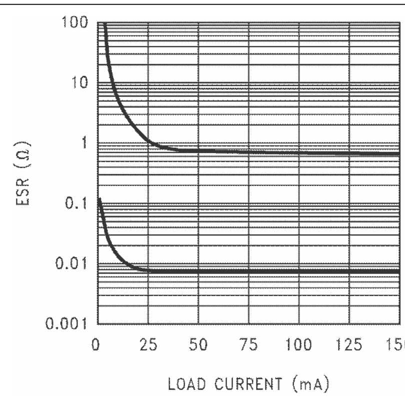


Figure 5-36. 2.2-μF Stable ESR Range for Output Voltage ≤ 2.3 V for Legacy Chip

5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, ON/$\overline{OFF}$ pin tied to V_{IN}, C_{IN} = 1.0 µF, and C_{OUT} = 4.7 µF (unless otherwise noted)

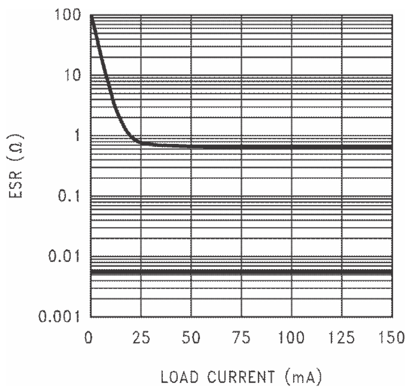


Figure 5-37. 4.7-µF Stable ESR Range for Output Voltage ≤ 2.3 V for Legacy Chip

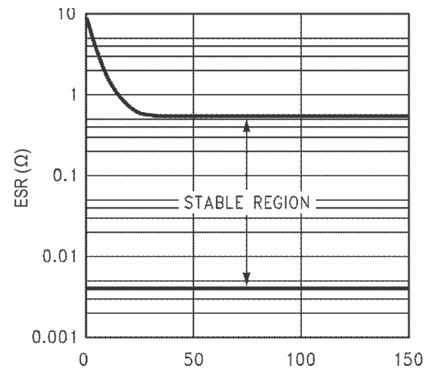


Figure 5-38. 2.2-µF, 3.3-µF Stable ESR Range for Output Voltage ≥ 2.5 V for Legacy Chip

6 Detailed Description

6.1 Overview

The LP2985 is a fixed-output, low-noise, high PSRR, low-dropout regulator that offers exceptional, cost-effective performance for both portable and nonportable applications. The LP2985 has an output tolerance of ±1% across load, and temperature variation (for the new chip) and is capable of delivering 150mA of continuous load current.

This device features integrated overcurrent protection, thermal shutdown, and output enable. The new chip version also features internal output pulldown and has a built-in soft-start mechanism for controlled inrush current. This device delivers excellent line and load transient performance. The operating ambient temperature range of the device is –40°C to +125°C.

6.2 Functional Block Diagrams

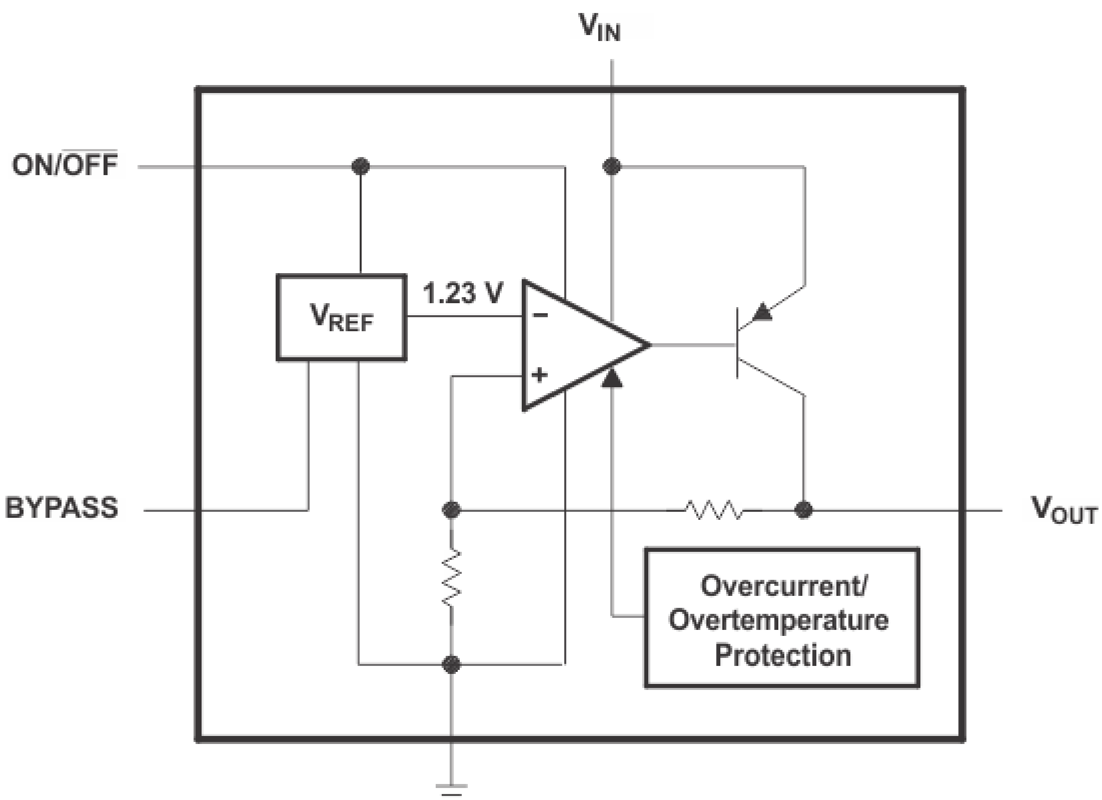


Figure 6-1. Functional Block Diagram (Legacy Chip)

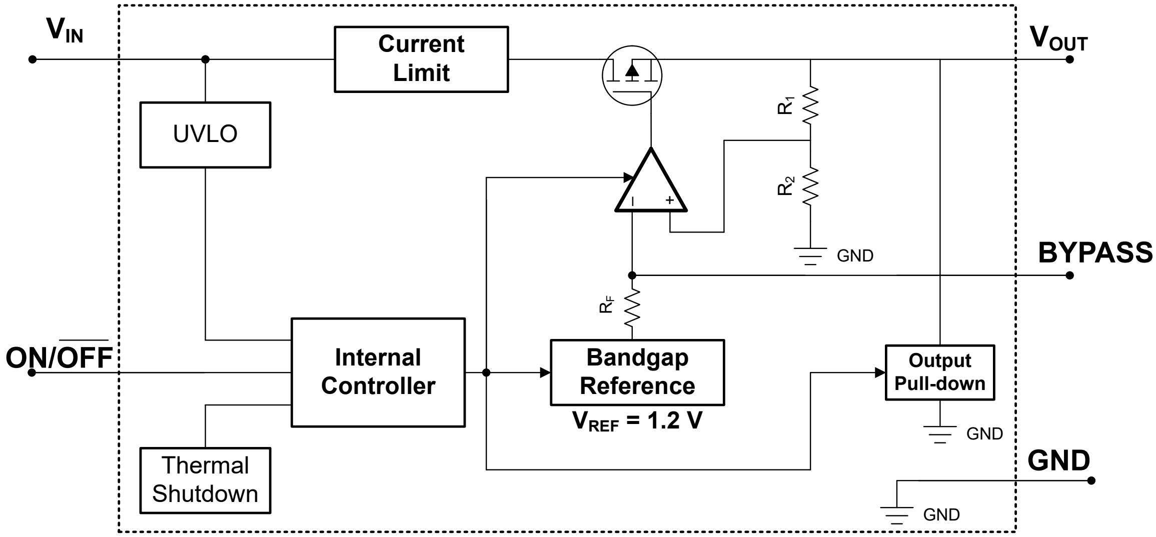


Figure 6-2. Functional Block Diagram (New Chip)

6.3 Feature Description

6.3.1 Output Enable

The ON/$\overline{\text{OFF}}$ pin for the device is an active-high pin. The output voltage is enabled when the voltage of the ON/$\overline{\text{OFF}}$ pin is greater than the high-level input voltage of the ON/$\overline{\text{OFF}}$ pin and disabled with the ON/$\overline{\text{OFF}}$ pin voltage is less than the low-level input voltage of the ON/$\overline{\text{OFF}}$ pin. If independent control of the output voltage is not needed, connect the ON/$\overline{\text{OFF}}$ pin to the input of the device.

In the legacy chip, for proper operation of the ON/$\overline{\text{OFF}}$ functionality, apply a signal with a slew rate of ≥40mV/µs. No slew rate consideration is required for the new chip.

The new chip has an internal pulldown circuit that activates when the device is disabled. Pull the ON/$\overline{\text{OFF}}$ pin voltage lower than the low-level input voltage of the ON/$\overline{\text{OFF}}$ pin, to actively discharge the output voltage.

6.3.2 Dropout Voltage

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage (V_{IN} – V_{OUT}) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \tag{1}$$

6.3.3 Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a brick-wall scheme. In a high-load current fault, the brick-wall scheme limits the output current to the current limit (I_{CL}). I_{CL} is listed in the *Electrical Characteristics* table.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{CL}]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application note.

Figure 6-3 shows a diagram of the current limit.

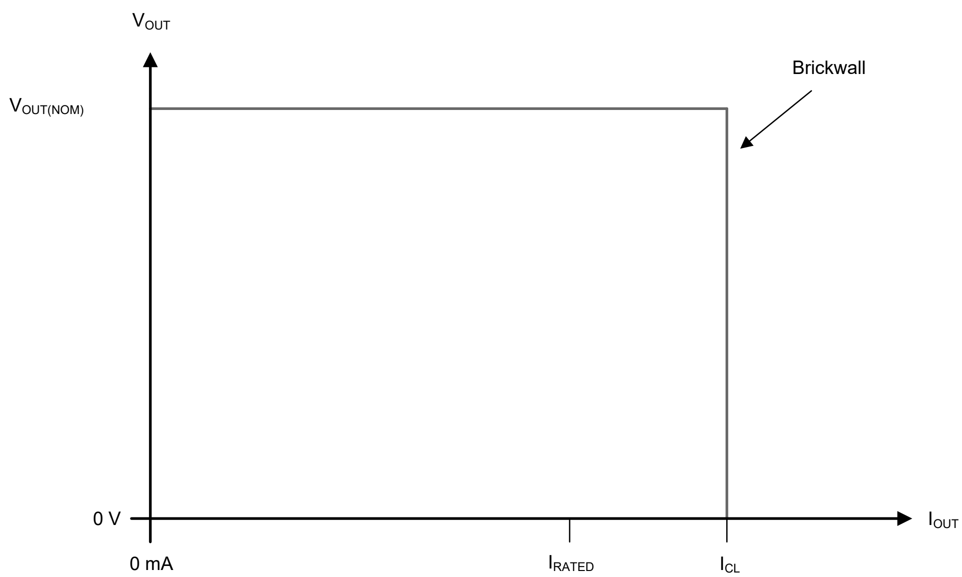


Figure 6-3. Current Limit

6.3.4 Undervoltage Lockout (UVLO)

The new chip has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage, allowing a controlled and consistent turn on and off of the output voltage. To prevent the device from turning off if the input drops during turn on, the UVLO has hysteresis as specified in the *Electrical Characteristics* table.

6.3.5 Output Pulldown

The new chip has an output pulldown circuit. The output pulldown activates in the following conditions:

- When the device is disabled ($V_{ON/\overline{OFF}} < V_{ON/\overline{OFF}(LOW)}$)
- If 1.0 V < V_{IN} < V_{UVLO}

Do not rely on the output pulldown circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can flow from the output to the input. This reverse current flow can cause damage to the device. See the *Reverse Current* section for more details.

6.3.6 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis assures that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short, thus the device can cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start up can be high from large V_{IN} – V_{OUT} voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start up completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

6.4 Device Functional Modes

6.4.1 Device Functional Mode Comparison

Table 6-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

Table 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	$V_{ON/\overline{OFF}}$	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{ON/\overline{OFF}} > V_{ON/\overline{OFF}(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{ON/\overline{OFF}} > V_{ON/\overline{OFF}(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{ON/\overline{OFF}} < V_{ON/\overline{OFF}(LOW)}$	Not applicable	$T_J > T_{SD(shutdown)}$

6.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The ON/$\overline{\text{OFF}}$ voltage has previously exceeded the ON/$\overline{\text{OFF}}$ rising threshold voltage and has not yet decreased to less than the enable falling threshold

6.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during start up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

6.4.4 Disabled

The output of the device can be shutdown by forcing the voltage of the ON/$\overline{\text{OFF}}$ pin to less than the maximum ON/$\overline{\text{OFF}}$ pin low-level input voltage (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Recommended Capacitor Types

7.1.1.1 Recommended Capacitors (Legacy Chip)

Preferably, use ceramic capacitors on the output of the LP2985 for several reasons. For capacitances ranging from 2.2μF to 4.7μF, ceramic capacitors have the lowest cost and lowest ESR, making these components choice candidates for filtering high-frequency noise. For instance, a typical 2.2μF ceramic capacitor has an ESR ranging from 10mΩ to 20mΩ, which satisfies the minimum ESR requirements of the regulator. Ceramic capacitors have one major disadvantage to be taken into account: a poor temperature coefficient, where the capacitance varies significantly with temperature. For instance, a large-value ceramic capacitor (≥ 2.2μF) potentially loses more than half of the capacitance as the temperature rises from 25°C to 85°C. Thus, a 2.2μF capacitor at 25°C drops well below the minimum C_{OUT} required for stability, as ambient temperature rises. For this reason, select an output capacitor that maintains the minimum 2.2μF required for stability over the entire operating temperature range. There are some ceramic capacitors that maintain a ±15% capacitance tolerance over temperature.

Tantalum capacitors are able to be used at the output of the LP2985, but there are significant disadvantages prohibiting this usage:

- In the 1μF to 4.7μF range, tantalum capacitors are more expensive than ceramics of the equivalent capacitance and voltage ratings.
- Tantalum capacitors have higher ESR values than equivalent-sized ceramic counterparts. Thus, to meet the ESR requirements, a higher-capacitance tantalum is required, at the expense of larger size and higher cost.
- The ESR of a tantalum capacitor increases as temperature drops, as much as double from +25°C to –40°C. Thus, maintain ESR margins over the temperature range to prevent regulator instability.

7.1.1.2 Recommended Capacitors (New Chip)

The new chip is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but use good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature. Using Y5V-rated capacitors is discouraged because of large variations in capacitance.

Maximum supported ESR range across complete temperature (−40°C to +125°C) and load current range (0mA−150mA) is less than 1Ω. For existing implementations, where different capacitor types with higher ESR values are used, use a low ESR, 100nF MLCC capacitor. Place this capacitor as close as possible to the device output (V_{OUT}) pin.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. Generally, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors listed in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

7.1.2 Input and Output Capacitor Requirements

7.1.2.1 Input Capacitor Requirements

For the legacy chip, a minimum value of 1μF (over the entire operating temperature range) is required at the input of the LP2985. In addition, place this input capacitor within 1cm of the input pin, connected to a clean analog ground. There are no equivalent series resistance (ESR) requirements for this capacitor; increase capacitance without limit.

For the new chip, although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. Use an input capacitor if the source impedance is more than 0.5Ω. Use a higher value capacitor if large, fast rise-time load or line transients are anticipated. Use this capacitor if the device is located several inches from the input power source.

7.1.2.2 Output Capacitor Requirements

For the legacy chip, the LP2985 permits using low ESR capacitors at the output, including ceramic capacitors that have an ESR as low as 5mΩ. Tantalum and film capacitors are also available if size and cost are not issues. Place the output capacitor within 1cm of the output pin. Make sure this capacitor returns to a clean analog ground. As with other PNP LDOs, stability conditions require the output capacitor to have a minimum capacitance and an ESR that falls within a certain range.

- Minimum C_{OUT}: 2.2µF (increase this capacitance without limit to improve transient response stability margin)
- ESR range: see Figure 5-36 through Figure 5-38

Both the minimum capacitance and ESR requirement are critical to be met over the entire operating temperature range. Depending on the type of capacitors used, both these parameters potentially vary significantly with temperature (see the *Recommended Capacitors (Legacy Chip)* section).

For the new chip, dynamic performance of the device is improved with the use of an output capacitor. Use an output capacitor within the range specified in the *Recommended Operating Conditions* table for stability. Review the *Recommended Capacitors (New Chip)* section for further information on supported output capacitors.

7.1.3 Noise Bypass Capacitor (C_{BYPASS})

The LP2985 allows for low-noise performance with the use of a bypass capacitor that is connected to the internal band-gap reference with the BYPASS pin. This high-impedance band-gap circuitry is biased in the microampere range and, thus, cannot be loaded significantly, otherwise, the output (and, correspondingly, the output of the regulator) changes. Thus, for best output accuracy, dc leakage current through C_{BYPASS} must be minimized as much as possible and must never exceed 100 nA. The C_{BYPASS} capacitor also impacts the start-up behavior of the regulator. Inrush current and start-up time increase with larger bypass capacitor values.

Use a 10-nF capacitor for C_{BYPASS}. Ceramic and film capacitors are good choices for this purpose.

7.1.4 Reverse Current

Excessive reverse current can damage this device. Reverse current flows through the intrinsic body diode of the pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} \leq V_{IN} + 0.3$ V.

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, use external protection to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated.

Figure 7-1 shows one approach for protecting the device.

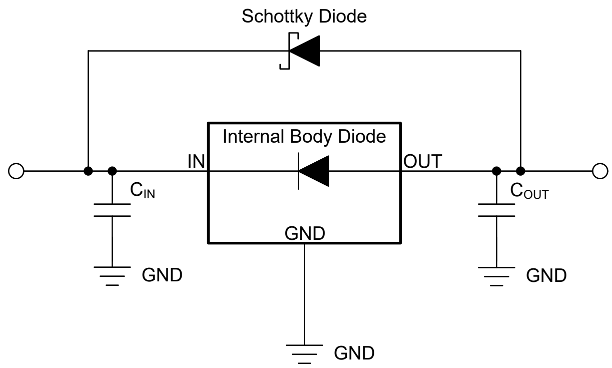


Figure 7-1. Example Circuit for Reverse Current Protection Using a Schottky Diode

7.1.5 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation (P_D).

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \tag{2}$$

Note

Power dissipation can be minimized, and therefore greater efficiency can be achieved, by correct selection of the system voltage rails. For the lowest power dissipation use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to the following equation, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \tag{3}$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance.

7.1.6 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the linear regulator when in-circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter (ψ_{JT}) and junction-to-board characterization parameter (ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J), as described in the following equations. Use the junction-to-top characterization parameter (ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. Use the junction-to-board characterization parameter (ψ_{JB}) with the PCB surface temperature 1 mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \psi_{JT} \times P_D \tag{4}$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

$$T_J = T_B + \psi_{JB} \times P_D \tag{5}$$

where:

- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the *Semiconductor and IC Package Thermal Metrics* application note.

7.2 Typical Application

Figure 7-2 shows the standard usage of the LP2985 as a low-dropout regulator.

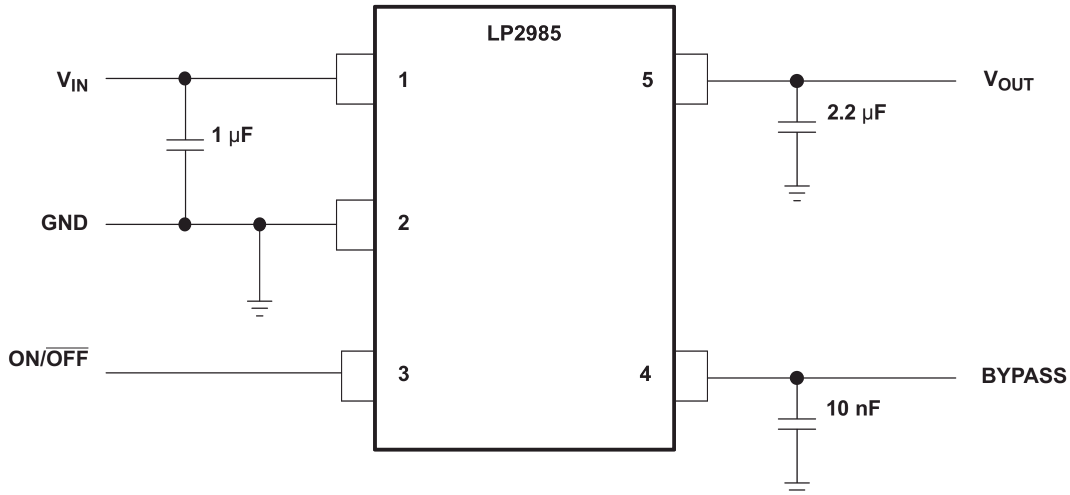


Figure 7-2. LP2985 Typical Application

7.2.1 Design Requirements

Minimum C_{OUT} value for stability (can be increased without limit for improved stability and transient response)

ON/$\overline{\text{OFF}}$ must be actively terminated. Connect to V_{IN} if shutdown feature is not used.

Optional BYPASS capacitor for low-noise operation.

7.2.2 Detailed Design Procedure

7.2.2.1 ON/$\overline{\text{OFF}}$ Operation

The LP2985 allows for a shutdown mode via the ON/$\overline{\text{OFF}}$ pin. Driving the pin LOW (≤ 0.4 V) turns the device OFF; conversely, a HIGH (≥ 1.2 V) turns the device ON. If the shutdown feature is not used, connect ON/$\overline{\text{OFF}}$ to the input to ensure that the regulator is on at all times. For proper operation, do not leave ON/$\overline{\text{OFF}}$ unconnected.

7.2.3 Application Curves

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, ON/$\overline{\text{OFF}}$ pin tied to V_{IN}, C_{IN} = 1.0 µF, and C_{OUT} = 4.7 µF (unless otherwise noted)

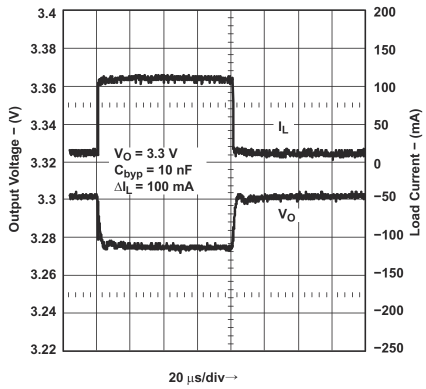


Figure 7-3. Load Transient Response for Legacy Chip

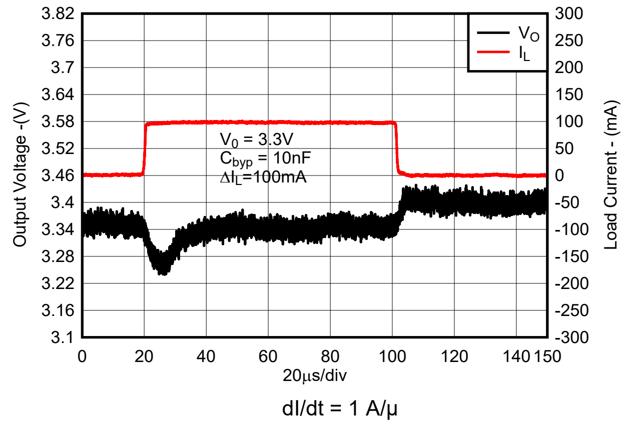


Figure 7-4. Load Transient Response for New Chip

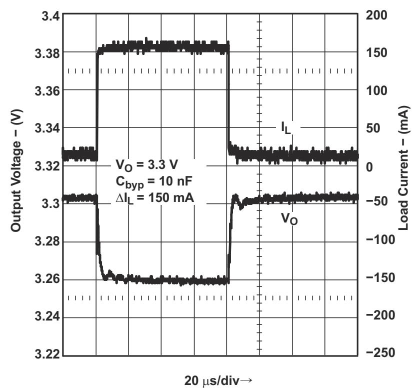


Figure 7-5. Load Transient Response for Legacy Chip

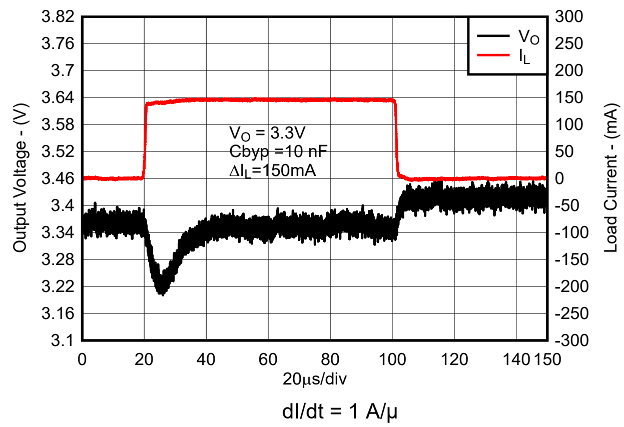


Figure 7-6. Load Transient for New Chip

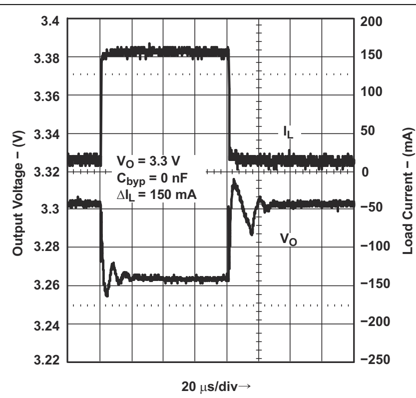


Figure 7-7. Load Transient Response for Legacy Chip

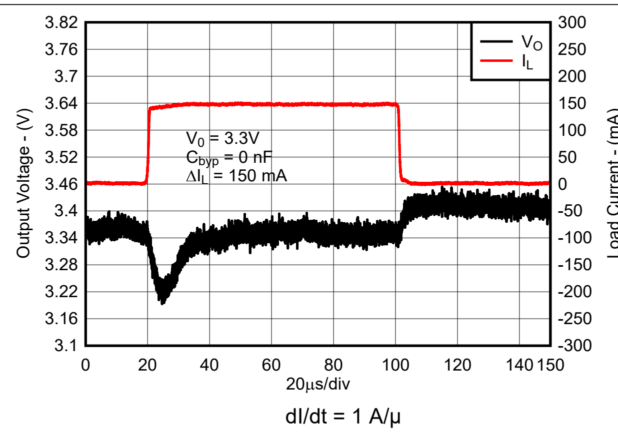


Figure 7-8. Load Transient Response for New Chip

7.2.3 Application Curves (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, ON/$\overline{OFF}$ pin tied to V_{IN}, C_{IN} = 1.0 µF, and C_{OUT} = 4.7 µF (unless otherwise noted)

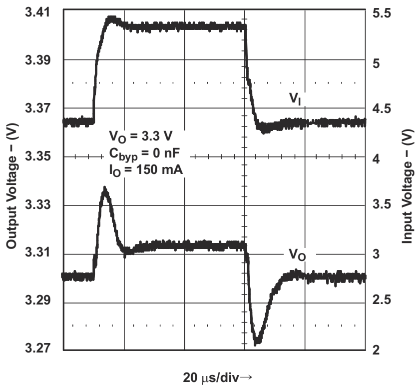
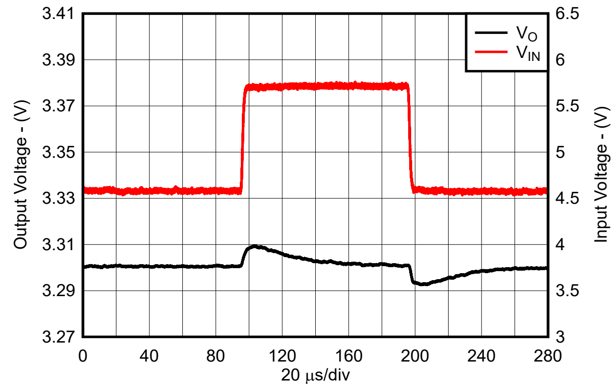


Figure 7-9. Line Transient Response for Legacy Chip



V_{OUT} = 3.3 V, C_{BYP} = 0 nF, ΔV_{IN} = 1 V, I_{OUT} = 150 mA, dV/dt = 1 V/µ

Figure 7-10. Line Transient Response for New Chip

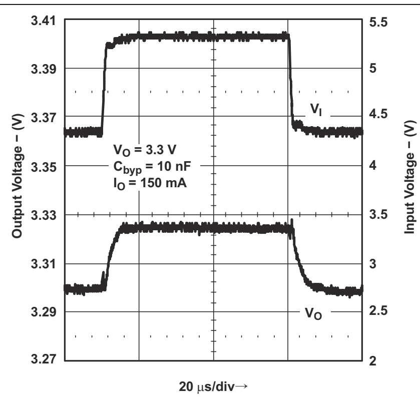
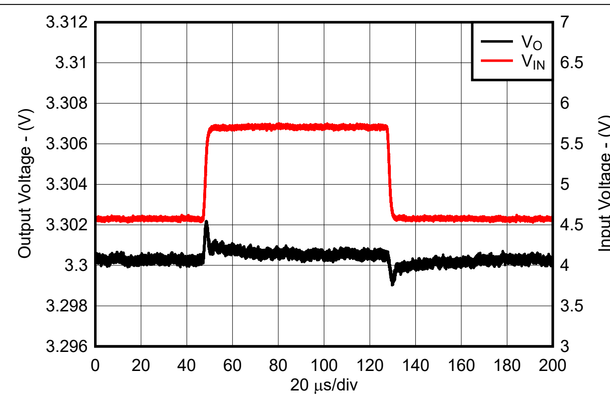


Figure 7-11. Line Transient Response for Legacy Chip



V_{OUT} = 3.3 V, C_{BYP} = 10 nF, ΔV_{IN} = 1 V, I_{OUT} = 150 mA, dV/dt = 1 V/µ

Figure 7-12. Line Transient Response for New Chip

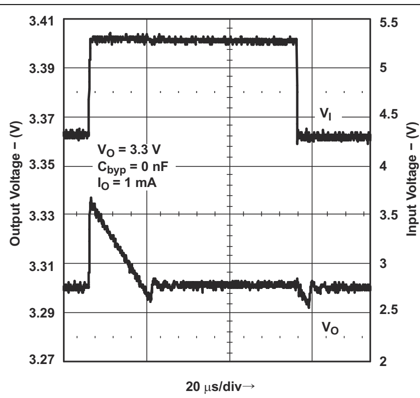
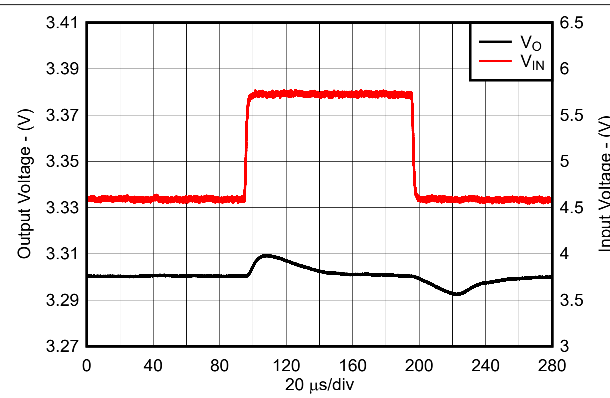


Figure 7-13. Line Transient Response for Legacy Chip



V_{OUT} = 3.3 V, C_{BYP} = 0 nF, ΔV_{IN} = 1 V, I_{OUT} = 1 mA, dV/dt = 1 V/µ

Figure 7-14. Line Transient Response for New Chip

7.2.3 Application Curves (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, ON/$\overline{OFF}$ pin tied to V_{IN}, C_{IN} = 1.0 µF, and C_{OUT} = 4.7 µF (unless otherwise noted)

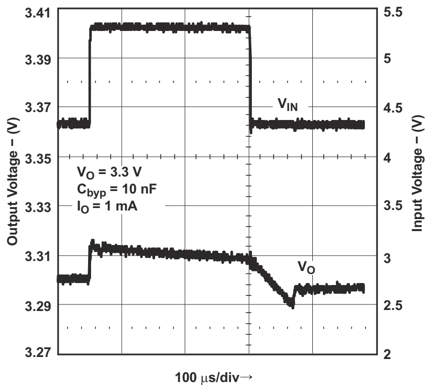
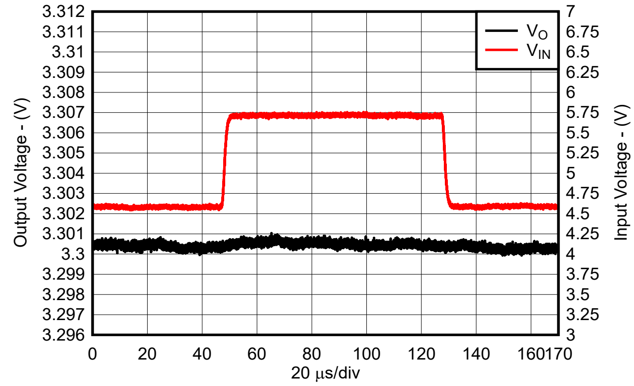


Figure 7-15. Line Transient Response for Legacy Chip



V_{OUT} = 3.3 V, C_{BYP} = 10 nF, ΔV_{IN} = 1 V, I_{OUT} = 1 mA, dV/dt = 1 V/µ

Figure 7-16. Line Transient Response for New Chip

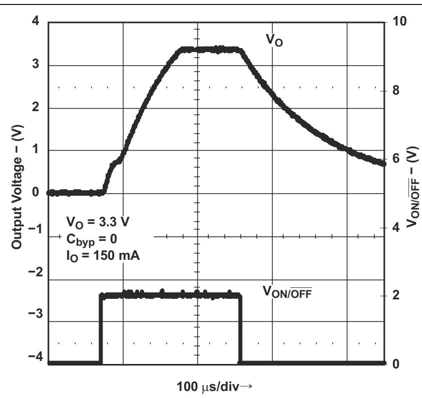


Figure 7-17. Turn-On Time for Legacy Chip

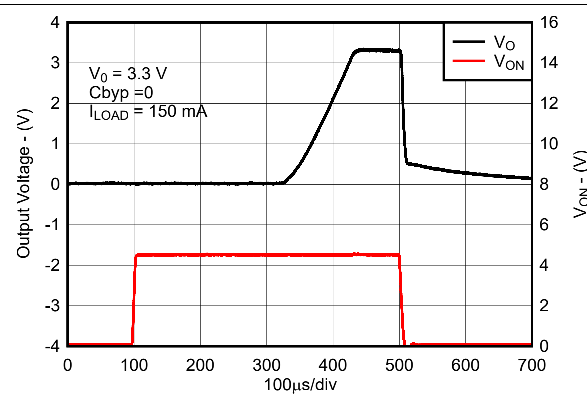


Figure 7-18. Turn-On Time for New Chip

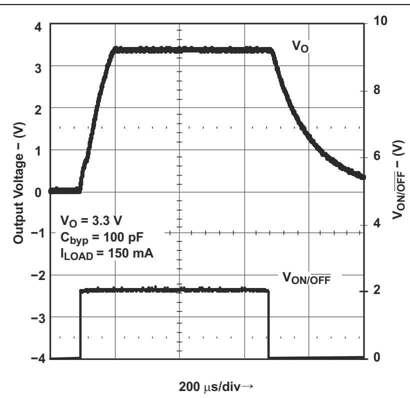


Figure 7-19. Turn-On Time for Legacy Chip

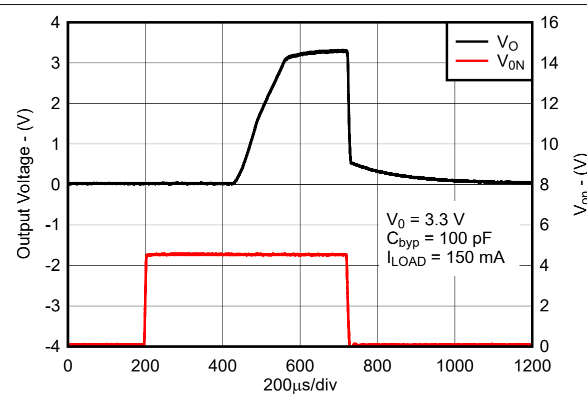
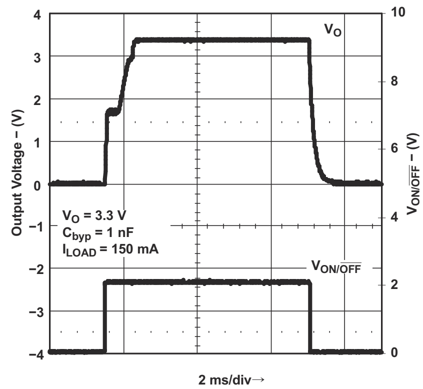


Figure 7-20. Turn-On Time for New Chip

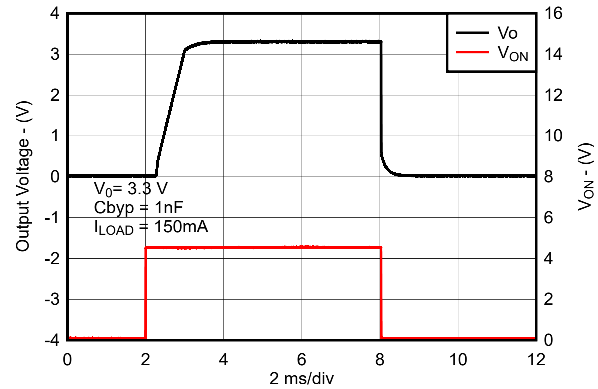
7.2.3 Application Curves (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, ON/$\overline{OFF}$ pin tied to V_{IN}, C_{IN} = 1.0 µF, and C_{OUT} = 4.7 µF (unless otherwise noted)



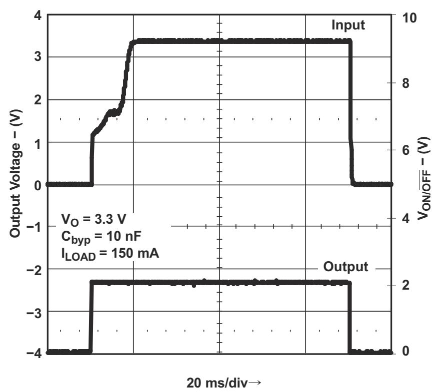
C_{OUT} = 4.7 µF

Figure 7-21. Turn-On Time for Legacy Chip



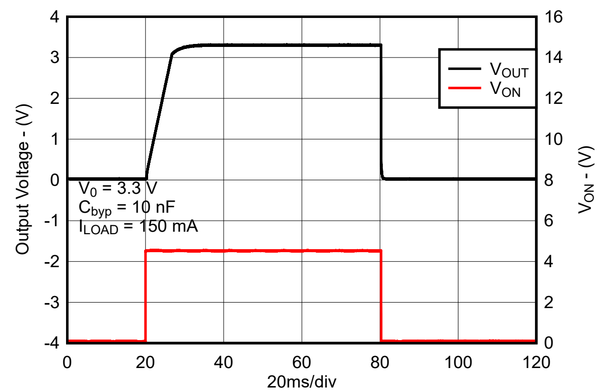
C_{OUT} = 4.7 µF

Figure 7-22. Turn-On Time for New Chip



C_{OUT} = 4.7 µF

Figure 7-23. Turn-On Time



C_{OUT} = 4.7 µF

Figure 7-24. Turn-On Time for New Chip

7.3 Power Supply Recommendations

A power supply can be used at the input voltage within the ranges given in the *Recommended Operating Conditions* table. Use bypass capacitors as described in the *Layout Guidelines* section.

7.4 Layout

7.4.1 Layout Guidelines

- Bypass the input pin to ground with a bypass capacitor.
- The optimum placement of the bypass capacitor is closest to the V_{IN} of the device and GND of the system. Care must be taken to minimize the loop area formed by the bypass capacitor connection, the V_{IN} pin, and the GND pin of the system.
- For operation at full-rated load, use wide trace lengths to eliminate IR drop and heat dissipation.

7.4.2 Layout Example

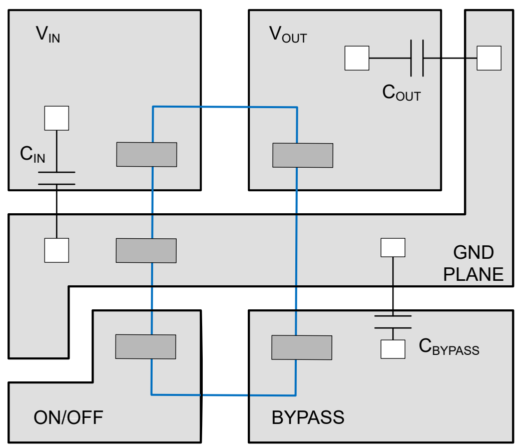


Figure 7-25. Layout Diagram

8 Device and Documentation Support

8.1 Device Support

8.1.1 Device Nomenclature

Table 8-1. Available Options

PRODUCT(1)	DESCRIPTION
LP2985**c-xxyyyz*M3***	**c** is the accuracy specification for the legacy chip (*A* or blank). See the *Electrical Characteristics* table for more information. This character is insignificant for the new chip. **xx** is the nominal output voltage (for example, 33 = 3.3V; 50 = 5.0V). **yyy** is the package designator (DBV = SOT-23). **z** is the reel designator size. See the Package Addendum for more information on package quantity. This device ships with the legacy chip (CSO: DLN or GF8) or the new chip (CSO: RFB), which uses the latest manufacturing flow. The reel packaging label provides CSO information to distinguish which chip is used. Device performance for new and legacy chips is denoted throughout the document. **M3** is a suffix designator only significant for the new chip with CSO:RFB, which uses the latest manufacturing flow.

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision R (July 2023) to Revision S (May 2025)	Page
• Added nomenclature distinguishing between new chip and legacy chip information throughout document	1
• Changed *Overview* section: changed 1% to ±1%, deleted line variation, and clarified new chip features	15
• Added *Functional Block Diagram (Legacy Chip)* figure	15
• Changed *Output Enable* section to identify differences between new and legacy chip functionality	16
• Changed *Recommended Capacitor Types* section and added subsections	20
• Changed *Input and Output Capacitor Requirements* section	20
• Changed *Device Nomenclature* section	30

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP2985-10DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LRCG
LP2985-10DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LRCG
LP2985-10DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LRCG
LP2985-10DBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LRCG
LP2985-18DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(LPHG, LPHL)
LP2985-18DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(LPHG, LPHL)
LP2985-18DBVRE4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LPHG
LP2985-18DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LPHG
LP2985-18DBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LPHG
LP2985-18DBVRM3	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LPHG
LP2985-18DBVRM3.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LPHG
LP2985-18DBVT	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 125	(LPHG, LPHL)
LP2985-18DBVTG4	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LPHG
LP2985-18DBVTG4.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LPHG
LP2985-25DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(LPLG, LPLL)
LP2985-25DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(LPLG, LPLL)
LP2985-25DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LPLG, LPLL)
LP2985-25DBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LPLG, LPLL)
LP2985-28DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(LPGG, LPGL)
LP2985-28DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(LPGG, LPGL)
LP2985-28DBVTG4	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LPGG
LP2985-28DBVTG4.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LPGG
LP2985-29DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LPMG
LP2985-29DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LPMG
LP2985-30DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(LPNG, LPNL)
LP2985-30DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LPNG, LPNL)
LP2985-30DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LPNG, LPNL)
LP2985-30DBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LPNG, LPNL)
LP2985-30DBVT	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 125	(LPNG, LPNL)

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP2985-33DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(LPFG, LPFL)
LP2985-33DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(LPFG, LPFL)
LP2985-33DBVRE4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LPFG
LP2985-33DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LPFG
LP2985-33DBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LPFG
LP2985-33DBVRM3	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LPFG
LP2985-33DBVRM3.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LPFG
LP2985-33DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(LPFG, LPFL)
LP2985-33DBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(LPFG, LPFL)
LP2985-33DBVTG4	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 125	LPFG
LP2985-33DBVTM3	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LPFG
LP2985-33DBVTM3.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LPFG
LP2985-50DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(LPSG, LPSL)
LP2985-50DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LPSG, LPSL)
LP2985-50DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(LPSG, LPSL)
LP2985-50DBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LPSG, LPSL)
LP2985-50DBVTG4	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LPSG, LPSL)
LP2985-50DBVTG4.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LPSG, LPSL)
LP2985-50DBVTM3	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LPSG
LP2985-50DBVTM3.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LPSG
LP2985A-10DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LRDG
LP2985A-10DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LRDG
LP2985A-10DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LRDG
LP2985A-10DBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LRDG
LP2985A-18DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(LPTG, LPTL)
LP2985A-18DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(LPTG, LPTL)
LP2985A-18DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LPTG
LP2985A-18DBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LPTG
LP2985A-18DBVT	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 125	(LPTG, LPTL)
LP2985A-25DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(LPUG, LPUL)
LP2985A-25DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LPUG, LPUL)

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP2985A-25DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LPUG, LPUL)
LP2985A-25DBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LPUG, LPUL)
LP2985A-25DBVRM3	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-45 to 125	(LP7G, LPUG)
LP2985A-25DBVRM3.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-45 to 125	(LP7G, LPUG)
LP2985A-25DBVT	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 125	(LPUG, LPUL)
LP2985A-28DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(LPJG, LPJL)
LP2985A-28DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LPJG, LPJL)
LP2985A-29DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LPZG, LPZL)
LP2985A-29DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LPZG, LPZL)
LP2985A-30DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(LRAG, LRAL)
LP2985A-30DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(LRAG, LRAL)
LP2985A-30DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LRAG, LRAL)
LP2985A-30DBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LRAG, LRAL)
LP2985A-33DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(LPKG, LPKL)
LP2985A-33DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LPKG, LPKL)
LP2985A-33DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LPKG
LP2985A-33DBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LPKG
LP2985A-33DBVRM3	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LPKG
LP2985A-33DBVRM3.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LPKG
LP2985A-33DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(LPFG, LPKG, LPKL)
LP2985A-33DBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(LPFG, LPKG, LPKL)
LP2985A-33DBVTE4	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LPKG
LP2985A-33DBVTG4	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LPKG
LP2985A-33DBVTG4.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LPKG
LP2985A-50DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(LR1G, LR1L)
LP2985A-50DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LR1G, LR1L)
LP2985A-50DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LR1G, LR1L)
LP2985A-50DBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LR1G, LR1L)
LP2985A-50DBVRM3	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LR1G

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP2985A-50DBVRM3.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LR1G
LP2985A-50DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(LPSG, LR1G, LR1L)
LP2985A-50DBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(LPSG, LR1G, LR1L)

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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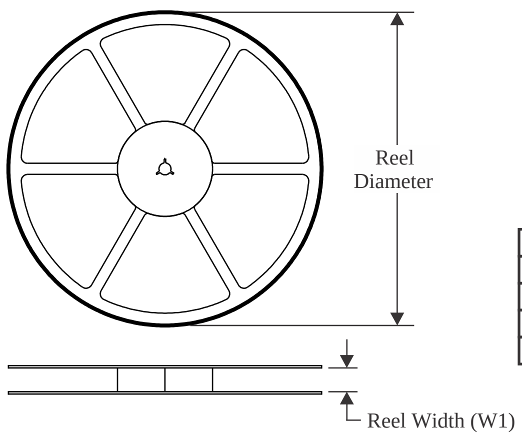
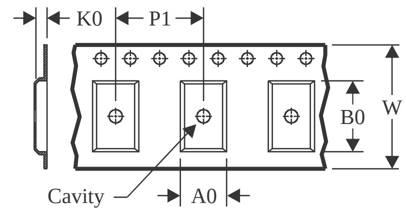
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

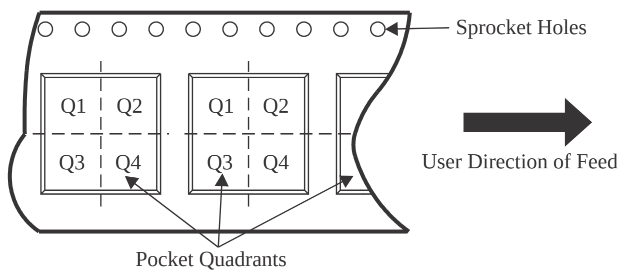


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

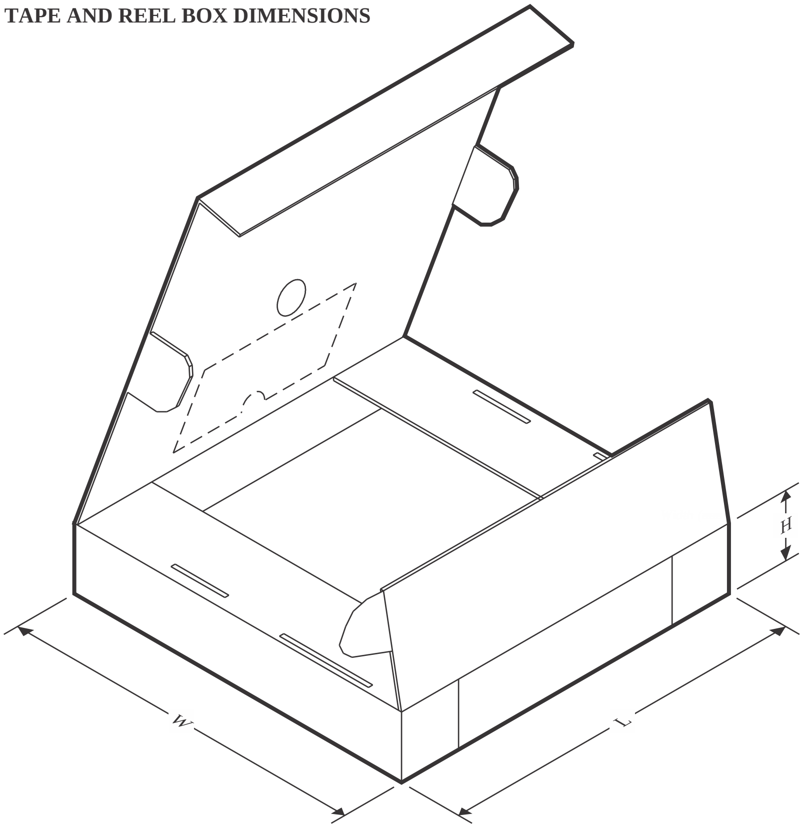


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2985-10DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LP2985-10DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
LP2985-18DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985-18DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985-18DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
LP2985-18DBVRM3	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985-18DBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LP2985-25DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985-28DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985-28DBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
LP2985-29DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LP2985-30DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985-30DBVRG4	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985-33DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985-33DBVRG4	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985-33DBVRM3	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2985-33DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985-33DBVTM3	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985-50DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985-50DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985-50DBVTG4	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985-50DBVTM3	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985A-10DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LP2985A-10DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
LP2985A-18DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985A-18DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LP2985A-25DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985A-25DBVRG4	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985A-25DBVRM3	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985A-28DBVR	SOT-23	DBV	5	3000	180.0	9.2	3.17	3.23	1.37	4.0	8.0	Q3
LP2985A-28DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LP2985A-29DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LP2985A-30DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985A-33DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985A-33DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985A-33DBVRG4	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985A-33DBVRM3	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985A-33DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985A-33DBVTG4	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985A-50DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985A-50DBVRG4	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985A-50DBVRM3	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985A-50DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

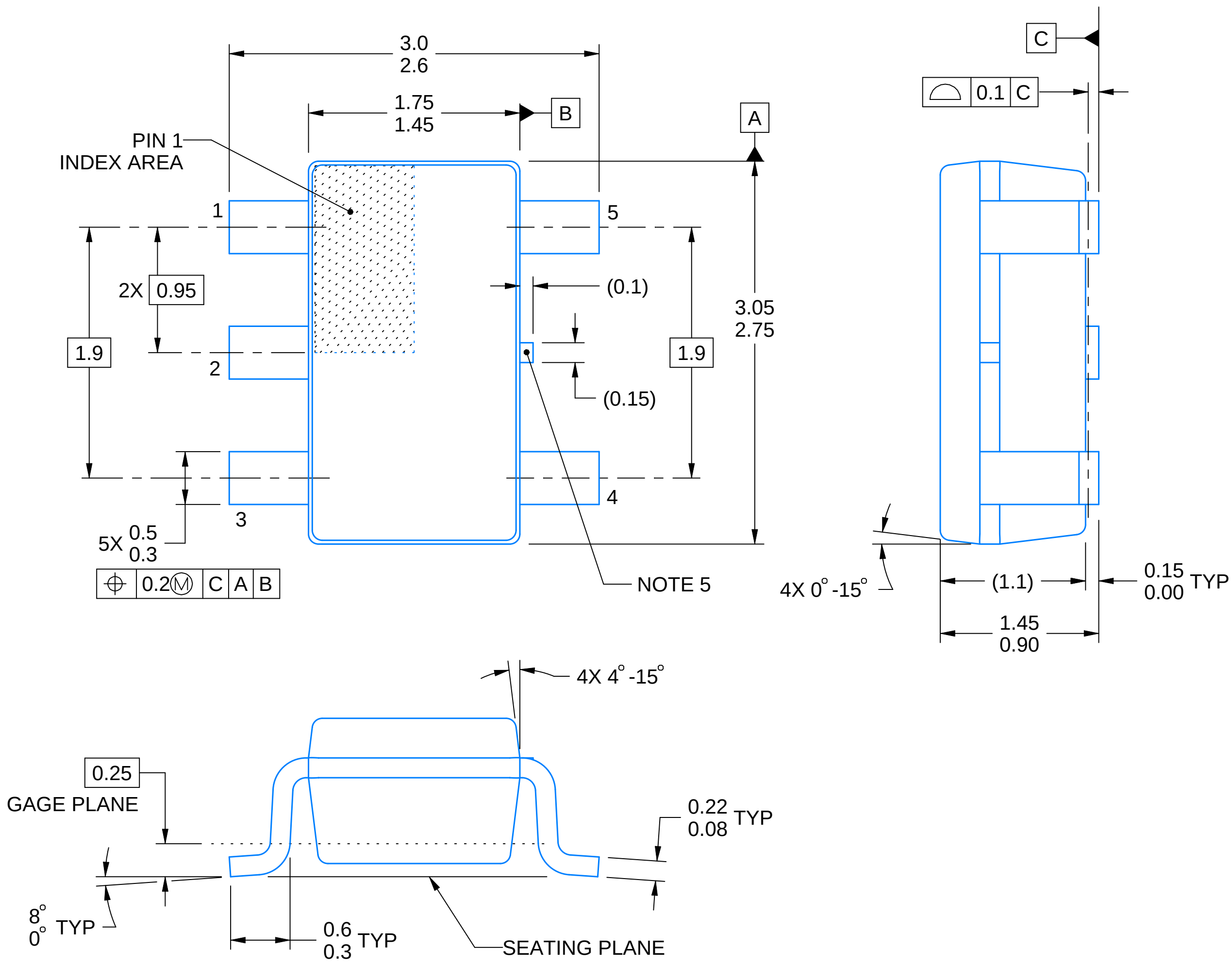
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2985-10DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
LP2985-10DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
LP2985-18DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2985-18DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985-18DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
LP2985-18DBVRM3	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985-18DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
LP2985-25DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2985-28DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2985-28DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
LP2985-29DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
LP2985-30DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2985-30DBVRG4	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985-33DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985-33DBVRG4	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985-33DBVRM3	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985-33DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
LP2985-33DBVTM3	SOT-23	DBV	5	250	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2985-50DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985-50DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
LP2985-50DBVTG4	SOT-23	DBV	5	250	210.0	185.0	35.0
LP2985-50DBVTM3	SOT-23	DBV	5	250	210.0	185.0	35.0
LP2985A-10DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
LP2985A-10DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
LP2985A-18DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985A-18DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
LP2985A-25DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2985A-25DBVRG4	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985A-25DBVRM3	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2985A-28DBVR	SOT-23	DBV	5	3000	205.0	200.0	33.0
LP2985A-28DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
LP2985A-29DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
LP2985A-30DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2985A-33DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2985A-33DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985A-33DBVRG4	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985A-33DBVRM3	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2985A-33DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
LP2985A-33DBVTG4	SOT-23	DBV	5	250	210.0	185.0	35.0
LP2985A-50DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985A-50DBVRG4	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985A-50DBVRM3	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2985A-50DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0



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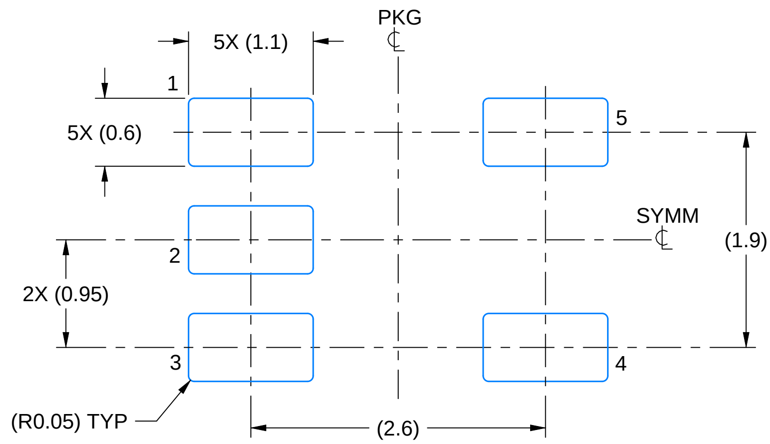
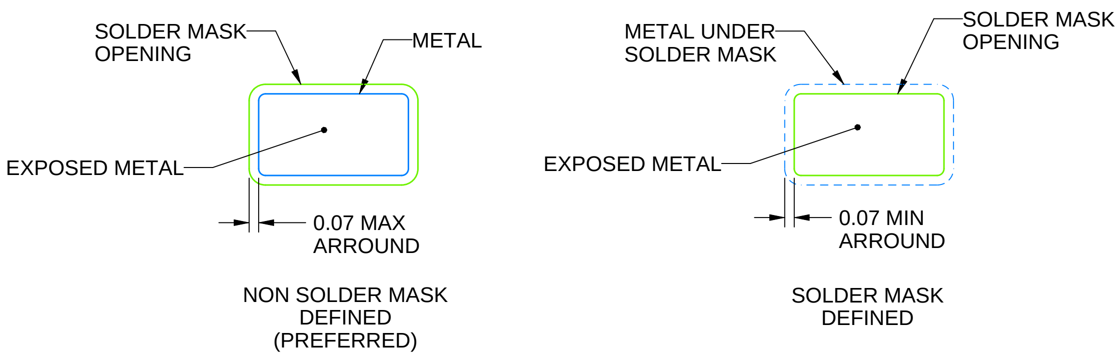
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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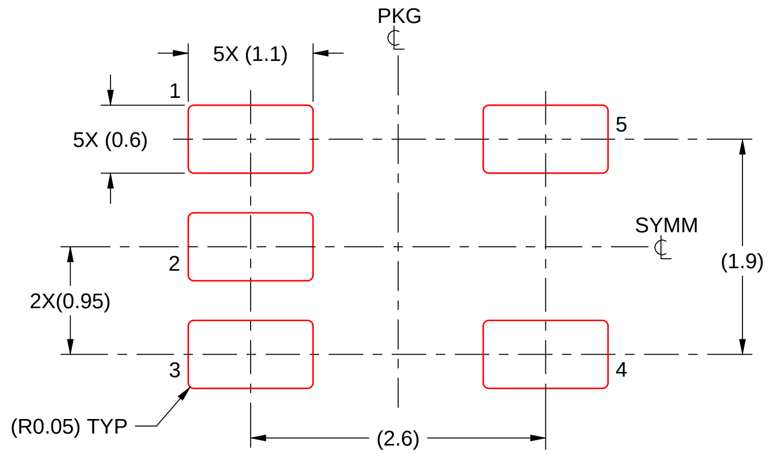
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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