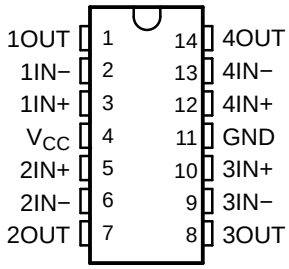
FEATURES

- **Low Supply Current . . . 85 μA Typ**
- **Low Offset Voltage . . . 2 mV Typ**
- **Low Input Bias Current . . . 2 nA Typ**
- **Input Common Mode to GND**
- **Wide Supply Voltage . . . 3 V < V_{CC} < 32 V**
- **Pin Compatible With LM324**
- **Applications**
  - **LCD Displays**
  - **Portable Instrumentation**
  - **Sensor/Metering Equipment**
  - **Consumer Electronics (MP3 Players, Toys, Etc.)**
  - **Power Supplies**

D, N, OR PW PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The LP324 and LP2902 are quadruple low-power operational amplifiers especially suited for battery-operated applications. Good input specifications and wide supply-voltage range still are achieved, despite the ultra-low supply current. Single-supply operation is achieved with an input common-mode range that includes GND.

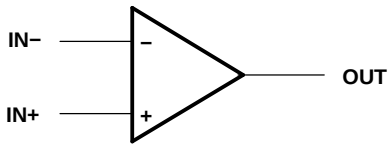
The LP324 and LP2902 are ideal in applications where wide supply voltage and low power are more important than speed and bandwidth. These applications include portable instrumentation, LCD displays, consumer electronics (MP3 players, toys, etc.), and power supplies.

ORDERING INFORMATION

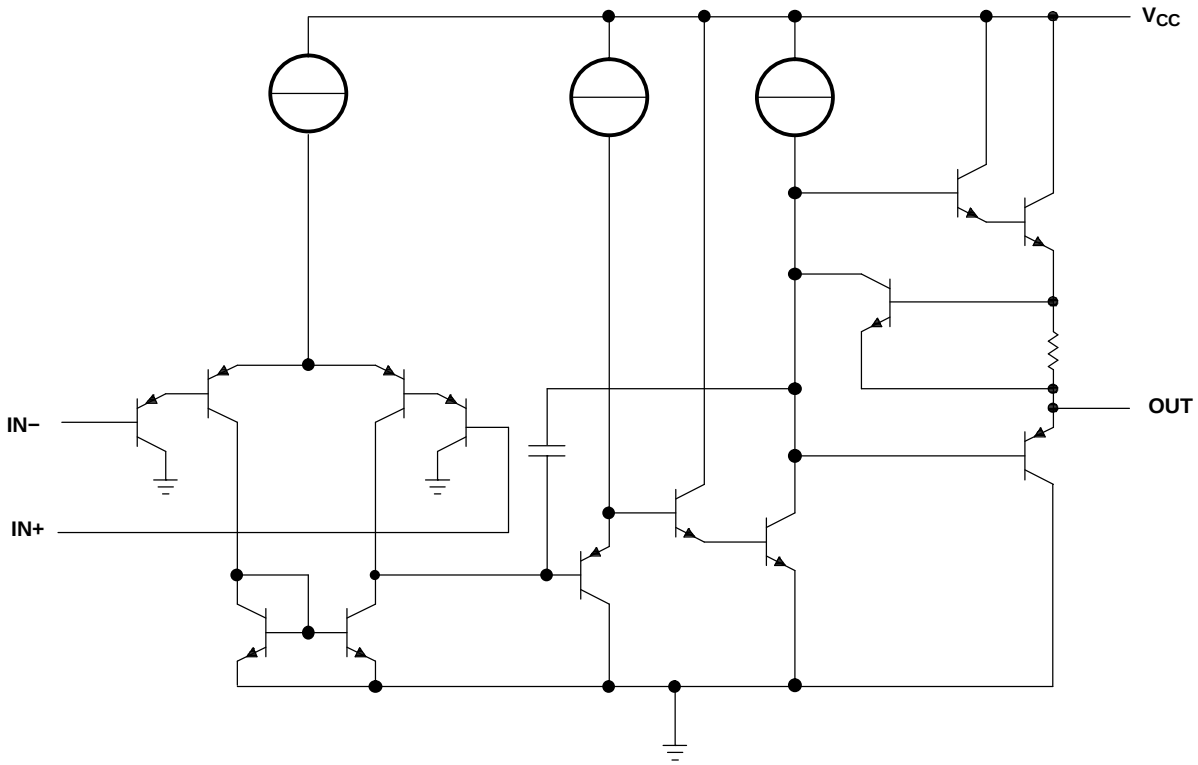
T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube of 25	LP324N	LP324N
	SOIC – D	Tube of 50	LP324D	LP324
		Reel of 2500	LP324DR	
	TSSOP – PW	Tube of 90	LP324PW	LP324
		Reel of 2000	LP324PWR	
–40°C to 85°C	PDIP – N	Tube of 25	LP2902N	LP2902N
	SOIC – D	Tube of 50	LP2902D	LP2902
		Reel of 2500	LP2902DR	
	TSSOP – PW	Tube of 50	LP2902PW	LP2902
		Reel of 2500	LP2902PWR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

SYMBOL (EACH AMPLIFIER)



SCHEMATIC (EACH AMPLIFIER)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range(2)			±16 or 32	V
V_{ID}	Differential input voltage(3)			±32	V
V_I	Input voltage (either input)		–0.3	32	V
	Duration of output short circuit (one amplifier) to ground at (or below) T_A = 25°C, V_{CC} ≤ 15 V(4)			Unlimited	
θ_{JA}	Package thermal impedance(5)(6)	D package		86	°C/W
		N package		80	
		PW package		113	
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values (except differential voltages and V_{CC} specified for the measurement of I_{OS}) are with respect to the network GND.
(3) Differential voltages are at IN+, with respect to IN–.
(4) Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.
(5) Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.

ESD Protection

TEST CONDITIONS	TYP	UNIT
Human-Body Model	±2	kV

Electrical Characteristics

T_A = 25°C, V_{CC} = 5 V, V_{IC} = V_{CC}/2, R_L = 100 kΩ to GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)	T_A(2)	LP324			LP2902			UNIT
				MIN	TYP(3)	MAX	MIN	TYP(3)	MAX	
V_{IO}	Input offset voltage		25°C		2	4		2	4	mV
			Full range			9			10	
I_{IB}	Input bias current		25°C		2	10		2	20	nA
			Full range			20			40	
I_{IO}	Input offset current		25°C		0.2	2		0.5	4	nA
			Full range			4			8	
A_V	Large-signal voltage gain	R_L = 10 kΩ to GND, V_{CC} = 30 V	25°C	50	100		40	70		V/mV
			Full range	40			30			
CMRR	Common-mode rejection ratio	V_{CC} = 30 V, V_{IC} = 0 V to V_{CC} – 1.5 V	25°C	80	90		80	90		dB
			Full range	75			75			
k_{VSR}	Power-supply rejection ratio	V_{CC} = 5 V to 30 V	25°C	80	90		80	90		V
			Full range	75			75			
I_{CC}	Supply current	R_L = ∞	25°C		85	150		85	150	µA
			Full range			250			275	
V_{OH}	Output voltage swing (high)	I_L = 0.35 mA to GND, V_{IC} = 0 V	25°C	3.4	3.6		3.4	3.6		V
			Full range	V_{CC} – 1.9			V_{CC} – 1.9			
V_{OL}	Output voltage swing (low)	I_L = 0.35 mA from V_{CC}, V_{IC} = 0 V	25°C	0.82	0.7		0.82	0.7		V
			Full range	1			1			
I_O	Output source current	V_O = 3 V, V_{ID} = 1 V	25°C	7	10		7	10		mA
			Full range	4			4			
I_O	Output sink current	V_O = 1.5 V, V_{ID} = –1 V	25°C	4	5		4	5		mA
			Full range	3			3			
		V_O = 1.5 V, V_{ID} = –1 V, V_{IC} = 0 V	25°C	2	4		2	4		
			Full range	1			1			
$I_{OS,GND}$	Output short to GND	V_{ID} = 1 V	25°C		20	35		20	35	mA
			Full range			40			40	
$I_{OS,VCC}$	Output short to V_{CC}	V_{ID} = –1 V	25°C		15	30		15	30	mA
			Full range			45			45	
$\propto V_{IO}$	Input offset voltage drift		25°C		10			10		µV/°C
$\propto I_{IO}$	Input offset current drift		25°C		10			10		pA/°C

(1) For full-range temperature limits: V_{CC} = 3 V to 32 V, V_{ICR} = 0 V to V_{CC} – 1.5 V (unless otherwise noted)
(2) Full range is 0°C to 70°C for LP324 and –40°C to 85°C for LP2902.
(3) All typical values are at T_A = 25°C.

Operating Conditions

V_{CC} = ±15 V, T_A = 25°C

PARAMETER		TYP	UNIT
GBW	Gain bandwidth product	100	kHz
SR	Slew rate	50	V/ms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP2902D	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 85	LP2902
LP2902DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LP2902
LP2902DR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LP2902
LP2902DR.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LP2902
LP2902N	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	LP2902N
LP2902N.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	LP2902N
LP2902PW	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	-40 to 85	LP2902
LP2902PWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LP2902
LP2902PWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LP2902
LP2902PWR.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LP2902
LP2902PWRE4	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
LP324D	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	0 to 70	LP324
LP324DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	LP324
LP324DR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LP324
LP324DR.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LP324
LP324DRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LP324
LP324DRG4.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LP324
LP324N	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	LP324N
LP324N.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	LP324N
LP324PW	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	0 to 70	LP324
LP324PWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LP324
LP324PWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LP324
LP324PWR.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LP324

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

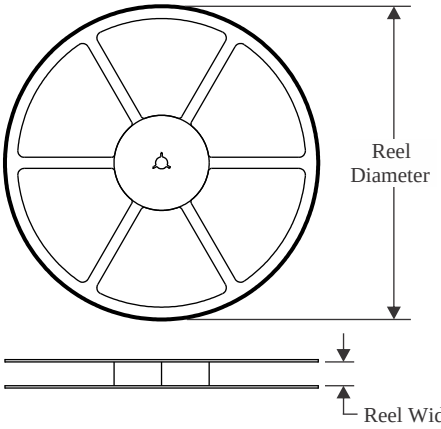
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

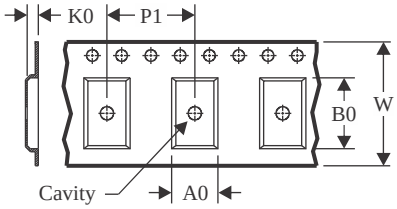
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

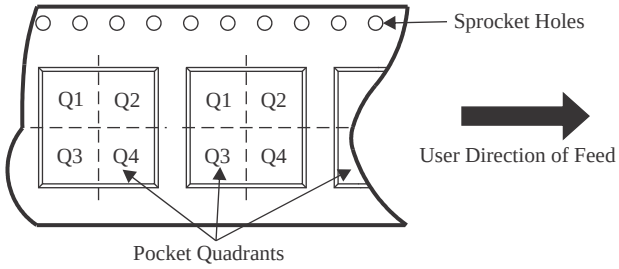


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

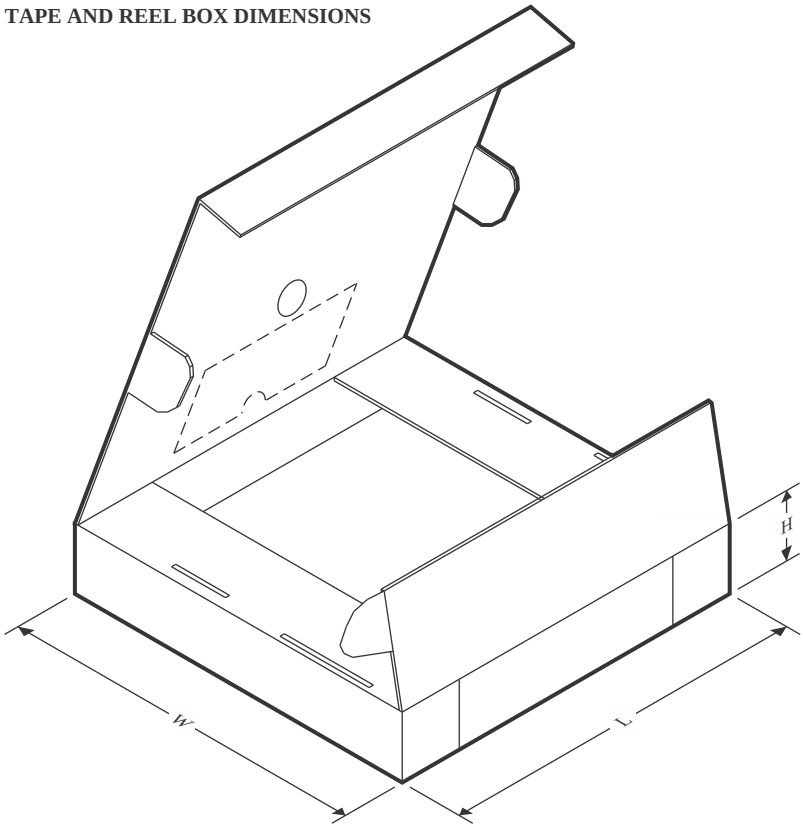
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2902DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LP2902PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LP324DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LP324DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LP324PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

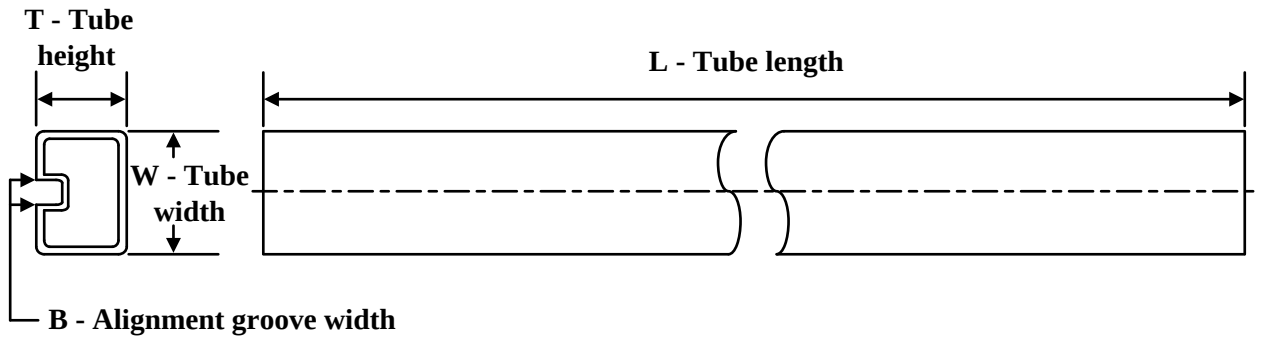
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2902DR	SOIC	D	14	2500	353.0	353.0	32.0
LP2902PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
LP324DR	SOIC	D	14	2500	353.0	353.0	32.0
LP324DRG4	SOIC	D	14	2500	340.5	336.1	32.0
LP324PWR	TSSOP	PW	14	2000	353.0	353.0	32.0

TUBE



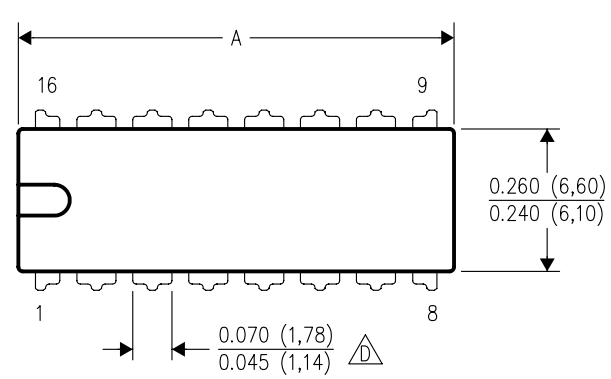
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LP2902N	N	PDIP	14	25	506	13.97	11230	4.32
LP2902N.A	N	PDIP	14	25	506	13.97	11230	4.32
LP324N	N	PDIP	14	25	506	13.97	11230	4.32
LP324N.A	N	PDIP	14	25	506	13.97	11230	4.32

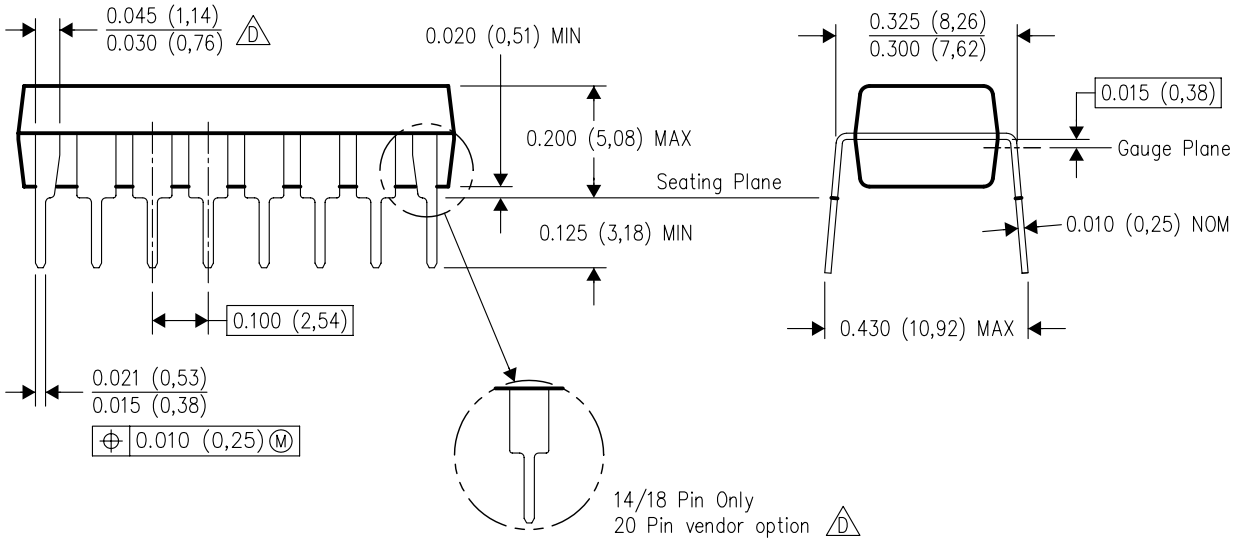
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

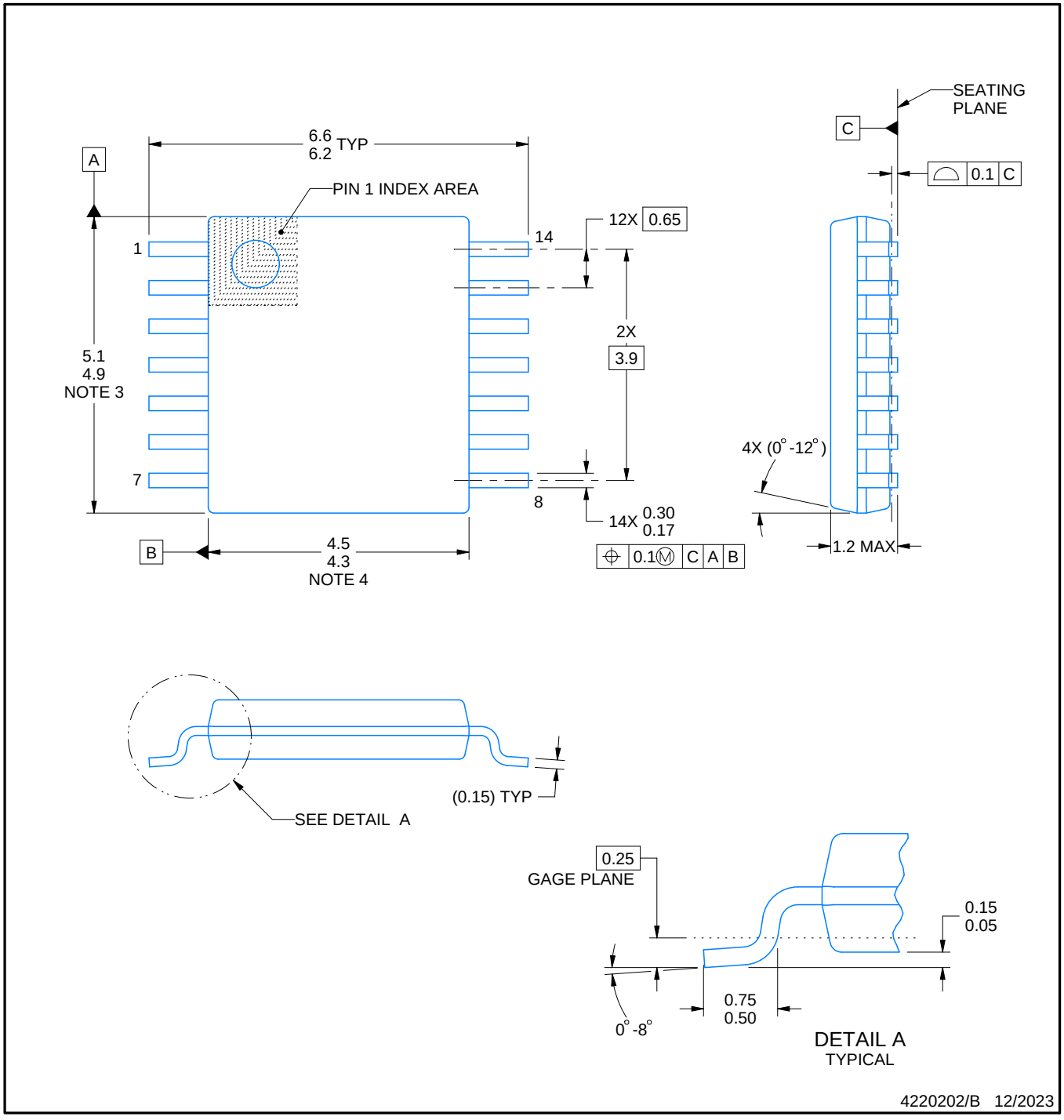
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

PW0014A

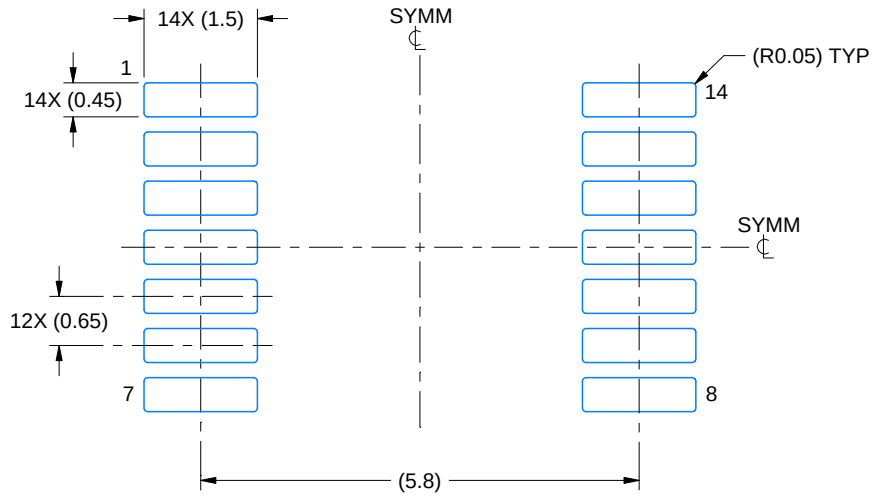
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

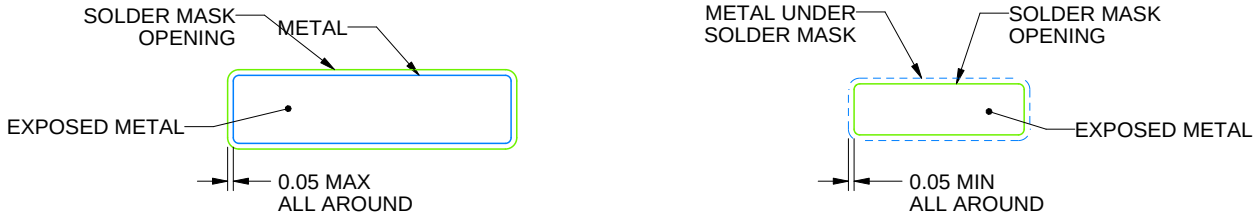


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

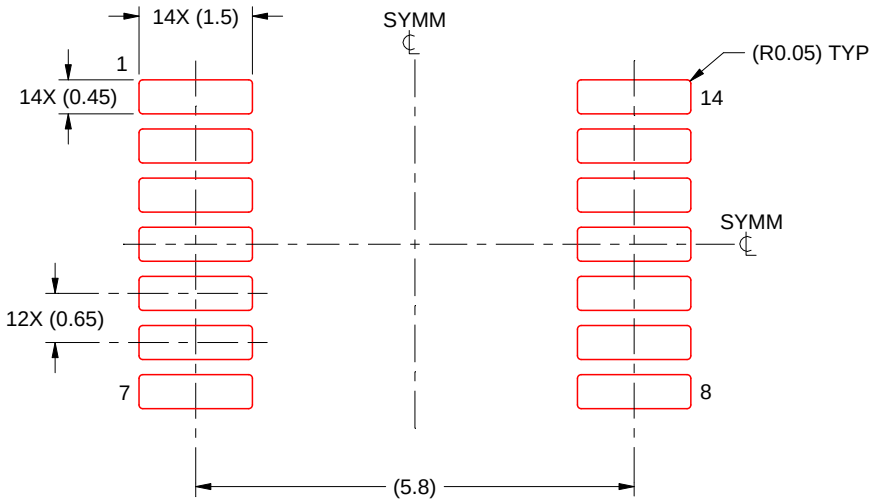


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

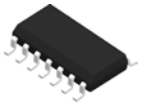


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

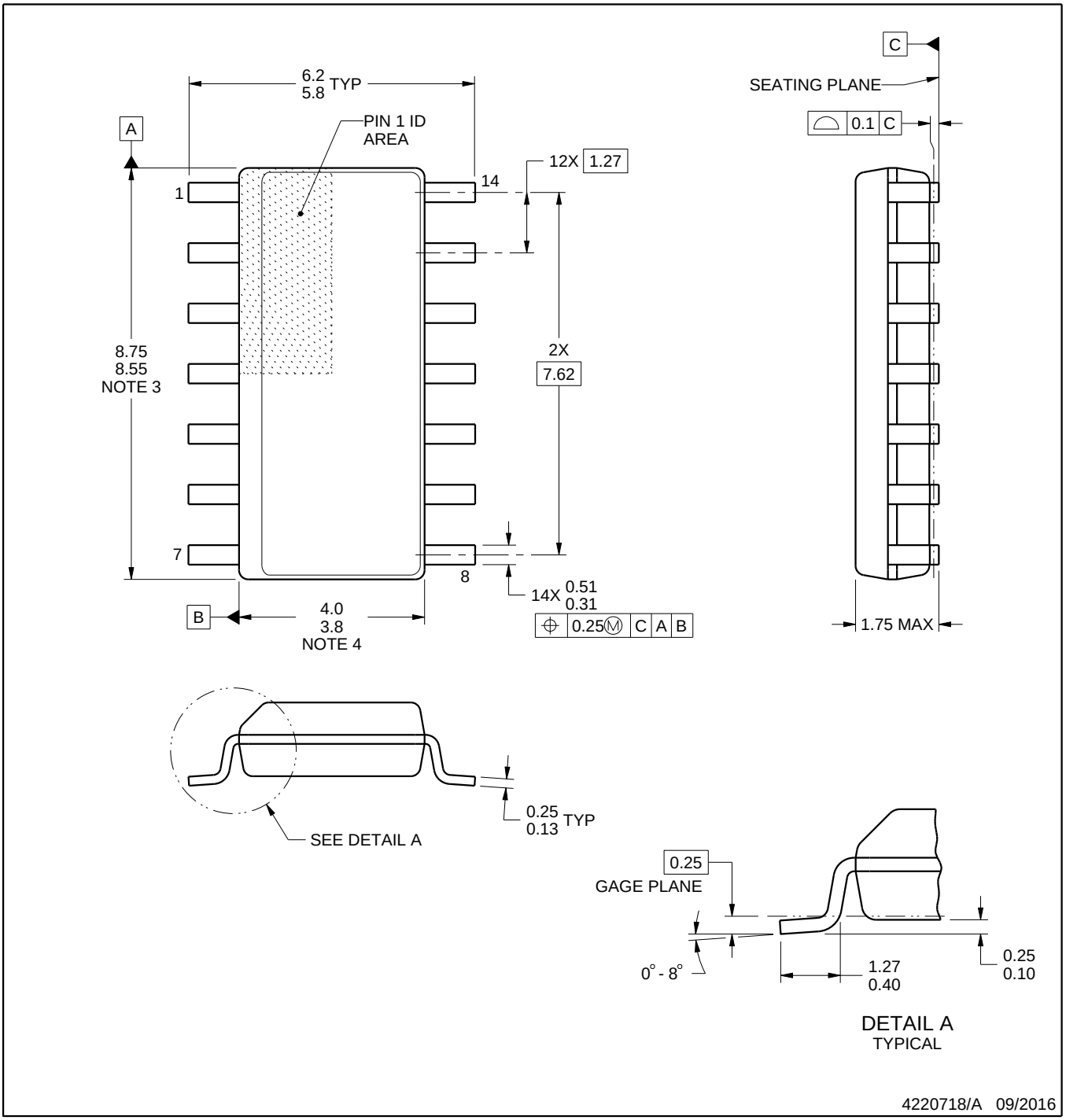


PACKAGE OUTLINE

D0014A

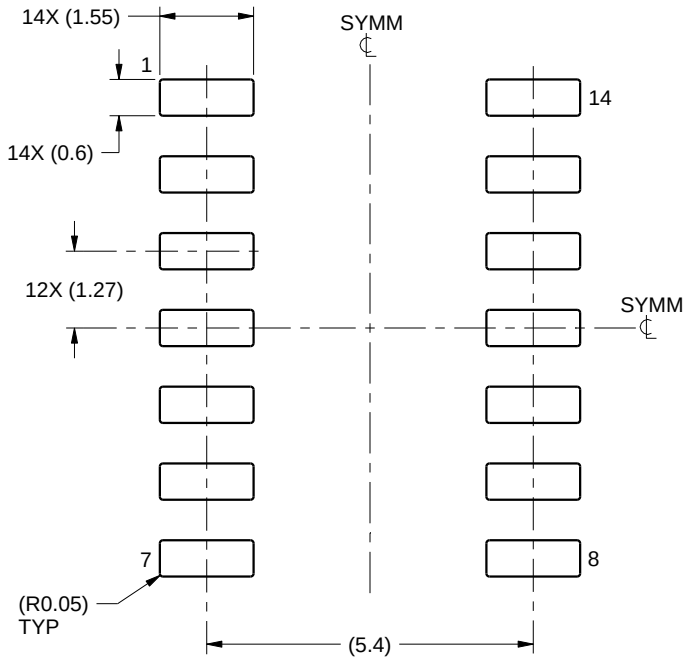
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

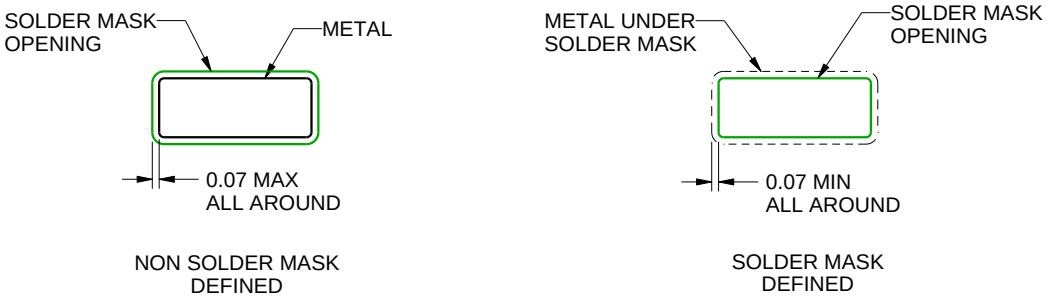


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

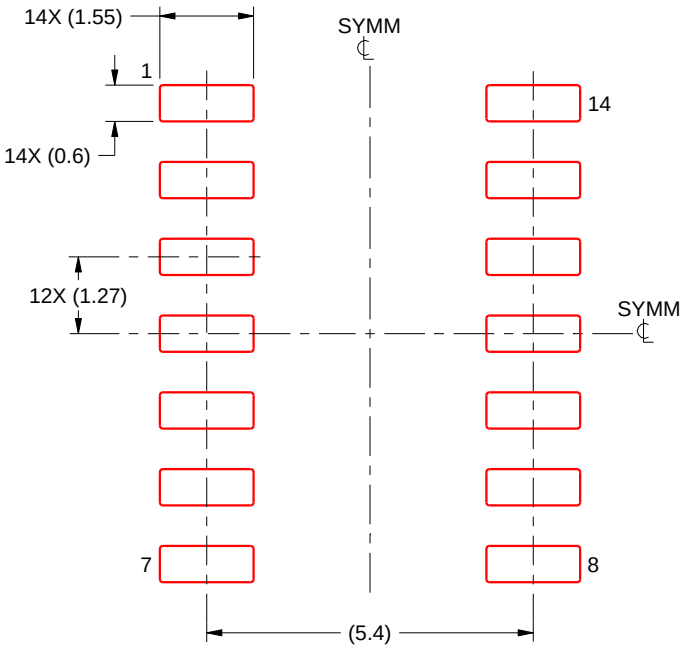
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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