LMX243x PLLatinum™ Dual High-Frequency Synthesizer for RF Personal Communications

1 Features

- Low Current Consumption
  - LMX2430 (RF/IF): 2.8 mA/ 1.4 mA
  - LMX2433 (RF/IF): 3.2 mA/ 2 mA
  - LMX2434 (RF/IF): 4.6 mA/ 2.4 mA
- 2.25-V to 2.75-V Operation
- Synchronous/Asynchronous Power Down
- Multiple PLL Options:
  - LMX2430 (RF/IF): 3 GHz /0.8 GHz
  - LMX2433 (RF/IF): 3.6 GHz /1.7 GHz
  - LMX2434 (RF/IF): 5 GHz /2.5 GHz
- Programmable Charge-Pump Current Levels
  - RF and IF: 1 or 4 mA
- Fastlock With Integrated Time-Out Counters
- Digital Filtered Lock-Detect Output
- Analog Lock Detect (Push-Pull / Open-Drain)
- 1.8-V MICROWIRE Logic Interface

2 Applications

- Mobile Handsets
- Cordless Handsets
- Wireless Data
- Cable TV Tuners

3 Description

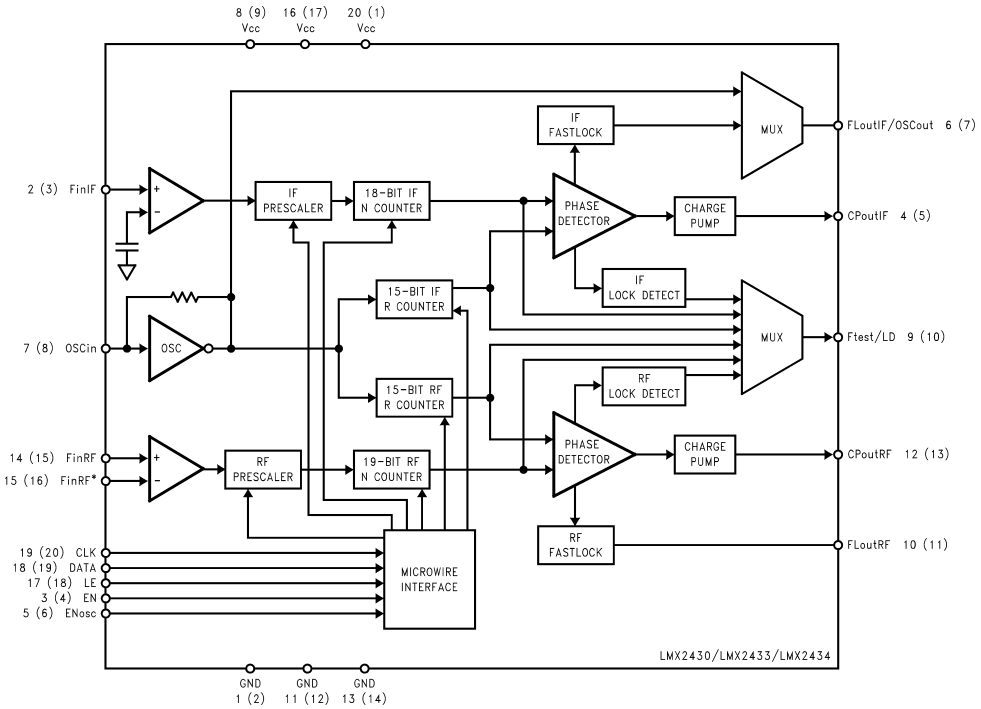
Using a proprietary digital-phase, locked-loop technique, the LMX243x devices generate very stable, low-noise control signals for RF and IF voltage controlled oscillators. Both the RF and IF synthesizers include a two-level programmable charge pump. Both the RF and IF PLLs have dedicated fastlock circuitry with integrated time-out counters which require only a single word write to power up or change frequencies.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMX243x	ULGA (20)	3.50 mm × 3.50 mm
	TSSOP (20)	6.50 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Block Diagram



NOTE: 1 (2) refers to Pin 1 of the 20-Pin ULGA and Pin 2 of the 20-Pin TSSOP

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (March 2013) to Revision D — **Page**

- Shortened data sheet title *LMX243x PLLatinum™ Dual High-Frequency Synthesizer for RF Personal Communications LMX2430 3 GHz/0.8 GHz, LMX2433 3.6 GHz/1.7 GHz, LMX2434 5 GHz/2.5 GHz* to *LMX243x PLLatinum™ Dual High-Frequency Synthesizer for RF Personal Communications* because the extra information is also listed in *Features* ... 1
- Added *Device Information* table, *Pin Configuration and Functions* section, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision B (March 2013) to Revision C — **Page**

- Changed layout of National Data Sheet to TI format ... 40

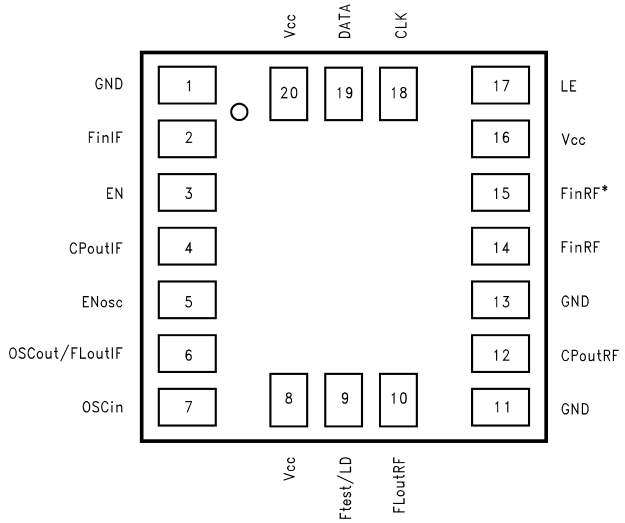
5 Description continued

The LMX243x devices are high-performance frequency synthesizers with integrated dual-modulus prescalers. A 32/33 or a 16/17 prescale ratio can be selected for the 5-GHz LMX2434 RF synthesizer. An 8/9 or a 16/17 prescale ratio can be selected for both the LMX2430 and LMX2433 RF synthesizers. The IF circuitry contains an 8/9 or a 16/17 prescaler.

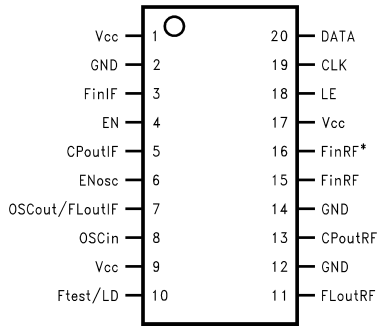
Serial data is transferred to the devices through a three-wire interface (DATA, LE, CLK). A low voltage logic interface allows direct connection to 1.8-V devices. Supply voltages from 2.25 V to 2.75 V are supported.

6 Pin Configuration and Functions

NPE Package
20-Pin ULGA Ultra Thin Chip Scale
Top View



PW Package
20-Pin TSSOP Thin Shrink Small Outline
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	ULGA	TSSOP		
CLK	18	19	I	MICROWIRE Clock input. High-impedance CMOS input. DATA is clocked into the 24-bit shift register on the rising edge of CLK.
CPoutIF	4	5	O	IF PLL charge-pump output. The output is connected to the external loop filter, which drives the input of the IF VCO.
CPoutRF	12	13	O	RF PLL charge-pump output. The output is connected to the external loop filter, which drives the input of the RF VCO.
DATA	19	20	I	MICROWIRE Data input. High-impedance CMOS input. Binary serial data. The MSB of DATA is shifted in first. The two last bits are the control bits.
EN	3	4	I	Chip Enable input. High-Impedance CMOS input. When this pin is set HIGH, the RF and IF PLLs are powered up. Power down is then controlled through the MICROWIRE. When this pin is set LOW, the device is asynchronously powered down, and the charge-pump output is forced to a high-impedance state (tri-state).
ENosc	5	6	I	Oscillator Enable input. High-impedance CMOS input. When this pin is set HIGH, the oscillator buffer is always powered up, independent of the state of the EN pin. When this pin is set LOW, the OSCout/ FLoutIF pin functions as an IF fastlock output, which connects a resistor in parallel to R2 of the external loop filter.
FinIF	2	3	I	IF PLL prescaler input. Small signal input from the VCO.
FLoutRF	10	11	O	RF PLL fastlock output. This pin connects a resistor in parallel to R2 of the external loop filter. This pin can also function as a general-purpose CMOS tri-state output.
FinRF	14	15	I	RF PLL prescaler input. Small-signal input from the VCO.
FinRF*	15	16	I	RF PLL prescaler complementary input. For single-ended operation, this pin must be AC grounded through a 100-pF capacitor. The LMX243x can be driven differentially when the AC-coupled capacitor is omitted.

Pin Functions (continued)

PIN			I/O	DESCRIPTION
NAME	ULGA	TSSOP		
Ftest/LD	9	10	O	Programmable multiplexed output. Functions as a general-purpose CMOS tri-state output, N and R divider output, RF/ IF PLL push-pull analog lock-detect output, RF/ IF PLL open-drain analog lock-detect output, or RF/ IF PLL digital filtered lock-detect output.
GND	1	2	—	Ground for the IF PLL analog and digital circuits, MICROWIRE, Ftest/LD and oscillator circuits.
	11	12		
	13	14		
LE	17	18	I	MICROWIRE Latch Enable input. High-impedance CMOS input. When LE transitions HIGH, DATA stored in the shift register is loaded into one of 6 internal control registers.
OSCout/ FLoutIF	6	7	O	Oscillator output/ IF PLL fastlock output. The output configuration is dependent on the state of the ENosc pin. When ENosc is set LOW, the pin functions as an IF fastlock output, which connects a resistor in parallel to R2 of the external loop filter. This configuration also functions as a general-purpose CMOS tri-state output. When ENosc is set HIGH, the pin functions as an oscillator output so that an external crystal can be used.
OSCin	7	8	I	Reference oscillator input. The input has an approximate Vcc/2 threshold and is driven by an external AC-coupled source.
Vcc	16	17	—	Power supply bias for the RF PLL analog circuits. Vcc may range from 2.25 V to 2.75 V. Bypass capacitors must be placed as close as possible to this pin and be connected directly to the ground plane.
	8	9		
	20	1		

7 Specifications

7.1 Absolute Maximum Ratings

See (1)(2)(3)(4)

		MIN	MAX	UNIT
	Power supply voltage V_{CC} to GND	−0.3	3.25	V
V_I	Voltage on any pin to GND V_I must be < +3.25 V	−0.3	V_{CC} + 0.3	V
T_L	Lead temperature (solder 4 seconds)		260	°C
T_{stg}	Storage temperature	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) This device is a high-performance RF integrated circuit with an ESD rating < 2000 V and is ESD-sensitive. Handling and assembly of this device must be done at ESD-protected work stations.
(3) GND = 0 V.
(4) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/Distributors for availability and specifications.

7.2 Recommended Operating Conditions

	MIN	MAX	UNIT
Power supply voltage Vcc to GND	2.25	2.75	V
Operating temperature, T_A	−40	85	°C

7.3 Thermal Information

THERMAL METRIC(1)		LMX243x		UNIT
		NPE (ULGA)	PW (TSSOP)	
		20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	80.9	111.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	22.5	44.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40	63.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	6.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	40	62.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.4 Electrical Characteristics

V_{CC} = EN = 2.5 V, −40°C ≤ T_A ≤ +85°C, unless otherwise specified

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC} PARAMETERS							
I_{CCRF}	Power supply current, RF synthesizer	LMX2430	CLK, DATA and LE = 0 V OSCin = GND RF_PD Bit = 0 IF_PD Bit = 1 RF_P Bit = 0		2.8	3.6	mA
		LMX2433			3.2	4.4	mA
		LMX2434			4.6	6.2	mA
I_{CCIF}	Power supply current, IF synthesizer	LMX2430	CLK, DATA and LE = 0 V OSCin = GND RF_PD Bit = 1 IF_PD Bit = 0 IF_P Bit = 0		1.4	2	mA
		LMX2433			2	2.8	mA
		LMX2434			2.4	3.5	mA
I_{CCPD}	Power-down current		EN, ENosc, CLK, DATA and LE = 0 V			10	µA
RF SYNTHESIZER PARAMETERS							
f_{FinRF}	RF operating frequency	LMX2430	RF_P Bit = 0	250		2500	MHz
			RF_P Bit = 1	250		3000	MHz
		LMX2433	RF_P Bit = 0	500		3000	MHz
			RF_P Bit = 1	500		3600	MHz
		LMX2434	RF_P Bit = 0 or 1	1000		5000	MHz
N_{RF}	N divider range		P = 8 / 9(1)	24		262,151	
			P = 16 / 17(1)	48		524,287	
			P = 32 / 33(1)	96		524,287	
R_{RF}	RF R divider range			3		32,767	
f_{COMPRF}	RF phase detector frequency					10	MHz
p_{FinRF}	RF input sensitivity		LMX2430 / 33 2.25 V ≤ V_{CC} ≤ 2.75 V(2)	−15		0	dBm
			LMX2434 2.35 V ≤ V_{CC} ≤ 2.75 V(2)	−12		0	dBm
$I_{CPoutRF}$ Source	RF charge-pump output source current		$V_{CPoutRF}$ = V_{CC} / 2 RF_CPG Bit = 0(3)		–1		mA
			$V_{CPoutRF}$ = V_{CC} / 2 RF_CPG Bit = 1(3)		–4		mA
$I_{CPoutRF}$ Sink	RF charge-pump output sink current		$V_{CPoutRF}$ = V_{CC} / 2 RF_CPG Bit = 0(3)		1		mA
			$V_{CPoutRF}$ = V_{CC} / 2 RF_CPG Bit = 1(3)		4		mA

(1) Some of the values in this range are illegal divide ratios (B < A). To obtain continuous legal division, the Minimum Divide Ratio must be calculated. Use N ≥ P * (P−1), where P is the value of the prescaler selected.
(2) Refer to *LMX243x FinRF Sensitivity Test Set-Up*.
(3) Refer to *LMX243x Charge Pump Test Set-Up*.

Electrical Characteristics (continued)

V_{CC} = EN = 2.5 V, −40°C ≤ T_A ≤ +85°C, unless otherwise specified

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CPoutRF\ TRI}$	RF charge-pump output tri-state current		0.5 V ≤ $V_{CPoutRF}$ ≤ V_{CC} – 0.5 V (3)	–2.5		2.5	nA
$I_{CPoutRF\ \%MIS}$	RF charge-pump output sink current vs charge-pump output source current mismatch		$V_{CPoutRF}$ = V_{CC} / 2 (4)		3%	10%	
$I_{CPoutRF\ \%V_{CPoutRF}}$	RF charge-pump output current magnitude variation vs charge-pump output voltage		0.5 V ≤ $V_{CPoutRF}$ ≤ V_{CC} – 0.5 V (4)		5%	15%	
$I_{CPoutRF\ \%T_A}$	RF charge-pump output current magnitude variation vs temperature		$V_{CPoutRF}$ = V_{CC} / 2 (4)		2%		
IF SYNTHESIZER PARAMETERS							
f_{FinIF}	IF operating frequency	LMX2430	IF_P Bit = 0 or 1	100		800	MHz
		LMX2433	IF_P Bit = 0 or 1	250		1700	MHz
		LMX2434	IF_P Bit = 0 or 1	500		2500	MHz
N_{IF}	IF N divider range		P = 8/9 (1)	24		131,079	
			P = 16/17 (1)	48		262,143	
R_{IF}	IF R divider range			3		32,767	
f_{COMPIF}	IF phase detector frequency					10	MHz
p_{FinIF}	IF input sensitivity		2.25 V ≤ V_{CC} ≤ 2.75 V (2)	–15		0	dBm
$I_{CPoutIF}$ Source	IF charge-pump output source current		$V_{CPoutIF}$ = V_{CC}/2 IF_CPG Bit = 0 (3)		–1		mA
			$V_{CPoutIF}$ = V_{CC}/2 IF_CPG Bit = 1 (3)		–4		mA
$I_{CPoutIF}$ Sink	IF charge-pump output sink current		$V_{CPoutIF}$ = V_{CC}/2 IF_CPG Bit = 0 (3)		1		mA
			$V_{CPoutIF}$ = V_{CC}/2 IF_CPG Bit = 1 (3)		4		mA
$I_{CPoutIF\ TRI}$	IF charge-pump output tri-state current		0.5 V ≤ $V_{CPoutIF}$ ≤ V_{CC} – 0.5 V (3)	–2.5		2.5	nA
$I_{CPoutIF\ \%MIS}$	IF charge-pump output sink current vs charge-pump output source current mismatch		$V_{CPoutIF}$ = V_{CC}/2 (4)		3%	10%	
$I_{CPoutIF\ \%V_{CPoutIF}}$	IF charge-pump output current magnitude variation vs charge-pump output voltage		0.5 V ≤ $V_{CPoutIF}$ ≤ V_{CC} – 0.5 V (4)		5%	15%	
$I_{CPoutIF\ \%T_A}$	IF charge-pump output current magnitude variation vs temperature		$V_{CPoutIF}$ = V_{CC}/2 (4)		2%		
OSCILLATOR PARAMETERS							
f_{OSCin}	Oscillator operating frequency			1		256	MHz
v_{OSCin}	Oscillator sensitivity		See (5)	0.5		V_{CC}	V_{PP}
I_{OSCin}	Oscillator input current		V_{OSCin} = V_{CC}			100	µA
			V_{OSCin} = 0 V	–100			µA
DIGITAL INTERFACE (DATA, CLK, LE, EN, ENosc, Ftest/LD, FLoutRF, OSCout/ FLoutIF)							
V_{IH}	High-level input voltage			1.6			V
V_{IL}	Low-level input voltage					0.4	V
I_{IH}	High-level input current		V_{IH} = V_{CC}			1	µA
I_{IL}	Low-level input current		V_{IL} = 0 V	−1			µA
V_{OH}	High-level output voltage		I_{OH} = −500 µA	V_{CC} − 0.4			V
V_{OL}	Low-level output voltage		I_{OL} = 500 µA			0.4	V

(4) Refer to *Charge Pump Current Specification Definitions* for details on how these measurements are made.
(5) Refer to *LMX243x OSCin Sensitivity Test Set-Up*.

Electrical Characteristics (continued)

V_{CC} = EN = 2.5 V, −40°C ≤ T_A ≤ +85°C, unless otherwise specified

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
PHASE NOISE CHARACTERISTICS							
$L_{NRF}(f)$	RF synthesizer normalized phase noise contribution(6)		TCXO Reference Source RF_CPG Bit = 1 IF_PD Bit = 1		–219		dBc/Hz
$L_{NIF}(f)$	IF synthesizer normalized phase noise contribution(6)		TCXO Reference Source IF_CPG Bit = 1 RF_PD Bit = 1		–214		dBc/Hz
$L_{RF}(f)$	RF synthesizer single-side band phase noise measured	LMX2430	f_{FinRF} = 2750 MHz f = 10-kHz offset f_{COMPRF} = 1 MHz Loop Bandwidth = 100 kHz N_{RF} = 2750 f_{OSCin} = 10 MHz v_{OSCin} = 1 V_{PP} RF_CPG Bit = 1 IF_PD Bit = 1 T_A = 25°C(7)		–90.3		dBc/Hz
		LMX2433	f_{FinRF} = 3200 MHz f = 10-kHz offset f_{COMPRF} = 1 MHz Loop Bandwidth = 100 kHz N_{RF} = 3200 f_{OSCin} = 10 MHz v_{OSCin} = 1 V_{PP} RF_CPG Bit = 1 IF_PD Bit = 1 T_A = 25°C(7)		–88.9		dBc/Hz
		LMX2434	f_{FinRF} = 4700 MHz f = 10-kHz offset f_{COMPRF} = 1 MHz Loop Bandwidth = 100 kHz N_{RF} = 4700 f_{OSCin} = 10 MHz v_{OSCin} = 1 V_{PP} RF_CPG Bit = 1 IF_PD Bit = 1 T_A = 25°C(7)		–85.6		dBc/Hz

(6) Normalized Phase Noise Contribution is defined as $L_N(f) = L(f) - 20 \log (N) - 10 \log (f_{COMP})$, where L(f) is defined as the single side band phase noise measured at an offset frequency, f, in a 1-Hz bandwidth. The offset frequency, f, must be chosen sufficiently smaller than the loop bandwidth of the PLL, yet large enough to avoid substantial phase noise contribution from the reference source. N is the value selected for the feedback divider and f_{COMP} is the RF/IF phase and frequency detector comparison frequency.
(7) The synthesizer phase noise is measured with the LMX2430PW/LMX2430NPE evaluation boards and the HP8566B Spectrum Analyzer.

7.5 Timing Requirements

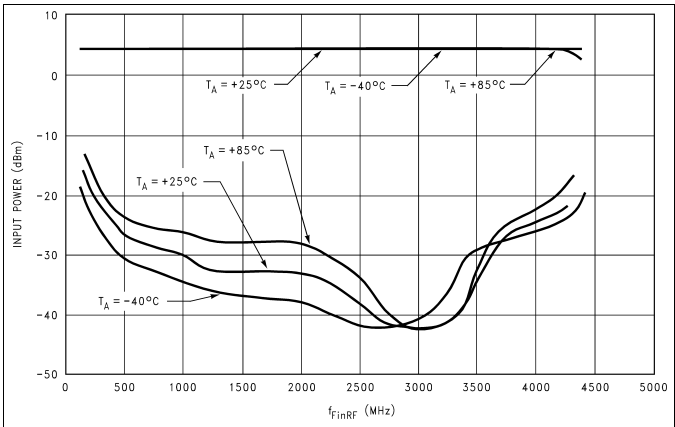
See (1)

		MIN	NOM	MAX	UNIT
MICROWIRE INTERFACE					
t_{CS}	DATA to CLK set-up time	50			ns
t_{CH}	DATA to CLK hold time	10			ns
t_{CWH}	CLK pulse width HIGH	50			ns
t_{CWL}	CLK pulse width LOW	50			ns
t_{ES}	CLK to LE set-up time	50			ns
t_{EW}	LE pulse width	50			ns

(1) Refer to *LMX243x Serial Data Input Timing* figure.

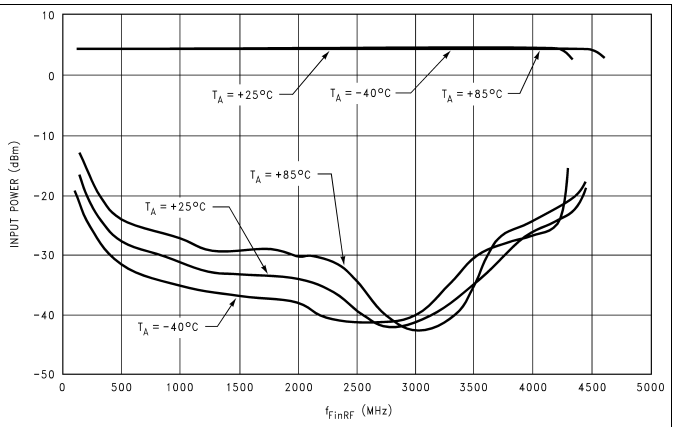
7.6 Typical Characteristics

7.6.1 Sensitivity



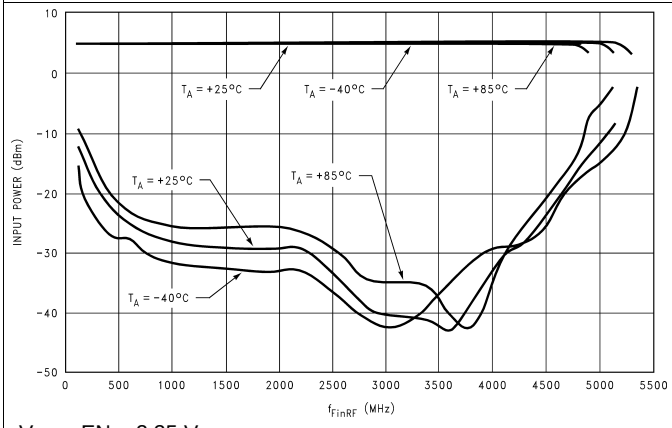
V_{CC} = EN = 2.25 V

Figure 1. LMX2430 FinRF Input Power vs Frequency



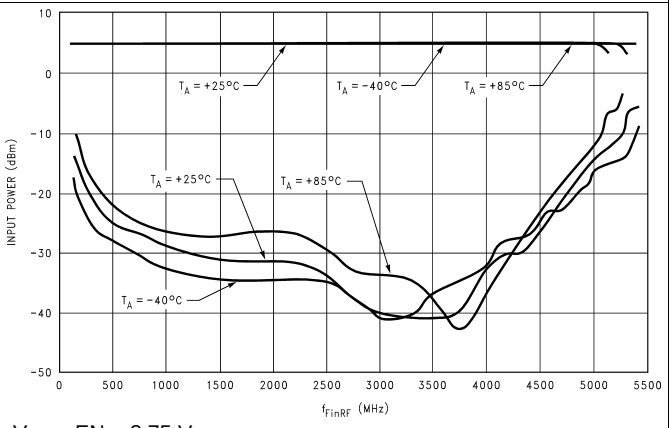
V_{CC} = EN = 2.75 V

Figure 2. LMX2430 FinRF Input Power vs Frequency



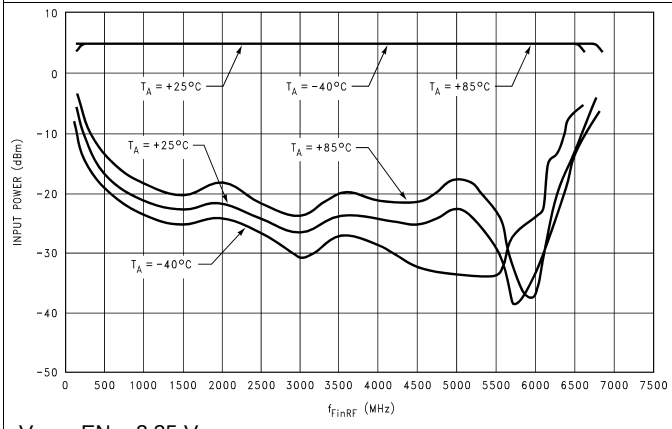
V_{CC} = EN = 2.25 V

Figure 3. LMX2433 FinRF Input Power vs Frequency



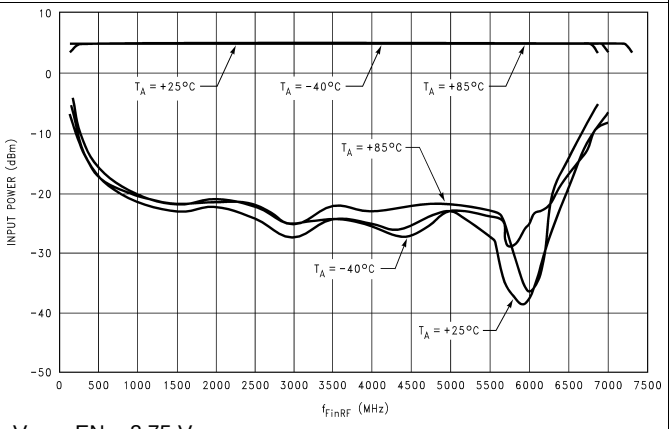
V_{CC} = EN = 2.75 V

Figure 4. LMX2433 FinRF Input Power vs Frequency



V_{CC} = EN = 2.35 V

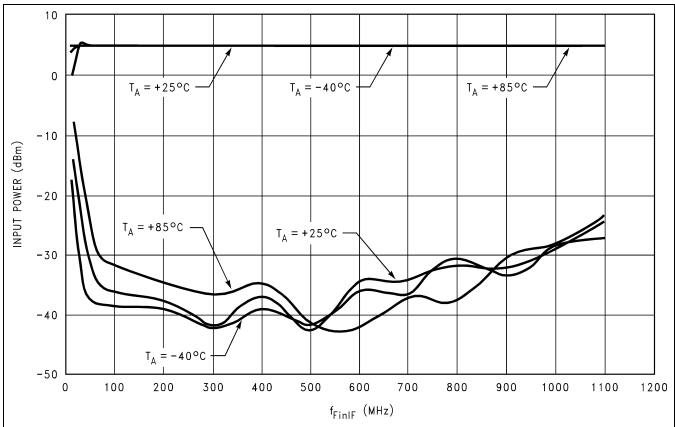
Figure 5. LMX2434 FinRF Input Power vs Frequency



V_{CC} = EN = 2.75 V

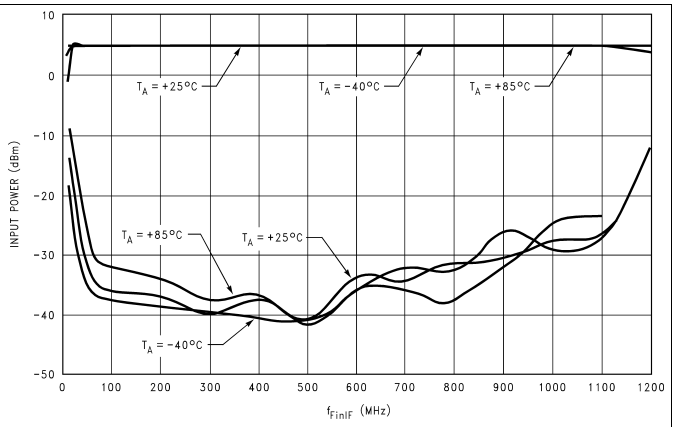
Figure 6. LMX2434 FinRF Input Power vs Frequency

Sensitivity (continued)



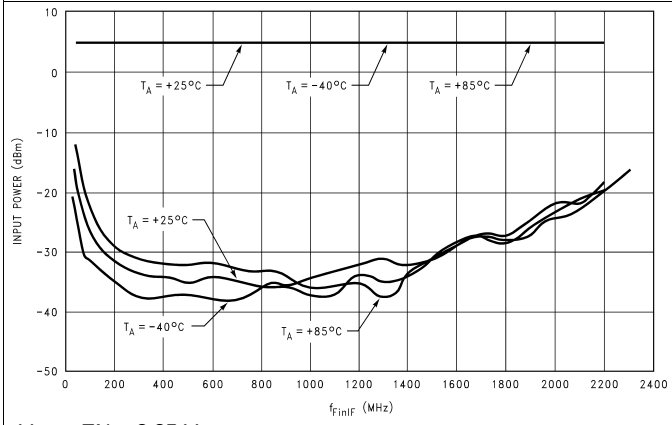
V_{CC} = EN = 2.25 V

Figure 7. LMX2430 FinIF Input Power vs Frequency



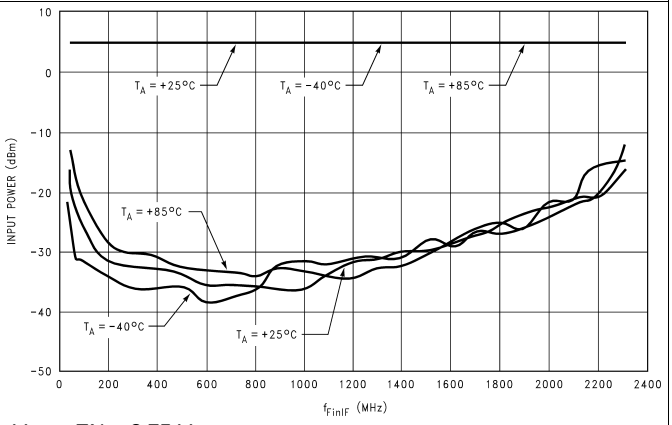
V_{CC} = EN = 2.75 V

Figure 8. LMX2430 FinIF Input Power vs Frequency



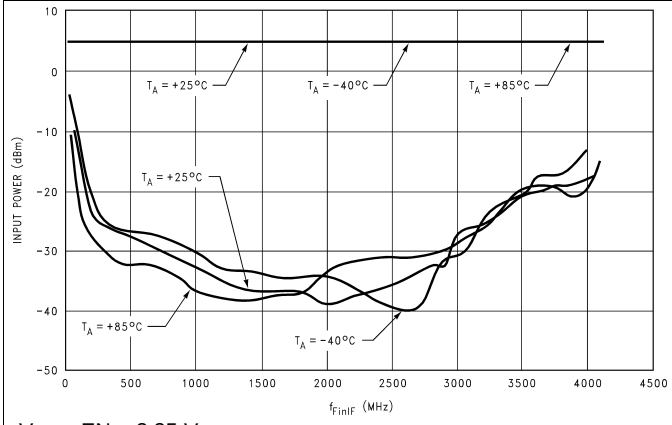
V_{CC} = EN = 2.25 V

Figure 9. LMX2433 FinIF Input Power vs Frequency



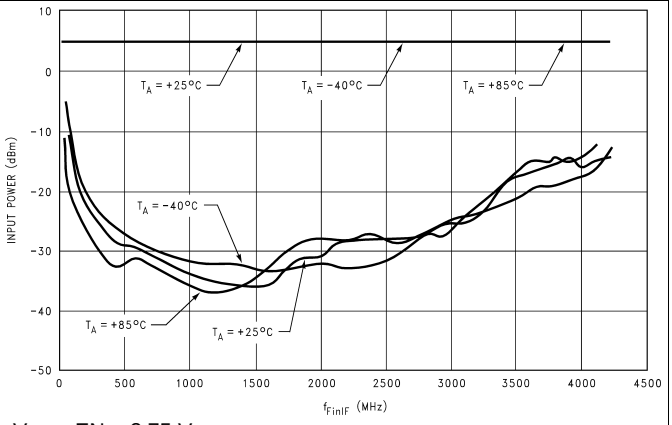
V_{CC} = EN = 2.75 V

Figure 10. LMX2433 FinIF Input Power vs Frequency



V_{CC} = EN = 2.25 V

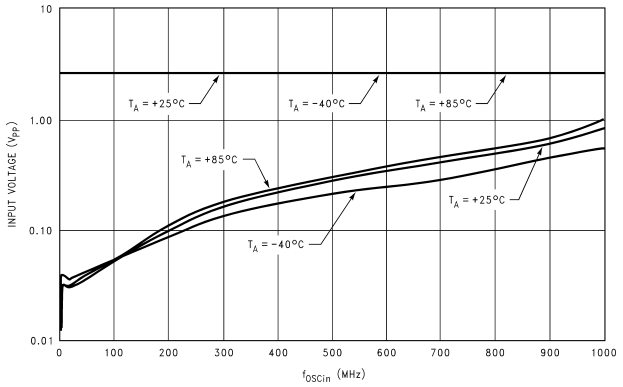
Figure 11. LMX2434 FinIF Input Power vs Frequency



V_{CC} = EN = 2.75 V

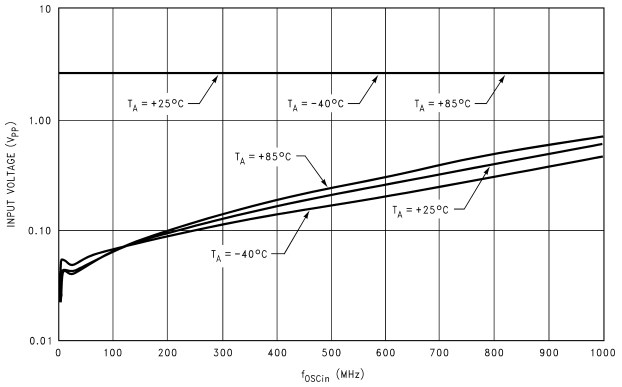
Figure 12. LMX2434 FinIF Input Power vs Frequency

Sensitivity (continued)



V_{CC} = EN = 2.25 V

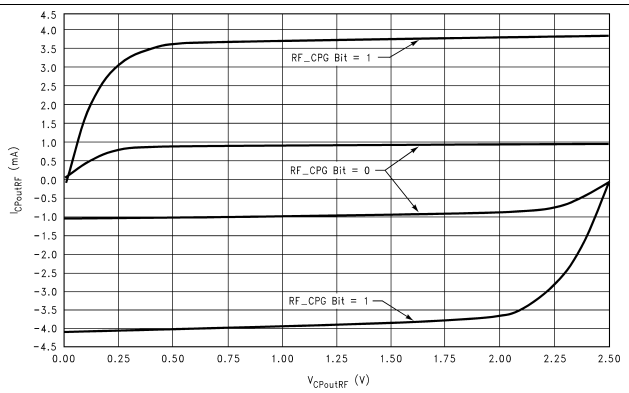
Figure 13. LMX243x OSCin Input Voltage vs Frequency



V_{CC} = EN = 2.75 V

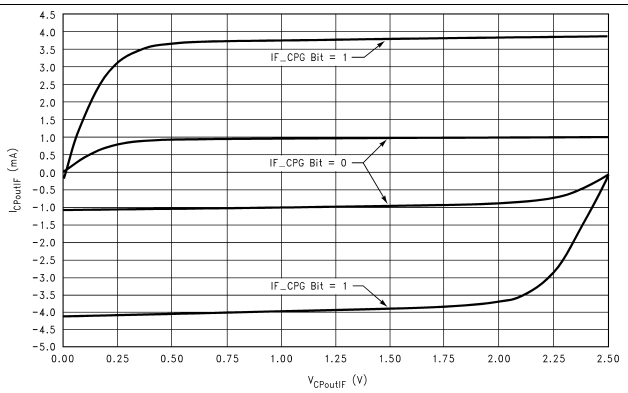
Figure 14. LMX243x OSCin Input Voltage vs Frequency

7.6.2 Charge Pump



V_{CC} = EN = 2.5 V −40°C ≤ T_A ≤ +85°C

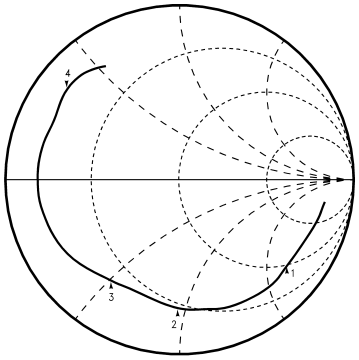
Figure 15. LMX243x RF Charge-Pump Sweeps



V_{CC} = EN = 2.5 V −40°C ≤ T_A ≤ +85°C

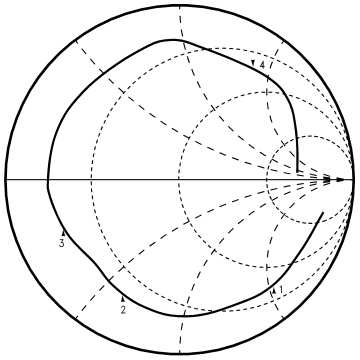
Figure 16. LMX243x IF Charge-Pump Sweeps

7.6.3 Input Impedance



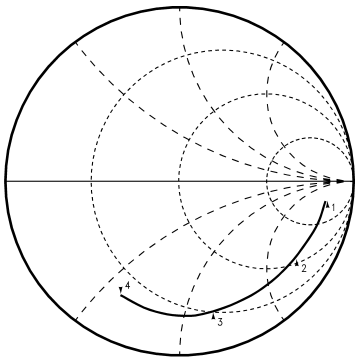
V_{CC} = EN = 2.5 V T_A = 25°C

Figure 17. LMX243x ULGA FinRF Input Impedance



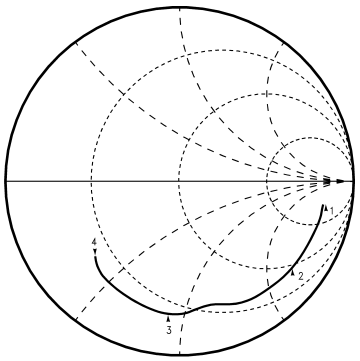
V_{CC} = EN = 2.5 V T_A = 25°C

Figure 18. LMX243x TSSOP FinRF Input Impedance



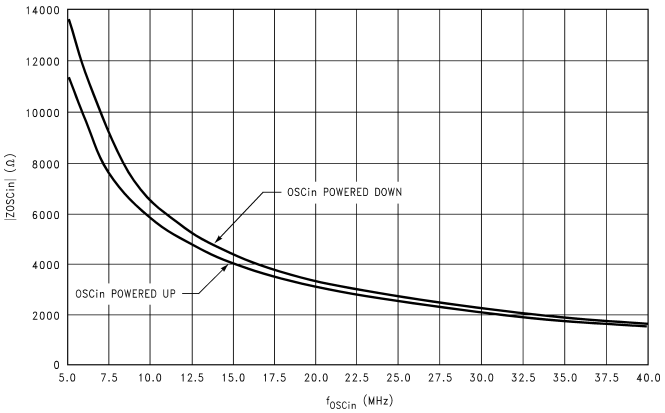
V_{CC} = EN = 2.5 V T_A = 25°C

Figure 19. LMX243x ULGA FinIF Input Impedance



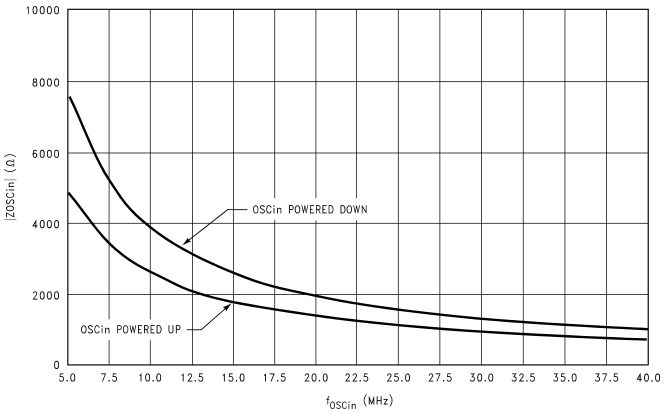
V_{CC} = EN = 2.5 V T_A = 25°C

Figure 20. LMX243x TSSOP FinIF Input Impedance



V_{CC} = EN = 2.5 V T_A = 25°C

Figure 21. LMX243x ULGA OSCin Input Impedance vs Frequency



V_{CC} = EN = 2.5 V T_A = 25°C

Figure 22. LMX233xU TSSOP OSCin Input Impedance vs Frequency

8 Parameter Measurement Information

8.1 Bench Test Setups

8.1.1 LMX243x Charge-Pump Test Setup

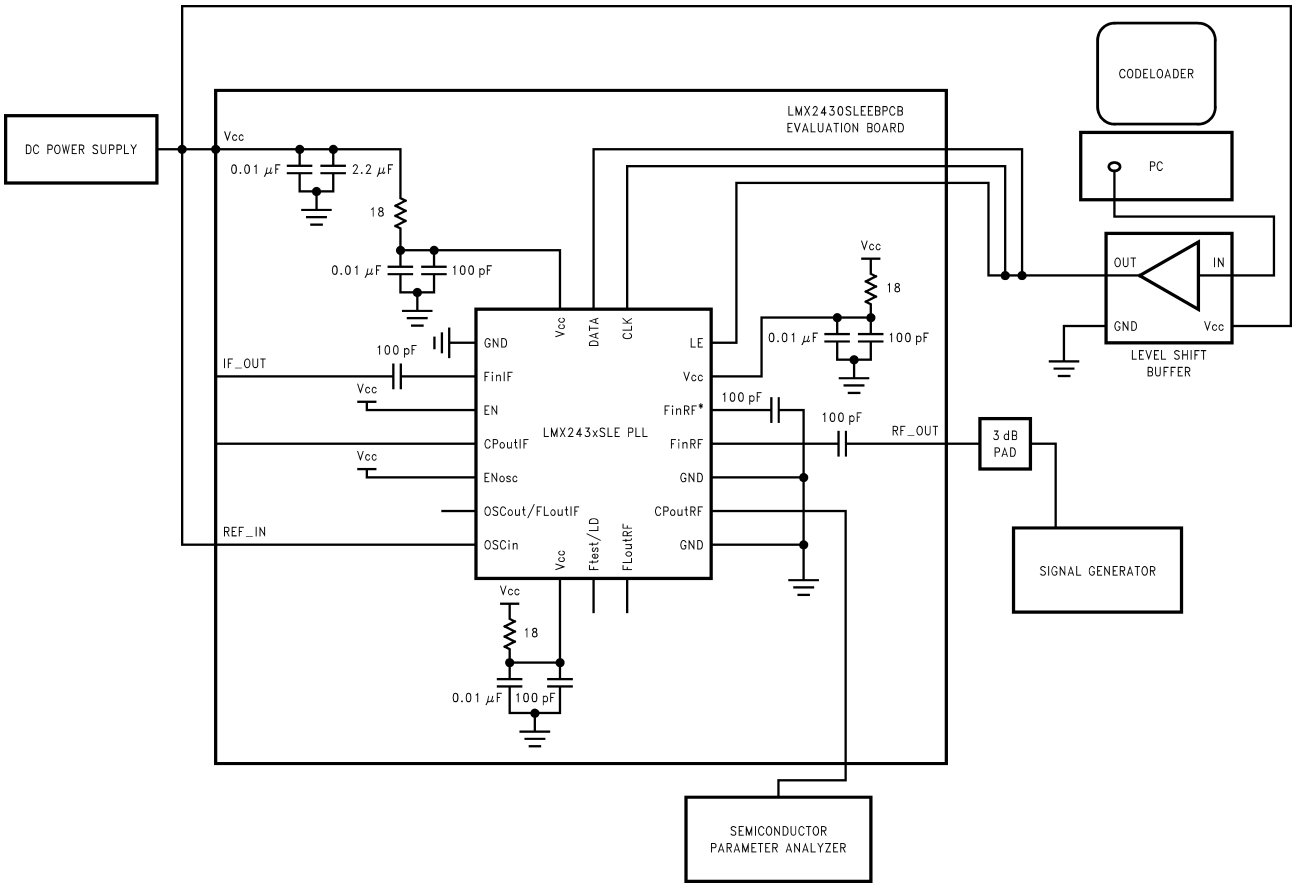


Figure 23. Charge-Pump Current Test Setup

Figure 23 shows the setup required to measure the RF charge-pump sink current of the LMX243x device. The same setup is used for the LMX2430PW evaluation board. The purpose of this test is to assess the functionality of the RF charge pump. The IF charge pump is evaluated in the same way.

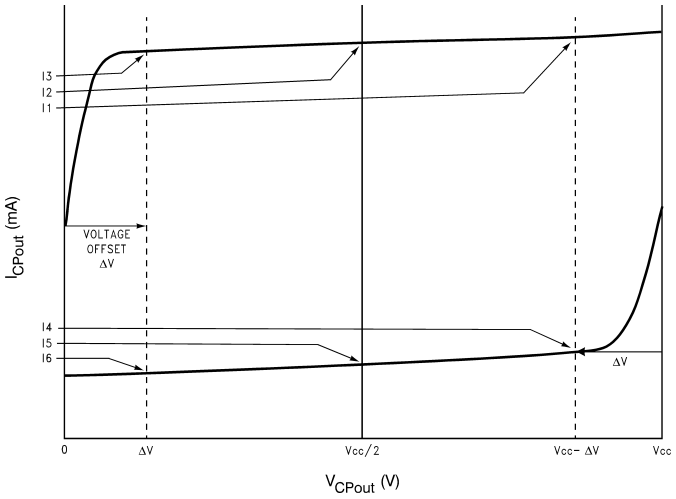
This setup uses an open-loop configuration. A power supply is connected to V_{CC}. By means of a signal generator, a 10-MHz signal is typically applied to the FinRF pin. The signal is one of two inputs to the phase / frequency detector (PFD). The 3-dB pad provides a 50-Ω match between the PLL and the signal generator. The OSCin pin is tied to Vcc. This establishes the other input to the PFD. Alternatively, this input can be tied directly to the ground plane. The EN and ENosc pins are also both tied to Vcc. A semiconductor parameter analyzer is connected to the CPoutRF pin and used to measure the sink, source, and tri-state leakage currents.

Let F_r represent the frequency of the signal applied to the OSCin pin, which is simply zero in this case (DC), and let F_p represent the frequency of the signal applied to the FinRF pin. The PFD is sensitive to the rising edges of F_r and F_p. Assuming positive VCO characteristics (RF_CPP bit = 1); the charge pump turns ON, and sinks current when the first rising edge of F_p is detected. Because F_r has no rising edge, the charge pump continues to sink current indefinitely. In order to measure the RF charge-pump source current, the RF_CPP bit is simply set to 0 (negative VCO characteristics) in CodeLoader. Similarly, in order to measure the tri-state leakage current, the RF_CPT bit is set to 1.

Bench Test Setups (continued)

The measurements are typically taken over supply voltage and temperature. The measurements are also typically taken at the HIGH and LOW charge-pump current gains. The charge-pump current gain can be controlled by the RF_CPG bit in CodeLoader. Once the charge-pump currents are determined, the (i) charge-pump output current magnitude variation versus charge-pump output voltage, (ii) charge-pump output sink current versus charge-pump output source current mismatch, and (iii) charge-pump output current magnitude versus temperature, can be calculated. Refer to the *Charge Pump Current Specifications Definition* for more details.

8.1.2 Charge-Pump Current Specification Definitions



I1 = Charge-Pump Sink Current at V_{CPout} = Vcc − ΔV
I2 = Charge-Pump Sink Current at V_{CPout} = Vcc//2
I3 = Charge-Pump Sink Current at V_{CPout} = ΔV
I4 = Charge-Pump Source Current at V_{CPout} = Vcc − ΔV
I5 = Charge-Pump Source Current at V_{CPout} = Vcc/2
I6 = Charge-Pump Source Current at V_{CPout} = ΔV
ΔV = Voltage offset from the positive and negative rails. Dependent on the VCO tuning range relative to Vcc and GND. Typical values are between 0.5V and 1.0V.
V_{CPout} refers to either $V_{CPoutRF}$ or $V_{CPoutIF}$
I_{CPout} refers to either $I_{CPoutRF}$ or $I_{CPoutIF}$

Figure 24. Charge-Pump Parameters

8.1.2.1 Charge-Pump Output Current Variation vs Charge-Pump Output Voltage

$$I_{CPout}\ Vs\ V_{CPout} = \frac{(|I1| - |I3|)}{(|I1| + |I3|)} \times 100\% = \frac{(|I4| - |I6|)}{(|I4| + |I6|)} \times 100\% \quad (1)$$

8.1.2.2 Charge-Pump Sink Current vs Charge-Pump Output Source Current Mismatch

$$I_{CPout}\ Sink\ Vs\ I_{CPout}\ Source = \frac{|I2| - |I5|}{\frac{1}{2}(|I2| + |I5|)} \times 100\% \quad (2)$$

Bench Test Setups (continued)

8.1.2.3 Charge-Pump Output Current Variation vs Temperature

$$I_{CPout}\ Vs\ T_A = \frac{\left|I_2\right|_{T_A} - \left|I_2\right|_{T_A = 25°C}}{\left|I_2\right|_{T_A = 25°C}} \times 100\%$$

$$= \frac{\left|I_5\right|_{T_A} - \left|I_5\right|_{T_A = 25°C}}{\left|I_5\right|_{T_A = 25°C}} \times 100\% \quad (3)$$

8.1.3 LMX243x FinRF Sensitivity Test Setup

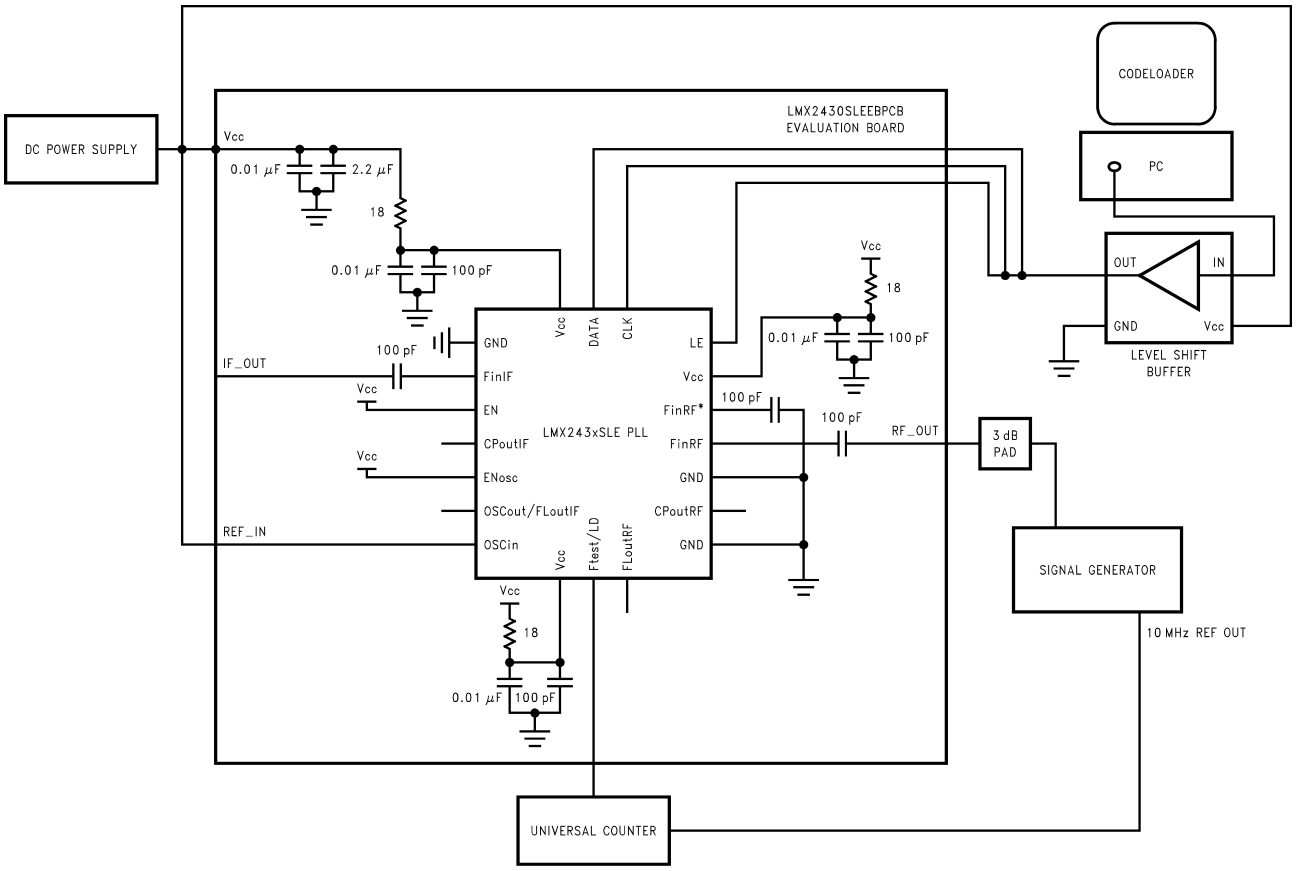


Figure 25. RF Input Sensitivity Test Setup

Figure 25 shows the setup required to measure the RF input sensitivity level of the LMX243x device. The same setup is used for the LMX2430PW evaluation board. The purpose of this test is to measure the acceptable signal level to the FinRF input of the PLL chip. Outside the acceptable signal range, the feedback divider begins to divide incorrectly and miscount the frequency. The FinIF sensitivity is evaluated in the same way.

The setup uses an open-loop configuration. A power supply is connected to Vcc. The IF PLL is powered down (IF_PD bit = 1). By means of a signal generator, an RF signal is applied to the FinRF pin. The 3-dB pad provides a 50-Ω match between the PLL and the signal generator. The EN, ENosc, and OSCin pins are all tied to V_{CC}. The N value is typically set to 10000 in CodeLoader, that is, RF_B word = 156 and RF_A word = 16 for RF_P bit = 0 (LMX2434) or RF_P bit = 1 (LMX2430 and LMX2433). The feedback divider output is routed to the Ftest/LD

Bench Test Setups (continued)

pin by selecting the RF_N/2 Frequency word (MUX[3:0] word = 15) in CodeLoader. A Universal Counter is connected to the Ftest/LD pin and used to monitor the output frequency of the feedback divider. The expected frequency must be the signal generator frequency divided by twice the corresponding counter value, that is, 20,000. The factor of two comes in because the LMX43x device has an internal /2 circuit which is used to provide a 50% duty cycle.

Sensitivity is typically measured over frequency, supply voltage and temperature. In order to perform the measurement, the temperature, frequency, and supply voltage is set to a fixed value, and the power level of the signal at FinRF is varied. Sensitivity is reached when the frequency error of the divided RF input is greater than or equal to 1 Hz. The power attenuation from the cable and the 3-dB pad must be accounted for. The feedback divider miscounts if too much or too little power is applied to the FinRF input. Therefore, the allowed input power level is bounded by the upper and lower sensitivity limits. In a typical application, if the power level to the FinRF input approaches the sensitivity limits, this can introduce spurs or cause degradation to the phase noise. When the power level gets even closer to these limits, or exceeds them, the RF PLL loses lock.

8.1.4 LMX243x OSCin Sensitivity Test Setup

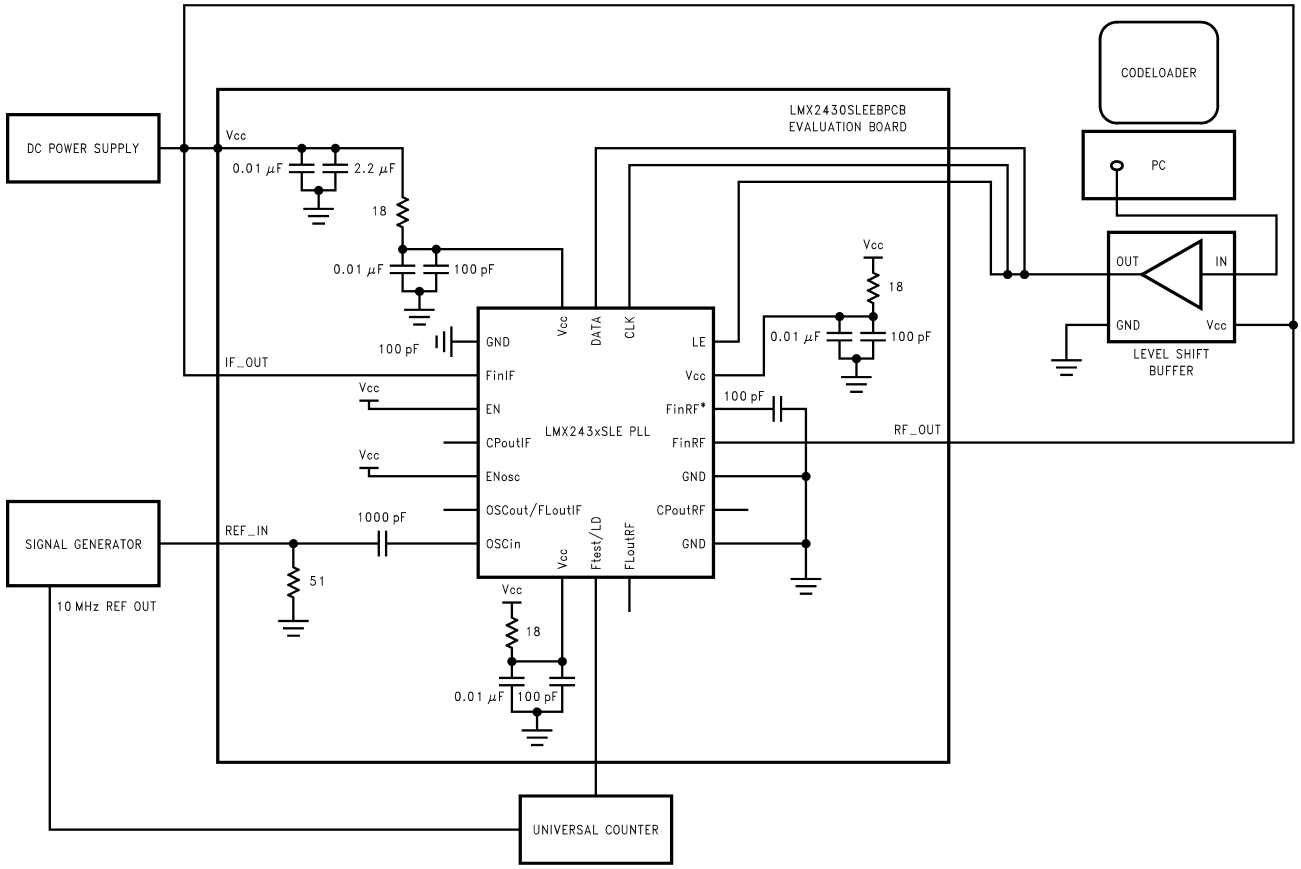


Figure 26. OSCin Sensitivity Test Setup

Figure 26 shows the setup required to measure the OSCin buffer sensitivity level in the LMX243x device. The same setup is used for the LMX2430PW evaluation board. This setup is similar to the FinRF sensitivity setup except that the signal generator is now connected to the OSCin pin, and both Fin pins are tied to V_{CC}. The 51-Ω shunt resistor matches the OSCin input to the signal generator. The R counter is typically set to 1000, that is, RF_R word = 1000 or IF_R word = 1000. The reference divider output is routed to the Ftest/LD pin by selecting

Bench Test Setups (continued)

the RF_R/ 2 frequency word (MUX[3:0] word = 14) or the IF_R/ 2 frequency word (MUX[3:0] word = 12) in CodeLoader. A universal counter is connected to the Ftest/LD pin and is used to monitor the output frequency of the reference divider. The expected frequency must be the signal generator frequency divided by twice the corresponding counter value, that is, 2000. The factor of two comes in because the LMX243x device has an internal /2 circuit which is used to provide a 50% duty cycle.

In a similar way, sensitivity is typically measured over frequency, supply voltage and temperature. In order to perform the measurement, the temperature, frequency, and supply voltage is set to a fixed value and the power level (voltage level) of the signal at OSCin is varied. Sensitivity is reached when the frequency error of the divided input signal is greater than or equal to 1 Hz.

8.1.5 LMX243x FinRF Input Impedance Test Setup

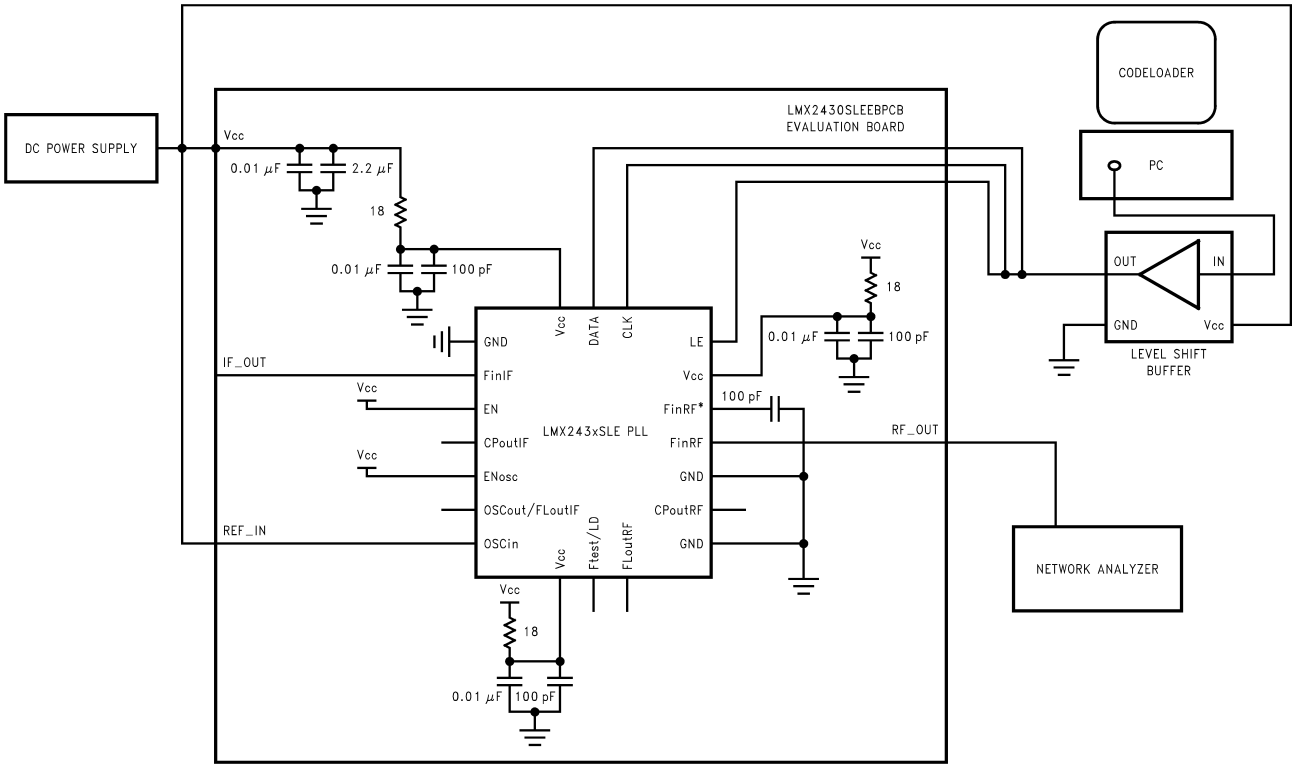
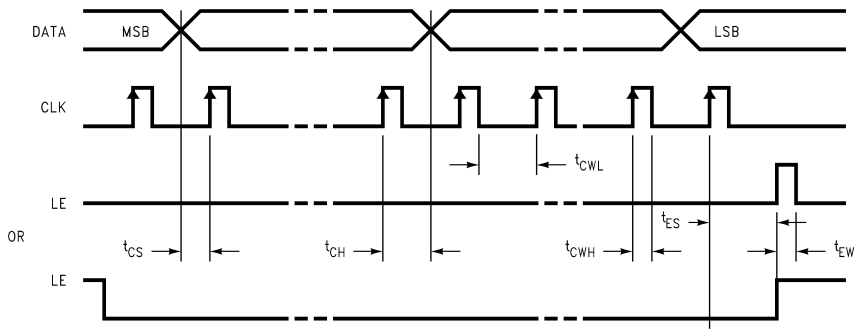


Figure 27. Imput Impedance Test Setup



Notes:
1. DATA is clocked into the 24-bit shift register on the rising edge of CLK
2. The MSB of DATA is shifted in first.

Figure 28. LMX243x Serial Data Input Timing

Bench Test Setups (continued)

Figure 28 shows the setup required to measure the RF input impedance of the LMX243x device. The same setup is used for the LMX2430PW evaluation board. Measuring the input impedance of the device facilitates the design of appropriate matching networks to match the PLL to the VCO, or in more critical situations, to the characteristic impedance of the printed-circuit-board (PCB) trace, to prevent undesired transmission line effects. The FinIF input impedance is evaluated in the same way.

Before the actual measurements are taken, the network analyzer must be calibrated, that is, the error coefficients must be calculated. The calibration standard of the network analyzer is used to calculate these coefficients. The calibration standard includes an open, short and a matched load. A 1-port calibration is implemented here.

To calculate the coefficients, the PLL chip is first removed from the PCB. A piece of semi-rigid coaxial cable is then soldered to the pad on the PCB which is equivalent to the FinRF pin on the PLL chip. Proper grounding near the exposed tip of the semi-rigid coaxial cable is required for accurate results. The DC blocking capacitor is removed for this test. The network analyzer port is then connected to the other end of the semi-rigid coaxial cable. In this way, the semi-rigid coaxial cable acts as a transmission line. This transmission line adds electrical length and produces an offset from the reference plane of the network analyzer; therefore, it must be included in the calibration. The desired operating frequency is then set. The typical frequency range selected for the RF synthesizer of the LMX243x device is from 100 MHz to 6000 MHz.

The network analyzer calculates the calibration coefficients based on the measured S_{11} parameters. With this all done, calibration is now complete.

The PLL chip is then placed on the PCB, and a power supply connected to V_{CC}. The EN, ENosc, and OSCin pins are all tied to V_{CC}. Alternatively, the OSCin pin can be tied to ground. In this setup, the complementary input (FinRF*) is AC-coupled to ground. With the network analyzer still connected to the semi-rigid coaxial cable, the measured FinRF impedance is displayed.

The OSCin input impedance is measured in the same way. The impedance is measured when the oscillator buffer is powered up (ENosc is set HIGH) and when the oscillator buffer is powered down (ENosc pin is set LOW).

Table 1. LMX243x ULGA FinRF Input Impedance Table(1)

f_{FinRF} (MHz)	|Γ|	ANGLE (Γ) (°)	Re {ZFinRF} (Ω)	Im {ZFinRF} (Ω)	|ZFinRF| (Ω)
100	0.86	–8.63	334.27	–339.55	476.48
200	0.86	–10.72	265.44	–313.48	410.77
300	0.85	–13.48	202.09	–281.42	346.46
400	0.84	–17.01	150.76	–245.31	287.93
500	0.83	–21.05	112.18	–212.85	240.60
600	0.82	–25.32	85.96	–185.41	204.37
700	0.82	–29.78	67.32	–162.49	175.88
800	0.81	–34.35	54.27	–143.15	153.09
900	0.80	–39.02	44.76	–127.07	134.72
1000	0.80	–43.83	37.32	–113.62	119.59
1100	0.79	–48.76	31.65	–102.07	106.86
1200	0.79	–53.90	27.30	–91.89	95.86
1300	0.78	–59.07	23.84	–82.83	86.19
1400	0.78	–64.41	21.34	–74.84	77.82
1500	0.77	–70.04	19.20	–67.56	70.24
1600	0.76	–75.84	17.46	–60.88	63.33
1700	0.75	–82.06	16.27	–54.72	57.09
1800	0.73	–88.56	15.36	–48.89	51.25
1900	0.72	–95.19	14.90	–43.34	45.83
2000	0.70	–101.45	14.32	–38.66	41.23

(1) V_{CC} = EN = 2.5 V, T_A = 25°C

Bench Test Setups (continued)

Table 1. LMX243x ULGA FinRF Input Impedance Table(1) (continued)

f_{FinRF} (MHz)	|Γ|	ANGLE (Γ) (°)	Re {ZFinRF} (Ω)	Im {ZFinRF} (Ω)	|ZFinRF| (Ω)
2100	0.68	–107.85	14.10	–34.26	37.05
2200	0.67	–114.12	13.81	–30.35	33.34
2300	0.66	–120.12	13.27	–27.09	30.17
2400	0.66	–126.01	12.50	–24.00	27.06
2500	0.67	–131.82	11.68	–21.22	24.22
2600	0.69	–137.96	10.55	–18.24	21.07
2700	0.71	–144.21	9.53	–15.58	18.26
2800	0.72	–150.25	8.55	–12.92	15.49
2900	0.74	–156.23	7.75	–10.25	12.85
3000	0.75	–161.92	7.22	–7.77	10.61
3100	0.76	–167.18	6.87	–5.48	8.79
3200	0.77	–172.05	6.63	–3.42	7.46
3300	0.77	–177.55	6.40	–1.49	6.57
3400	0.78	179.16	6.18	0.35	6.19
3500	0.79	174.92	5.99	2.18	6.37
3600	0.79	170.77	5.85	3.99	7.08
3700	0.80	166.54	5.74	5.80	8.16
3800	0.80	162.52	5.73	7.56	9.49
3900	0.80	158.74	5.73	9.22	10.86
4000	0.80	155.06	5.68	10.84	12.24
4100	0.80	151.49	5.69	12.38	13.62
4200	0.80	148.28	5.70	13.78	14.91
4300	0.80	146.02	5.73	14.88	15.95
4400	0.80	144.12	5.60	15.84	16.80
4500	0.82	142.31	5.41	16.66	17.52
4600	0.83	140.78	5.29	17.42	18.21
4700	0.83	139.65	5.14	17.95	18.67
4800	0.84	138.75	4.99	18.38	19.05
4900	0.84	137.79	4.84	18.85	19.46
5000	0.84	136.82	4.92	19.79	20.39
5100	0.84	135.77	4.88	18.89	19.51
5200	0.84	134.64	4.99	20.44	21.04
5300	0.84	133.33	5.11	21.16	21.77
5400	0.84	131.68	5.25	21.96	22.58
5500	0.83	129.77	5.43	23.01	23.64
5600	0.83	127.55	5.70	24.16	24.82
5700	0.82	125.41	6.03	25.33	26.04
5800	0.82	123.35	6.42	26.41	27.18
5900	0.81	121.68	6.75	27.30	28.12
6000	0.80	120.42	7.11	28.00	28.89

Table 2. LMX243x TSSOP FinRF Input Impedance Table(1)

f_{FinRF} (MHz)	|Γ|	Angle (Γ) (°)	Re {ZFinRF} (Ω)	Im {ZFinRF} (Ω)	|ZFinRF| (Ω)
100	0.86	–12.47	214.61	–314.33	380.61
200	0.85	–15.35	166.75	–270.14	317.46
300	0.84	–19.41	122.76	–228.38	259.28
400	0.83	–24.22	89.48	–193.48	213.17
500	0.82	–28.97	67.73	–167.98	181.12
600	0.82	–33.65	52.07	–148.64	157.5
700	0.82	–38.37	41.64	–131.88	138.3
800	0.82	–43.22	34.6	–117.36	122.35
900	0.81	–48.37	29.69	–104.33	108.47
1000	0.8	–53.84	25.88	–92.74	96.28
1100	0.79	–59.8	22.78	–82.21	85.31
1200	0.78	–66.29	20.17	–72.67	75.42
1300	0.77	–73.3	17.88	–64.06	66.51
1400	0.76	–80.74	15.93	–56.21	58.42
1500	0.75	–88.27	14.5	–49.36	51.45
1600	0.74	–95.87	13.27	–43.3	45.29
1700	0.73	–103.41	12.42	–37.96	39.94
1800	0.72	–110.77	11.67	–33.2	35.19
1900	0.71	–118.23	11.2	–28.78	30.88
2000	0.7	–125.46	11.25	–24.74	27.18
2100	0.68	–131.35	11.37	–21.6	24.41
2200	0.68	–137.19	10.94	–18.79	21.74
2300	0.68	–143.41	10.37	–15.88	18.97
2400	0.69	–149.45	9.7	–13.18	16.36
2500	0.71	–156.15	8.62	–10.26	13.4
2600	0.73	–163.87	7.79	–6.92	10.42
2700	0.74	–171.33	7.47	–3.71	8.34
2800	0.75	–178.24	7.3	0.76	7.34
2900	0.75	174.91	7.24	2.18	7.56
3000	0.75	168.09	7.33	5.12	8.94
3100	0.74	161.11	7.53	8.14	11.09
3200	0.74	153.92	7.83	11.3	13.75
3300	0.74	146.42	8.19	14.72	16.85
3400	0.74	138.67	8.59	18.36	20.27
3500	0.74	130.89	8.97	22.22	23.96
3600	0.75	123.33	9.3	26.23	27.83
3700	0.76	116.17	9.54	30.32	31.79
3800	0.77	109.55	9.74	34.42	35.77
3900	0.78	103.54	9.91	38.43	39.69
4000	0.79	98.25	10.2	42.23	43.44
4100	0.79	93.38	10.71	45.97	47.2
4200	0.79	88.86	11.7	49.59	50.95
4300	0.78	85.1	13.43	52.63	54.32
4400	0.77	82.09	14.79	55.23	57.18
4500	0.77	78.59	16.13	58.48	60.66
4600	0.76	74.73	17.9	62.3	64.82

(1) V_{CC} = EN = 2.5 V, T_A = 25°C

Table 2. LMX243x TSSOP FinRF Input Impedance Table(1) (continued)

f_{FinRF} (MHz)	|Γ|	Angle (Γ) (°)	Re {ZFinRF} (Ω)	Im {ZFinRF} (Ω)	|ZFinRF| (Ω)
4700	0.76	70.66	19.89	66.66	69.56
4800	0.75	66.05	22.5	72.05	75.48
4900	0.75	61.68	25.37	77.73	81.77
5000	0.75	57.35	28.56	84.19	88.9
5100	0.76	53.11	31.7	91.39	96.73
5200	0.77	48.79	34.78	100.34	106.2
5300	0.78	43.56	40.56	112.59	119.67
5400	0.78	38.11	52.53	125.62	136.16
5500	0.76	32.89	71.05	135.74	153.21
5600	0.73	27.85	95.57	142.32	171.43
5700	0.71	21.89	133.18	141.32	194.19
5800	0.68	15.38	177.08	116.75	212.1
5900	0.65	9.47	207.23	77.49	221.24
6000	0.64	4.15	222.92	35.24	225.69

Table 3. LMX243x ULGA FinIF Input Impedance Table(1)

f_{FinIF} (MHz)	|Γ|	Angle (Γ) (°)	Re {ZFinIF} (Ω)	Im {ZFinIF} (Ω)	|ZFinIF| (Ω)
100	0.87	–6.19	446.34	–341.41	561.94
200	0.86	–8.1	353.77	–328.44	482.73
300	0.85	–10.98	257.5	–300.77	395.94
400	0.84	–14.21	188.33	–268.39	327.87
500	0.83	–17.67	141.63	–235.88	275.13
600	0.83	–21.32	109.44	–206.86	234.03
700	0.82	–25.13	86.57	–182.41	201.91
800	0.81	–29.04	70.47	–161.46	176.17
900	0.8	–32.99	58.9	–144.27	155.83
1000	0.79	–36.73	50.96	–130.45	140.05
1100	0.79	–40.28	44.21	–120.14	128.02
1200	0.79	–44.11	37.38	–111.08	117.2
1300	0.79	–48.38	31.82	–101.96	106.81
1400	0.79	–52.91	27.95	–93.09	97.2
1500	0.78	–57.26	25.34	–85.47	89.15
1600	0.77	–61.56	23.28	–78.74	82.11
1700	0.77	–66.01	20.98	–72.74	75.71
1800	0.77	–71.39	18.4	–66.32	68.83
1900	0.77	–77.74	15.22	–59.4	61.32
2000	0.76	–84.72	15.02	–52.48	54.59
2100	0.73	–92.59	14.39	–46.17	48.36
2200	0.71	–100.18	14.07	–40.46	42.84
2300	0.69	–107.33	13.94	–35.79	38.41
2400	0.68	–114.48	13.37	–31.55	34.27
2500	0.68	–118.42	12.71	–28.62	31.32

(1) V_{CC} = EN = 2.5 V, T_A = 25°C

Table 4. LMX243x TSSOP FinIF Input Impedance Table(1)

f_{FinIF} (MHz)	|Γ|	Angle (Γ) (°)	Re {ZFinIF} (Ω)	Im {ZFinIF} (Ω)	|ZFinIF| (Ω)
100	0.87	–7.11	400.44	–348.14	530.62
200	0.86	–9.92	288.69	–318.81	430.1
300	0.85	–13.64	198.42	–281.45	344.36
400	0.84	–17.47	141.73	–246.13	284.02
500	0.84	–21.42	105.75	–214.58	239.22
600	0.83	–25.39	82	–188.43	205.5
700	0.83	–29.46	65.48	–166.34	178.76
800	0.82	–33.67	53.78	–147.46	156.96
900	0.81	–37.99	45.17	–131.83	139.35
1000	0.80	–42.47	38.82	–117.87	124.1
1100	0.79	–46.96	33.93	–106.36	111.64
1200	0.79	–51.67	29.53	–96.2	100.63
1300	0.78	–57.02	25.26	–86.47	90.08
1400	0.77	–63.11	22.15	–76.93	80.06
1500	0.76	–69.26	20.49	–68.42	71.42
1600	0.74	–74.82	19.54	–61.59	64.62
1700	0.74	–79.79	17.7	–56.35	59.06
1800	0.74	–86.55	15.09	–50.74	52.94
1900	0.74	–94.37	13.38	–44.56	46.53
2000	0.73	–101.95	12.62	–38.87	40.87
2100	0.72	–108.92	12.21	–34.18	36.3
2200	0.71	–115.63	11.65	–30.11	32.29
2300	0.71	–123.23	11.13	–25.97	28.25
2400	0.69	–131.44	11.08	–21.74	24.4
2500	0.67	–138.35	11.54	–18.31	21.64

(1) V_{CC} = EN = 2.5 V, T_A = 25°C

Table 5. LMX243x ULGA OSCin Input Impedance Table(1)

f_{OSCin} (MHz)	ENosc = 1			ENosc = 0		
	Re {ZOSCin} (Ω)	Im {ZOSCin} (Ω)	|ZOSCin| (Ω)	Re {ZOSCin} (Ω)	Im {ZOSCin} (Ω)	|ZOSCin| (Ω)
5	5032.01	–10120.58	11302.53	2641.63	–13293.58	13553.5
7.5	2529.17	–7382.23	7803.46	1108.82	–8932.61	9001.17
10	1412.1	–5693.56	5866.06	526.74	–6461.11	6482.55
12.5	1051.18	–4930.8	5041.6	330.16	–5452.11	5462.1
15	710.63	–4099.58	4160.72	233.66	–4455.98	4462.1
17.5	545.87	–3584.6	3625.92	212.67	–3822.33	3828.24
20	442.32	–3125.21	3156.35	192.16	–3306.06	3311.64
22.5	314.15	–2806.1	2823.63	112.07	–2963.67	2965.79
25	316.48	–2518.94	2538.75	143.65	–2657.93	2661.81
27.5	223.49	–2280.02	2290.95	84.09	–2405.34	2406.81
30	196.9	–2105.11	2114.3	40.38	–2196.07	2196.45
32.5	175.38	–1942.45	1950.35	77.29	–2044.88	2046.34
35	158.95	–1816.83	1823.77	67.31	–1898.92	1900.12
37.5	137.8	–1701.59	1707.16	51.11	–1775.84	1776.58
40	114.2	–1573.28	1577.42	50.39	–1652.06	1652.83

(1) V_{CC} = EN = 2.5 V, T_A = 25°C

Table 6. LMX243x TSSOP OSCin Input Impedance Table(1)

f_{OSCin} (MHz)	ENosc = 1			ENosc = 0		
	Re {ZOSCin} (Ω)	Im {ZOSCin} (Ω)	|ZOSCin| (Ω)	Re {ZOSCin} (Ω)	Im {ZOSCin} (Ω)	|ZOSCin| (Ω)
5	1111.3	–4814.09	4940.69	654.13	–7449.33	7477.99
7.5	628.81	–3411.8	3469.26	388.42	–5150.6	5165.22
10	359.99	–2623.46	2648.04	237.72	–3892.18	3899.44
12.5	284.12	–2065	2084.46	159	–2988.66	2992.88
15	203.53	–1801.24	1812.7	152.53	–2597.16	2601.63
17.5	134.32	–1548.5	1554.32	82.41	–2222.34	2223.86
20	109.85	–1343.3	1347.78	60.86	–1956.99	1957.94
22.5	80.56	–1192.73	1195.45	47.56	–1730.53	1731.18
25	69.37	–1063.72	1065.98	47.47	–1553.43	1554.15
27.5	60.1	–973.84	975.7	37.83	–1414.54	1415.04
30	50.3	–890.31	891.73	34.8	–1290.03	1290.5
32.5	45.52	–816.01	817.28	29.72	–1188.88	1189.25
35	41.55	–758.24	759.38	31.5	–1096.89	1097.35
37.5	37.73	–707.57	708.57	23.04	–1024.88	1025.14
40	36.09	–661.87	662.86	22.61	–963.11	963.38

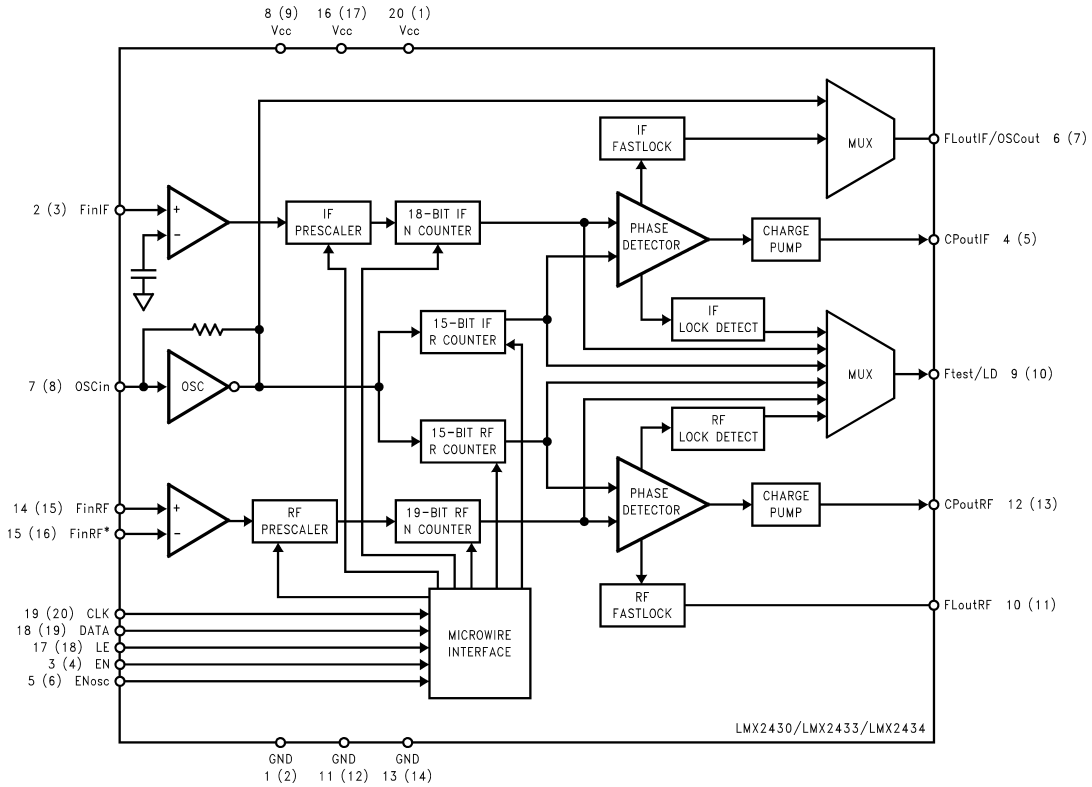
(1) V_{CC} = EN = 2.5 V, T_A = 25°C

9 Detailed Description

9.1 Overview

The basic phase-lock-loop (PLL) configuration consists of a high-stability crystal reference oscillator, a frequency synthesizer such as the LMX243x, a voltage controlled oscillator (VCO), and a passive loop filter. The frequency synthesizer includes a phase detector, current-mode charge pump, programmable reference R and feedback N frequency dividers. The VCO frequency is established by dividing the crystal reference signal down through the reference divider to obtain a comparison reference frequency. This reference signal, f_r, is then presented to the input of a phase / frequency detector and compared with the feedback signal, f_p, which was obtained by dividing the VCO frequency down by way of the feedback divider. The phase and frequency detector (PFD) measures the phase error between the f_r and f_p signals and outputs control signals that are directly proportional to the phase error. The charge pump then pumps charge into or out of the loop filter based on the magnitude and direction of the phase error. The loop filter converts the charge into a stable control voltage for the VCO. The function of the PFD is to adjust the voltage presented to the VCO until the frequency of the feedback signal and phase match that of the reference signal. When this *phase-locked* condition exists, the VCO frequency is N times that of the comparison frequency, where N is the feedback divider ratio.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Reference Oscillator Input

The reference oscillator frequency for both the RF and IF PLLs is provided from an external reference through the OSCin pin. The reference buffer circuit supports input frequencies from 5 to 40 MHz with a minimum input sensitivity of 0.5 V_{PP}. The reference buffer circuit has an approximate Vcc/2 input threshold and can be driven from an external AC-coupled source. Typically, the OSCin pin is connected to the output of a crystal oscillator.

9.3.2 Reference Dividers (R Counters)

The reference dividers divide the reference input signal, OSCin, by a factor of R. The output of the reference divider circuits feeds the reference input of the phase detector. This reference input to the phase detector is often referred to as the comparison frequency. The divide ratio must be chosen such that the maximum phase comparison frequency (f_{COMPRF} or f_{COMPIF}) of 10 MHz is not exceeded.

The RF and IF reference dividers are each comprised of 15-bit CMOS binary counters that support a continuous integer divide ratio from 3 to 32,767. The RF and IF reference divider circuits are clocked by the output of the reference buffer circuit which is common to both. Refer to *RF_R[14:0] - RF Synthesizer Programmable Reference Divider (R Counter) (R0[17:3])* and *IF_R[14:0] - IF Synthesizer Programmable Reference Divider (R Counter) (R3[17:3])* for details on how to program the RF_R and IF_R counters.

9.3.3 Prescalers

The FinRF and FinIF input pins drive the input of a differential-pair amplifier. The output of the differential-pair amplifier drives a chain of D-type flip-flops in a dual modulus configuration. The output of the prescaler is used to clock the subsequent feedback dividers. The RF PLL complementary inputs can be driven differentially, or the negative input can be AC-coupled to ground through an external capacitor for single-ended configuration. A 16/17 or a 32/33 prescale ratio can be selected for the 5-GHz LMX2434 RF synthesizer. An 8/9 or a 16/17 prescale ratio can be selected for both the LMX2430 and LMX2433 RF synthesizers. The IF PLL is single-ended, and an 8/9 or a 16/17 prescale ratio can be selected for the IF synthesizer.

9.3.4 Programmable Feedback Dividers (N Counters)

The programmable feedback dividers operate in concert with the prescalers to divide the input signal, Fin, by a factor of N. The output of the programmable reference divider is provided to the feedback input of the phase detector circuit. The divide ratio must be chosen so that the maximum phase comparison frequency (f_{COMPRF} or f_{COMPIF}) of 10 MHz is not exceeded.

The programmable feedback divider circuit is comprised of an A counter (swallow counter) and a B counter (programmble binary counter). For both the LMX2430 and LMX2433, the RF_A counter is a 4-bit swallow counter, programmable from 0 to 15. The LMX2434 RF_A counter is a 5-bit swallow counter, programmable from 0 to 31. The LMX243x IF_A counter is a 4-bit swallow counter, programmable from 0 to 15. For both the LMX2430 and LMX2433, the RF_B counter is a 15-bit binary counter, programmable from 3 to 32,767. The LMX2434 RF_B counter is a 14-bit binary counter, programmable from 3 to 16,383. The LMX243x IF_B is a 14-bit binary counter programmable from 3 to 16,383. A continuous integer divide ratio is achieved if $N \geq P \times (P-1)$, where P is the value of the prescaler selected.

Divide ratios less than the minimum continuous divide ratio are achievable as long as the binary programmable counter value is greater than the swallow counter value ($B \geq A$). Refer to *RF_A[3:0] - LMX2430/33 RF Synthesizer Swallow Counter (A Counter) (R1[6:3])*, *RF_A[4:0] - LMX2434 RF Synthesizer Swallow Counter (A Counter) (R1[7:3])*, *RF_B[14:0] - LMX2430/33 RF Synthesizer Programmable Binary Counter (B Counter) (R1[21:7])*, *RF_B[13:0] - LMX2434 RF Synthesizer Programmable Binary Counter (B Counter) (R1[21:8])*, *IF_A[3:0] - IF Synthesizer Swallow Counter (A Counter) (R4[6:3])*, and *IF_B[13:0] - IF Synthesizer Programmable Binary Counter (B Counter) (R4[20:7])* for details on how to program the A and B counters. Equation 4 and Equation 5 are useful in determining and programming a particular value of N:

$$N = (P \times B) + A \quad (4)$$

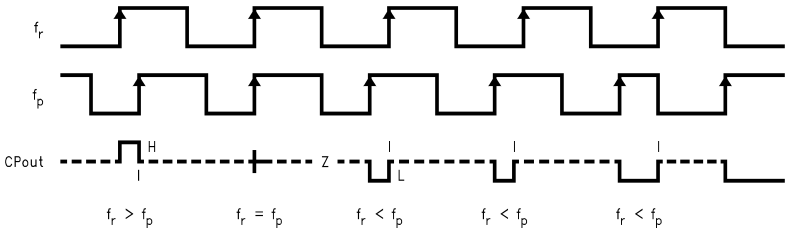
$$Fin = N \times f_{COMP} \quad (5)$$

Feature Description (continued)

9.3.5 Phase / Frequency Detectors

The RF and IF PFDs are driven from their respective N and R counter outputs. The maximum frequency for both the RF and IF phase detector inputs is 10 MHz. The PFD outputs control the respective charge pumps. The polarity of the pump-up or pump-down control signals are programmed using the *RF_CPP* or *IF_CPP* control bits, depending on whether the RF or IF VCO characteristics are positive or negative. Refer to *RF_CPP - RF Synthesizer Phase Detector Polarity (R0[18])* and *IF_CPP - IF Synthesizer Phase Detector Polarity (R3[18])* for more details. The PFDs have a detection range of −2π to +2π. The PFDs also receive a feedback signal from the charge pump in order to eliminate dead zone.

9.3.5.1 Phase Comparator and Internal Charge-Pump Characteristics



Notes:

1. The minimum width of the pump-up and pump-down current pulses occur at the CPoutRF or CPoutIF pins when the loop is phase locked.
2. The diagram assumes positive VCO characteristic that is, RF_CPP or IF_CPP = 1.
3. f_r is the PFD input from the reference divider (R counter).
4. f_p is the PFD input from the programmable feedback divider (N counter).
5. CPout refers to either the RF or IF charge-pump output

Figure 29. Phase Detector and Charge-Pump Operation

9.3.6 Charge Pumps

The charge pump directs charge into or out of an external loop filter. The loop filter converts the charge into a stable control voltage which is applied to the tuning input of the VCO. The charge pump steers the VCO control voltage towards V_{CC} during pump-up events and towards GND during pump-down events. When locked, CPoutRF or CPoutIF are primarily in a tri-state mode with small corrections occurring at the phase comparator rate. The charge-pump output current magnitude can be selected by toggling the *RF_CPG* or *IF_CPG* control bits.

9.3.7 Microwire Serial Interface

The programmable register set is accessed through the MICROWIRE serial interface. A low voltage logic interface allows direct connection to 1.8-V devices. The interface is comprised of three signal pins: CLK, DATA and LE. Serial data is clocked into the 24-bit shift register on the rising edge of CLK. The last two bits decode the internal control register address. When LE transitions HIGH, DATA stored in the shift register is loaded into one of four control registers depending on the state of the address bits. The MSB of DATA is loaded in first. The synthesizers can be programmed even in power-down mode. A complete programming description is provided in *Programming*.

9.3.8 Multi-Function Outputs

The Ftest/LD output pin of the LMX243x device is a multi-function output that can be configured as a general-purpose CMOS tri-state output, push-pull analog lock-detect output, open-drain analog lock-detect output, digital filtered lock-detect output, or used to monitor the output of the various reference divider (R counter) or feedback divider (N counter) circuits. The Ftest/LD control word is used to select the desired output function. When the PLL is in power-down mode, the Ftest/LD output is disabled and is in a high-impedance state. A complete programming description of the multi-function output is provided in *MUX[3:0] - Multifunction Output Select (R3[23:22]:R0[23:22])*.

Feature Description (continued)

9.3.8.1 Push-Pull Analog Lock-Detect Output

An analog lock-detect status generated from the phase detector is available on the Ftest/LD output pin if selected. A push-pull configuration can be selected for the lock-detect output signal. With this configuration, the lock-detect output goes HIGH when the charge pump is inactive. It goes LOW when the charge pump is active during a comparison cycle. Narrow low-going pulses are observed when the charge pump turns on.

There are three separate push-pull analog lock-detect signals that are routed to the multiplexer. Two of these monitor the lock status of the individual synthesizers. The third detects the condition when both the RF and IF synthesizers are in a locked state. External circuitry is required to provide a steady DC signal to indicate when the PLL is in a locked state. Refer to *MUX[3:0] - Multifunction Output Select (R3[23:22]:R0[23:22])* for details on how to program the different push-pull analog lock-detect options.

9.3.8.2 Open-Drain Analog Lock-Detect Output

The lock-detect output can be an open-drain configuration. In this configuration, the lock-detect output goes to a high impedance state when the charge pump is inactive. It goes LOW when the charge pump is active during a comparison cycle. When a pullup resistor is used, narrow low-going pulses are observed when the charge pump turns on.

Similarly, three separate open-drain analog lock-detect signals are routed to the multiplexer. Two of these monitor the lock status of the individual synthesizers. The third detects the condition when both the RF and IF synthesizers are in a locked state. External circuitry is required to provide a steady DC signal to indicate when the PLL is in a locked state. Refer to *MUX[3:0] - Multifunction Output Select (R3[23:22]:R0[23:22])* for details on how to program the different open-drain analog lock-detect options.

9.3.8.3 Digital Filtered Lock-Detect Output

A digital filtered lock-detect status generated from the phase detector is also available on the Ftest/LD output pin if selected. The lock-detect digital filter compares the difference between the phases of the inputs to the PFD to an RC-generated delay of approximately 15 ns. If the phase error is less than the 15-ns RC delay for 5 consecutive reference cycles, the PLL enters a locked state (HIGH). Once in lock, the RC delay is changed to approximately 30 ns. Once the phase error becomes greater than the 30-ns RC delay, the PLL falls out of lock (LOW). When the PLL is in power-down mode, the Ftest/LD output is forced LOW. A flow chart of the digital filtered lock-detect output is shown in Figure 30.

Feature Description (continued)

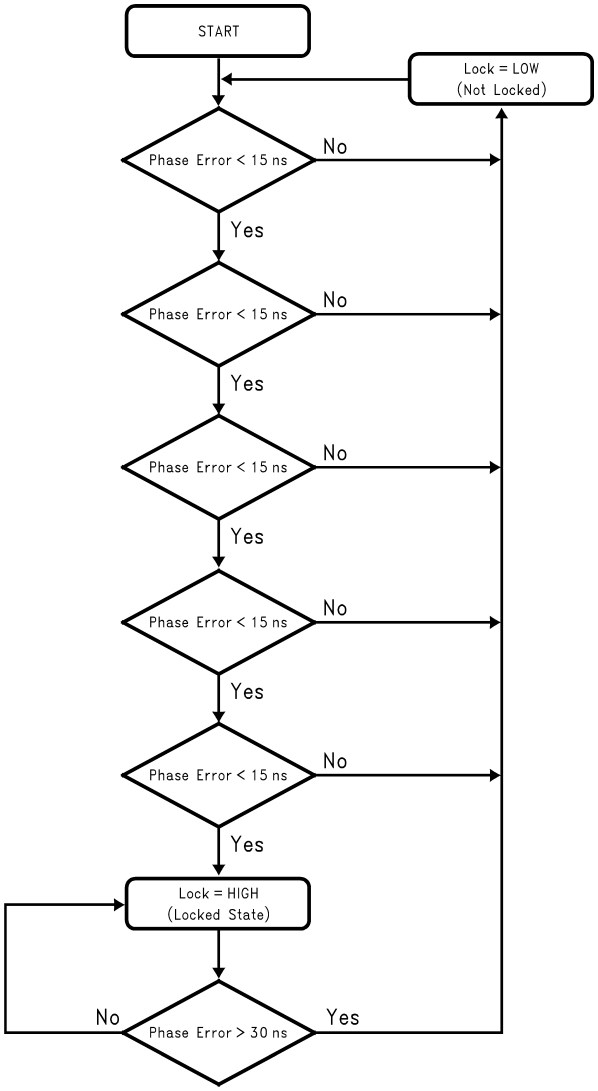


Figure 30. Digital Lock-Detect Operation

Similarly, three separate digital filtered lock-detect signals are routed to the multiplexer. Two of these monitor the lock status of the individual synthesizers. The third detects the condition when both the RF and IF synthesizers are in a locked state. External circuitry is not required when the digital filtered lock-detect option is selected. Refer to *MUX[3:0] - Multifunction Output Select (R3[23:22]:R0[23:22])* for details on how to program the different digital filtered lock-detect options.

9.3.8.4 Reference Divider and Feedback Divider Output

The outputs of the various N and R dividers can be monitored by selecting the appropriate Ftest/LD word. This is essential when performing OSCin or Fin sensitivity measurements. Refer to the *LMX243x FinRF Sensitivity Test Setup* or *LMX243x OSCin Sensitivity Test Setup* sections for more details.

Feature Description (continued)

NOTE

The R and N outputs that are routed to the Ftest/LD are R/2 and N/2, respectively. The internal /2 circuit is used to provide a 50% duty cycle. Refer to *MUX[3:0] - Multifunction Output Select (R3[23:22]:R0[23:22])* for more details on how to route the appropriate divider output to the Ftest/LD pin.

9.3.9 Fastlock Output

The LMX243x fastlock feature allows a faster loop response time during lock aquisition. The loop response time (lock time) can be approximately halved if the loop bandwidth is doubled. In order to achieve this, the same gain / phase relationship must be maintained when the loop bandwidth is doubled. When the FLoutRF or OSCout/ FLoutIF pins are configured as fastLock outputs, an open-drain device is enabled. The open-drain device switches in a resistor parallel, and of equal value, to R2 of the external loop filter.

The loop bandwidth is effectively doubled and stability is maintained. Once locked to the correct frequency, the PLL returns to a steady-state condition. The LMX243x offers two methods to achieve fastlock: manual and automatic. Manual fastlock is achieved by increasing the charge pump current from 1 mA (RF_CPG/ IF_CPG Bit = 0) in the steady-state mode, to 4 mA (RF_CPG/ IF_CPG Bit = 1) in fastlock mode. Automatic fastlock is achieved by programming the time-out counter register (RF_TOC/ IF_TOC) with the appropriate number of phase comparison cycles that the RF/ IF synthesizer spends in the fastlock state. Refer to *R2 Register* and *R5 Register* for details on how to configure the FLoutRF or OSCout/ FLoutIF output to an open-drain fastlock output.

9.3.10 Counter Reset

When the RF_RST/ IF_RST bit is enabled, both the feedback divider (RF_N/ IF_N) and reference divider (RF_R/ IF_R) are held at their load point. When the device is programmed to normal operation, both the feedback divider and reference divider are enabled and resume counting in close alignment to each other. Refer to *RF_RST - RF Synthesizer Counter Reset (R0[21])* and *IF_RST - IF Synthesizer Counter Reset (R3[21])* for more details.

9.4 Device Functional Modes

9.4.1 Power Control

The LMX243x device can be asynchronously powered down when the EN pin is set LOW, independent of the state of the power-down bits.

NOTE

The OSCout/ FLoutIF pin can still be enabled if the ENosc pin is set HIGH, independent of the state of the EN pin. This capability allows the oscillator buffer to be used as a crystal oscillator.

When EN is set HIGH, power down is controlled through the MICROWIRE. The power-down word is comprised of the *RF_PD*/ *IF_PD* bit, in conjunction with the *RF_CPT*/ *IF_CPT* bit. The power-down control word is used to set the operating mode of the device. Refer to *RF_CPT - RF Synthesizer Charge-Pump Tri-State (R0[20])*, *RF_PD - RF Synthesizer Power Down (R1[23])*, *IF_CPT - IF Synthesizer Charge-Pump Tri-State (R3[20])*, and *IF_PD - IF Synthesizer Power Down (R4[23])* for details on how to program the RF or IF power-down bits.

When either synthesizer is powered down, the respective prescaler, phase detector, and charge-pump circuit is disabled. The CPoutRF/ CPoutIF, FinRF/ FinIF, and FinRF* pins are all forced to a high impedance state. The reference divider and feedback divider circuits are held at the load point during power down. The oscillator buffer is disabled when the ENosc pin is set LOW. The OSCin pin is forced to a HIGH state through an approximate 100-kΩ resistance when this condition exists. When either synthesizer is activated, the respective prescaler, phase detector, charge-pump circuit, and the oscillator buffer are all powered up. The feedback divider and

Device Functional Modes (continued)

reference divider are held at their load point. This allows the reference oscillator, feedback divider, reference divider, and prescaler circuitry to reach proper bias levels. After a finite delay, the feedback and reference dividers are enabled and resume counting in close alignment (the maximum error is one prescaler cycle). The MICROWIRE control register remains active and capable of loading and latching data while in power-down mode.

9.4.1.1 Synchronous Power-Down Mode

In this mode, the power-down function is gated by the charge pump. When the device is configured for synchronous power down, the device enters the power-down mode upon completion of the next charge-pump pulse event.

9.4.1.2 Asynchronous Power-Down Mode

In the asynchronous power-down mode, the power-down function is NOT gated by the completion of a charge-pump pulse event. When the device is configured for asynchronous power down, the part goes into power-down mode immediately.

Table 7. Power-Down Modes

EN PIN	RF_CPT / IF_CPT BIT	RF_PD / IF_PD BIT	OPERATING MODE
0	X(1)	X(1)	Asynchronous Power Down
1	0	0	PLL Active. Normal Operation
1	1	0	PLL Active. Charge-Pump Output in High-Impedance State
1	0	1	Synchronous Power Down
1	1	1	Asynchronous Power Down

(1) X refers to a don't care condition.

9.5 Programming

9.5.1 Microwire Interface

The 24-bit shift register is loaded through the MICROWIRE interface. The shift register consists of a 21-bit *DATA[20:0] FIELD* and a 3-bit *ADDRESS[2:0] FIELD* as shown in Table 8. The ADDRESS FIELD is used to decode the internal control register address. When LE transitions HIGH, DATA stored in the shift register is loaded into one of 6 control registers depending on the state of the ADDRESS bits. The MSB of DATA is loaded into the shift register first. The DATA FIELD assignments are shown in *Control Register Content Map*.

Table 8. Register Structure

MSB		LSB
DATA[20:0]		ADDRESS[2:0]
23	3 2	0

9.5.2 Control Register Location

The ADDRESS[2:0] bits decode the internal register address. The Table 9 shows how the ADDRESS bits are mapped into the target control register.

Table 9. Control Register Locations

ADDRESS[2:0] FIELD			TARGET REGISTER
0	0	0	R0
0	0	1	R1
0	1	0	R2
0	1	1	R3
1	0	0	R4
1	0	1	R5

9.6 Register Maps

9.6.1 Control Register Content Map

The control register content map describes how the bits within each control register are allocated to specific control functions. The bits that are marked 0 must be programmed as such to ensure proper device operation.

Table 10. Control Register Content Map

REG	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[20:0] FIELD																					ADDRESS [2:0] FIELD		
R0	MUX[3:2]		RF_RST	RF_CPT	RF_CPG	RF_CPP	RF_R[14:0]															0	0	0
R1	RF_PD	RF_P	LMX2430/33 RF_B[14:0]															LMX2430/33 RF_A[3:0]				0	0	1
R1	RF_PD	RF_P	LMX2434 RF_B[13:0]														LMX2434 RF_A[4:0]					0	0	1
R2	0	0	0	0	0	0	0	0	0	RF_TOC[11:0]												0	1	0
R3	MUX[1:0]		IF_RST	IF_CPT	IF_CPG	IF_CPP	IF_R[14:0]															0	1	1
R4	IF_PD	IF_P	0	IF_B[13:0]														IF_A[3:0]				1	0	0
R5	0	0	0	0	0	0	0	0	0	IF_TOC[11:0]												1	0	1

9.6.2 R0 Register

The R0 register contains the RF_R, RF_CPP, RF_CPG, RF_CPT, and RF_RST control words, in addition to two of the four bits that compose the MUX control word. The detailed descriptions and programming information for each control word is discussed in the following sections.

Table 11. R0 Register

REG	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[20:0] FIELD																					ADDRESS [2:0] FIELD		
R0	MUX[3:2]		RF_RST	RF_CPT	RF_CPG	RF_CPP	RF_R[14:0]															0	0	0

9.6.2.1 RF_R[14:0] - RF Synthesizer Programmable Reference Divider (R Counter) (R0[17:3])

The RF reference divider (RF_R) can be programmed to support divide ratios from 3 to 32,767. Divide ratios less than 3 are prohibited.

Table 12. PLL R Divider

DIVIDE RATIO	RF_R[14:0]														
	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
3	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
32767	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

9.6.2.2 RF_CPP - RF Synthesizer Phase Detector Polarity (R0[18])

The RF_CPP bit is used to control the PFD polarity of the RF synthesizer based on the VCO tuning characteristics.

Table 13. Phase Detector Polarity

CONTROL BIT	REGISTER LOCATION	DESCRIPTION	FUNCTION	
			0	1
RF_CPP	R0[18]	RF Phase and Frequency Detector Polarity	RF VCO Negative Tuning Characteristics	RF VCO Positive Tuning Characteristics

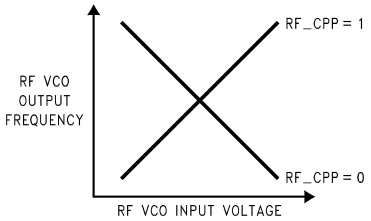


Figure 31. RF VCO Characteristics

9.6.2.3 RF_CPG - RF Synthesizer Charge-Pump Current Gain (R0[19])

The RF_CPG bit controls the charge-pump gain of the RF synthesizer. Two gain levels are available.

Table 14. Charge-Pump Polarity

CONTROL BIT	REGISTER LOCATION	DESCRIPTION	FUNCTION	
			0	1
RF_CPG	R0[19]	RF Charge-Pump Current Gain	LOW 1 mA	HIGH 4 mA

9.6.2.4 RF_CPT - RF Synthesizer Charge-Pump Tri-State (R0[20])

The RF_CPT bit allows the charge pump to be switched between a normal operating mode and a high-impedance output state. This happens asynchronously with the change in the RF_CPT bit.

Furthermore, the RF_CPT bit operates in conjuction with the RF_PD bit to set a synchronous or an asynchronous power-down mode. Refer to *RF_PD - RF Synthesizer Power Down (R1[23])* for more details on how to program the RF_PD bit.

Table 15. Charge-Pump Tri-State

CONTROL BIT	REGISTER LOCATION	DESCRIPTION	FUNCTION	
			0	1
RF_CPT	R0[20]	RF Charge-Pump tri-state	RF Charge Pump Normal Operation	RF Charge-Pump Output in High Impedance State

9.6.2.5 RF_RST - RF Synthesizer Counter Reset (R0[21])

The RF_RST bit resets the RF_A, RF_B and RF_R counters. After removing the reset, the RF_A and RF_B counters resume counting in close alignment with the RF_R counter. The maximum error is one prescaler cycle.

Table 16. N Counter Reset

CONTROL BIT	REGISTER LOCATION	DESCRIPTION	FUNCTION	
			0	1
RF_RST	R0[21]	RF Counter Reset	RF_A, RF_B and RF_R Normal Operation	RF_A, RF_B and RF_R Reset

9.6.3 R1 Register

The R1 register contains the RF_A, RF_B, RF_P, and RF_PD control words. The RF_A and RF_B control words are used to set up the programmable feedback divider. The detailed descriptions and programming information for each control word is discussed in the following sections.

Table 17. RI Register

REG	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[20:0] FIELD																					ADDRESS [2:0] FIELD		
R1	RF_PD	RF_P	LMX2430/33 RF_B[14:0]															LMX2430/33 RF_A[3:0]				0	0	1
R1	RF_PD	RF_P	LMX2434 RF_B[13:0]														LMX2434 RF_A[4:0]					0	0	1

9.6.3.1 LMX243x RF Synthesizer Swallow Counter

9.6.3.1.1 RF_A[3:0] - LMX2430/33 RF Synthesizer Swallow Counter (A Counter) (R1[6:3])

The RF_A control word is used to set up the A counter of the RF synthesizer. For both the LMX2430 and LMX2433, the A counter is a 4-bit swallow counter used in the programmable feedback divider. The RF_A control word can be programmed to values ranging from 0 to 15.

Table 18. RF_A Divider for LMX2430/33

DIVIDE RATIO	LMX2430/33 RF_A[3:0]			
	3	2	1	0
0	0	0	0	0
1	0	0	0	1
•	•	•	•	•
15	1	1	1	1

9.6.3.1.2 RF_A[4:0] - LMX2434 RF Synthesizer Swallow Counter (A Counter) (R1[7:3])

The LMX2434 A counter is a 5-bit swallow counter used in the programmable feedback divider. The RF_A control word can be programmed to values ranging from 0 to 31.

Table 19. RF A Divider for LMX2434

DIVIDE RATIO	LMX2434 RF_A[4:0]				
	4	3	2	1	0
0	0	0	0	0	0
1	0	0	0	0	1
•	•	•	•	•	•
31	1	1	1	1	1

9.6.3.2 LMX243x RF Synthesizer Programmable Binary Counter

9.6.3.2.1 RF_B[14:0] - LMX2430/33 RF Synthesizer Programmable Binary Counter (B Counter) (R1[21:7])

The RF_B control word is used to set up the B counter of the RF synthesizer. For both the LMX2430 and LMX2433, the B counter is a 15-bit programmable binary counter used in the programmable feedback divider. The RF_B control word can be programmed to values ranging from 3 to 32,767. Divide ratios less than 3 are prohibited.

Table 20. RF B Divider for LMX2430/33

DIVIDE RATIO	LMX2430/33 RF_B[14:0]														
	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
3	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
32767	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

9.6.3.2.2 RF_B[13:0] - LMX2434 RF Synthesizer Programmable Binary Counter (B Counter) (R1[21:8])

The LMX2434 B counter is a 14-bit programmable binary counter used in the programmable feedback divider. The RF_B control word can be programmed to values ranging from 3 to 16,383. Divide ratios less than 3 are prohibited.

Table 21. RF B Divider for LMX2434

DIVIDE RATIO	LMX2434 RF_B[13:0]													
	13	12	11	10	9	8	7	6	5	4	3	2	1	0
3	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

9.6.3.3 LMX243x RF Synthesizer Prescaler Select

9.6.3.3.1 RF_P - LMX2430/33 RF Synthesizer Prescaler Select (R1[22])

Both the LMX2430 and LMX2433 RF synthesizers use a selectable dual-modulus prescaler. An 8/9 or a 16/17 prescale ratio can be selected.

Table 22. Prescaler Select Bit for LMX2430/33

CONTROL BIT	REGISTER LOCATION	DESCRIPTION	FUNCTION	
			0	1
RF_P	R1[22]	LMX2430/33 RF Prescaler Select	8/9 Prescaler Selected	16/17 Prescaler Selected

9.6.3.3.2 RF_P - LMX2434 RF Synthesizer Prescaler Select (R1[22])

The LMX2434 RF synthesizer uses a selectable dual-modulus prescaler. A 16/17 or a 32/33 prescale ratio can be selected.

Table 23. Prescaler Select Bit for LMX2434

CONTROL BIT	REGISTER LOCATION	DESCRIPTION	FUNCTION	
			0	1
RF_P	R1[22]	LMX2434 RF Prescaler Select	16/17 Prescaler Selected	32/33 Prescaler Selected

9.6.3.4 RF_PD - RF Synthesizer Power Down (R1[23])

The RF_PD bit is used to switch the RF PLL between a powered-up and powered-down mode.

Furthermore, the RF_PD bit operates in conjunction with the RF_CPT bit to set a synchronous or an asynchronous power-down mode. Refer to *RF_CPT - RF Synthesizer Charge-Pump Tri-State (R0[20])* for more details on how to program the RF_CPT bit.

Table 24. Power Down Bit

CONTROL BIT	REGISTER LOCATION	DESCRIPTION	FUNCTION	
			0	1
RF_PD	R1[23]	RF Power down	RF PLL Active	RF PLL Power down

9.6.4 R2 Register

The R2 Register contains the RF_TOC control word. The RF_TOC is used to set up the fastlock circuitry of the RF synthesizer. The RF_TOC is a 12-bit binary counter programmable from 0 to 4095.

Table 25. R2 Register

REG	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[20:0] FIELD																					ADDRESS [2:0] FIELD		
R2	0	0	0	0	0	0	0	0	0	RF_TOC[11:0]												0	1	0

9.6.4.1 RF_TOC[0:11] - RF Synthesizer Time-Out Counter (R2[14:3])

The FLoutRF pin can be configured as a general-purpose CMOS tri-state output or as a fastlock output by programming the RF_TOC appropriately. When the RF_TOC is programmed from 0 to 3, automatic fastlock is disabled, and the FLoutRF pin is either configured as a general-purpose CMOS tri-state output or manual fastlock is enabled. When the RF_TOC is programmed to 0, the FLoutRF pin is in tri-state (high impedance) mode. The charge-pump current is then the value specified by RF_CPG (R0[19]). When the RF_TOC is programmed to 1, the FLoutRF pin is pulled to a LOW state. The charge-pump current is then set to a HIGH gain state (RF_CPG bit = 1). This condition is known as the manual fastlock. When the RF_TOC is programmed to 2, the FLout_RF pin is again pulled to a LOW state, but this time the charge-pump current is the value specified by RF_CPG (R0[19]). When the RF_TOC is programmed to 3, the FLoutRF pin is pulled to a HIGH state. Again, the charge-pump current is the value specified by RF_CPG (R0[19]). When the RF_TOC is programmed from 4 to 4095, fastlock is enabled, and the FLoutRF pin is pulled to a LOW state. Fastlock time outs after the specified number of PFD events. At this time, the FLoutRF pin switches to tri-state (high impedance) mode. The value programmed into RF_TOC represents the number of PFD events that the RF synthesizer spends in the fastlock state.

NOTE

Any write to the RF_TOC requires a PFD event on the RF synthesizer to latch the contents. This means that writes to the RF_TOC take effect synchronously with the next PFD event.

Table 26. Fastlock Time-Out Counter

RF_TOC[11:0]	FASTLOCK MODE	FASTLOCK PERIOD [PFD EVENTS]	FLoutRF PIN FUNCTIONALITY / STATE	$I_{CPoutRF}$ MAGNITUDE
0	Disabled	N/A	General-Purpose. High Impedance State	$I_{CPoutRF}$ magnitude controlled by R0[19]
1	Enabled Manual Fastlock	N/A	General-Purpose. Logic LOW State	$I_{CPoutRF}$ = 4 mA
2	Disabled	N/A	General-Purpose. Logic LOW State	$I_{CPoutRF}$ magnitude controlled by R0[19]
3	Disabled	N/A	General-Purpose. Logic HIGH State	$I_{CPoutRF}$ magnitude controlled by R0[19]
4	Enabled Automatic Fastlock	4	FastLock. Logic LOW State. Switches to High Impedance after 4 PFD events	$I_{CPoutRF}$ = 4 mA Switches to 1 mA after 4 PFD events
…	…	…	…	…
4095	Enabled Automatic Fastlock	4095	FastLock. Logic LOW State. Switches to High Impedance after 4095 PFD events	$I_{CPoutRF}$ = 4 mA Switches to 1 mA after 4095 PFD events

9.6.4.2 R3 Register

The R3 register contains the IF_R, IF_CPP, IF_CPG, IF_CPT, and IF_RST control words, in addition to two of the four bits that compose the MUX control word. The detailed descriptions and programming information for each control word is discussed in the following sections.

Table 27. R3 Register

REG	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[20:0] FIELD																					ADDRESS [2:0] FIELD		
R3	MUX[1:0]		IF_RST	IF_CPT	IF_CPG	IF_CPP	IF_R[14:0]															0	1	1

9.6.4.2.1 IF_R[14:0] - IF Synthesizer Programmable Reference Divider (R Counter) (R3[17:3])

The IF reference divider (IF_R) can be programmed to support divide ratios from 3 to 32,767. Divide ratios less than 3 are prohibited.

Table 28. IF R Divider

DIVIDE RATIO	IF_R[14:0]														
	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
3	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
32767	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

9.6.4.2.2 IF_CPP - IF Synthesizer Phase Detector Polarity (R3[18])

The IF_CPP bit is used to control the PFD polarity of the IF synthesizer based on the VCO tuning characteristics.

Table 29. IF PLL Charge-Pump Polarity

CONTROL BIT	REGISTER LOCATION	DESCRIPTION	FUNCTION	
			0	1
IF_CPP	R3[18]	IF PFD Polarity	IF VCO Negative Tuning Characteristics	IF VCO Positive Tuning Characteristics

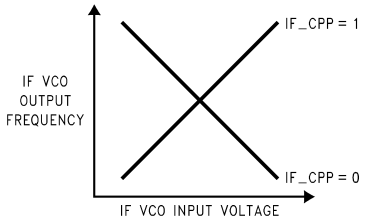


Figure 32. IF VCO Characteristics

9.6.4.2.3 IF_CPG - IF Synthesizer Charge-Pump Current Gain (R3[19])

The IF_CPG bit controls the charge-pump gain of the IF synthesizer. Two gain levels are available.

Table 30. IF PLL Phase Detector Polarity Bit

CONTROL BIT	REGISTER LOCATION	DESCRIPTION	FUNCTION	
			0	1
IF_CPG	R3[19]	IF Charge-Pump Current Gain	LOW 1 mA	HIGH 4 mA

9.6.4.2.4 IF_CPT - IF Synthesizer Charge-Pump Tri-State (R3[20])

The IF_CPT bit allows the charge pump to be switched between a normal operating mode and a high impedance output state. This happens asynchronously with the change in the IF_CPT bit.

Furthermore, the IF_CPT bit operates in conjuction with the IF_PD bit to set a synchronous or an asynchronous power-down mode. Refer to *IF_PD - IF Synthesizer Power Down (R4[23])* for more details on how to program the IF_PD bit.

Table 31. IF PLL Charge-Pump Polarity Bit

CONTROL BIT	REGISTER LOCATION	DESCRIPTION	FUNCTION	
			0	1
IF_CPT	R3[20]	IF Charge-Pump Tri-State	IF Charge Pump Normal Operation	IF Charge-Pump Output in High Impedance State

9.6.4.2.5 IF_RST - IF Synthesizer Counter Reset (R3[21])

The IF_RST bit resets of the IF_A, IF_B and IF_R counters. After removing the reset, the IF_A and IF_B counters resume counting in close alignment with the IF_R counter. The maximum error is one prescaler cycle.

Table 32. IF PLL Counter Reset

CONTROL BIT	REGISTER LOCATION	DESCRIPTION	FUNCTION	
			0	1
IF_RST	R3[21]	IF Counter Reset	IF_A, IF_B and IF_R Normal Operation	IF_A, IF_B and IF_R Reset

9.6.5 R4 Register

The R4 register contains the IF_A, IF_B, IF_P, and IF_PD control words. The IF_A and IF_B control words are used to set up the programmable feedback divider. The detailed descriptions and programming information for each control word is discussed in the following sections. R4[21] is always set to 0.

Table 33. R4 Register

REG	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[20:0] FIELD																					ADDRESS [2:0] FIELD		
R4	IF_PD	IF_P	0	IF_B[13:0]														IF_A[3:0]				1	0	0

9.6.5.1 IF_A[3:0] - IF Synthesizer Swallow Counter (A Counter) (R4[6:3])

The IF_A control word is used to set up the A counter of the IF synthesizer. The A counter is a 4-bit swallow counter used in the programmable feedback divider. The IF_A control word can be programmed to values ranging from 0 to 15.

Table 34. IF A counter Bit

DIVIDE RATIO	IF_A[3:0]			
	3	2	1	0
0	0	0	0	0
1	0	0	0	1
•	•	•	•	•
15	1	1	1	1

9.6.5.2 IF_B[13:0] - IF Synthesizer Programmable Binary Counter (B Counter) (R4[20:7])

The IF_B control word is used to set up the B counter of the IF synthesizer. The B counter is a 14-bit programmable binary counter used in the programmable feedback divider. The IF_B control word can be programmed to values ranging from 3 to 16,383. Divide ratios less than 3 are prohibited.

Table 35. IF B Counter

DIVIDE RATIO	IF_B[13:0]													
	13	12	11	10	9	8	7	6	5	4	3	2	1	0
3	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

9.6.5.2.1 IF_P - IF Synthesizer Prescaler Select (R4[22])

The LMX243x IF synthesizer uses a selectable dual modulus prescaler. An 8/9 or a 16/17 prescale ratio can be selected.

Table 36. IF Prescaler Select Bit

CONTROL BIT	REGISTER LOCATION	DESCRIPTION	FUNCTION	
			0	1
IF_P	R4[22]	IF Prescaler Select	8/9 Prescaler Selected	16/17 Prescaler Selected

9.6.5.3 IF_PD - IF Synthesizer Power Down (R4[23])

The IF_PD bit is used to switch the IF PLL between a powered-up and powered-down mode.

Furthermore, the IF_PD bit operates in conjuction with the IF_CPT bit to set a synchronous or an asynchronous power-down mode. Refer to *IF_CPT - IF Synthesizer Charge-Pump Tri-State (R3[20])* for more details on how to program the IF_CPT bit.

Table 37. IF PLL Powerdown Bit

CONTROL BIT	REGISTER LOCATION	DESCRIPTION	FUNCTION	
			0	1
IF_PD	R4[23]	IF Power down	IF PLL Active	IF PLL Power down

9.6.6 R5 Register

The R5 Register contains the IF_TOC control word. The IF_TOC is used to set up the fastlock circuitry of the IF synthesizer. The IF_TOC is a 12-bit binary counter programmable from 0 to 4095.

Table 38. R5 Register

REG	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[20:0] FIELD																					ADDRESS [2:0] FIELD		
R5	0	0	0	0	0	0	0	0	0	IF_TOC[11:0]												1	0	1

9.6.6.1 IF_TOC[0:11] - IF Synthesizer Time-Out Counter (R5[14:3])

The OSCout/ FLoutIF pin can be configured as a general-purpose CMOS tri-state output or as a fastlock output by programming the IF_TOC appropriately. When the IF_TOC is programmed from 0 to 3, automatic fastlock is disabled, and the OSCout/ FLoutIF pin is configured as a general-purpose CMOS tri-state output or manual fastlock is enabled. When the IF_TOC is programmed to 0, the OSCout/ FLoutIF pin is in tri-state (high impedance) mode. The charge-pump current is then the value specified by IF_CPG (R3[19]). When the IF_TOC is programmed to 1, the OSCout/ FLoutIF pin is pulled to a LOW state. The charge-pump current is then set to a HIGH gain state (IF_CPG bit = 1). This condition is known as the manual fastlock. When the IF_TOC is programmed to 2, the OSCout/ FLout_IF pin is again pulled to a LOW state, but this time the charge-pump current is the value specified by IF_CPG (R3[19]). When the IF_TOC is programmed to 3, the OSCout/ FLoutIF pin is pulled to a HIGH state. Again, the charge-pump current is the value specified by IF_CPG (R3[19]). When the IF_TOC is programmed from 4 to 4095, fastlock is enabled, and the OSCout/ FLoutIF pin is pulled to a LOW state. Fastlock timeouts after the specified number of PFD events. At this time, the OSCout/ FLoutIF pin switches to tri-state (high impedance) mode. The value programmed into IF_TOC represents the number of PFD events that the IF synthesizer spends in the fastlock state.

NOTE

Any write to the IF_TOC requires a PFD event on the IF synthesizer to latch the contents. This means that writes to the IF_TOC take effect synchronously with the next PFD event.

Table 39. IF PLL Fastlock Time-Out Counter

IF_TOC[11:0]	FASTLOCK MODE	FASTLOCK PERIOD [PFD Events]	OSCout/ FLoutIF PIN FUNCTIONALITY / STATE	$I_{CPoutIF}$ MAGNITUDE
0	Disabled	N/A	General-Purpose. High Impedance State	$I_{CPoutIF}$ magnitude controlled by R3[19]
1	Enabled Manual Fastlock	N/A	General-Purpose. Logic LOW State	$I_{CPoutIF}$ = 4 mA
2	Disabled	N/A	General-Purpose. Logic LOW State	$I_{CPoutIF}$ magnitude controlled by R3[19]
3	Disabled	N/A	General-Purpose. Logic HIGH State	$I_{CPoutIF}$ magnitude controlled by R3[19]
4	Enabled Automatic Fastlock	4	FastLock. Logic LOW State. Switches to High Impedance after 4 PFD events	$I_{CPoutIF}$ = 4 mA Switches to 1 mA after 4 PFD events
…	…	…	…	…
4095	Enabled Automatic Fastlock	4095	FastLock. Logic LOW State. Switches to High Impedance after 4095 PFD events	$I_{CPoutIF}$ = 4 mA Switches to 1 mA after 4095 PFD events

9.6.7 MUX[3:0] - Multifunction Output Select (R3[23:22]:R0[23:22])

The MUX control word is used to determine which signal is routed to the Ftest/LD pin.

Table 40. Multifunction Output Select(1)

MUX[3:0]				MUX OUTPUT STATE
0	0	0	0	High Impedance (Tri-state) State Output
0	0	0	1	Logic HIGH State Output
0	0	1	0	Logic LOW State Output
0	0	1	1	RF PLL and IF PLL Digital Lock Detect. Open-Drain Output
0	1	0	0	RF PLL Digital Lock Detect. Open-Drain Output
0	1	0	1	IF PLL Digital Lock Detect. Open-Drain Output
0	1	1	0	RF PLL and IF PLL Analog Lock Detect. Open-Drain Output
0	1	1	1	RF PLL Analog Lock Detect. Open-Drain Output
1	0	0	0	IF PLL Analog Lock Detect. Open-Drain Output
1	0	0	1	RF PLL and IF PLL Analog Lock Detect. Push-Pull Output
1	0	1	0	RF PLL Analog Lock Detect. Push-Pull Output
1	0	1	1	IF PLL Analog Lock Detect. Push-Pull Output
1	1	0	0	IF_R/ 2 Frequency
1	1	0	1	IF_N/ 2 Frequency
1	1	1	0	RF_R/ 2 Frequency
1	1	1	1	RF_N/ 2 Frequency

(1) 1. RF_N = (RF_B × RF_P) + RF_A
2. IF_N = (IF_B × IF_P) + IF_A

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The LMX2430 family of devices can be used in a broad class of applications. LMX2430x devices have very low current consumption and are well-suited for many lower power applications. Because these devices have two PLLs, they can be used to generate two distinct frequencies. However, it is a perfectly valid thing to only use one of the PLLs and power down the other side. When only one side is used, be sure to power the other side down, but do NOT disconnect the power pins for the unused side as they are shared across several internal blocks. When the unused side is powered down, it draws no current, and the counters and charge pump are not running or generating any noise and spurs. Figure 33 generally applies to most applications.

10.2 Typical Application

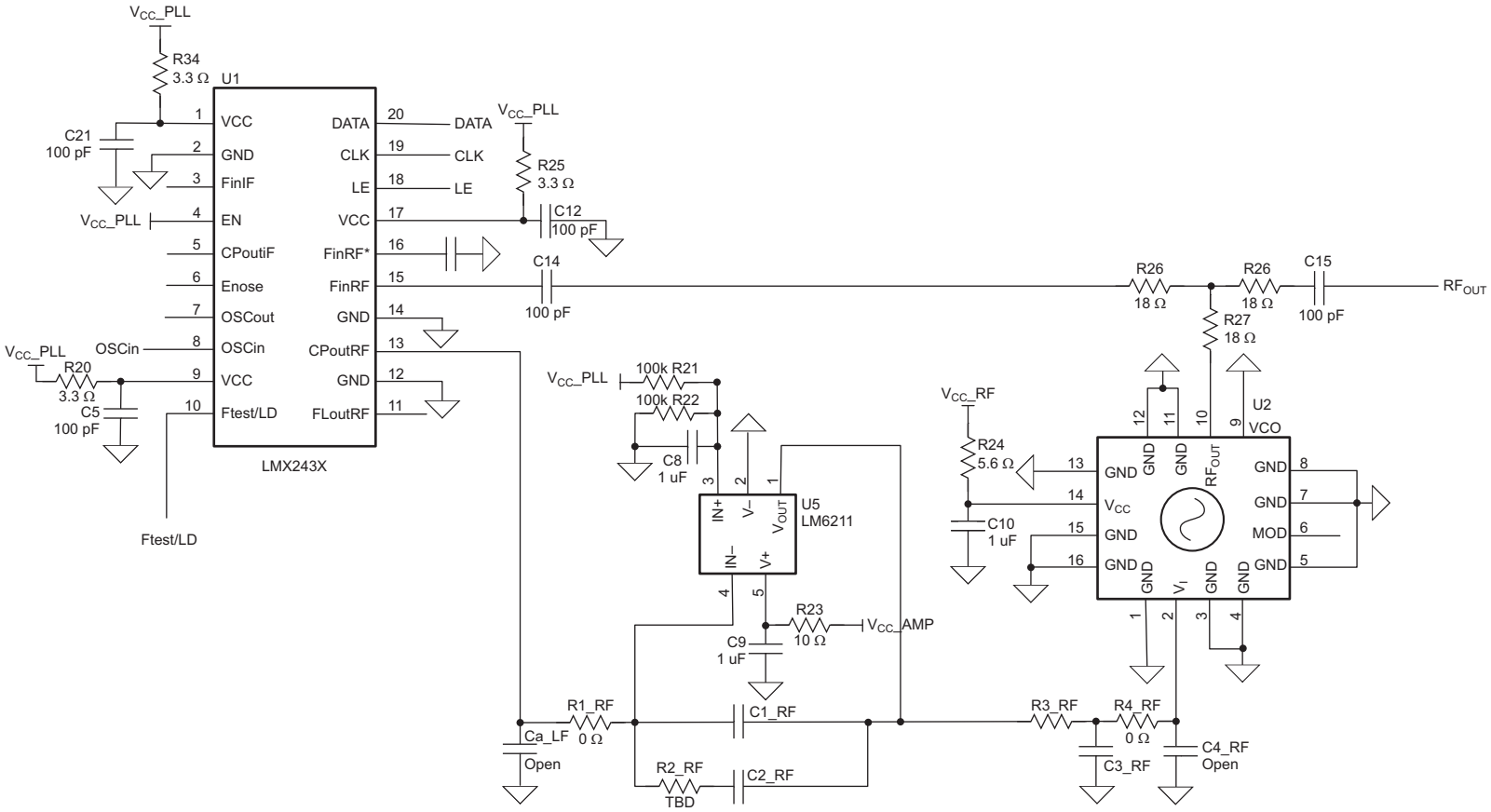


Figure 33. Typical Use Case

10.2.1 Design Requirements

Table 41 lists the design parameters of the LMX243x.

Table 41. Design Parameters

PARAMETER		VALUE
K_{PD}	Charge-Pump Gain	4 mA
C_{VCO}	VCO Input Capacitance	22 pF
f_{PD}	Phase Detector Frequency	1 MHz
f_{OSC}	OSCin Frequency	100 MHz
BW	Loop Bandwidth	31.1 kHz
PM	Phase Margin	59.6 degrees
Gamma	Gamma	0.9
T3/T1	T3/T1 Ratio	177.1%
C1_RF	Loop Filter Components	270 pF
C2_RF		10 nF
C3_RF		1 nF
C4_RF		Open
R2_RF		1.8 Ω
R3_RF		820 Ω
R4_RF		0 Ω

10.2.2 Detailed Design Procedure

The loop filter design is key and involves trade-offs between lock time, phase noise, and spurs. The TI website has references and design and simulation tools that can be used to design the loop filter and simulate the performance.

10.2.3 Application Curves

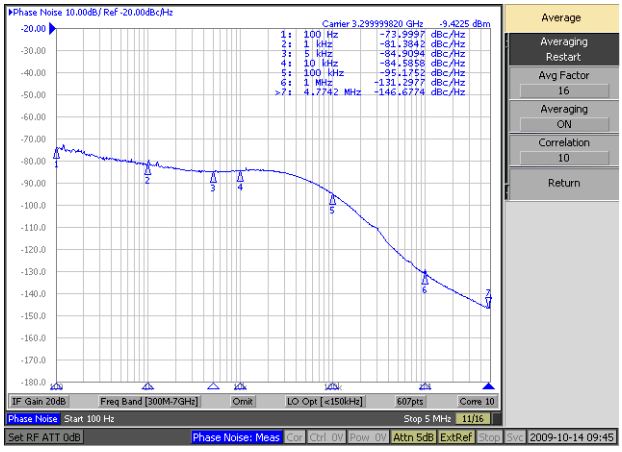


Figure 34. Phase Noise

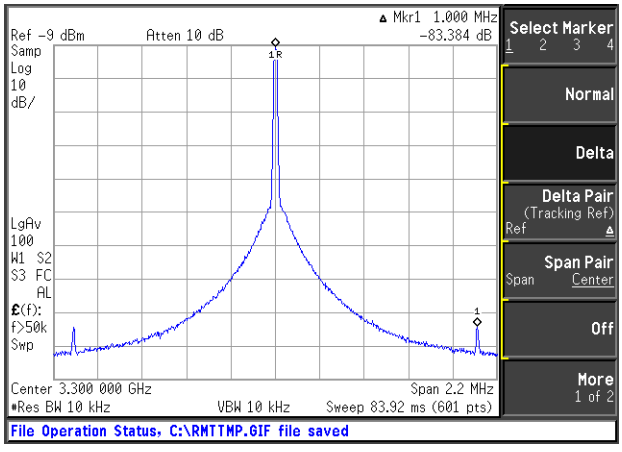


Figure 35. Phase Detector Spurs

11 Power Supply Recommendations

Low-noise regulators are generally recommended for the supply pins. It is acceptable to have one regulator supply the part, although it is best to implement individual bypassing as shown in the *Layout Guidelines* for the best spur performance. The charge-pump pins are typically the most sensitive to supply noise, but the external VCO used with this device is likely to be orders of magnitude more sensitive.

12 Layout

12.1 Layout Guidelines

In general, there are two cases for layout:

1. *Use as a single PLL:* In this case, all power supply pins must be connected, but for those on the unused PLL, bypassing is not necessary, and they can be shorted together. Leave unused outputs unconnected, and do not ground them.
2. *Use as a dual PLL:* In this case, supply coupling is much more critical as there can be crosstalk between the two PLLs. There must be isolation in the form of resistors or inductors between the charge-pump supply pins, and decoupling capacitors are more important.

12.2 Layout Example

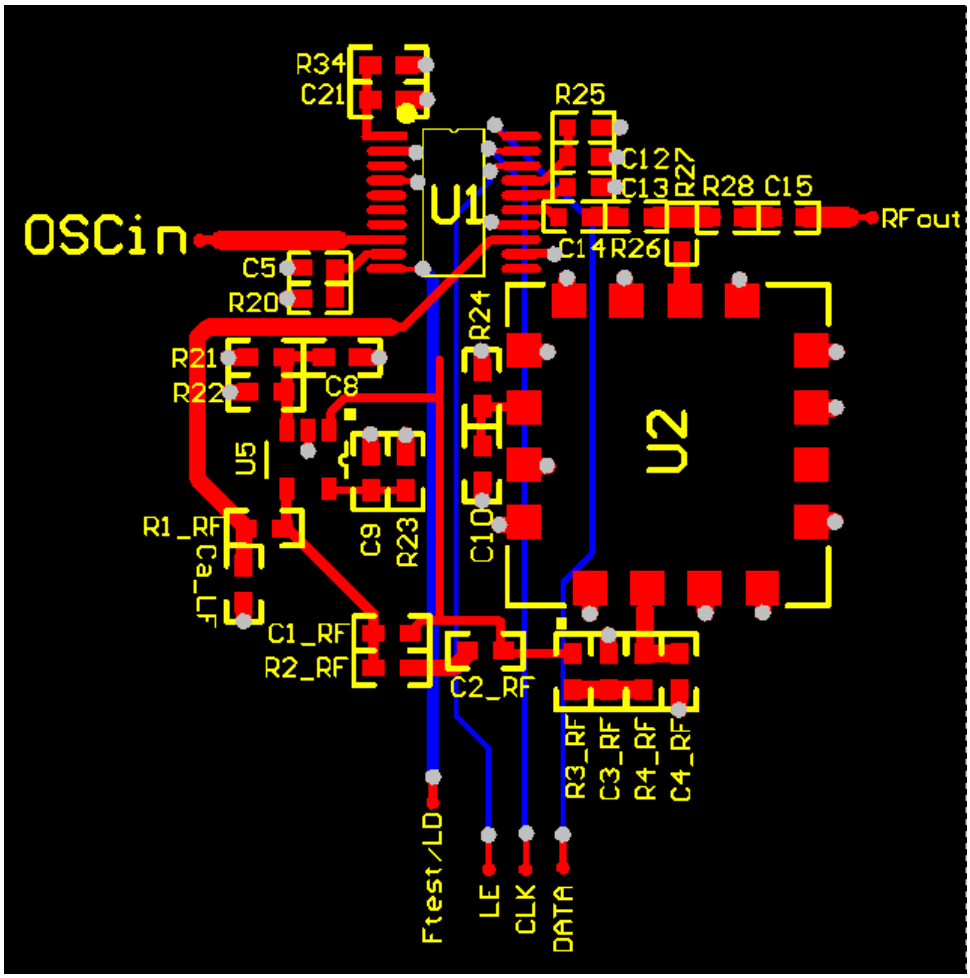


Figure 36. Layout Example

13 Device and Documentation Support

13.1 Device Support

13.1.1 Device Nomenclature

13.1.1.1 List of Definitions

f_{COMP}: RF or IF phase detector comparison frequency

Fin: RF or IF input frequency

A: RF_A or IF_A counter value

B: RF_B or IF_B counter value

P: Preset modulus of the dual modulus prescaler
LMX2430 RF synthesizer: P = 8 or 16
LMX2433 RF synthesizer: P = 8 or 16
LMX2434 RF synthesizer: P = 16 or 32
LMX243x IF synthesizer: P = 8 or 16

13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 42. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LMX2430	Click here	Click here	Click here	Click here	Click here
LMX2433	Click here	Click here	Click here	Click here	Click here
LMX2434	Click here	Click here	Click here	Click here	Click here

13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

PLLatinum, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMX2430SLEX/NOPB	Active	Production	ULGA (NPE) | 20	2500 | LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-40 to 85	X2430 SLE
LMX2430SLEX/NOPB.A	Active	Production	ULGA (NPE) | 20	2500 | LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-40 to 85	X2430 SLE
LMX2430TM/NOPB	Active	Production	TSSOP (PW) | 20	73 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMX2430 TM>D
LMX2430TM/NOPB.A	Active	Production	TSSOP (PW) | 20	73 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMX2430 TM>D
LMX2430TMX/NOPB	Active	Production	TSSOP (PW) | 20	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMX2430 TM>D
LMX2430TMX/NOPB.A	Active	Production	TSSOP (PW) | 20	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMX2430 TM>D
LMX2433SLEX/NOPB	Active	Production	ULGA (NPE) | 20	2500 | LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-40 to 85	X2433 SLE
LMX2433SLEX/NOPB.A	Active	Production	ULGA (NPE) | 20	2500 | LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-40 to 85	X2433 SLE
LMX2434SLEX/NOPB	Active	Production	ULGA (NPE) | 20	2500 | LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-40 to 85	X2434 SLE
LMX2434SLEX/NOPB.A	Active	Production	ULGA (NPE) | 20	2500 | LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-40 to 85	X2434 SLE

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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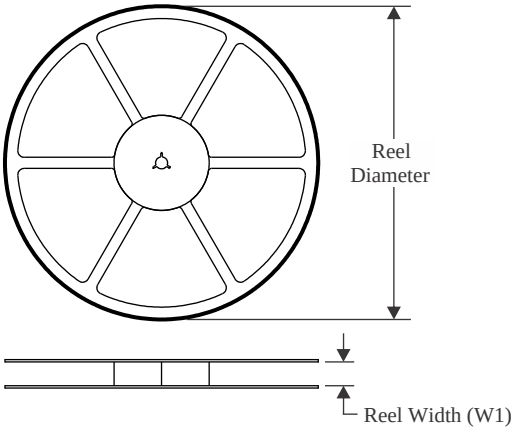
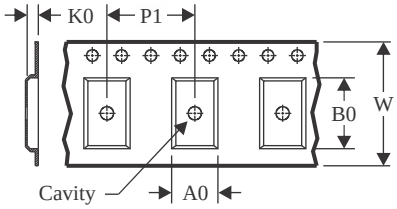
TAPE AND REEL INFORMATION

REEL DIMENSIONS

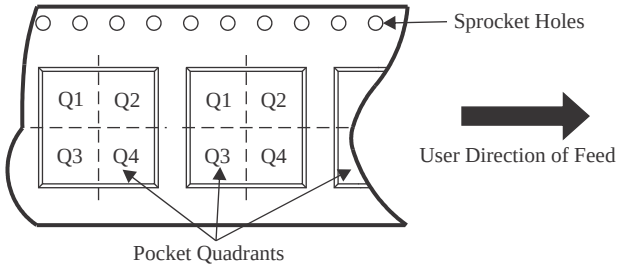


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

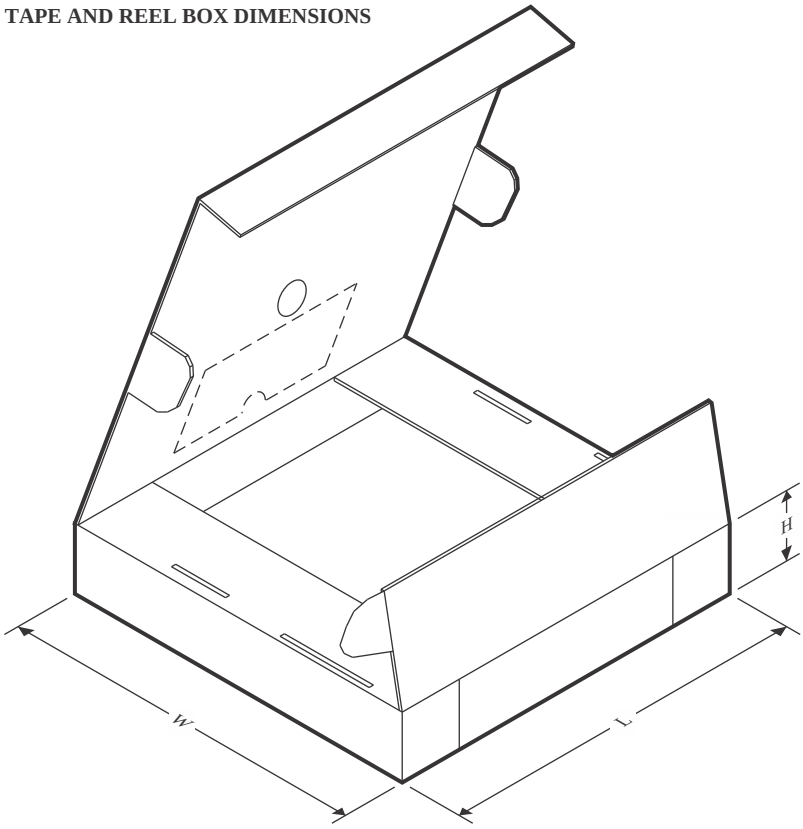
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMX2430SLEX/NOPB	ULGA	NPE	20	2500	330.0	12.4	3.8	3.8	1.6	8.0	12.0	Q1
LMX2430TMX/NOPB	TSSOP	PW	20	2500	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
LMX2433SLEX/NOPB	ULGA	NPE	20	2500	330.0	12.4	3.8	3.8	1.6	8.0	12.0	Q1
LMX2434SLEX/NOPB	ULGA	NPE	20	2500	330.0	12.4	3.8	3.8	1.6	8.0	12.0	Q1

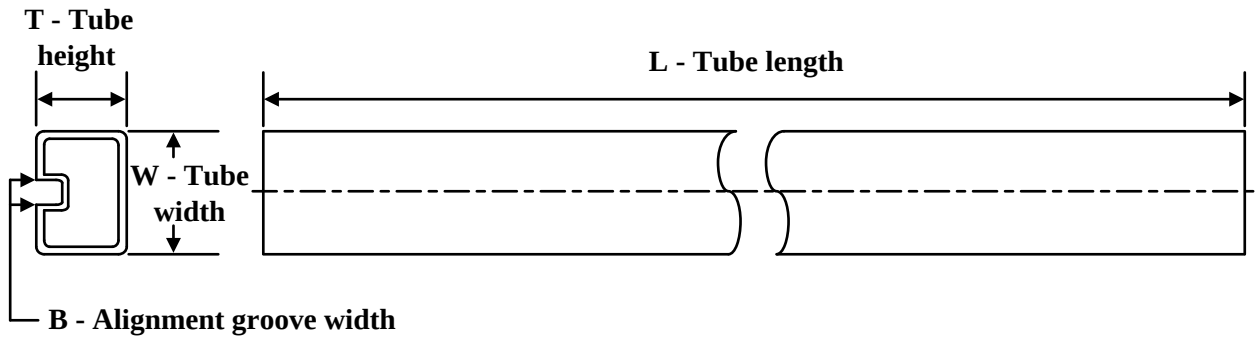
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

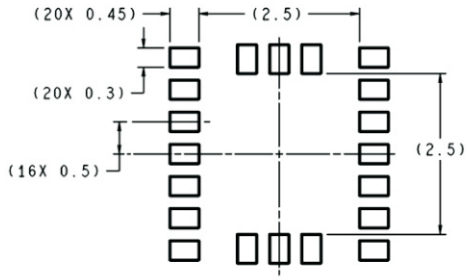
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMX2430SLEX/NOPB	ULGA	NPE	20	2500	367.0	367.0	35.0
LMX2430TMX/NOPB	TSSOP	PW	20	2500	367.0	367.0	35.0
LMX2433SLEX/NOPB	ULGA	NPE	20	2500	367.0	367.0	35.0
LMX2434SLEX/NOPB	ULGA	NPE	20	2500	367.0	367.0	35.0

TUBE



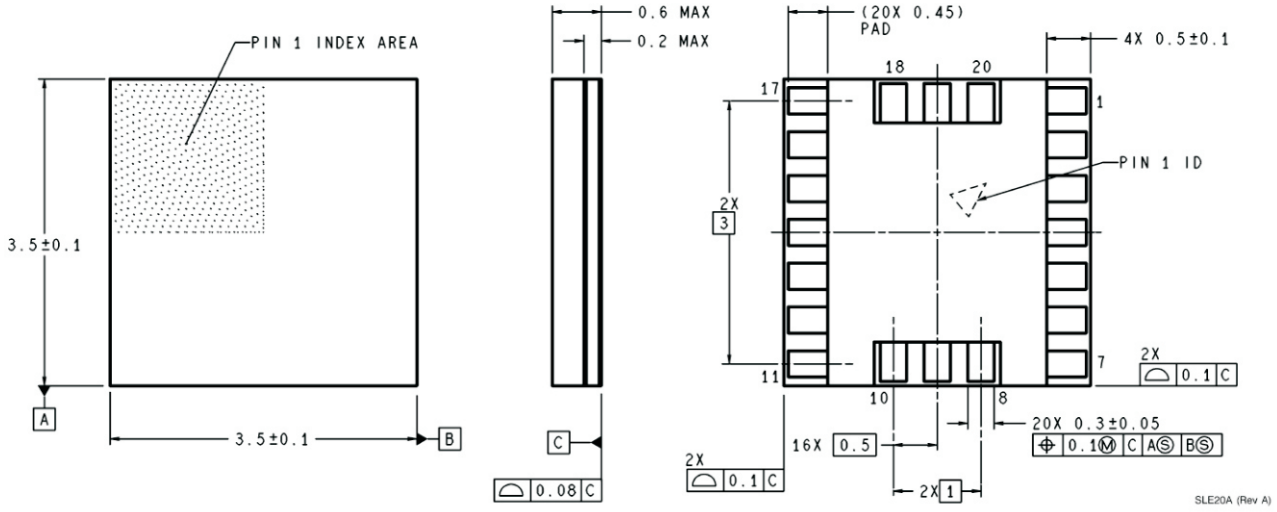
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMX2430TM/NOPB	PW	TSSOP	20	73	495	8	2514.6	4.06
LMX2430TM/NOPB.A	PW	TSSOP	20	73	495	8	2514.6	4.06



RECOMMENDED LAND PATTERN
1:1 RATIO WITH PACKAGE SOLDER PADS

DIMENSIONS ARE IN MILLIMETERS

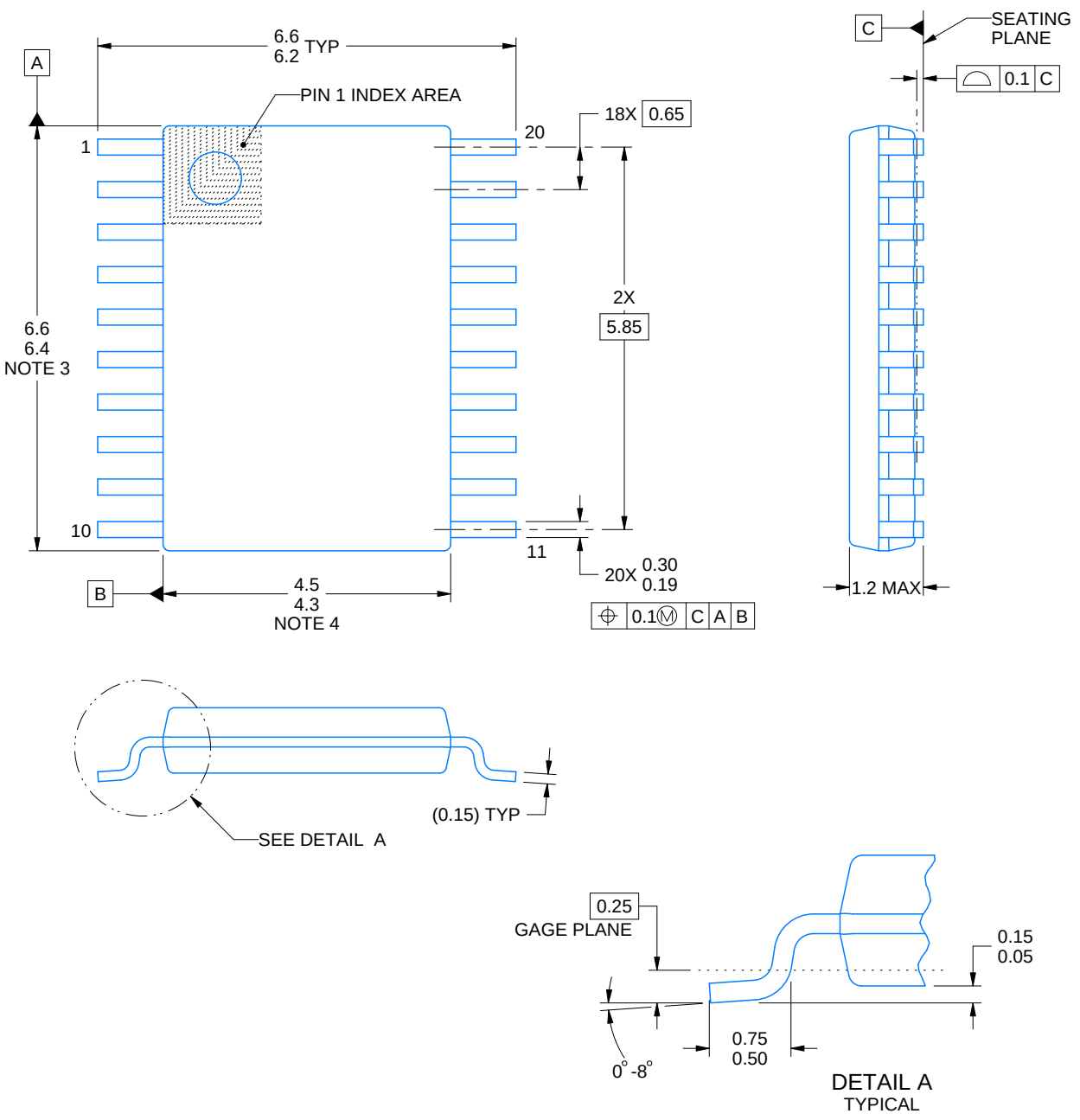


PACKAGE OUTLINE

PW0020A

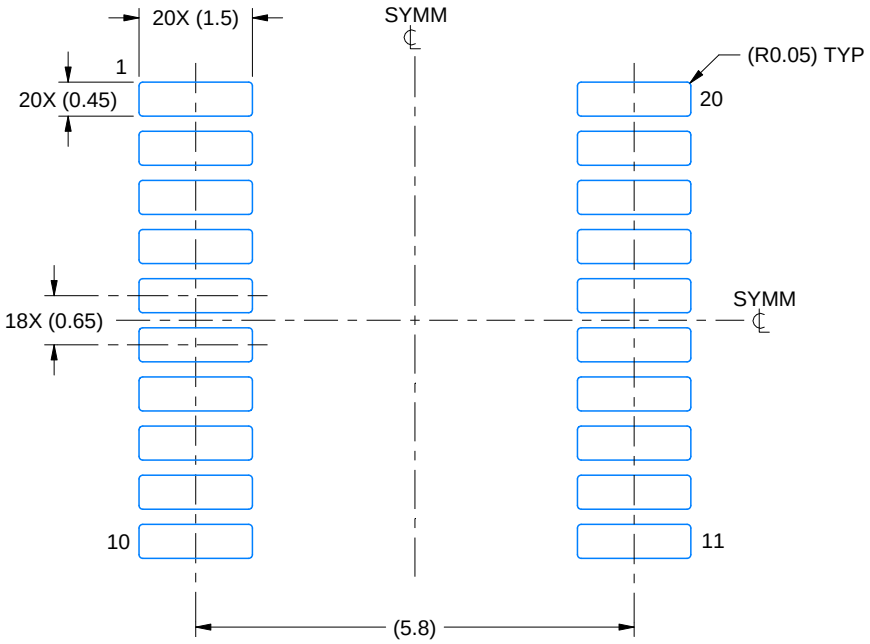
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



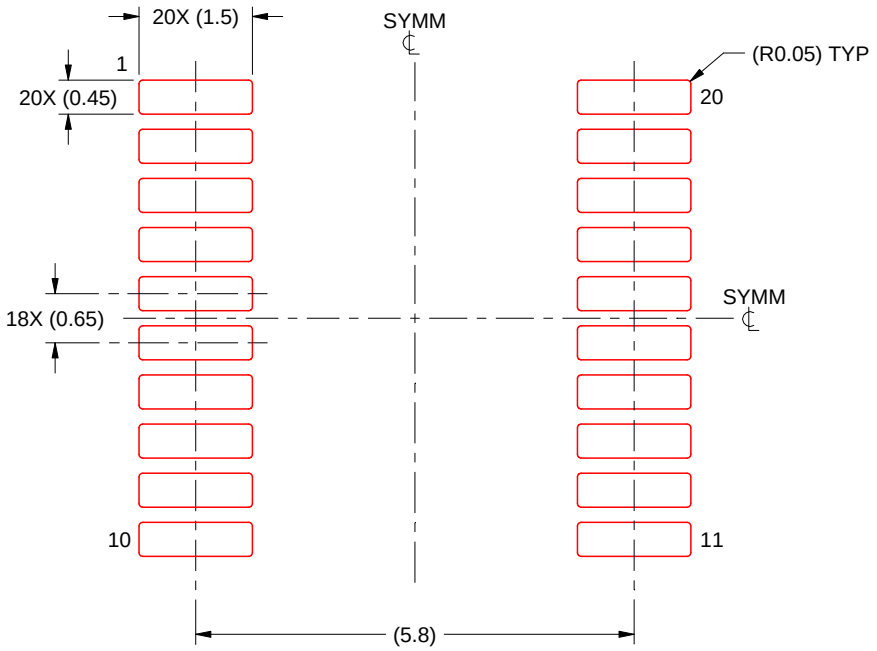
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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