LMV716 5 MHz, Low Noise, RRO, Dual Operational Amplifier with CMOS Input

Check for Samples: LMV716

FEATURES

- **(Typical Values, V^+ = 3.3V, T_A = 25°C, unless Otherwise Specified)**
- **Input Noise Voltage 12.8 nV/√Hz**
- **Input Bias Current 0.6 pA**
- **Offset Voltage 1.6 mV**
- **CMRR 80 dB**
- **Open Loop Gain 122 dB**
- **Rail-to-Rail Output**
- **GBW 5 MHz**
- **Slew Rate 5.8 V/µs**
- **Supply Current 1.6 mA**
- **Supply Voltage Range 2.7V to 5V**
- **Operating Temperature −40°C to 85°C**
- **8-pin VSSOP Package**

APPLICATIONS

- **Active Filters**
- **Transimpedance Amplifiers**
- **Audio Preamp**
- **HDD Vibration Cancellation Circuitry**

DESCRIPTION

The LMV716 is a dual operational amplifier with both low supply voltage and low supply current, making it ideal for portable applications. The LMV716 CMOS input stage drives the I_{BIAS} current down to 0.6 pA; this coupled with the low noise voltage of 12.8 nV/√Hz makes the LMV716 perfect for applications requiring active filters, transimpedance amplifiers, and HDD vibration cancellation circuitry.

Along with great noise sensitivity, small signal applications will benefit from the large gain bandwidth of 5 MHz coupled with the minimal supply current of 1.6 mA and a slew rate of 5.8 V/µs.

The LMV716 provides rail-to-rail output swing into heavy loads. The input common-mode voltage range includes ground, which is ideal for ground sensing applications.

The LMV716 has a supply voltage spanning 2.7V to 5V and is offered in an 8-pin VSSOP package that functions across the wide temperature range of −40°C to 85°C. This small package makes it possible to place the LMV716 next to sensors, thus reducing external noise pickup.

Typical Application Circuit

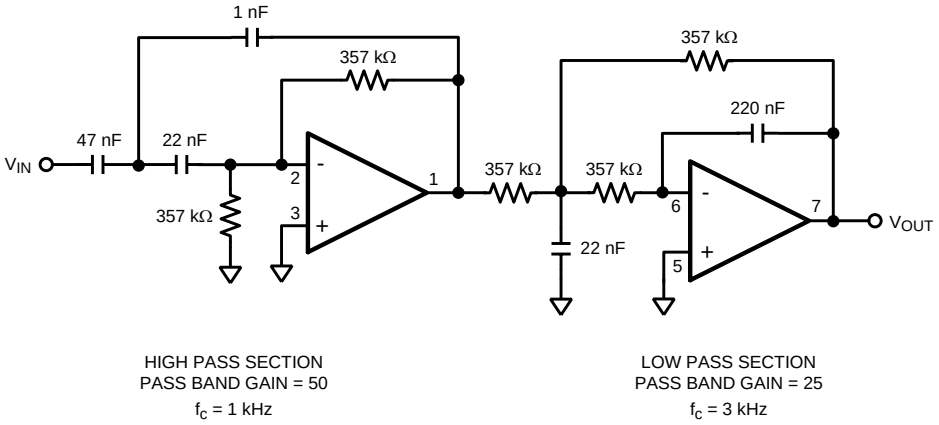


Figure 1. High Gain Band Pass Filter

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

ESD Tolerance (3)	
Human Body Model	2000V
Machine Model	200V
Supply Voltage ($V^+ - V^-$)	5.5V
Storage Temperature Range	−65°C to 150°C
Junction Temperature (4)	150°C max
Mounting Temperature	
Infrared or Convection (20 sec)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human Body Model is 1.5 kΩ in series with 100 pF. Machine Model is 0Ω in series with 100 pF.
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)}-T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Operating Ratings (1)

Supply Voltage	2.7V to 5V
Temperature Range	−40°C to 85°C
Thermal Resistance (θ_{JA})	
8-Pin VSSOP	195°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.

3.3V Electrical Characteristics (1)

Unless otherwise specified, all limits are ensured for T_J = 25°C, V^+ = 3.3V, V^- = 0V. V_{CM} = V^+/2. **Boldface** limits apply at the temperature extremes (2).

Symbol	Parameter	Condition	Min (3)	Typ (4)	Max (3)	Units
V_{OS}	Input Offset Voltage	V_{CM} = 1V		1.6	5 **6**	mV
I_B	Input Bias Current	(5)		0.6	115 **130**	pA
I_{OS}	Input Offset Current			1		pA
CMRR	Common Mode Rejection Ratio	0 ≤ V_{CM} ≤ 2.1V	60 **50**	80		dB
PSRR	Power Supply Rejection Ratio	2.7V ≤ V^+ ≤ 5V, V_{CM} = 1V	70 **60**	82		dB
CMVR	Common Mode Voltage Range	For CMRR ≥ 50 dB	−0.2		2.2	V
A_{VOL}	Open Loop Voltage Gain	Sourcing R_L = 10 kΩ to V^+/2, V_O = 1.65V to 2.9V	80 **76**	122		dB
		Sinking R_L = 10 kΩ to V^+/2, V_O = 0.4V to 1.65V	80 **76**	122		
		Sourcing R_L = 600Ω to V^+/2, V_O = 1.65V to 2.8V	80 **76**	105		
		Sinking R_L = 600Ω to V^+/2, V_O = 0.5V to 1.65V	80 **76**	112		
V_O	Output Swing High	R_L = 10 kΩ to V^+/2	3.22 **3.17**	3.29		V
		R_L = 600Ω to V^+/2	3.12 **3.07**	3.22		
	Output Swing Low	R_L = 10 kΩ to V^+/2		0.03	0.12 **0.16**	
		R_L = 600Ω to V^+/2		0.07	0.23 **0.27**	
I_{OUT}	Output Current	Sourcing, V_O = 0V	20 **15**	31		mA
		Sinking, V_O = 3.3V	30 **25**	41		
I_S	Supply Current	V_{CM} = 1V		1.6	2.0 **3**	mA
SR	Slew Rate	(6)		5.8		V/µs
GBW	Gain Bandwidth			5		MHz
e_n	Input-Referred Voltage Noise	f = 1 kHz		12.8		nV/√Hz
i_n	Input-Referred Current Noise	f = 1 kHz		0.01		pA/√Hz

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factor testing conditions result in very limited self-heating of the device such that T_J = T_A. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A. Absolute Maximum Ratings indicate junction temperature limits beyond which the device maybe permanently degraded, either mechanically or electrically.
(2) Boldface limits apply to temperature range of −40°C to 85°C.
(3) All limits are specified by testing or statistical analysis.
(4) Typical values represent the most likely parametric norm.
(5) Input bias current is specified by design.
(6) Number specified is the lower of the positive and negative slew rates.

CONNECTION DIAGRAM

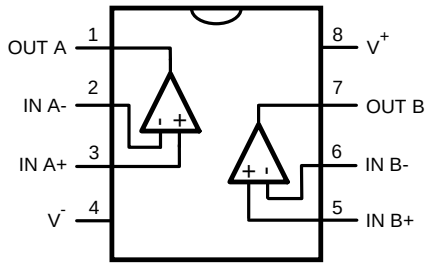
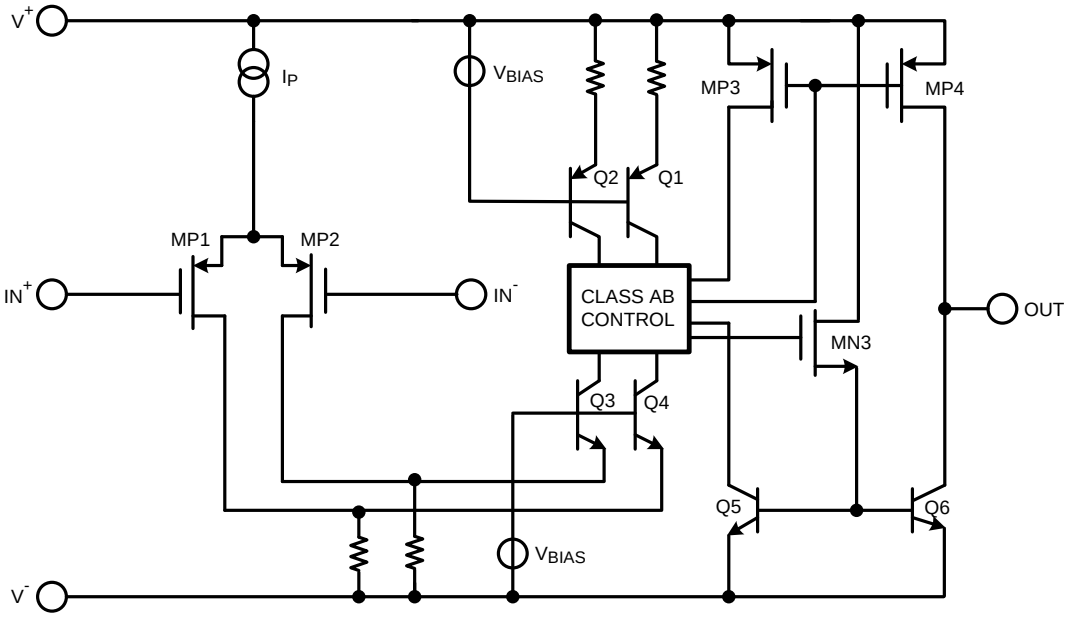


Figure 2. Top View - 8-Pin VSSOP

Simplified Schematic



Typical Performance Characteristics

Unless otherwise specified, V^+ 3.3V, T_J = 25°C.

Supply Current vs. Supply Voltage

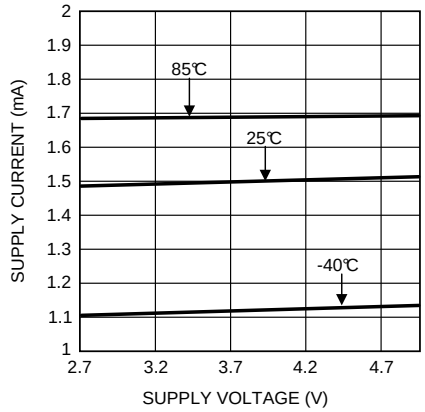


Figure 3.

Offset Voltage vs. Common Mode

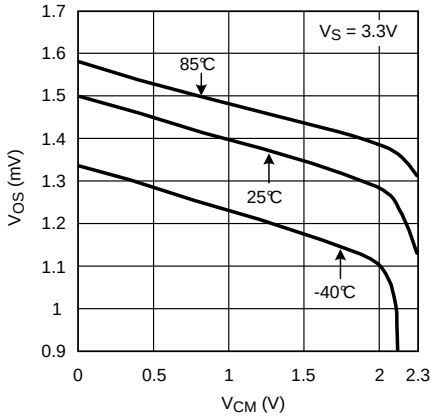


Figure 4.

Input Bias Current vs. Common Mode

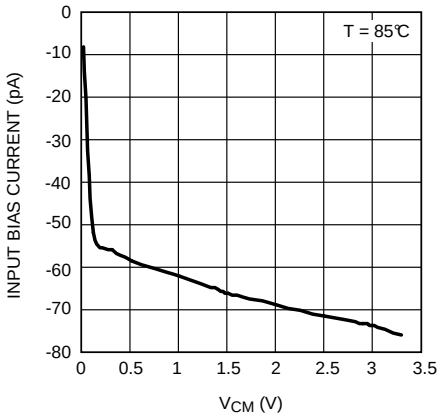


Figure 5.

Input Bias Current vs. Common Mode

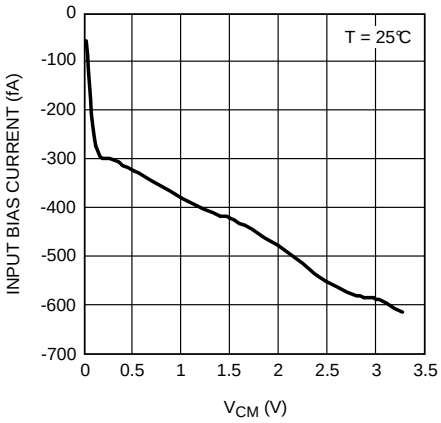


Figure 6.

Input Bias Current vs. Common Mode

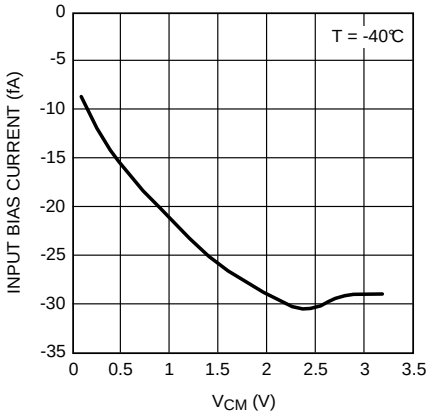


Figure 7.

Output Positive Swing vs. Supply Voltage

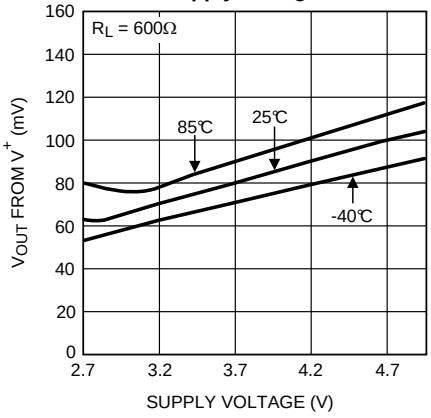


Figure 8.

Typical Performance Characteristics (continued)

Unless otherwise specified, V^+ 3.3V, T_J = 25°C.

Output Negative Swing vs. Supply Voltage

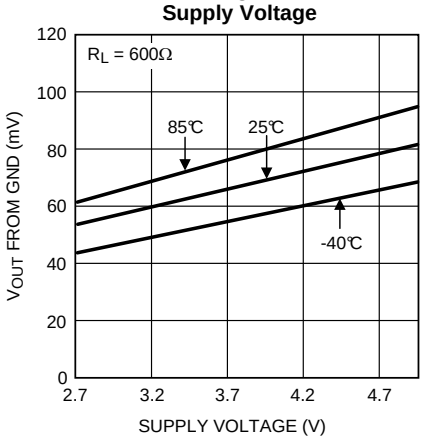


Figure 9.

Output Positive Swing vs. Supply Voltage

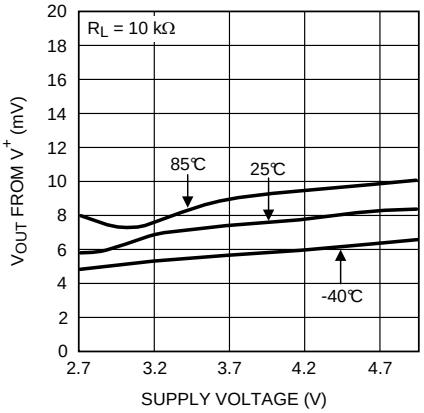


Figure 10.

Output Negative Swing vs. Supply Voltage

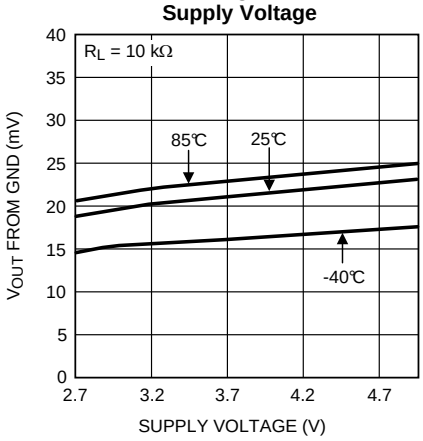


Figure 11.

Sinking Current vs. V_{OUT}

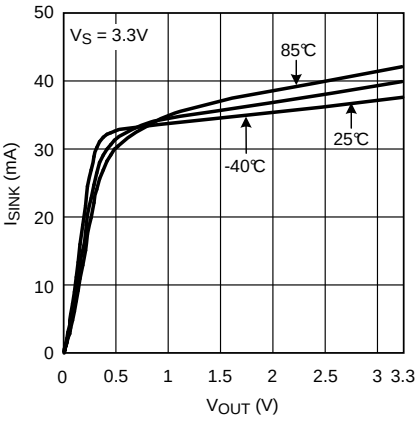


Figure 12.

Sourcing Current vs. V_{OUT}

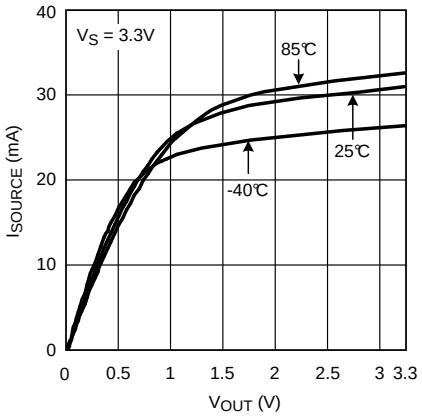


Figure 13.

PSRR vs. Frequency

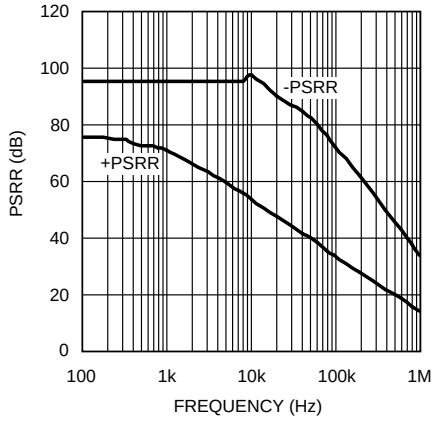


Figure 14.

Typical Performance Characteristics (continued)

Unless otherwise specified, V^+ 3.3V, T_J = 25°C.

CMRR vs. Frequency

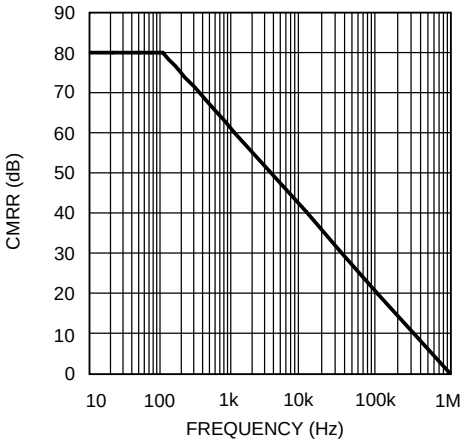


Figure 15.

Crosstalk Rejection

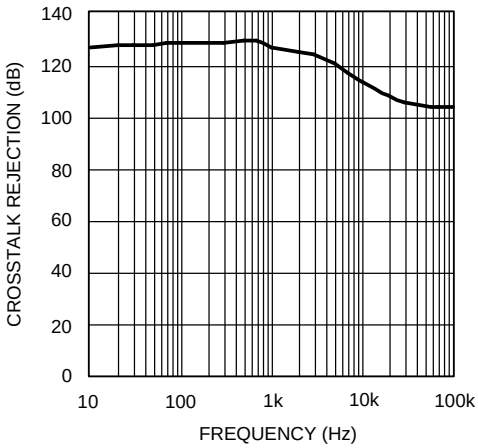


Figure 16.

Inverting Large Signal Pulse Response

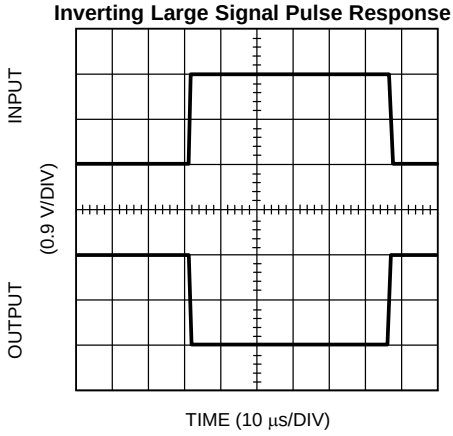


Figure 17.

Inverting Small Signal Pulse Response

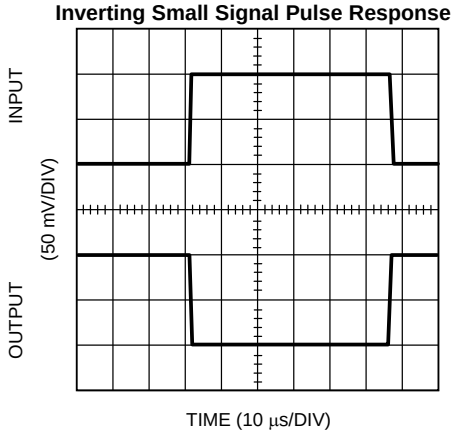


Figure 18.

Non-Inverting Large Signal Pulse Response

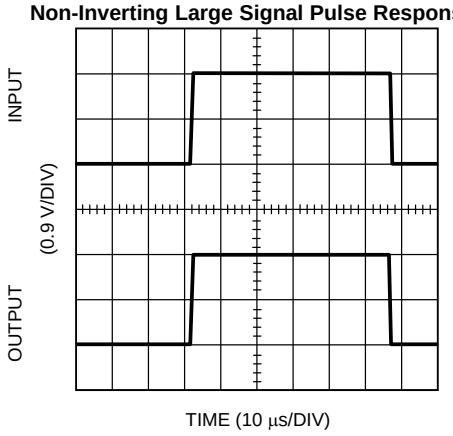


Figure 19.

Non-Inverting Small Signal Pulse Response

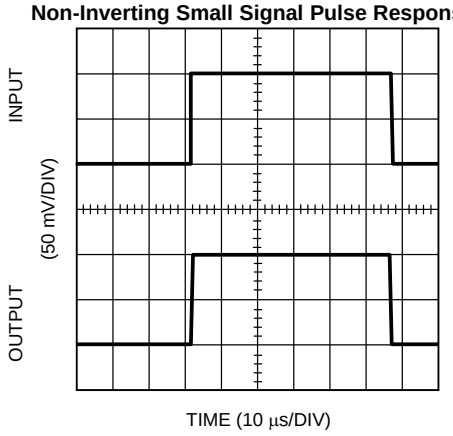


Figure 20.

Typical Performance Characteristics (continued)

Unless otherwise specified, V^+ 3.3V, T_J = 25°C.

Open Loop Frequency vs. R_L

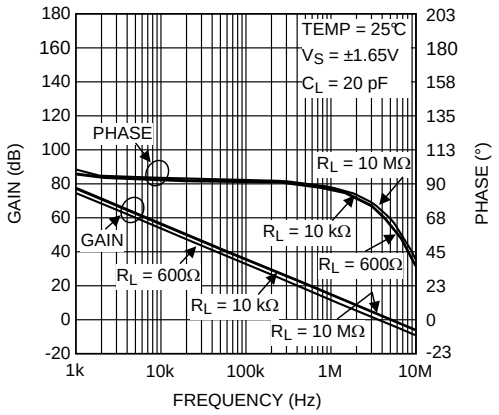


Figure 21.

Open Loop Frequency Response over Temperature

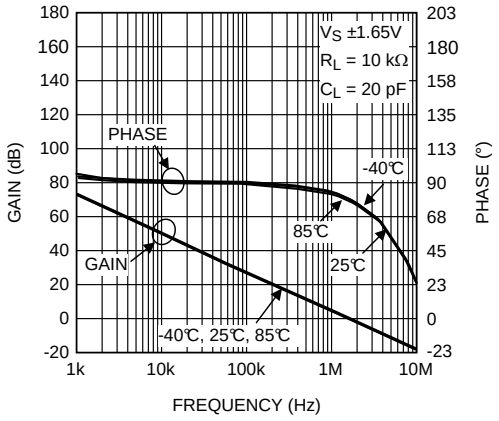


Figure 22.

Open Loop Frequency Response vs. C_L

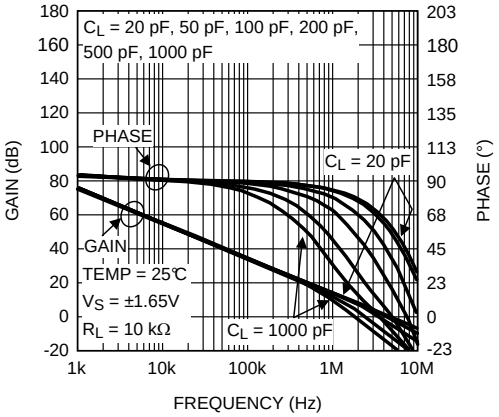


Figure 23.

Open Loop Frequency Response vs. C_L

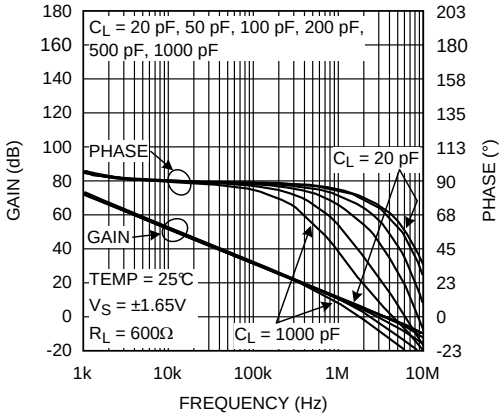


Figure 24.

Voltage Noise vs. Frequency

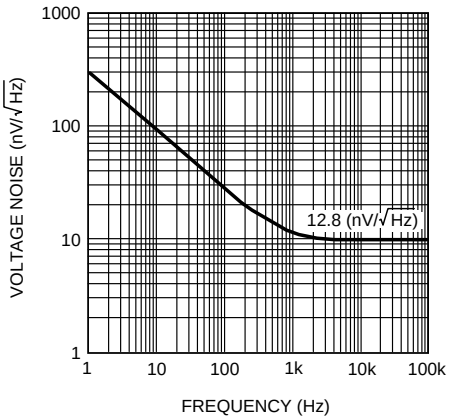


Figure 25.

APPLICATION INFORMATION

With the low supply current of only 1.6 mA, the LMV716 offers users the ability to maximize battery life. This makes the LMV716 ideal for battery powered systems. The LMV716's rail-to-rail output swing provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

CAPACITIVE LOAD TOLERANCE

The LMV716, when in a unity-gain configuration, can directly drive large capacitive loads in unity-gain without oscillation. The unity-gain follower is the most sensitive configuration to capacitive loading; direct capacitive loading reduces the phase margin of amplifiers. The combination of the amplifier's output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation. To drive a heavier capacitive load, the circuit in Figure 26 can be used.

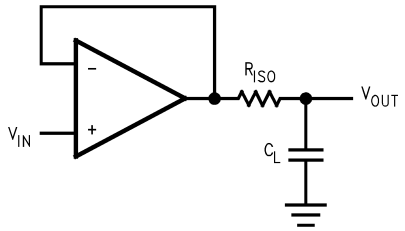


Figure 26. Indirectly Driving a Capacitive Load using Resistive Isolation

In Figure 26, the isolation resistor R_{ISO} and the load capacitor C_L form a pole to increase stability by adding more phase margin to the overall system. The desired performance depends on the value of R_{ISO}. The bigger the R_{ISO} resistor value, the more stable V_{OUT} will be.

The circuit in Figure 27 is an improvement to the one in Figure 26 because it provides DC accuracy as well as AC stability. If there were a load resistor in Figure 26, the output would be voltage divided by R_{ISO} and the load resistor. Instead, in Figure 27, R_F provides the DC accuracy by using feed-forward techniques to connect V_{IN} to R_L. Due to the input bias current of the LMV716, the designer must be cautious when choosing the value of R_F. C_F and R_{ISO} serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop. Increased capacitive drive is possible by increasing the value of C_F. This in turn will slow down the pulse response.

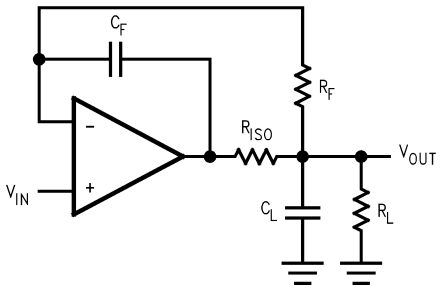


Figure 27. Indirectly Driving a Capacitive Load with DC Accuracy

DIFFERENCE AMPLIFIER

The difference amplifier allows the subtraction of two voltages or, as a special case, the cancellation of a signal common to two inputs. It is useful as a computational amplifier in making a differential to single-ended conversion or in rejecting a common mode signal.

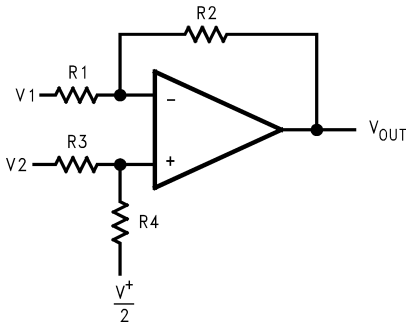


Figure 28. Difference Amplifier

$$V_{OUT} = \left(\frac{R1 + R2}{R3 + R4}\right)\frac{R4}{R1}V_2 - \frac{R2}{R1}V_1 + \left(\frac{R1 + R2}{R3 + R4}\right)\frac{R3}{R1} \bullet \frac{V^+}{2}$$

for R1 = R3 and R2 = R4

$$V_{OUT} = \frac{R2}{R1}\left(V_2 - V_1\right) + \frac{V^+}{2} \quad (1)$$

SINGLE-SUPPLY INVERTING AMPLIFIER

There may be cases where the input signal going into the amplifier is negative. Because the amplifier is operating in single supply voltage, a voltage divider using R_3 and R_4 is implemented to bias the amplifier so the inverting input signal is within the input common voltage range of the amplifier. The capacitor C_1 is placed between the inverting input and resistor R_1 to block the DC signal going into the AC signal source, V_{IN}. The values of R_1 and C_1 affect the cutoff frequency, fc = ½π R_1C_1. As a result, the output signal is centered around mid-supply (if the voltage divider provides $V^+/2$ at the non-inverting input). The output can swing to both rails, maximizing the signal-to-noise ratio in a low voltage system.

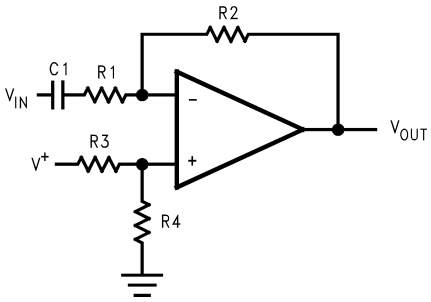


Figure 29. Single-supply Inverting Amplifier

$$V_{OUT} = -\frac{R2}{R1}V_{IN} \quad (2)$$

INSTRUMENTATION AMPLIFIER

Measurement of very small signals with an amplifier requires close attention to the input impedance of the amplifier, the overall signal gain from both inputs to the output, as well as, the gain from each input to the output. This is because we are only interested in the difference of the two inputs and the common signal is considered noise. A classic solution is an instrumentation amplifier. Instrumentation amplifiers have a finite, accurate, and stable gain. Also they have extremely high input impedances and very low output impedances. Finally they have an extremely high CMRR so that the amplifier can only respond to the differential signal.

Three-Op-Amp Instrumentation Amplifier

A typical instrumentation amplifier is shown in Figure 30.

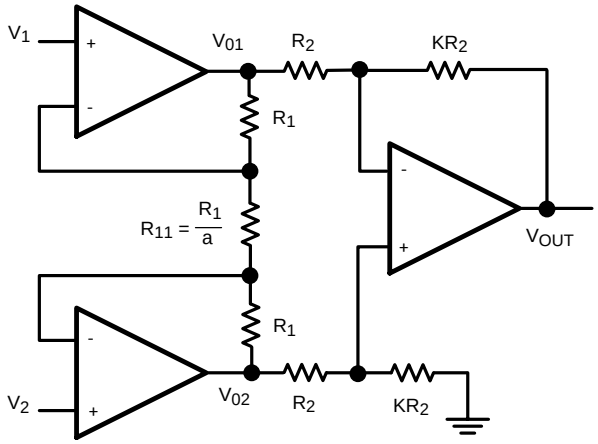


Figure 30. Three-Op-Amp Instrumentation Amplifier

There are two stages in this configuration. The last stage, the output stage, is a differential amplifier. In an ideal case the two amplifiers of the first stage, the input stage, would be set up as buffers to isolate the inputs. However they cannot be connected as followers due to the mismatch of real amplifiers. The circuit in Figure 30 utilizes a balancing resistor between the two amplifiers to compensate for this mismatch. The product of the two stages of gain will be the gain of the instrumentation amplifier circuit. Ideally, the CMRR should be infinite. However the output stage has a small non-zero common mode gain which results from resistor mismatch.

In the input stage of the circuit, current is the same across all resistors. This is due to the high input impedance and low input bias current of the LMV716. With the node equations we have:

$$\text{GIVEN: } I_{R_1} = I_{R_{11}} \tag{3}$$

By Ohm's Law:

$$\begin{aligned} V_{O1} - V_{O2} &= (2R_1 + R_{11})\, I_{R_{11}} \\ &= (2a + 1)\, R_{11} \bullet I_{R_{11}} \\ &= (2a + 1)\, V_{R_{11}} \end{aligned} \tag{4}$$

However:

$$V_{R_{11}} = V_1 - V_2 \tag{5}$$

So we have:

$$V_{O1} - V_{O2} = (2a + 1)\,(V_1 - V_2) \tag{6}$$

Now looking at the output of the instrumentation amplifier:

$$\begin{aligned} V_O &= \frac{KR_2}{R_2}\,(V_{O2} - V_{O1}) \\ &= -K\,(V_{O1} - V_{O2}) \end{aligned} \tag{7}$$

Substituting from Equation 6:

$$V_O = -K\,(2a + 1)\,(V_1 - V_2) \tag{8}$$

This shows the gain of the instrumentation amplifier to be:

$$-K(2a+1) \tag{9}$$

Typical values for this circuit can be obtained by setting: a = 12 and K = 4. This results in an overall gain of −100.

Three LMV716 amplifiers are used along with 1% resistors to minimize resistor mismatch. Resistors used to build the circuit are: R_1 = 21.6 kΩ, R_{11} = 1.8 kΩ, R_2 = 2.5 kΩ with K = 40 and a = 12. This results in an overall gain of −K(2a+1) = −1000.

Two-Op-Amp Instrumentation Amplifier

A two-op-amp instrumentation amplifier can also be used to make a high-input impedance DC differential amplifier Figure 31). As in the three op amp circuit, this instrumentation amplifier requires precise resistor matching for good CMRR. R_4 should be equal to R_1, and R_3 should equal R_2.

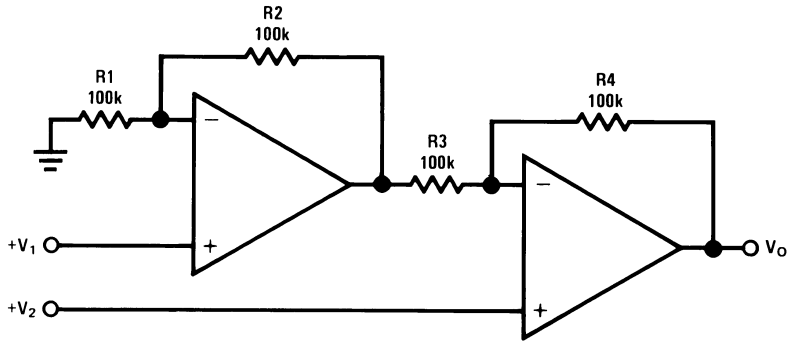


Figure 31. Two-Op-Amp Instrumentation Amplifier

$$V_O = \left(1 + \frac{R4}{R3}\right)(V_2 - V_1), \text{ where R1 = R4 and R2 = R3}$$

$$\text{As shown: } V_O = 2(V_2 - V_1) \tag{10}$$

ACTIVE FILTERS

Active filters are circuits with amplifiers, resistors, and capacitors. The use of amplifiers instead of inductors, which are used in passive filters, enhances the circuit performance while reducing the size and complexity of the filter. The simplest active filters are designed using an inverting op amp configuration where at least one reactive element has been added to the configuration. This means that the op amp will provide "frequency-dependent" amplification, since reactive elements are frequency dependent devices.

Low Pass Filter

The following shows a very simple low pass filter.

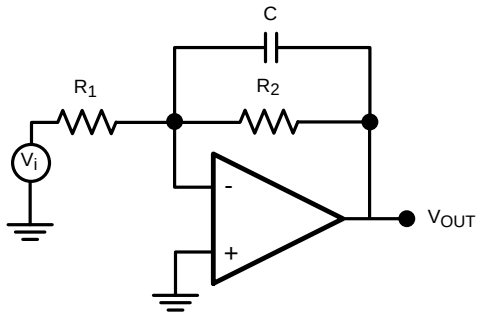


Figure 32. Low Pass Filter

The transfer function can be expressed as follows:

By KCL:

$$\frac{-V_i}{R_1} - \frac{V_O}{\left[\frac{1}{jwc}\right]} - \frac{V_O}{R_2} = O \tag{11}$$

Simplifying this further results in:

$$V_O = \frac{-R_2}{R_1}\left[\frac{1}{jwcR_2 + 1}\right] V_i \tag{12}$$

or

$$\frac{V_O}{V_i} = \frac{-R_2}{R_1}\left[\frac{1}{jwcR_2 + 1}\right] \tag{13}$$

Now, substituting ω=2πf, so that the calculations are in f(Hz) rather than in ω(rad/s), and setting the DC gain $\left[\frac{-R_2}{R_1} = H_O\right]$ and $H = \frac{V_O}{V_i}$

$$H = H_O\left[\frac{1}{j2\pi fcR_2 + 1}\right] \tag{14}$$

set: $f_O = \frac{1}{2\pi R_1 C}$

$$H = H_O\left[\frac{1}{1 + j\,(f/f_0)}\right] \tag{15}$$

Low pass filters are known as lossy integrators because they only behave as integrators at higher frequencies. The general form of the bode plot can be predicted just by looking at the transfer function. When the f/f_O ratio is small, the capacitor is, in effect, an open circuit and the amplifier behaves at a set DC gain. Starting at f_O, which is the −3 dB corner, the capacitor will have the dominant impedance and hence the circuit will behave as an integrator and the signal will be attenuated and eventually cut. The bode plot for this filter is shown in Figure 33.

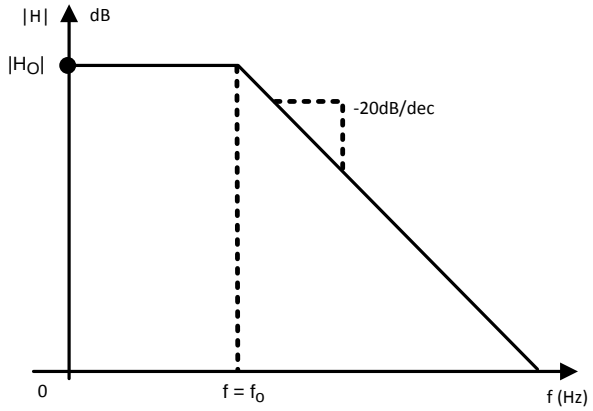


Figure 33. Low Pass Filter Transfer Function

High Pass Filter

The transfer function of a high pass filter can be derived in much the same way as the previous example. A typical first order high pass filter is shown below:

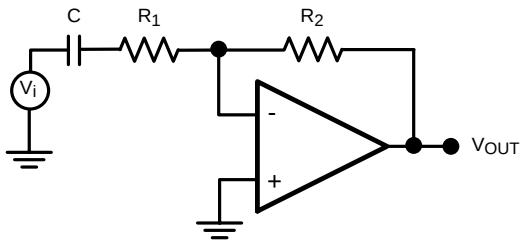


Figure 34. High Pass Filter

Writing the KCL for this circuit :

(V_1 denotes the voltage between C and R_1)

$$\frac{V_1 - V_i}{\frac{1}{jwC}} = \frac{V_1 - V^-}{R_1} \tag{16}$$

$$\frac{V^- + V_1}{R_1} = \frac{V^- + V_O}{R_2} \tag{17}$$

Solving these two equations to find the transfer function and using:

$$f_O = \frac{1}{2\pi R_1 C} \tag{18}$$

(high frequency gain) $H_O = \frac{-R_2}{R_1}$ and $H = \frac{V_O}{V_i}$

Which gives:

$$H = H_O \frac{j\,(f/f_O)}{1 + j\,(f/f_O)} \tag{19}$$

Looking at the transfer function, it is clear that when f/f_O is small, the capacitor is open and therefore, no signal is getting to the amplifier. As the frequency increases the amplifier starts operating. At $f = f_O$ the capacitor behaves like a short circuit and the amplifier will have a constant, high frequency gain of H_O. Figure 35 shows the transfer function of this high pass filter.

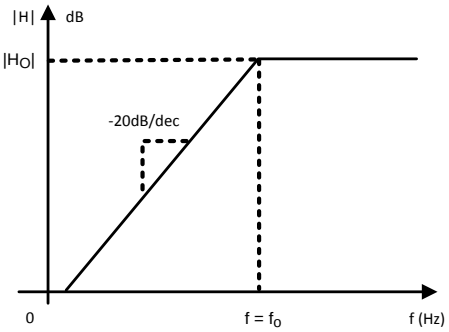


Figure 35. High Pass Filter Transfer Function

Band Pass Filter

Combining a low pass filter and a high pass filter will generate a band pass filter. Figure 36 offers an example of this type of circuit.

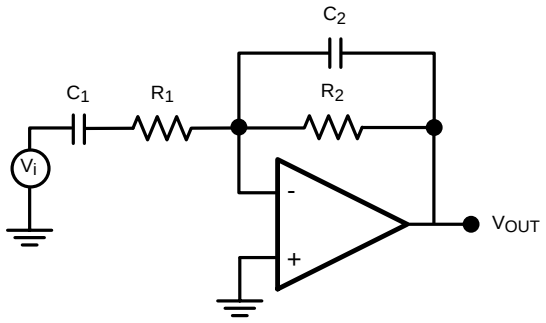


Figure 36. Band Pass Filter

In this network the input impedance forms the high pass filter while the feedback impedance forms the low pass filter. If the designer chooses the corner frequencies so that $f_1 < f_2$, then all the frequencies between, $f_1 \le f \le f_2$, will pass through the filter while frequencies below f_1 and above f_2 will be cut off.

The transfer function can be easily calculated using the same methodology as before and is shown in Figure 37.

$$H = H_O \frac{j\,(f/f_1)}{[1 + j\,(f/f_1)]\;\;[1 + j\,(f/f_2)]} \tag{20}$$

Where

$$f_1 = \frac{1}{2\pi R_1 C_1}$$

$$f_2 = \frac{1}{2\pi R_2 C_2}$$

$$H_O = \frac{-R_2}{R_1} \tag{21}$$

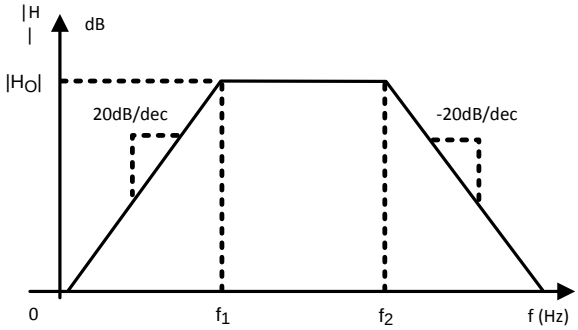


Figure 37. Band Pass Filter Transfer Function

STATE VARIABLE ACTIVE FILTER

State variable active filters are circuits that can simultaneously represent high pass, band pass, and low pass filters. The state variable active filter uses three separate amplifiers to achieve this task. A typical state variable active filter is shown in Figure 38. The first amplifier in the circuit is connected as a gain stage. The second and third amplifiers are connected as integrators, which means they behave as low pass filters. The feedback path from the output of the third amplifier to the first amplifier enables this low frequency signal to be fed back with a

finite and fairly low closed loop gain. This is while the high frequency signal on the input is still gained up by the open loop gain of the first amplifier. This makes the first amplifier a high pass filter. The high pass signal is then fed into a low pass filter. The outcome is a band pass signal, meaning the second amplifier is a band pass filter. This signal is then fed into the third amplifiers input and so, the third amplifier behaves as a simple low pass filter.

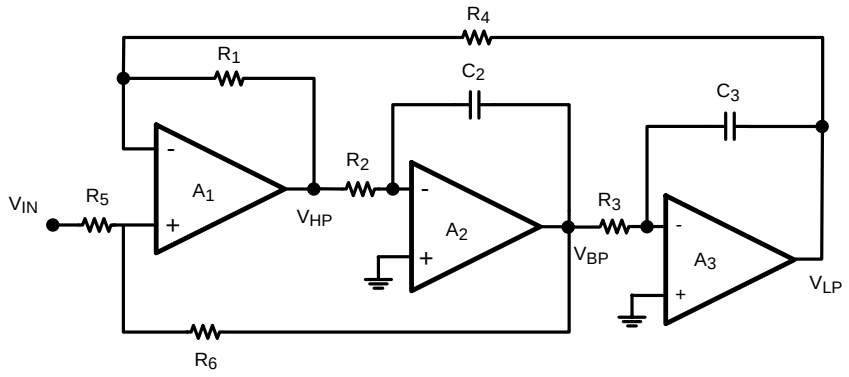
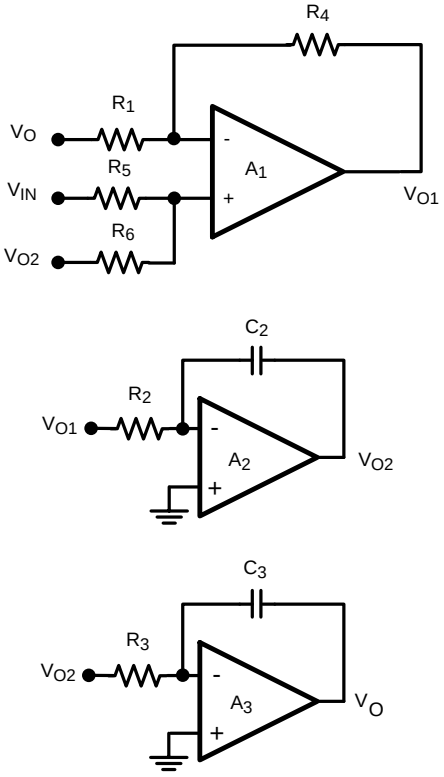


Figure 38. State Variable Active Filter

The transfer function of each filter needs to be calculated. The derivations will be more trivial if each stage of the filter is shown on its own.

The three components are:



For A_1 the relationship between input and output is:

$$V_{O1} = \frac{-R_4}{R_1} V_0 + \left[\frac{R_6}{R_5 + R_6}\right]\left[\frac{R_1 + R_4}{R_1}\right] V_{IN} + \left[\frac{R_5}{R_5 + R_6}\right]\left[\frac{R_1 + R_4}{R_1}\right] V_{O2} \quad (22)$$

This relationship depends on the output of all the filters. The input-output relationship for A_2 can be expressed as:

$$V_{O2} = \frac{-1}{s\,C_2R_2}\ V_{O1} \tag{23}$$

And finally this relationship for A_3 is as follows:

$$V_O = \frac{-1}{s\,C_3R_3}\ V_{O2} \tag{24}$$

Re-arranging these equations, one can find the relationship between V_O and V_{IN} (transfer function of the low pass filter), V_{O1} and V_{IN} (transfer function of the high pass filter), and V_{O2} and V_{IN} (transfer function of the band pass filter) These relationships are as follows:

Low Pass Filter

$$\frac{V_O}{V_{IN}} = \frac{\left[\frac{R_1+R_4}{R_1}\right]\left[\frac{R_6}{R_5+R_6}\right]\left[\frac{1}{C_2C_3R_2R_3}\right]}{s^2 + s\left[\frac{1}{C_2R_2}\right]\left[\frac{R_5}{R_5+R_6}\right]\left[\frac{R_1+R_4}{R_1}\right] + \left[\frac{1}{C_2C_3R_2R_3}\right]} \tag{25}$$

(26)

High Pass Filter

$$\frac{V_{O1}}{V_{IN}} = \frac{s^2\left[\frac{R_1+R_4}{R_1}\right]\left[\frac{R_6}{R_5+R_6}\right]}{s^2 + s\left[\frac{1}{C_2R_2}\right]\left[\frac{R_5}{R_5+R_6}\right]\left[\frac{R_1+R_4}{R_1}\right] + \left[\frac{1}{C_2C_3R_2R_3}\right]} \tag{27}$$

Band Pass Filter

$$\frac{V_{O2}}{V_{IN}} = \frac{s\left[\frac{1}{C_2R_2}\right]\left[\frac{R_1+R_4}{R_1}\right]\left[\frac{R_6}{R_5+R_6}\right]}{s^2 + s\left[\frac{1}{C_2R_2}\right]\left[\frac{R_5}{R_5+R_6}\right]\left[\frac{R_1+R_4}{R_1}\right] + \left[\frac{1}{C_2C_3R_2R_3}\right]} \tag{28}$$

The center frequency and Quality Factor for all of these filters is the same. The values can be calculated in the following manner:

$$\omega_c = \sqrt{\frac{1}{C_2C_3R_2R_3}}$$

and

$$Q = \sqrt{\frac{C_2R_2}{C_3R_3}}\left[\frac{R_5+R_6}{R_6}\right]\left[\frac{R_1}{R_1+R_4}\right] \tag{29}$$

Designing a band pass filter with a center frequency of 10 kHz and Quality Factor of 5.5

To do this, first consider the Quality Factor. It is best to pick convenient values for the capacitors. $C_2 = C_3 = 1000$ pF. Also, choose $R_1 = R_4 = 30$ kΩ. Now values of R_5 and R_6 need to be calculated. With the chosen values for the capacitors and resistors, Q reduces to:

$$Q = \frac{11}{2} = \frac{1}{2}\left[\frac{R_5+R_6}{R_6}\right] \tag{30}$$

or

$$R_5 = 10R_6 \; R_6 = 1.5\ k\Omega \; R_5 = 15\ k\Omega \tag{31}$$

Also, for f = 10 kHz, the center frequency is ωc = 2πf = 62.8 kHz.

Using the expressions above, the appropriate resistor values will be $R_2 = R_3 = 16\ k\Omega$.

The DC gain of this circuit is:

$$\text{DC GAIN} = \left[\frac{R_1 + R_4}{R_1}\right]\left[\frac{R_6}{R_5 + R_6}\right] = -14.8\ \text{dB} \tag{32}$$

REVISION HISTORY

Changes from Revision A (March 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	18

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMV716MM/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	AR3A
LMV716MM/NOPB.A	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	AR3A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

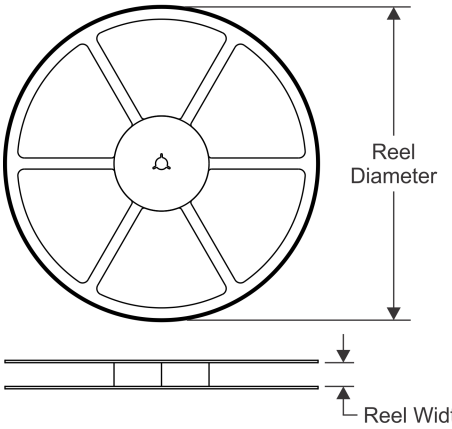
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

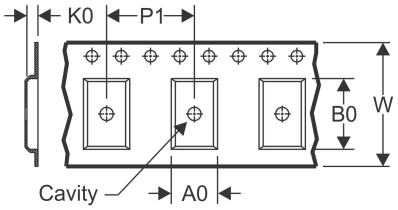
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

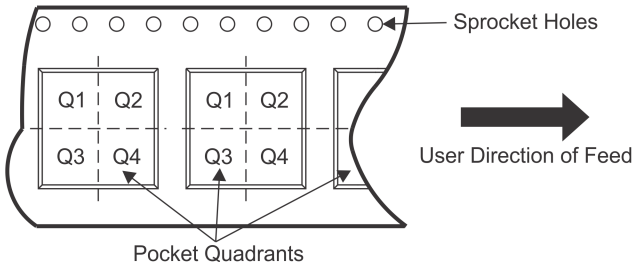


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

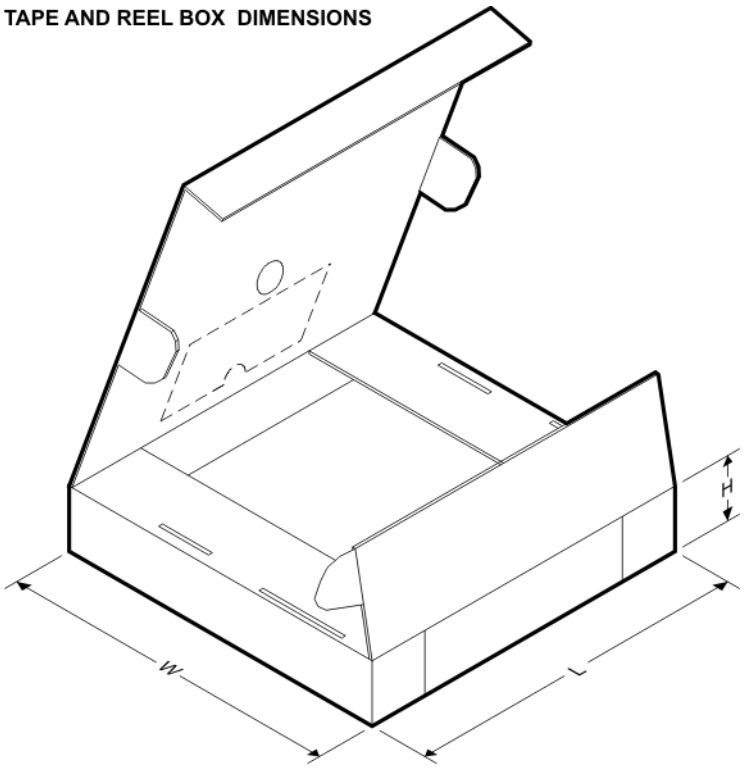
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV716MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

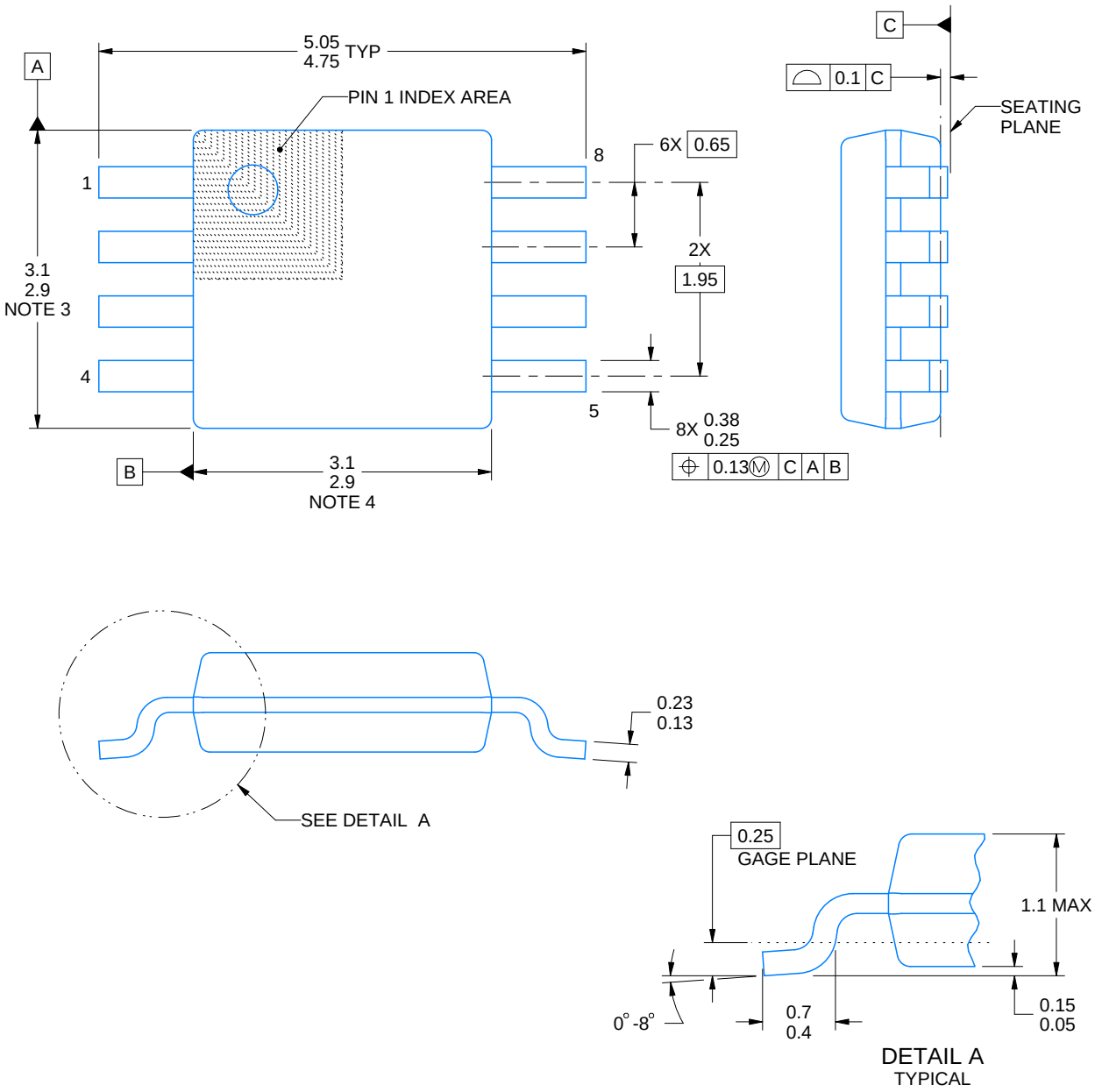
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV716MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



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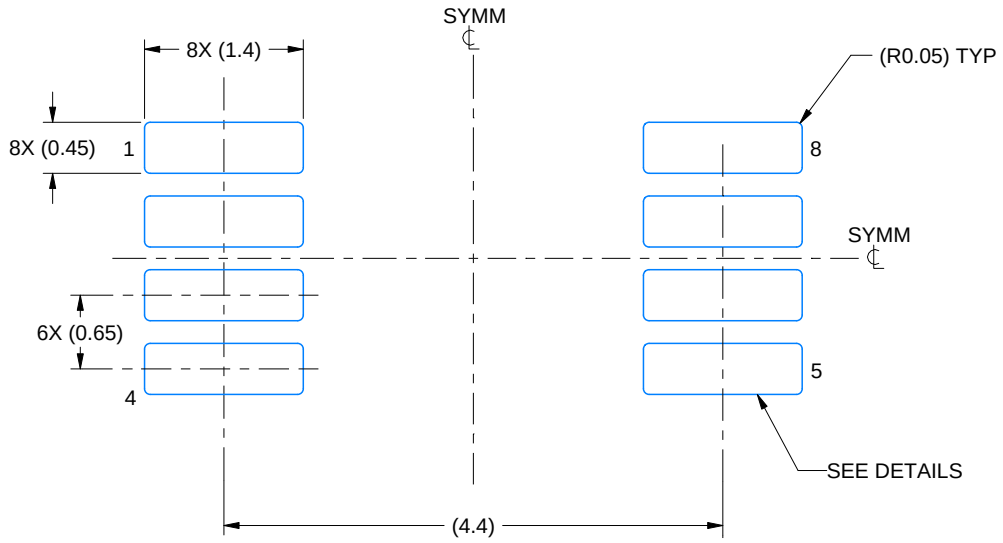
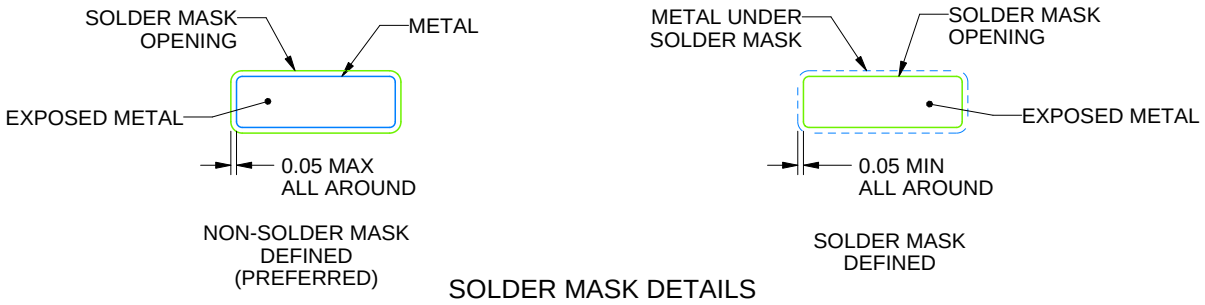
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

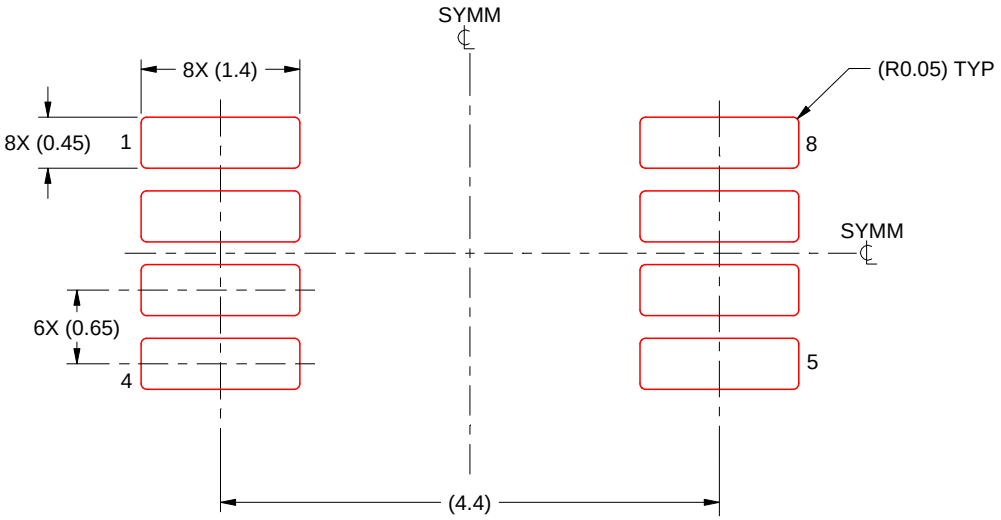


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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