LMV60x 1-MHz, Low-Power, General-Purpose, 2.7-V Operational Amplifiers

1 Features

- Typical 2.7-V Supply Values; Unless Otherwise Noted
- Ensured 2.7-V and 5-V Specifications
- Supply Current (Per Amplifier): 100 µA
- Gain Bandwidth Product: 1 MHz
- Shutdown Current (LMV601): 45 pA
- Turnon Time from Shutdown (LMV601): 5 µs
- Input Bias Current: 20 fA

2 Applications

- Cordless and Cellular Phones
- Laptops
- PDAs
- PCMCIA and Audio
- Portable and Battery-Powered Electronic Equipment
- Supply Current Monitoring
- Battery Monitoring
- Buffers
- Filters
- Drivers

3 Description

The LMV60x devices are single, dual, and quad low-voltage, low-power operational amplifiers. They are designed specifically for low-voltage, general-purpose applications. Other important product characteristics are low input bias current, rail-to-rail output, and wide temperature range. The LMV60x have 29-nV voltage noise at 10 KHz, 1-MHz GBW, 1-V/µs slew rate, 0.25-mV Vos. The LMV60x operates from a single supply voltage as low as 2.7 V, while drawing 100-µA (typical) quiescent current. In shutdown mode, the current can be reduced to 45 pA.

The industrial-plus temperature range of −40°C to 125°C allows the LMV60x to accommodate a broad range of extended environment applications.

The LMV601 offers a shutdown pin that can be used to disable the device. Once in shutdown mode, the supply current is reduced to 45 pA (typical).

The LMV601 is offered in the tiny 6-pin SC70 package, the LMV602 in space-saving 8-pin VSSOP and SOIC, and the LMV604 in 14-pin TSSOP and SOIC. These small package amplifiers offer an ideal solution for applications requiring minimum PCB footprint. Applications with area constrained printed-circuit board requirements include portable and battery-operated electronics.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMV601	SC70 (6)	2.00 mm × 1.25 mm
LMV602	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm
LMV604	SOIC (8)	4.90 mm × 3.91 mm
	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Sample and Hold Circuit

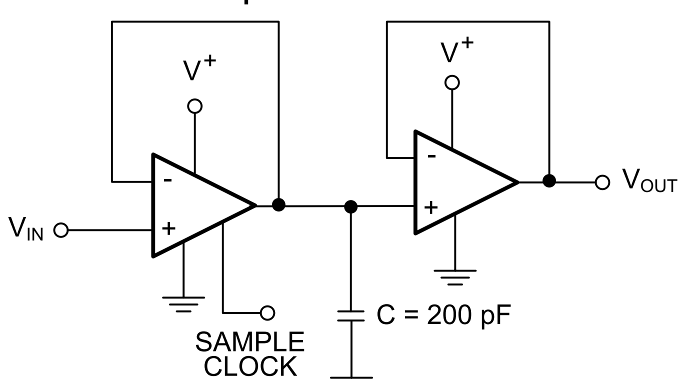


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (March 2013) to Revision C — **Page**

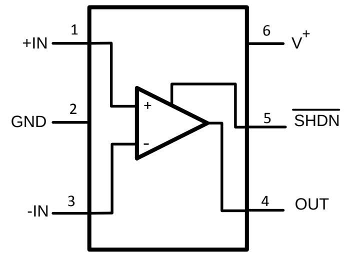
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed *Thermal Information* table to align with JEDEC standards ... 5
- Changed ON mode (LMV601) typical value for V_{SD} in *Electrical Characteristics – DC (2.7 V)* from '1.7 to 2.7' to '1.7' ... 6
- Changed ON Mode (LMV601) max value for V_{SD} in *Electrical Characteristics – DC (2.7 V)* from '2.4 to 2.7' to '2.7' ... 6
- Changed Shutdown mode (LMV601) typical value for V_{SD} in *Electrical Characteristics – DC (2.7 V)* from '0 to 1' to '0' ... 6
- Changed Shutdown mode (LMV601) max value for V_{SD} in *Electrical Characteristics – DC (2.7 V)* from '0 to 0.8' to '0.8' ... 6
- Deleted '–0.2 to 4.2 (Range)' from V_{CM} in *Electrical Characteristics – DC (5 V)* ... 7
- Changed ON mode (LMV601) typical value for V_{SD} in *Electrical Characteristics – DC (5 V)* from '3.1 to 5' to '3.1' ... 7
- Changed ON mode (LMV601) max value for V_{SD} in *Electrical Characteristics – DC (5 V)* from '4.5 to 5' to '5' ... 7
- Changed Shutdown mode (LMV601) typical value for V_{SD} in *Electrical Characteristics – DC (5 V)* from '0 to 1' to '1' ... 7
- Changed Shutdown mode (LMV601) max value for V_{SD} in *Electrical Characteristics – DC (5 V)* from '0 to 0.8' to '0.8' ... 7

Changes from Revision A (March 2012) to Revision B — **Page**

- Changed layout of National Data Sheet to TI format ... 16

5 Pin Configuration and Functions

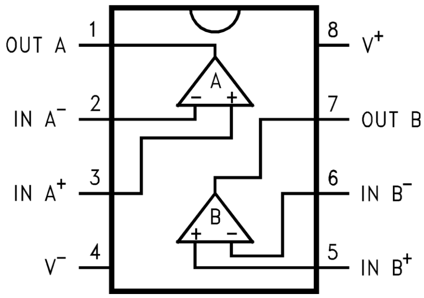
LMV601
DCK Package
6-Pin SC70
Top View



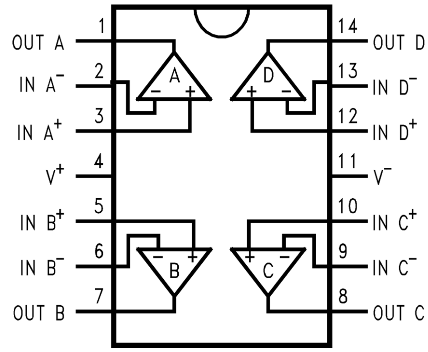
Pin Functions: LMV601

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	2	P	Supply negative input
+IN	1	I	Noninverting input
–IN	3	I	Inverting input
OUT	4	O	Output
SHDN	5	I	Active low enable input
V+	6	P	Positive supply input

LMV602
DGK or D Packages
8-Pin VSSOP or SOIC
Top View



LMV604
PW or D Packages
14-Pin TSSOP and SOIC
Top View



Pin Functions: LMV602, LMV604

PIN			I/O	DESCRIPTION
NAME	NO.			
	LMV602	LMV604		
+INA	3	3	I	Noninverting input, channel A
+INB	5	5	I	Noninverting input, channel B
+INC	—	10	I	Noninverting input, channel C
+IND	—	12	I	Noninverting input, channel D
–INA	2	2	I	Inverting input, channel A
–INB	6	6	I	Inverting input, channel B
–INC	—	9	I	Inverting input, channel C
–IND	—	13	I	Inverting input, channel D
OUTA	1	1	O	Output, channel A
OUTB	7	7	O	Output, channel B
OUTC	—	8	O	Output, channel C
OUTD	—	14	O	Output, channel D
V+	8	4	P	Positive (highest) power supply
V–	4	11	P	Negative (lowest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1][2]

	MIN	MAX	UNIT
Differential input voltage	±Supply Voltage		
Supply voltage, (V+) – (V–)		6	V
Output short circuit to V+	See[3]		
Output short circuit to V–	See[4]		
Junction temperature, T_J[5]		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Shorting output to V+ adversely affects reliability.
(4) Shorting output to V– adversely affects reliability.
(5) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM)[1][1]	±2000	V
		Machine model (MM)[2]	±200	

(1) Human-Body Model, applicable std. MIL-STD-883, Method 3015.7.
(2) Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage	2.7	5.5	V
Temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		LMV601	LMV602		LMV604		UNIT
		DCK (SC70)	D (SOIC)	DGK (VSSOP)	D (SOIC)	PW (TSSOP)	
		6 PINS	8 PINS	8 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	229.1	120.8	178.3	91.5	123.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	116.1	65.2	68.4	49.7	50.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	53.3	61.4	98.8	46	66.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.8	16.1	9.8	12.4	6.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	52.7	60.8	97.3	45.7	65.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics – DC (2.7 V)

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 2.7 V, V^- = 0 V, V_{CM} = V^+ / 2, V_O = V^+ / 2 and R_L > 1 MΩ.[1]

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OS}	Input offset voltage	LMV601			0.25	4	mV
		LMV602 and LMV604			0.55	5	mV
TCV_{OS}	Input offset voltage average drift				1.7		µV/°C
I_B	Input bias current				0.02		pA
I_{OS}	Input offset current				6.6		fA
I_S	Supply current	Per amplifier			100	170	µA
		Shutdown mode, V_{SD} = 0 V (LMV601)			45 pA	1	µA
CMRR	Common-mode rejection ratio	0 V ≤ V_{CM} ≤ 1.7 V			80		dB
PSRR	Power supply rejection ratio	2.7 V ≤ V^+ ≤ 5 V			82		dB
V_{CM}	Input common-mode voltage	For CMRR ≥ 50 dB		0		1.7	V
A_V	Large signal voltage gain	R_L = 10 kΩ to 1.35 V			113		dB
V_O	Output swing	R_L = 10 kΩ to 1.35 V	Swing high		5	30	mV
			Swing low	30	5.3		mV
I_O	Output short-circuit current	Sourcing LMV601 and LMV602			32		mA
		Sourcing LMV604			24		mA
		Sinking			24		mA
t_{on}	Turnon time from shutdown	(LMV601)			5		µs
V_{SD}	Shutdown pin voltage range	ON mode (LMV601)			1.7	2.7	V
		Shutdown mode (LMV601)			0	0.8	V

(1) Values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No assurance of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$.

6.6 Electrical Characteristics – AC (2.7 V)

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 2.7 V, V^- = 0 V, V_{CM} = V^+ / 2, V_O = V^+ / 2 and R_L > 1 MΩ.[1]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate	R_L = 10 kΩ,[2]		1		V/µs
GBW	Gain bandwidth product	R_L = 100 kΩ, C_L = 200 pF		1		MHz
Φ_m	Phase margin	R_L = 100 kΩ		72		deg
G_m	Gain margin	R_L = 100 kΩ		20		dB
e_n	Input-referred voltage noise	f = 1 kHz		40		nV/√Hz
i_n	Input-referred current noise	f = 1 kHz		0.001		pA/√Hz
THD	Total harmonic distortion	f = 1 kHz, A_V = 1 R_L = 600 Ω, V_{IN} = 1 V_{PP}		0.017%		

(1) Values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No assurance of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$.
(2) Connected as voltage follower with 2-V_{PP} step input. Number specified is the slower of the positive and negative slew rates.

6.7 Electrical Characteristics – DC (5 V)

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OS}	Input offset voltage	LMV601			0.25	4	mV
		LMV602 and LMV604			0.7	5	
TCV_{OS}	Input offset voltage average drift				1.9		µV/°C
I_B	Input bias current				0.02		pA
I_{OS}	Input offset current				6.6		fA
I_S	Supply current	Per amplifier			107	200	µA
		Shutdown mode, V_{SD} = 0 V (LMV601)			0.033	1	µA
CMRR	Common-mode rejection ratio	$0 V \le V_{CM} \le 4 V$			86		dB
PSRR	Power supply rejection ratio	$2.7 V \le V^+ \le 5 V$			82		dB
V_{CM}	Input common-mode voltage	For CMRR ≥ 50 dB		0		4	V
A_V	Large signal voltage gain(2)	R_L = 10 kΩ to 2.5 V			116		dB
V_O	Output swing	R_L = 10 kΩ to 2.5 V	Swing high		7	30	mV
			Swing low	30	7		
I_O	Output short-circuit current	Sourcing			113		mA
		Sinking			75		
t_{on}	Turnon time from shutdown	(LMV601)			5		µs
V_{SD}	Shutdown pin voltage range	ON mode (LMV601)			3.1	5	V
		Shutdown mode (LMV601)			0	0.8	

(1) Values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No assurance of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$.
(2) R_L is connected to mid-supply. The output voltage is GND + 0.2 V ≤ V_O ≤ V^+ − 0.2 V

6.8 Electrical Characteristics – AC (5 V)

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 5 V, V^- = 0 V, $V_{CM} = V^+ / 2$, $V_O = V^+ / 2$ and R_L > 1 MΩ.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate	R_L = 10 kΩ,(1)		1		V/µs
GBW	Gain bandwidth product	R_L = 100 kΩ, C_L = 200 pF		1		MHz
Φ_m	Phase margin	R_L = 100 kΩ		72		°
G_m	Gain margin	R_L = 100 kΩ		20		dB
e_n	Input-referred voltage noise	f = 1 kHz		39		nV/√Hz
i_n	Input-referred current noise	f = 1 kHz		0.001		pA/√Hz
THD	Total harmonic distortion	f = 1 kHz, A_V = 1 R_L = 600 Ω, V_{IN} = 1 V_{PP}		0.012%		

(1) Connected as voltage follower with 2-V_{PP} step input. Number specified is the slower of the positive and negative slew rates.

6.9 Typical Characteristics

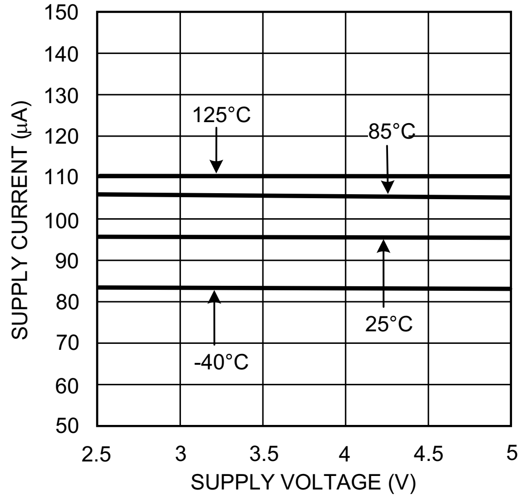


Figure 1. Supply Current vs Supply Voltage (LMV601)

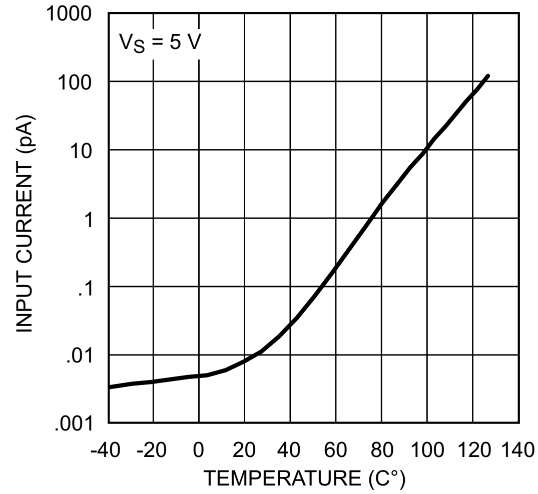


Figure 2. Input Current vs Temperature

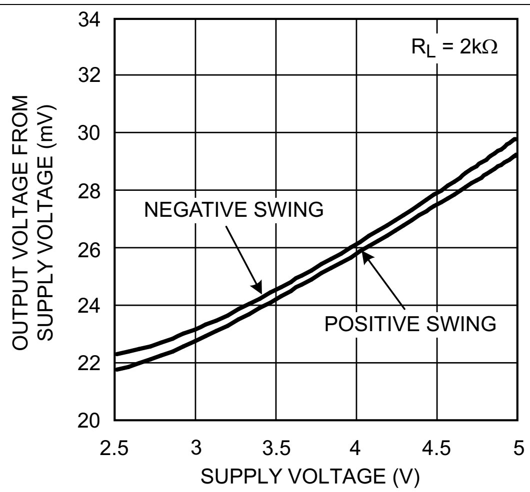


Figure 3. Output Voltage Swing vs Supply Voltage

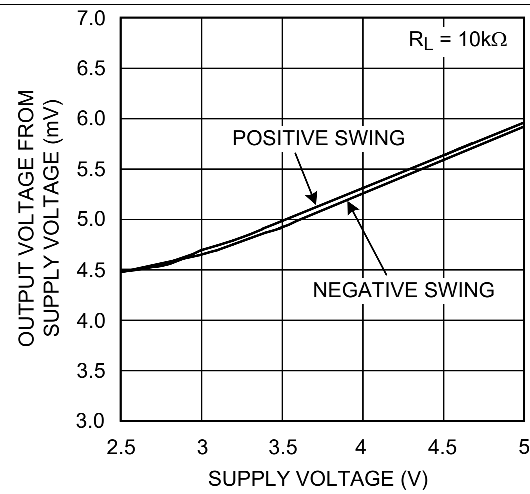


Figure 4. Output Voltage Swing vs Supply Voltage

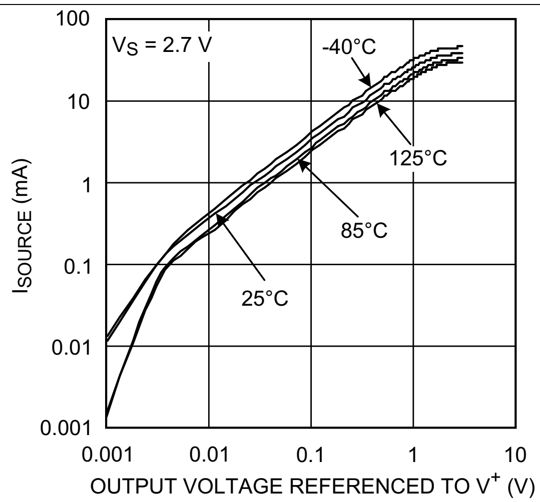


Figure 5. I_{SOURCE} vs V_{OUT}

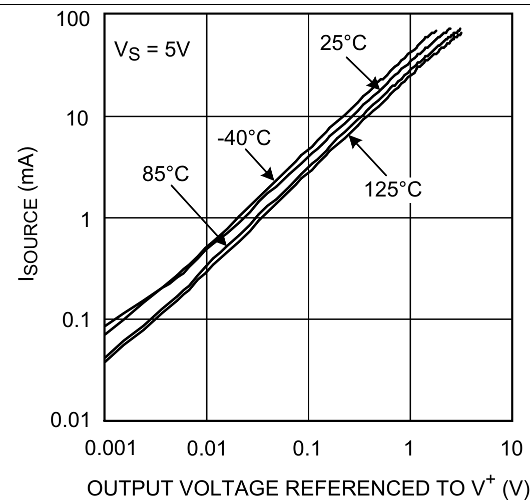


Figure 6. I_{SOURCE} vs V_{OUT}

Typical Characteristics (continued)

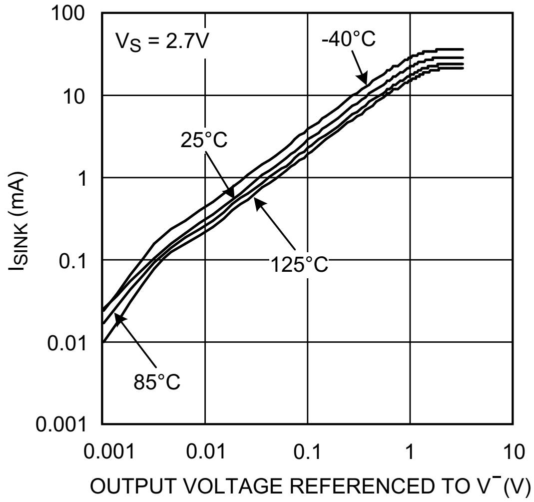


Figure 7. I_{SINK} vs V_{OUT}

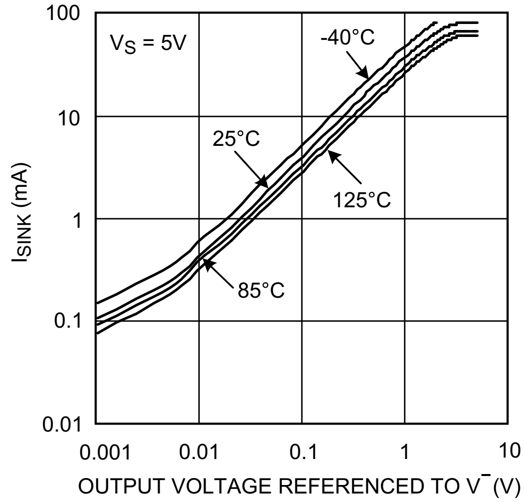


Figure 8. I_{SINK} vs V_{OUT}

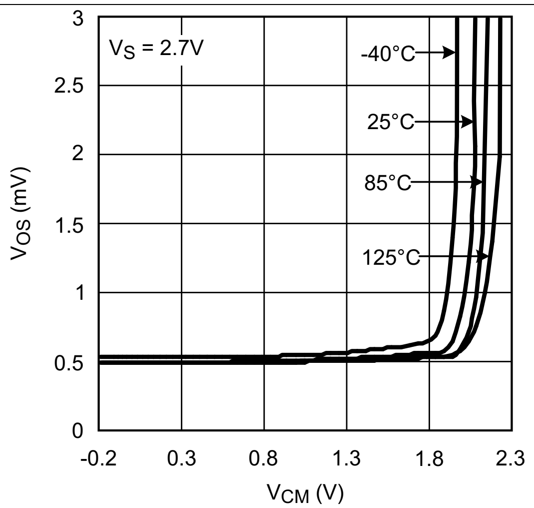


Figure 9. V_{OS} vs V_{CM}

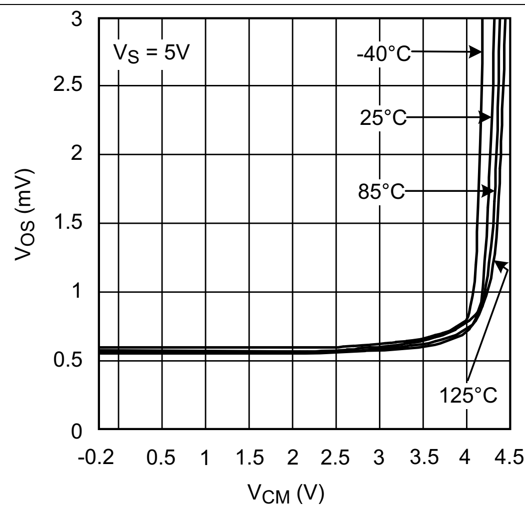


Figure 10. V_{OS} vs V_{CM}

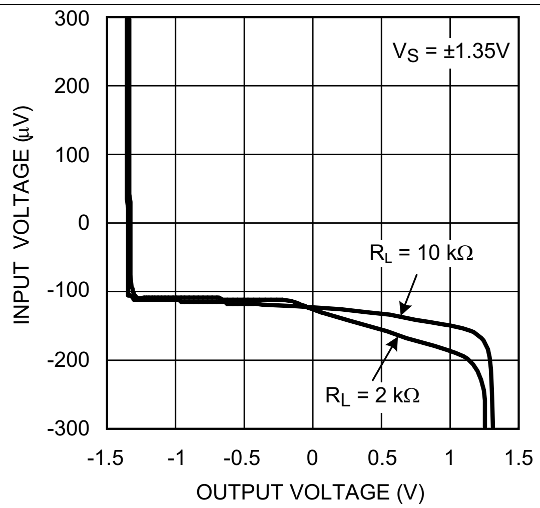


Figure 11. V_{IN} vs V_{OUT}

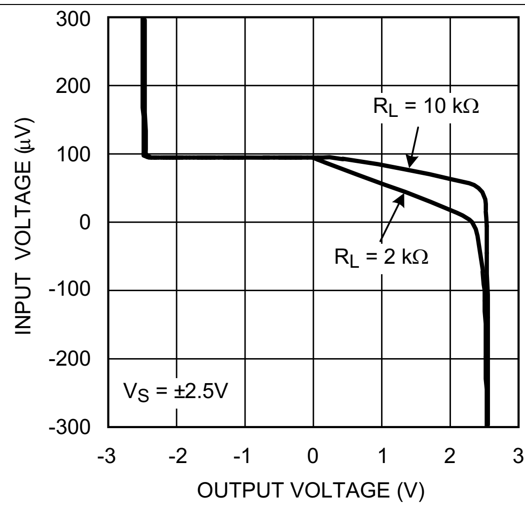


Figure 12. V_{IN} vs V_{OUT}

Typical Characteristics (continued)

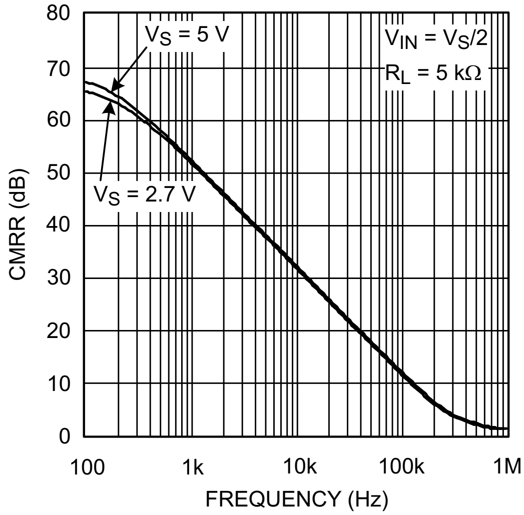


Figure 13. CMRR vs Frequency

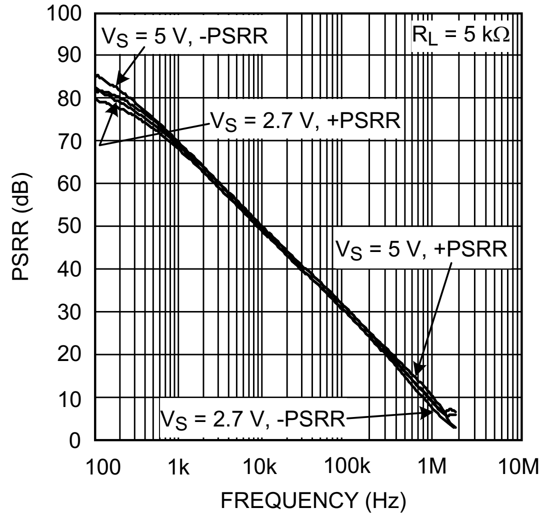


Figure 14. PSRR vs Frequency

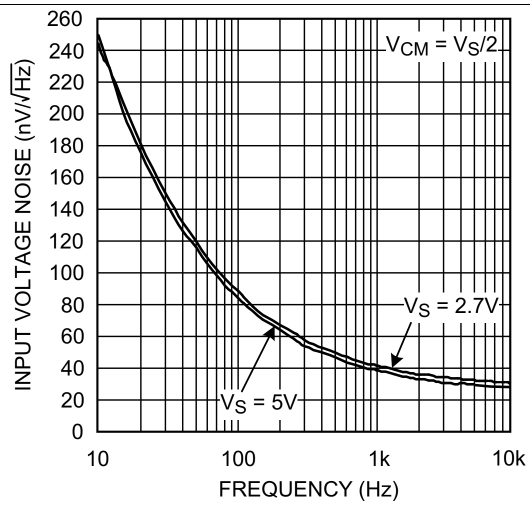


Figure 15. Input Voltage Noise vs Frequency

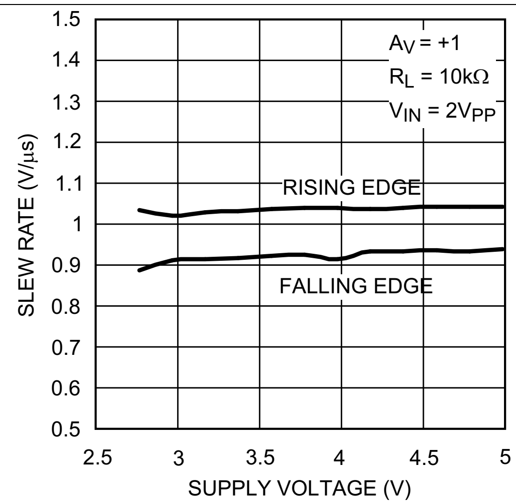


Figure 16. Slew Rate vs V_{SUPPLY}

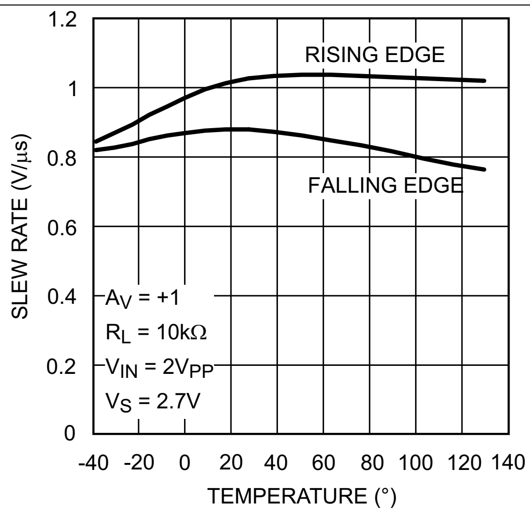


Figure 17. Slew Rate vs Temperature

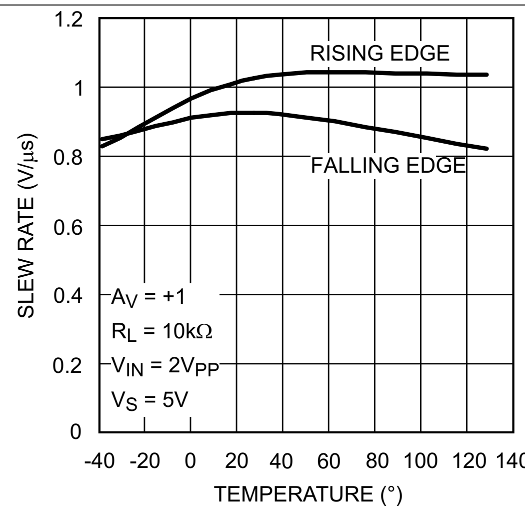


Figure 18. Slew Rate vs Temperature

Typical Characteristics (continued)

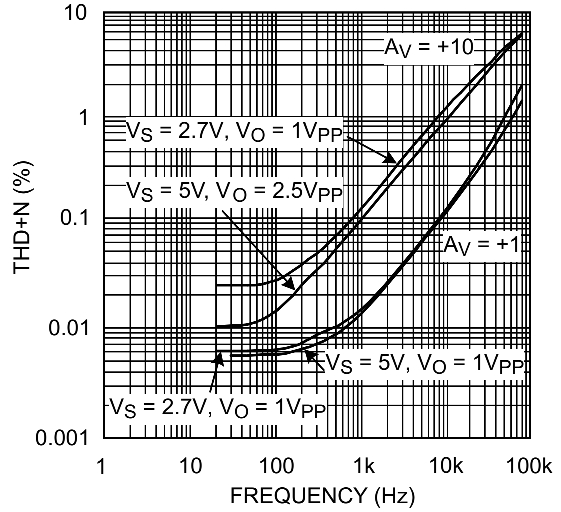


Figure 19. THD+N vs Frequency

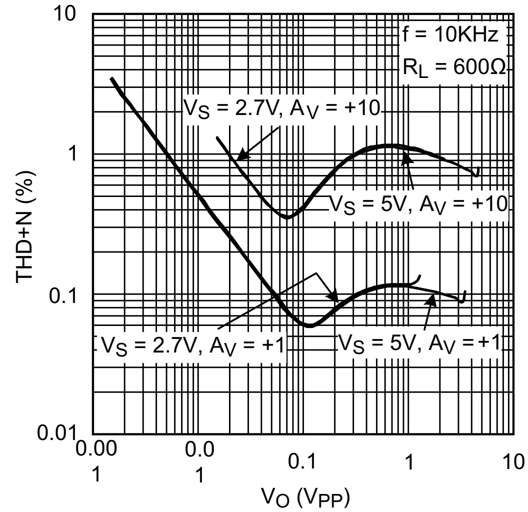


Figure 20. THD+N vs V_{OUT}

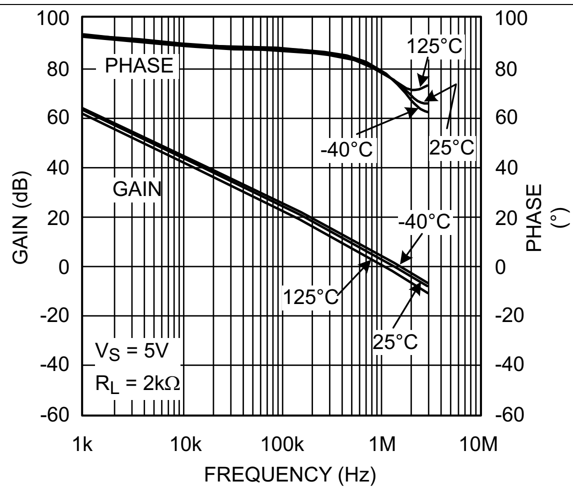


Figure 21. Open-Loop Frequency Over Temperature

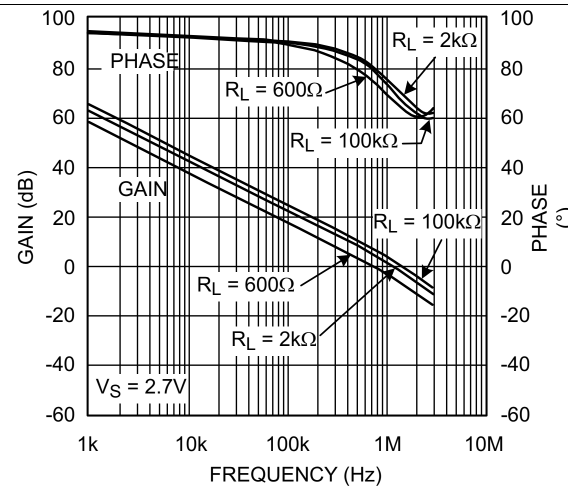


Figure 22. Open-Loop Frequency Response

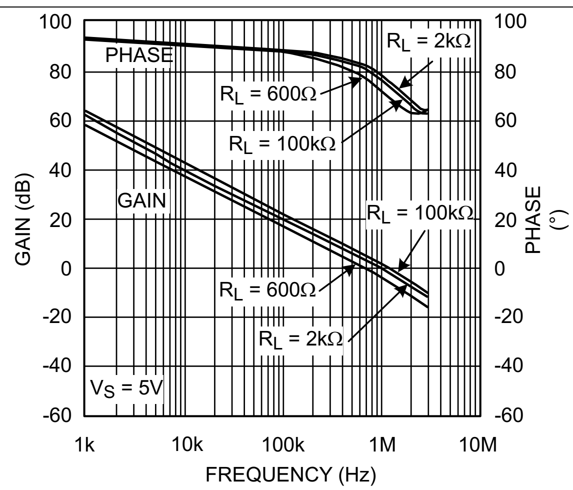


Figure 23. Open-Loop Frequency Response

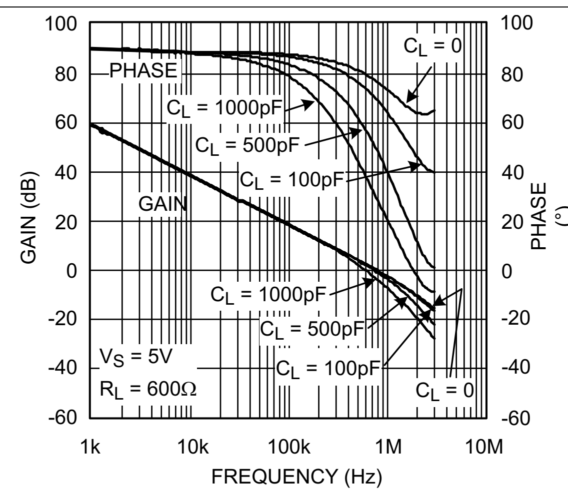


Figure 24. Gain and Phase vs C_L

Typical Characteristics (continued)

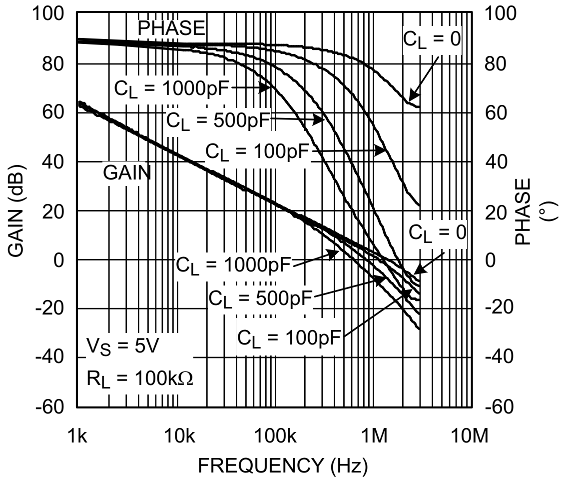


Figure 25. Gain and Phase vs C_L

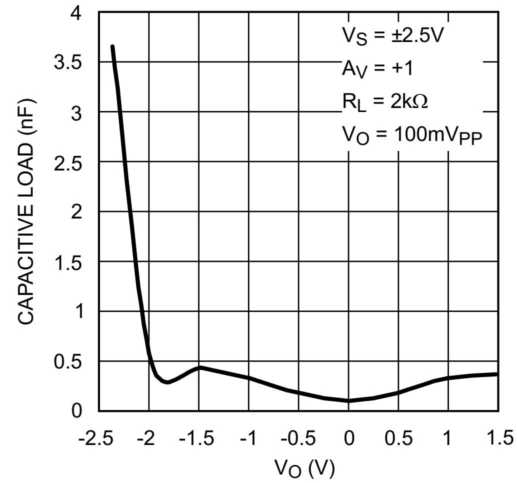


Figure 26. Stability vs Capacitive Load

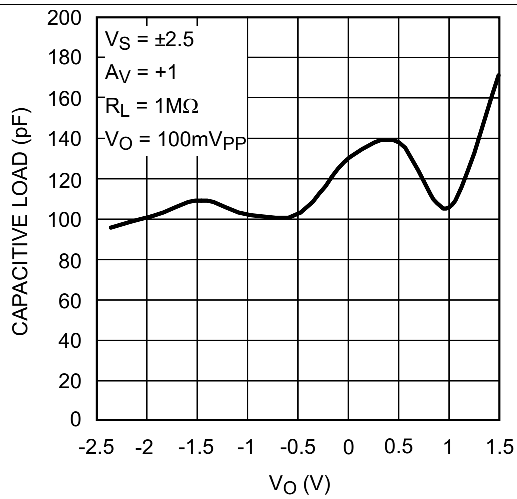


Figure 27. Stability vs Capacitive Load

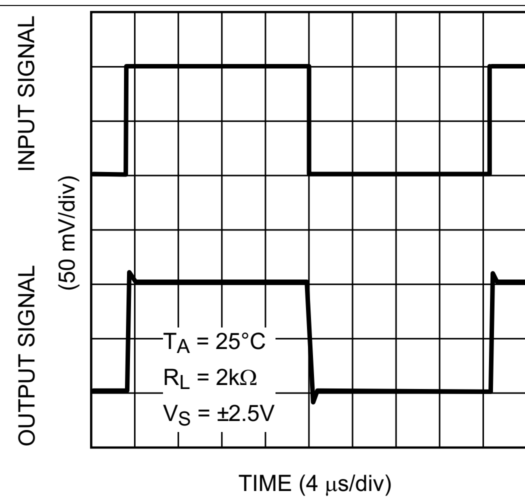


Figure 28. Noninverting Small Signal Pulse Response

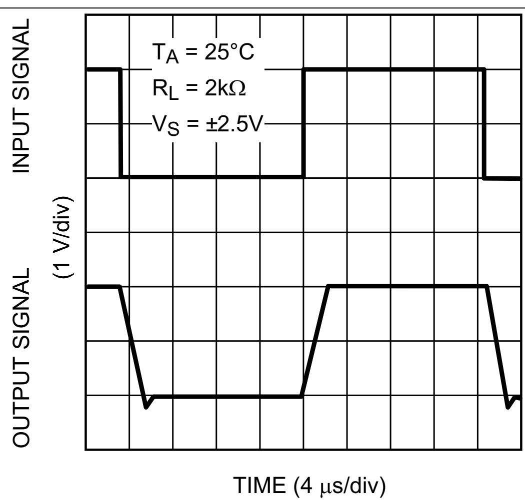


Figure 29. Noninverting Large Signal Pulse Response

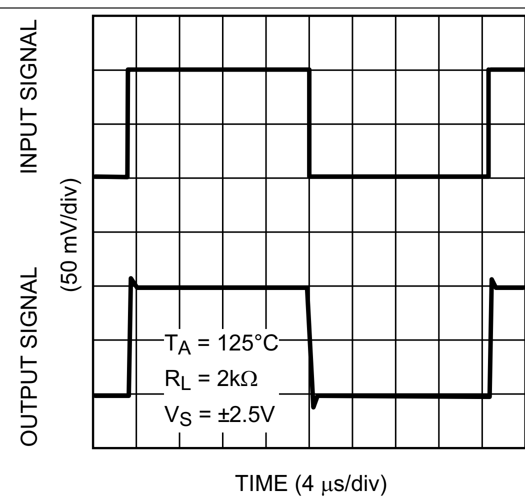


Figure 30. Noninverting Small Signal Pulse Response

Typical Characteristics (continued)

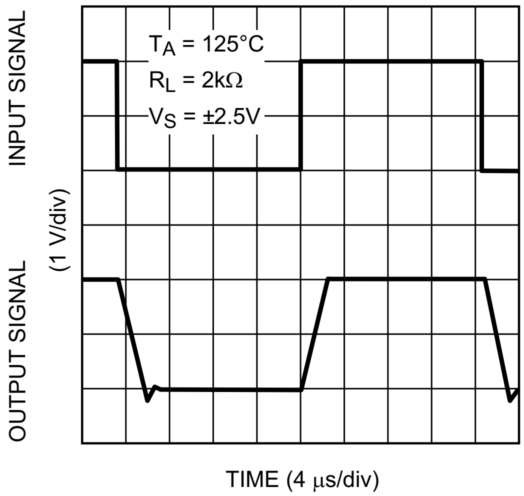


Figure 31. Noninverting Large Signal Pulse Response

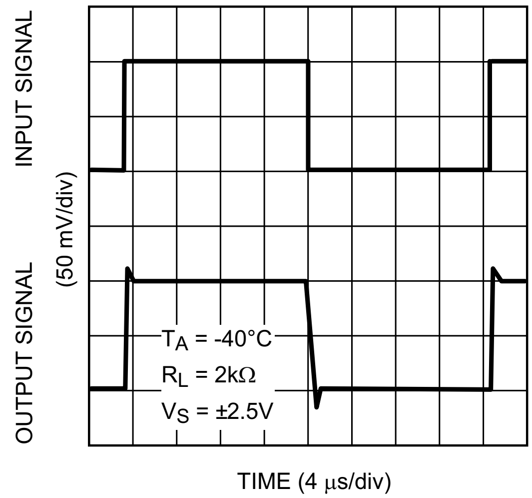


Figure 32. Noninverting Small Signal Pulse Response

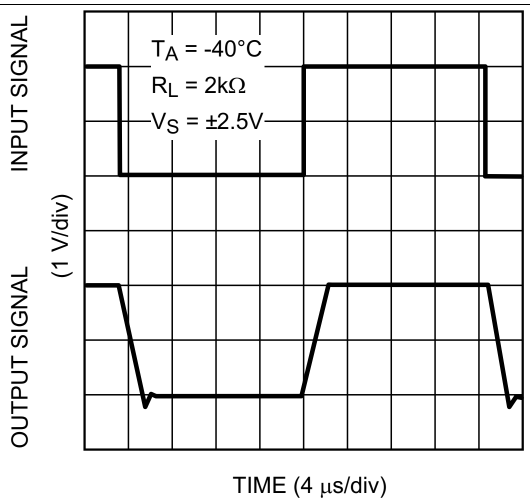


Figure 33. Noninverting Large Signal Pulse Response

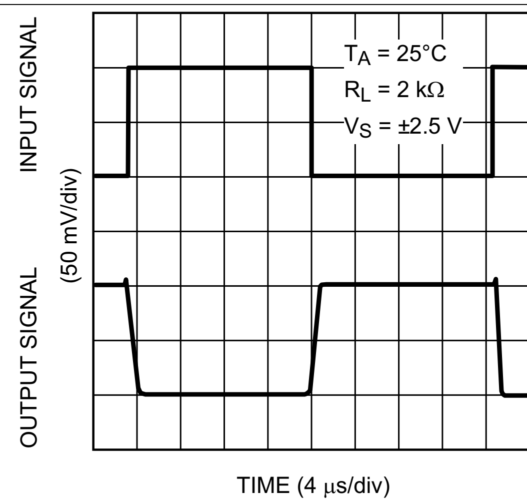


Figure 34. Inverting Small Signal Pulse Response

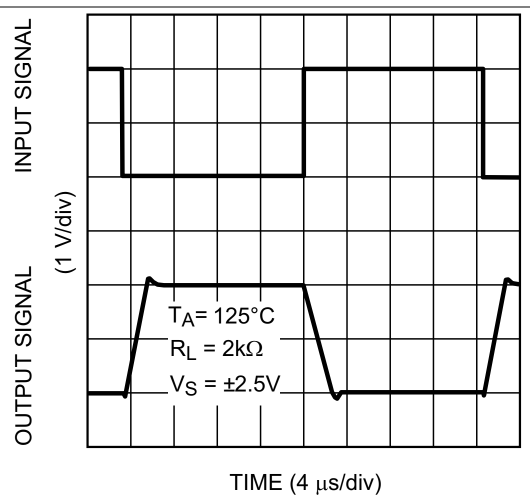


Figure 35. Inverting Large Signal Pulse Response

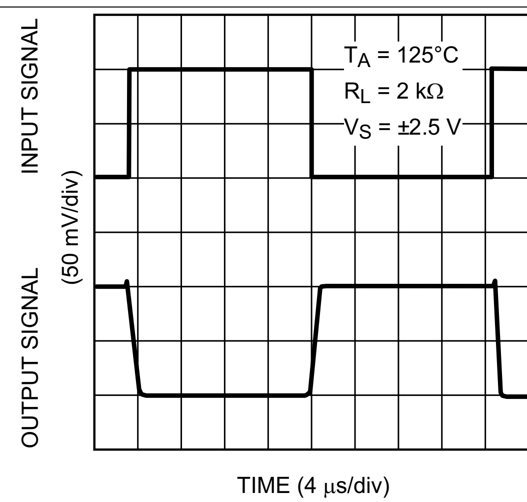


Figure 36. Inverting Small Signal Pulse Response

Typical Characteristics (continued)

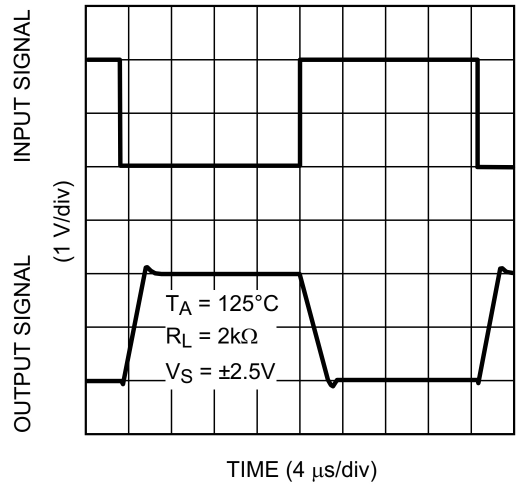


Figure 37. Inverting Large Signal Pulse Response

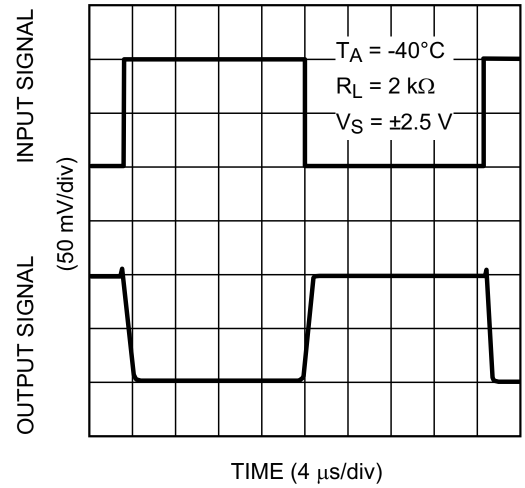


Figure 38. Inverting Small Signal Pulse Response

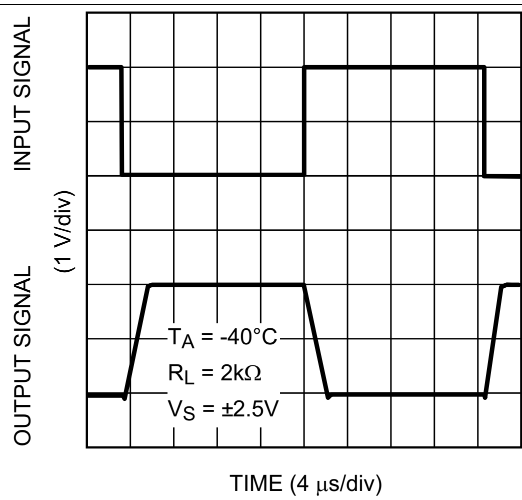


Figure 39. Inverting Large Signal Pulse Response

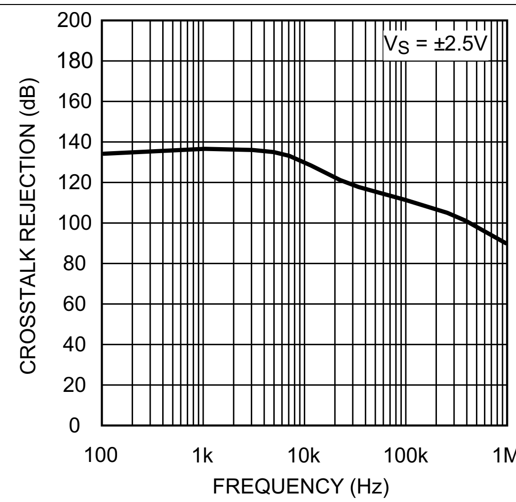


Figure 40. Crosstalk Rejection vs Frequency

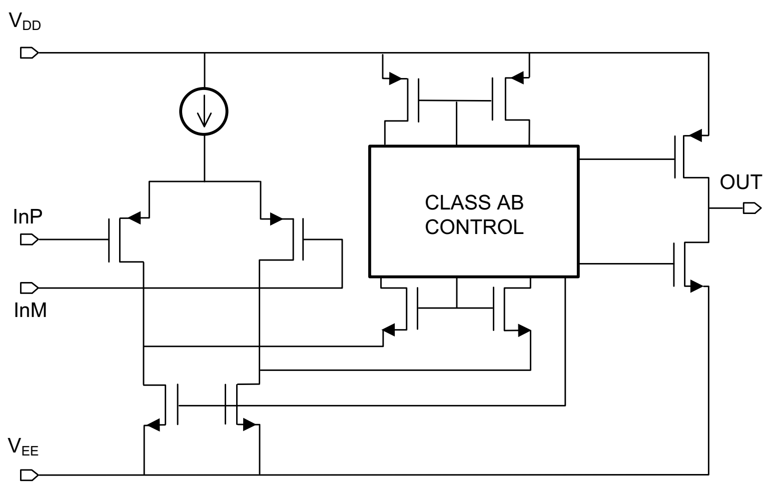
7 Detailed Description

7.1 Overview

The LMV60x family of amplifiers features low-voltage, low-power, and rail-to-rail output operational amplifiers designed for low-voltage portable applications. The family is designed using all CMOS technology. This results in an ultra-low input bias current. The LMV601 has a shutdown option, which can be used in portable devices to increase battery life.

A simplified schematic of the LMV60x family of amplifiers is shown in *Functional Block Diagram*. The PMOS input differential pair allows the input to include ground. The output of this differential pair is connected to the Class AB turnaround stage. This Class AB turnaround has a lower quiescent current, compared to regular turnaround stages. This results in lower offset, noise, and power dissipation, while slew rate equals that of a conventional turnaround stage. The output of the Class AB turnaround stage provides gate voltage to the complementary common-source transistors at the output stage. These transistors enable the device to have rail-to-rail output.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Class AB Turnaround Stage Amplifier

This patented folded cascode stage has a combined class AB amplifier stage, which replaces the conventional folded cascode stage. Therefore, the class AB folded cascode stage runs at a much lower quiescent current compared to conventional folded cascode stages. This results in significantly smaller offset and noise contributions. The reduced offset and noise contributions in turn reduce the offset voltage level and the voltage noise level at the input of the LMV60x. Also the lower quiescent current results in a high open-loop gain for the amplifier. The lower quiescent current does not affect the slew rate of the amplifier nor its ability to handle the total current swing coming from the input stage.

The input voltage noise of the device at low frequencies, below 1 kHz, is slightly higher than devices with a BJT input stage. However, the PMOS input stage results in a much lower input bias current and the input voltage noise drops at frequencies above 1 kHz.

7.4 Device Functional Modes

7.4.1 Low Input Bias Current

The LMV60x amplifiers have a PMOS input stage. As a result, they have a much lower input bias current than devices with BJT input stages. This feature makes these devices ideal for sensor circuits. A typical curve of the input bias current of the LMV601 is shown in Figure 41.

Device Functional Modes (continued)

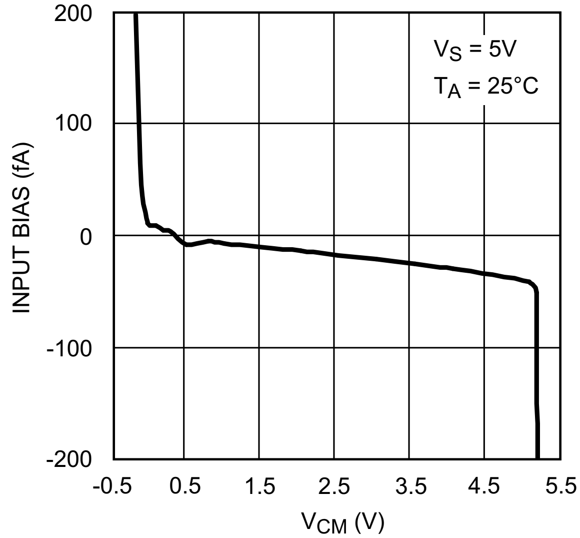


Figure 41. Input Bias Current vs V_{CM}

7.4.2 Shutdown Feature

The LMV601 is capable of being turned off to conserve power and increase battery life in portable devices. Once in shutdown mode the supply current is drastically reduced, 1 µA maximum, and the output is *tri-stated*.

The device is disabled when the shutdown pin voltage is pulled low. The shutdown pin must never be left unconnected. Leaving the pin floating results in an undefined operation mode and the device may oscillate between shutdown and active modes.

The LMV601 typically turns on 2.8 µs after the shutdown voltage is pulled high. The device turns off in less than 400 ns after shutdown voltage is pulled low. Figure 42 and Figure 43 show the turnon and turnoff time of the LMV601, respectively. To reduce the effect of the capacitance added to the circuit by the scope probe, in the turnoff time circuit a resistive load of 600 Ω is added. Figure 44 and Figure 45 show the test circuits used to obtain the two plots.

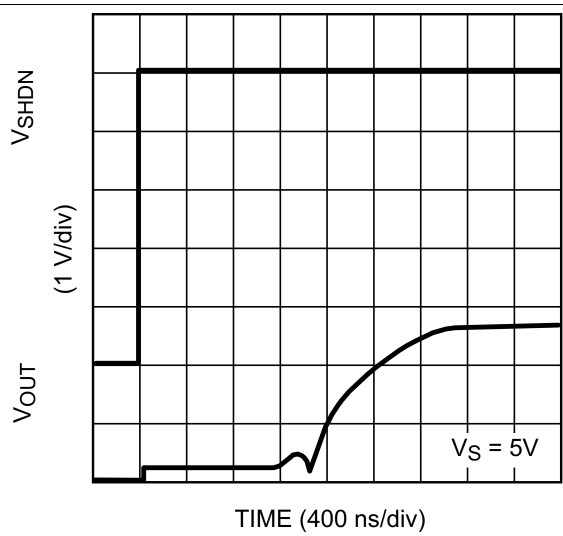


Figure 42. Turnon Time

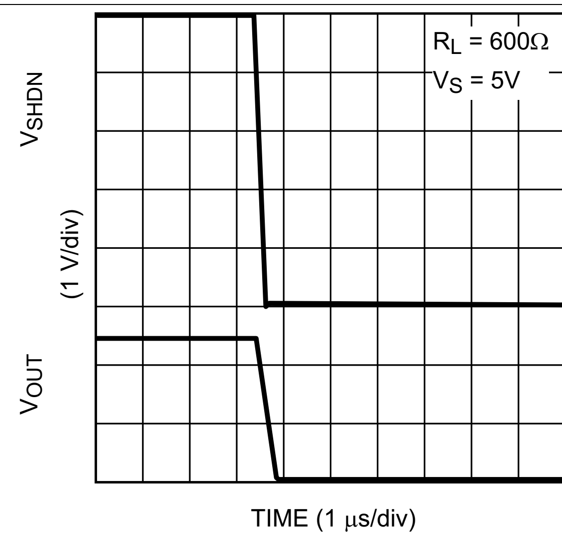


Figure 43. Turnoff Time

Device Functional Modes (continued)

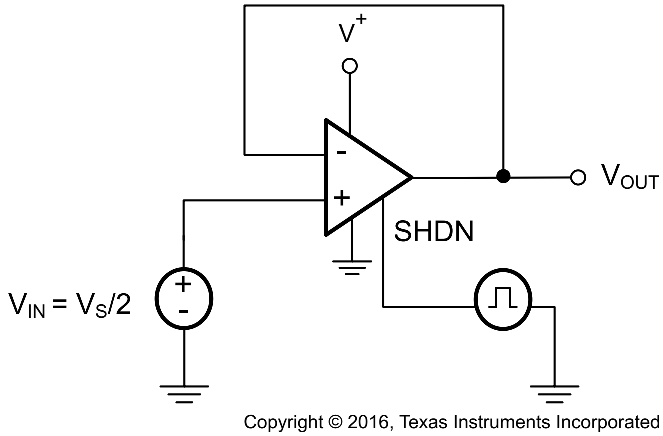


Figure 44. Turnon Time

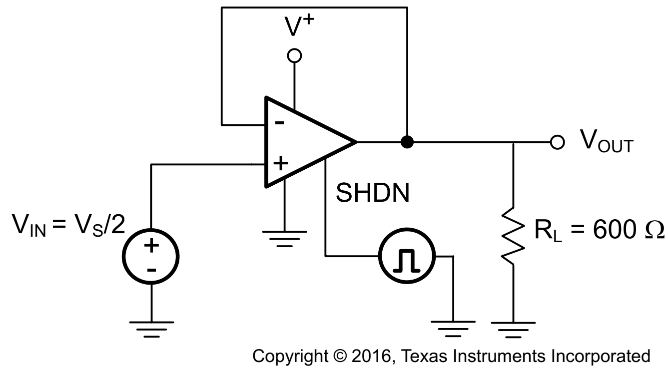


Figure 45. Turnoff Time

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMV60x family of amplifiers features low-voltage, low-power, and rail-to-rail output operational amplifiers designed for low-voltage portable applications.

8.2 Typical Application

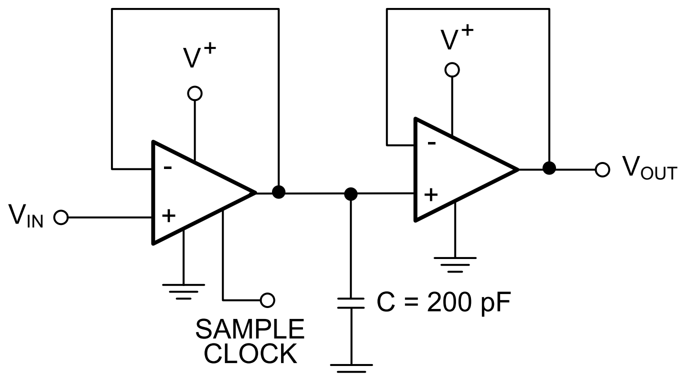


Figure 46. Sample and Hold Circuit

8.2.1 Design Requirements

The lower input bias current of the LMV601 results in a very high input impedance. The output impedance when the device is in shutdown mode is quite high. These high impedances, and the ability of the shutdown pin to be derived from a separate power source, make LMV601 a good choice for sample and hold circuits. The sample clock must be connected to the shutdown pin of the amplifier to rapidly turn the device on or off.

8.2.2 Detailed Design Procedure

Figure 46 shows the schematic of a simple sample-and-hold circuit. When the sample clock is high, the first amplifier is in normal operation mode and the second amplifier acts as a buffer. The capacitor, which appears as a load on the first amplifier, is charging at this time. The voltage across the capacitor is that of the noninverting input of the first amplifier because it is connected as a voltage-follower. When the sample clock is low, the first amplifier is shut off, bringing the output impedance to a high value. The high impedance of this output, along with the very high impedance on the input of the second amplifier, prevents the capacitor from discharging. There is very little voltage droop while the first amplifier is in shutdown mode. The second amplifier, which is still in normal operation mode and is connected as a voltage-follower, also provides the voltage sampled on the capacitor at its output.

Typical Application (continued)

8.2.3 Application Curve

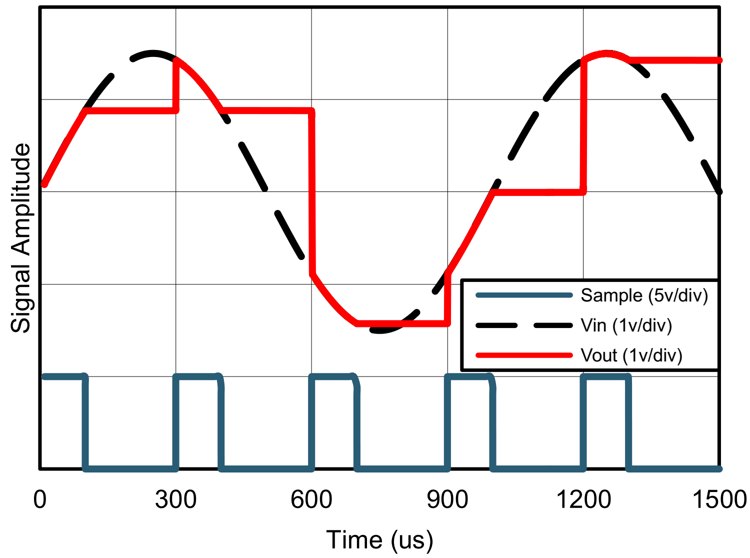


Figure 47. Sample-and-Hold Circuit Results

8.3 Dos and Don'ts

Do properly bypass the power supplies.

Do add series resistence to the output when driving capacitive loads, particularly cables, Muxes, and ADC inputs.

Do add series current-limiting resistors and external Schottky clamp diodes if input voltage is expected to exceed the supplies. Limit the current to 1 mA or less (1 kΩ per volt).

9 Power Supply Recommendations

For proper operation, the power supplies must be properly decoupled. For decoupling the supply lines, TI recommends that 10-nF capacitors be placed as close as possible to the operational amplifier power supply pins. For a single supply, place a capacitor between V^+ and V^- supply leads. For dual supplies, place one capacitor between V^+ and ground, and one capacitor between V^- and ground.

10 Layout

10.1 Layout Guideline

To properly bypass the power supply, consider the placement of several components on the printed-circuit boad. A 6.8-µF or greater tantalum capacitor must be placed at the point where the power supply for the amplifier is introduced onto the board. Another 0.1-µF ceramic capacitor must be placed as close as possible to the power supply pin of the amplifier. If the amplifier is operated in a single power supply, only the V^+ pin must be bypassed with a 0.1-µF capacitor. If the amplifier is operated in a dual power supply, both V^+ and $V^–$ pins must be bypassed.

It is good practice to use a ground plane on a printed-circuit board to provide all components with a low inductive ground connection.

TI recommends surface-mount components in 0805 size or smaller in the LMV601-N application circuits. Designers can take advantage of the VSSOP miniature sizes to condense board layout to save space and reduce stray capacitance.

10.2 Layout Example

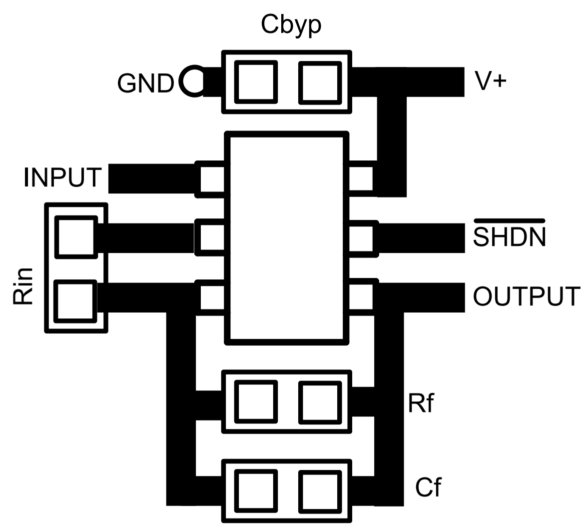


Figure 48. PCB Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

- LMV601 PSPICE Model (zip file)
- LMV601 PSPICE Model (zip file)
- LMV602 PSPICE Model (zip file)
- LMV604 PSPICE Model (zip file)
- TINA-TI SPICE-Based Analog Simulation Program
- DIP Adapter Evaluation Module
- TI Universal Operational Amplifier Evaluation Module
- TI Filterpro Software

11.2 Documentation Support

11.2.1 Related Documentation

For additional applications, see the following:

AN-31 Op Amp Circuit Collection (SNLA140)

11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LMV601	Click here	Click here	Click here	Click here	Click here
LMV602	Click here	Click here	Click here	Click here	Click here
LMV604	Click here	Click here	Click here	Click here	Click here

11.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.6 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.7 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMV601MG/NOPB	Active	Production	SC70 (DCK) | 6	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AUA
LMV601MG/NOPB.A	Active	Production	SC70 (DCK) | 6	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AUA
LMV601MGX/NOPB	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AUA
LMV601MGX/NOPB.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AUA
LMV602MA/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMV60 2MA
LMV602MA/NOPB.A	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMV60 2MA
LMV602MAX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMV60 2MA
LMV602MAX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMV60 2MA
LMV602MAX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	SN	Level-1-260C-UNLIM	-40 to 125	LMV60 2MA
LMV602MM/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AC9A
LMV602MM/NOPB.A	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AC9A
LMV602MMX/NOPB	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AC9A
LMV602MMX/NOPB.A	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AC9A
LMV604MA/NOPB	Active	Production	SOIC (D) | 14	55 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMV604MA
LMV604MA/NOPB.A	Active	Production	SOIC (D) | 14	55 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMV604MA
LMV604MA/NOPB.B	Active	Production	SOIC (D) | 14	55 | TUBE	-	SN	Level-1-260C-UNLIM	-40 to 125	LMV604MA
LMV604MAX/NOPB	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMV604MA
LMV604MAX/NOPB.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMV604MA
LMV604MAX/NOPB.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	-	SN	Level-1-260C-UNLIM	-40 to 125	LMV604MA
LMV604MT/NOPB	Active	Production	TSSOP (PW) | 14	94 | TUBE	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LMV604 MT
LMV604MT/NOPB.A	Active	Production	TSSOP (PW) | 14	94 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMV604 MT
LMV604MTX/NOPB	Active	Production	TSSOP (PW) | 14	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LMV604 MT

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMV604MTX/NOPB.A	Active	Production	TSSOP (PW) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMV604 MT

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

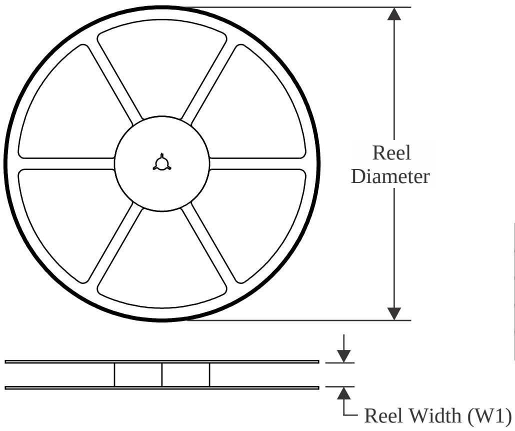
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

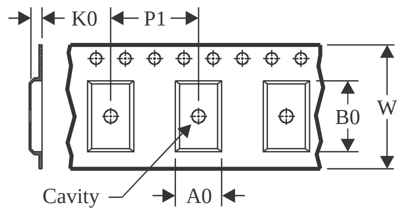
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

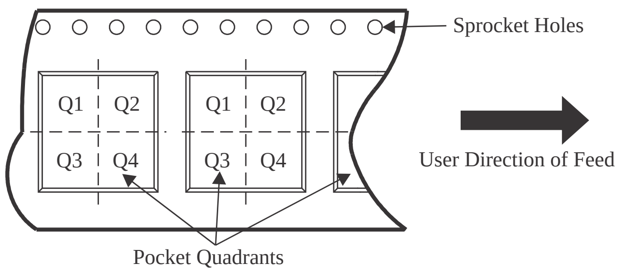


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

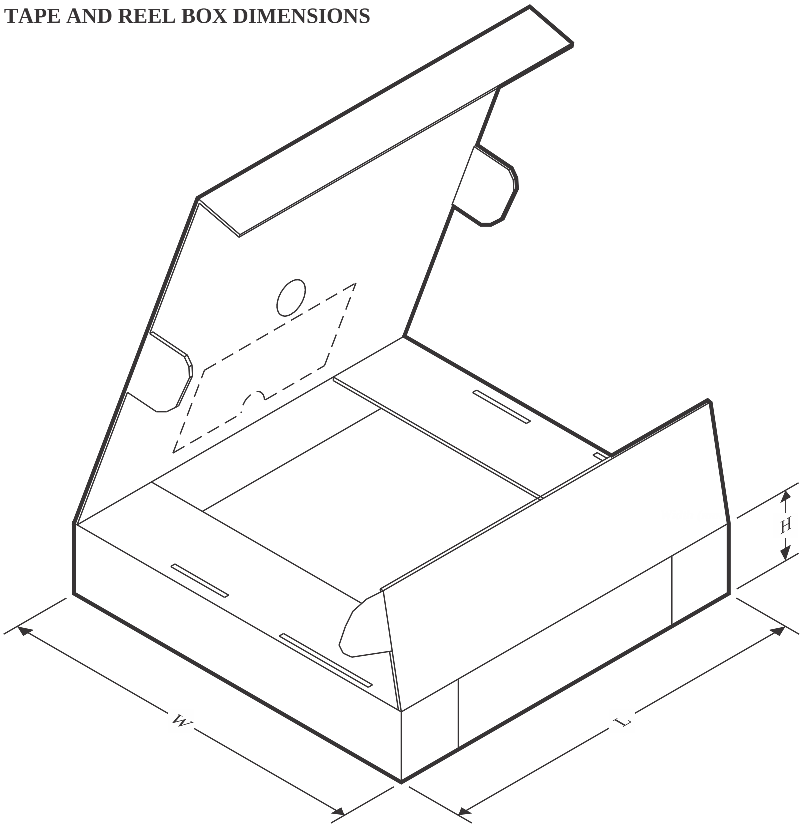
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV601MG/NOPB	SC70	DCK	6	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV601MGX/NOPB	SC70	DCK	6	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV602MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMV602MM/NOPB	VSSOP	DGK	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV602MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV604MAX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMV604MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

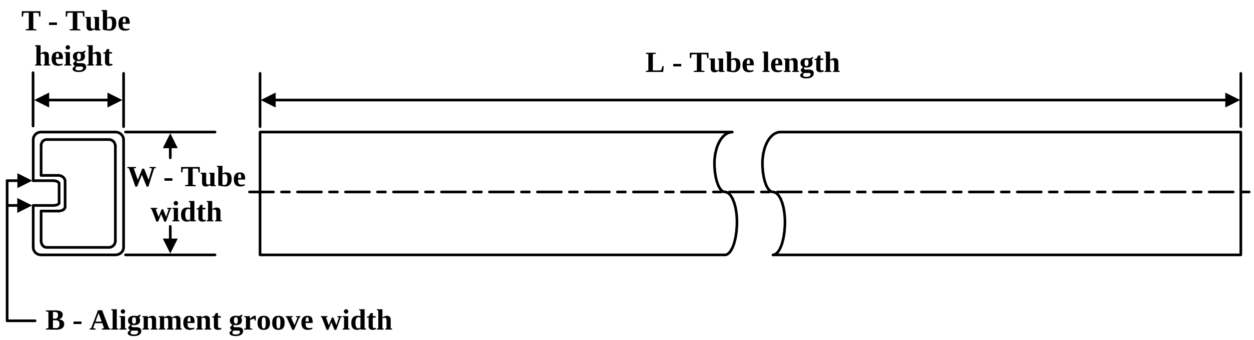
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

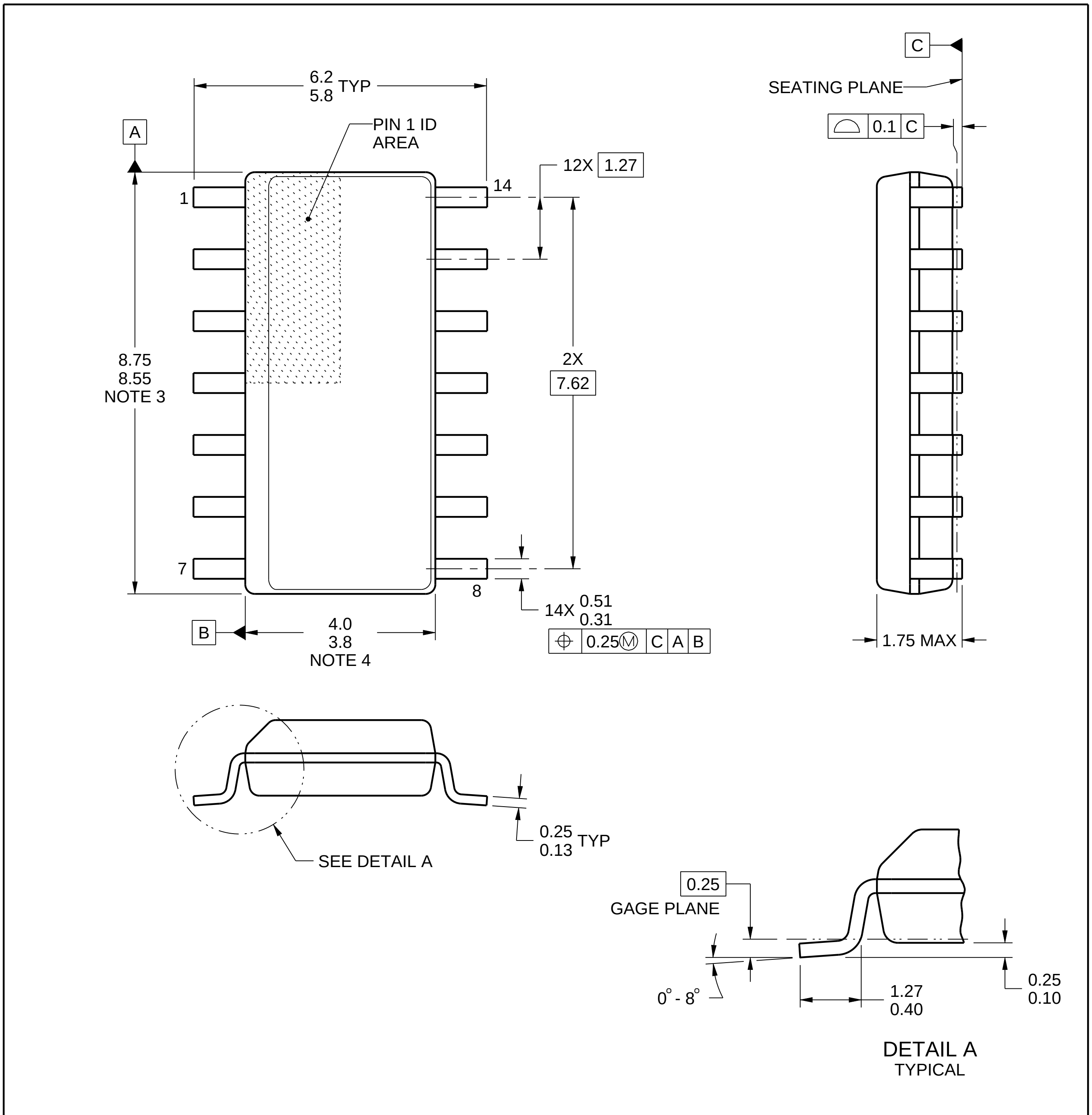
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV601MG/NOPB	SC70	DCK	6	1000	208.0	191.0	35.0
LMV601MGX/NOPB	SC70	DCK	6	3000	208.0	191.0	35.0
LMV602MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMV602MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LMV602MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMV604MAX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0
LMV604MTX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

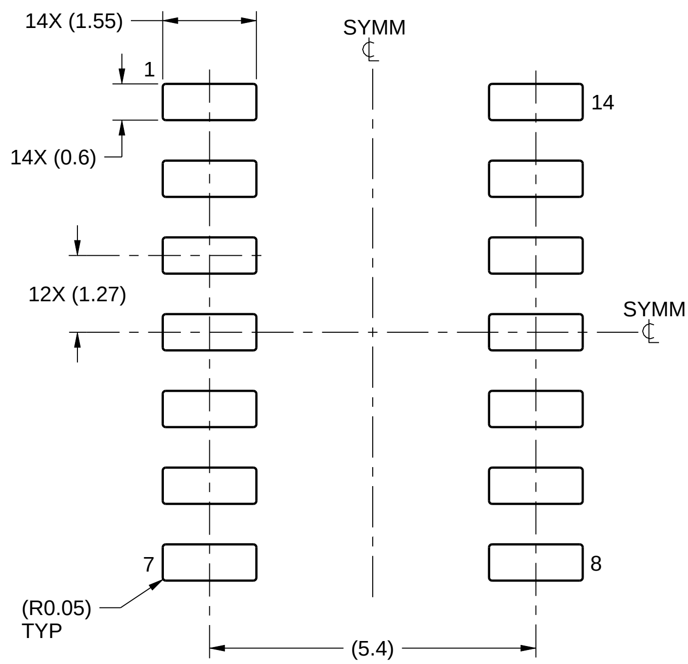
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMV602MA/NOPB	D	SOIC	8	95	495	8	4064	3.05
LMV602MA/NOPB.A	D	SOIC	8	95	495	8	4064	3.05
LMV604MA/NOPB	D	SOIC	14	55	495	8	4064	3.05
LMV604MA/NOPB.A	D	SOIC	14	55	495	8	4064	3.05
LMV604MA/NOPB.B	D	SOIC	14	55	495	8	4064	3.05
LMV604MT/NOPB	PW	TSSOP	14	94	530	10.2	3600	3.5
LMV604MT/NOPB	PW	TSSOP	14	94	495	8	2514.6	4.06
LMV604MT/NOPB.A	PW	TSSOP	14	94	530	10.2	3600	3.5
LMV604MT/NOPB.A	PW	TSSOP	14	94	495	8	2514.6	4.06



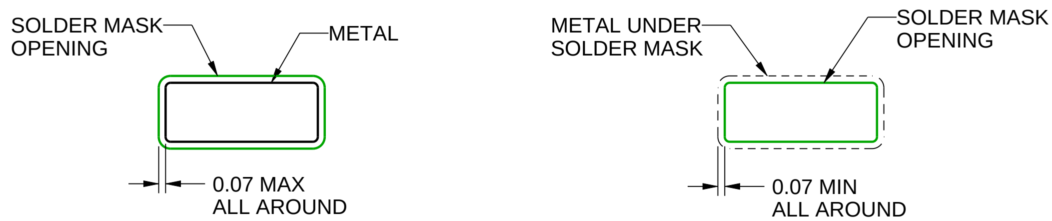
4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



NON SOLDER MASK
DEFINED

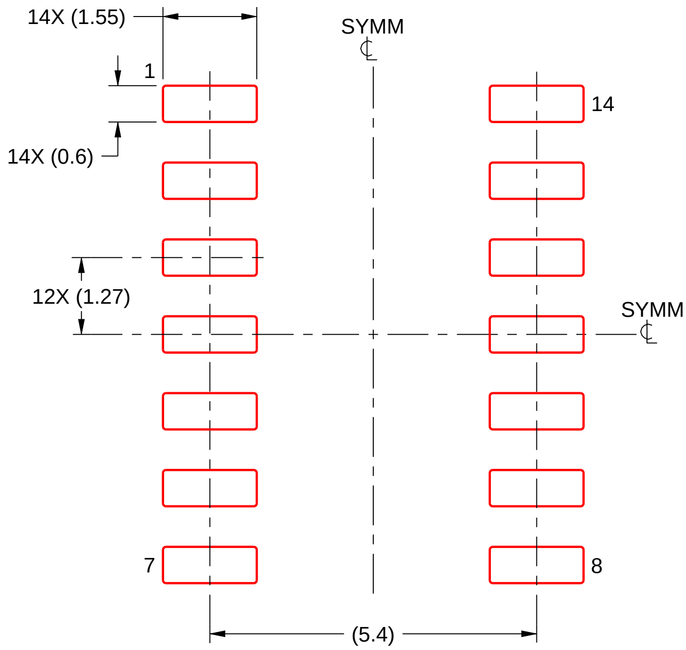
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

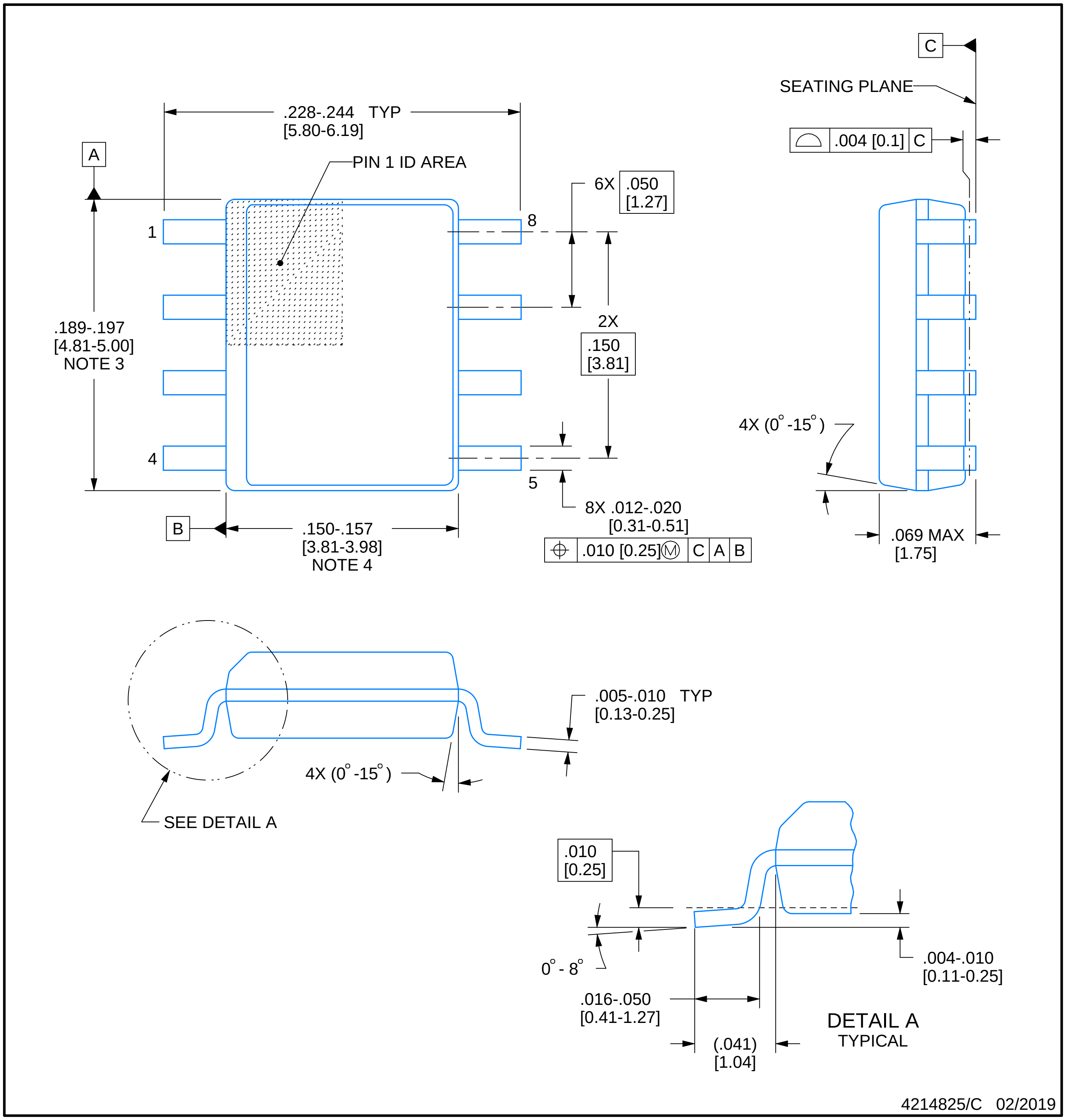


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

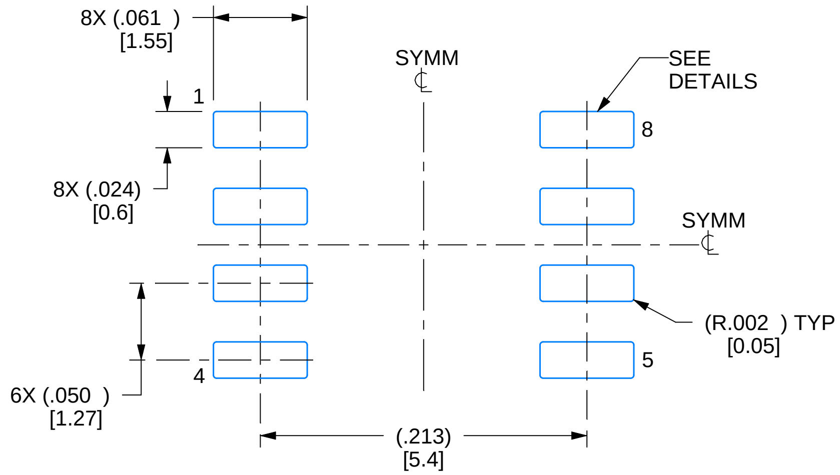
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

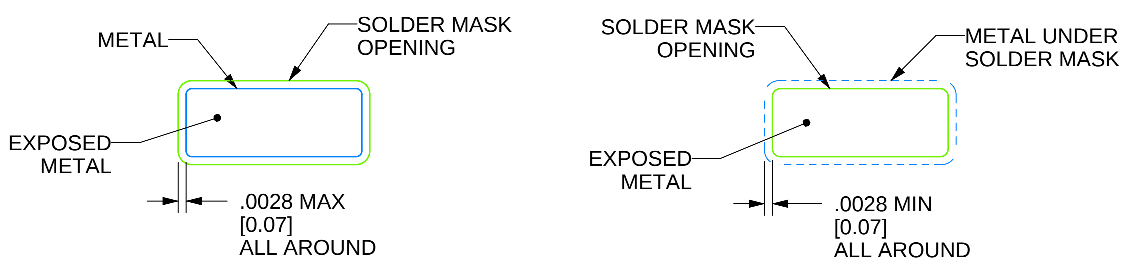


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED

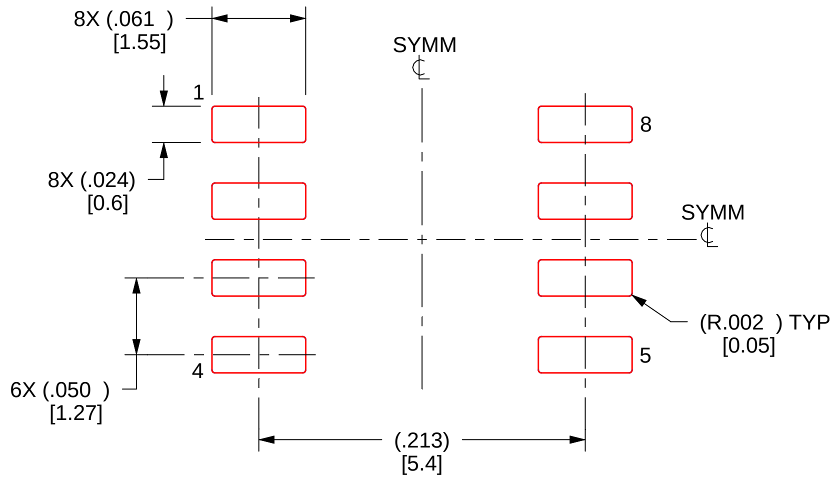
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

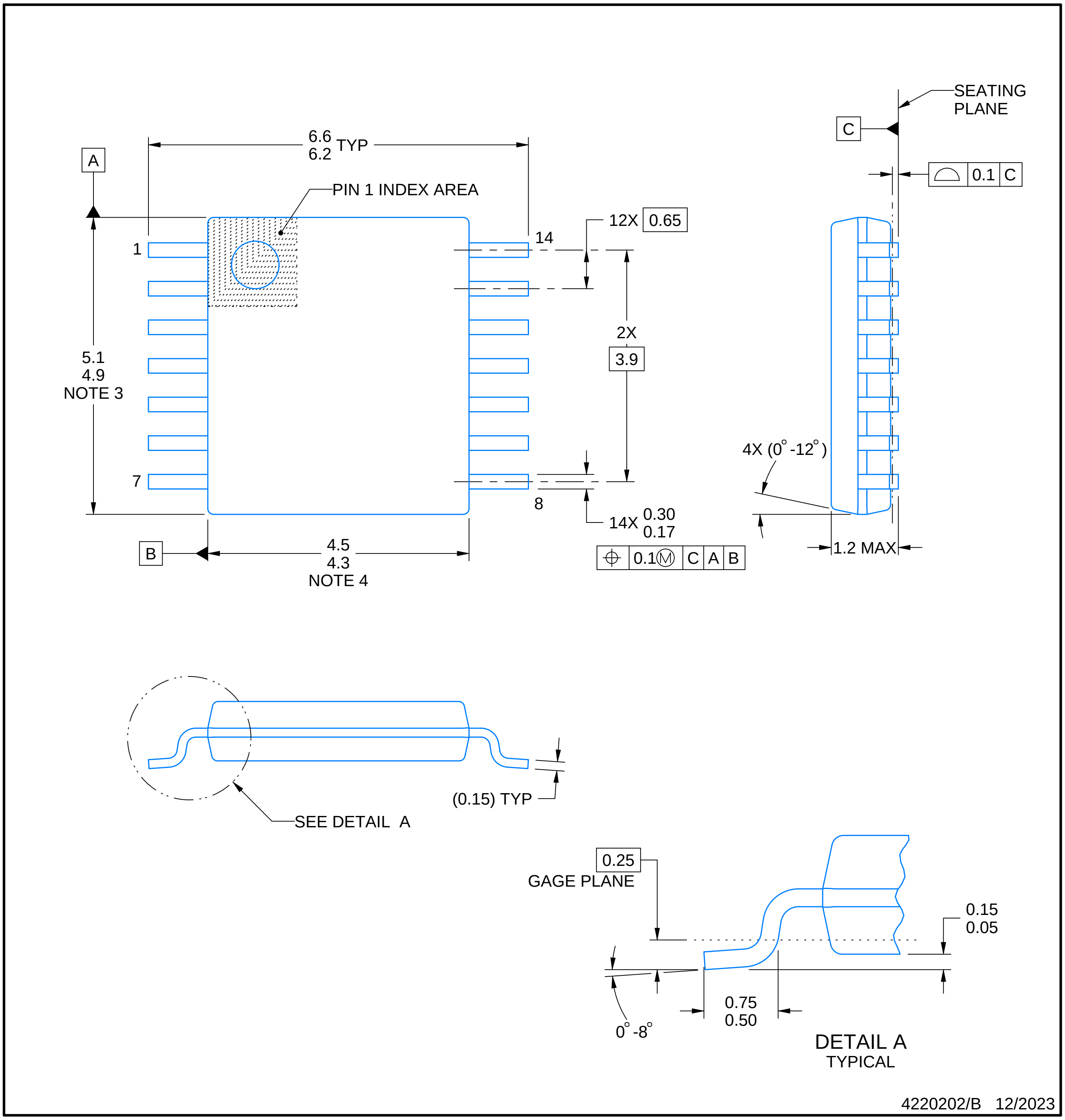


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

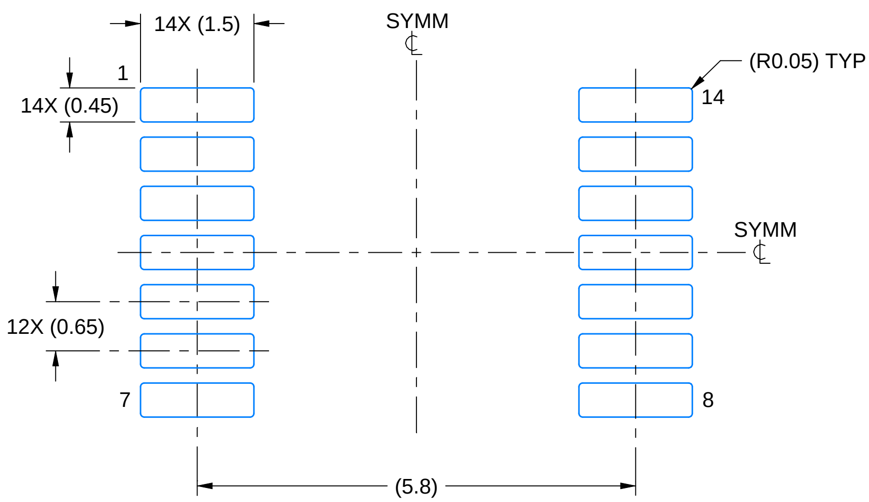
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

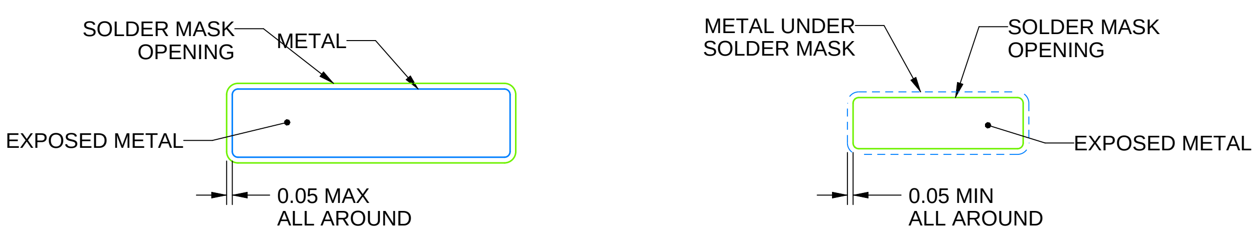


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

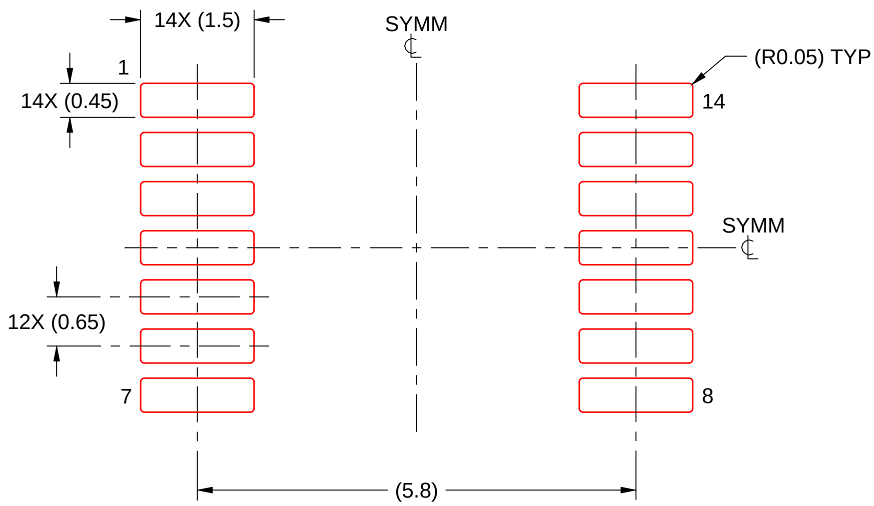


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

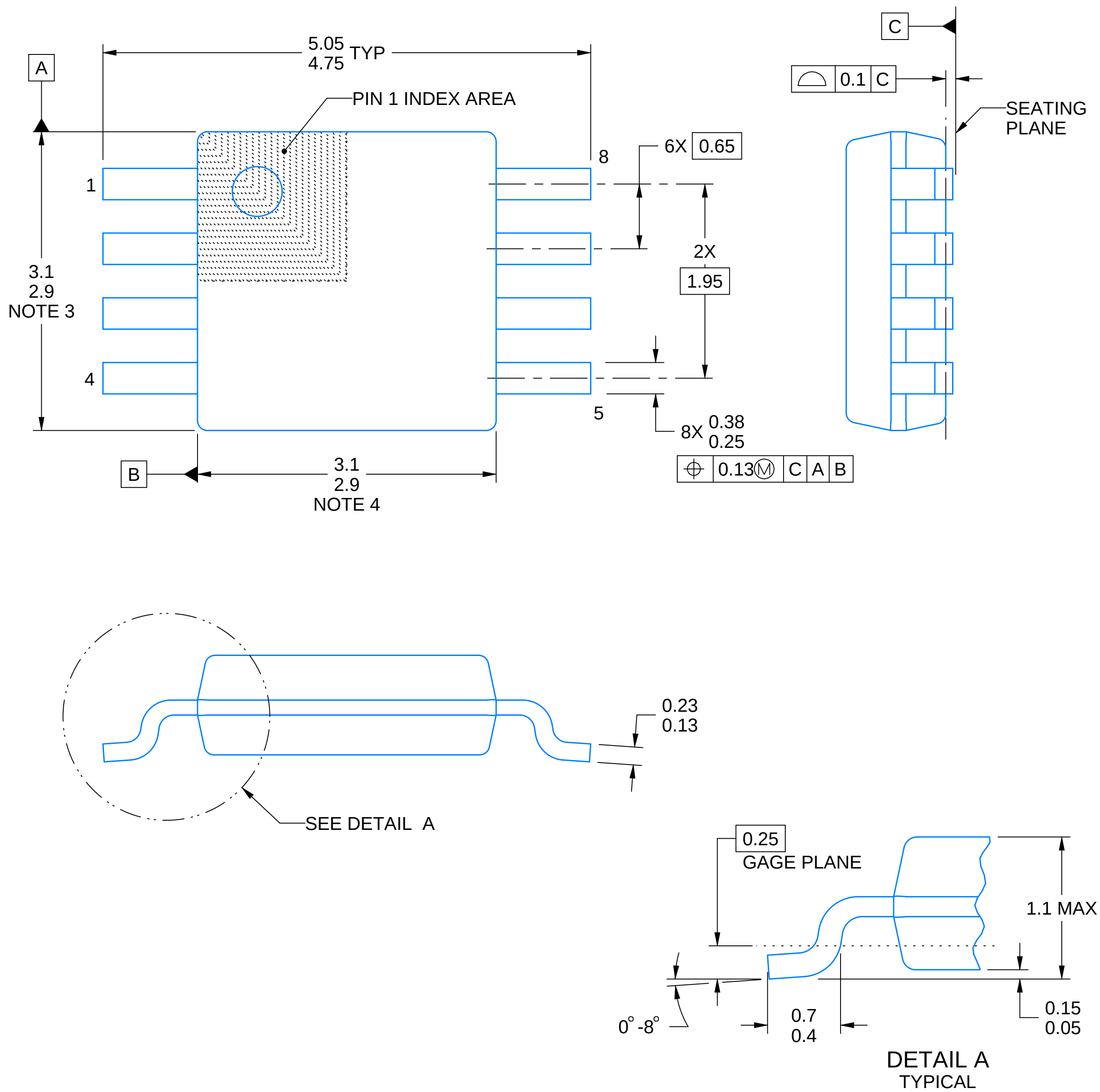


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

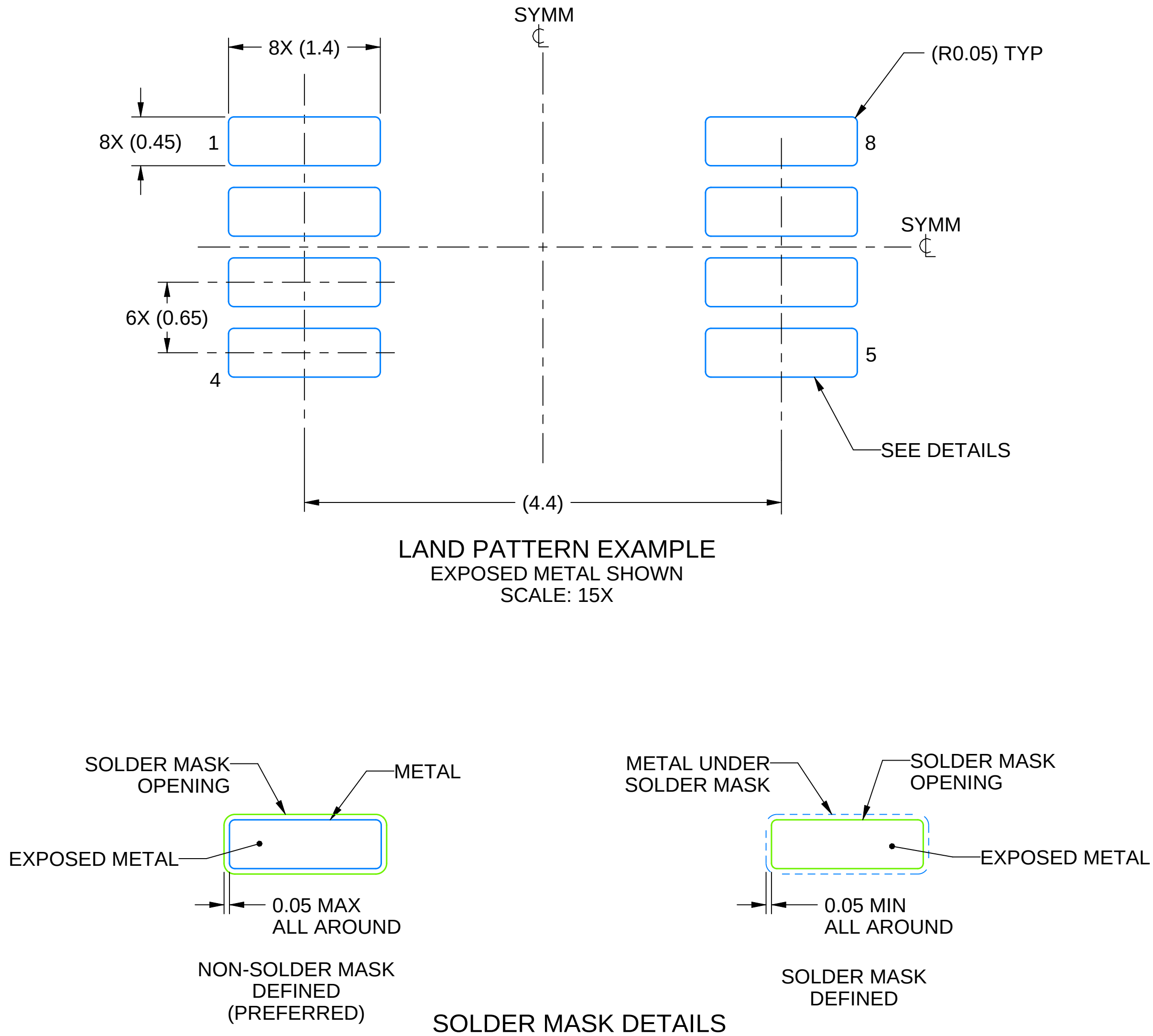


4214862/A 04/2023

PowerPAD is a trademark of Texas Instruments.

NOTES:

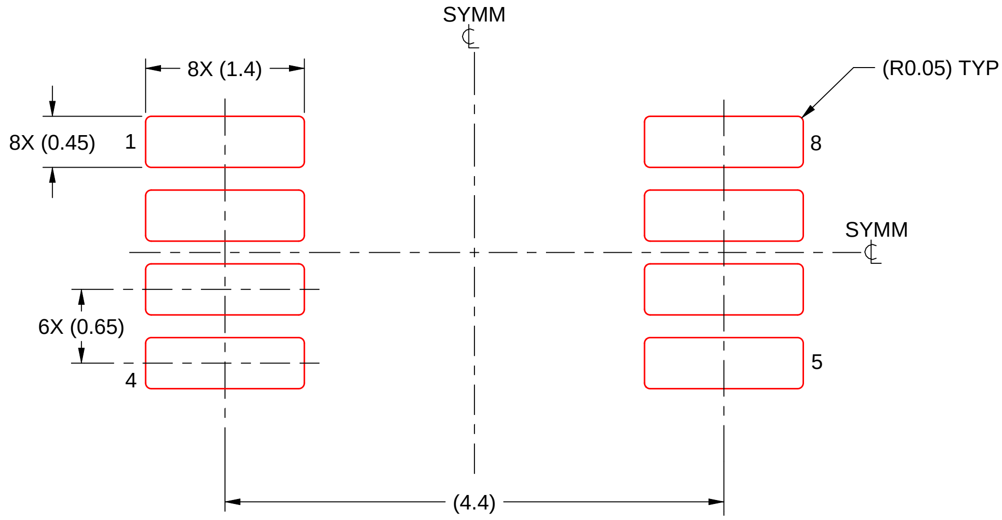
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

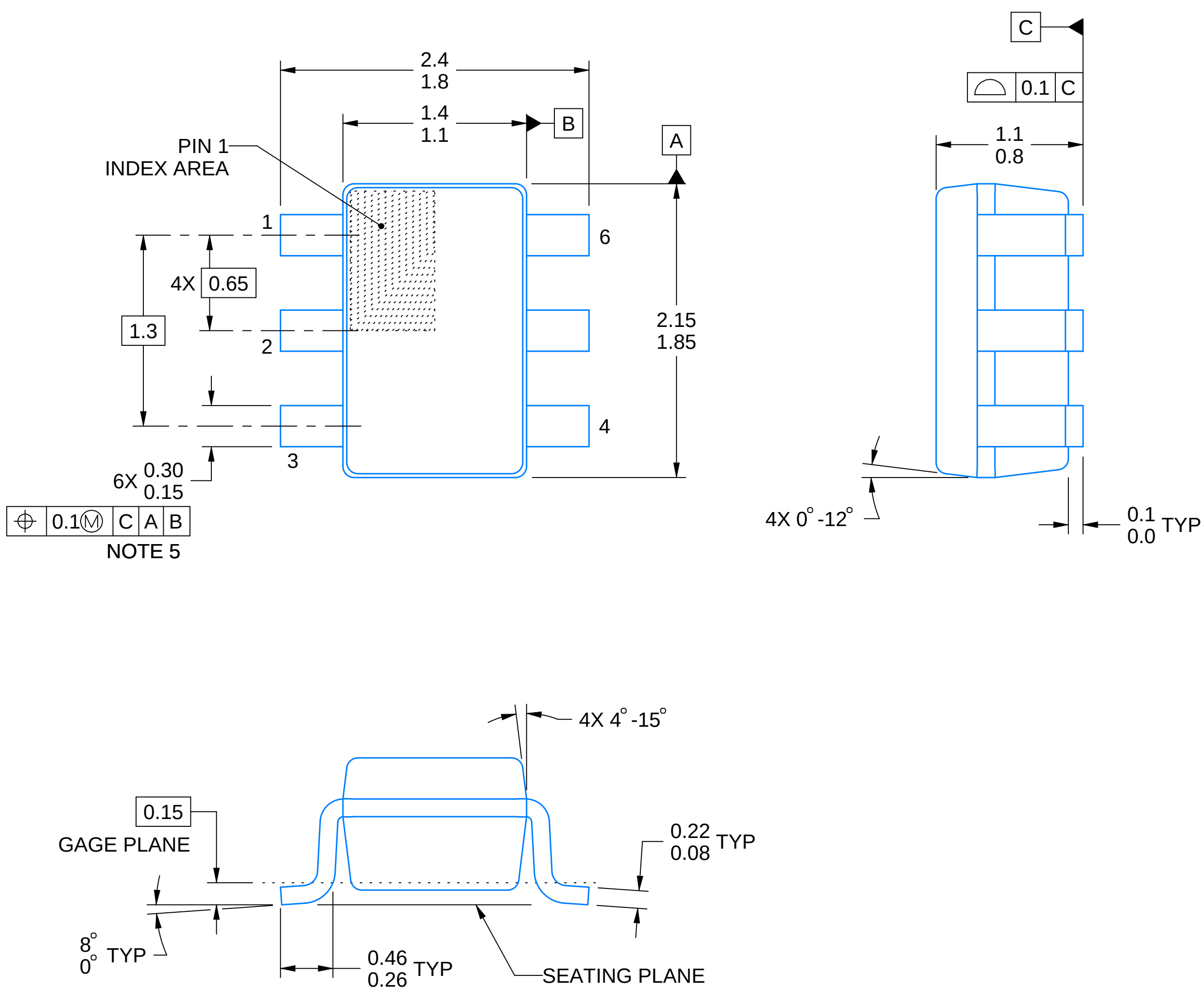


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

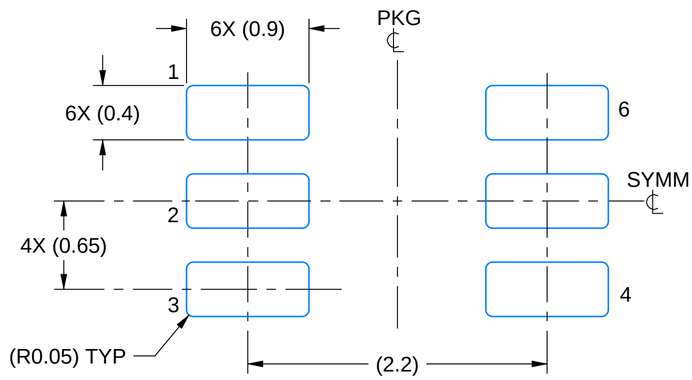
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



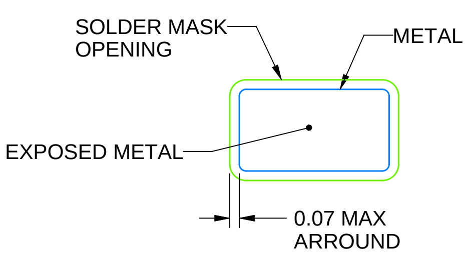
4214835/D 11/2024

NOTES:

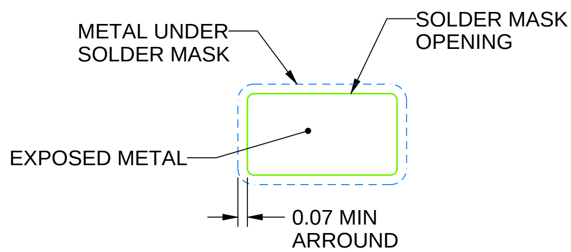
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



NON SOLDER MASK
DEFINED
(PREFERRED)



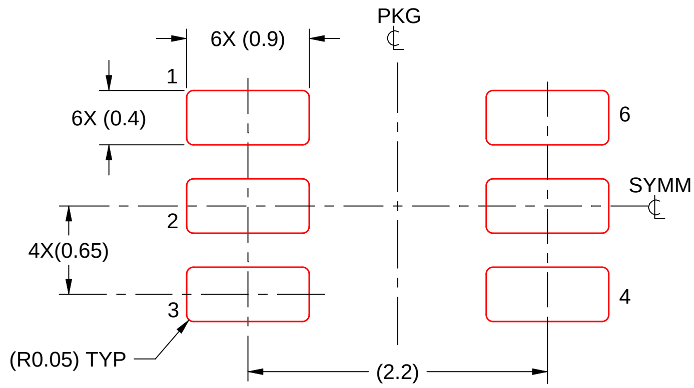
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214835/D 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/D 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.