LMR62014 SIMPLE SWITCHER® 20Vout, 1.4A Step-Up Voltage Regulator in SOT-23

Check for Samples: LMR62014

FEATURES

- **Input Voltage Range of 2.7V to 14V**
- **Output Voltage up to 20V**
- **Switch Current up to 1.4A**
- **1.6 MHz Switching Frequency**
- **Low Shutdown Iq, <1 µA**
- **Cycle-by-Cycle Current Limiting**
- **Internally Compensated**
- **5-Pin SOT-23 Packaging (2.92 x 2.84 x 1.08mm)**
- **Fully Enabled for WEBENCH® Power Designer**

PERFORMANCE BENEFITS

- **Extremely Easy to Use**
- **Tiny Overall Solution Reduces System Cost**

APPLICATIONS

- **Boost Conversions from 3.3V, 5V, and 12V Rails**
- **Space Constrained Applications**
- **Embedded Systems**
- **LCD Displays**
- **LED Applications**

DESCRIPTION

The LMR62014 switching regulator is a current-mode boost converter operating at fixed frequency of 1.6 MHz.

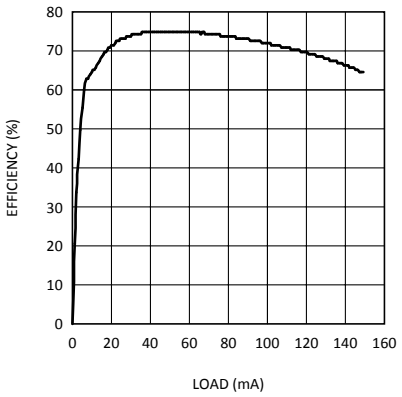
The use of SOT-23 package, made possible by the minimal power loss of the internal 1.4A switch, and use of small inductors and capacitors result in the industry's highest power density. The LMR62014 is capable of greater than 90% duty cycle, making it ideal for boosting to voltages up to 20V.

These parts have a logic-level shutdown pin that can be used to reduce quiescent current and extend battery life.

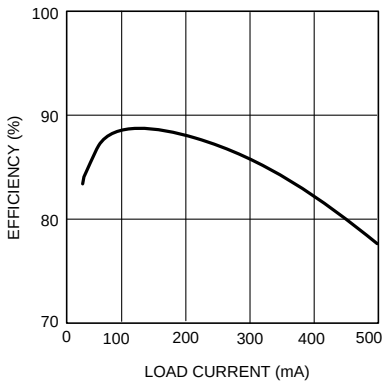
Protection is provided through cycle-by-cycle current limiting and thermal shutdown. Internal compensation simplifies design and reduces component count.

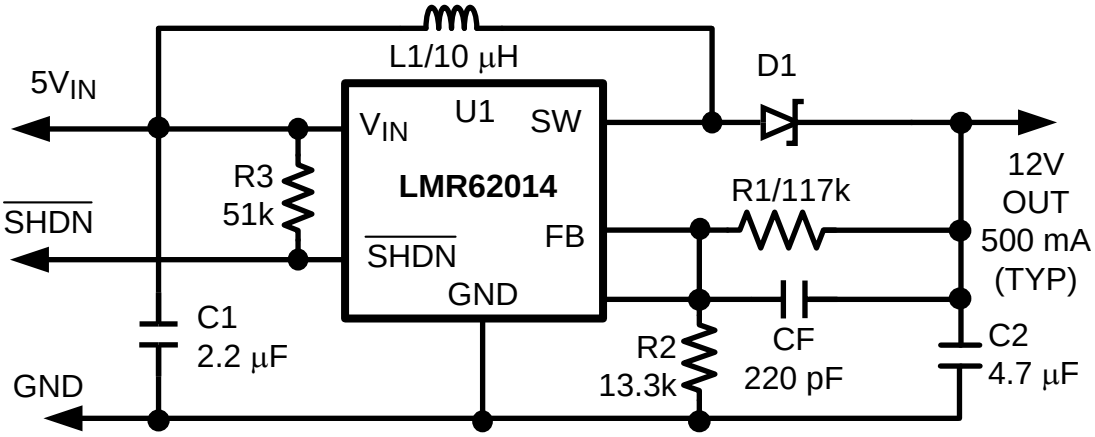
System Performance

Efficiency vs Load Current
V_{IN} = 3.3V, V_{OUT} = 12V



Efficiency vs Load Current
V_{IN} = 5V, V_{OUT} = 12V





Connection Diagram

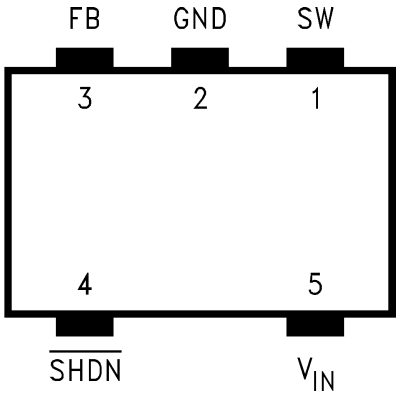


Figure 1. 5-Lead SOT-23 (Top View)
See DBV Package

PIN DESCRIPTIONS

Pin	Name	Function
1	SW	Drain of the internal FET switch.
2	GND	Analog and power ground.
3	FB	Feedback point that connects to external resistive divider.
4	$\overline{SHDN}$	Shutdown control input. Connect to Vin if the feature is not used.
5	V_{IN}	Analog and power input.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	−40°C to +125°C
Lead Temp. (Soldering, 5 sec.)	300°C
Power Dissipation(3)	Internally Limited
FB Pin Voltage	−0.4V to +6V
SW Pin Voltage	−0.4V to +22V
Input Supply Voltage	−0.4V to +14.5V
$\overline{SHDN}$ Pin Voltage	−0.4V to VIN + 0.3V
θ_{J-A} (SOT-23)	265°C/W
ESD Rating Human Body Model(4)	2 kV
For soldering specifications see SNOA549	

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of the limits set forth under the operating ratings which specify the intended range of operating conditions.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

(3) The maximum power dissipation which can be safely dissipated for any application is a function of the maximum junction temperature, $T_J(MAX)$ = 125°C, the junction-to-ambient thermal resistance for the SOT-23 package, θ_{J-A} = 265°C/W, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature for designs using this device can be calculated using the formula: $P_{(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{J-A}} = \frac{125 - T_A}{265}$ If power dissipation exceeds the maximum specified above, the internal thermal protection circuitry will protect the device by reducing the output voltage as required to maintain a safe junction temperature.

(4) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.

Electrical Characteristics

Limits in standard typeface are for T_J = 25°C, and limits in **boldface type** apply over the full operating temperature range (−40°C ≤ T_J ≤ +125°C). Unless otherwise specified: V_{IN} = 5V, V_{SHDN} = 5V, I_L = 0A.

Symbol	Parameter	Conditions		Min (1)	Typical (2)	Max (1)	Units
V_{IN}	Input Voltage			**2.7**		**14**	V
$V_{OUT\ (MIN)}$	Minimum Output Voltage Under Load	R_L = 43Ω (3)	V_{IN} = 2.7V	**5.4**	7		V
			V_{IN} = 3.3V	**8**	10		
			V_{IN} = 5V	**13**	17		
		R_L = 15Ω (3)	V_{IN} = 2.7V	**3.75**	5		
			V_{IN} = 3.3V	**5**	6.5		
			V_{IN} = 5V	**8.75**	11		
I_{SW}	Switch Current Limit	See (4)		1.8 **1.4**	2		A
$R_{DS}(ON)$	Switch ON Resistance	I_{SW} = 100 mA, Vin = 5V			260	400 **500**	mΩ
		I_{SW} = 100 mA, Vin = 3.3V			300	450 **550**	
$SHDN_{TH}$	Shutdown Threshold	Device ON		**1.5**			V
		Device OFF				**0.50**	
I_{SHDN}	Shutdown Pin Bias Current	V_{SHDN} = 0			0		µA
		V_{SHDN} = 5V			0	**2**	
V_{FB}	Feedback Pin Reference Voltage	V_{IN} = 3V		**1.205**	1.230	**1.255**	V
I_{FB}	Feedback Pin Bias Current	V_{FB} = 1.23V			60	**500**	nA
I_Q	Quiescent Current	V_{SHDN} = 5V, Switching			2	**3.0**	mA
		V_{SHDN} = 5V, Not Switching			400	**500**	µA
		V_{SHDN} = 0			0.024	1	
$\frac{\Delta V_{FB}}{\Delta V_{IN}}$	FB Voltage Line Regulation	2.7V ≤ V_{IN} ≤ 14V			0.02		%/V
F_{SW}	Switching Frequency (5)			**1**	1.6	**1.85**	MHz
D_{MAX}	Maximum Duty Cycle (5)			**86**	93		%
I_L	Switch Leakage	Not Switching V_{SW} = 5V				1	µA

(1) Limits are ensured by testing, statistical correlation, or design.
(2) Typical values are derived from the mean value of a large quantity of samples tested during characterization and represent the most likely expected value of the parameter at room temperature.
(3) L = 10 µH, C_{OUT} = 4.7 µF, duty cycle = maximum
(4) Switch current limit is dependent on duty cycle (see Typical Performance Characteristics).
(5) Specified limits are the same for Vin = 3.3V input.

Typical Performance Characteristics

Unless otherwise specified: V_{IN} = 5V, $\overline{SHDN}$ pin tied to V_{IN}.

Iq Vin (Active) vs Temperature

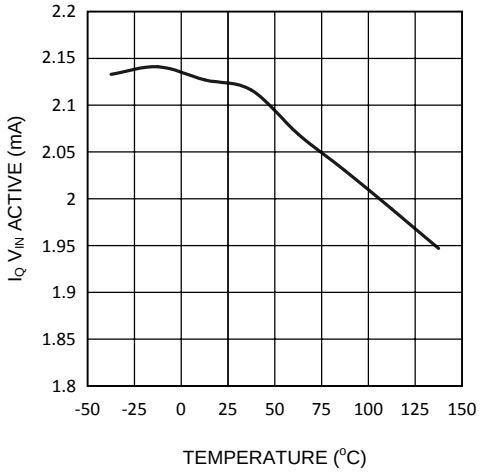


Figure 2.

Oscillator Frequency vs Temperature

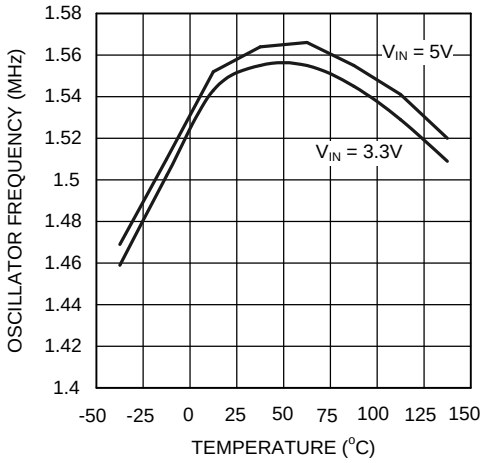


Figure 3.

Max. Duty Cycle vs Temperature

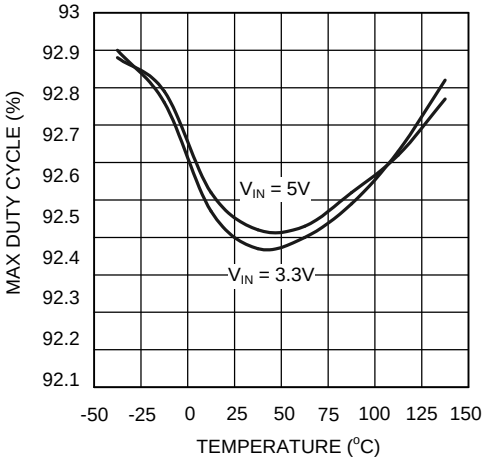


Figure 4.

Iq Vin (Idle) vs Temperature

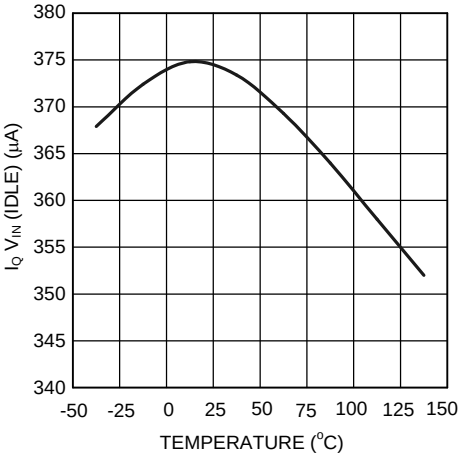


Figure 5.

Feedback Bias Current vs Temperature

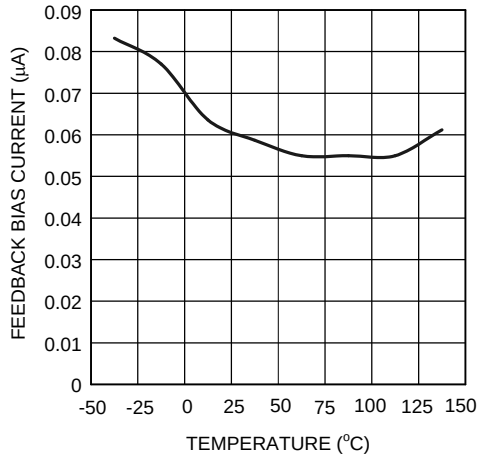


Figure 6.

Feedback Voltage vs Temperature

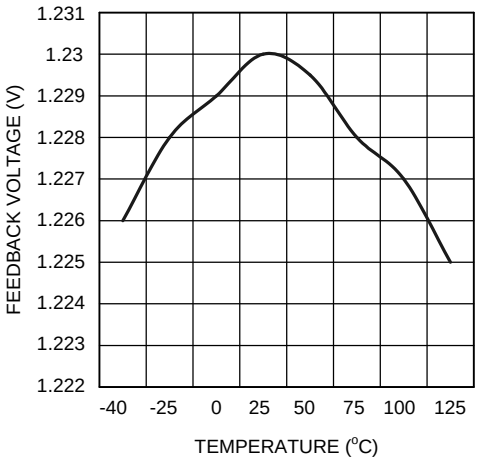


Figure 7.

Typical Performance Characteristics (continued)

Unless otherwise specified: V_{IN} = 5V, $\overline{SHDN}$ pin tied to V_{IN}.

R_{DS}(ON) vs Temperature

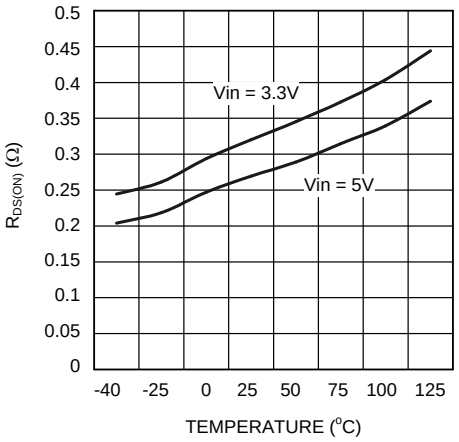


Figure 8.

Current Limit vs Temperature

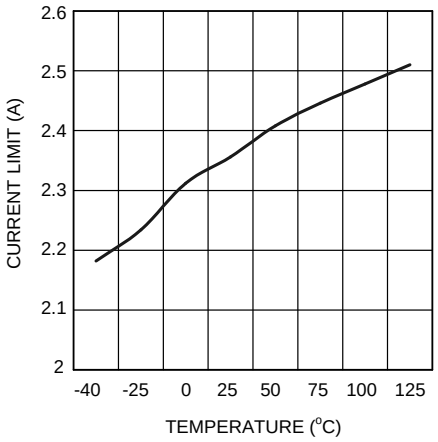


Figure 9.

R_{DS}(ON) vs V_{IN}

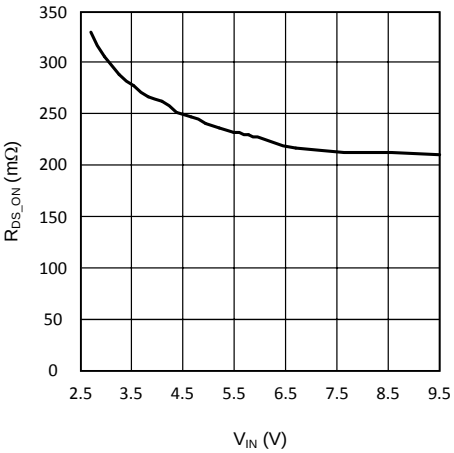


Figure 10.

Efficiency vs Load Current
V_{IN} = 2.7V, V_{OUT} = 5V

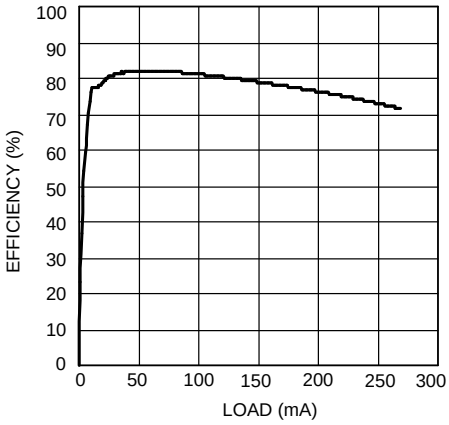


Figure 11.

Efficiency vs Load Current
V_{IN} = 3.3V, V_{OUT} = 5V

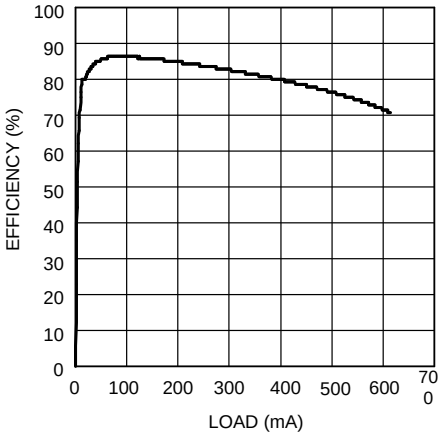


Figure 12.

Efficiency vs Load Current
V_{IN} = 4.2V, V_{OUT} = 5V

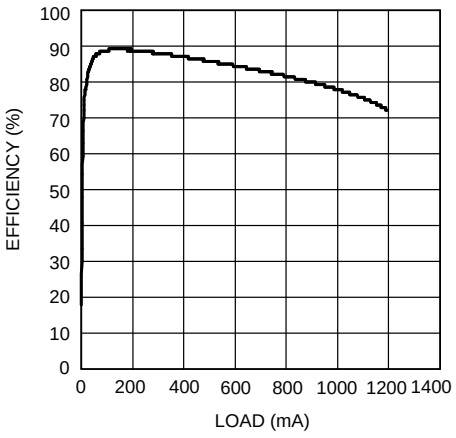


Figure 13.

Typical Performance Characteristics (continued)

Unless otherwise specified: V_{IN} = 5V, $\overline{SHDN}$ pin tied to V_{IN}.

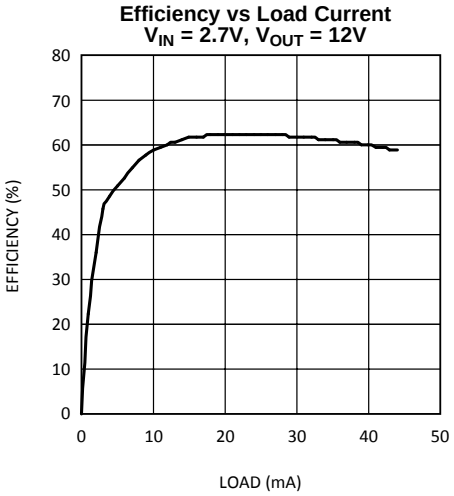


Figure 14.

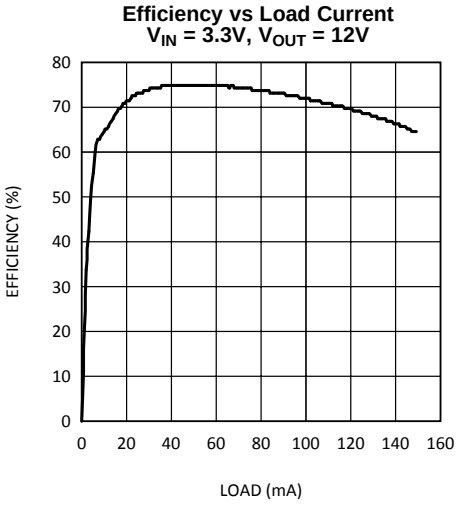


Figure 15.

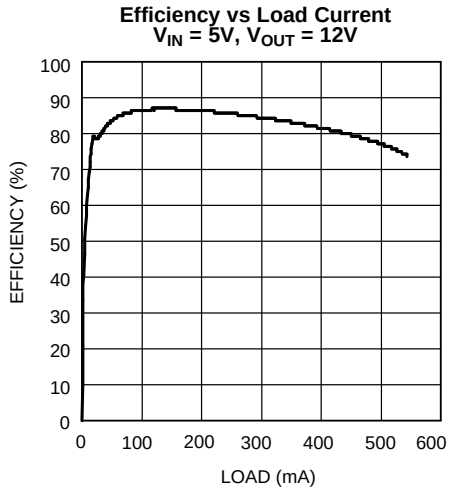


Figure 16.

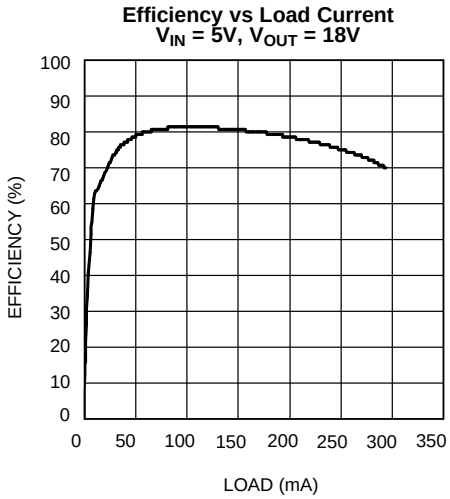
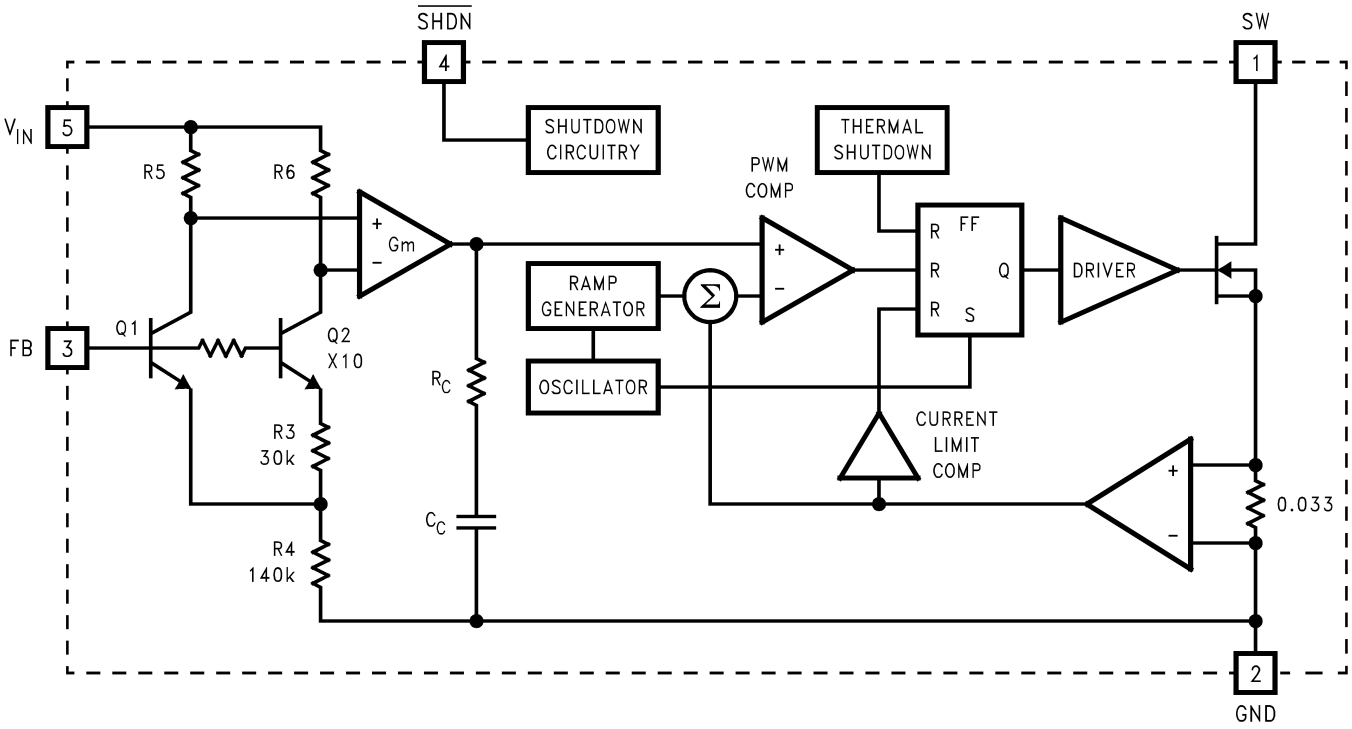


Figure 17.

Block Diagram



THEORY OF OPERATION

The LMR62014 is a switching converter IC that operates at a fixed frequency (1.6 MHz) for fast transient response over a wide input voltage range and incorporates pulse-by-pulse current limiting protection. Because this is current mode control, a 33 mΩ sense resistor in series with the switch FET is used to provide a voltage (which is proportional to the FET current) to both the input of the pulse width modulation (PWM) comparator and the current limit amplifier.

At the beginning of each cycle, the S-R latch turns on the FET. As the current through the FET increases, a voltage (proportional to this current) is summed with the ramp coming from the ramp generator and then fed into the input of the PWM comparator. When this voltage exceeds the voltage on the other input (coming from the Gm amplifier), the latch resets and turns the FET off. Since the signal coming from the Gm amplifier is derived from the feedback (which samples the voltage at the output), the action of the PWM comparator constantly sets the correct peak current through the FET to keep the output voltage in regulation.

Q1 and Q2 along with R3 - R6 form a bandgap voltage reference used by the IC to hold the output in regulation. The currents flowing through Q1 and Q2 will be equal, and the feedback loop will adjust the regulated output to maintain this. Because of this, the regulated output is always maintained at a voltage level equal to the voltage at the FB node "multiplied up" by the ratio of the output resistive divider.

The current limit comparator feeds directly into the flip-flop that drives the switch FET. If the FET current reaches the limit threshold, the FET is turned off and the cycle terminated until the next clock pulse. The current limit input terminates the pulse regardless of the status of the output of the PWM comparator.

Application Hints

SELECTING THE EXTERNAL CAPACITORS

The best capacitors for use with the LMR62014 are multi-layer ceramic capacitors. They have the lowest ESR (equivalent series resistance) and highest resonance frequency which makes them optimum for use with high frequency switching converters.

When selecting a ceramic capacitor, only X5R and X7R dielectric types should be used. Other types such as Z5U and Y5F have such severe loss of capacitance due to effects of temperature variation and applied voltage, they may provide as little as 20% of rated capacitance in many typical applications. Always consult capacitor manufacturer’s data curves before selecting a capacitor.

SELECTING THE OUTPUT CAPACITOR

A single ceramic capacitor of value 4.7 µF to 10 µF will provide sufficient output capacitance for most applications. If larger amounts of capacitance are desired for improved line support and transient response, tantalum capacitors can be used. Aluminum electrolytics with ultra low ESR such as Sanyo Oscon can be used, but are usually prohibitively expensive. Typical AI electrolytic capacitors are not suitable for switching frequencies above 500 kHz due to significant ringing and temperature rise due to self-heating from ripple current. An output capacitor with excessive ESR can also reduce phase margin and cause instability.

In general, if electrolytics are used, it is recommended that they be paralleled with ceramic capacitors to reduce ringing, switching losses, and output voltage ripple.

SELECTING THE INPUT CAPACITOR

An input capacitor is required to serve as an energy reservoir for the current which must flow into the coil each time the switch turns ON. This capacitor must have extremely low ESR, so ceramic is the best choice. We recommend a nominal value of 2.2 µF, but larger values can be used. Since this capacitor reduces the amount of voltage ripple seen at the input pin, it also reduces the amount of EMI passed back along that line to other circuitry.

FEED-FORWARD COMPENSATION

Although internally compensated, the feed-forward capacitor Cf is required for stability (see Basic Application Circuit). Adding this capacitor puts a zero in the loop response of the converter. The recommended frequency for the zero fz should be approximately 6 kHz. Cf can be calculated using the formula:

$$Cf = 1 / (2 \times \pi \times R1 \times fz) \quad (1)$$

SELECTING DIODES

The external diode used in the typical application should be a Schottky diode.The diode must be rated to handle the maximum output voltage and load current. A 20V diode such as the MBR0520 is recommended.

The MBR05XX series of diodes are designed to handle a maximum average current of 0.5A. For applications exceeding 0.5A average, a Toshiba CRS08 can be used.

LAYOUT HINTS

High frequency switching regulators require very careful layout of components in order to get stable operation and low noise. All components must be as close as possible to the LMR62014 device. It is recommended that a 4-layer PCB be used so that internal ground planes are available.

As an example, a recommended layout of components is shown:

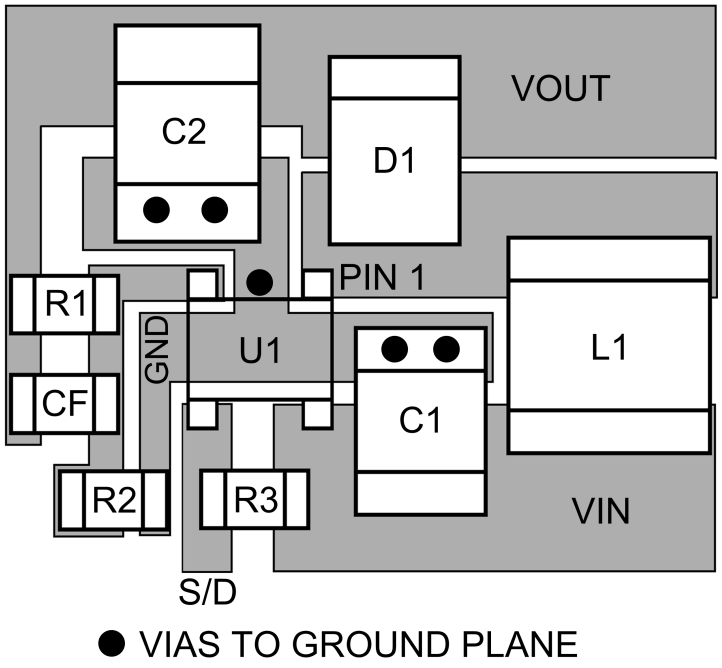


Figure 18. Recommended PCB Component Layout

Some additional guidelines to be observed:

1. Keep the path between L1, D1, and C2 extremely short. Parasitic trace inductance in series with D1 and C2 will increase noise and ringing.
2. The feedback components R1, R2 and CF must be kept close to the FB pin of U1 to prevent noise injection on the FB pin trace.
3. If internal ground planes are available (recommended) use vias to connect directly to ground at pin 2 of U1, as well as the negative sides of capacitors C1 and C2.

SETTING THE OUTPUT VOLTAGE

The output voltage is set using the external resistors R1 and R2 (see Basic Application Circuit). A value of approximately 13.3 kΩ is recommended for R2 to establish a divider current of approximately 92 µA. R1 is calculated using the formula:

$$R1 = R2 \times (V_{OUT}/1.23 - 1) \quad (2)$$

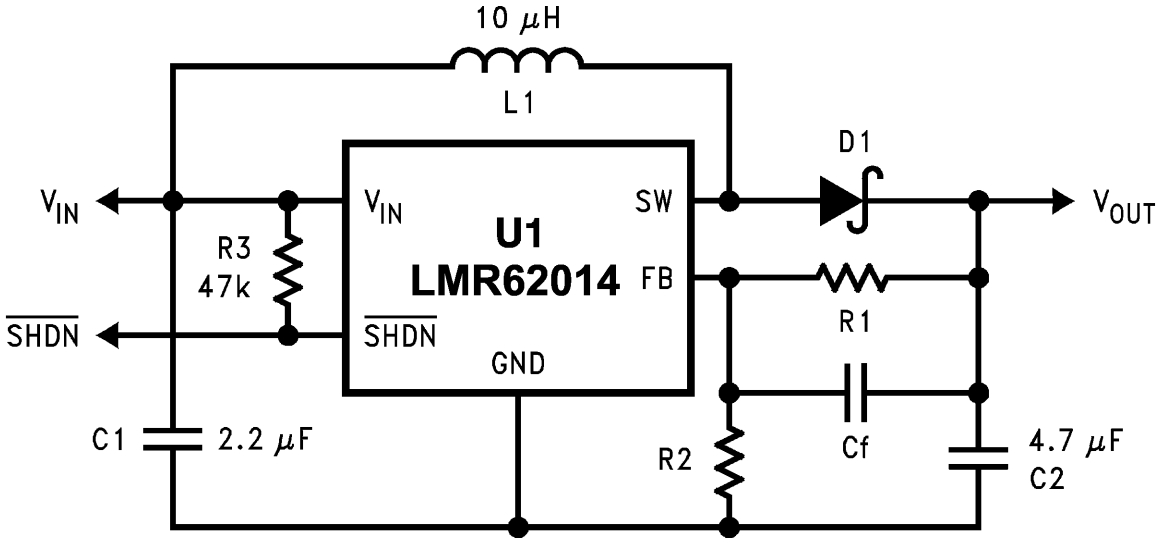


Figure 19. Basic Application Circuit

DUTY CYCLE

The maximum duty cycle of the switching regulator determines the maximum boost ratio of output-to-input voltage that the converter can attain in continuous mode of operation. The duty cycle for a given boost application is defined as:

$$\text{Duty Cycle} = \frac{V_{OUT} + V_{DIODE} - V_{IN}}{V_{OUT} + V_{DIODE} - V_{SW}} \quad (3)$$

This applies for continuous mode operation.

INDUCTANCE VALUE

The first question we are usually asked is: “How small can I make the inductor?” (because they are the largest sized component and usually the most costly). The answer is not simple and involves trade-offs in performance. Larger inductors mean less inductor ripple current, which typically means less output voltage ripple (for a given size of output capacitor). Larger inductors also mean more load power can be delivered because the energy stored during each switching cycle is:

$$E = L/2 \times (Ip)^2 \quad (4)$$

where

- “Ip” is the peak inductor current.

An important point to observe is that the LMR62014 will limit its switch current based on peak current. This means that since Ip(max) is fixed, increasing L will increase the maximum amount of power available to the load. Conversely, using too little inductance may limit the amount of load current which can be drawn from the output.

Best performance is usually obtained when the converter is operated in “continuous” mode at the load current range of interest, typically giving better load regulation and less output ripple. Continuous operation is defined as not allowing the inductor current to drop to zero during the cycle. It should be noted that all boost converters shift over to discontinuous operation as the output load is reduced far enough, but a larger inductor stays “continuous” over a wider load current range.

To better understand these trade-offs, a typical application circuit (5V to 12V boost with a 10 µH inductor) will be analyzed. We will assume:

V_{IN} = 5V, V_{OUT} = 12V, V_{DIODE} = 0.5V, V_{SW} = 0.5V (5)

Since the frequency is 1.6 MHz (nominal), the period is approximately 0.625 µs. The duty cycle will be 62.5%, which means the ON time of the switch is 0.390 µs. It should be noted that when the switch is ON, the voltage across the inductor is approximately 4.5V.

Using the equation:

V = L (di/dt) (6)

We can then calculate the di/dt rate of the inductor which is found to be 0.45 A/µs during the ON time. Using these facts, we can then show what the inductor current will look like during operation:

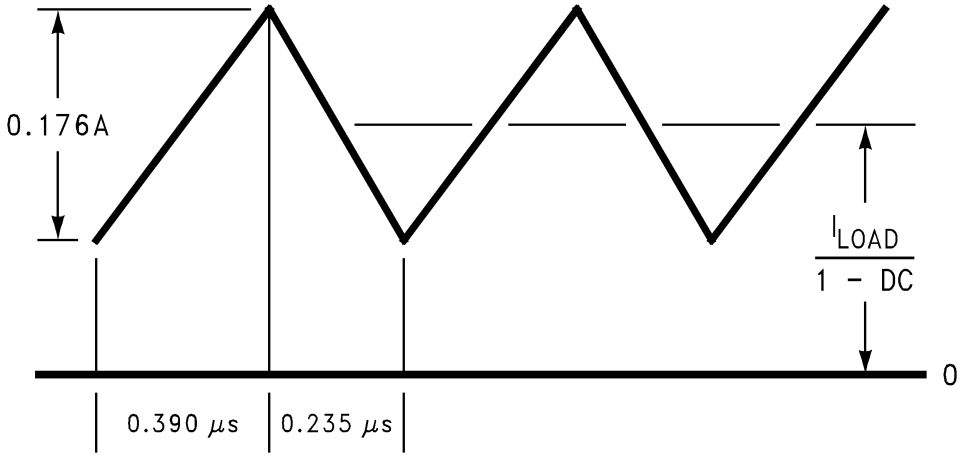


Figure 20. 10 µH Inductor Current, 5V–12V Boost (LMR62014X)

During the 0.390 µs ON time, the inductor current ramps up 0.176A and ramps down an equal amount during the OFF time. This is defined as the inductor “ripple current”. It can also be seen that if the load current drops to about 33 mA, the inductor current will begin touching the zero axis which means it will be in discontinuous mode. A similar analysis can be performed on any boost converter, to make sure the ripple current is reasonable and continuous operation will be maintained at the typical load current values.

MAXIMUM SWITCH CURRENT

The maximum FET switch current available before the current limiter cuts in is dependent on duty cycle of the application. This is illustrated in the graphs below which show typical values of switch current as a function of effective (actual) duty cycle:

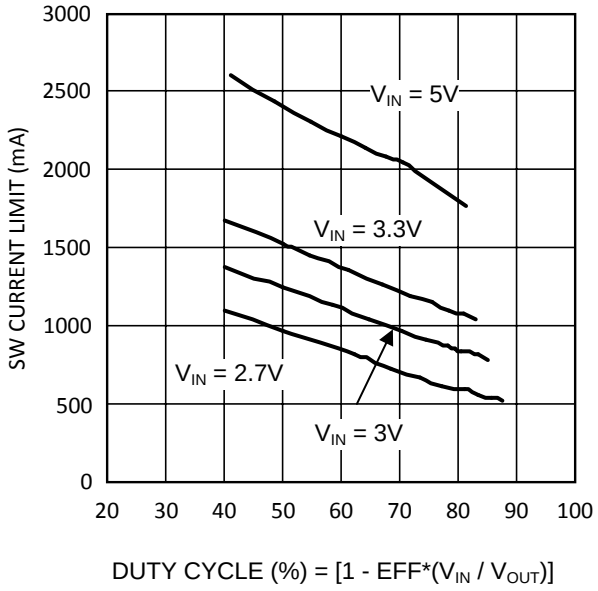


Figure 21. Switch Current Limit vs Duty Cycle

CALCULATING LOAD CURRENT

As shown in Figure 20 which depicts inductor current, the load current is related to the average inductor current by the relation:

$$I_{LOAD} = I_{IND}(AVG) \times (1 - DC)$$

where

- "DC" is the duty cycle of the application. (7)

The switch current can be found by:

$$I_{SW} = I_{IND}(AVG) + ½ (I_{RIPPLE}) \quad (8)$$

Inductor ripple current is dependent on inductance, duty cycle, input voltage and frequency:

$$I_{RIPPLE} = DC \times (V_{IN}-V_{SW}) / (f \times L) \quad (9)$$

combining all terms, we can develop an expression which allows the maximum available load current to be calculated:

$$I_{LOAD}(max) = (1 - DC) \times \left(I_{SW}(max) - \frac{DC\,(V_{IN} - V_{SW})}{2fL}\right) \quad (10)$$

The equation shown to calculate maximum load current takes into account the losses in the inductor or turn-OFF switching losses of the FET and diode. For actual load current in typical applications, we took bench data for various input and output voltages that displayed the maximum load current available for a typical device in graph form:

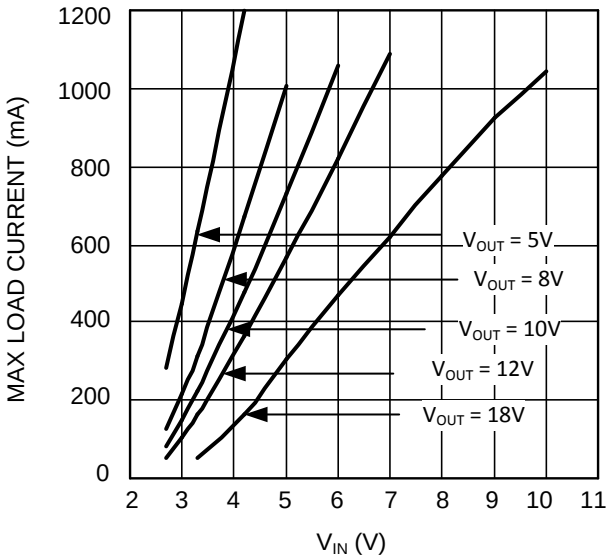


Figure 22. Max. Load Current (typ) vs V_{IN}

DESIGN PARAMETERS V_{SW} AND I_{SW}

The value of the FET "ON" voltage (referred to as V_{SW} in the equations) is dependent on load current. A good approximation can be obtained by multiplying the "ON Resistance" of the FET times the average inductor current.

FET on resistance increases at V_{IN} values below 5V, since the internal N-FET has less gate voltage in this input voltage range (see Typical Performance Characteristics curves). Above V_{IN} = 5V, the FET gate voltage is internally clamped to 5V.

The maximum peak switch current the device can deliver is dependent on duty cycle. For higher duty cycles, see Typical Performance Characteristics curves.

THERMAL CONSIDERATIONS

At higher duty cycles, the increased ON time of the FET means the maximum output current will be determined by power dissipation within the LMR62014 FET switch. The switch power dissipation from ON-state conduction is calculated by:

$$P_{(SW)} = DC \times I_{IND}(AVE)^2 \times R_{DS}(ON) \quad (11)$$

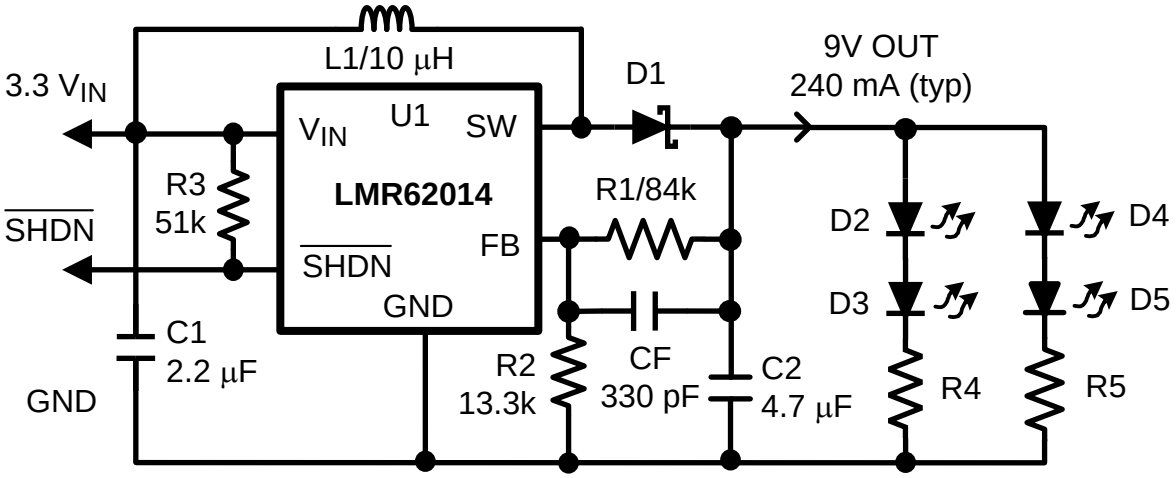
There will be some switching losses as well, so some derating needs to be applied when calculating IC power dissipation.

INDUCTOR SUPPLIERS

Recommended suppliers of inductors for this product include, but are not limited to Sumida, Coilcraft, Panasonic, TDK and Murata. When selecting an inductor, make certain that the continuous current rating is high enough to avoid saturation at peak currents. A suitable core type must be used to minimize core (switching) losses, and wire power losses must be considered when selecting the current rating.

SHUTDOWN PIN OPERATION

The device is turned off by pulling the shutdown pin low. If this function is not going to be used, the pin should be tied directly to V_{IN}. If the SHDN function will be needed, a pull-up resistor must be used to V_{IN} (approximately 50k-100kΩ recommended). The SHDN pin must not be left unterminated.



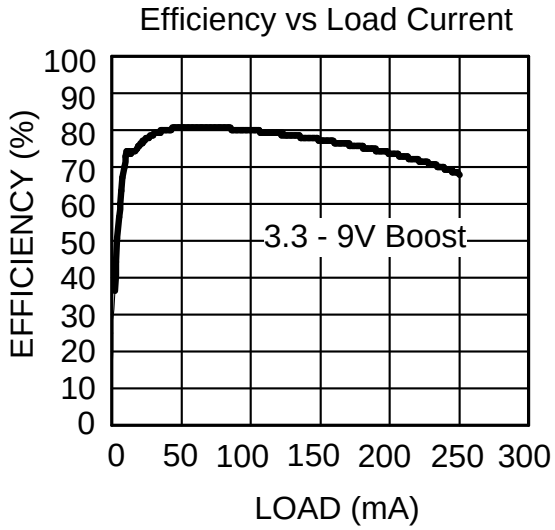


Figure 23. Flash LED Application

REVISION HISTORY

Changes from Revision A (April 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	15

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMR62014XMF/NOPB	Active	Production	SOT-23 (DBV) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SH1B
LMR62014XMF/NOPB.A	Active	Production	SOT-23 (DBV) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SH1B
LMR62014XMF/NOPB.B	Active	Production	SOT-23 (DBV) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SH1B
LMR62014XMFE/NOPB	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SH1B
LMR62014XMFE/NOPB.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SH1B
LMR62014XMFE/NOPB.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SH1B
LMR62014XMFX/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SH1B
LMR62014XMFX/NOPB.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SH1B
LMR62014XMFX/NOPB.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SH1B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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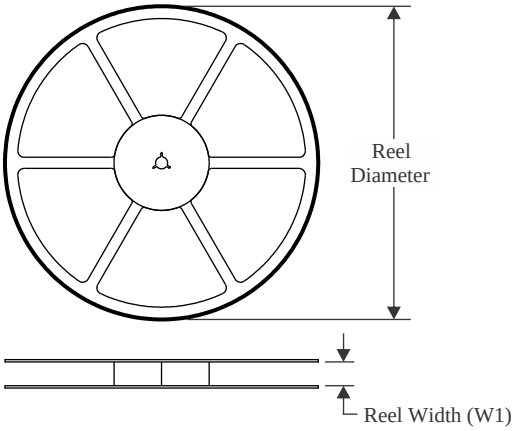
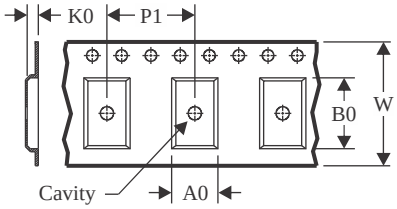
TAPE AND REEL INFORMATION

REEL DIMENSIONS

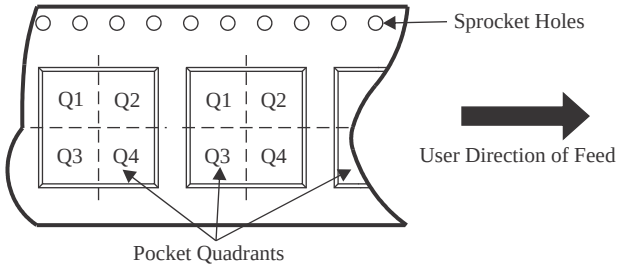


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

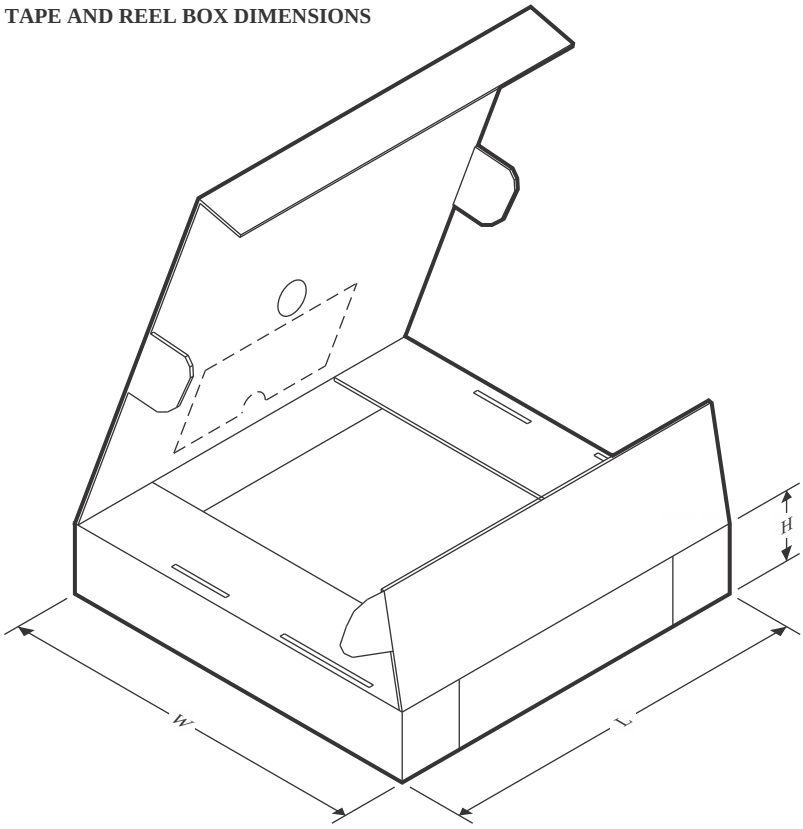
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMR62014XMF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMR62014XMFE/NOPB	SOT-23	DBV	5	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMR62014XMFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

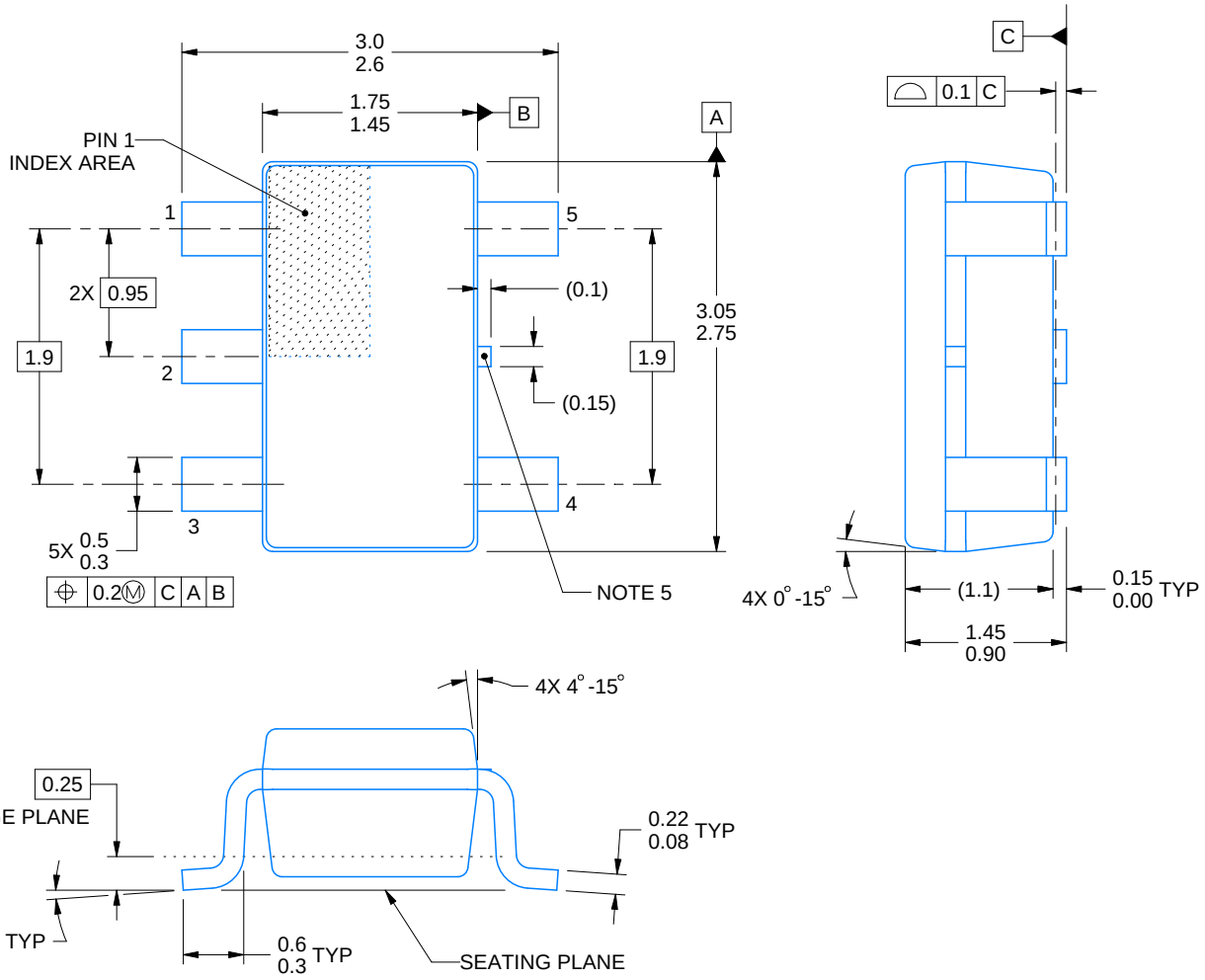
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMR62014XMF/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LMR62014XMFE/NOPB	SOT-23	DBV	5	250	208.0	191.0	35.0
LMR62014XMFX/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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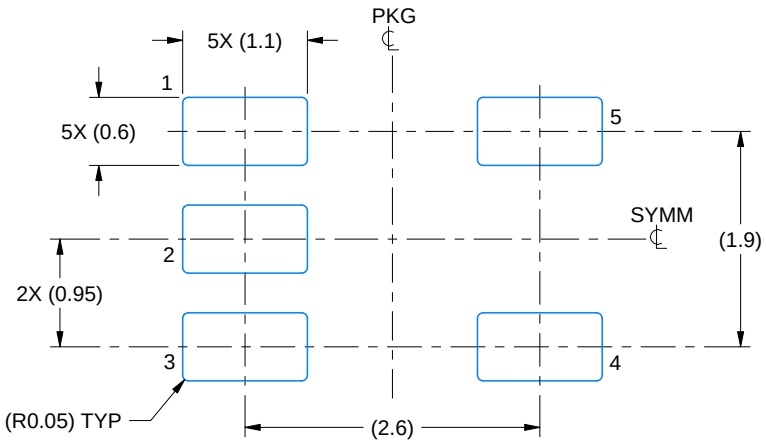
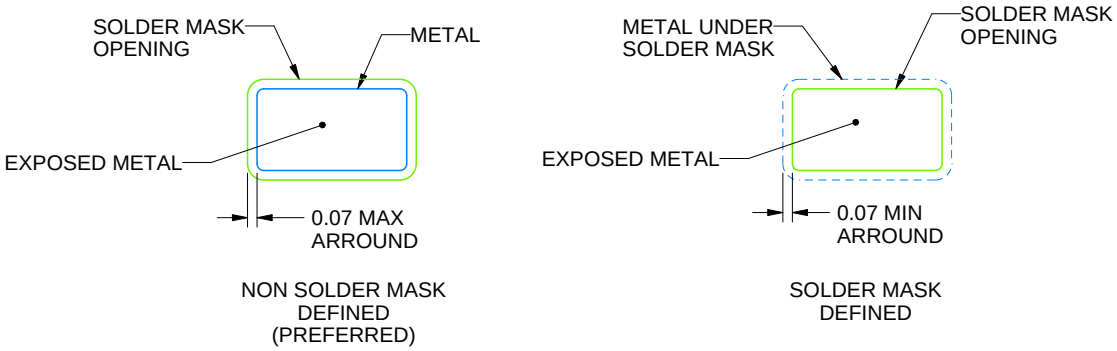
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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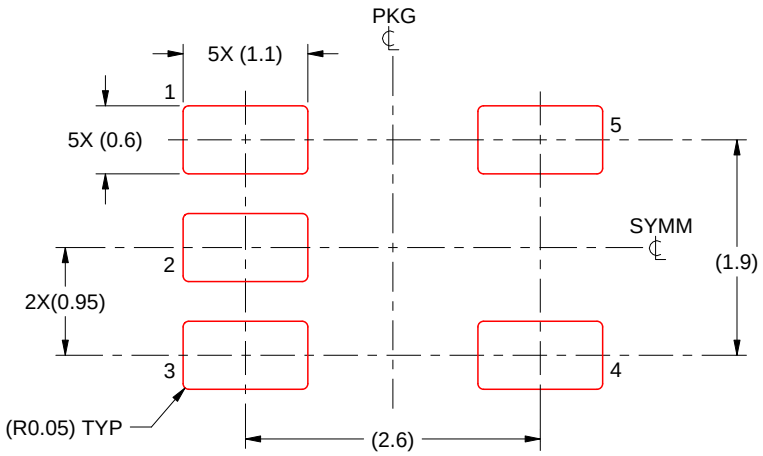
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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