LMR12010 3-V to 20-V, 1-A Step-Down DC/DC Switching Regulator in SOT-23

1 Features

- Input Voltage Range of 3 V to 20 V
- Output Voltage Range of 0.8 V to 17 V
- Output Current up to 1 A
- 1.6 MHz (LMR12010X) and 3 MHz (LMR12010Y) Switching Frequencies
- Low Shutdown I_Q, 30 nA Typical
- Internal Soft Start
- Internally Compensated
- Current-Mode PWM Operation
- Thermal Shutdown
- Tiny Overall Solution Reduces System Cost
- Thin 6-Pin SOT-23 Package (2.97 × 1.65 × 1 mm)
- Create a custom design using the LMR12010 with the WEBENCH® Power Designer

2 Applications

- Point-of-Load Conversions from 3.3-V, 5-V, and 12-V Rails
- Space Constrained Applications
- Battery Powered Equipment
- Industrial Distributed Power Applications
- Power Meters
- Portable Hand-Held Instruments

3 Description

The LMR12010 regulator is a monolithic, high frequency, PWM step-down DC/DC converter in a 6-pin thin SOT23 package. It provides all the active functions to provide local DC/DC conversion with fast transient response and accurate regulation in the smallest possible PCB area.

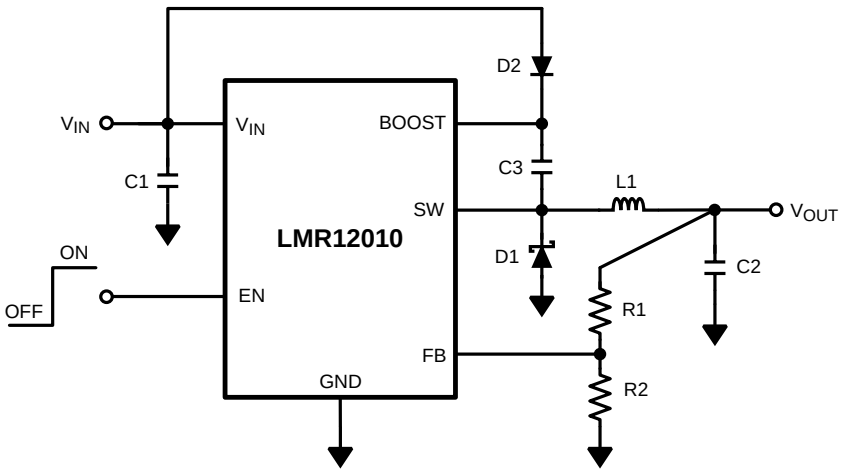
With a minimum of external components and online design support through WEBENCH, the LMR12010 is easy to use. The ability to drive 1-A loads with an internal 300-mΩ NMOS switch using state-of-the-art 0.5-µm BiCMOS technology results in the best power density available. The world class control circuitry allows for on-times as low as 13 ns, thus supporting exceptionally high frequency conversion over the entire 3-V to 20-V input operating range down to the minimum output voltage of 0.8 V. Switching frequency is internally set to 1.6 MHz (LMR12010X) or 3 MHz (LMR12010Y), allowing the use of extremely small surface mount inductors and chip capacitors. Even though the operating frequencies are very high, efficiencies up to 90% are easy to achieve. External shutdown is included, featuring an ultra-low standby current of 30 nA. The LMR12010 utilizes current-mode control and internal compensation to provide high-performance regulation over a wide range of operating conditions. Additional features include internal soft-start circuitry to reduce inrush current, pulse-by-pulse current limit, thermal shutdown, and output overvoltage protection.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMR12010	SOT-23-THIN (6)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 Recommended Operating Ratings ... 4
6.3 Electrical Characteristics ... 5
6.4 Typical Characteristics ... 6
7 Detailed Description ... 9
7.1 Overview ... 9
7.2 Functional Block Diagram ... 10
7.3 Feature Description ... 11
8 Application and Implementation ... 15
8.1 Application Information ... 15
8.2 Typical Application ... 15
9 Layout ... 21
9.1 Layout Considerations ... 21
9.2 Calculating The LMR12010 Junction Temperature 21
10 Device and Documentation Support ... 24
10.1 Device Support ... 24
10.2 Receiving Notification of Documentation Updates 24
10.3 Community Resources ... 24
10.4 Trademarks ... 24
10.5 Electrostatic Discharge Caution ... 24
10.6 Glossary ... 25
11 Mechanical, Packaging, and Orderable Information ... 25

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2011) to Revision B	Page
• Editorial changes only; add WEBENCH links	1

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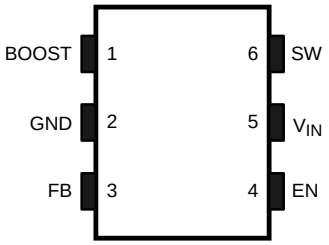
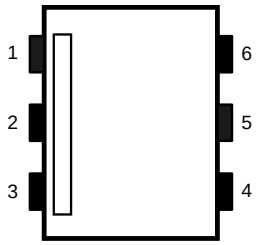
5 Pin Configuration and Functions

DDC Package
6-Pin SOT-23-THIN
Top View



Pin 1 Identification



Pin Descriptions

PIN		DESCRIPTION
NO.	NAME	
1	BOOST	Boost voltage that drives the internal NMOS control switch. A bootstrap capacitor is connected between the BOOST and SW pins.
2	GND	Signal and Power ground pin. Place the bottom resistor of the feedback network as close as possible to this pin for accurate regulation.
3	FB	Feedback pin. Connect FB to the external resistor divider to set output voltage.
4	EN	Enable control input. Logic high enables operation. Do not allow this pin to float or be greater than V_{IN} + 0.3V.
5	V_{IN}	Input supply voltage. Connect a bypass capacitor to this pin.
6	SW	Output switch. Connects to the inductor, catch diode, and bootstrap capacitor.

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6 Specifications

6.1 Absolute Maximum Ratings

See notes (1)(2).

V_{IN}	-0.5V to 24V
SW Voltage	-0.5V to 24V
Boost Voltage	-0.5V to 30V
Boost to SW Voltage	-0.5V to 6.0V
FB Voltage	-0.5V to 3.0V
EN Voltage	-0.5V to (V_{IN} + 0.3V)
Junction Temperature	150°C
ESD Susceptibility (3)	2kV
Storage Temperature Range	-65°C to 150°C
For soldering specifications: see SNOA549	

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended operating ratings indicate conditions for which the device is intended to be functional, but specific performance is not verified. For verified specifications and the test conditions, see *Electrical Characteristics*
(2) If Military/Aerospace specified devices are required,contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Human body model, 1.5kΩ in series with 100pF.

6.2 Recommended Operating Ratings (1)

V_{IN}	3V to 20V
SW Voltage	-0.5V to 20V
Boost Voltage	-0.5V to 25V
Boost to SW Voltage	1.6V to 5.5V
Junction Temperature Range	−40°C to +125°C
Thermal Resistance θ_{JA} (2)	118°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended operating ratings indicate conditions for which the device is intended to be functional, but specific performance is not verified. For verified specifications and the test conditions, see *Electrical Characteristics*
(2) Thermal shutdown will occur if the junction temperature exceeds 165°C. The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a 3” x 3” PC board with 2oz. copper on 4 layers in still air. For a 2 layer board using 1 oz. copper in still air, θ_{JA} = 204°C/W.

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6.3 Electrical Characteristics

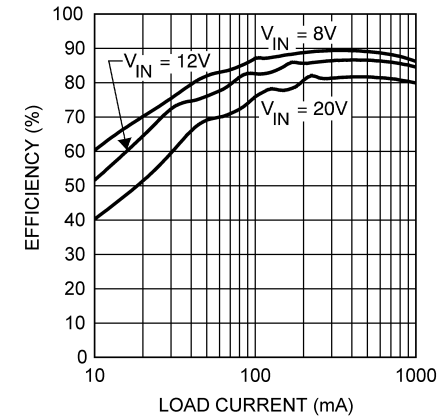
Specifications with standard typeface are for T_J = 25°C, and those in **boldface type** apply over the full **Operating Temperature Range** (T_J = -40°C to 125°C). V_{IN} = 5 V, V_{BOOST} - V_{SW} = 5V unless otherwise specified. Datasheet min/max specification limits are specified by design, test, or statistical analysis.

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
V_{FB}	Feedback Voltage		**0.784**	0.800	**0.816**	V
$\Delta V_{FB}/\Delta V_{IN}$	Feedback Voltage Line Regulation	V_{IN} = 3V to 20V		0.01		% / V
I_{FB}	Feedback Input Bias Current	Sink/Source		10	**250**	nA
UVLO	Undervoltage Lockout	V_{IN} Rising		2.74	**2.90**	V
	Undervoltage Lockout	V_{IN} Falling	**2.0**	2.3		
	UVLO Hysteresis		**0.30**	0.44	**0.62**	
F_{SW}	Switching Frequency	LMR12010X	**1.2**	1.6	**1.9**	MHz
		LMR12010Y	**2.2**	3.0	**3.6**	
D_{MAX}	Maximum Duty Cycle	LMR12010X	**85%**	92%		
		LMR12010Y	**78%**	85%		
D_{MIN}	Minimum Duty Cycle	LMR12010X		2%		
		LMR12010Y		8%		
$R_{DS(ON)}$	Switch ON Resistance	V_{BOOST} - V_{SW} = 3V		300	**600**	mΩ
I_{CL}	Switch Current Limit	V_{BOOST} - V_{SW} = 3V	**1.2**	1.7	**2.5**	A
I_Q	Quiescent Current	Switching		1.5	**2.5**	mA
	Quiescent Current (shutdown)	V_{EN} = 0V		30		nA
I_{BOOST}	Boost Pin Current	LMR12010X (50% Duty Cycle)		2.5	**3.5**	mA
		LMR12010Y (50% Duty Cycle)		4.25	**6.0**	
V_{EN_TH}	Shutdown Threshold Voltage	V_{EN} Falling			**0.4**	V
	Enable Threshold Voltage	V_{EN} Rising	**1.8**			
I_{EN}	Enable Pin Current	Sink/Source		10		nA
I_{SW}	Switch Leakage			40		nA

(1) Specified to Average Outgoing Quality Level (AOQL).
(2) Typicals represent the most likely parametric norm.

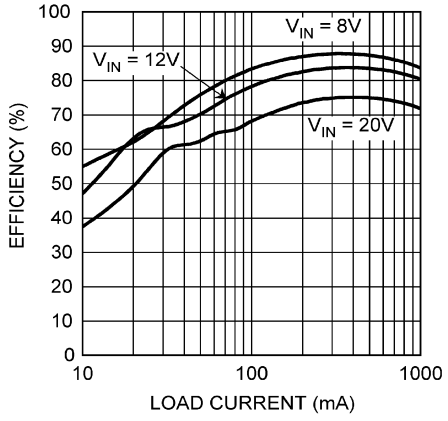
6.4 Typical Characteristics

All curves taken at V_{IN} = 5V, V_{BOOST} - V_{SW} = 5V, L1 = 4.7 µH ("X"), L1 = 2.2 µH ("Y") and T_A = 25°C, unless specified otherwise.



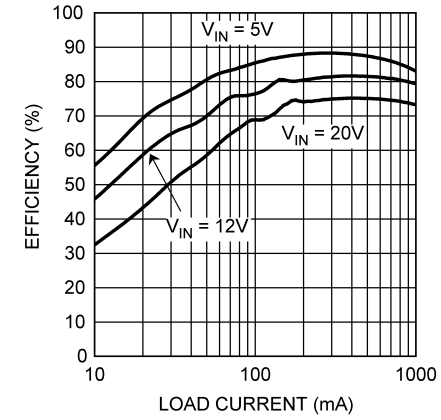
V_{OUT} = 5 V

Figure 1. Efficiency vs Load Current - "X"



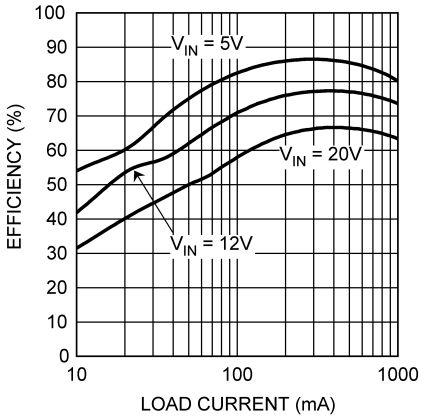
V_{OUT} = 5 V

Figure 2. Efficiency vs Load Current - "Y"



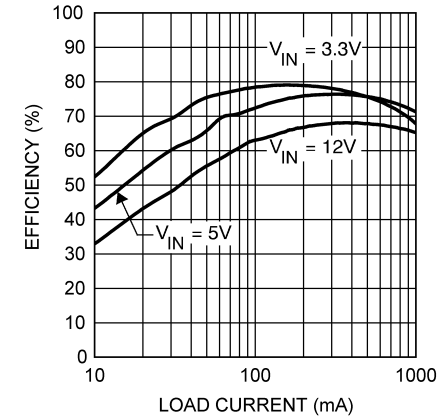
V_{OUT} = 3.3 V

Figure 3. Efficiency vs Load Current - "X"



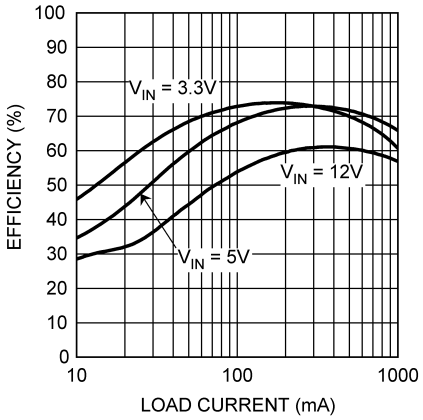
V_{OUT} = 3.3 V

Figure 4. Efficiency vs Load Current - "Y"



V_{OUT} = 1.5 V

Figure 5. Efficiency vs Load Current - "X"



V_{OUT} = 1.5 V

Figure 6. Efficiency vs Load Current - "Y"

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Typical Characteristics (continued)

All curves taken at V_{IN} = 5V, V_{BOOST} - V_{SW} = 5V, L1 = 4.7 µH ("X"), L1 = 2.2 µH ("Y") and T_A = 25°C, unless specified otherwise.

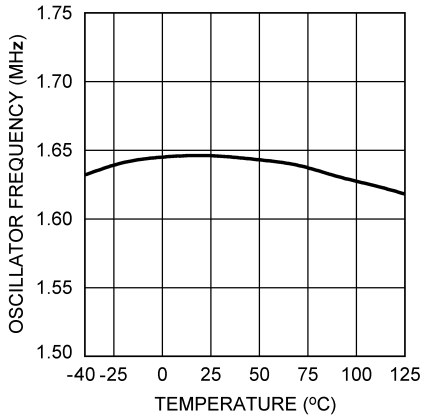


Figure 7. Oscillator Frequency vs Temperature - "X"

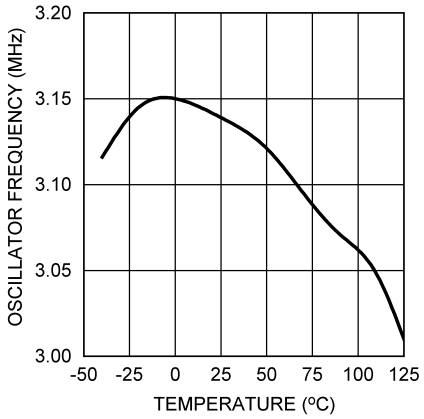
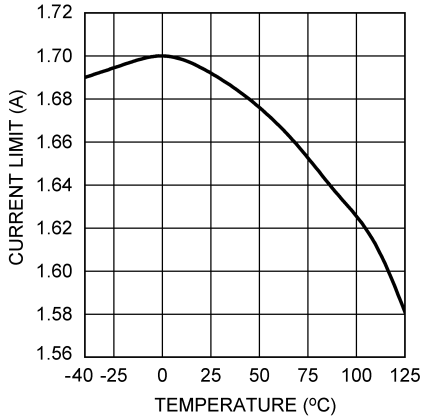
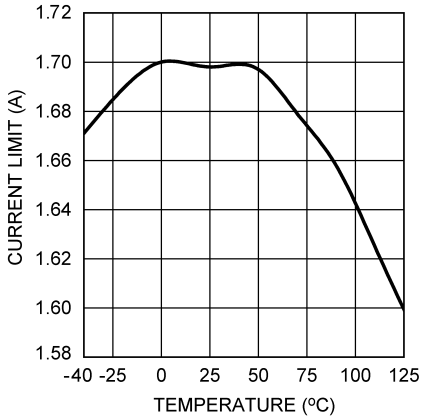


Figure 8. Oscillator Frequency vs Temperature - "Y"



V_{IN} = 5 V

Figure 9. Current Limit vs Temperature



V_{IN} = 20 V

Figure 10. Current Limit vs Temperature

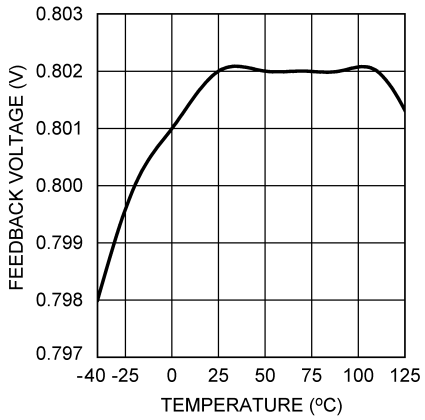


Figure 11. V_{FB} vs Temperature

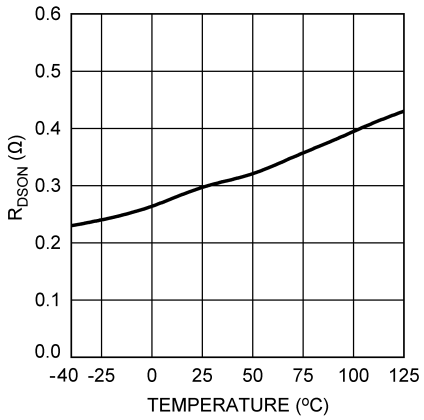


Figure 12. R_{DSON} vs Temperature

Typical Characteristics (continued)

All curves taken at V_{IN} = 5V, V_{BOOST} - V_{SW} = 5V, L1 = 4.7 µH ("X"), L1 = 2.2 µH ("Y") and T_A = 25°C, unless specified otherwise.

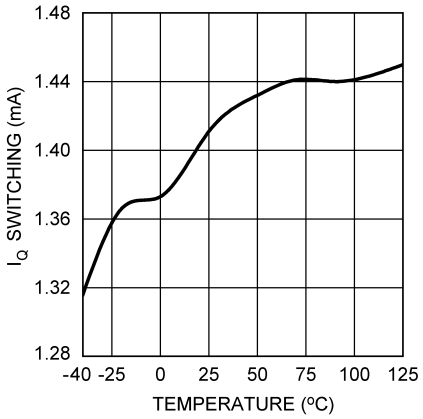


Figure 13. I_Q Switching vs Temperature

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7 Detailed Description

7.1 Overview

The LMR12010 is a constant frequency PWM buck regulator IC that delivers a 1-A load current. The regulator has a preset switching frequency of either 3 MHz (LMR12010Y) or 1.6 MHz (LMR12010X). These high frequencies allow the LMR12010 to operate with small surface mount capacitors and inductors, resulting in DC/DC converters that require a minimum amount of board space. The LMR12010 is internally compensated, so it is simple to use, and requires few external components. The LMR12010 uses current-mode control to regulate the output voltage.

The following operating description of the LMR12010 refers to the functional block diagram (*Functional Block Diagram*) and to the waveforms in Figure 14. The LMR12010 supplies a regulated output voltage by switching the internal NMOS control switch at constant frequency and variable duty cycle. A switching cycle begins at the falling edge of the reset pulse generated by the internal oscillator. When this pulse goes low, the output control logic turns on the internal NMOS control switch. During this on-time, the SW pin voltage (V_{SW}) swings up to approximately V_{IN}, and the inductor current (I_L) increases with a linear slope. I_L is measured by the current-sense amplifier, which generates an output proportional to the switch current. The sense signal is summed with the regulator's corrective ramp and compared to the error amplifier's output, which is proportional to the difference between the feedback voltage and V_{REF}. When the PWM comparator output goes high, the output switch turns off until the next switching cycle begins. During the switch off-time, inductor current discharges through Schottky diode D1, which forces the SW pin to swing below ground by the forward voltage (V_D) of the catch diode. The regulator loop adjusts the duty cycle (D) to maintain a constant output voltage.

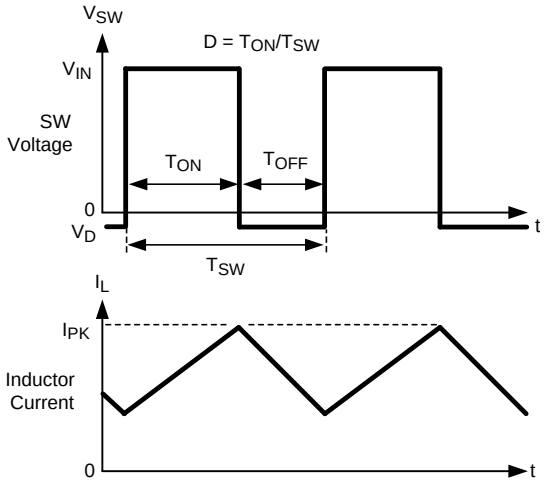
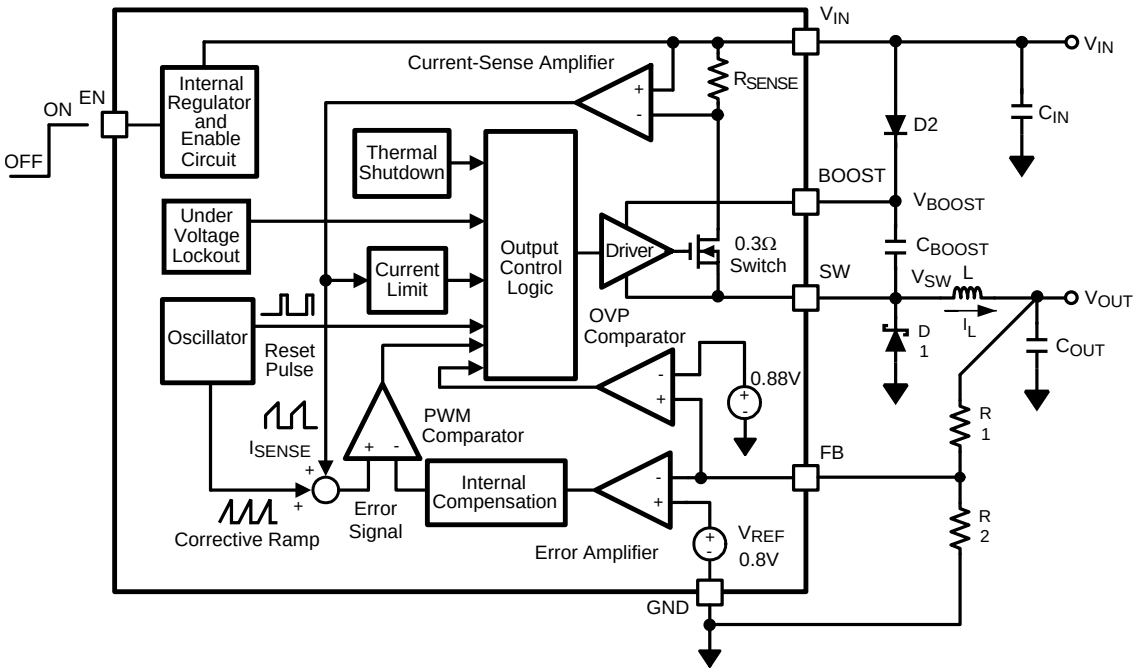


Figure 14. LMR12010 Waveforms Of SW Pin Voltage and Inductor Current

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Boost Function

Capacitor C_{BOOST} and diode D2 in Figure 15 are used to generate a voltage V_{BOOST}. $V_{BOOST} – V_{SW}$ is the gate-drive voltage to the internal NMOS control switch. To properly drive the internal NMOS switch during its on-time, V_{BOOST} needs to be at least 1.6 V greater than V_{SW}. Although the LMR12010 operates with this minimum voltage, it may not have sufficient gate drive to supply large values of output current. Therefore, it is recommended that V_{BOOST} be greater than 2.5 V above V_{SW} for best efficiency. $V_{BOOST} – V_{SW}$ should not exceed the maximum operating limit of 5.5 V.

$5.5\ V > V_{BOOST} – V_{SW} > 2.5\ V$ for best performance.

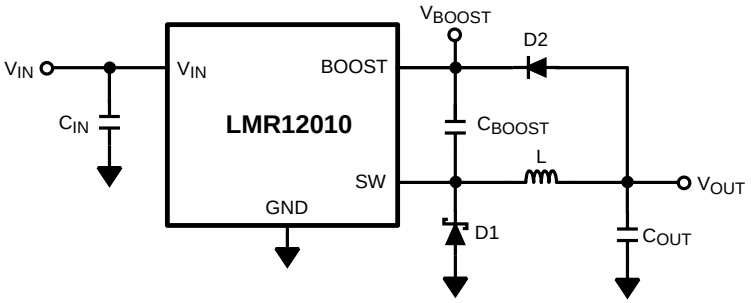

Figure 15. V_{OUT} Charges C_{BOOST}

When the LMR12010 starts up, internal circuitry from the BOOST pin supplies a maximum of 20 mA to C_{BOOST}. This current charges C_{BOOST} to a voltage sufficient to turn the switch on. The BOOST pin continues to source current to C_{BOOST} until the voltage at the feedback pin is greater than 0.76 V.

There are various methods to derive V_{BOOST}:

1. From the input voltage (V_{IN})
2. From the output voltage (V_{OUT})
3. From an external distributed voltage rail (V_{EXT})
4. From a shunt or series zener diode

In the *Functional Block Diagram*, capacitor C_{BOOST} and diode D2 supply the gate-drive current for the NMOS switch. Capacitor C_{BOOST} is charged via diode D2 by V_{IN}. During a normal switching cycle, when the internal NMOS control switch is off (T_{OFF}) (refer to Figure 14), V_{BOOST} equals V_{IN} minus the forward voltage of D2 (V_{FD2}), during which the current in the inductor (L) forward biases the Schottky diode D1 (V_{FD1}). Therefore the voltage stored across C_{BOOST} is

$$V_{BOOST} – V_{SW} = V_{IN} – V_{FD2} + V_{FD1} \quad (1)$$

When the NMOS switch turns on (T_{ON}), the switch pin rises to

$$V_{SW} = V_{IN} – (R_{DSON} \times I_L), \quad (2)$$

forcing V_{BOOST} to rise thus reverse biasing D2. The voltage at V_{BOOST} is then

$$V_{BOOST} = 2\ V_{IN} – (R_{DSON} \times I_L) – V_{FD2} + V_{FD1} \quad (3)$$

which is approximately

$$2V_{IN} – 0.4\ V \quad (4)$$

for many applications. Thus the gate-drive voltage of the NMOS switch is approximately

$$V_{IN} – 0.2\ V \quad (5)$$

An alternate method for charging C_{BOOST} is to connect D2 to the output as shown in Figure 15. The output voltage must be between 2.5 V and 5.5 V, so that proper gate voltage will be applied to the internal switch. In this circuit, C_{BOOST} provides a gate-drive voltage that is slightly less than V_{OUT}.

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Feature Description (continued)

In applications where both V_{IN} and V_{OUT} are greater than 5.5 V, or less than 3 V, C_{BOOST} cannot be charged directly from these voltages. If V_{IN} and V_{OUT} are greater than 5.5 V, C_{BOOST} can be charged from V_{IN} or V_{OUT} minus a zener voltage by placing a zener diode D3 in series with D2, as shown in Figure 16. When using a series zener diode from the input, ensure that the regulation of the input supply doesn't create a voltage that falls outside the recommended V_{BOOST} voltage.

$(V_{INMAX} – V_{D3}) < 5.5$ V

$(V_{INMIN} – V_{D3}) > 1.6$ V

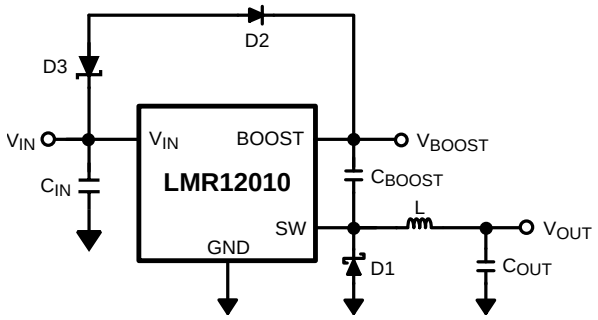

Figure 16. Zener Reduces Boost Voltage From V_{IN}

An alternative method is to place the zener diode D3 in a shunt configuration as shown in Figure 17. A small 350-mW to 500-mW, 5.1-V zener in a SOT-23 or SOD package can be used for this purpose. Place a small ceramic capacitor such as a 6.3-V, 0.1-µF capacitor (C4) in parallel with the zener diode. When the internal NMOS switch turns on, a pulse of current is drawn to charge the internal NMOS gate capacitance. The 0.1 µF parallel shunt capacitor ensures that the V_{BOOST} voltage is maintained during this time.

Resistor R3 should be chosen to provide enough RMS current to the zener diode (D3) and to the BOOST pin. A recommended choice for the zener current (I_{ZENER}) is 1 mA. The current I_{BOOST} into the BOOST pin supplies the gate current of the NMOS control switch and varies typically according to the following formula for the X version:

$$I_{BOOST} = 0.56 \times (D + 0.54) \times (V_{ZENER} – V_{D2}) \text{ mA} \quad (6)$$

I_{BOOST} can be calculated for the Y version using the following:

$$I_{BOOST} = (D + 0.5) \times (V_{ZENER} - V_{D2}) \text{ mA}$$

where

- D is the duty cycle
- V_{ZENER} and V_{D2} are in volts
- I_{BOOST} is in milliamps (7)

V_{ZENER} is the voltage applied to the anode of the boost diode (D2), and V_{D2} is the average forward voltage across D2. Note that this formula for I_{BOOST} gives typical current. For the worst case I_{BOOST}, increase the current by 40%. In that case, the worst case boost current will be

$$I_{BOOST\text{-}MAX} = 1.4 \times I_{BOOST} \quad (8)$$

R3 will then be given by

$$R3 = (V_{IN} – V_{ZENER}) / (1.4 \times I_{BOOST} + I_{ZENER}) \quad (9)$$

For example, using the X-version let V_{IN} = 10 V, V_{ZENER} = 5 V, V_{D2} = 0.7 V, I_{ZENER} = 1 mA, and duty cycle D = 50%. Then

$$I_{BOOST} = 0.56 \times (0.5 + 0.54) \text{ x } (5 – 0.7) \text{ mA} = 2.5 \text{ mA} \quad (10)$$

$$R3 = (10 \text{ V} – 5 \text{ V}) / (1.4 \times 2.5 \text{ mA} + 1 \text{ mA}) = 1.11 \text{ k}\Omega \quad (11)$$

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Feature Description (continued)

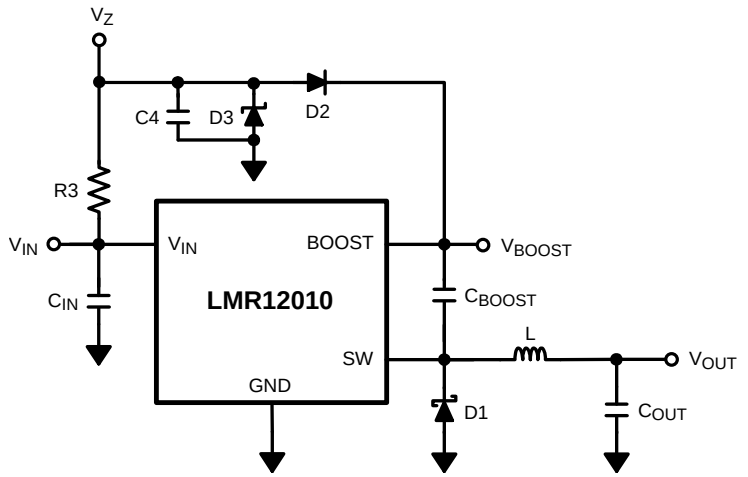

Figure 17. Boost Voltage Supplied From the Shunt Zener on V_{IN}

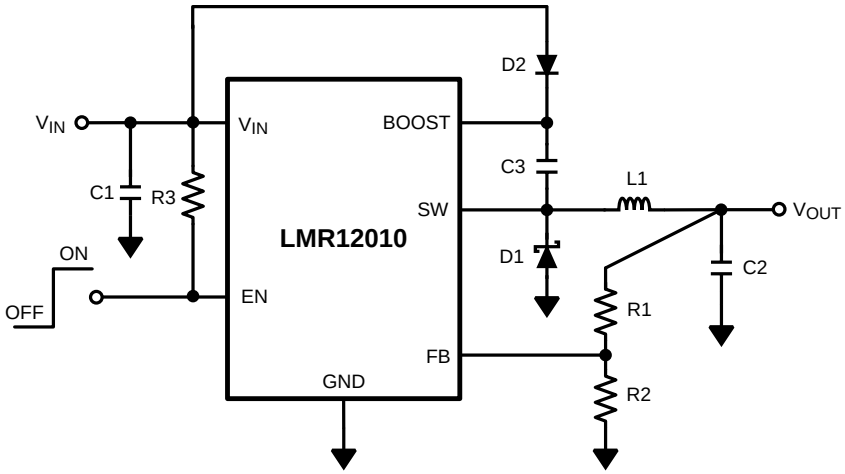

Figure 18. V_{BOOST} Derived From V_{IN}

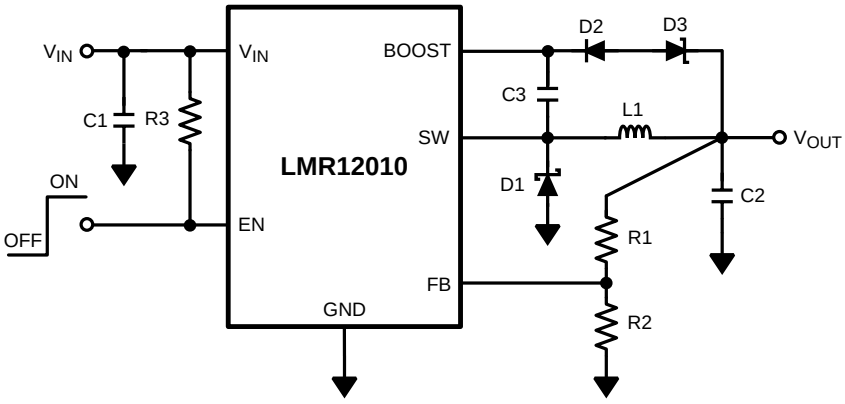

Figure 19. V_{BOOST} Derived From Series Zener Diode (V_{OUT})

Feature Description (continued)

7.3.2 Enable Pin / Shutdown Mode

The LMR12010 has a shutdown mode that is controlled by the enable pin (EN). When a logic low voltage is applied to EN, the part is in shutdown mode and its quiescent current drops to typically 30 nA. Switch leakage adds another 40 nA from the input supply. The voltage at this pin must never exceed V_{IN} + 0.3 V.

7.3.3 Soft Start

This function forces V_{OUT} to increase at a controlled rate during start up. During soft start, the error amplifier's reference voltage ramps from 0V to its nominal value of 0.8 V in approximately 200 µs. This forces the regulator output to ramp up in a more linear and controlled fashion, which helps reduce inrush current. Under some circumstances at start-up, an output voltage overshoot may still be observed. This may be due to a large output load applied during start up. Large amounts of output external capacitance can also increase output voltage overshoot. A simple solution is to add a feed forward capacitor with a value between 470 pf and 1000 pf across the top feedback resistor (R1).

7.3.4 Output Overvoltage Protection

The overvoltage comparator compares the FB pin voltage to a voltage that is 10% higher than the internal reference Vref. Once the FB pin voltage goes 10% above the internal reference, the internal NMOS control switch is turned off, which allows the output voltage to decrease toward regulation.

7.3.5 Undervoltage Lockout

Undervoltage lockout (UVLO) prevents the LMR12010 from operating until the input voltage exceeds 2.74 V (typical).

The UVLO threshold has approximately 440 mV of hysteresis, so the part will operate until V_{IN} drops below 2.3 V (typical). Hysteresis prevents the part from turning off during power up if V_{IN} is non-monotonic.

7.3.6 Current Limit

The LMR12010 uses cycle-by-cycle current limiting to protect the output switch. During each switching cycle, a current limit comparator detects if the output switch current exceeds 1.7 A (typical), and turns off the switch until the next switching cycle begins.

7.3.7 Thermal Shutdown

Thermal shutdown limits total power dissipation by turning off the output switch when the IC junction temperature exceeds 165°C. After thermal shutdown occurs, the output switch doesn't turn on until the junction temperature drops to approximately 150°C.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMR12010 regulator is a monolithic, high frequency, PWM step-down DC/DC converter in a 6-pin thin SOT23 package. Switching frequency is internally set to 1.6 MHz (LMR12010X) or 3 MHz (LMR12010Y), allowing the use of extremely small surface mount inductors and chip capacitors.

8.2 Typical Application

Typical Application

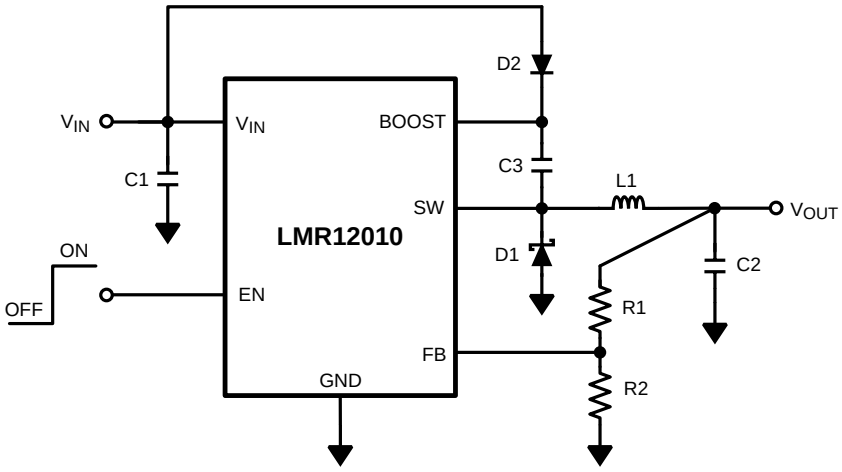

Figure 20. Typical Application Schematic

8.2.1 Detailed Design Procedure

8.2.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMR12010 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

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Typical Application (continued)

8.2.1.2 Inductor Selection

The duty cycle (D) can be approximated quickly using the ratio of output voltage (V_O) to input voltage (V_{IN}):

$$D = \frac{V_O}{V_{IN}} \quad (12)$$

The catch diode (D1) forward voltage drop and the voltage drop across the internal NMOS must be included to calculate a more accurate duty cycle. Calculate D by using the following formula:

$$D = \frac{V_O + V_D}{V_{IN} + V_D - V_{SW}} \quad (13)$$

V_{SW} can be approximated by:

$$V_{SW} = I_O \times R_{DS(ON)} \quad (14)$$

The diode forward drop (V_D) can range from 0.3V to 0.7V depending on the quality of the diode. The lower V_D is, the higher the operating efficiency of the converter.

The inductor value determines the output ripple current. Lower inductor values decrease the size of the inductor, but increase the output ripple current. An increase in the inductor value will decrease the output ripple current. The ratio of ripple current (Δi_L) to output current (I_O) is optimized when it is set between 0.3 and 0.4 at 1 A. The ratio r is defined as:

$$r = \frac{\Delta i_L}{I_O} \quad (15)$$

One must also ensure that the minimum current limit (1.2 A) is not exceeded, so the peak current in the inductor must be calculated. The peak current (I_{LPK}) in the inductor is calculated by:

$$I_{LPK} = I_O + \Delta I_L/2 \quad (16)$$

If r = 0.5 at an output of 1 A, the peak current in the inductor will be 1.25 A. The minimum verified current limit over all operating conditions is 1.2 A. One can either reduce r to 0.4 resulting in a 1.2-A peak current, or make the engineering judgement that 50 mA over will be safe enough with a 1.7-A typical current limit and 6 sigma limits. When the designed maximum output current is reduced, the ratio r can be increased. At a current of 0.1 A, r can be made as high as 0.9. The ripple ratio can be increased at lighter loads because the net ripple is actually quite low, and if r remains constant the inductor value can be made quite large. An equation empirically developed for the maximum ripple ratio at any current below 2 A is:

$$r = 0.387 \times I_{OUT}^{-0.3667} \quad (17)$$

Note that this is just a guideline.

The LMR12010 operates at frequencies allowing the use of ceramic output capacitors without compromising transient response. Ceramic capacitors allow higher inductor ripple without significantly increasing output ripple. See the Output Capacitor for more details on calculating output voltage ripple.

Now that the ripple current or ripple ratio is determined, the inductance is calculated by:

$$L = \frac{V_O + V_D}{I_O \times r \times f_S} \times (1-D)$$

where

- f_s is the switching frequency
- I_O is the output current

(18)

When selecting an inductor, make sure that it is capable of supporting the peak output current without saturating. Inductor saturation will result in a sudden reduction in inductance and prevent the regulator from operating correctly. Because of the speed of the internal current limit, the peak current of the inductor need only be specified for the required maximum output current. For example, if the designed maximum output current is 0.5 A and the peak current is 0.7 A, then the inductor should be specified with a saturation current limit of >0.7 A.

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Typical Application (continued)

There is no need to specify the saturation or peak current of the inductor at the 1.7-A typical switch current limit. The difference in inductor size is a factor of 5. Because of the operating frequency of the LMR12010, ferrite based inductors are preferred to minimize core losses. This presents little restriction since the variety of ferrite based inductors is huge. Lastly, inductors with lower series resistance (DCR) provide better operating efficiency. For recommended inductors see example circuits.

8.2.1.3 Input Capacitor

An input capacitor is necessary to ensure that V_{IN} does not drop excessively during switching transients. The primary specifications of the input capacitor are capacitance, voltage, RMS current rating, and equivalent series inductance (ESL). The recommended input capacitance is 10 µF, although 4.7 µF works well for input voltages below 6 V. The input voltage rating is specifically stated by the capacitor manufacturer. Make sure to check any recommended deratings and also verify if there is any significant change in capacitance at the operating input voltage and the operating temperature. The input capacitor maximum RMS input current rating (I_{RMS-IN}) must be greater than:

$$I_{RMS-IN} = I_O \times \sqrt{D \times \left(1-D+\frac{r^2}{12}\right)} \tag{19}$$

It can be shown from Equation 19 that maximum RMS capacitor current occurs when D = 0.5. Always calculate the RMS at the point where the duty cycle, D, is closest to 0.5. The ESL of an input capacitor is usually determined by the effective cross sectional area of the current path. A large leaded capacitor will have high ESL and a 0805 ceramic chip capacitor will have very low ESL. At the operating frequencies of the LMR12010, certain capacitors may have an ESL so large that the resulting impedance ($2\pi fL$) will be higher than that required to provide stable operation. As a result, surface mount capacitors are strongly recommended. Sanyo POSCAP, Tantalum or Niobium, Panasonic SP or Cornell Dubilier ESR, and multilayer ceramic capacitors (MLCC) are all good choices for both input and output capacitors and have very low ESL. For MLCCs TI recommends using X7R or X5R dielectrics. Consult capacitor manufacturer datasheet to see how rated capacitance varies over operating conditions.

8.2.1.4 Output Capacitor

The output capacitor is selected based upon the desired output ripple and transient response. The initial current of a load transient is provided mainly by the output capacitor. The output ripple of the converter is:

$$\Delta V_O = \Delta i_L \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C_O}\right) \tag{20}$$

When using MLCCs, the ESR is typically so low that the capacitive ripple may dominate. When this occurs, the output ripple will be approximately sinusoidal and 90° phase shifted from the switching action. Given the availability and quality of MLCCs and the expected output voltage of designs using the LMR12010, there is really no need to review any other capacitor technologies. Another benefit of ceramic capacitors is their ability to bypass high frequency noise. A certain amount of switching edge noise will couple through parasitic capacitances in the inductor to the output. A ceramic capacitor will bypass this noise while a tantalum will not. Since the output capacitor is one of the two external components that control the stability of the regulator control loop, most applications will require a minimum at 10 µF of output capacitance. Capacitance can be increased significantly with little detriment to the regulator stability. Like the input capacitor, recommended multilayer ceramic capacitors are X7R or X5R. Again, verify actual capacitance at the desired operating voltage and temperature.

Check the RMS current rating of the capacitor. The RMS current rating of the capacitor chosen must also meet the following condition:

$$I_{RMS-OUT} = I_O \times \frac{r}{\sqrt{12}} \tag{21}$$

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Typical Application (continued)

8.2.1.5 Catch Diode

The catch diode (D1) conducts during the switch off-time. A Schottky diode is recommended for its fast switching times and low forward voltage drop. The catch diode should be chosen so that its current rating is greater than:

$$I_{D1} = I_O \times (1\text{-}D) \quad (22)$$

The reverse breakdown rating of the diode must be at least the maximum input voltage plus appropriate margin. To improve efficiency choose a Schottky diode with a low forward voltage drop.

8.2.1.6 Boost Diode

A standard diode such as the 1N4148 type is recommended. For V_{BOOST} circuits derived from voltages less than 3.3 V, a small-signal Schottky diode is recommended for greater efficiency. A good choice is the BAT54 small signal diode.

8.2.1.7 Boost Capacitor

A ceramic 0.01µF capacitor with a voltage rating of at least 6.3 V is sufficient. The X7R and X5R MLCCs provide the best performance.

8.2.1.8 Output Voltage

The output voltage is set using the following equation where R2 is connected between the FB pin and GND, and R1 is connected between V_O and the FB pin. A good value for R2 is 10 kΩ.

$$R1 = \left(\frac{V_O}{V_{REF}} - 1 \right) \times R2 \quad (23)$$

8.2.1.9 Calculating Efficiency, and Junction Temperature

The complete LMR12010 DC/DC converter efficiency can be calculated in the following manner.

$$\eta = \frac{P_{OUT}}{P_{IN}} \quad (24)$$

Or

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}} \quad (25)$$

Calculations for determining the most significant power losses are shown below. Other losses totaling less than 2% are not discussed.

Power loss (P_{LOSS}) is the sum of two basic types of losses in the converter, switching and conduction. Conduction losses usually dominate at higher output loads, where as switching losses remain relatively fixed and dominate at lower output loads. The first step in determining the losses is to calculate the duty cycle (D).

$$D = \frac{V_{OUT} + V_D}{V_{IN} + V_D - V_{SW}} \quad (26)$$

V_{SW} is the voltage drop across the internal NFET when it is on, and is equal to:

$$V_{SW} = I_{OUT} \times R_{DSON} \quad (27)$$

V_D is the forward voltage drop across the Schottky diode. It can be obtained from the Electrical Characteristics. If the voltage drop across the inductor (V_{DCR}) is accounted for, the equation becomes:

$$D = \frac{V_O + V_D + V_{DCR}}{V_{IN} + V_D - V_{SW}} \quad (28)$$

This usually gives only a minor duty cycle change, and has been omitted in the examples for simplicity.

The conduction losses in the free-wheeling Schottky diode are calculated as follows:

$$P_{DIODE} = V_D \times I_{OUT}(1\text{-}D) \quad (29)$$

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Typical Application (continued)

Often this is the single most significant power loss in the circuit. Care should be taken to choose a Schottky diode that has a low forward voltage drop.

Another significant external power loss is the conduction loss in the output inductor. The equation can be simplified to:

$$P_{IND} = I_{OUT}^2 \times R_{DCR} \quad (30)$$

The LMR12010 conduction loss is mainly associated with the internal NFET:

$$P_{COND} = I_{OUT}^2 \times R_{DSON} \times D \quad (31)$$

Switching losses are also associated with the internal NFET. They occur during the switch on and off transition periods, where voltages and currents overlap resulting in power loss. The simplest means to determine this loss is to empirically measuring the rise and fall times (10% to 90%) of the switch at the switch node:

$$P_{SWF} = 1/2(V_{IN} \times I_{OUT} \times freq \times T_{FALL}) \quad (32)$$

$$P_{SWR} = 1/2(V_{IN} \times I_{OUT} \times freq \times T_{RISE}) \quad (33)$$

$$P_{SW} = P_{SWF} + P_{SWR} \quad (34)$$

Table 1. Typical Rise And Fall Times vs Input Voltage

V_{IN}	T_{RISE}	T_{FALL}
5 V	8 ns	4 ns
10 V	9 ns	6 ns
15 V	10 ns	7 ns

Another loss is the power required for operation of the internal circuitry:

$$P_Q = I_Q \times V_{IN} \quad (35)$$

I_Q is the quiescent operating current, and is typically around 1.5mA. The other operating power that needs to be calculated is that required to drive the internal NFET:

$$P_{BOOST} = I_{BOOST} \times V_{BOOST} \quad (36)$$

V_{BOOST} is normally between 3 VDC and 5 VDC. The I_{BOOST} rms current is approximately 4.25 mA. Total power losses are:

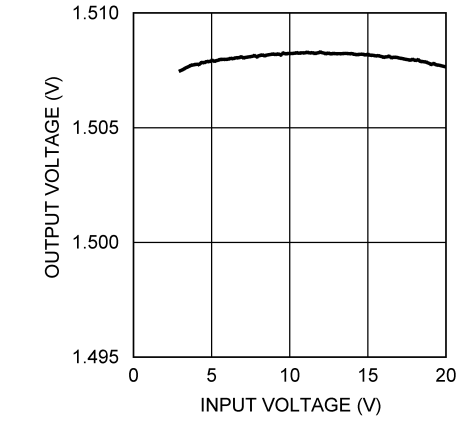
$$\Sigma P_{COND} + P_{SW} + P_{DIODE} + P_{IND} + P_Q + P_{BOOST} = P_{LOSS} \quad (37)$$

Table 2. Design Example 1

V_{IN}	5 V	P_{OUT}	2.5 W
V_{OUT}	2.5 V	P_{DIODE}	151 mW
I_{OUT}	1 A	P_{IND}	75 mW
V_D	0.35 V	P_{SWF}	53 mW
Freq	3 MHz	P_{SWR}	53 mW
I_Q	1.5 mA	P_{COND}	187 mW
T_{RISE}	8 ns	P_Q	7.5 mW
T_{FALL}	8 ns	P_{BOOST}	21 mW
R_{DSON}	330 mΩ	P_{LOSS}	**548 mW**
IND_{DCR}	75 mΩ		
D	**0.568**		

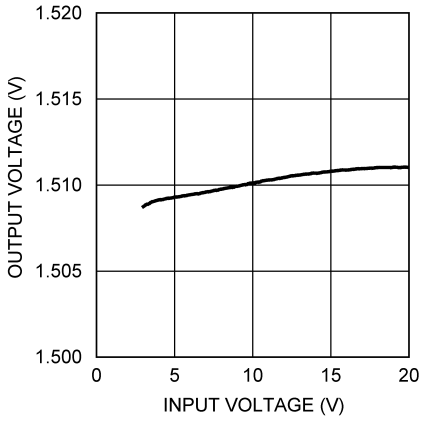
η = 82%

8.2.2 Application Curves



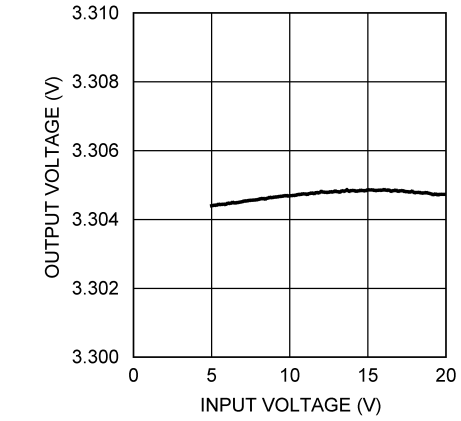
V_{OUT} = 1.5 V I_{OUT} = 500 mA

Figure 21. Line Regulation - "X"



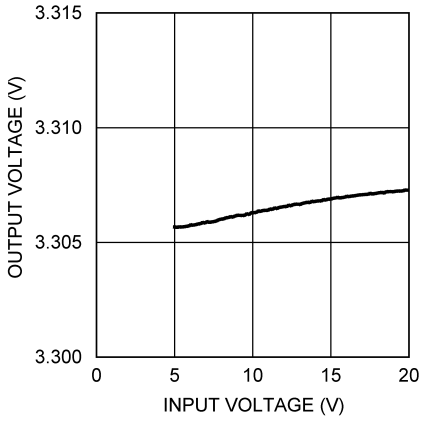
V_{OUT} = 1.5 V I_{OUT} = 500 mA

Figure 22. Line Regulation - "Y"



V_{OUT} = 3.3 V I_{OUT} = 500 mA

Figure 23. Line Regulation - "X"



V_{OUT} = 3.3 V I_{OUT} = 500 mA

Figure 24. Line Regulation - "Y"

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9 Layout

9.1 Layout Considerations

When planning layout there are a few things to consider when trying to achieve a clean, regulated output. The most important consideration when completing the layout is the close coupling of the GND connections of the C_{IN} capacitor and the catch diode D1. These ground ends should be close to one another and be connected to the GND plane with at least two through-holes. Place these components as close to the IC as possible. Next in importance is the location of the GND connection of the C_{OUT} capacitor, which should be near the GND connections of C_{IN} and D1.

There should be a continuous ground plane on the bottom layer of a two-layer board except under the switching node island.

The FB pin is a high impedance node and care should be taken to make the FB trace short to avoid noise pickup and inaccurate regulation. The feedback resistors should be placed as close as possible to the IC, with the GND of R2 placed as close as possible to the GND of the IC. The V_{OUT} trace to R1 should be routed away from the inductor and any other traces that are switching.

High AC currents flow through the V_{IN}, SW and V_{OUT} traces, so they must be as short and wide as possible. However, making the traces wide increases radiated noise, so the designer must make this trade-off. Radiated noise can be decreased by choosing a shielded inductor.

The remaining components should also be placed as close as possible to the IC. Refer to the LMR12010 demo board as an example of a good layout.

9.2 Calculating The LMR12010 Junction Temperature

Thermal Definitions:

- T_J = Chip junction temperature
- T_A = Ambient temperature
- $R_{\theta JC}$ = Thermal resistance from chip junction to device case
- $R_{\theta JA}$ = Thermal resistance from chip junction to ambient air

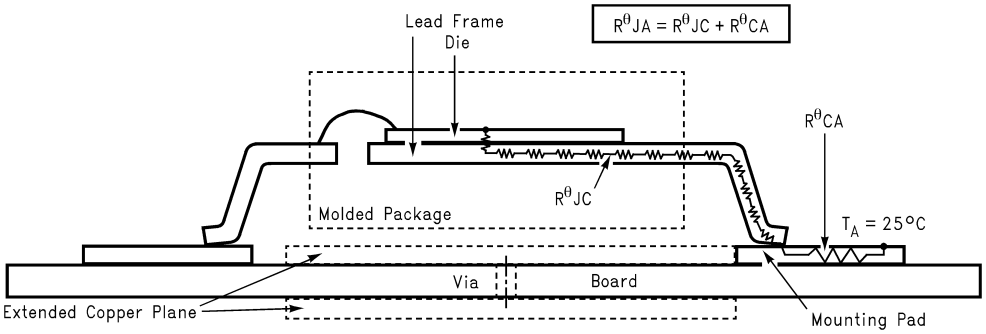

Figure 25. Cross-Sectional View of Integrated Circuit Mounted on a Printed Circuit Board.

Heat in the LMR12010 due to internal power dissipation is removed through conduction and/or convection.

Conduction: Heat transfer occurs through cross sectional areas of material. Depending on the material, the transfer of heat can be considered to have poor to good thermal conductivity properties (insulator vs conductor).

Heat transfer goes as:

silicon→package→lead frame→PCB.

Convection: Heat transfer is by means of airflow. This could be from a fan or natural convection. Natural convection occurs when air currents rise from the hot device to cooler air.

Thermal impedance is defined as:

$$R_\theta = \frac{\Delta T}{\text{Power}} \tag{38}$$

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Calculating The LMR12010 Junction Temperature (continued)

Thermal impedance from the silicon junction to the ambient air is defined as:

$$R_{\theta JA} = \frac{T_J - T_A}{Power} \quad (39)$$

This impedance can vary depending on the thermal properties of the PCB. This includes PCB size, weight of copper used to route traces and ground plane, and number of layers within the PCB. The type and number of thermal vias can also make a large difference in the thermal impedance. Thermal vias are necessary in most applications. They conduct heat from the surface of the PCB to the ground plane. Place two to four thermal vias close to the ground pin of the device.

The datasheet specifies two different $R_{\theta JA}$ numbers for the 6-pin SOT-23-THIN package. The two numbers show the difference in thermal impedance for a four-layer board with 2-oz. copper traces, vs. a four-layer board with 1oz. copper. $R_{\theta JA}$ equals 120°C/W for 2-oz. copper traces and GND plane, and 235°C/W for 1oz. copper traces and GND plane.

Method 1:

To accurately measure the silicon temperature for a given application, two methods can be used. The first method requires the user to know the thermal impedance of the silicon junction to case. ($R_{\theta JC}$) is approximately 80°C/W for the 6-pin SOT-23-THIN package. Knowing the internal dissipation from the efficiency calculation given previously, and the case temperature, which can be empirically measured on the bench we have:

$$R_{\theta JA} = \frac{T_J - T_C}{Power} \quad (40)$$

Therefore:

$$T_J = (R_{\theta JC} \times P_{LOSS}) + T_C \quad (41)$$

Table 3. Design Example 2

V_{IN}	5 V	P_{OUT}	2.5 W
V_{OUT}	2.5 V	P_{DIODE}	151 mW
I_{OUT}	1 A	P_{IND}	75 mW
V_D	0.35 V	P_{SWF}	53 mW
Freq	3 MHz	P_{SWR}	53 mW
I_Q	1.5 mA	P_{COND}	187 mW
T_{RISE}	8 ns	P_Q	7.5 mW
T_{FALL}	8 ns	P_{BOOST}	21 mW
R_{DSON}	330 mΩ	P_{LOSS}	**548 mW**
IND_{DCR}	75 mΩ		
D	**0.568**		

$$\Sigma P_{COND} + P_{SWF} + P_{SWR} + P_Q + P_{BOOST} = P_{INTERNAL}$$

$$P_{INTERNAL} = \mathbf{322\ mW}$$

$$T_J = (R_{\theta JC} \times Power) + T_C = 80^oC/W \times 322\ mW + T_C \quad (42)$$

The second method can give a very accurate silicon junction temperature. The first step is to determine $R_{\theta JA}$ of the application. The LMR12010 has over-temperature protection circuitry. When the silicon temperature reaches 165°C, the device stops switching. The protection circuitry has a hysteresis of 15°C. Once the silicon temperature has decreased to approximately 150°C, the device will start to switch again. Knowing this, the $R_{\theta JA}$ for any PCB can be characterized during the early stages of the design by raising the ambient temperature in the given application until the circuit enters thermal shutdown. If the SW pin is monitored, it will be obvious when the internal NFET stops switching indicating a junction temperature of 165°C. Knowing the internal power dissipation from the above methods, the junction temperature and the ambient temperature, $R_{\theta JA}$ can be determined.

$$R_{\theta JA} = \frac{165^oC - T_A}{P_{INTERNAL}} \quad (43)$$

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Once this is determined, the maximum ambient temperature allowed for a desired junction temperature can be found.

Table 4. Design Example 3

Package	SOT23-6		
V_{IN}	12 V	P_{OUT}	2.475 W
V_{OUT}	3.3 V	P_{DIODE}	523 mW
I_{OUT}	750 mA	P_{IND}	56.25 mW
V_D	0.35 V	P_{SWF}	108 mW
Freq	3 MHz	P_{SWR}	108 mW
I_Q	1.5 mA	P_{COND}	68.2 mW
I_{BOOST}	4 mA	P_Q	18 mW
V_{BOOST}	5 V	P_{BOOST}	20 mW
T_{RISE}	8 ns	P_{LOSS}	**902 mW**
T_{FALL}	8 ns		
R_{DSON}	400 mΩ		
IND_{DCR}	75 mΩ		
D	**30.3%**		

$$\Sigma P_{COND} + P_{SWF} + P_{SWR} + P_Q + P_{BOOST} = P_{INTERNAL}$$

$$P_{INTERNAL} = \mathbf{322\ mW} \quad (44)$$

Using a standard Texas Instruments 6-pin SOT-23-THIN demonstration board to determine the $R_{\theta JA}$ of the board. The four-layer PCB is constructed using FR4 with 1/2-oz copper traces. The copper ground plane is on the bottom layer. The ground plane is accessed by two vias. The board measures 2.5 cm × 3 cm. It was placed in an oven with no forced airflow.

The ambient temperature was raised to 94°C, and at that temperature, the device went into thermal shutdown.

$$R_{\theta JA} = \frac{165^oC - 94^oC}{322\ mW} = 220^oC/W \quad (45)$$

If the junction temperature was to be kept below 125°C, then the ambient temperature cannot go above 54.2°C.

$$T_J – (R_{\theta JA} \times P_{LOSS}) = T_A \quad (46)$$

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10 Device and Documentation Support

10.1 Device Support

10.1.1 Third-Party Products Disclaimer

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10.1.2 Development Support

10.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMR12010 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

10.4 Trademarks

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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10.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMR12010XMK/NOPB	Active	Production	SOT-23-THIN (DDC) | 6	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SF7B
LMR12010XMK/NOPB.A	Active	Production	SOT-23-THIN (DDC) | 6	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SF7B
LMR12010XMKE/NOPB	Active	Production	SOT-23-THIN (DDC) | 6	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SF7B
LMR12010XMKE/NOPB.A	Active	Production	SOT-23-THIN (DDC) | 6	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SF7B
LMR12010XMKX/NOPB	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SF7B
LMR12010XMKX/NOPB.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SF7B
LMR12010YMK/NOPB	Active	Production	SOT-23-THIN (DDC) | 6	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SF8B
LMR12010YMK/NOPB.A	Active	Production	SOT-23-THIN (DDC) | 6	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SF8B
LMR12010YMKE/NOPB	Active	Production	SOT-23-THIN (DDC) | 6	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SF8B
LMR12010YMKE/NOPB.A	Active	Production	SOT-23-THIN (DDC) | 6	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SF8B
LMR12010YMKX/NOPB	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SF8B
LMR12010YMKX/NOPB.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SF8B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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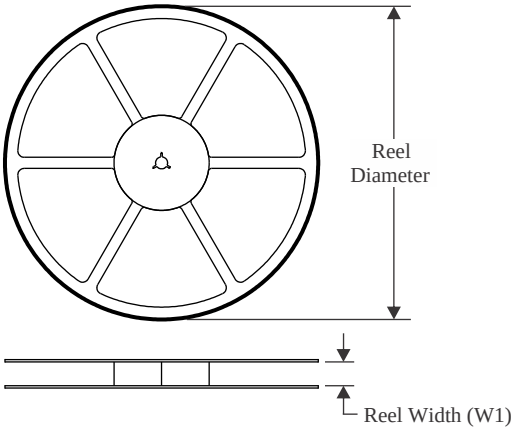
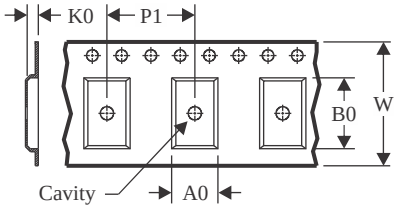
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

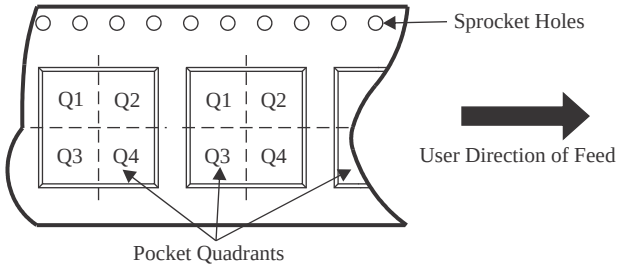


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

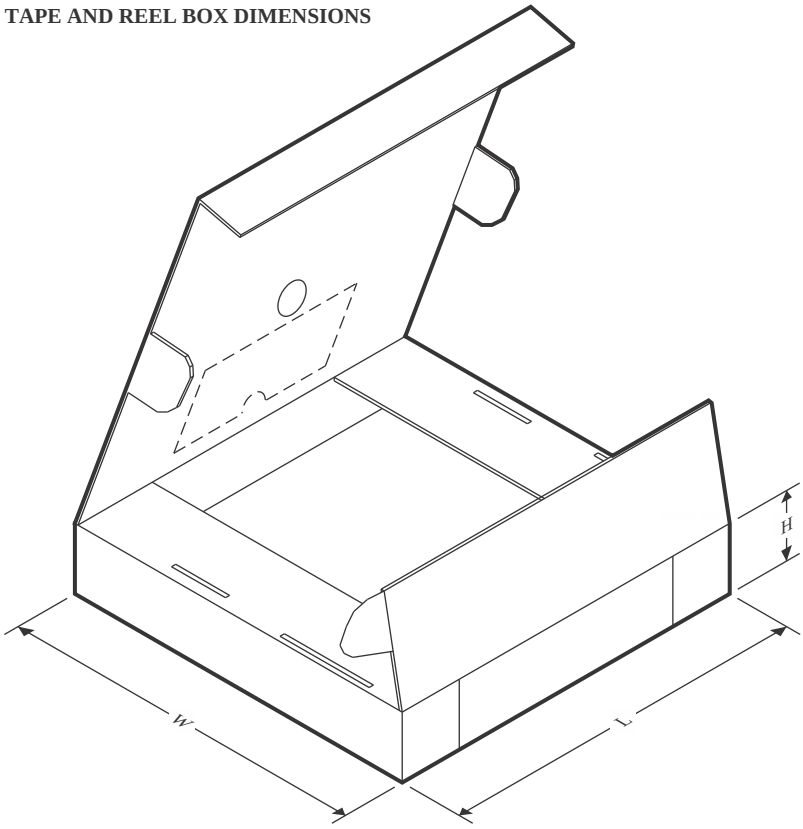
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMR12010XMK/NOPB	SOT-23-THIN	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMR12010XMKE/NOPB	SOT-23-THIN	DDC	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMR12010XMKX/NOPB	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMR12010YMK/NOPB	SOT-23-THIN	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMR12010YMKE/NOPB	SOT-23-THIN	DDC	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMR12010YMKX/NOPB	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

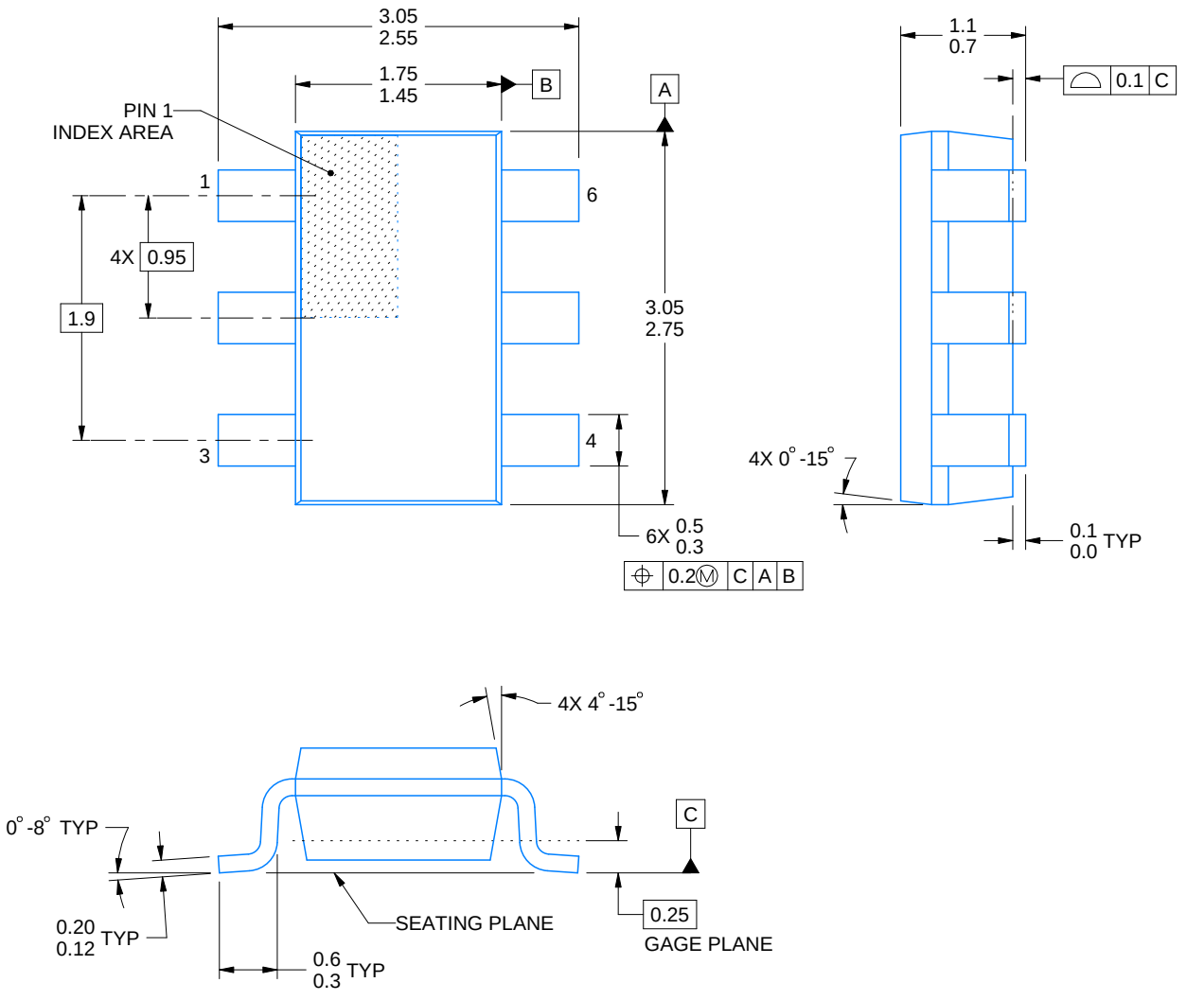
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMR12010XMK/NOPB	SOT-23-THIN	DDC	6	1000	208.0	191.0	35.0
LMR12010XMKE/NOPB	SOT-23-THIN	DDC	6	250	208.0	191.0	35.0
LMR12010XMKX/NOPB	SOT-23-THIN	DDC	6	3000	208.0	191.0	35.0
LMR12010YMK/NOPB	SOT-23-THIN	DDC	6	1000	208.0	191.0	35.0
LMR12010YMKE/NOPB	SOT-23-THIN	DDC	6	250	208.0	191.0	35.0
LMR12010YMKX/NOPB	SOT-23-THIN	DDC	6	3000	208.0	191.0	35.0

PACKAGE OUTLINE

DDC0006A

SOT-23 - 1.1 max height

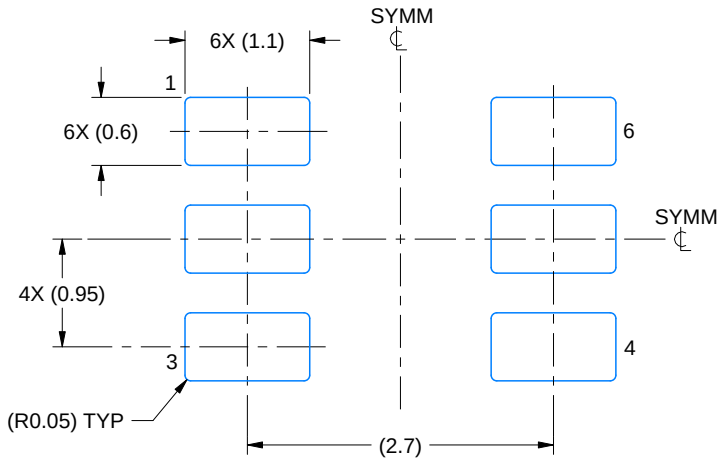
SMALL OUTLINE TRANSISTOR



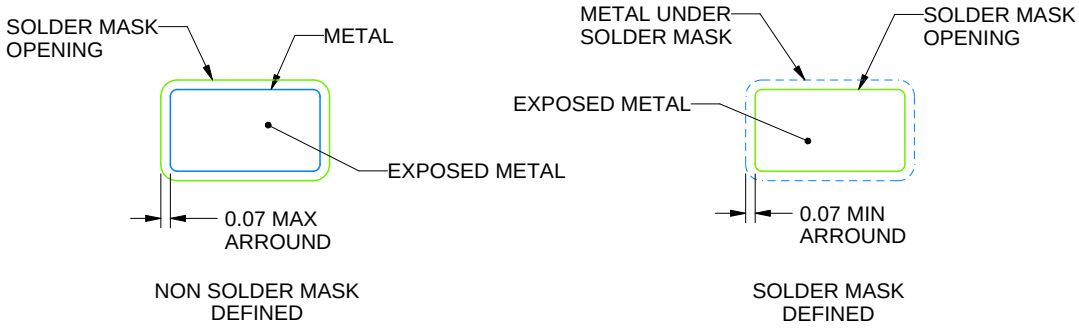
4214841/E 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X



SOLDERMASK DETAILS

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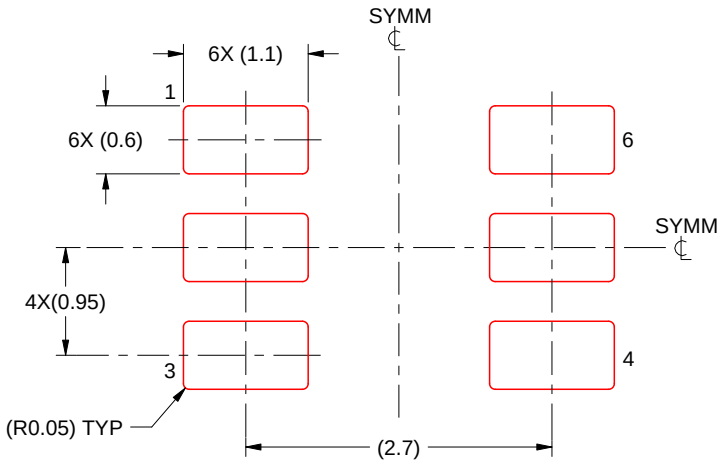
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214841/E 08/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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