

Single and Dual Precision, 17 MHz, Low Noise, CMOS Input Amplifiers

Check for Samples: [LMP7715](#), [LMP7716](#), [LMP7716Q](#)

FEATURES

- Unless Otherwise Noted, Typical Values at $V_S = 5V$.
 - Input Offset Voltage $\pm 150 \mu V$ (Max)
 - Input Bias Current 100 fA
 - Input Voltage Noise $5.8 nV/\sqrt{Hz}$
 - Gain Bandwidth Product 17 MHz
 - Supply Current (LMP7715) 1.15 mA
 - Supply Current (LMP7716/LMP7716Q) 1.30 mA
 - Supply Voltage Range 1.8V to 5.5V
 - THD+N @ $f = 1 kHz$ 0.001%
 - Operating Temperature Range $-40^\circ C$ to $125^\circ C$
 - Rail-to-rail Output Swing
 - Space Saving SOT-23 Package (LMP7715)
 - 8-Pin VSSOP Package (LMP7716/LMP7716Q)
 - LMP7716Q is AEC-Q100 Grade 1 Qualified and is Manufactured on an Automotive Grade Flow

APPLICATIONS

- Active Filters and Buffers
- Sensor Interface Applications
- Transimpedance Amplifiers
- Automotive

DESCRIPTION

The LMP7715/LMP7716/LMP7716Q are single and dual low noise, low offset, CMOS input, rail-to-rail output precision amplifiers with high gain bandwidth products. The LMP7715/LMP7716/LMP7716Q are part of the LMP™ precision amplifier family and are ideal for a variety of instrumentation applications.

Utilizing a CMOS input stage, the LMP7715/LMP7716/LMP7716Q achieve an input bias current of 100 fA, an input referred voltage noise of $5.8 nV/\sqrt{Hz}$, and an input offset voltage of less than $\pm 150 \mu V$. These features make the LMP7715/LMP7716/LMP7716Q superior choices for precision applications.

Consuming only 1.15 mA of supply current, the LMP7715 offers a high gain bandwidth product of 17 MHz, enabling accurate amplification at high closed loop gains.

The LMP7715/LMP7716/LMP7716Q have a supply voltage range of 1.8V to 5.5V, which makes these ideal choices for portable low power applications with low supply voltage requirements.

The LMP7715/LMP7716/LMP7716Q are built with TI's advanced VIP50 process technology. The LMP7715 is offered in a 5-pin SOT-23 package and the LMP7716/LMP7716Q is offered in an 8-pin VSSOP.

The LMP7716Q incorporates enhanced manufacturing and support processes for the automotive market, including defect detection methodologies. Reliability qualification is compliant with the requirements and temperature grades defined in the AEC-Q100 standard.



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Typical Performance

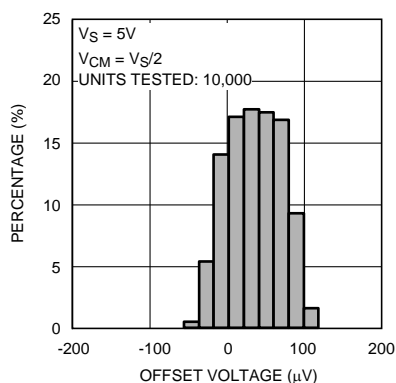


Figure 1. Offset Voltage Distribution

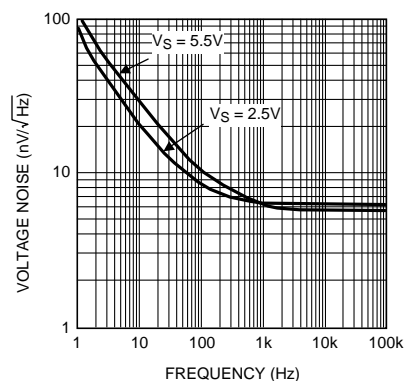


Figure 2. Input Referred Voltage Noise



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾⁽²⁾

| | | |
|--------------------------------------|------------------------------------|--------------------------------|
| ESD Tolerance ⁽³⁾ | Human Body Model | 2000V |
| | Machine Model | 200V |
| | Charge-Device Model | 1000V |
| V_{IN} Differential | | $\pm 0.3V$ |
| Supply Voltage ($V_S = V^+ - V^-$) | | 6.0V |
| Voltage on Input/Output Pins | | $V^+ + 0.3V, V^- - 0.3V$ |
| Storage Temperature Range | | $-65^\circ C$ to $150^\circ C$ |
| Junction Temperature ⁽⁴⁾ | | $+150^\circ C$ |
| Soldering Information | Infrared or Convection (20 sec) | $235^\circ C$ |
| | Wave Soldering Lead Temp. (10 sec) | $260^\circ C$ |

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics Tables.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
- (4) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

Operating Ratings⁽¹⁾

| | | |
|---|---|--------------------------------|
| Temperature Range ⁽²⁾ | | $-40^\circ C$ to $125^\circ C$ |
| Supply Voltage ($V_S = V^+ - V^-$) | $0^\circ C \leq T_A \leq 125^\circ C$ | 1.8V to 5.5V |
| | $-40^\circ C \leq T_A \leq 125^\circ C$ | 2.0V to 5.5V |
| Package Thermal Resistance (θ_{JA}) ⁽²⁾ | 5-Pin SOT-23 | $180^\circ C/W$ |
| | 8-Pin VSSOP | $236^\circ C/W$ |

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics Tables.
- (2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

2.5V Electrical Characteristics

Unless otherwise specified, all limits are ensured for $T_A = 25^\circ\text{C}$, $V^+ = 2.5\text{V}$, $V^- = 0\text{V}$, $V_O = V_{CM} = V^+/2$. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Min ⁽¹⁾ | Typ ⁽²⁾ | Max ⁽¹⁾ | Units |
|-------------|--|--|---|--------------------|--|------------------------------|
| V_{OS} | Input Offset Voltage | $-20^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ | | ± 20 | ± 180 ± 330 | μV |
| | | $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ | | ± 20 | ± 180 ± 430 | |
| TC V_{OS} | Input Offset Voltage Temperature Drift ⁽³⁾⁽⁴⁾ | LMP7715 | | -1 | ± 4 | $\mu\text{V}/^\circ\text{C}$ |
| | | LMP7716/LMP7716Q | | -1.75 | | |
| I_B | Input Bias Current | $V_{CM} = 1.0\text{V}^{(4)(5)}$ | $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ | 0.05 | 1 25 | pA |
| | | | $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ | 0.05 | 1 100 | |
| I_{OS} | Input Offset Current | $V_{CM} = 1\text{V}^{(4)}$ | | 0.006 | 0.5 50 | pA |
| CMRR | Common Mode Rejection Ratio | $0\text{V} \leq V_{CM} \leq 1.4\text{V}$ | 83 80 | 100 | | dB |
| PSRR | Power Supply Rejection Ratio | $2.0\text{V} \leq V^+ \leq 5.5\text{V}$ $V^- = 0\text{V}$, $V_{CM} = 0$ | 85 80 | 100 | | dB |
| | | $1.8\text{V} \leq V^+ \leq 5.5\text{V}$ $V^- = 0\text{V}$, $V_{CM} = 0$ | 85 | 98 | | |
| CMVR | Common Mode Voltage Range | CMRR $\geq 80\text{ dB}$ CMRR $\geq 78\text{ dB}$ | -0.3 -0.3 | | 1.5 1.5 | V |
| A_{VOL} | Open Loop Voltage Gain | LMP7715, $V_O = 0.15$ to 2.2V $R_L = 2\text{ k}\Omega$ to $V^+/2$ | 88 82 | 98 | | dB |
| | | LMP7716/LMP7716Q, $V_O = 0.15$ to 2.2V $R_L = 2\text{ k}\Omega$ to $V^+/2$ | 84 80 | 92 | | |
| | | LMP7715, $V_O = 0.15$ to 2.2V $R_L = 10\text{ k}\Omega$ to $V^+/2$ | 92 88 | 110 | | |
| | | LMP7716/ LMP7716Q, $V_O = 0.15$ to 2.2V $R_L = 10\text{ k}\Omega$ to $V^+/2$ | 90 86 | 95 | | |
| V_{OUT} | Output Voltage Swing High | $R_L = 2\text{ k}\Omega$ to $V^+/2$ | | 25 | 70 77 | mV from either rail |
| | | $R_L = 10\text{ k}\Omega$ to $V^+/2$ | | 20 | 60 66 | |
| | Output Voltage Swing Low | $R_L = 2\text{ k}\Omega$ to $V^+/2$ | | 30 | 70 73 | |
| | | $R_L = 10\text{ k}\Omega$ to $V^+/2$ | | 15 | 60 62 | |
| I_{OUT} | Output Current | Sourcing to V^- $V_{IN} = 200\text{ mV}^{(6)}$ | 36 30 | 52 | | mA |
| | | Sinking to V^+ $V_{IN} = -200\text{ mV}^{(6)}$ | 7.5 5.0 | 15 | | |
| I_S | Supply Current | LMP7715 | | 0.95 | 1.30 1.65 | mA |
| | | LMP7716/LMP7716Q (per channel) | | 1.10 | 1.50 1.85 | |
| SR | Slew Rate | $A_V = +1$, Rising (10% to 90%) | | 8.3 | | $\text{V}/\mu\text{s}$ |
| | | $A_V = +1$, Falling (90% to 10%) | | 10.3 | | |

- (1) Limits are 100% production tested at 25°C . Limits over the operating temperature range are specified through correlations using the Statistical Quality Control (SQC) method.
- (2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
- (3) Offset voltage average drift is determined by dividing the change in V_{OS} at the temperature extremes by the total temperature change.
- (4) This parameter is specified by design and/or characterization and is not tested in production.
- (5) Positive current corresponds to current flowing into the device.
- (6) The short circuit test is a momentary open loop test.

2.5V Electrical Characteristics (continued)

Unless otherwise specified, all limits are ensured for $T_A = 25^\circ\text{C}$, $V^+ = 2.5\text{V}$, $V^- = 0\text{V}$, $V_O = V_{CM} = V^+/2$. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Min ⁽¹⁾ | Typ ⁽²⁾ | Max ⁽¹⁾ | Units |
|--------|--------------------------------------|--|--------------------|--------------------|--------------------|------------------------|
| GBW | Gain Bandwidth | | | 14 | | MHz |
| e_n | Input Referred Voltage Noise Density | $f = 400\text{ Hz}$ | | 6.8 | | nV/ |
| | | $f = 1\text{ kHz}$ | | 5.8 | | |
| i_n | Input Referred Current Noise Density | $f = 1\text{ kHz}$ | | 0.01 | | pA/ $\sqrt{\text{Hz}}$ |
| THD+N | Total Harmonic Distortion + Noise | $f = 1\text{ kHz}$, $A_V = 1$, $R_L = 100\text{ k}\Omega$ $V_O = 0.9\text{ V}_{PP}$ | | 0.003 | | % |
| | | $f = 1\text{ kHz}$, $A_V = 1$, $R_L = 600\Omega$ $V_O = 0.9\text{ V}_{PP}$ | | 0.004 | | |

5V Electrical Characteristics

Unless otherwise specified, all limits are ensured for $T_A = 25^\circ\text{C}$, $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = V^+/2$. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Min ⁽¹⁾ | Typ ⁽²⁾ | Max ⁽¹⁾ | Units |
|-------------|--|---|---------------------|--------------------|--|------------------------------|
| V_{OS} | Input Offset Voltage | $-20^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ | | ± 10 | ± 150 ± 300 | μV |
| | | $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ | | ± 10 | ± 150 ± 400 | |
| TC V_{OS} | Input Offset Voltage Temperature Drift ⁽³⁾⁽⁴⁾ | LMP7715 | | -1 | ± 4 | $\mu\text{V}/^\circ\text{C}$ |
| | | LMP7716/LMP7716Q | | -1.75 | | |
| I_B | Input Bias Current | $V_{CM} = 2.0\text{V}^{(4)(5)}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ | | 0.1 | 1 25 | pA |
| | | $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ | | 0.1 | 1 100 | |
| I_{OS} | Input Offset Current | $V_{CM} = 2.0\text{V}^{(4)}$ | | 0.01 | 0.5 50 | pA |
| CMRR | Common Mode Rejection Ratio | $0\text{V} \leq V_{CM} \leq 3.7\text{V}$ | 85 82 | 100 | | dB |
| PSRR | Power Supply Rejection Ratio | $2.0\text{V} \leq V^+ \leq 5.5\text{V}$ $V^- = 0\text{V}$, $V_{CM} = 0$ | 85 80 | 100 | | dB |
| | | $1.8\text{V} \leq V^+ \leq 5.5\text{V}$ $V^- = 0\text{V}$, $V_{CM} = 0$ | 85 | 98 | | |
| CMVR | Common Mode Voltage Range | CMRR $\geq 80\text{ dB}$ CMRR $\geq 78\text{ dB}$ | -0.3 -0.3 | | 4 4 | V |
| A_{VOL} | Open Loop Voltage Gain | LMP7715, $V_O = 0.3\text{ to }4.7\text{V}$ $R_L = 2\text{ k}\Omega$ to $V^+/2$ | 88 82 | 107 | | dB |
| | | LMP7716/LMP7716Q, $V_O = 0.3\text{ to }4.7\text{V}$ $R_L = 2\text{ k}\Omega$ to $V^+/2$ | 84 80 | 90 | | |
| | | LMP7715, $V_O = 0.3\text{ to }4.7\text{V}$ $R_L = 10\text{ k}\Omega$ to $V^+/2$ | 92 88 | 110 | | |
| | | LMP7716/LMP7716Q, $V_O = 0.3\text{ to }4.7\text{V}$ $R_L = 10\text{ k}\Omega$ to $V^+/2$ | 90 86 | 95 | | |

(1) Limits are 100% production tested at 25°C . Limits over the operating temperature range are specified through correlations using the Statistical Quality Control (SQC) method.

(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.

(3) Offset voltage average drift is determined by dividing the change in V_{OS} at the temperature extremes by the total temperature change.

(4) This parameter is specified by design and/or characterization and is not tested in production.

(5) Positive current corresponds to current flowing into the device.

5V Electrical Characteristics (continued)

Unless otherwise specified, all limits are ensured for $T_A = 25^\circ\text{C}$, $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = V^+/2$. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Min ⁽¹⁾ | Typ ⁽²⁾ | Max ⁽¹⁾ | Units |
|-----------|--------------------------------------|--|--------------------|--------------------|---------------------|------------------------------|
| V_{OUT} | Output Voltage Swing High | $R_L = 2\text{ k}\Omega$ to $V^+/2$ | | 32 | 70 77 | mV from either rail |
| | | $R_L = 10\text{ k}\Omega$ to $V^+/2$ | | 22 | 60 66 | |
| | Output Voltage Swing Low | $R_L = 2\text{ k}\Omega$ to $V^+/2$ (LMP7715) | | 42 | 70 73 | |
| | | $R_L = 2\text{ k}\Omega$ to $V^+/2$ (LMP7716/LMP7716Q) | | 45 | 75 78 | |
| | | $R_L = 10\text{ k}\Omega$ to $V^+/2$ | | 20 | 60 62 | |
| I_{OUT} | Output Current | Sourcing to V^- $V_{IN} = 200\text{ mV}^{(6)}$ | 46 38 | 66 | | mA |
| | | Sinking to V^+ $V_{IN} = -200\text{ mV}^{(6)}$ | 10.5 6.5 | 23 | | |
| I_S | Supply Current | LMP7715 | | 1.15 | 1.40 1.75 | mA |
| | | LMP7716/LMP7716Q (per channel) | | 1.30 | 1.70 2.05 | |
| SR | Slew Rate | $A_V = +1$, Rising (10% to 90%) | 6.0 | 9.5 | | V/ μs |
| | | $A_V = +1$, Falling (90% to 10%) | 7.5 | 11.5 | | |
| GBW | Gain Bandwidth | | | 17 | | MHz |
| e_n | Input Referred Voltage Noise Density | $f = 400\text{ Hz}$ | | 7.0 | | $\text{nV}/\sqrt{\text{Hz}}$ |
| | | $f = 1\text{ kHz}$ | | 5.8 | | |
| i_n | Input Referred Current Noise Density | $f = 1\text{ kHz}$ | | 0.01 | | $\text{pA}/\sqrt{\text{Hz}}$ |
| THD+N | Total Harmonic Distortion + Noise | $f = 1\text{ kHz}$, $A_V = 1$, $R_L = 100\text{ k}\Omega$ $V_O = 4\text{ V}_{PP}$ | | 0.001 | | % |
| | | $f = 1\text{ kHz}$, $A_V = 1$, $R_L = 600\Omega$ $V_O = 4\text{ V}_{PP}$ | | 0.004 | | |

(6) The short circuit test is a momentary open loop test.

Connection Diagram

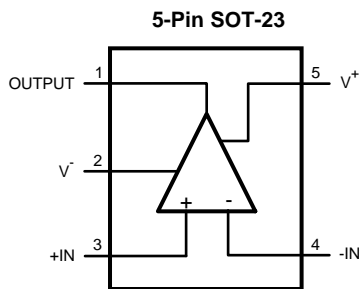


Figure 3. Top View

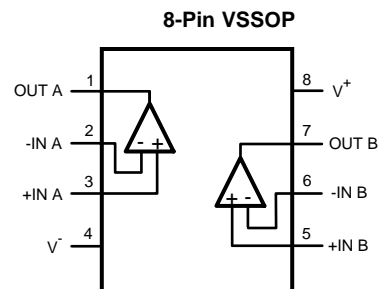


Figure 4. Top View

Typical Performance Characteristics

Unless otherwise noted: $T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$, $V_{CM} = V_S/2$.

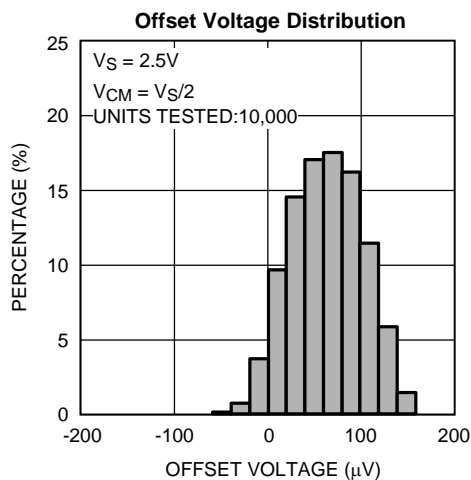


Figure 5.

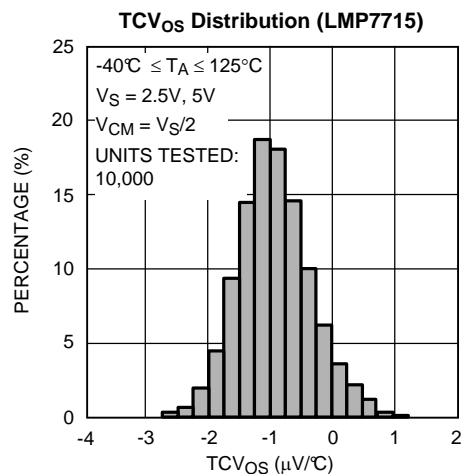


Figure 6.

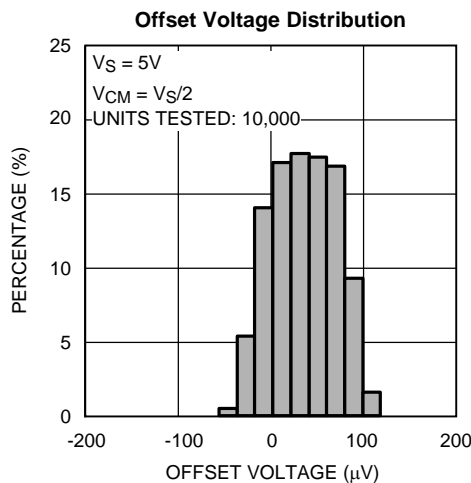


Figure 7.

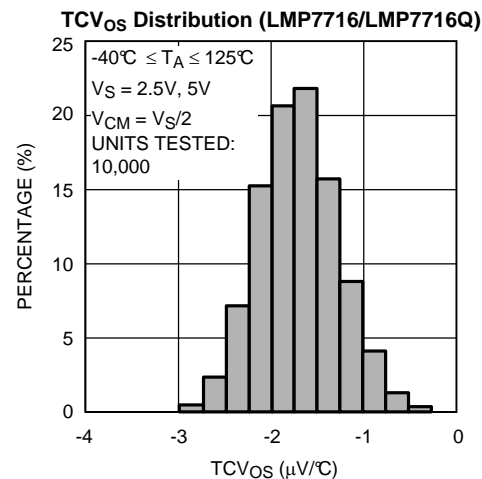


Figure 8.

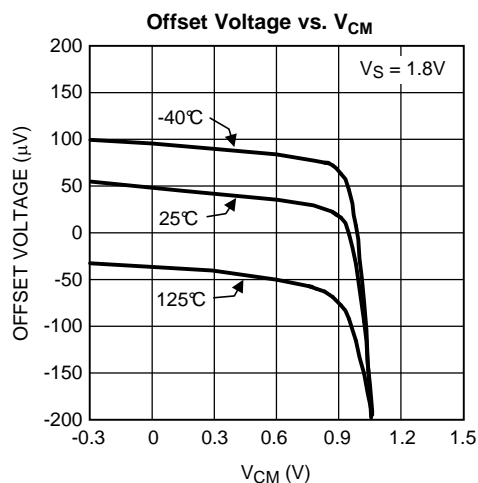


Figure 9.

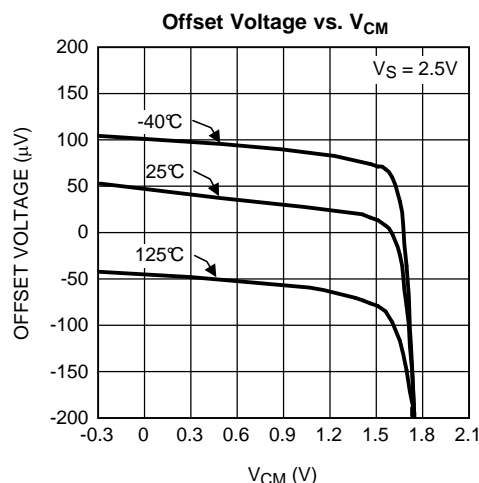


Figure 10.

Typical Performance Characteristics (continued)

Unless otherwise noted: $T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$, $V_{CM} = V_S/2$.

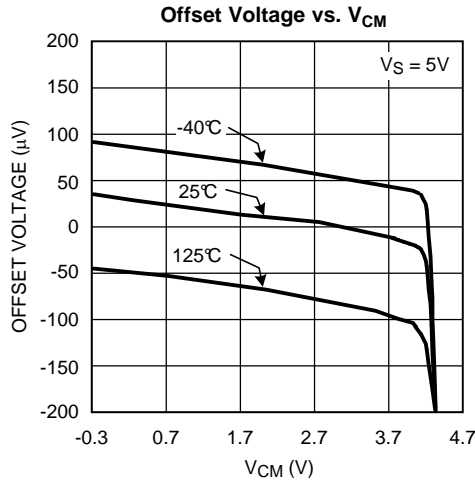


Figure 11.

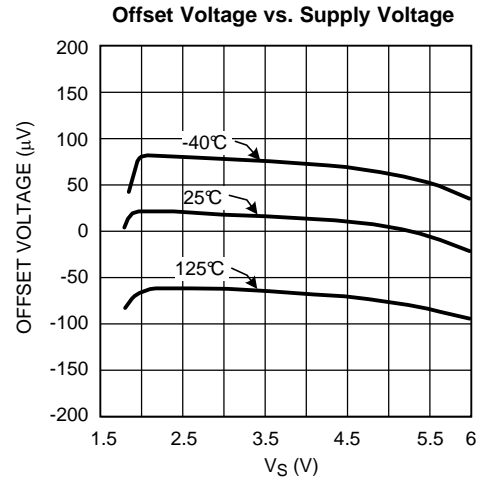


Figure 12.

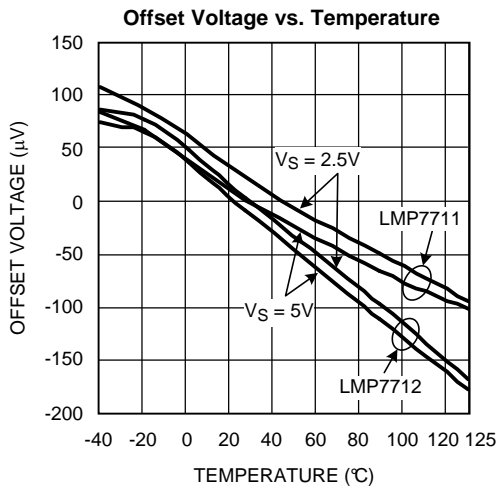


Figure 13.

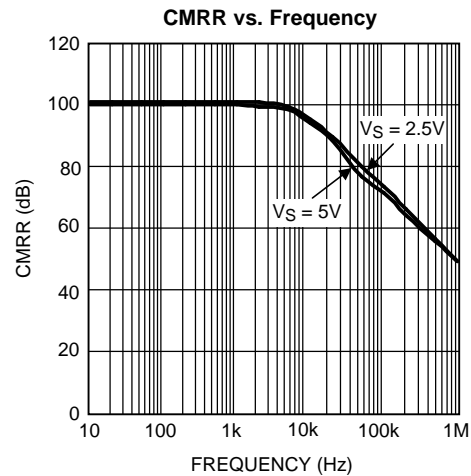


Figure 14.

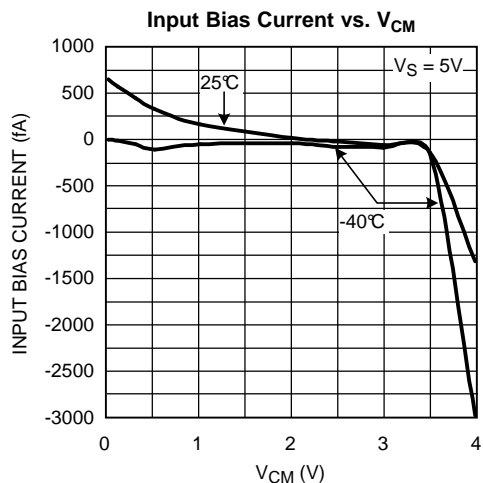


Figure 15.

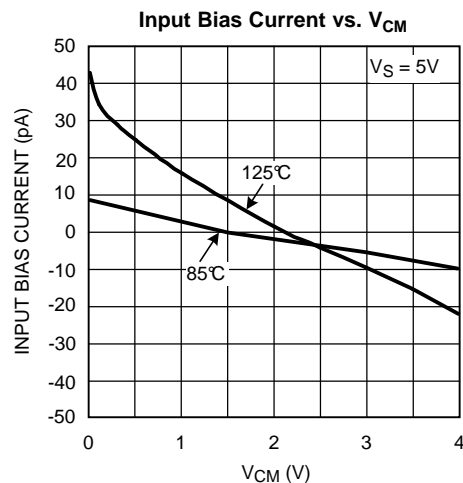


Figure 16.

Typical Performance Characteristics (continued)

Unless otherwise noted: $T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$, $V_{CM} = V_S/2$.

Supply Current vs. Supply Voltage (LMP7715)

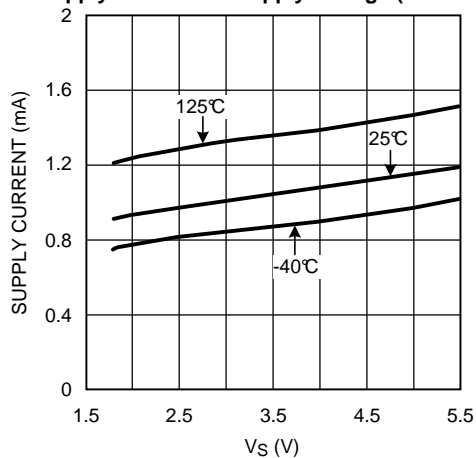


Figure 17.

Supply Current vs. Supply Voltage (LMP7716/LMP7716Q)

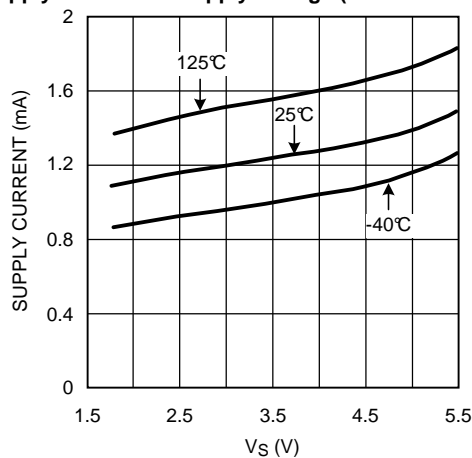


Figure 18.

Crosstalk Rejection Ratio (LMP7716/LMP7716Q)

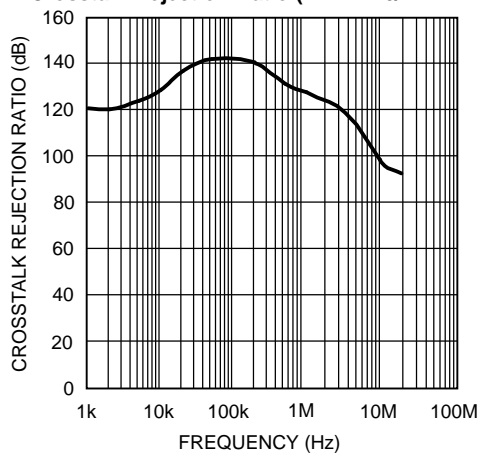


Figure 19.

Sourcing Current vs. Supply Voltage

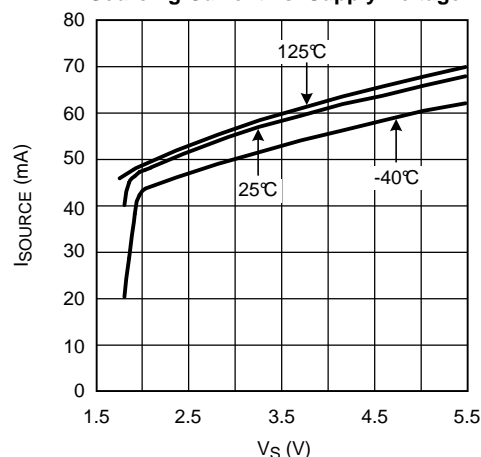


Figure 20.

Sinking Current vs. Supply Voltage

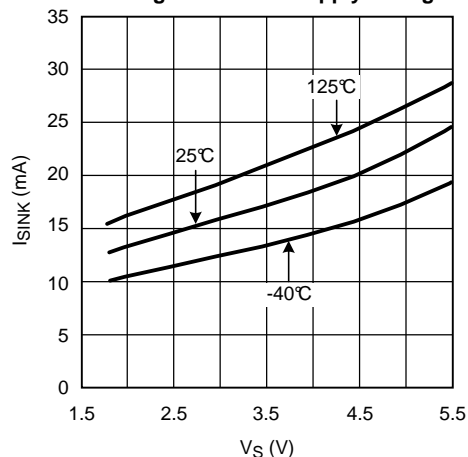


Figure 21.

Sourcing Current vs. Output Voltage

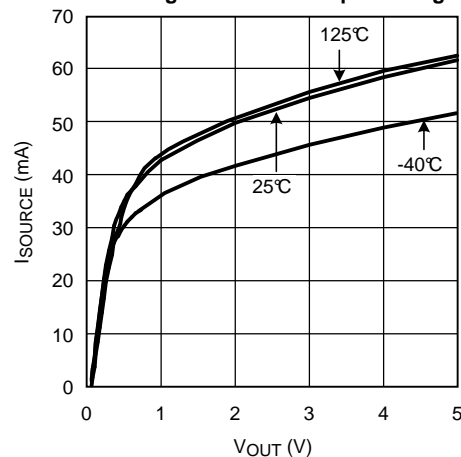


Figure 22.

Typical Performance Characteristics (continued)

Unless otherwise noted: $T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$, $V_{CM} = V_S/2$.

Sinking Current vs. Output Voltage

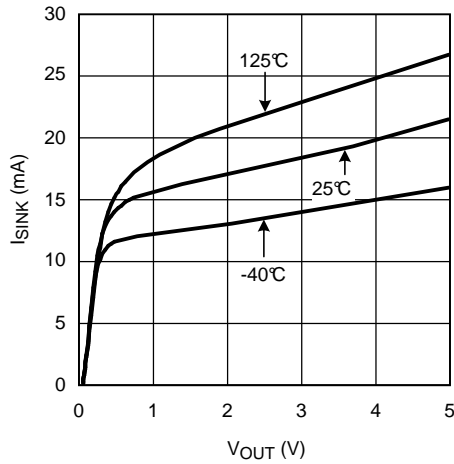


Figure 23.

Output Swing High vs. Supply Voltage

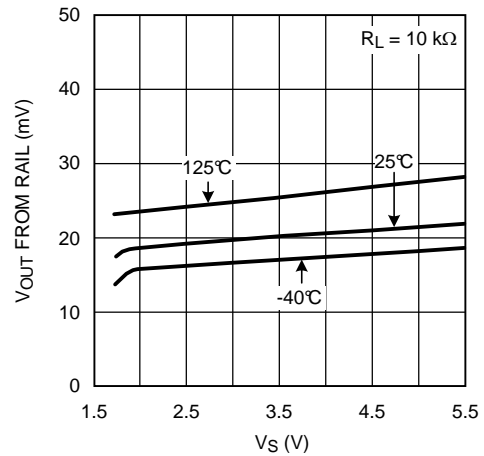


Figure 24.

Output Swing Low vs. Supply Voltage

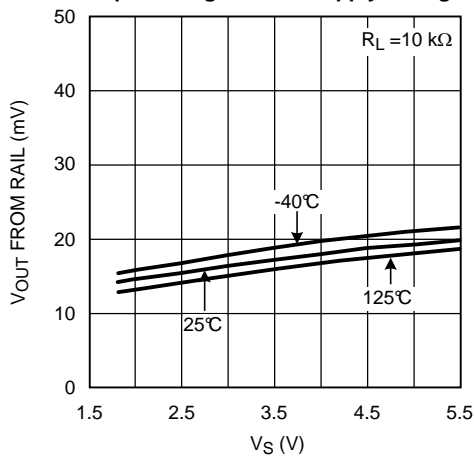


Figure 25.

Output Swing High vs. Supply Voltage

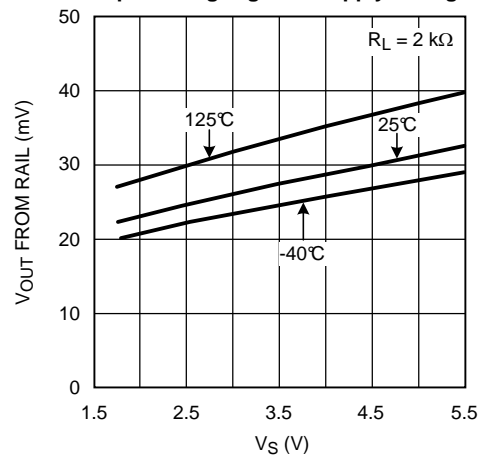


Figure 26.

Output Swing Low vs. Supply Voltage

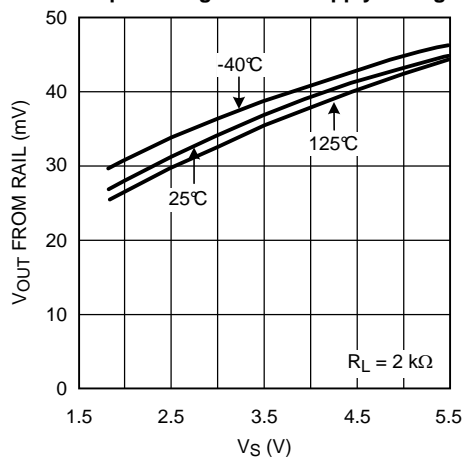


Figure 27.

Output Swing High vs. Supply Voltage

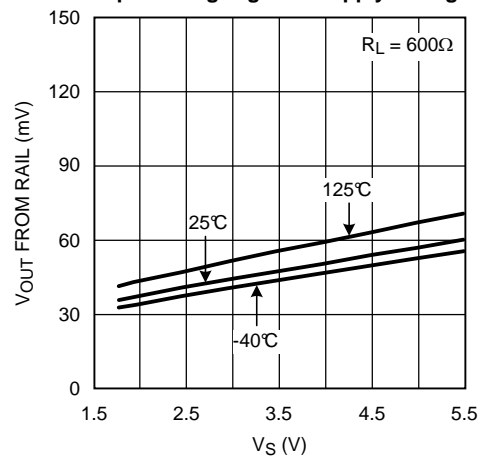


Figure 28.

Typical Performance Characteristics (continued)

Unless otherwise noted: $T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$, $V_{CM} = V_S/2$.

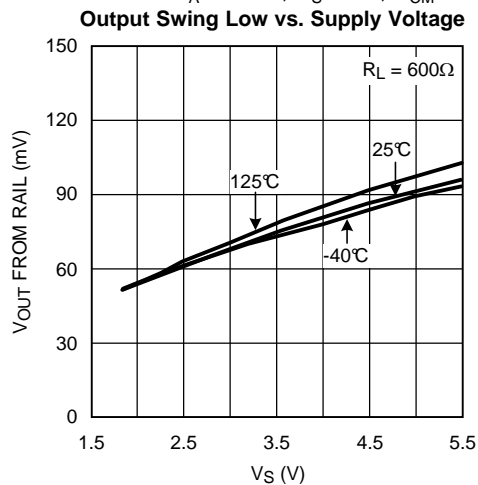


Figure 29.

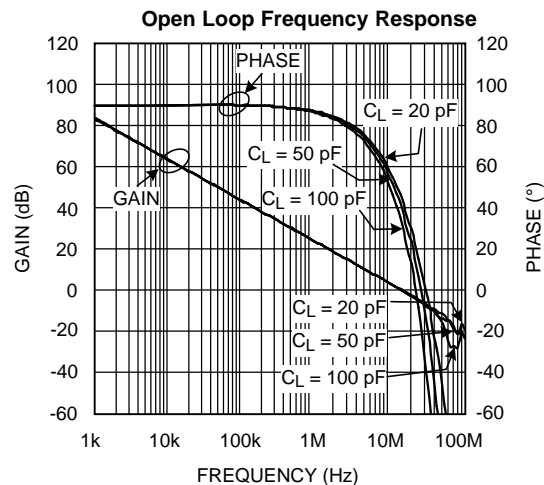


Figure 30.

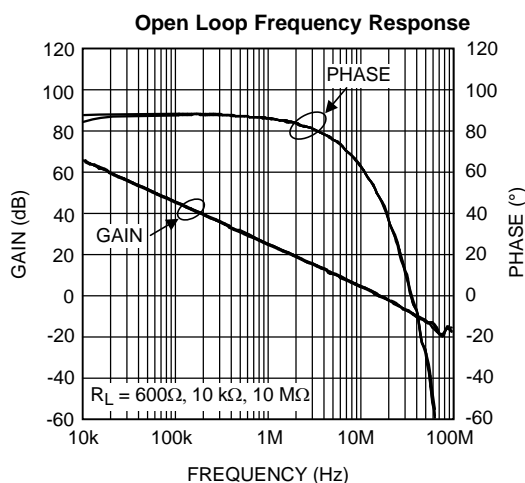


Figure 31.

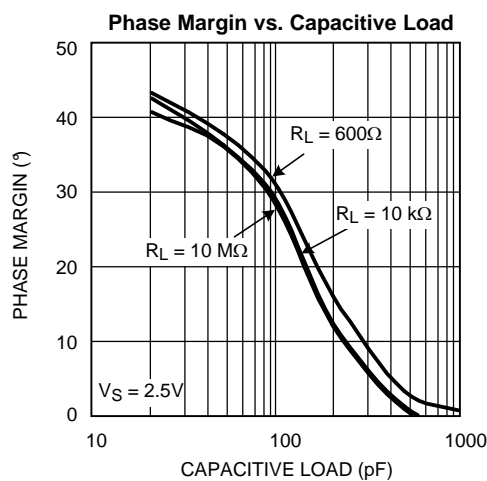


Figure 32.

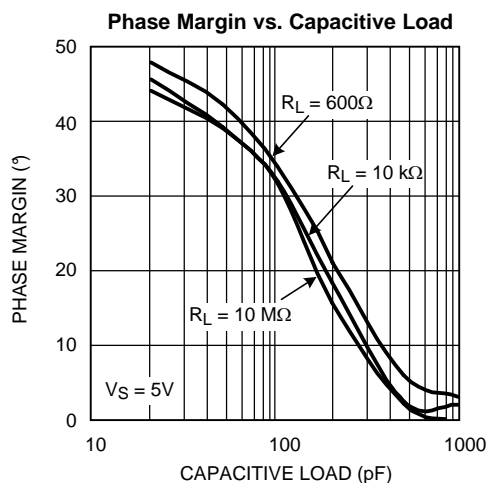


Figure 33.

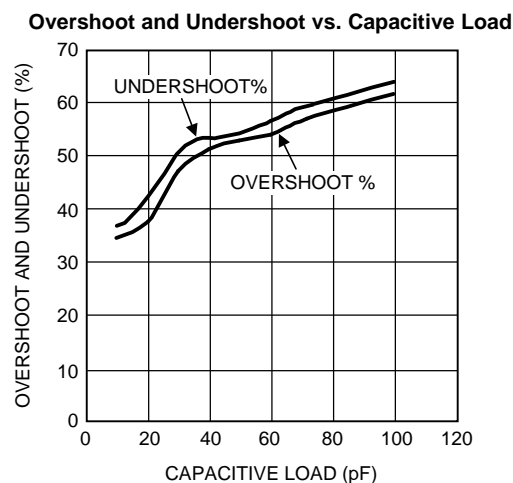


Figure 34.

Typical Performance Characteristics (continued)

Unless otherwise noted: $T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$, $V_{CM} = V_S/2$.

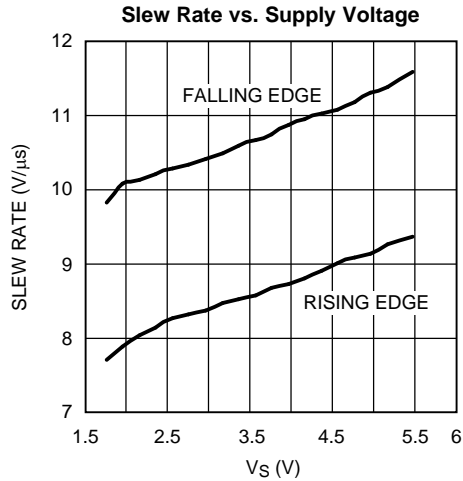


Figure 35.

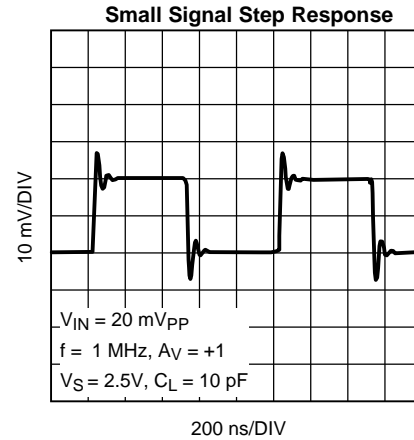


Figure 36.

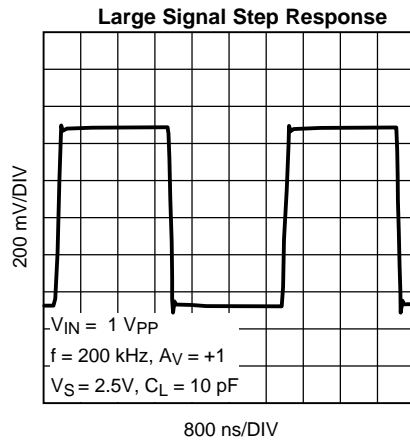


Figure 37.

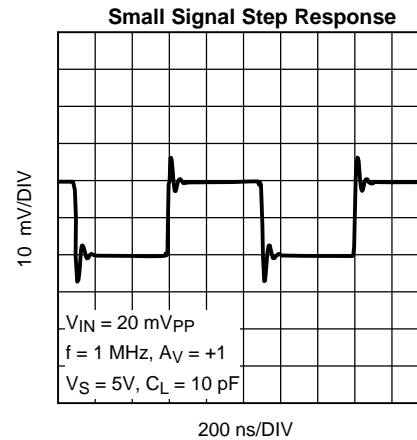


Figure 38.

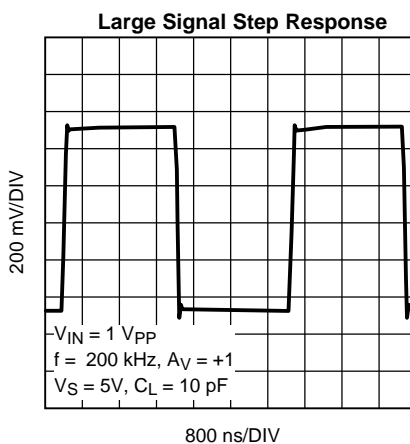


Figure 39.

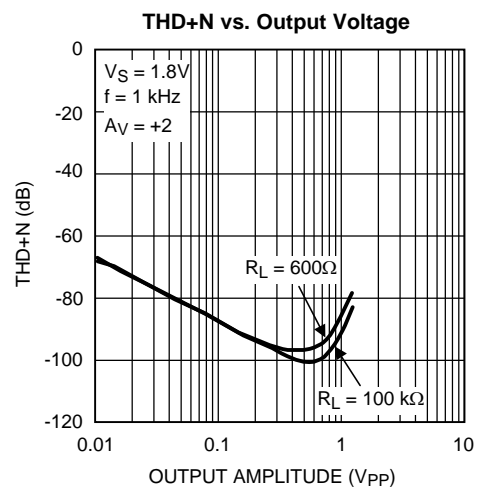


Figure 40.

Typical Performance Characteristics (continued)

Unless otherwise noted: $T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$, $V_{CM} = V_S/2$.

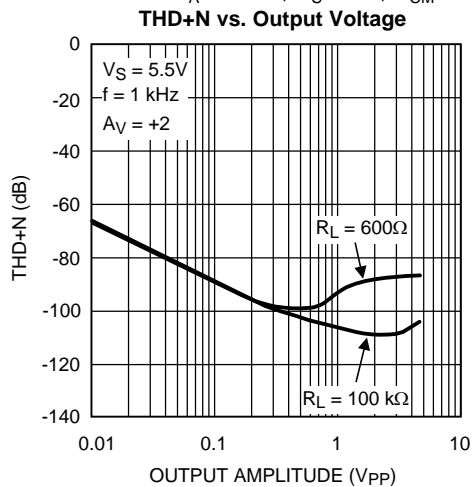


Figure 41.

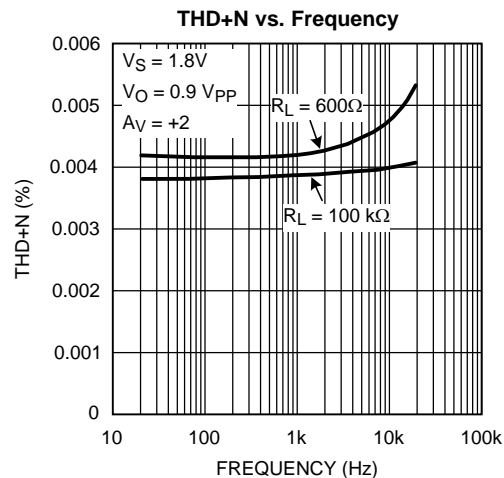


Figure 42.

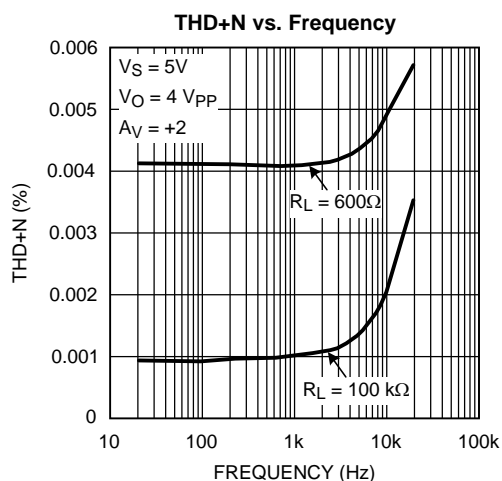


Figure 43.

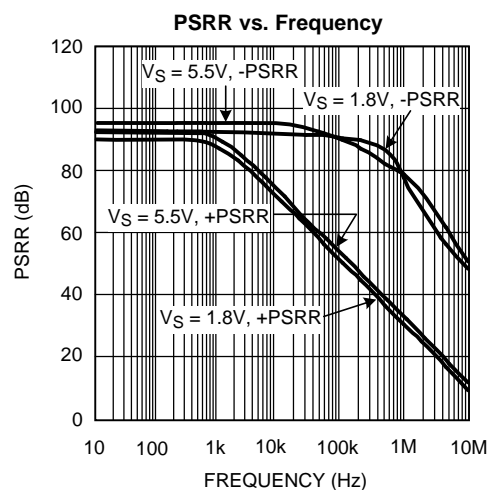


Figure 44.

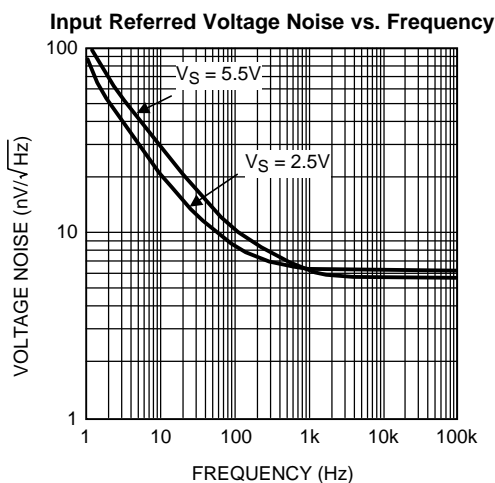


Figure 45.

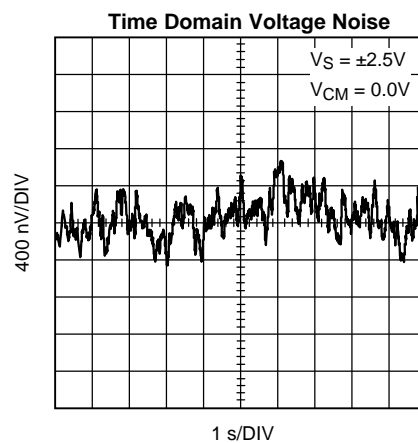


Figure 46.

Typical Performance Characteristics (continued)

Unless otherwise noted: $T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$, $V_{CM} = V_S/2$.

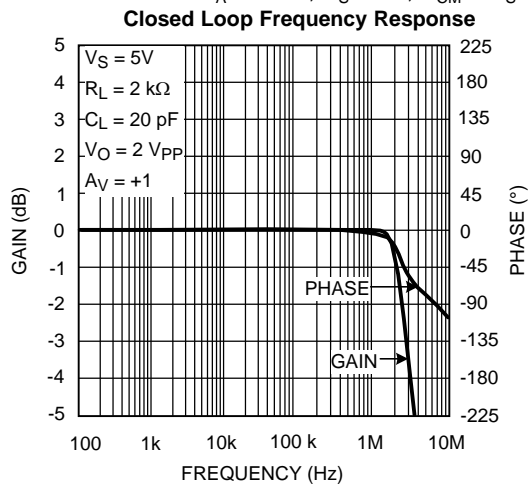


Figure 47.

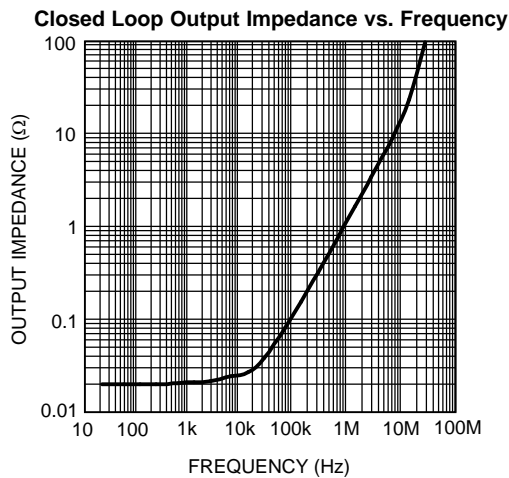


Figure 48.

APPLICATION INFORMATION

LMP7715/LMP7716/LMP7716Q

The LMP7715/LMP7716/LMP7716Q are single and dual, low noise, low offset, rail-to-rail output precision amplifiers with a wide gain bandwidth product of 17 MHz and low supply current. The wide bandwidth makes the LMP7715/LMP7716/LMP7716Q ideal choices for wide-band amplification in portable applications.

The LMP7715/LMP7716/LMP7716Q are superior for sensor applications. The very low input referred voltage noise of only 5.8 nV/√Hz at 1 kHz and very low input referred current noise of only 10 fA/√Hz mean more signal fidelity and higher signal-to-noise ratio.

The LMP7715/LMP7716/LMP7716Q have a supply voltage range of 1.8V to 5.5V over a wide temperature range of 0°C to 125°C. This is optimal for low voltage commercial applications. For applications where the ambient temperature might be less than 0°C, the LMP7715/LMP7716/LMP7716Q are fully operational at supply voltages of 2.0V to 5.5V over the temperature range of -40°C to 125°C.

The outputs of the LMP7715/LMP7716/LMP7716Q swing within 25 mV of either rail providing maximum dynamic range in applications requiring low supply voltage. The input common mode range of the LMP7715/LMP7716/LMP7716Q extends to 300 mV below ground. This feature enables users to utilize this device in single supply applications.

The use of a very innovative feedback topology has enhanced the current drive capability of the LMP7715/LMP7716/LMP7716Q, resulting in sourcing currents of as much as 47 mA with a supply voltage of only 1.8V.

The LMP7715 is offered in the space saving SOT-23 package and the LMP7716/LMP7716Q is offered in an 8-pin VSSOP. These small packages are ideal solutions for applications requiring minimum PC board footprint.

CAPACITIVE LOAD

The unity gain follower is the most sensitive configuration to capacitive loading. The combination of a capacitive load placed directly on the output of an amplifier along with the output impedance of the amplifier creates a phase lag which in turn reduces the phase margin of the amplifier. If phase margin is significantly reduced, the response will be either underdamped or the amplifier will oscillate.

The LMP7715/LMP7716/LMP7716Q can directly drive capacitive loads of up to 120 pF without oscillating. To drive heavier capacitive loads, an isolation resistor, R_{ISO} as shown in Figure 49, should be used. This resistor and C_L form a pole and hence delay the phase lag or increase the phase margin of the overall system. The larger the value of R_{ISO} , the more stable the output voltage will be. However, larger values of R_{ISO} result in reduced output swing and reduced output current drive.

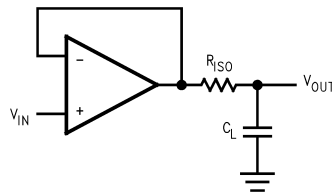


Figure 49. Isolating Capacitive Load

INPUT CAPACITANCE

CMOS input stages inherently have low input bias current and higher input referred voltage noise. The LMP7715/LMP7716/LMP7716Q enhance this performance by having the low input bias current of only 50 fA, as well as, a very low input referred voltage noise of 5.8 nV/√Hz. In order to achieve this a larger input stage has been used. This larger input stage increases the input capacitance of the LMP7715/LMP7716/LMP7716Q. Figure 50 shows typical input common mode capacitance of the LMP7715/LMP7716/LMP7716Q.

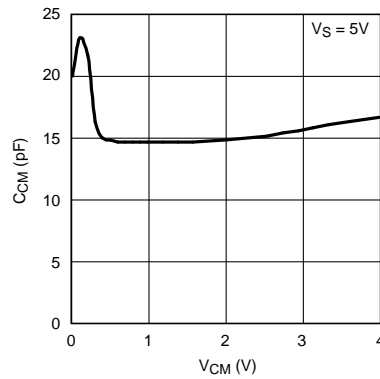
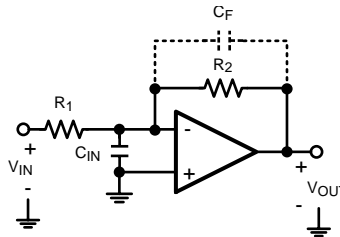


Figure 50. Input Common Mode Capacitance

This input capacitance will interact with other impedances, such as gain and feedback resistors which are seen on the inputs of the amplifier, to form a pole. This pole will have little or no effect on the output of the amplifier at low frequencies and under DC conditions, but will play a bigger role as the frequency increases. At higher frequencies, the presence of this pole will decrease phase margin and also cause gain peaking. In order to compensate for the input capacitance, care must be taken in choosing feedback resistors. In addition to being selective in picking values for the feedback resistor, a capacitor can be added to the feedback path to increase stability.

The DC gain of the circuit shown in Figure 51 is simply $-R_2/R_1$.



$$A_V = - \frac{V_{OUT}}{V_{IN}} = - \frac{R_2}{R_1}$$

Figure 51. Compensating for Input Capacitance

For the time being, ignore C_F . The AC gain of the circuit in Figure 51 can be calculated as follows:

$$\frac{V_{OUT}}{V_{IN}}(s) = \frac{-R_2/R_1}{1 + \frac{s}{\left(\frac{A_0 R_1}{R_1 + R_2}\right)} + \frac{s^2}{\left(\frac{A_0}{C_{IN} R_2}\right)}} \quad (1)$$

This equation is rearranged to find the location of the two poles:

$$P_{1,2} = \frac{-1}{2C_{IN}} \left[\frac{1}{R_1} + \frac{1}{R_2} \pm \sqrt{\left(\frac{1}{R_1} + \frac{1}{R_2}\right)^2 - \frac{4 A_0 C_{IN}}{R_2}} \right] \quad (2)$$

As shown in Equation 2, as the values of R_1 and R_2 are increased, the magnitude of the poles are reduced, which in turn decreases the bandwidth of the amplifier. Figure 52 shows the frequency response with different value resistors for R_1 and R_2 . Whenever possible, it is best to choose smaller feedback resistors.

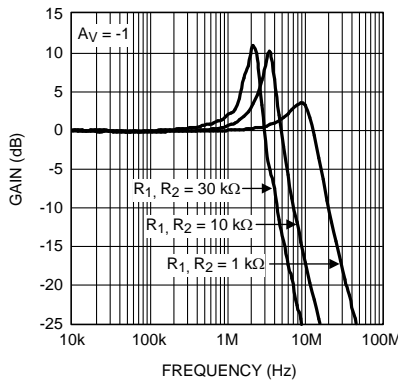


Figure 52. Closed Loop Frequency Response

As mentioned before, adding a capacitor to the feedback path will decrease the peaking. This is because C_F will form yet another pole in the system and will prevent pairs of poles, or complex conjugates from forming. It is the presence of pairs of poles that cause the peaking of gain. Figure 53 shows the frequency response of the schematic presented in Figure 51 with different values of C_F . As can be seen, using a small value capacitor significantly reduces or eliminates the peaking.

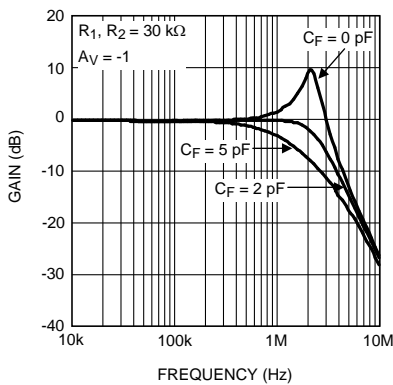


Figure 53. Closed Loop Frequency Response

TRANSIMPEDANCE AMPLIFIER

In many applications the signal of interest is a very small amount of current that needs to be detected. Current that is transmitted through a photodiode is a good example. Barcode scanners, light meters, fiber optic receivers, and industrial sensors are some typical applications utilizing photodiodes for current detection. This current needs to be amplified before it can be further processed. This amplification is performed using a current-to-voltage converter configuration or transimpedance amplifier. The signal of interest is fed to the inverting input of an op amp with a feedback resistor in the current path. The voltage at the output of this amplifier will be equal to the negative of the input current times the value of the feedback resistor. Figure 54 shows a transimpedance amplifier configuration. C_D represents the photodiode parasitic capacitance and C_{CM} denotes the common-mode capacitance of the amplifier. The presence of all of these capacitances at higher frequencies might lead to less stable topologies at higher frequencies. Care must be taken when designing a transimpedance amplifier to prevent the circuit from oscillating.

With a wide gain bandwidth product, low input bias current and low input voltage and current noise, the LMP7715/LMP7716/LMP7716Q are ideal for wideband transimpedance applications.

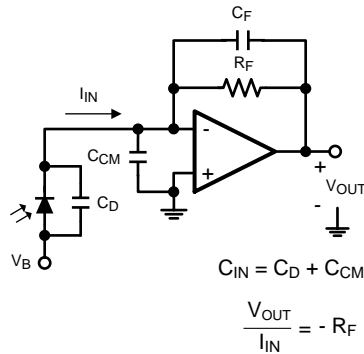


Figure 54. Transimpedance Amplifier

A feedback capacitance C_F is usually added in parallel with R_F to maintain circuit stability and to control the frequency response. To achieve a maximally flat, 2nd order response, R_F and C_F should be chosen by using [Equation 3](#)

$$C_F = \sqrt{\frac{C_{IN}}{GBWP * 2 \pi R_F}} \quad (3)$$

Calculating C_F from [Equation 3](#) can sometimes result in capacitor values which are less than 2 pF. This is especially the case for high speed applications. In these instances, it is often more practical to use the circuit shown in [Figure 55](#) in order to allow more sensible choices for C_F . The new feedback capacitor, C_F' , is $(1 + R_B/R_A) C_F$. This relationship holds as long as $R_A \ll R_F$.

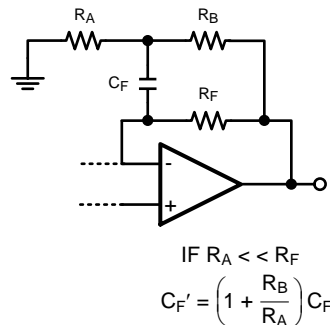


Figure 55. Modified Transimpedance Amplifier

SENSOR INTERFACE

The LMP7715/LMP7716/LMP7716Q have low input bias current and low input referred noise, which make them ideal choices for sensor interfaces such as thermopiles, Infra Red (IR) thermometry, thermocouple amplifiers, and pH electrode buffers.

Thermopiles generate voltage in response to receiving radiation. These voltages are often only a few microvolts. As a result, the operational amplifier used for this application needs to have low offset voltage, low input voltage noise, and low input bias current. [Figure 56](#) shows a thermopile application where the sensor detects radiation from a distance and generates a voltage that is proportional to the intensity of the radiation. The two resistors, R_A and R_B , are selected to provide high gain to amplify this signal, while C_F removes the high frequency noise.

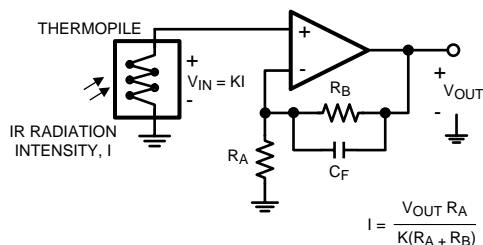


Figure 56. Thermopile Sensor Interface

PRECISION RECTIFIER

Rectifiers are electrical circuits used for converting AC signals to DC signals. Figure 57 shows a full-wave precision rectifier. Each operational amplifier used in this circuit has a diode on its output. This means for the diodes to conduct, the output of the amplifier needs to be positive with respect to ground. If V_{IN} is in its positive half cycle then only the output of the bottom amplifier will be positive. As a result, the diode on the output of the bottom amplifier will conduct and the signal will show at the output of the circuit. If V_{IN} is in its negative half cycle then the output of the top amplifier will be positive, resulting in the diode on the output of the top amplifier conducting and delivering the signal from the amplifier's output to the circuit's output.

For $R_2/R_1 \geq 2$, the resistor values can be found by using the equation shown in Figure 57. If $R_2/R_1 = 1$, then R_3 should be left open, no resistor needed, and R_4 should simply be shorted.

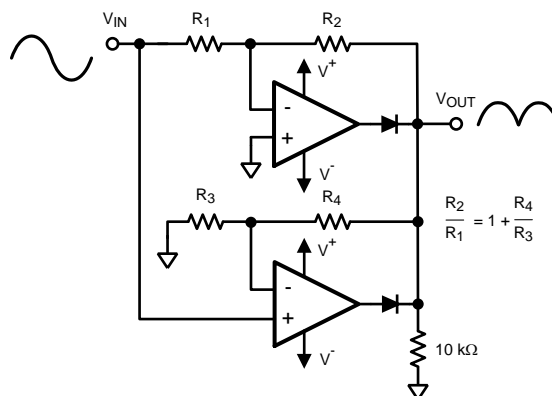


Figure 57. Precision Rectifier

REVISION HISTORY

| Changes from Revision D (March 2013) to Revision E | Page |
|--|--------------------|
| • Changed layout of National Data Sheet to TI format | 18 |

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|----------------------------------|---------------|----------------------|--------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|------------------|---------------------|
| LMP7715MF/NOPB | Active | Production | SOT-23 (DBV) 5 | 1000 SMALL T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | AV3A |
| LMP7715MF/NOPB.A | Active | Production | SOT-23 (DBV) 5 | 1000 SMALL T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | AV3A |
| LMP7715MFE/NOPB | Active | Production | SOT-23 (DBV) 5 | 250 SMALL T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | AV3A |
| LMP7715MFE/NOPB.A | Active | Production | SOT-23 (DBV) 5 | 250 SMALL T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | AV3A |
| LMP7715MFE/NOPB.B | Active | Production | SOT-23 (DBV) 5 | 250 SMALL T&R | - | SN | Level-1-260C-UNLIM | -40 to 125 | AV3A |
| LMP7715MFX/NOPB | Active | Production | SOT-23 (DBV) 5 | 3000 LARGE T&R | Yes | Call TI Sn | Level-1-260C-UNLIM | -40 to 125 | AV3A |
| LMP7715MFX/NOPB.A | Active | Production | SOT-23 (DBV) 5 | 3000 LARGE T&R | Yes | Call TI | Level-1-260C-UNLIM | -40 to 125 | AV3A |
| LMP7715MFX/NOPB.B | Active | Production | SOT-23 (DBV) 5 | 3000 LARGE T&R | - | Call TI | Level-1-260C-UNLIM | -40 to 125 | AV3A |
| LMP7716MM/NOPB | Active | Production | VSSOP (DGK) 8 | 1000 SMALL T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | AX3A |
| LMP7716MM/NOPB.A | Active | Production | VSSOP (DGK) 8 | 1000 SMALL T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | AX3A |
| LMP7716MME/NOPB | Active | Production | VSSOP (DGK) 8 | 250 SMALL T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | AX3A |
| LMP7716MME/NOPB.A | Active | Production | VSSOP (DGK) 8 | 250 SMALL T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | AX3A |
| LMP7716MMX/NOPB | Active | Production | VSSOP (DGK) 8 | 3500 LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | AX3A |
| LMP7716MMX/NOPB.A | Active | Production | VSSOP (DGK) 8 | 3500 LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | AX3A |
| LMP7716Q-MDA.A | Active | Production | DIESALE (Y) 0 | 374 NOT REQUIRED | Yes | Call TI | Level-1-NA-UNLIM | See LMP7716Q-MDA | |
| LMP7716Q-MWA.A | Active | Production | WAFERSALE (YS) 0 | 1 NOT REQUIRED | - | Call TI | Level-1-NA-UNLIM | -40 to 125 | |
| LMP7716QMM/NOPB | Active | Production | VSSOP (DGK) 8 | 1000 SMALL T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | AR5A |
| LMP7716QMM/NOPB.A | Active | Production | VSSOP (DGK) 8 | 1000 SMALL T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | AR5A |
| LMP7716QMME/NOPB | Active | Production | VSSOP (DGK) 8 | 250 SMALL T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | AR5A |
| LMP7716QMME/NOPB.A | Active | Production | VSSOP (DGK) 8 | 250 SMALL T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | AR5A |
| LMP7716QMMX/NOPB | Active | Production | VSSOP (DGK) 8 | 3500 LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | AR5A |
| LMP7716QMMX/NOPB.A | Active | Production | VSSOP (DGK) 8 | 3500 LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | AR5A |
| LMP7716QMMX/NOPB.B | Active | Production | VSSOP (DGK) 8 | 3500 LARGE T&R | - | SN | Level-1-260C-UNLIM | -40 to 125 | AR5A |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LMP7716, LMP7716-Q1 :

● Catalog : [LMP7716](#)

● Automotive : [LMP7716-Q1](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LMP7715MF/NOPB | SOT-23 | DBV | 5 | 1000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LMP7715MFE/NOPB | SOT-23 | DBV | 5 | 250 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LMP7715MFX/NOPB | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LMP7716MM/NOPB | VSSOP | DGK | 8 | 1000 | 177.8 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LMP7716MME/NOPB | VSSOP | DGK | 8 | 250 | 177.8 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LMP7716MMX/NOPB | VSSOP | DGK | 8 | 3500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LMP7716QMM/NOPB | VSSOP | DGK | 8 | 1000 | 177.8 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LMP7716QMME/NOPB | VSSOP | DGK | 8 | 250 | 177.8 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LMP7716QMMX/NOPB | VSSOP | DGK | 8 | 3500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LMP7715MF/NOPB | SOT-23 | DBV | 5 | 1000 | 208.0 | 191.0 | 35.0 |
| LMP7715MFE/NOPB | SOT-23 | DBV | 5 | 250 | 208.0 | 191.0 | 35.0 |
| LMP7715MFX/NOPB | SOT-23 | DBV | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| LMP7716MM/NOPB | VSSOP | DGK | 8 | 1000 | 208.0 | 191.0 | 35.0 |
| LMP7716MME/NOPB | VSSOP | DGK | 8 | 250 | 208.0 | 191.0 | 35.0 |
| LMP7716MMX/NOPB | VSSOP | DGK | 8 | 3500 | 356.0 | 356.0 | 35.0 |
| LMP7716QMM/NOPB | VSSOP | DGK | 8 | 1000 | 208.0 | 191.0 | 35.0 |
| LMP7716QMME/NOPB | VSSOP | DGK | 8 | 250 | 208.0 | 191.0 | 35.0 |
| LMP7716QMMX/NOPB | VSSOP | DGK | 8 | 3500 | 356.0 | 356.0 | 35.0 |

DBV0005A**PACKAGE OUTLINE****SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK0008A**PACKAGE OUTLINE****VSSOP - 1.1 mm max height**

SMALL OUTLINE PACKAGE



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NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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