LMK1C1102, LMK1C1103, LMK1C1104
SNAS791D – DECEMBER 2019 – REVISED FEBRUARY 2022

LMK1C110x 1.8-V, 2.5-V, and 3.3-V LVCMOS Clock Buffer Family

1 Features

- High-performance 1:2, 1:3 or 1:4 LVCMOS clock buffer
- Very low output skew < 50 ps
- Extremely low additive jitter < 50 fs maximum
  - 7.5 fs typical at V_{DD} = 3.3 V
  - 10 fs typical at V_{DD} = 2.5 V
  - 19.2 fs typical at V_{DD} = 1.8 V
- Very low propagation delay < 3 ns
- Synchronous output enable
- Supply voltage: 3.3 V, 2.5 V, or 1.8 V
  - 3.3-V tolerant input at all supply voltages
  - Fail-safe inputs
- f_{max} = 250 MHz for 3.3 V
  f_{max} = 200 MHz for 2.5 V and 1.8 V
- Operating temperature range: –40°C to 125°C
- Available in 8-pin TSSOP package
- Available in 8-pin WSON package

2 Applications

- Factory automation & control
- Telecommunications equipment
- Data center & enterprise computing
- Grid infrastructure
- Motor drives
- Medical imaging

3 Description

The LMK1C110x is a modular, high-performance, low-skew, general-purpose clock buffer family from Texas Instruments. The entire family is designed with a modular approach in mind. Three different fan-out variations, 1:2, 1:3, 1:4, are available.

All of the devices within this family are pin-compatible to each other and backwards compatible to the CDCLVC110x family for easy handling.

All family members share the same high performing characteristics such as low additive jitter, low skew, and wide operating temperature range.

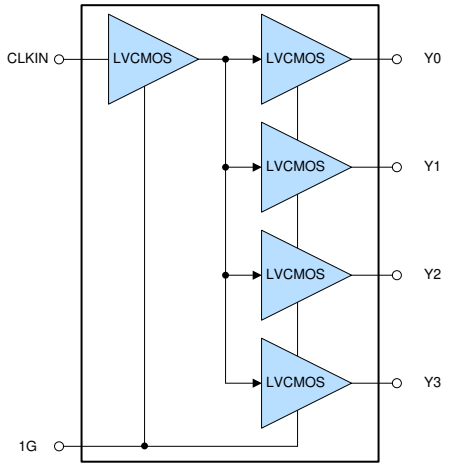
The LMK1C110x supports a synchronous output enable control (1G) which switches the outputs into a low state when 1G is low. These devices have a fail-safe input that prevents oscillation at the outputs in the absence of an input signal and allows for input signals before VDD is supplied.

The LMK1C110x family operates in a 1.8-V, 2.5-V and 3.3-V environment and are characterized for operation from –40°C to 125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMK1C1102	TSSOP (8)	3.00 mm × 4.40 mm
LMK1C1103		
LMK1C1104		
LMK1C1102	WSON (8)	2.00 mm × 2.00 mm
LMK1C1104		

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Functional Block Diagram

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4 Revision History

Changes from Revision C (June 2021) to Revision D (February 2022) **Page**

- Added fail-safe input details to *Description* section....1
- Changed part-to-part skew maximum from 450 ps to 250 ps....6
- Added the *Fail-Safe Inputs* section....10

Changes from Revision B (June 2020) to Revision C (June 2021) **Page**

- Changed text format, numbering format for tables, figures, and cross-references throughout the document....1
- Added LMK1C1102/04 DQF (WSON) package....1
- Added the *Device Comparison* table....3
- Added pinout diagrams for the DQF (WSON) package variant of the LMK1C1102 and LMK1C1104....3
- Added information pertaining to the layout of LMK1C1102/04 WSON package variant....14
- Removed *Related Links* section....15

Changes from Revision A (February 2020) to Revision B (June 2020) **Page**

- Added fan-out variation information to *Description* section....1
- Removed LMK1C1104PW pinout from the first page....1
- Added LMK1C1102 and LMK1C1103 pinout diagrams....3

Changes from Revision * (December 2019) to Revision A (February 2020) **Page**

- Added the LMK1C1102 and LMK1C1103 to the data sheet....1
- Changed the *Power Supply Recommendations* section....13

5 Device Comparison

Table 5-1. Device Comparison

DEVICE	NUMBER OF OUTPUTS	PACKAGE
LMK1C1102	2	TSSOP (8), 3.00 mm x 4.40 mm
LMK1C1103	3	
LMK1C1104	4	
LMK1C1106	6	TSSOP (14), 5.00 mm x 4.40 mm
LMK1C1108	8	TSSOP (16), 5.00 mm x 4.40 mm
LMK1C1102	2	WSON (8), 2.00 mm x 2.00 mm
LMK1C1104	4	

6 Pin Configuration and Functions

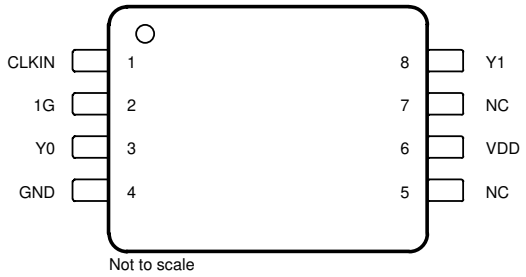
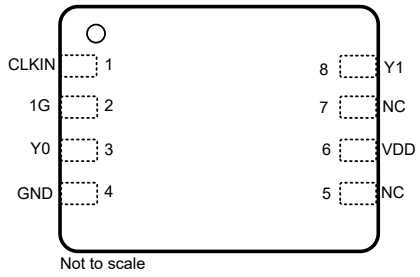


Figure 6-1. LMK1C1102 PW Package 8-Pin TSSOP Top View



1. The DQF (WSON) package is equivalent to the DFN package of other vendors.

Figure 6-2. LMK1C1102 DQF Package 8-Pin WSON Top View

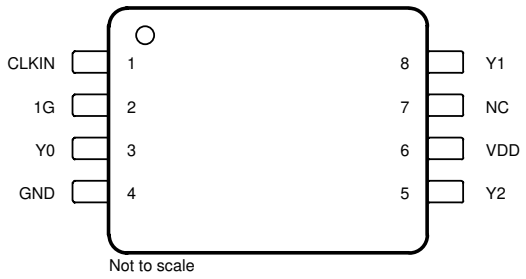


Figure 6-3. LMK1C1103 PW Package 8-Pin TSSOP Top View

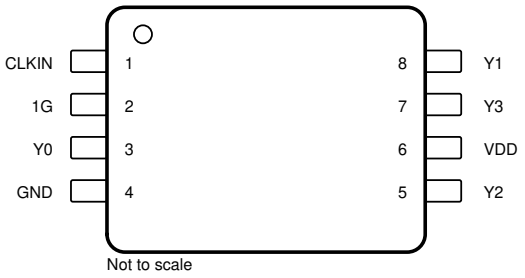
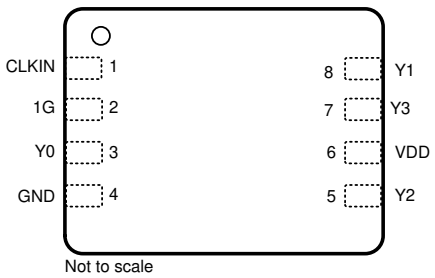


Figure 6-4. LMK1C1104 PW Package 8-Pin TSSOP Top View



1. The DQF (WSON) package is equivalent to the DFN package of other vendors.

Figure 6-5. LMK1C1104 DQF Package 8-Pin WSON Top View

Table 6-1. Pin Functions

PIN				TYPE	DESCRIPTION
NAME	LMK1C1102	LMK1C1103	LMK1C1104		
LVCMOS CLOCK INPUT					
CLKIN	1	1	1	Input	Single-ended clock input with internal 300-kΩ (typical) pulldown resistor to GND. Typically connected to a single-ended clock input.
CLOCK OUTPUT ENABLE					
1G	2	2	2	Input	Global Output Enable with internal 300-kΩ (typical) pulldown resistor to GND. Typically connected to VDD with external pullup resistor. HIGH: outputs enabled LOW: outputs disabled
LVCMOS CLOCK OUTPUT					
Y0	3	3	3	Output	LVCMOS output. Typically connected to a receiver. Unused outputs can be left floating.
Y1	8	8	8		
Y2	—	5	5		
Y3	—	—	7		
SUPPLY VOLTAGE					
VDD	6	6	6	Power	Power supply terminal. Typically connected to a 3.3-V, 2.5-V, or 1.8-V supply. The VDD pin is typically connected to an external 0.1-µF capacitor near the pin.
GROUND					
GND	4	4	4	GND	Power supply ground.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD}	Supply voltage	–0.5	3.6	V
V_{CLKIN}	Input voltage (CLKIN)			
V_{IN}	Input voltage (1G)			
V_{Yn}	Output pins (Yn)	–0.5	V_{DD} + 0.3	
I_{IN}	Input current	–20	20	mA
I_O	Continuous output current	–50	50	mA
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±9000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DD}	Core supply voltage	3.3-V supply	3.135	3.3	3.465	V
		2.5-V supply	2.375	2.5	2.625	
		1.8-V supply	1.71	1.8	1.89	
T_A	Operating free-air temperature		–40		125	°C
T_J	Operating junction temperature		–40		150	°C

7.4 Thermal Information

THERMAL METRIC(1)		LMK1C1104		UNIT
		DQF(WSON)	PW (TSSOP)	
		8 PINS	8 PINS	
R_{qJA}	Junction-to-ambient thermal resistance	163	181.9	°C/W
$R_{qJC(top)}$	Junction-to-case (top) thermal resistance	105.7	76.6	°C/W
R_{qJB}	Junction-to-board thermal resistance	84.2	111.6	°C/W
Y_{JT}	Junction-to-top characterization parameter	16.7	16	°C/W
Y_{JB}	Junction-to-board characterization parameter	83.9	110.1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

VDD = 3.3 V ± 5 %, –40°C ≤ TA ≤ 125°C. Typical values are at VDD = 3.3 V, 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT CONSUMPTION						
I_{DD}	Core supply current, static	All-outputs disabled, f_{IN} = 0 V		25	45	µA
I_{DD}	Core supply current	All-outputs disabled, f_{IN} = 100 MHz		8	15	mA
		All-outputs active, f_{IN} = 100 MHz, C_L = 5pF, V_{DD} = 1.8 V		14	20	
		All-outputs active, f_{IN} = 100 MHz, C_L = 5pF, V_{DD} = 2.5 V		21	30	
		All-outputs active, f_{IN} = 100 MHz, C_L = 5pF, V_{DD} = 3.3 V		33	40	
CLOCK INPUT						
f_{IN_SE}	Input frequency	V_{DD} = 3.3 V	DC		250	MHz
		V_{DD} = 2.5 V and 1.8 V	DC		200	
V_{IH}	Input high voltage		0.7 x V_{DD}			V
V_{IL}	Input low voltage				0.3 x V_{DD}	
dV_{IN}/dt	Input slew rate	20% - 80% of input swing	0.1			V/ns
I_{IN_LEAK}	Input leakage current		–50		50	uA
C_{IN_SE}	Input capacitance	at 25°C		7		pF
CLOCK OUTPUT FOR ALL V_{DD} LEVELS						
f_{OUT}	Output frequency	V_{DD} = 3.3 V			250	MHz
		V_{DD} = 2.5 V and 1.8 V			200	
ODC	Output duty cycle	With 50% duty cycle input (for all VDD)	45		55	%
t_{START}	Start-up time before output is active	See (1)			3	ms
t_{1G_ON}	Output enable time	See (2)			5	cycles
t_{1G_OFF}	Output disable time	See (3)			5	cycles
CLOCK OUTPUT FOR V_{DD} = 3.3 V ± 5%						
V_{OH}	Output high voltage	I_{OH} = 1 mA	2.8			V
V_{OL}	Output low voltage	I_{OL} = 1 mA			0.2	
$t_{RISE-FALL}$	Output rise and fall time	20/80%, C_L= 5 pF, fIN = 156.25 MHz		0.35	0.7	ns
$t_{OUTPUT-SKEW}$	Output-output skew	See (4)		25	50	ps
$t_{PART-SKEW}$	Part-to-part skew				250	
$t_{PROP-DELAY}$	Propagation delay	See (5)		1.5	2	ns
$t_{JITTER-ADD}$	Additive Jitter	f_{IN} = 156.25 MHz, Input slew rate = 2 V/ns, Integration range = 12 kHz - 20 MHz		8	20	fs, RMS
R_{OUT}	Output impedance			50		Ω
CLOCK OUTPUT FOR V_{DD} = 2.5 V ± 5%						
V_{OH}	Output high voltage	I_{OH} = 1 mA	0.8 x V_{DD}			V
V_{OL}	Output low voltage	I_{OL} = 1 mA			0.2 x V_{DD}	
$t_{RISE-FALL}$	Output rise and fall time	20/80%, C_L= 5 pF, f_{IN} = 156.25 MHz		0.33	0.8	ns
$t_{OUTPUT-SKEW}$	Output-output skew	See (4)			50	ps
$t_{PART-SKEW}$	Part-to-part skew				400	
$t_{PROP-DELAY}$	Propagation delay	See (5)		1.5	2.5	ns
$t_{JITTER-ADD}$	Additive Jitter	f_{IN} = 156.25 MHz, Input slew rate = 2 V/ns, Integration range = 12 kHz - 20 MHz		11	27	fs, RMS
R_{OUT}	Output impedance			52.5		Ω

VDD = 3.3 V ± 5 %, –40°C ≤ TA ≤ 125°C. Typical values are at VDD = 3.3 V, 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CLOCK OUTPUT FOR V_{DD} = 1.8 V ± 5%						
V_{OH}	Output high voltage	I_{OH} = 1 mA	0.8 x V_{DD}			V
V_{OL}	Output low voltage	I_{OL} = 1 mA			0.2 x V_{DD}	V
$t_{RISE-FALL}$	Output rise and fall time	20/80%, C_L= 5 pF, f_{IN} = 156.25 MHz		0.38	1	ns
$t_{OUTPUT-SKEW}$	Output-output skew	See (4)			50	ps
$t_{PART-SKEW}$	Part-to-part skew				900	ps
$t_{PROP-DELAY}$	Propagation delay	See (5)		1.5	3	ns
$t_{JITTER-ADD}$	Additive Jitter	f_{IN} = 156.25 MHz, Input slew rate = 2 V/ns, Integration range = 12 kHz - 20 MHz		17.5	50	fs, RMS
R_{OUT}	Output impedance			60		Ω
GENERAL PURPOSE INPUT (1G)						
V_{IH}	High-level input voltage		0.75 x V_{DD}			V
V_{IL}	Low-level input voltage				0.25 x V_{DD}	V
I_{IH}	Input high-level current	V_{IH} = V_{DD_REF}	–50		50	µA
I_{IL}	Input low-level current	V_{IL} = GND	–50		50	µA

(1) Measured from VDD stable to output active, when 1G = HIGH.
(2) Measured from 1G rising edge crossing VIH to first rising edge of Yn.
(3) Measured from 1G falling edge crossing VIL to last falling edge of Yn.
(4) Measured from rising edge of any Yn output to any other Ym output.
(5) Measured from rising edge of CLKIN to any Yn output.

7.6 Timing Requirements

VDD = 3.3 V ± 5 %, –40°C ≤ TA ≤ 125°C

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
V/t_{RAMP}	V_{DD} ramp rate		0.1		50	V/ms

7.7 Typical Characteristics

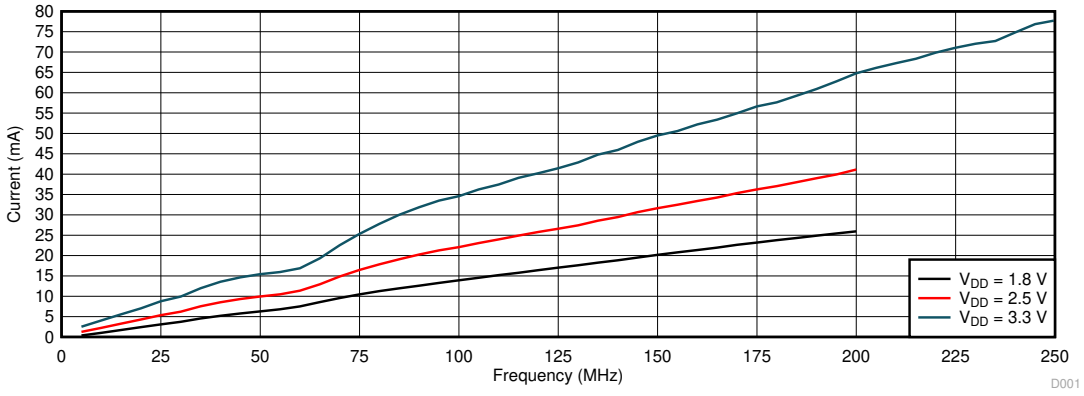


Figure 7-1. Device Power Consumption vs. Clock Frequency (Load 5 pF)

8 Parameter Measurement Information

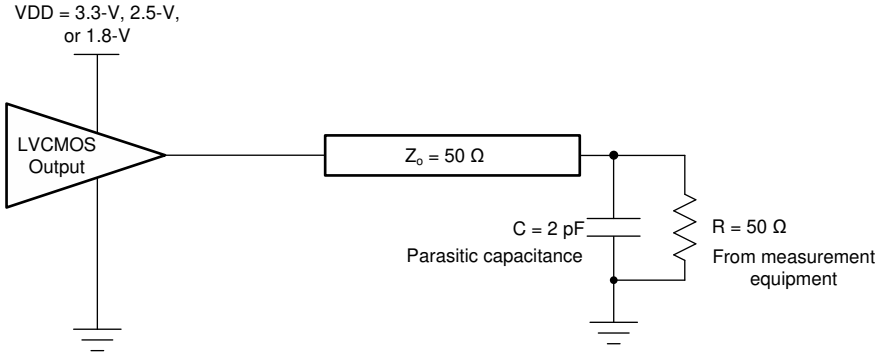


Figure 8-1. Test Load Circuit

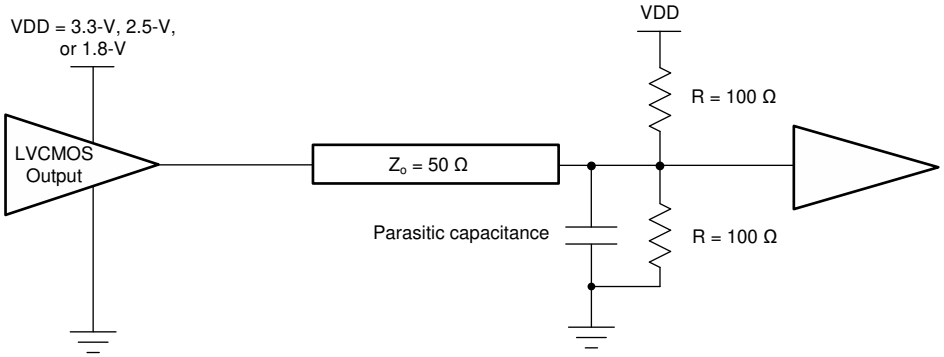


Figure 8-2. Application Load With 50-Ω Termination

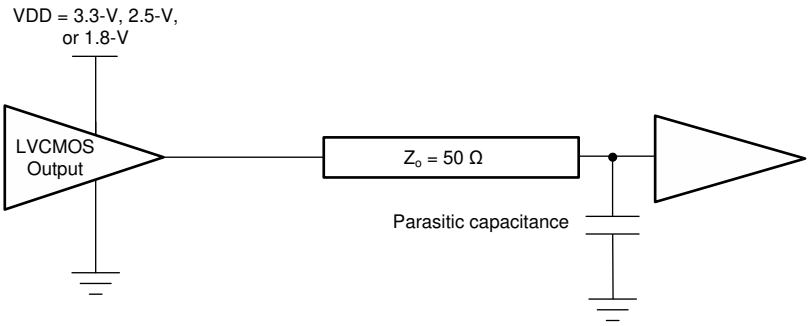


Figure 8-3. Application Load With Termination

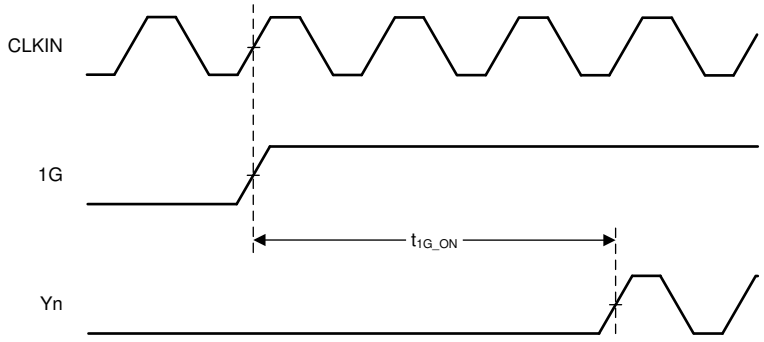


Figure 8-4. t_{1G_ON} Output Enable Time

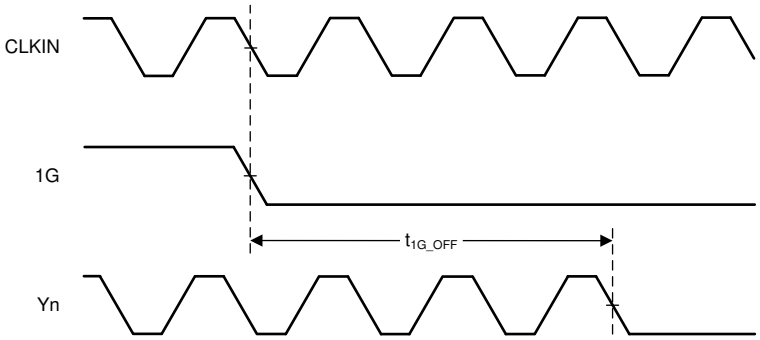


Figure 8-5. t_{1G_OFF} Output Disable Time

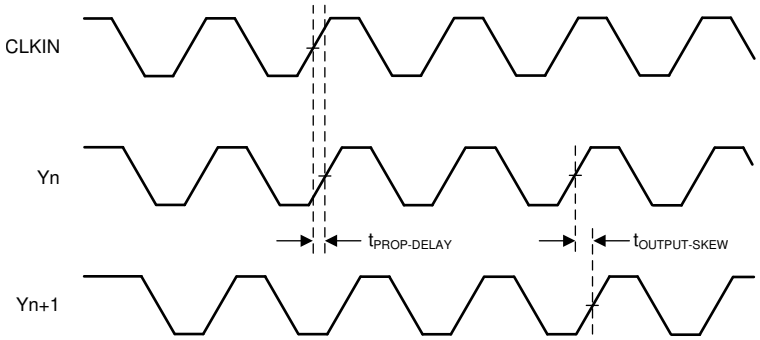


Figure 8-6. Propagation Delay $t_{PROP-DELAY}$ and Output Skew $t_{OUTPUT-SKEW}$

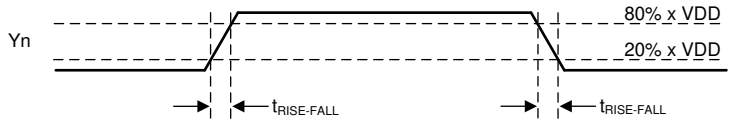


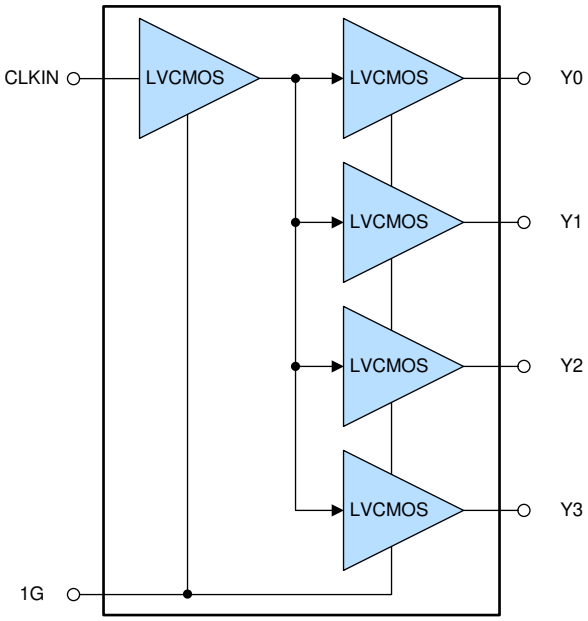
Figure 8-7. Rise and Fall Time $t_{RISE-FALL}$

9 Detailed Description

9.1 Overview

The LMK1C110x family of devices is part of a low-jitter and low-skew LVCMOS fan-out buffer solution. For best signal integrity, it is important to match the characteristic impedance of the LMK1C110x's output driver with that of the transmission line.

9.2 Functional Block Diagram



9.3 Feature Description

The outputs of the LMK1C110x can be disabled by driving the synchronous output enable pin (1G) low. Unused output can be left floating to reduce overall system component cost. Supply and ground pins must be connected to V_{DD} and GND, respectively.

9.3.1 Fail-Safe Inputs

The LMK1C110x family of devices is designed to support fail-safe input operation. This feature allows the user to drive the device inputs before VDD is applied without damaging the device. Refer to *Absolute Maximum Ratings* for more information on the maximum input supported by the device. The device also incorporates an input hysteresis that prevents random oscillation in absence of an input signal, allowing the input pins to be left open.

9.4 Device Functional Modes

The LMK1C110x operates from 1.8-V, 2.5-V, or 3.3-V supplies. Table 9-1 shows the output logics of the LMK1C110x.

Table 9-1. Output Logic Table

INPUTS		OUTPUTS
CLKIN	1G	Yn
X	L	L
L	H	L
H	H	H

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The LMK1C110x family is a low additive jitter LVCMOS buffer solution that can operate up to 250-MHz at V_{DD} = 3.3 V and 200 MHz at V_{DD} = 2.5 V to 1.8 V. Low output skew as well as the ability for synchronous output enable is featured to simultaneously enable or disable buffered clock outputs as necessary in the application.

10.2 Typical Application

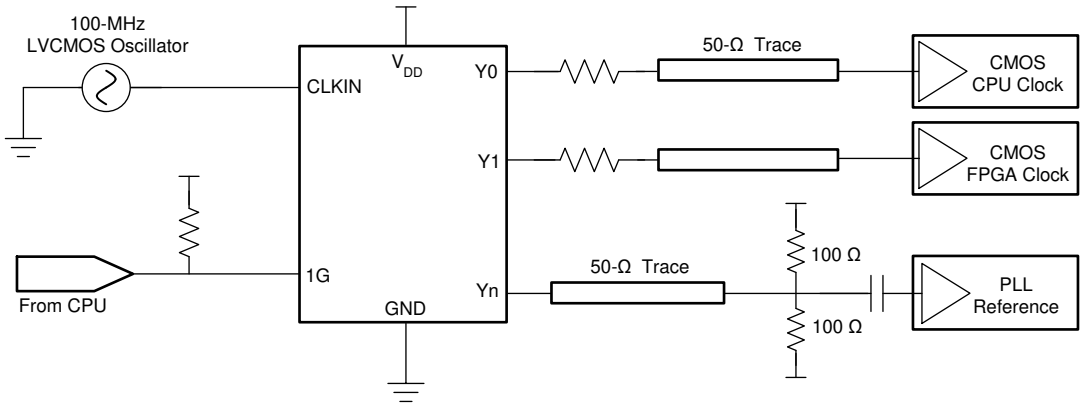


Figure 10-1. System Configuration Example

10.2.1 Design Requirements

The LMK1C110x shown in Figure 10-1 is configured to fan out a 100-MHz signal from a local LVCMOS oscillator. The CPU is configured to control the output state through 1G.

The configuration example is driving three LVCMOS receivers in a backplane application with the following properties:

- The CPU clock can accept a full swing DC-coupled LVCMOS signal. A series resistor is placed near the LMK1C110x to closely match the characteristic impedance of the trace to minimize reflections.
- The FPGA clock is similarly DC-coupled with an appropriate series resistor placed near the LMK1C110x.
- The PLL in this example can accept a lower amplitude signal, so a Thevenin's equivalent termination is used. The PLL receiver features internal biasing, so AC coupling can be used when common-mode voltage is mismatched.

10.2.2 Detailed Design Procedure

Unused outputs can be left floating. See the *Power Supply Recommendations* section for recommended filtering techniques.

10.2.3 Application Curves

The low additive jitter of the LMK1C110x is shown in Figure 10-2.

Figure 10-3 shows the low-noise 156.25-MHz reference source with 25.6-fs RMS jitter driving the LMK1C110x, resulting in 26.7-fs RMS jitter when integrated from 12 kHz to 20 MHz at 3.3-V supply. The resultant additive jitter measured is a low 7.6-fs RMS for this configuration.

Figure 10-4 shows the low-noise 156.25-MHz reference source with 25.6-fs RMS jitter driving the LMK1C110x, resulting in 27.5-fs RMS jitter when integrated from 12 kHz to 20 MHz at 2.5-V supply. The resultant additive jitter measured is a low 10-fs RMS for this configuration.

Figure 10-5 shows the low-noise 156.25-MHz reference source with 25.6-fs RMS jitter driving the LMK1C110x, resulting in 32-fs RMS jitter when integrated from 12 kHz to 20 MHz at 1.8-V supply. The resultant additive jitter measured is a low 19.2-fs RMS for this configuration.

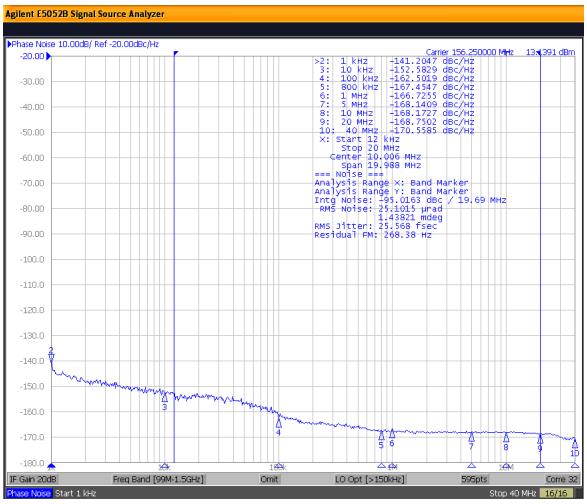


Figure 10-2. LMK1C110x Reference Phase Noise 25.6-fs (12 kHz to 20 MHz)

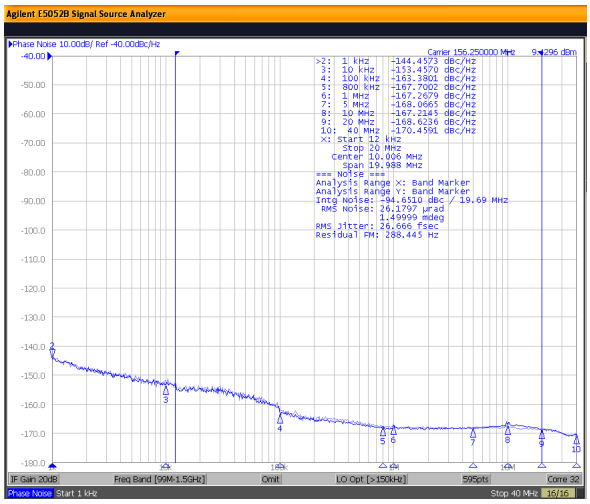


Figure 10-3. LMK1C110x 3.3-V Output Phase Noise 26.7-fs (12 kHz to 20 MHz)

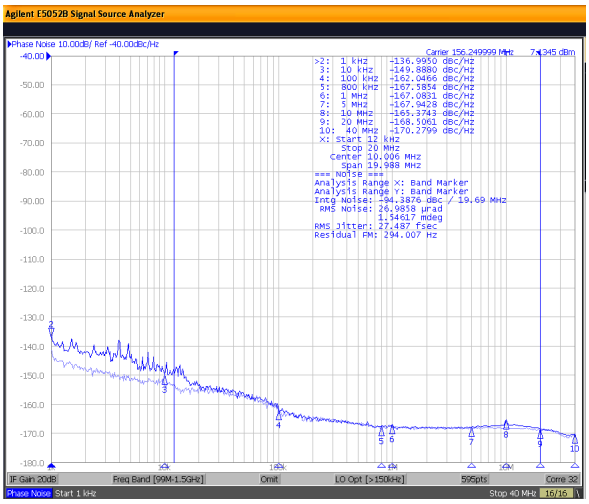


Figure 10-4. LMK1C110x 2.5-V Output Phase Noise 27.5-fs (12 kHz to 20 MHz)

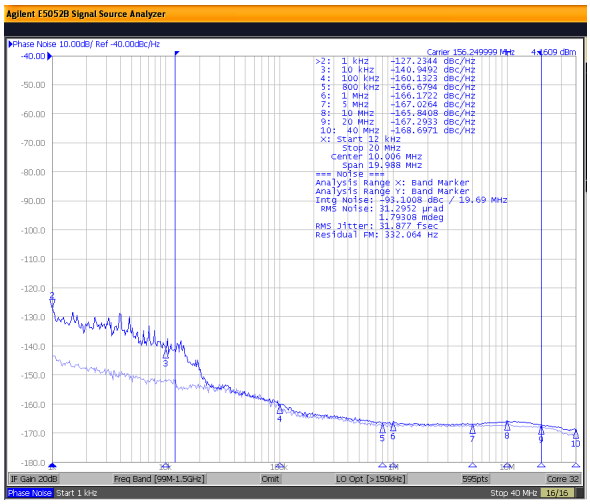


Figure 10-5. LMK1C110x 1.8-V Output Phase Noise 32-fs (12 kHz to 20 MHz)

11 Power Supply Recommendations

High-performance clock buffers can be sensitive to noise on the power supply, which may dramatically increase the additive jitter of the buffer. Thus, it is essential to manage any excessive noise from the system power supply, especially for applications where the jitter and phase noise performance is critical.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the very low impedance path for high-frequency noise and guard the power supply system against induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and should have low equivalent series resistance (ESR). To properly bypass the supply, the decoupling capacitors must be placed very close to the power-supply terminals, be connected directly to the ground plane, and laid out with short loops to minimize inductance. TI recommends adding as many high-frequency (for example, 0.1 µF) bypass capacitors, as there are supply terminals in the package. TI recommends, but does not require, inserting a ferrite bead between the board power supply and the chip power supply that isolates the high-frequency switching noises generated by the clock buffer; these beads prevent the switching noise from leaking into the board supply. It is imperative to choose an appropriate ferrite bead with very low DC resistance to provide adequate isolation between the board supply and the chip supply, as well as to maintain a voltage at the supply terminals that is greater than the minimum voltage required for proper operation.

Figure 11-1 shows this recommended power supply decoupling method.

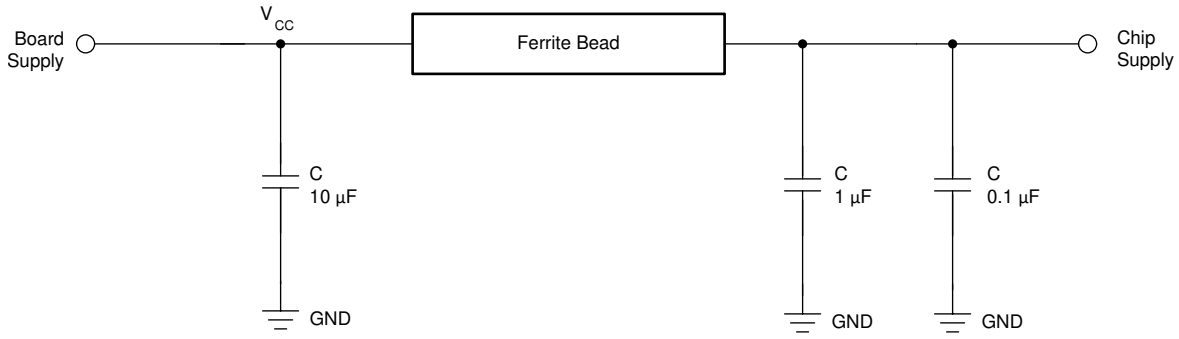


Figure 11-1. Power Supply Decoupling

12 Layout

12.1 Layout Guidelines

Figure 12-1 shows a conceptual layout detailing recommended placement of power supply bypass capacitors. For component side mounting, use 0402 body size capacitors to facilitate signal routing. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low-impedance connection to the ground plane.

Figure 12-2 provides a visual representation of the WSON device; it can be seen from the figure that similar to a DFN package, WSON doesn't have any leads.

12.2 Layout Example

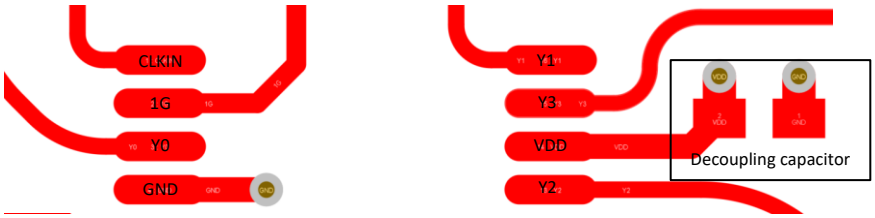


Figure 12-1. PCB Conceptual Layout

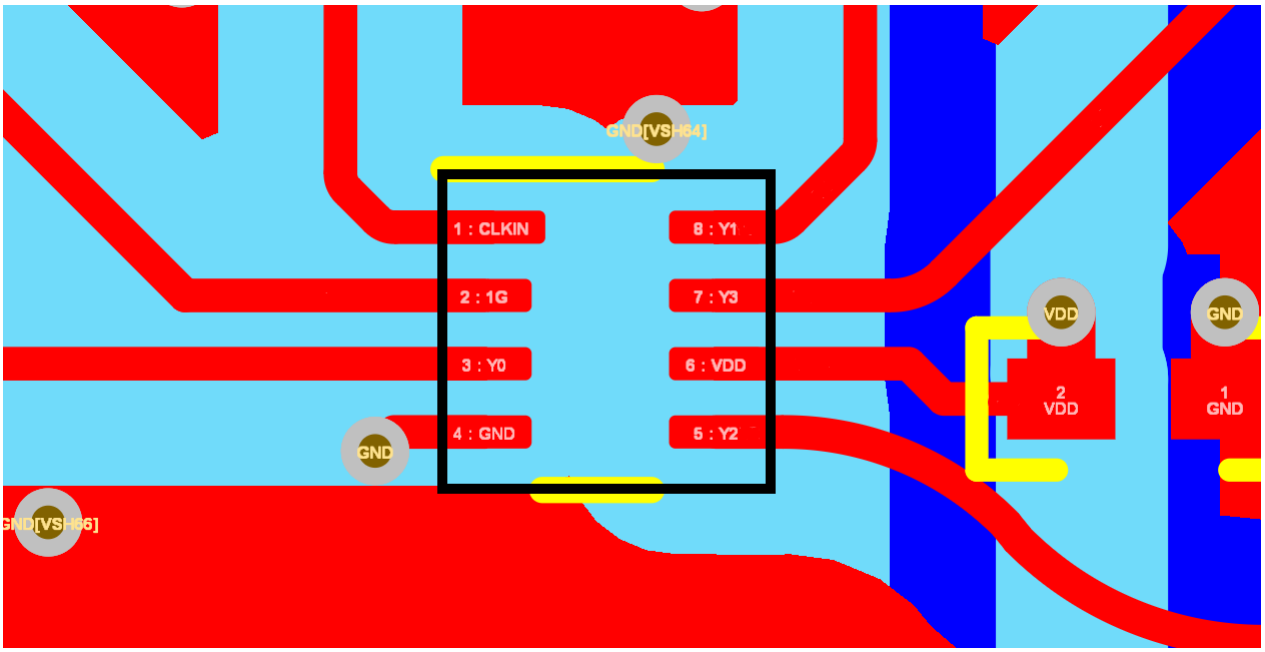


Figure 12-2. Layout illustration for 8-pin WSON device

13 Device and Documentation Support

13.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

13.3 Trademarks

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13.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMK1C1102DQFR	Active	Production	WSON (DQF) | 8	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	L1C2
LMK1C1102DQFR.A	Active	Production	WSON (DQF) | 8	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	L1C2
LMK1C1102DQFT	Active	Production	WSON (DQF) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	L1C2
LMK1C1102DQFT.A	Active	Production	WSON (DQF) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	L1C2
LMK1C1102PWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMK1C2
LMK1C1102PWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMK1C2
LMK1C1102PWRG4	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMK1C2
LMK1C1102PWRG4.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMK1C2
LMK1C1103PWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMK1C3
LMK1C1103PWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMK1C3
LMK1C1103PWRG4	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMK1C3
LMK1C1103PWRG4.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMK1C3
LMK1C1104DQFR	Active	Production	WSON (DQF) | 8	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	L1C4
LMK1C1104DQFR.A	Active	Production	WSON (DQF) | 8	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	L1C4
LMK1C1104DQFT	Active	Production	WSON (DQF) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	L1C4
LMK1C1104DQFT.A	Active	Production	WSON (DQF) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	L1C4
LMK1C1104PWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMK1C4
LMK1C1104PWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMK1C4
LMK1C1104PWRG4	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMK1C4
LMK1C1104PWRG4.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMK1C4

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

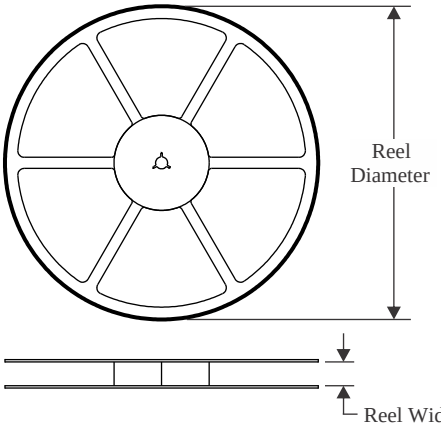
(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

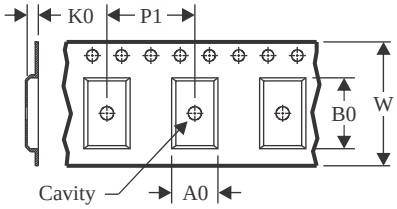
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

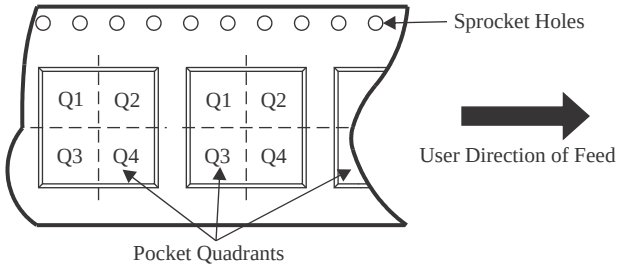


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

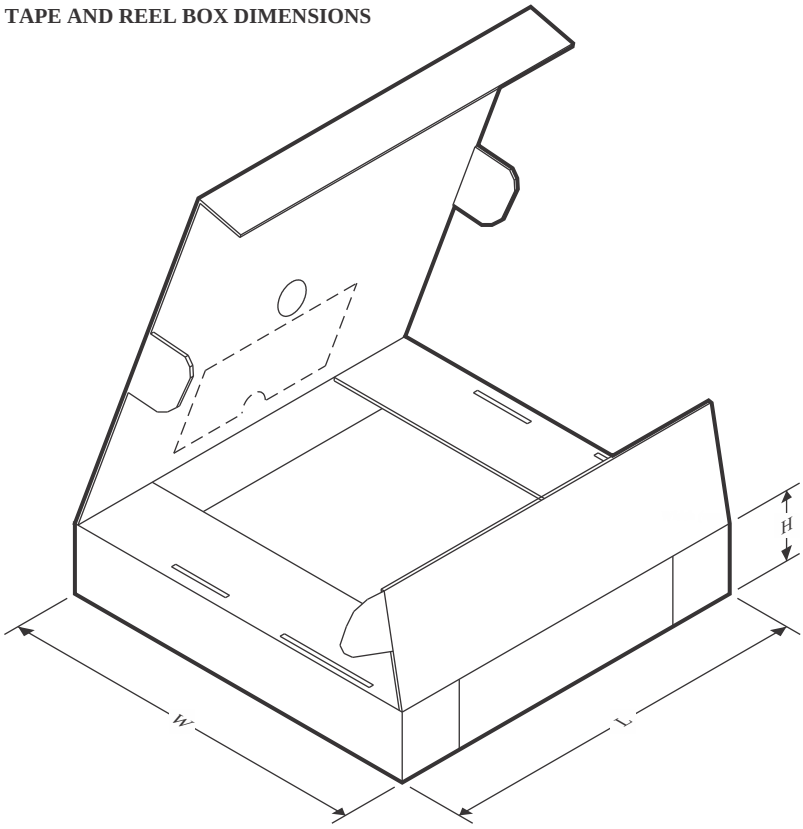
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMK1C1102DQFR	WSON	DQF	8	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
LMK1C1102DQFT	WSON	DQF	8	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
LMK1C1102PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LMK1C1102PWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LMK1C1103PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LMK1C1103PWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LMK1C1104DQFR	WSON	DQF	8	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
LMK1C1104DQFT	WSON	DQF	8	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
LMK1C1104PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LMK1C1104PWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

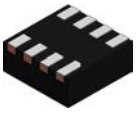


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMK1C1102DQFR	WSON	DQF	8	3000	205.0	200.0	33.0
LMK1C1102DQFT	WSON	DQF	8	250	205.0	200.0	33.0
LMK1C1102PWR	TSSOP	PW	8	2000	353.0	353.0	32.0
LMK1C1102PWRG4	TSSOP	PW	8	2000	353.0	353.0	32.0
LMK1C1103PWR	TSSOP	PW	8	2000	353.0	353.0	32.0
LMK1C1103PWRG4	TSSOP	PW	8	2000	353.0	353.0	32.0
LMK1C1104DQFR	WSON	DQF	8	3000	205.0	200.0	33.0
LMK1C1104DQFT	WSON	DQF	8	250	205.0	200.0	33.0
LMK1C1104PWR	TSSOP	PW	8	2000	353.0	353.0	32.0
LMK1C1104PWRG4	TSSOP	PW	8	2000	353.0	353.0	32.0

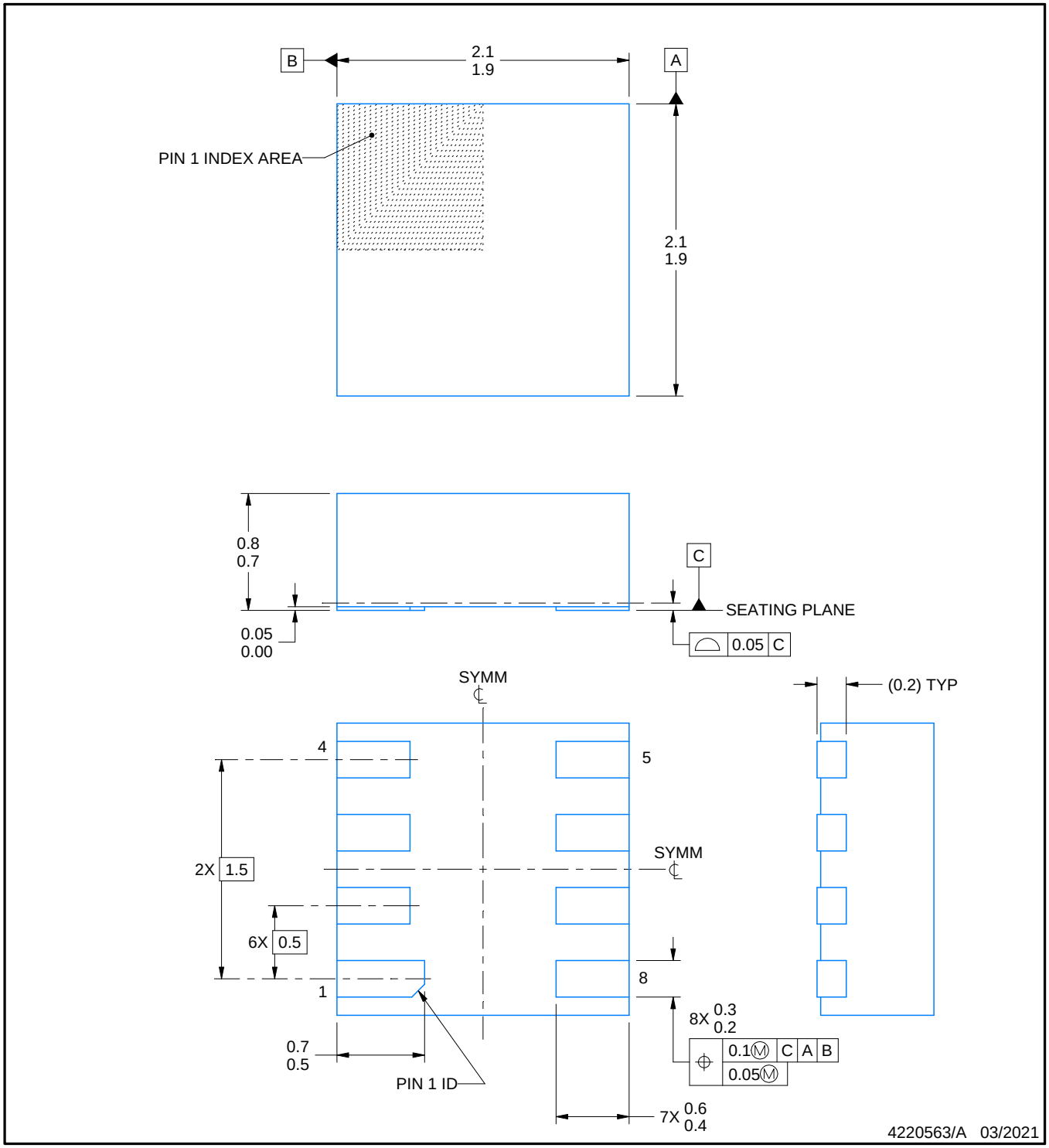
PACKAGE OUTLINE

DQF0008A



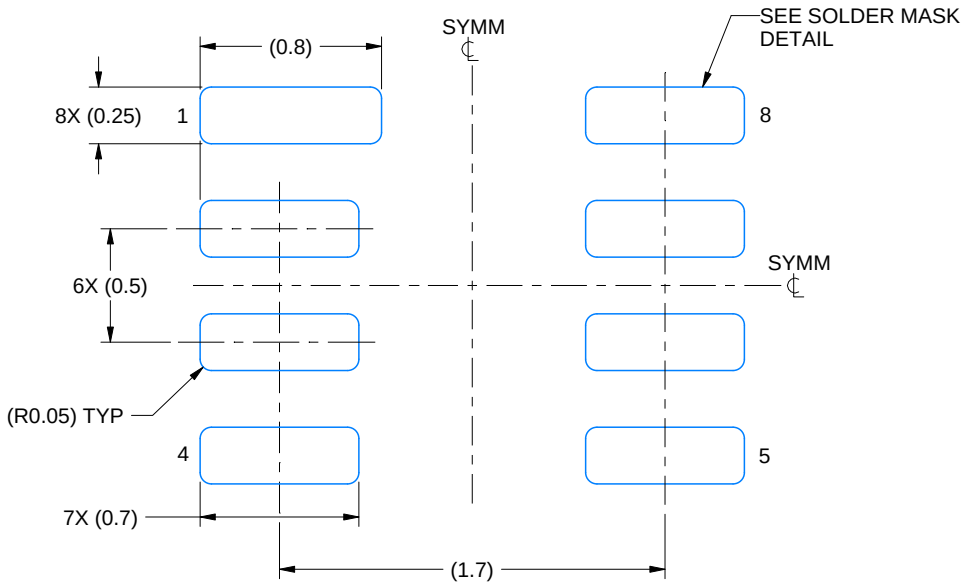
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

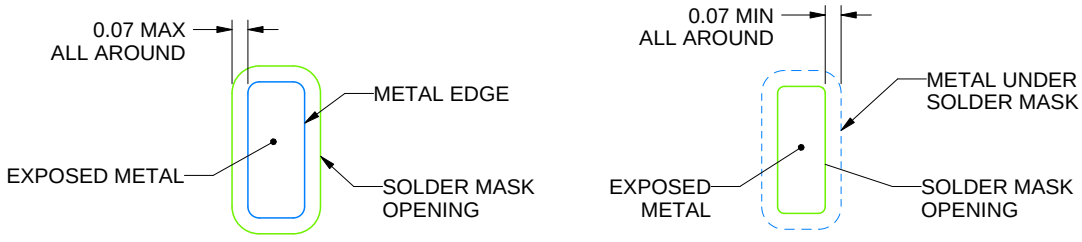


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X



SOLDER MASK DETAILS

4220563/A 03/2021

NOTES: (continued)

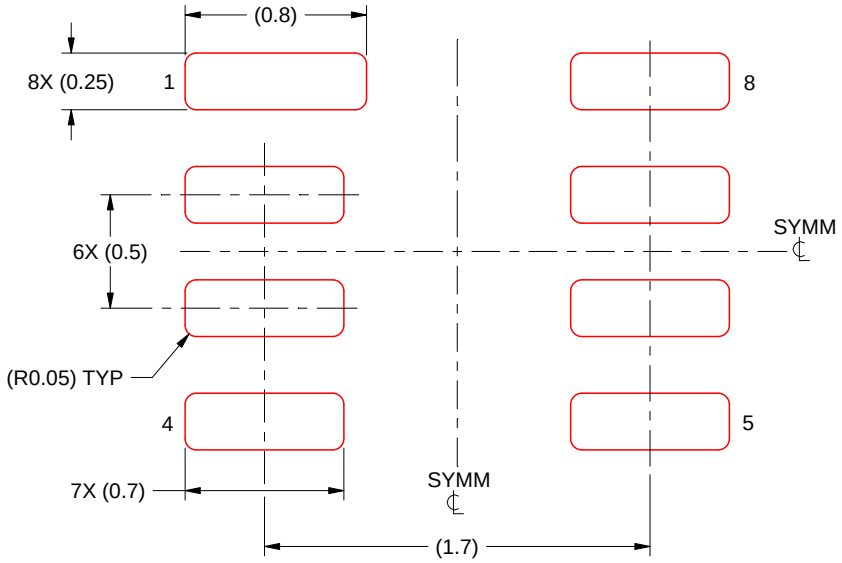
3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DQF0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 30X

4220563/A 03/2021

NOTES: (continued)

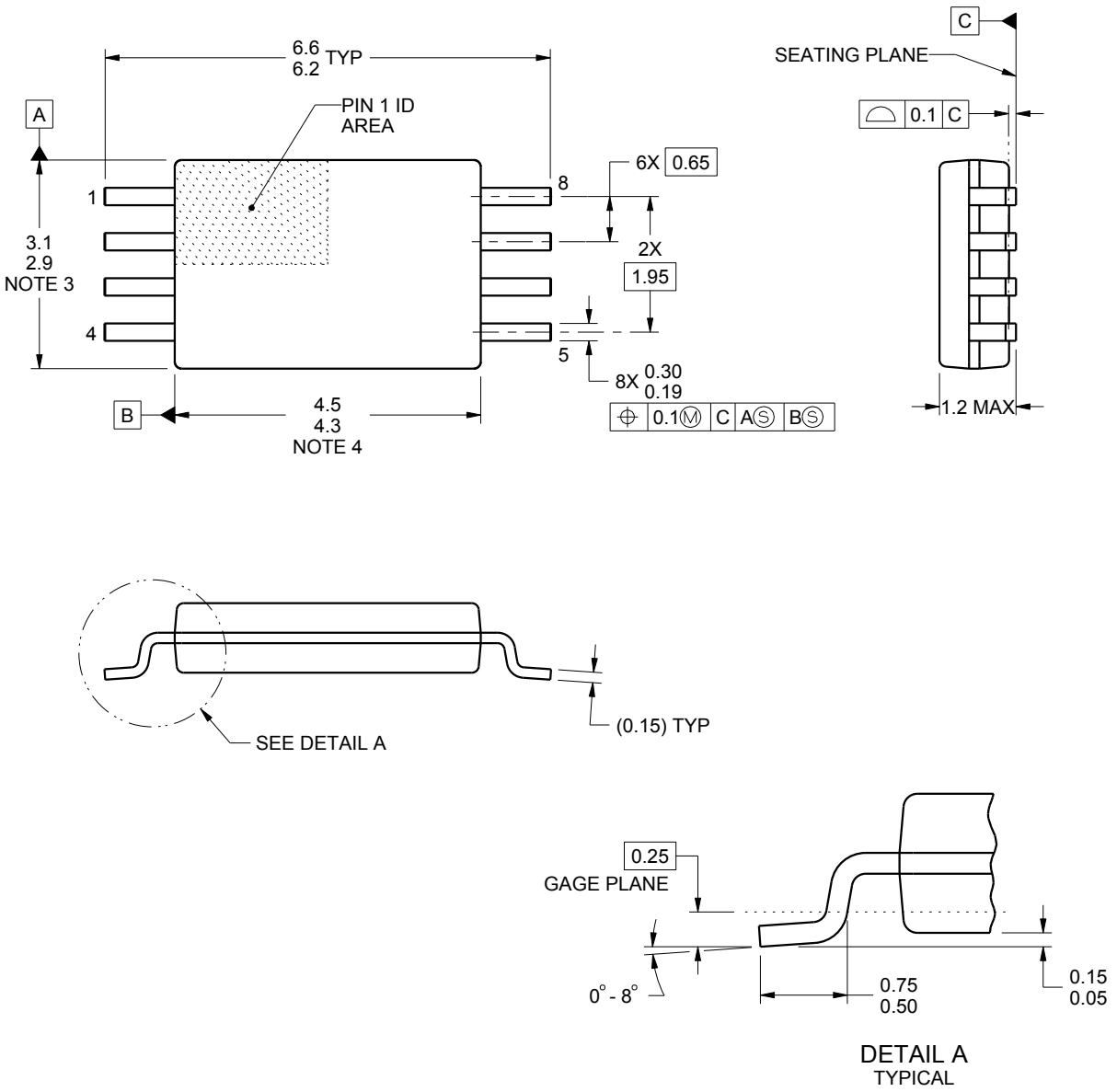
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PW0008A

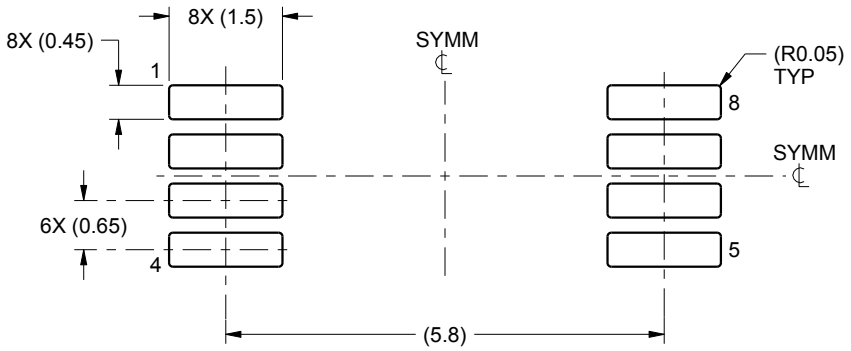
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

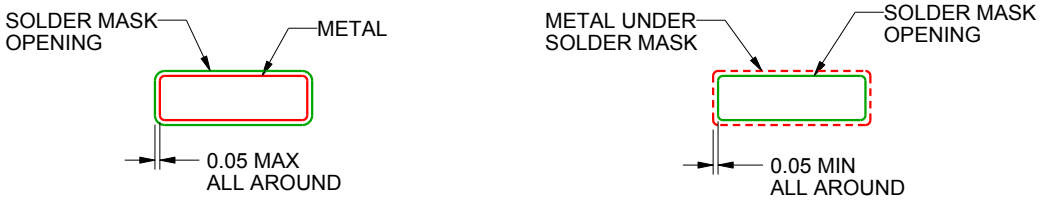


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

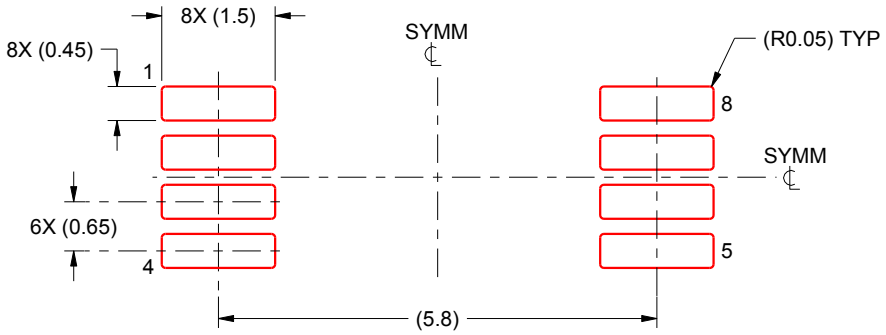


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025