

LMK1C110xA 1.8V, 2.5V, and 3.3V Low Noise Asynchronous LVCMOS Clock Buffer Family

1 Features

- High-performance 1:2, 1:3, 1:4, 1:6 and 1:8 LVCMOS clock buffer
- Very low output skew:
 - LMK1C1102A, LMK1C1103A and LMK1C1104A < 50ps
 - LMK1C1106 and LMK1C1108 < 55ps
- Extremely low additive jitter:
 - LMK1C1102A, LMK1C1103A and LMK1C1104A
 - 7.5fs typical at $V_{DD} = 3.3V$
 - 10fs typical at $V_{DD} = 2.5V$
 - 19.2fs typical at $V_{DD} = 1.8V$
 - LMK1C1106A and LMK1C1108A
 - 12fs typical at $V_{DD} = 3.3V$
 - 15fs typical at $V_{DD} = 2.5V$
 - 28fs typical at $V_{DD} = 1.8V$
- Very low propagation delay < 3ns
- Asynchronous output enable
- Supply voltage: 3.3V, 2.5V, or 1.8V
 - Fail-safe inputs: 3.3V tolerant input at all supply voltages
- $f_{max} = 250MHz$ for 3.3V
- $f_{max} = 200MHz$ for 2.5V or 1.8V
- Operating temperature range: $-40^{\circ}C$ to $125^{\circ}C$

2 Applications

- [Factory automation & control](#)
- [Telecommunications equipment](#)
- [Data center & enterprise computing](#)
- [Grid infrastructure](#)
- 1PPS Applications
- [Motor drives](#)
- [Medical imaging](#)

3 Description

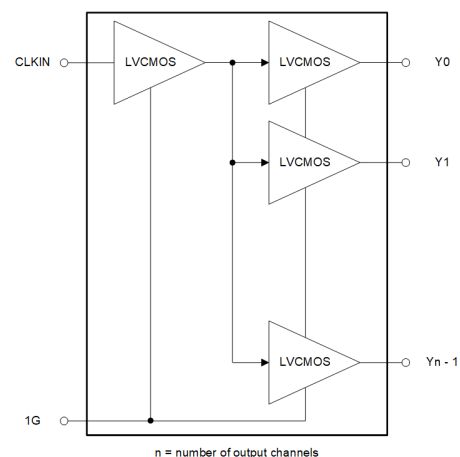
The LMK1C110xA is a modular, high-performance, low-skew, general-purpose clock buffer family from Texas Instruments. The entire family is designed with a modular approach in mind. Five different fan-out variations, 1:2, 1:3, 1:4, 1:6 and 1:8 are available.

All of the devices within this family are pin-compatible to each other and backwards compatible to the CDCLVC110x family for easy handling.

The LMK1C110xA supports a asynchronous output enable control (1G) which switches the outputs into a low state when 1G is low. Asynchronous enable and disable is helpful for 1PPS applications and DC inputs operations. These devices have a fail-safe input that prevents oscillation at the outputs in the absence of an input signal and allows for input signals before VDD is supplied.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
LMK1C1102A	TSSOP (8)	3.00mm × 4.40mm
LMK1C1103A		
LMK1C1104A		
LMK1C1106A	TSSOP (14)	5.00mm × 4.40mm
LMK1C1108A	TSSOP (16)	
LMK1C1102A ⁽³⁾	WSON (8)	2.00mm × 2.00mm
LMK1C1104A ⁽³⁾		



Functional Block Diagram



Table of Contents

1 Features	1	8.4 Device Functional Modes.....	14
2 Applications	1	9 Application and Implementation	15
3 Description	1	9.1 Application Information.....	15
4 Device Comparison	2	9.2 Typical Application.....	15
5 Pin Configuration and Functions	3	9.3 Power Supply Recommendations.....	15
6 Specifications	6	9.4 Layout.....	16
6.1 Absolute Maximum Ratings.....	6	10 Device and Documentation Support	18
6.2 ESD Ratings.....	6	10.1 Documentation Support.....	18
6.3 Recommended Operating Conditions.....	6	10.2 Receiving Notification of Documentation Updates..	18
6.4 Thermal Information.....	6	10.3 Support Resources.....	18
6.5 Electrical Characteristics.....	7	10.4 Trademarks.....	18
6.6 Timing Requirements.....	9	10.5 Electrostatic Discharge Caution.....	18
6.7 Typical Characteristics.....	9	10.6 Glossary.....	18
7 Parameter Measurement Information	11	11 Revision History	18
8 Detailed Description	13	12 Mechanical, Packaging, and Orderable Information	18
8.1 Overview.....	13	12.1 Tape and Reel Information.....	19
8.2 Functional Block Diagram.....	13		
8.3 Feature Description.....	14		

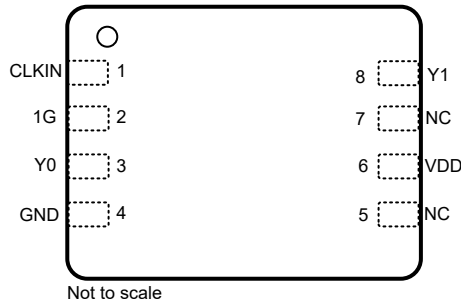
4 Device Comparison

Table 4-1. Device Comparison

DEVICE	Input	Output	Output Enable Option (1G)	PACKAGE
LMK1C1102	1	2	Synchronous	WSO (8), 2.00mm × 2.00mm
LMK1C1104	1	4	Synchronous	WSO (8), 2.00mm × 2.00mm
LMK1C1102	1	2	Synchronous	TSSOP (8), 3.00mm × 4.40mm
LMK1C1103	1	3	Synchronous	TSSOP (8), 3.00mm × 4.40mm
LMK1C1104	1	4	Synchronous	TSSOP (8), 3.00mm × 4.40mm
LMK1C1106	1	6	Synchronous	TSSOP (14), 5.00mm × 4.40mm
LMK1C1108	1	8	Synchronous	TSSOP (16), 5.00mm × 4.40mm
LMK1C1102A	1	2	Asynchronous	WSO (8), 2.00mm × 2.00mm
LMK1C1104A	1	4	Asynchronous	WSO (8), 2.00mm × 2.00mm
LMK1C1102A	1	2	Asynchronous	TSSOP (8), 3.00mm × 4.40mm
LMK1C1103A	1	3	Asynchronous	TSSOP (8), 3.00mm × 4.40mm
LMK1C1104A	1	4	Asynchronous	TSSOP (8), 3.00mm × 4.40mm
LMK1C1106A	1	6	Asynchronous	TSSOP (14), 5.00mm × 4.40mm
LMK1C1108A	1	8	Asynchronous	TSSOP (16), 5.00mm × 4.40mm
LMK1C1102-Q1 ⁽¹⁾	1	2	Synchronous	WSO (8), 2.00mm × 2.00mm
LMK1C1104-Q1 ⁽¹⁾	1	4	Synchronous	WSO (8), 2.00mm × 2.00mm
LMK1C1102-Q1 ⁽¹⁾	1	2	Synchronous	TSSOP (8), 3.00mm × 4.40mm
LMK1C1103-Q1 ⁽¹⁾	1	3	Synchronous	TSSOP (8), 3.00mm × 4.40mm
LMK1C1104-Q1 ⁽¹⁾	1	4	Synchronous	TSSOP (8), 3.00mm × 4.40mm
LMK1C1106-Q1 ⁽¹⁾	1	6	Synchronous	TSSOP (14), 5.00mm × 4.40mm
LMK1C1108-Q1 ⁽¹⁾	1	8	Synchronous	TSSOP (16), 5.00mm × 4.40mm

(1) Preview Only. Contact TI for more information on the device.

5 Pin Configuration and Functions



1. The DQF (WSO) package is equivalent to the DFN package of other vendors.

Figure 5-1. LMK1C1102A, 8-Pin DQF WSON Package (Top View)

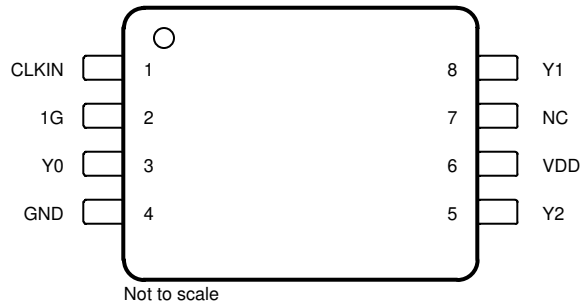


Figure 5-3. LMK1C1103A, 8-Pin PW TSSOP Package (Top View)

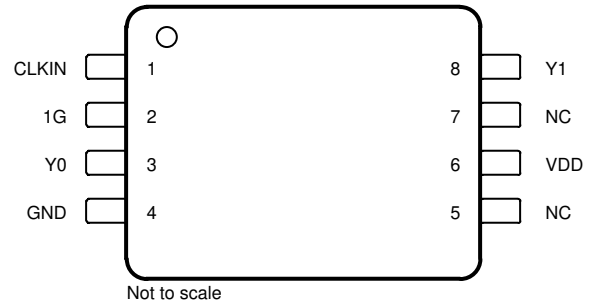
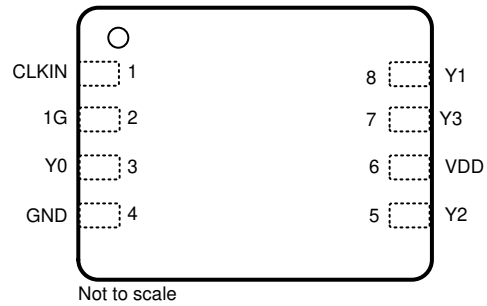


Figure 5-2. LMK1C1102A, 8-Pin PW TSSOP Package (Top View)



1. The DQF (WSO) package is equivalent to the DFN package of other vendors.

Figure 5-4. LMK1C1104A, 8-Pin DQF WSON Package (Top View)

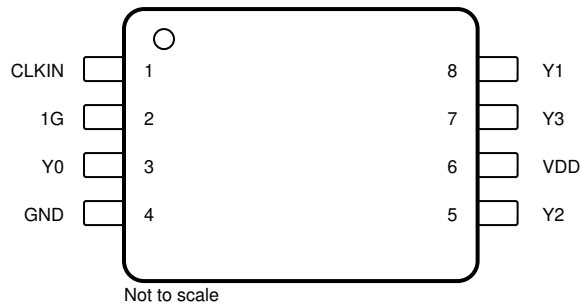


Figure 5-5. LMK1C1104A, 8-Pin PW TSSOP Package (Top View)

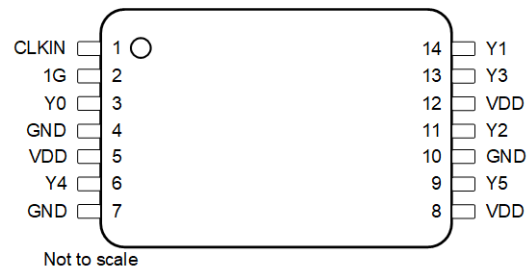


Figure 5-6. LMK1C1106A, 14-Pin PW TSSOP Package (Top View)



Figure 5-7. LMK1C1108A, 16-Pin PW TSSOP Package (Top View)

Table 5-1. Pin Functions

PIN						TYPE	DESCRIPTION
NAME	LMK1C 1102A	LMK1C 1103A	LMK1C 1104A	LMK1C 1106A	LMK1C 1108A		
LVCMOS CLOCK INPUT							
CLKIN	1	1	1	1	1	Input	Single-ended clock input with internal 300-kΩ (typical) pulldown resistor to GND. Typically connected to a single-ended clock input.
CLOCK OUTPUT ENABLE							
1G	2	2	2	2	2	Input	Global Output Enable with internal 300-kΩ (typical) pulldown resistor to GND. Typically connected to VDD with external pullup resistor. HIGH: outputs enabled LOW: outputs disabled
LVCMOS CLOCK OUTPUT							
Y0	3	3	3	3	3	Output	LVCMOS output. Typically connected to a receiver. Unused outputs can be left floating.
Y1	8	8	8	14	16		
Y2	—	5	5	11	13		
Y3	—	—	7	13	15		
Y4	—	—	—	6	6		
Y5	—	—	—	9	11		
Y6	—	—	—	—	8		
Y7	—	—	—	—	9		
SUPPLY VOLTAGE							
VDD	6	6	6	5	5	Power	Power supply terminal. Typically connected to a 3.3-V, 2.5-V, or 1.8-V supply. The VDD pin is typically connected to an external 0.1-μF capacitor near the pin.
				8	10		
				12	14		
GROUND							
GND	4	4	4	4	4	GND	Power supply ground.
				7	7		
				10	12		

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{DD}	Supply voltage	-0.5	3.6	V
V _{CLKIN}	Input voltage (CLKIN)			
V _{IN}	Input voltage (1G)			
V _{Yn}	Output pins (Yn)	-0.5	V _{DD} + 0.3	
I _{IN}	Input current	-20	20	mA
I _O	Continuous output current	-50	50	mA
T _{stg}	Storage temperature	-65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins ⁽¹⁾	±9000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V _{DD}	Core supply voltage	3.3-V supply	3.135	3.3	3.465	V
V _{DD}	Core supply voltage	2.5-V supply	2.375	2.5	2.625	V
V _{DD}	Core supply voltage	1.8-V supply	1.71	1.8	1.89	V
T _A	Operating free-air temperature		-40		125	°C
T _J	Operating junction temperature		-40		150	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LMK1C1102A LMK1C1103A LMK1C1104A		LMK1C1106A	LMK1C1108A	UNIT
		DQF(WSON)	PW (TSSOP)	PW (TSSOP)	PW (TSSOP)	
		8 PINS	8 PINS	14 PINS	16 PINS	
R _{qJA}	Junction-to-ambient thermal resistance	163	181.9	114.4	123.4	°C/W
R _{qJC(top)}	Junction-to-case (top) thermal resistance	105.7	76.6	45.2	53.1	°C/W
R _{qJB}	Junction-to-board thermal resistance	84.2	111.6	60.6	66.4	°C/W
Y _{JT}	Junction-to-top characterization parameter	16.7	16	5.9	8.9	°C/W

THERMAL METRIC ⁽¹⁾		LMK1C1102A LMK1C1103A LMK1C1104A		LMK1C1106A	LMK1C1108A	UNIT
		DQF(WSON)	PW (TSSOP)	PW (TSSOP)	PW (TSSOP)	
		8 PINS	8 PINS	14 PINS	16 PINS	
Y _{JB}	Junction-to-board characterization parameter	83.9	110.1	60	65.8	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

V_{DD} = 3.3V ± 5 %, –40°C ≤ TA ≤ 125°C. Typical values are at V_{DD} = 3.3V, 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
CURRENT CONSUMPTION							
I _{DD}	Core supply current, static	All-outputs disabled, f _{IN} = 0V		25	45	μA	
I _{DD}	Core supply current	All-outputs disabled, f _{IN} = 100MHz		8	15	mA	
		All-outputs active, f _{IN} = 100MHz, C _L = 5pF, V _{DD} = 1.8V		14	20		
		All-outputs active, f _{IN} = 100MHz, C _L = 5pF, V _{DD} = 2.5V		21	30		
		All-outputs active, f _{IN} = 100MHz, C _L = 5pF, V _{DD} = 3.3V		33	40		
CLOCK INPUT							
f _{IN_SE}	Input frequency	V _{DD} = 3.3V	DC		250	MHz	
		V _{DD} = 2.5V and 1.8V	DC		200		
V _{IH}	Input high voltage		0.7 x V _{DD}			V	
V _{IL}	Input low voltage		0.3 x V _{DD}				
dV _{IN} /dt	Input slew rate	20% - 80% of input swing	0.1			V/ns	
I _{IN_LEAK}	Input leakage current		–50			50	uA
C _{IN_SE}	Input capacitance	at 25°C	7			pF	
CLOCK OUTPUT FOR ALL V _{DD} LEVELS							
f _{OUT}	Output frequency	V _{DD} = 3.3V			250	MHz	
		V _{DD} = 2.5V and 1.8V			200		
ODC	Output duty cycle	With 50% duty cycle input (for all VDD)	45		55	%	
t _{1G_ON}	Output enable time	V _{DD} = 3.3V, Asynchronous version only, See (1)			6	ns	
t _{1G_ON}	Output enable time	V _{DD} = 2.5V, Asynchronous version only, See (1)			8	ns	
t _{1G_ON}	Output enable time	V _{DD} = 1.8V, Asynchronous version only, See (1)			10	ns	
t _{1G_OFF}	Output disable time	V _{DD} = 3.3, Asynchronous version only, See (2)			6	ns	
t _{1G_OFF}	Output disable time	V _{DD} = 2.5V, Asynchronous version only, See (2)			8	ns	
t _{1G_OFF}	Output disable time	V _{DD} = 1.8V, Asynchronous version only, See (2)			10.5	ns	
CLOCK OUTPUT FOR V _{DD} = 3.3V ± 5%							
V _{OH}	Output high voltage	I _{OH} = 1mA	2.8			V	
V _{OL}	Output low voltage	I _{OL} = 1mA	0.2				
t _{RISE-FALL}	Output rise and fall time	20/80%, C _L = 5pF, f _{IN} = 156.25MHz	0.35			0.7	ns

LMK1C1102A, LMK1C1103A, LMK1C1104A, LMK1C1106A, LMK1C1108A

SNAS947 – MAY 2025

VDD = 3.3V ± 5 %, –40°C ≤ TA ≤ 125°C. Typical values are at VDD = 3.3V, 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{OUTPUT-SKEW}	Output-output skew	LMK1C1102A, LMK1C1103A, LMK1C1104A. See (3)		25	50	ps
t _{OUTPUT-SKEW}	Output-output skew	LMK1C1106A, LMK1C1108A. See (3)		25	50	ps
t _{PART-SKEW}	Part-to-part skew	LMK1C1102A, LMK1C1103A, LMK1C1104A			250	ps
t _{PART-SKEW}	Part-to-part skew	LMK1C1106A, LMK1C1108A			280	ps
t _{PROP-DELAY}	Propagation delay	LMK1C1102A, LMK1C1103A, LMK1C1104A. See (4)		1.5	2	ns
t _{PROP-DELAY}	Propagation delay	LMK1C1106A, LMK1C1108A. See (4)		1.5	2.2	ns
t _{JITTER-ADD}	Additive Jitter	f _{IN} = 156.25MHz, Input slew rate = 2V/ns, Integration range = 12kHz - 20MHz		8	20	fs, RMS
R _{OUT}	Output impedance			50		Ω
CLOCK OUTPUT FOR V _{DD} = 2.5V ± 5%						
V _{OH}	Output high voltage	I _{OH} = 1mA	0.8 x V _{DD}			V
V _{OL}	Output low voltage	I _{OL} = 1mA	0.2 x V _{DD}			
t _{RISE-FALL}	Output rise and fall time	20/80%, C _L = 5pF, f _{IN} = 156.25MHz		0.33	0.8	ns
t _{OUTPUT-SKEW}	Output-output skew	LMK1C1102A, LMK1C1103A, LMK1C1104A. See (3)			50	ps
t _{OUTPUT-SKEW}	Output-output skew	LMK1C1106A, LMK1C1108A. See (3)			55	ps
t _{PART-SKEW}	Part-to-part skew	LMK1C1102A, LMK1C1103A, LMK1C1104A			400	ps
t _{PART-SKEW}	Part-to-part skew	LMK1C1106A, LMK1C1108A			450	ps
t _{PROP-DELAY}	Propagation delay	LMK1C1102A, LMK1C1103A, LMK1C1104A. See (4)		1.5	2.5	ns
t _{PROP-DELAY}	Propagation delay	LMK1C1106A, LMK1C1108A. See (4)		1.5	2.5	ns
t _{JITTER-ADD}	Additive Jitter	f _{IN} = 156.25MHz, Input slew rate = 2V/ns, Integration range = 12kHz - 20MHz		11	27	fs, RMS
R _{OUT}	Output impedance			52.5		Ω
CLOCK OUTPUT FOR V _{DD} = 1.8V ± 5%						
V _{OH}	Output high voltage	I _{OH} = 1 mA	0.8 x V _{DD}			V
V _{OL}	Output low voltage	I _{OL} = 1 mA	0.2 x V _{DD}			
t _{RISE-FALL}	Output rise and fall time	20/80%, C _L = 5 pF, f _{IN} = 156.25MHz		0.38	1	ns
t _{OUTPUT-SKEW}	Output-output skew	LMK1C1102A, LMK1C1103A, LMK1C1104A. See (3)			50	ps
t _{OUTPUT-SKEW}	Output-output skew	LMK1C1106A, LMK1C1108A. See (3)			55	ps
t _{PART-SKEW}	Part-to-part skew	LMK1C1102A, LMK1C1103A, LMK1C1104A			900	ps
t _{PART-SKEW}	Part-to-part skew	LMK1C1106A, LMK1C1108A			930	ps
t _{PROP-DELAY}	Propagation delay	LMK1C1102A, LMK1C1103A, LMK1C1104A. See (4)		1.5	3	ns
t _{PROP-DELAY}	Propagation delay	LMK1C1106A, LMK1C1108A. See (4)		1.5	3	ns
t _{JITTER-ADD}	Additive Jitter	f _{IN} = 156.25MHz, Input slew rate = 2V/ns, Integration range = 12kHz - 20MHz		17.5	50	fs, RMS
R _{OUT}	Output impedance			60		Ω
GENERAL PURPOSE INPUT (1G)						

VDD = 3.3V ± 5 %, –40°C ≤ TA ≤ 125°C. Typical values are at VDD = 3.3V, 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIH	High-level input voltage		0.75 x VDD			V
VIL	Low-level input voltage	LMK1C1102A, LMK1C1103A, LMK1C1104A			0.38 x VDD	
VIL	Low-level input voltage	LMK1C1106A, LMK1C1108A			0.25 x VDD	
IIH	Input high-level current	VIH = VDD_REF	–50		50	μA
IIL	Input low-level current	VIL = GND	–50		50	

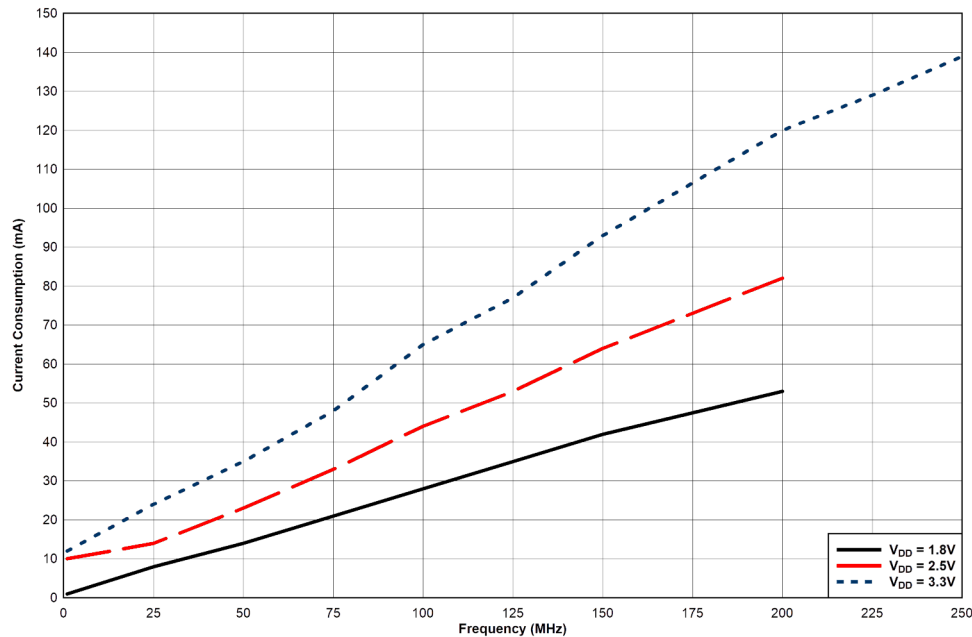
- (1) Measured from 1G rising edge crossing VIH to first rising edge of Yn.
- (2) Measured from 1G falling edge crossing VIL to last falling edge of Yn.
- (3) Measured from rising edge of any Yn output to any other Ym output.
- (4) Measured from rising edge of CLKIN to any Yn output.

6.6 Timing Requirements

VDD = 3.3 V ± 5 %, –40°C ≤ TA ≤ 125°C

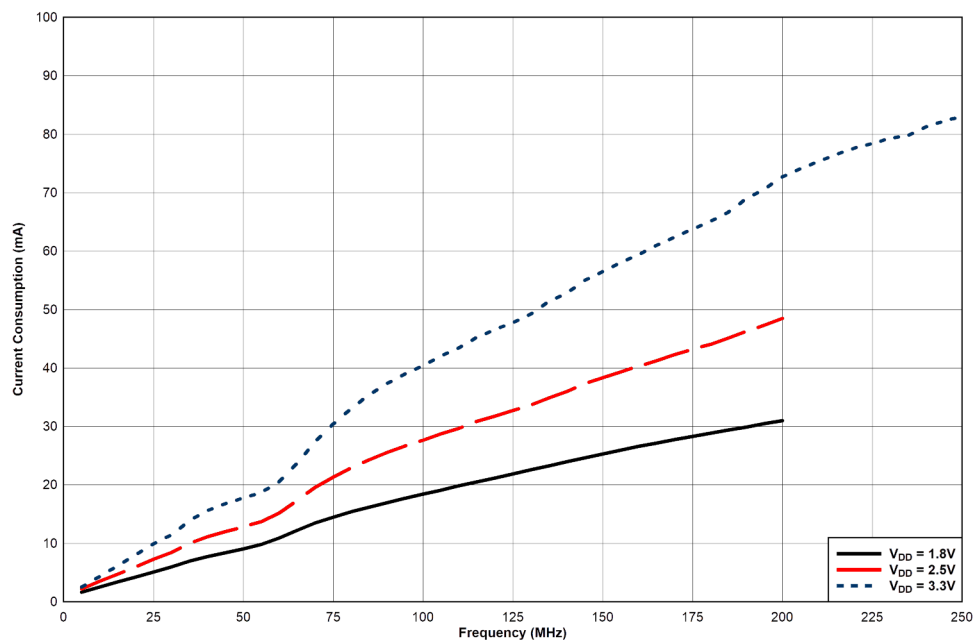
		MIN	NOM	MAX	UNIT
POWER SUPPLY					
V/tRAMP	VDD ramp rate	0.1		50	V/ms

6.7 Typical Characteristics



1. All outputs enabled.

LMK1C1106A and LMK1C1108A Device Power Consumption vs. Clock Frequency (Load 5 pF)



1. All outputs enabled.

Figure 6-1. LMK1C1102A, LMK1C1103A and LMK1C1104A Device Power Consumption vs. Clock Frequency (Load 5 pF)

7 Parameter Measurement Information

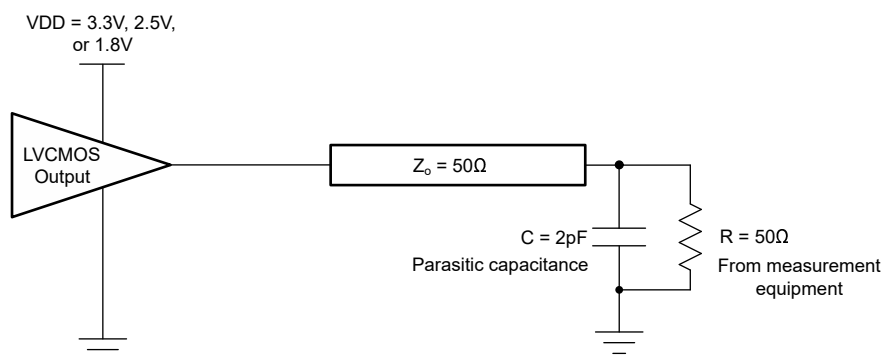


Figure 7-1. Test Load Circuit

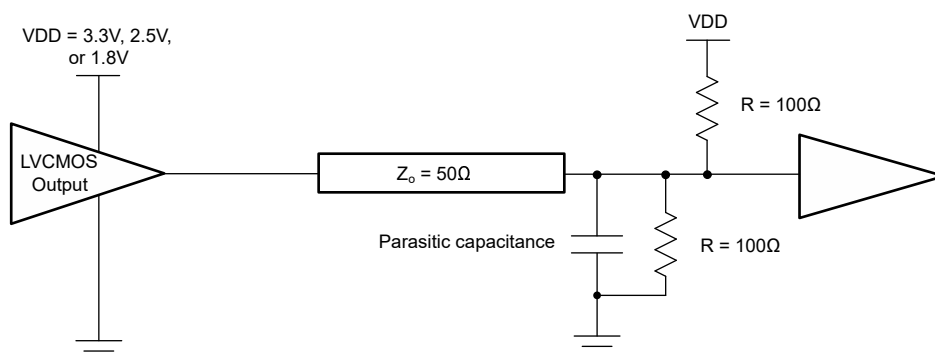


Figure 7-2. Application Load With 50-Ω Termination

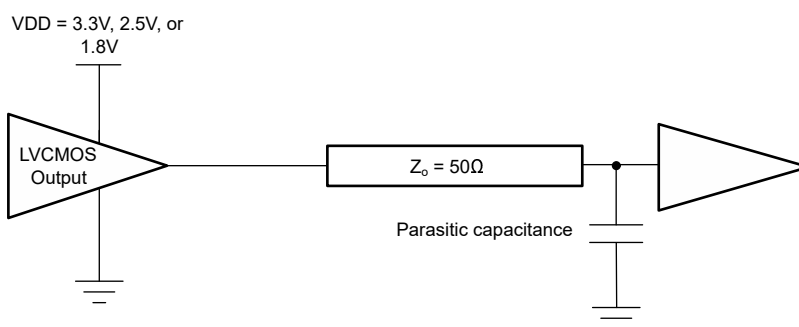


Figure 7-3. Application Load With Termination

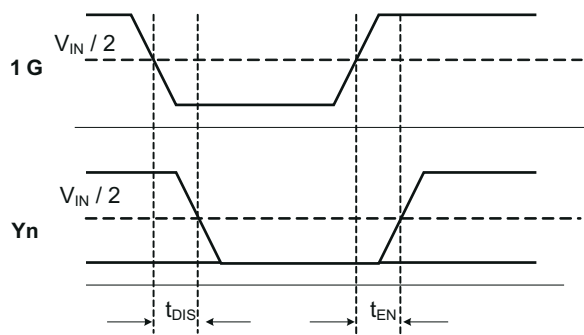


Figure 7-4. Output t_{1G_ON} and t_{1G_OFF} Time

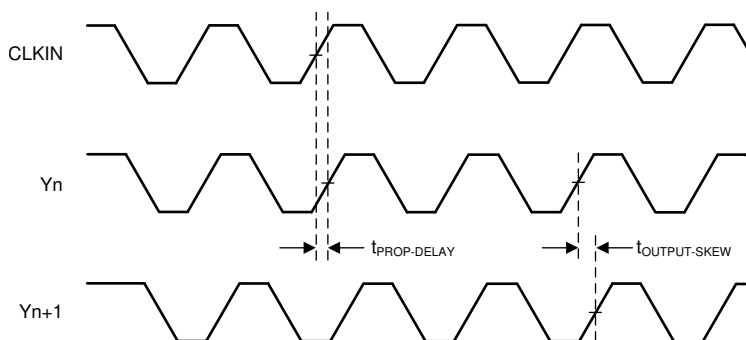


Figure 7-5. Propagation Delay $t_{\text{PROP-DELAY}}$ and Output Skew $t_{\text{OUTPUT-SKEW}}$

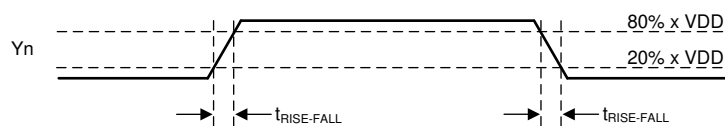


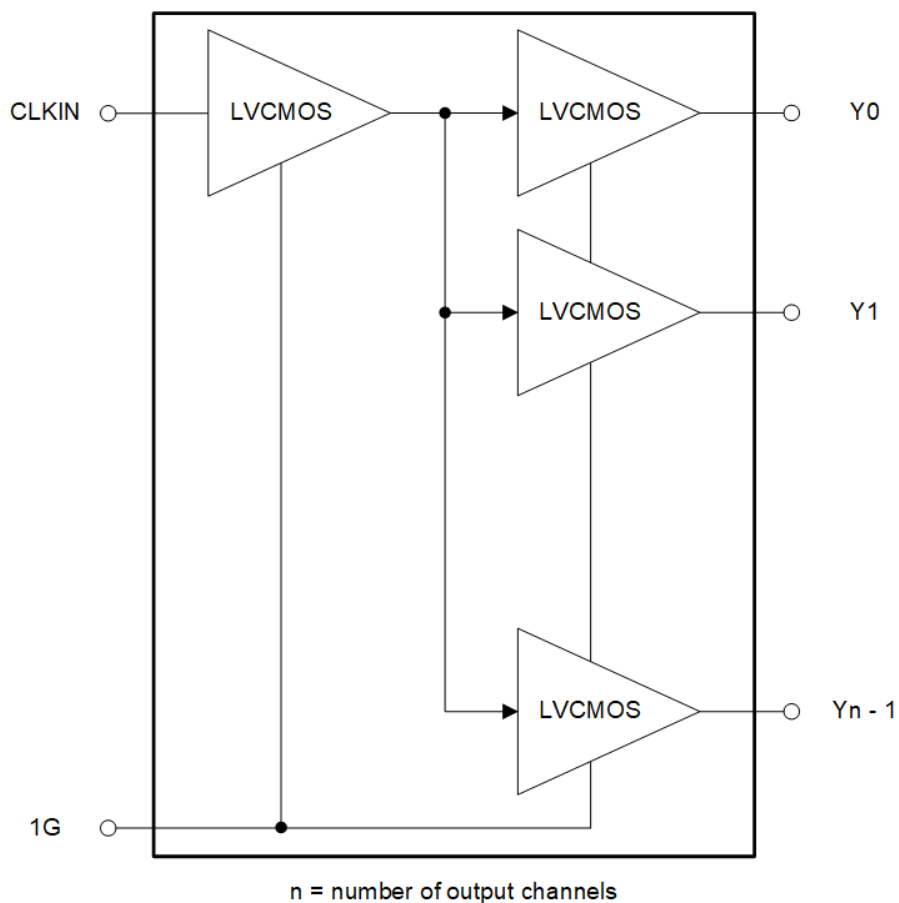
Figure 7-6. Rise and Fall Time $t_{\text{RISE-FALL}}$

8 Detailed Description

8.1 Overview

The LMK1C110xA family of devices is part of a low-jitter and low-skew LVCMOS fan-out buffer solution. Matching the characteristic impedance of the LMK1C110xA output driver with the characteristic impedance of the transmission driver is important for the best signal integrity.

8.2 Functional Block Diagram



8.3 Feature Description

The outputs of the LMK1C110xA can be disabled by driving the asynchronous output enable pin (1G) low. Unused output can be left floating to reduce overall system component cost. Supply and ground pins must be connected to V_{DD} and GND, respectively.

8.3.1 Fail-Safe Inputs

The LMK1C110xA family of devices is designed to support fail-safe input operation. This feature allows the user to drive the device inputs before VDD is applied without damaging the device. Refer to *Absolute Maximum Ratings* for more information on the maximum input supported by the device. The device also incorporates an input hysteresis that prevents random oscillation in absence of an input signal, allowing the input pins to be left open.

8.3.2 Asynchronous Output Enable

Asynchronous output enable immediately turns on the output when 1G pin is pulled high with minimum delay specified in [Section 6](#) compared to synchronous enable which relies on the input clock cycle to synchronize the outputs before enabling.

Asynchronous output enable is useful in applications like 1PPS where fast output enable is necessary. With 1G pin assertion, outputs are activated immediately compared to synchronous output enable. This feature is also useful for other SYNC signal applications where extra delay is unwanted.

Another useful feature for asynchronous output is using static "High" or "Low" signal during power up. Asynchronous output enable devices are not bound with input clock edges so if the clock input is static "High" the outputs follow the input and go "High" during power up. See [Section 4](#) for available output enable options from TI.

8.4 Device Functional Modes

The LMK1C110xA operates from 1.8-V, 2.5-V, or 3.3-V supplies. [Table 8-1](#) shows the output logic of the LMK1C110xA.

Table 8-1. Output Logic Table

INPUTS		OUTPUTS
CLKIN	1G	Yn
X	L	L
L	H	L
H	H	H

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The LMK1C110xA family is a low additive jitter LVCMOS buffer design that can operate up to 250MHz at $V_{DD} = 3.3V$ and 200MHz at $V_{DD} = 2.5V, 1.8V$. Low output skew as well as the ability for asynchronous output enable is featured to simultaneously enable or disable buffered clock outputs as necessary in the application.

9.2 Typical Application

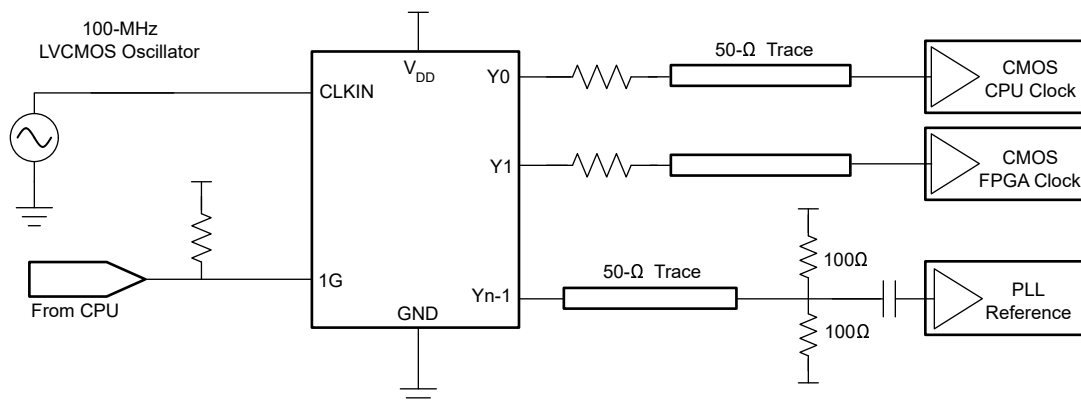


Figure 9-1. System Configuration Example

9.2.1 Design Requirements

The LMK1C110xA shown in [Figure 9-1](#) is configured to fan out a 100-MHz signal from a local LVCMOS oscillator. The CPU is configured to control the output state through 1G.

The configuration example is driving three LVCMOS receivers in a backplane application with the following properties:

- The CPU clock can accept a full swing DC-coupled LVCMOS signal. A series resistor R_S is placed near the LMK1C110xA to closely match the characteristic impedance of the trace to minimize reflections.
- The FPGA clock is similarly DC-coupled with an appropriate series resistor placed near the LMK1C110xA.
- The PLL in this example can accept a lower amplitude signal, so a Thevenin's equivalent termination (pull up to V_{DD} and pull down to GND) is used. The PLL receiver features internal biasing, so AC coupling can be used when common-mode voltage is mismatched.

9.2.2 Detailed Design Procedure

Unused outputs can be left floating. See [Power Supply Recommendations](#) for recommended filtering techniques.

9.3 Power Supply Recommendations

High-performance clock buffers can be sensitive to noise on the power supply, which can dramatically increase the additive jitter of the buffer. Thus, managing any excessive noise from the system power supply is essential, especially for applications where the jitter and phase noise performance is critical.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the very low impedance path for high-frequency noise and guard the power supply system against induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by

the device and must have low equivalent series resistance (ESR). To properly bypass the supply, the decoupling capacitors must be placed very close to the power-supply terminals, be connected directly to the ground plane, and laid out with short loops to minimize inductance. TI recommends adding as many high-frequency (for example, 0.1 μF) bypass capacitors, as there are supply terminals in the package. TI recommends, but does not require, inserting a ferrite bead between the board power supply and the chip power supply that isolates the high-frequency switching noises generated by the clock buffer; these beads prevent the switching noise from leaking into the board supply. Select an appropriate ferrite bead with very low DC resistance to provide adequate isolation between the board supply and the chip supply, as well as to maintain a voltage at the supply terminals that is greater than the minimum voltage required for proper operation.

Figure 9-2 shows this recommended power supply decoupling method.

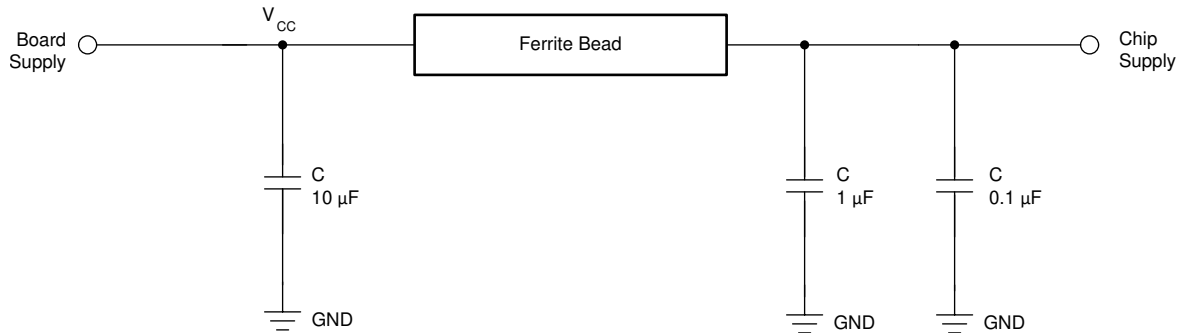


Figure 9-2. Power Supply Decoupling

9.4 Layout

9.4.1 Layout Guidelines

Figure 9-3 shows a conceptual layout detailing recommended placement of power supply bypass capacitors. For component side mounting, use 0402 body size capacitors to facilitate signal routing. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low-impedance connection to the ground plane.

9.4.2 Layout Example

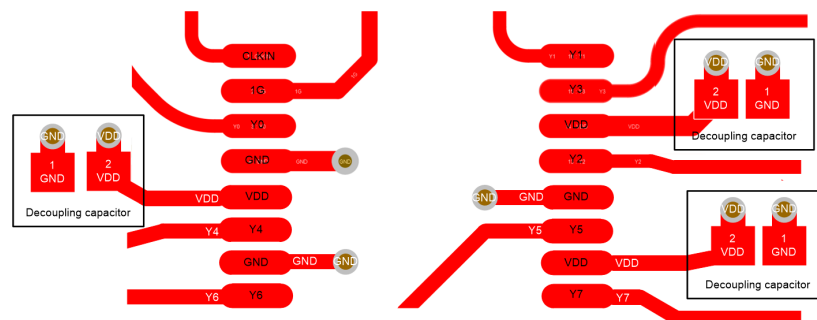


Figure 9-3. Layout Example for 14-Pin and 16-Pin PW Device

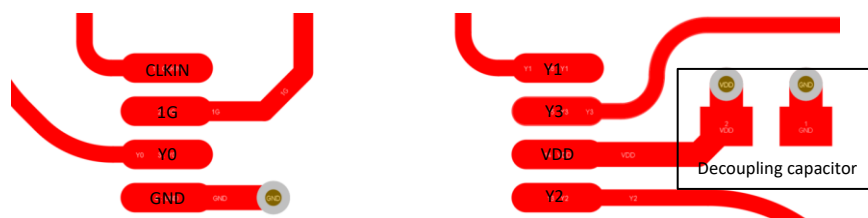


Figure 9-4. Layout Example for 8-Pin PW Device

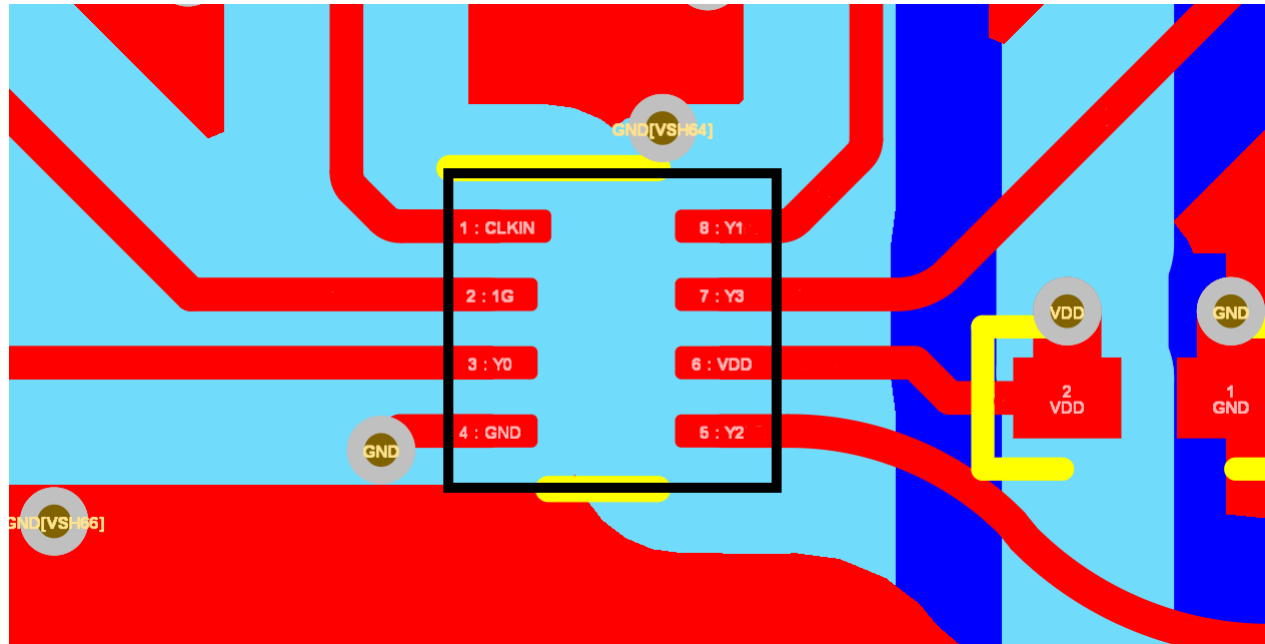


Figure 9-5. Layout Example for 8-Pin WSON Device

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [LMK1C1108EVM](#), EVM user's guide

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

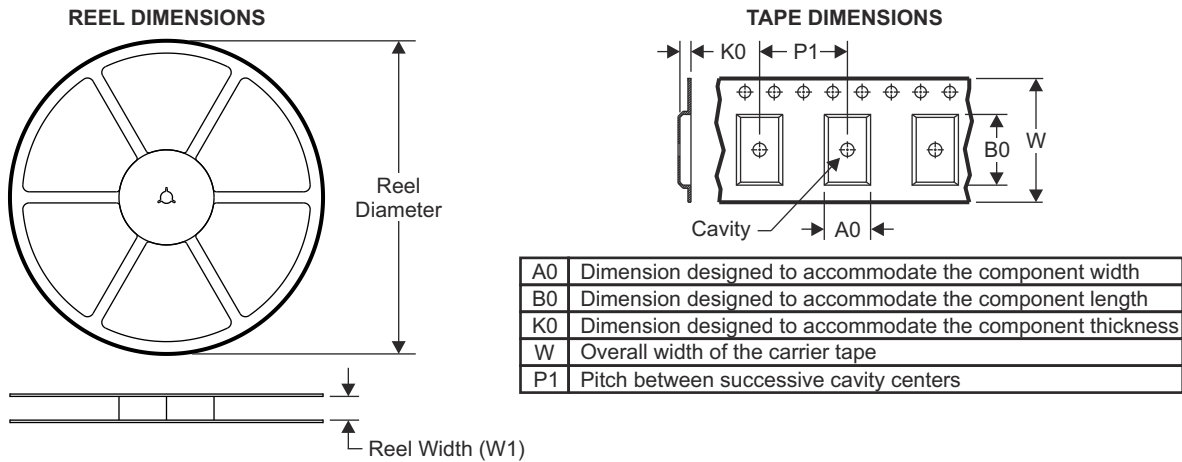
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2025	*	Initial Release

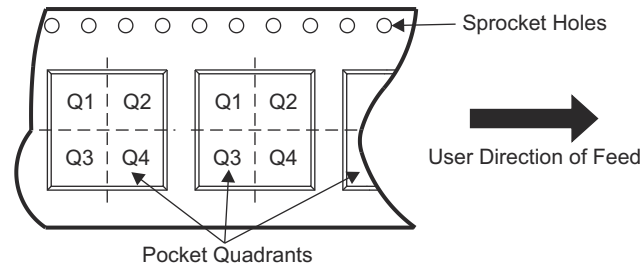
12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Tape and Reel Information

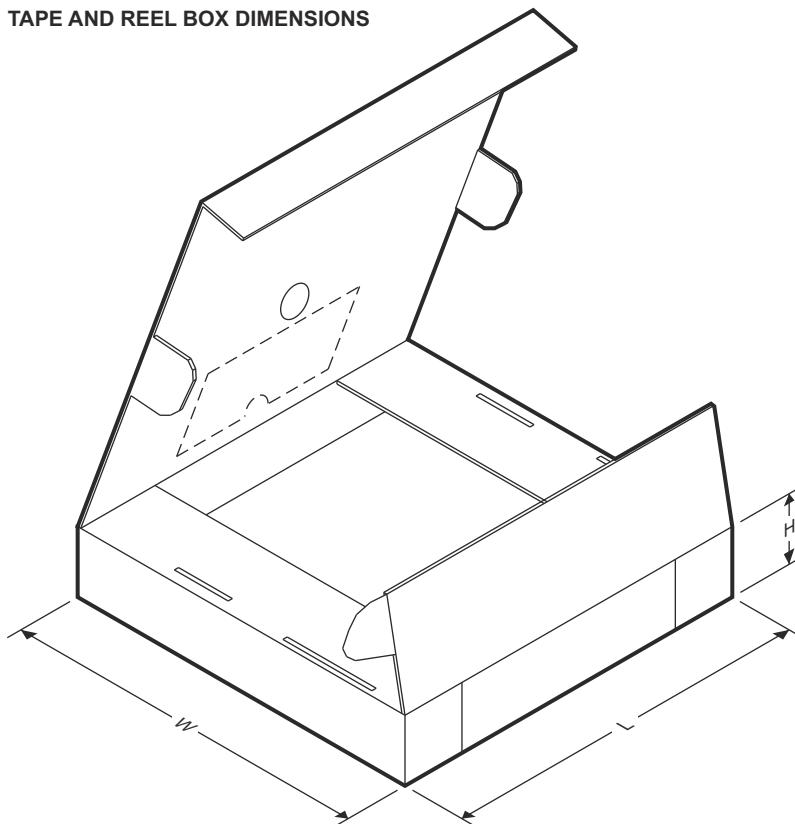


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMK1C1102APWR	TSSOP	PW	8	3000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LMK1C1103APWR	TSSOP	PW	8	3000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LMK1C1104APWR	TSSOP	PW	8	3000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LMK1C1106APWR	TSSOP	PW	14	3000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LMK1C1108APWR	TSSOP	PW	16	3000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LMK1C1102ADQFR	WSOP	DQF	8	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
LMK1C1104ADQFR	WSOP	DQF	8	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMK1C1102APWR	TSSOP	PW	8	3000	356	356	35
LMK1C1103APWR	TSSOP	PW	8	3000	356	356	35
LMK1C1104APWR	TSSOP	PW	8	3000	356	356	35
LMK1C1106APWR	TSSOP	PW	14	3000	356	356	35
LMK1C1108APWR	TSSOP	PW	16	3000	356	356	35
LMK1C1102ADQFR	WSOP	DQF	8	3000	205.0	200.0	33.0
LMK1C1104ADQFR	WSOP	DQF	8	3000	205.0	200.0	33.0

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMK1C1102ADQFR	Active	Production	WSOP (DQF) 8	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	L02A
LMK1C1102APWR	Active	Production	TSSOP (PW) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1102A
LMK1C1103APWR	Active	Production	TSSOP (PW) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1103A
LMK1C1104ADQFR	Active	Production	WSOP (DQF) 8	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	L04A
LMK1C1104APWR	Active	Production	TSSOP (PW) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1104A
LMK1C1106APWR	Active	Production	TSSOP (PW) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1106A
LMK1C1108APWR	Active	Production	TSSOP (PW) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1108A

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

NOTES:

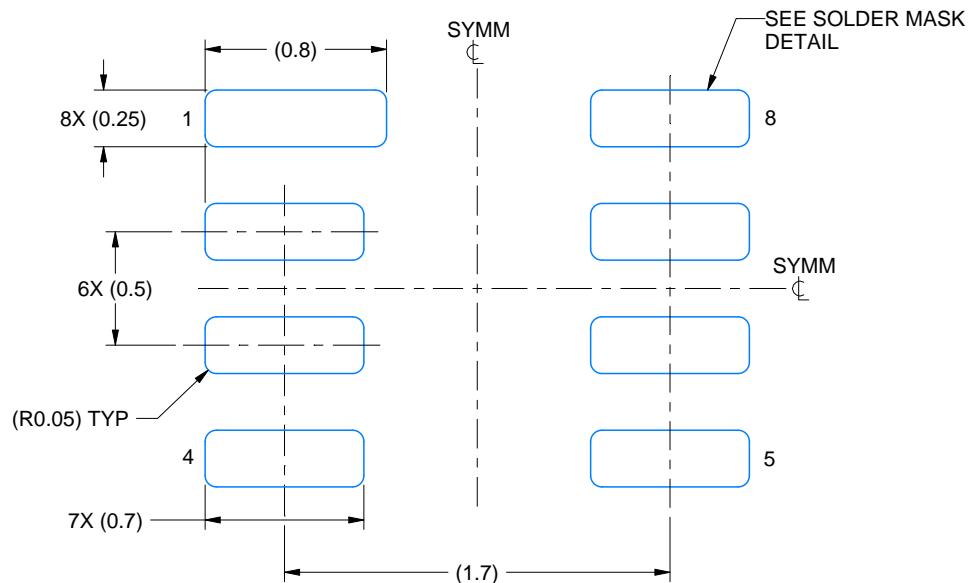
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

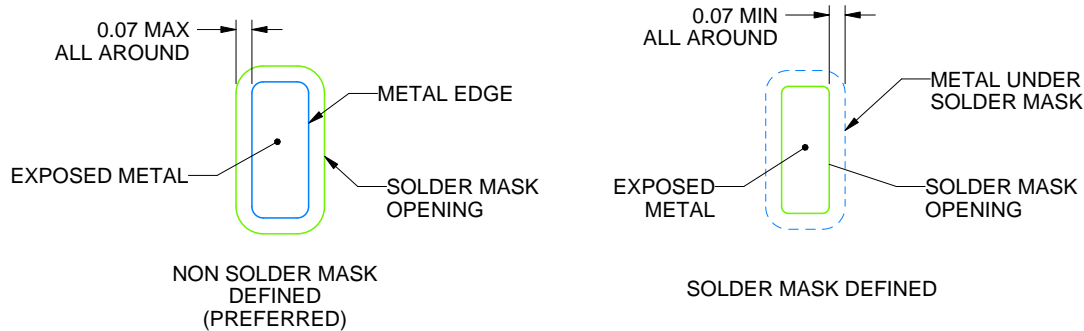
DQF0008A

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X



SOLDER MASK DETAILS

4220563/A 03/2021

NOTES: (continued)

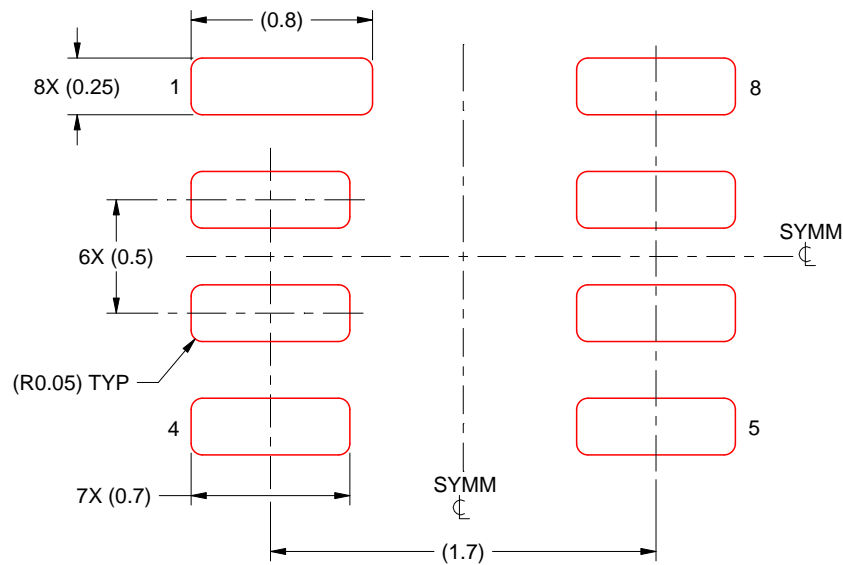
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).

EXAMPLE STENCIL DESIGN

DQF0008A

WSO - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 30X

4220563/A 03/2021

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PW0014A

PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW0008A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

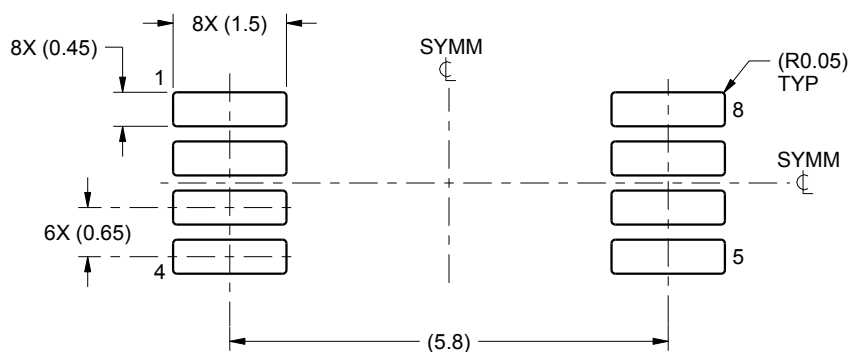
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

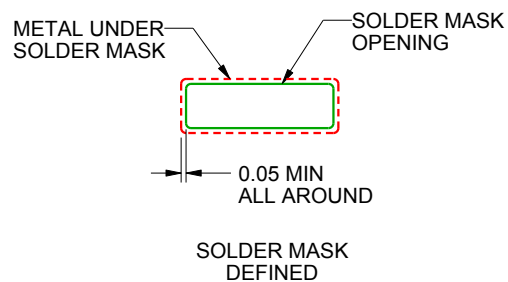
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated