

LMH6702QML-SP 1.7GHz, Ultra-Low-Distortion, Wideband Op Amp

1 Features

- $V_S = \pm 5V$, $T_A = 25^\circ C$, $A_V = +2V/V$, $R_L = 100\Omega$, $V_{OUT} = 2V_{PP}$, typical unless noted otherwise
- Available with radiation ensurance
 - High dose rate 300krad(Si)
 - ELDRS free 300krad(Si)
- -3dB bandwidth ($V_{OUT} = 0.2V_{PP}$) 720MHz
- Low noise 1.83nV/ \sqrt{Hz}
- Fast settling to 0.1% 13.4ns
- Fast slew rate 3100V/ μs
- Supply current 12.5mA
- Output current 80mA
- Low intermodulation distortion (75MHz) -67dBc
- Improved replacement for CLC409 and CLC449

2 Applications

- Flash A/D driver
- D/A transimpedance buffer
- Wide dynamic range IF amp
- Radar and communication receivers
- Line driver
- High-resolution video

3 Description

The LMH6702QML-SP is a very wideband, dc-coupled, monolithic operational amplifier designed specifically for wide-dynamic-range systems requiring exceptional signal fidelity. Benefiting from TI's current-feedback architecture, the LMH6702QML-SP offers unity gain stability at exceptional speed without need for external compensation.

With a 720MHz bandwidth ($A_V = 2V/V$, $V_O = 2V_{PP}$), 10-bit distortion levels through 60MHz ($R_L = 100\Omega$), 1.83nV/ \sqrt{Hz} input-referred noise, and 12.5mA supply current, the LMH6702QML-SP is an excellent driver or buffer for high-speed flash analog-to-digital (A/D) and digital-to-analog (D/A) converters.

The LMH6702QML-SP benefits wide dynamic range systems, such as radar and communication receivers, that require a wideband amplifier offering exceptional signal purity. The low input-referred noise and low harmonic and intermodulation distortion make this device an excellent choice for high-speed applications.

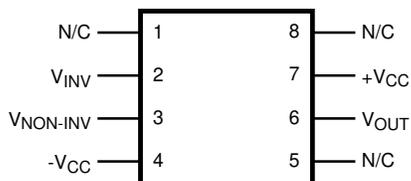
The LMH6702QML-SP is constructed using TI's VIP10 complimentary bipolar process and TI's proven current-feedback architecture.

Package Information

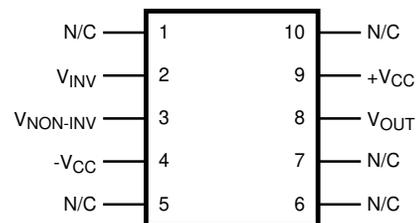
| PART NUMBER | PACKAGE ⁽¹⁾ | PACKAGE SIZE ⁽²⁾ |
|---------------|------------------------|-----------------------------|
| LMH6702QML-SP | NAB (CDIP, 8) | 10.16mm × 7.87mm |
| | NAC (CFP, 10) | 9.91mm × 6.45mm |

(1) For more information, see [Section 9](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



NAB Package, 8-Pin CDIP (Top View)



NAC Package, 10-Pin CLGA (Top View)



Table of Contents

| | | | |
|--|----------|--|-----------|
| 1 Features | 1 | 6 Application and Implementation | 9 |
| 2 Applications | 1 | 6.1 Application Information..... | 9 |
| 3 Description | 1 | 6.2 Layout..... | 11 |
| 4 Pin Configuration and Functions | 2 | 7 Device and Documentation Support | 12 |
| 5 Specifications | 3 | 7.1 Receiving Notification of Documentation Updates.... | 12 |
| 5.1 Absolute Maximum Ratings..... | 3 | 7.2 Support Resources..... | 12 |
| 5.2 Recommended Operating Conditions..... | 4 | 7.3 Trademarks..... | 12 |
| 5.3 Quality Conformance Inspection..... | 4 | 7.4 Electrostatic Discharge Caution..... | 12 |
| 5.4 Electrical Characteristics: DC Parameters..... | 5 | 7.5 Glossary..... | 12 |
| 5.5 Electrical Characteristics: AC Parameters..... | 5 | 8 Revision History | 12 |
| 5.6 Electrical Characteristics: Drift Values Parameters..... | 5 | 9 Mechanical, Packaging, and Orderable Information .. | 12 |
| 5.7 Typical Characteristics..... | 6 | | |

4 Pin Configuration and Functions

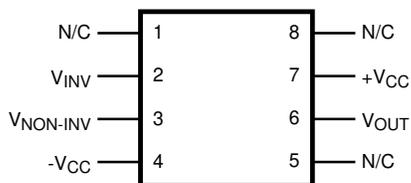


Figure 4-1. NAB Package, 8-Pin CDIP (Top View)

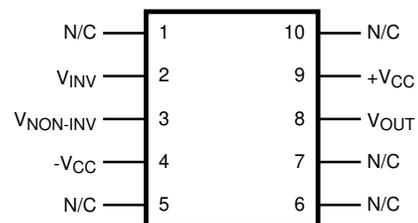


Figure 4-2. NAC Package, 10-Pin CLGA (Top View)

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | VALUE |
|--|--|
| Supply voltage (V_{CC}) | $\pm 6.75V_{DC}$ |
| Common-mode input voltage (V_{CM}) | V^- to V^+ |
| Power dissipation (P_D) ⁽²⁾ | 1W |
| Junction temperature (T_J) | 175°C |
| Lead temperature (soldering, 10 seconds) | 300°C |
| Storage temperature | $-65^\circ\text{C} \leq T_A \leq +150^\circ\text{C}$ |
| Thermal resistance | |
| θ_{JA} | |
| CDIP (still air) | 170°C/W |
| CDIP (500LF/min air flow) | 100°C/W |
| CLGA (still air) | 220°C/W |
| CLGA (500LF/min air flow) | 150°C/W |
| θ_{JC} | |
| CDIP | 35°C/W |
| CLGA | 37°C/W |
| Package weight (typical) | |
| CDIP | 1078mg |
| CLGA | 227mg |
| ESD tolerance ⁽³⁾ | 1000V |

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A) / \theta_{JA}$ or the number given in the *Absolute Maximum Ratings*, whichever is lower.
- (3) Human body model, 1.5k Ω in series with 100pF.

5.2 Recommended Operating Conditions

| | VALUE |
|---|---|
| Supply voltage (V_{CC}) | $\pm 5V_{DC}$ to $\pm 6V_{DC}$ |
| Gain | ± 1 to ± 10 |
| Ambient operating temperature (T_A) | -55°C to $+125^{\circ}\text{C}$ |

5.3 Quality Conformance Inspection

MIL-STD-883, Method 5005, Group A

| SUBGROUP | DESCRIPTION | TEMPERATURE ($^{\circ}\text{C}$) |
|----------|---------------------|------------------------------------|
| 1 | Static tests at | 25 |
| 2 | Static tests at | 125 |
| 3 | Static tests at | -55 |
| 4 | Dynamic tests at | 25 |
| 5 | Dynamic tests at | 125 |
| 6 | Dynamic tests at | -55 |
| 7 | Functional tests at | 25 |
| 8A | Functional tests at | 125 |
| 8B | Functional tests at | -55 |
| 9 | Switching tests at | 25 |
| 10 | Switching tests at | 125 |
| 11 | Switching tests at | -55 |

5.4 Electrical Characteristics: DC Parameters

The following conditions apply (unless otherwise specified)⁽¹⁾ ⁽²⁾:

$R_L = 100\Omega$, $V_{CC} = \pm 5V_{DC}$, $A_V = +2$ feedback resistor (R_F) = 250 Ω , gain resistor (R_G) = 250 Ω

| PARAMETER | | TEST CONDITIONS | NOTES | MIN | MAX | UNIT | SUB-GROUPS |
|-----------|----------------------------------|--|-------|------|-----|---------|------------|
| I_{BN} | Input bias current, noninverting | | | -15 | 15 | μA | 1, 2 |
| | | | | -21 | 21 | μA | 3 |
| I_{BI} | Input bias current, inverting | | | -30 | 30 | μA | 1, 2 |
| | | | | -34 | 34 | μA | 3 |
| V_{IO} | Input offset voltage | | | -4.5 | 4.5 | mV | 1, 3 |
| | | | | -6.0 | 6.0 | mV | 2 |
| I_{CC} | Supply current, no load | $R_L = \infty$ | | | 15 | mA | 1, 2, 3 |
| PSSR | Power supply rejection ratio | $-V_{CC} = -4.5V$ to $-5.0V$, $+V_{CC} = 4.5V$ to $5.0V$ | | 45 | | dB | 1, 2, 3 |

- (1) The algebraic convention, whereby the most negative value is a minimum and most positive is a maximum, is used in this table. Negative current shall be defined as conventional current flow out of a device terminal.
- (2) Pre- and post-irradiation limits are identical to those listed under the dc parameter tables. Post-irradiation testing is conducted at room temperature, 25°C, only. Testing is performed as specified in MIL-STD-883 Test Method 1019 Condition A. The ELDRS-Free part is also tested per Test Method 1019 Conditions D.

5.5 Electrical Characteristics: AC Parameters

The following conditions apply (unless otherwise specified)⁽¹⁾ ⁽²⁾:

$R_L = 100\Omega$, $V_{CC} = \pm 5V_{DC}$, $A_V = +2$ feedback resistor (R_F) = 250 Ω , gain resistor (R_G) = 250 Ω

| PARAMETER | | TEST CONDITIONS | NOTES | MIN | MAX | UNIT | SUB-GROUPS |
|-----------|-------------------------|------------------------------------|-------|-----|-----|------|------------|
| HD_3 | 3rd harmonic distortion | $2V_{PP}$ at 20MHz | | | -62 | dBc | 4 |
| GFPL | Gain flatness peaking | 0.1MHz to 75MHz, $V_O < 0.5V_{PP}$ | | | 0.4 | dB | 4 |
| GFPH | Gain flatness peaking | > 75MHz, $V_O < 0.5V_{PP}$ | | | 2.0 | dB | 4 |
| GFRH | Gain flatness rolloff | 75MHz to 125MHz, $V_O < 0.5V_{PP}$ | | | 0.2 | dB | 4 |
| HD_2 | 2nd harmonic distortion | $2V_{PP}$ at 20MHz | | | -52 | dBc | 4 |

- (1) The algebraic convention, whereby the most negative value is a minimum and most positive is a maximum, is used in this table. Negative current shall be defined as conventional current flow out of a device terminal.
- (2) These parameters are not post irradiation tested.

5.6 Electrical Characteristics: Drift Values Parameters

The following conditions apply (unless otherwise specified)⁽¹⁾:

$R_L = 100\Omega$, $V_{CC} = \pm 5V_{DC}$, $A_V = +2$ feedback resistor (R_F) = 250 Ω , gain resistor (R_G) = 250 Ω

Delta not required on B level product. Delta required for S-level product at Group B5 only, or as specified on the internal processing instruction (IPI).

| PARAMETER | | TEST CONDITIONS | PACKAGE | MIN | MAX | UNIT | SUB-GROUPS |
|-----------|---------------------------------|-----------------|---------|-------|------|---------|------------|
| I_{BN} | Input bias current noninverting | | NAB | -0.3 | 0.3 | μA | 1 |
| | | | NAC | -0.75 | 0.75 | | |
| I_{BI} | Input bias current inverting | | | -3.0 | 3.0 | μA | 1 |
| V_{IO} | Input offset voltage | | NAB | -0.3 | 0.3 | mV | 1 |
| | | | NAC | -1.0 | 1.0 | | |

- (1) The algebraic convention, whereby the most negative value is a minimum and most positive is a maximum, is used in this table. Negative current shall be defined as conventional current flow out of a device terminal.

5.7 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_L = 100\Omega$, and $R_F = 237\Omega$ (unless otherwise noted)

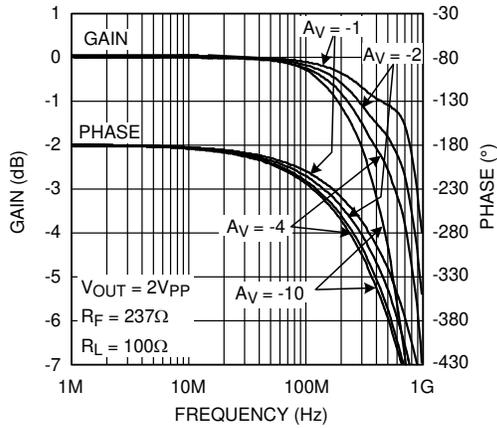


Figure 5-1. Inverting Frequency Response

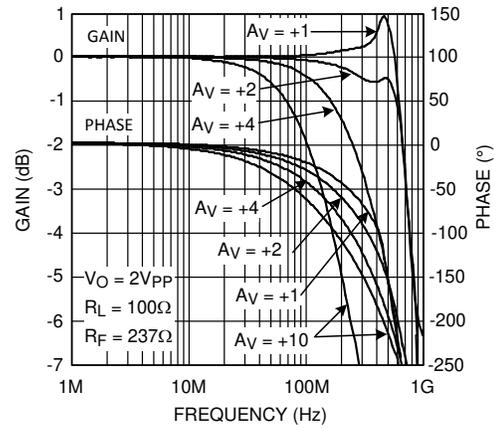


Figure 5-2. Noninverting Frequency Response

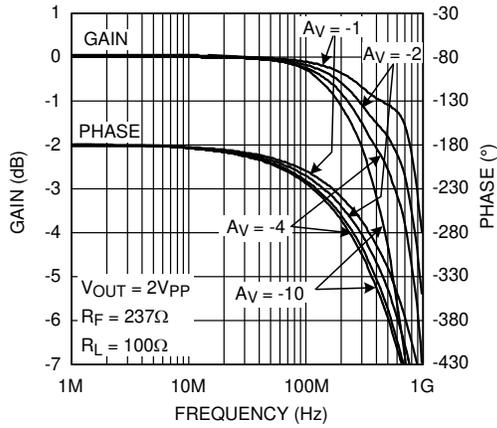


Figure 5-3. Inverting Frequency Response

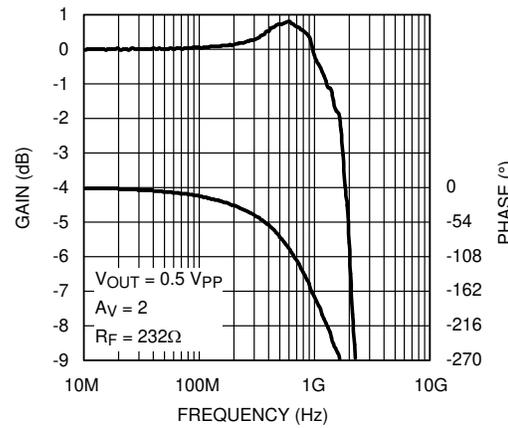


Figure 5-4. Small-Signal Bandwidth

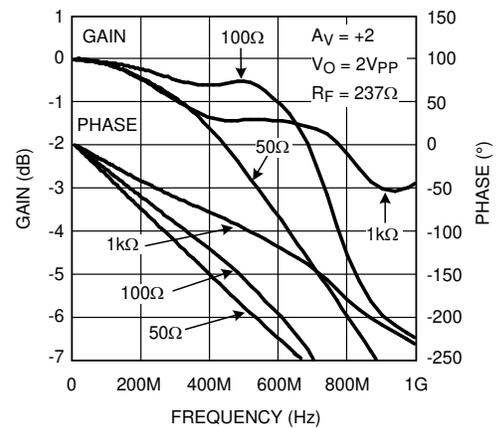


Figure 5-5. Frequency Response for Various R_L , $A_V = +2$

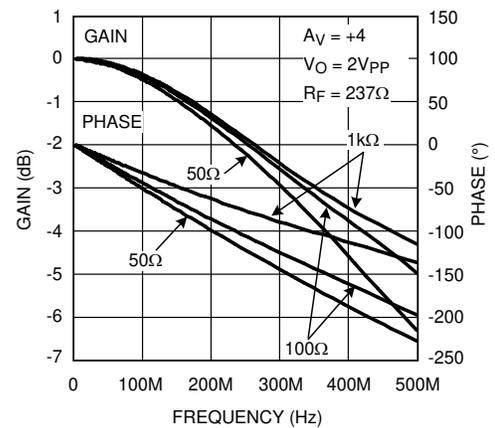


Figure 5-6. Frequency Response for Various R_L , $A_V = +4$

5.7 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_L = 100\Omega$, and $R_F = 237\Omega$ (unless otherwise noted)

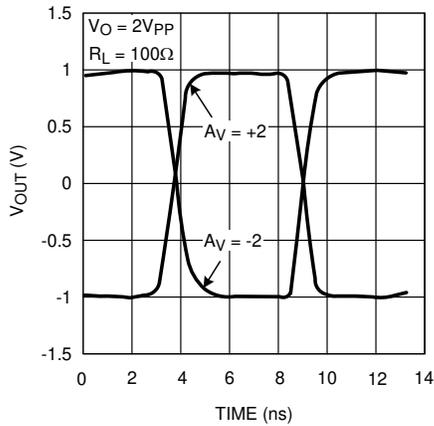


Figure 5-7. Step Response, 2V_{PP}

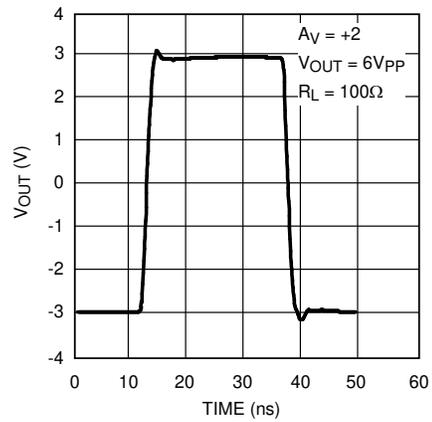


Figure 5-8. Step Response, 6V_{PP}

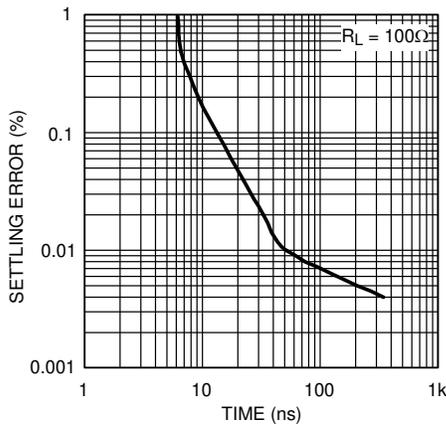


Figure 5-9. Percent Settling vs Time

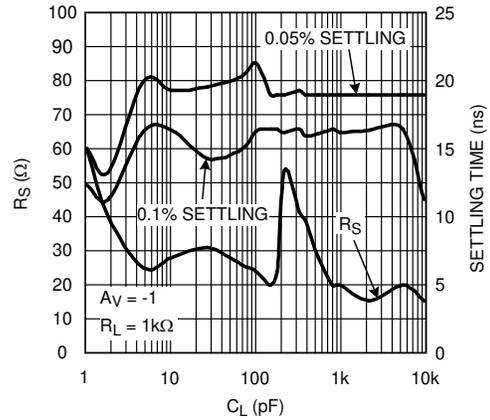


Figure 5-10. R_S and Settling Time vs C_L

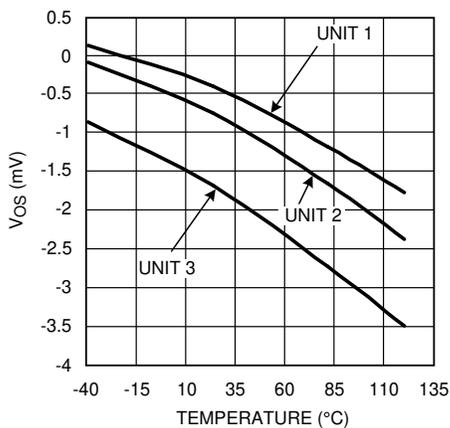


Figure 5-11. Input Offset for Three Representative Units

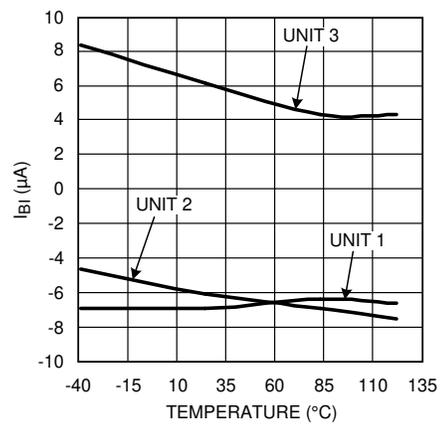


Figure 5-12. Inverting Input Bias for Three Representative Units

5.7 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_L = 100\Omega$, and $R_F = 237\Omega$ (unless otherwise noted)

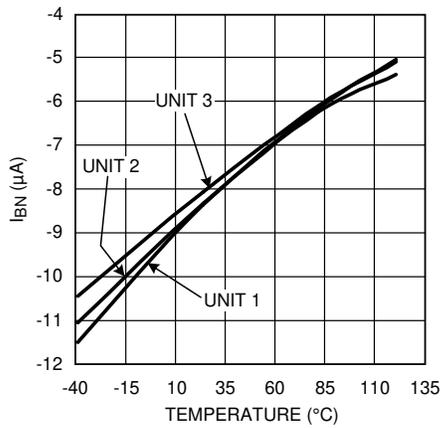


Figure 5-13. Noninverting Input Bias for Three Representative Units

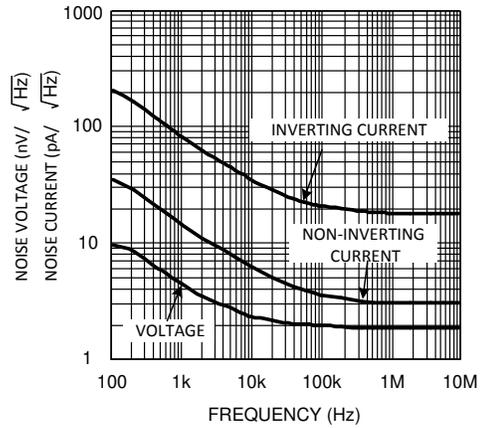


Figure 5-14. Noise

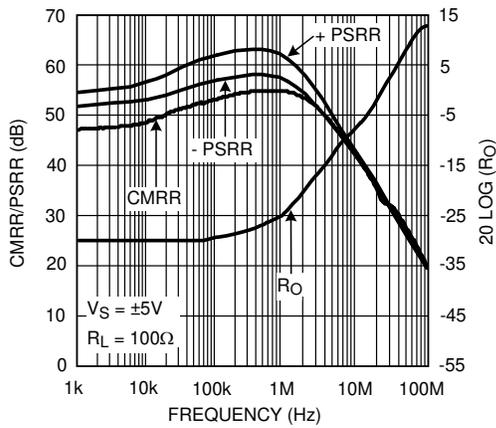


Figure 5-15. CMRR, PSRR, R_{OUT}

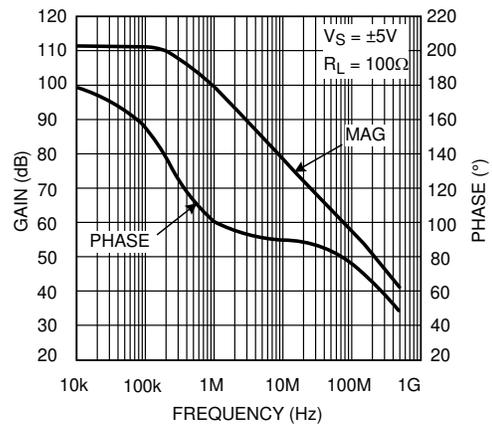


Figure 5-16. Transimpedance

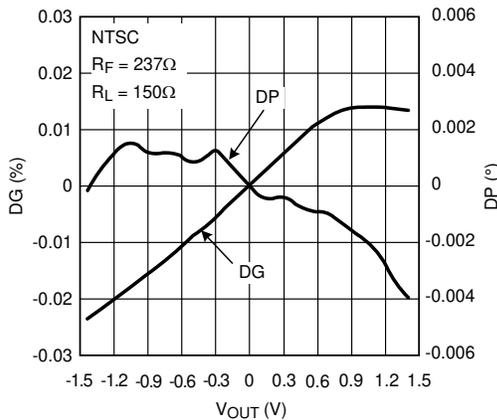


Figure 5-17. DG/DP (NTSC)

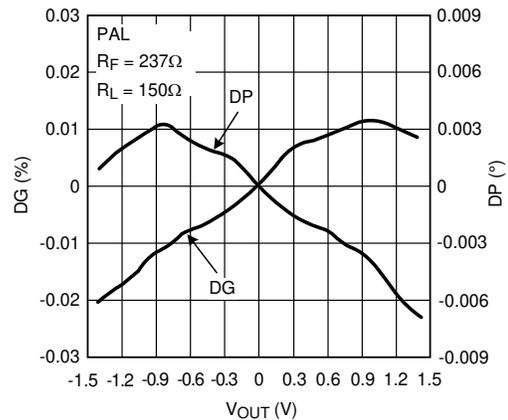


Figure 5-18. DG/DP (PAL)

6 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

6.1 Application Information

6.1.1 Feedback Resistor

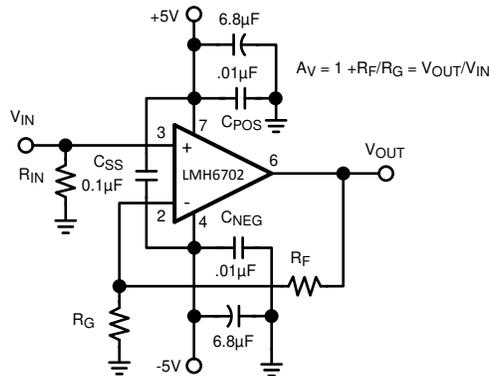


Figure 6-1. Recommended Noninverting Gain Circuit

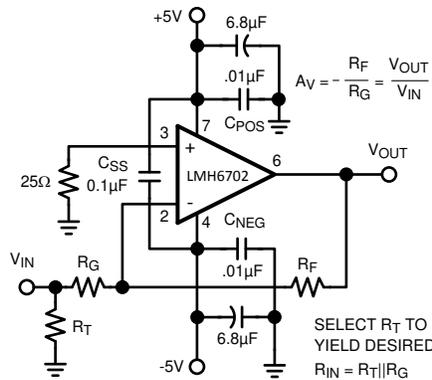


Figure 6-2. Recommended Inverting Gain Circuit

The LMH6702 achieves excellent pulse and distortion performance by using current feedback topology. The loop gain for a current-feedback op amp, and thus the frequency response, is predominantly set by the feedback-resistor value. The LMH6702 is optimized for use with a 237Ω feedback resistor. Using lower values can lead to excessive ringing in the pulse response while a higher value limits the bandwidth. Application Note OA-13 [SNOA366](#) discusses this configuration in detail along with the occasions where a different R_F can be advantageous.

6.1.2 Harmonic Distortion

The LMH6702 has been optimized for exceptionally low harmonic distortion while driving very demanding resistive or capacitive loads. Generally, when used as the input amplifier to very high-speed flash ADCs, the distortions introduced by the converter dominate over the low LMH6702 distortions. Capacitor C_{SS} , shown across the supplies in [Figure 6-1](#) and [Figure 6-2](#), is critical to achieving the lowest 2nd harmonic distortion.

For absolute minimum distortion levels, keep the supply decoupling currents (ground connections to C_{POS} , and C_{NEG} in [Figure 6-1](#) and [Figure 6-2](#)) separate from the ground connections to sensitive input circuitry (such as R_G , R_T , and R_{IN} ground connections). Splitting the ground plane in this manner, and separately routing the high frequency current spikes on the decoupling caps back to the power supply (similar to a *star connection* layout technique) provides minimum coupling back to the input circuitry and results in best harmonic distortion response (especially 2nd-order distortion).

If this layout technique has not been observed on a particular application board, the supply decoupling capacitors can adversely affect HD2 performance by increasing the coupling phenomenon already mentioned. [Figure 6-3](#) shows actual HD2 data on a board where the ground plane is shared between the supply decoupling capacitors and the rest of the circuit. After these capacitors are removed, the HD2 distortion levels reduce significantly, especially between 10MHz to 20MHz, as shown in [Figure 6-3](#).

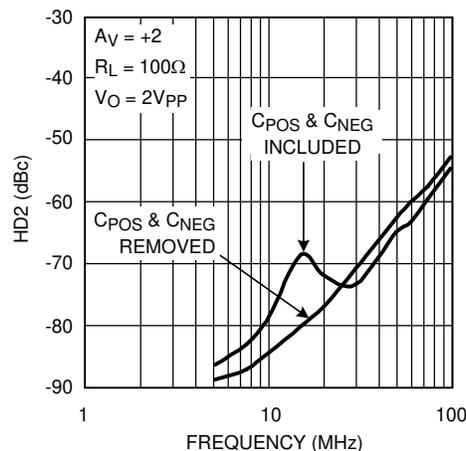


Figure 6-3. Decoupling Current Adverse Effect on a Board With Shared Ground Plane

At these extremely low distortion levels, the high-frequency behavior of decoupling capacitors themselves can be significant. In general, lower-value decoupling capacitors tend to have higher resonance frequencies, making lower-value decoupling capacitors more effective for higher-frequency regions. A particular application board that has been laid out correctly with ground returns split to minimize coupling benefits the most by having low-value and higher-value capacitors paralleled to take advantage of the effective bandwidth of each, and extend the low-distortion frequency range.

6.1.3 Capacitive Load Drive

[Figure 6-4](#) shows a typical application using the LMH6702 to drive an ADC.

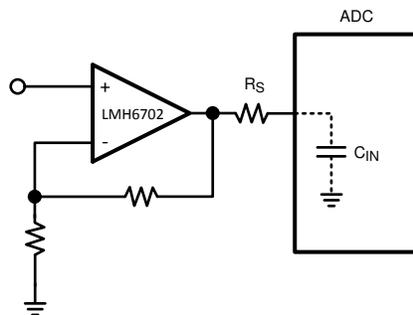


Figure 6-4. Input Amplifier to ADC

The series resistor, R_S , between the amplifier output and the ADC input is critical to achieving best system performance. This load capacitance, if applied directly to the output pin, can quickly lead to unacceptable levels of ringing in the pulse response. The plot of R_S and Settling Time vs C_L in the *Typical Characteristics* is an

excellent starting point for selecting R_S . The value derived in that plot minimizes the step settling time into a fixed discrete capacitive load with the output driving a very light resistive load (1k Ω). Sensitivity to capacitive loading is greatly reduced after the output is loaded more heavily. Therefore, for cases where the output is heavily loaded, R_S value can be reduced. The exact value can best be determined experimentally for these cases.

In applications where the LMH6702 is replacing the CLC409, take care when the device is lightly loaded and some capacitance is present at the output. As a result of the much higher frequency response of the LMH6702 compared to the CLC409, increased susceptibility to low value output capacitance (parasitic or inherent to the board layout or otherwise being part of the output load) is possible. As previously mentioned, this susceptibility is most noticeable when the LMH6702 resistive load is light. Parasitic capacitance can be minimized by careful layout. Addition of an output snubber R-C network also helps by increasing the high-frequency resistive loading.

Referring back to [Figure 6-4](#), consider several additional constraints in driving the capacitive input of an ADC. There is an option to increase R_S , band-limiting at the ADC input for either noise or Nyquist band-limiting purposes. However, increasing R_S too much can induce an unacceptably large input glitch due to switching transients coupling through from the convert signal. Also, C_{IN} is often a voltage-dependent capacitance. This input impedance nonlinearity induces distortion terms that increase as R_S is increased. Therefore, attempt only slight adjustments up or down from the recommended R_S value in optimizing system performance.

6.1.4 DC Accuracy and Noise

Example below shows the output offset computation equation for the noninverting configuration using the typical bias current and offset specifications for $A_V = +2$:

$$\text{Output Offset: } V_O = (\pm I_{BN} \times R_{IN} \pm V_{IO}) (1 + R_F/R_G) \pm |I_{BI}| \times R_F$$

Where R_{IN} is the equivalent input impedance on the noninverting input.

Example computation for $A_V = +2$, $R_F = 237\Omega$, $R_{IN} = 25\Omega$:

$$V_O = (\pm 6\mu\text{A} \times 25\Omega \pm 1\text{mV}) (1 + 237/237) \pm 8\mu\text{A} \times 237 = \pm 4.20\text{mV}$$

A good design, however, includes a worst-case calculation using minimum and maximum numbers in the data sheet tables to provide worst-case operation.

Further improvement in the output offset voltage and drift is possible using composite amplifiers. The two input bias currents are physically unrelated in both magnitude and polarity for the current feedback topology. Therefore, to cancel the effects by matching the source impedance for the two inputs (as is commonly done for matched input bias current devices) is not possible.

The total output noise is computed in a similar fashion to the output offset voltage. Using the input noise voltage and the two input noise currents, the output noise is developed through the same gain equations for each term but combined as the square root of the sum of squared contributing elements. See the [OA-12 Noise Analysis for Comlinear Amplifiers application report](#) for a full discussion of noise calculations for current-feedback amplifiers.

6.2 Layout

6.2.1 Layout Guidelines

Generally, a good high frequency layout keeps power supply and ground traces away from the inverting input and output pins. Parasitic capacitance on these nodes to ground cause frequency-response peaking and possible circuit oscillations (see the [OA-15 Frequent Faux Pas in Applying Wideband Current Feedback Amplifiers application report](#) for more information). Texas Instruments suggests the following evaluation boards as a guide for high-frequency layout and as an aid in device testing and characterization:

| DEVICE | PACKAGE | EVALUATION BOARD PART NUMBER |
|--------------|--------------|------------------------------|
| LMH6702QMLMF | SOT-23-5 | CLC730216 |
| LMH6702QMLMA | Plastic SOIC | CLC730227 |

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.2 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

7.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

7.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (March 2013) to Revision F (August 2024) Page

- Updated the numbering format for tables, figures, and cross-references throughout the document..... 1
- Changed input bias current noninverting limits from $\pm 0.3\mu\text{A}$ to $\pm 0.75\mu\text{A}$ for NAC package type in *LMH6702 Electrical Characteristics Drift Values Parameters* 5
- Changed input offset voltage limits from $\pm 0.3\text{mV}$ to $\pm 1\text{mV}$ for NAC package type in *LMH6702 Electrical Characteristics Drift Values Parameters* 5

Changes from Revision D (October 2011) to Revision E (March 2013) Page

- Changed layout of National data sheet to TI format..... 1

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---------------------------------|---------------|----------------------|----------------|--------------------------|-------------|--------------------------------------|-----------------------------------|--------------|---|
| 5962-0254601VPA | Active | Production | CDIP (NAB) 8 | 40 TUBE | No | SNPB | Level-1-NA-UNLIM | -55 to 125 | LMH6702J-QV 5962-02546 01VPA Q ACO 01VPA Q >T |
| 5962-0254601VZA | Active | Production | CFP (NAC) 10 | 54 JEDEC TRAY (5+1) | No | SNPB | Level-1-NA-UNLIM | -55 to 125 | LMH6702 WGQMLV Q 5962-02546 01VZA ACO 01VZA >T |
| 5962F0254601VPA | Active | Production | CDIP (NAB) 8 | 40 TUBE | No | SNPB | Level-1-NA-UNLIM | -55 to 125 | LMH6702JFQV 5962F02546 01VPA Q ACO 01VPA Q >T |
| 5962F0254601VZA | Active | Production | CFP (NAC) 10 | 54 JEDEC TRAY (5+1) | No | SNPB | Level-1-NA-UNLIM | -55 to 125 | LMH6702 WGFQMLV Q 5962F02546 01VZA ACO 01VZA >T |
| 5962F0254602VPA | Active | Production | CDIP (NAB) 8 | 40 TUBE | No | SNPB | Level-1-NA-UNLIM | -55 to 125 | LMH6702JFLQV 5962F02546 02VPA Q ACO 02VPA Q >T |
| LMH6702J-QMLV | Active | Production | CDIP (NAB) 8 | 40 TUBE | No | SNPB | Level-1-NA-UNLIM | -55 to 125 | LMH6702J-QV 5962-02546 01VPA Q ACO 01VPA Q >T |
| LMH6702J-QMLV.A | Active | Production | CDIP (NAB) 8 | 40 TUBE | No | SNPB | Level-1-NA-UNLIM | -55 to 125 | LMH6702J-QV 5962-02546 01VPA Q ACO 01VPA Q >T |
| LMH6702JFLQMLV | Active | Production | CDIP (NAB) 8 | 40 TUBE | No | SNPB | Level-1-NA-UNLIM | -55 to 125 | LMH6702JFLQV 5962F02546 02VPA Q ACO 02VPA Q >T |

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|--------------------------------|---------------|----------------------|----------------|--------------------------|-------------|--------------------------------------|-----------------------------------|--------------|---|
| LMH6702JFQMLV | Active | Production | CDIP (NAB) 8 | 40 TUBE | No | SNPB | Level-1-NA-UNLIM | -55 to 125 | LMH6702JFQV 5962F02546 01VPA Q ACO 01VPA Q >T |
| LMH6702JFQMLV.A | Active | Production | CDIP (NAB) 8 | 40 TUBE | No | SNPB | Level-1-NA-UNLIM | -55 to 125 | LMH6702JFQV 5962F02546 01VPA Q ACO 01VPA Q >T |
| LMH6702WG-QMLV | Active | Production | CFP (NAC) 10 | 54 JEDEC TRAY (5+1) | No | SNPB | Level-1-NA-UNLIM | -55 to 125 | LMH6702 WGQMLV Q 5962-02546 01VZA ACO 01VZA >T |
| LMH6702WG-QMLV.A | Active | Production | CFP (NAC) 10 | 54 JEDEC TRAY (5+1) | No | SNPB | Level-1-NA-UNLIM | -55 to 125 | LMH6702 WGQMLV Q 5962-02546 01VZA ACO 01VZA >T |
| LMH6702WGFQMLV | Active | Production | CFP (NAC) 10 | 54 JEDEC TRAY (5+1) | No | SNPB | Level-1-NA-UNLIM | -55 to 125 | LMH6702 WGFQMLV Q 5962F02546 01VZA ACO 01VZA >T |
| LMH6702WGFQMLV.A | Active | Production | CFP (NAC) 10 | 54 JEDEC TRAY (5+1) | No | SNPB | Level-1-NA-UNLIM | -55 to 125 | LMH6702 WGFQMLV Q 5962F02546 01VZA ACO 01VZA >T |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

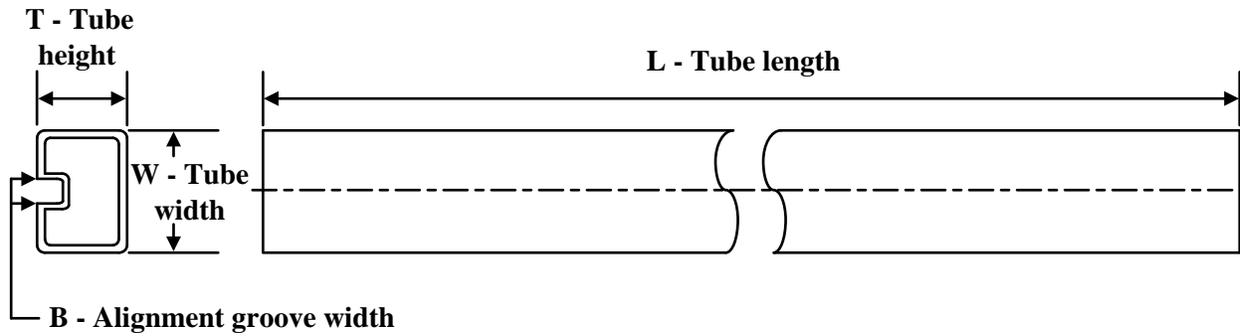
(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

- (4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

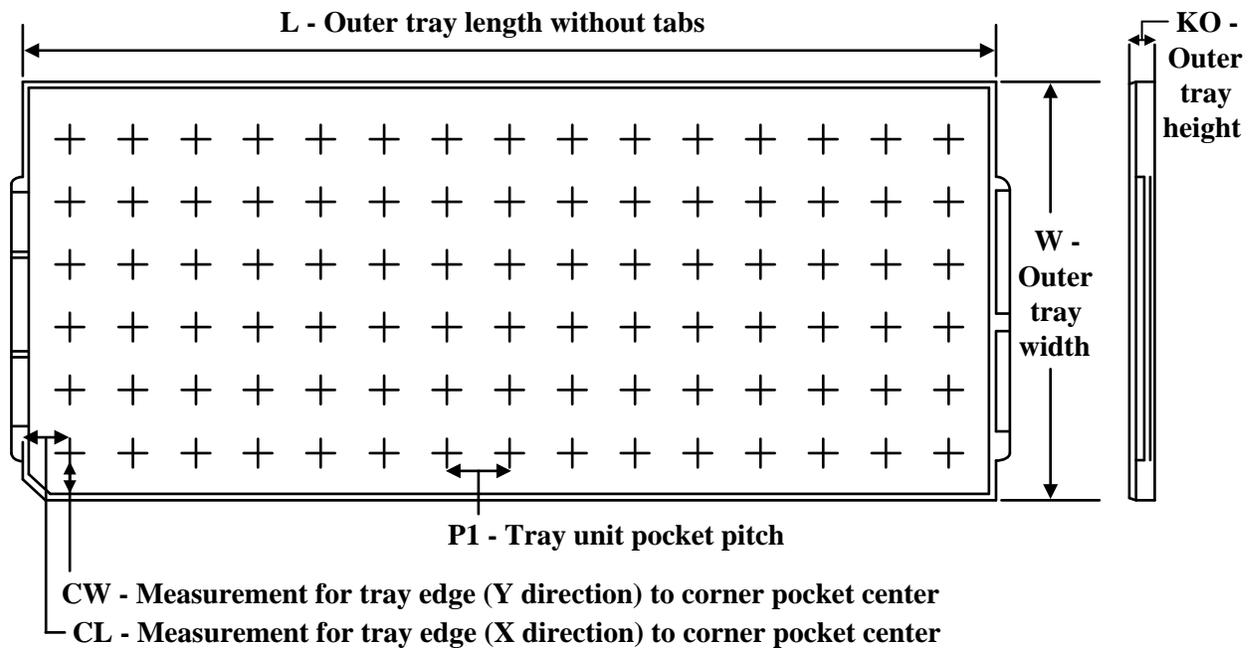
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-0254601VPA | NAB | CDIP | 8 | 40 | 506.98 | 15.24 | 13440 | NA |
| 5962F0254601VPA | NAB | CDIP | 8 | 40 | 506.98 | 15.24 | 13440 | NA |
| LMH6702J-QMLV | NAB | CDIP | 8 | 40 | 506.98 | 15.24 | 13440 | NA |
| LMH6702J-QMLV.A | NAB | CDIP | 8 | 40 | 506.98 | 15.24 | 13440 | NA |
| LMH6702JFQMLV | NAB | CDIP | 8 | 40 | 506.98 | 15.24 | 13440 | NA |
| LMH6702JFQMLV.A | NAB | CDIP | 8 | 40 | 506.98 | 15.24 | 13440 | NA |

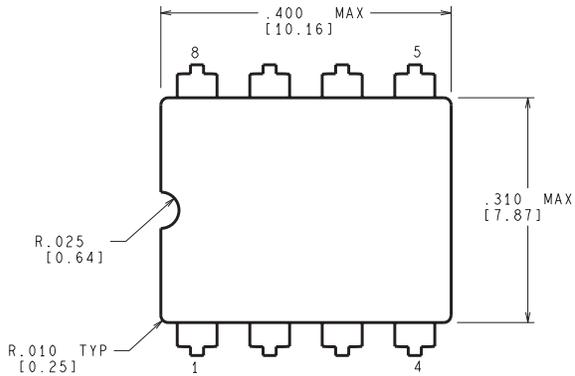
TRAY


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

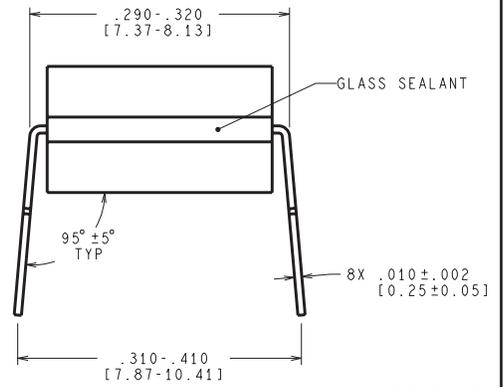
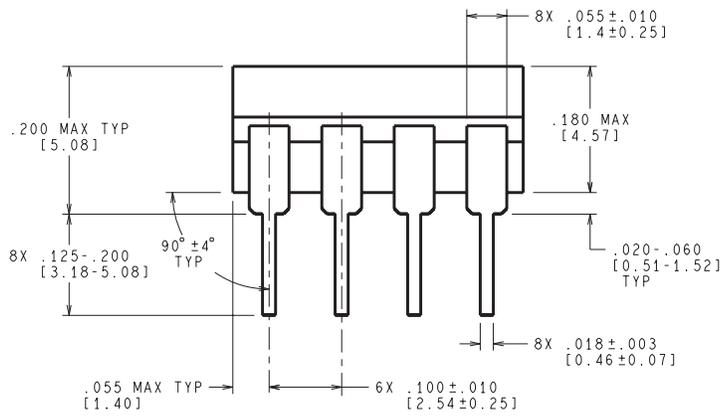
*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|------------------|--------------|--------------|------|-----|-------------------|----------------------|--------|--------|---------|---------|---------|---------|
| 5962-0254601VZA | NAC | CFP | 10 | 54 | 6 X 9 | 100 | 101.6 | 101.6 | 8001 | 2.78 | 16.08 | 16.08 |
| 5962F0254601VZA | NAC | CFP | 10 | 54 | 6 X 9 | 100 | 101.6 | 101.6 | 8001 | 2.78 | 16.08 | 16.08 |
| LMH6702WG-QMLV | NAC | CFP | 10 | 54 | 6 X 9 | 100 | 101.6 | 101.6 | 8001 | 2.78 | 16.08 | 16.08 |
| LMH6702WG-QMLV.A | NAC | CFP | 10 | 54 | 6 X 9 | 100 | 101.6 | 101.6 | 8001 | 2.78 | 16.08 | 16.08 |
| LMH6702WGFQMLV | NAC | CFP | 10 | 54 | 6 X 9 | 100 | 101.6 | 101.6 | 8001 | 2.78 | 16.08 | 16.08 |
| LMH6702WGFQMLV.A | NAC | CFP | 10 | 54 | 6 X 9 | 100 | 101.6 | 101.6 | 8001 | 2.78 | 16.08 | 16.08 |

NAB0008A



CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS



J08A (Rev M)

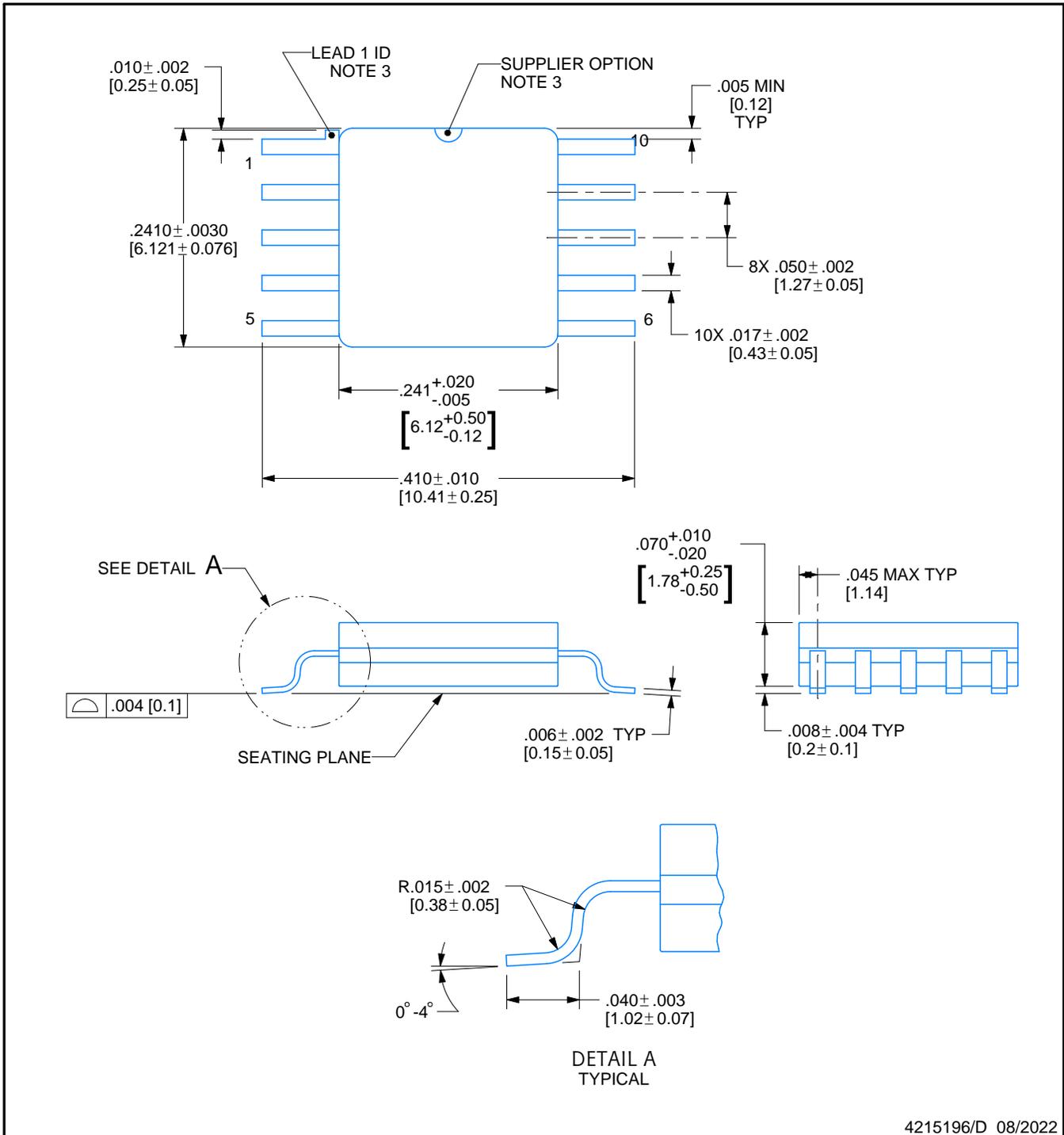


PACKAGE OUTLINE

NAC0010A

CFP - 2.33mm max height

CERAMIC FLATPACK



4215196/D 08/2022

NOTES:

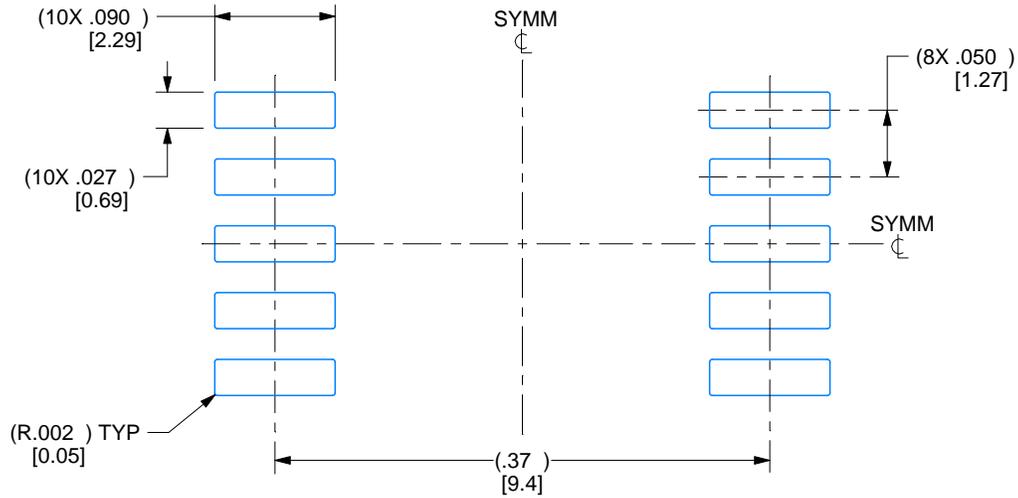
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. For solder thickness and composition, see the "Lead Finish Composition/Thickness" link in the packaging section of the Texas Instruments website
3. Lead 1 identification shall be:
 - a) A notch or other mark within this area
 - b) A tab on lead 1, either side
4. No JEDEC registration as of December 2021

EXAMPLE BOARD LAYOUT

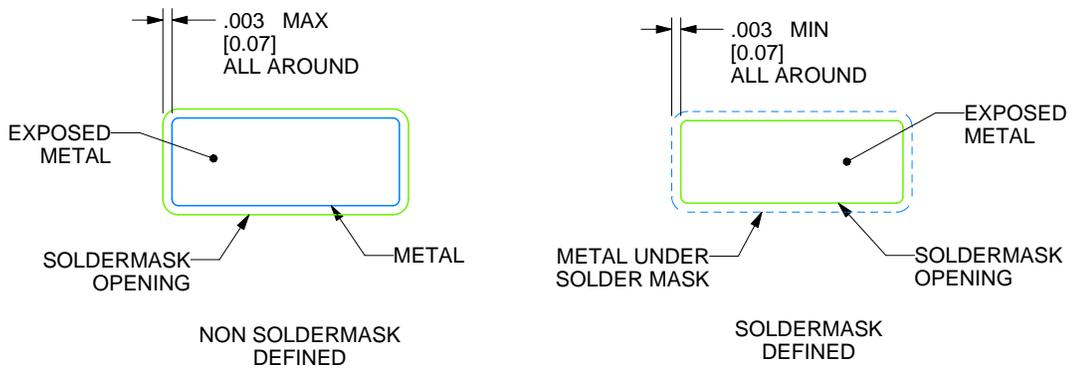
NAC0010A

CFP - 2.33mm max height

CERAMIC FLATPACK



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 7X



4215196/D 08/2022

REVISIONS

| REV | DESCRIPTION | E.C.N. | DATE | BY/APP'D |
|-----|--|---------|------------|-------------------------|
| A | RELEASE TO DOCUMENT CONTROL | 2197877 | 12/30/2021 | DAVID CHIN / ANIS FAUZI |
| B | NO CHANGE TO DRAWING; REVISION FOR YODA RELEASE; | 2198820 | 02/14/2022 | K. SINCERBOX |
| C | CHANGE PIN 1 ID LOCATION ON PIN | 2198845 | 02/18/2022 | D. CHIN / K. SINCERBOX |
| D | .2410± .0030 WAS .2700 +.0012/- .0002; | 2200915 | 08/08/2022 | D. CHIN / K. SINCERBOX |

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025