LMH6654, LMH6655 Single and Dual Low Power, 250 MHz, Low Noise Amplifiers

1 Features

- (V_S = ±5 V, T_J = 25 °C, Typical Values Unless Specified)
- Voltage Feedback Architecture
- Unity Gain Bandwidth 250 MHz
- Supply Voltage Range ±2.5V to ±6V
- Slew Rate 200 V/µsec
- Supply Current 4.5 mA/channel
- Input Common Mode Voltage −5.15V to +3.7V
- Output Voltage Swing (R_L = 100 Ω) −3.6V to 3.4V
- Input Voltage Noise 4.5 $nV/\sqrt{Hz}$
- Input Current Noise 1.7 $pA/\sqrt{Hz}$
- Settling Time to 0.01% 25 ns

2 Applications

- ADC Drivers
- Consumer Video
- Active Filters
- Pulse Delay Circuits
- xDSL Receiver
- Pre-amps

3 Description

The LMH6654 and LMH6655 single and dual high speed voltage feedback amplifiers are designed to have unity-gain stable operation with a bandwidth of 250 MHz. They operate from ±2.5 V to ±6 V and each channel consumes only 4.5 mA. The amplifiers feature very low voltage noise and wide output swing to maximize signal-to-noise ratio, and possess a true single supply capability with input common mode voltage range extending 150 mV below negative rail and within 1.3 V of the positive rail. The high speed and low power combination of the LMH6654 and LMH6655 make these products an ideal choice for many portable, high speed applications where power is at a premium.

The LMH6654 and LMH6655 are built on TI's Advance VIP10™ (Vertically Integrated PNP) complementary bipolar process.

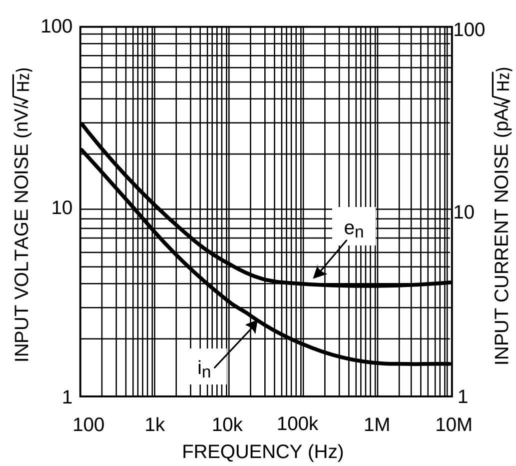
The LMH6654 is packaged in 5-Pin SOT-23 and 8-Pin SOIC. The LMH6655 is packaged in 8-Pin VSSOP (DGK) and 8-Pin SOIC.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMH6654	SOIC (8)	4.90 mm x 3.91 mm
LMH6654	SOT-23 (5)	2.90 mm x 1.60 mm
LMH6655	SOIC (8)	4.90 mm x 3.91 mm
LMH6655	VSSOP (8)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Figure 1. Input Voltage and Curernt Noise vs. Frequency (V_s= ±5V)



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (March 2013) to Revision E — **Page**

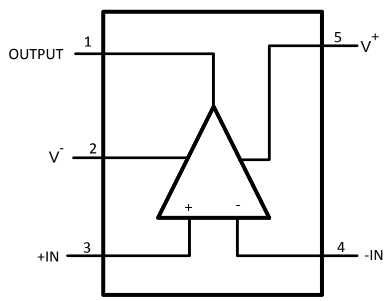
- Changed data sheet structure and organization. Added, updated, or renamed the following sections: Device Information Table, Application and Implementation; Power Supply Recommendations; Device and Documentation Support; Mechanical, Packaging, and Ordering Information. Deleted Switching Characteristics due to redundancy. ... 1
- Changed from Junction Temperature Range to "Operating Temperature Range" ... 4
- Deleted T_J = 25°C ... 5
- Deleted T_J = 25°C ... 7

Changes from Revision C (March 2013) to Revision D — **Page**

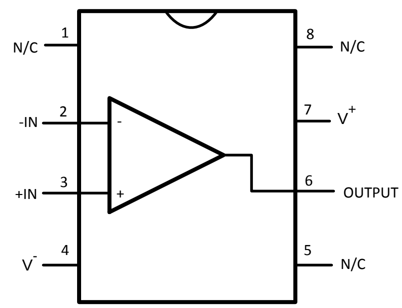
- Changed layout of National Data Sheet to TI format ... 19

5 Pin Configuration and Functions

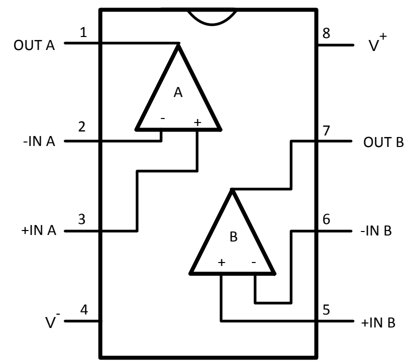
**5-Pin (LMH6654)
Package DBV
Top View**



**8-Pin (LMH6654)
Package D
Top View**



**8-Pin (LMH6655)
SOIC and VSSOP (DGK)
Top View**



Pin Functions

PIN				I/O	DESCRIPTION
NAME	LMH6654		LMH6655		
	DBV	D	DGK		
-IN	4	2		I	Inverting Input
+IN	3	3		I	Non-inverting Input
-IN A			2	I	ChA Inverting Input
+IN A			3	I	ChA Non-inverting Input
-IN B			6	I	ChB Inverting Input
+IN B			5	I	ChB Non-inverting Input
N/C		1, 5, 8		—	No Connection
OUT A			1	O	ChA Output
OUT B			7	O	ChB Output
OUTPUT	1	6		O	Output
V^-	2	4	4	I	Negative Supply
V^+	5	7	8	I	Positive Supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN} Differential			±1.2	V
Output Short Circuit Duration		See (2)		
Supply Voltage ($V^+ − V^−$)			13.2	V
Voltage at Input pins			V^+ +0.5 V^- -0.5	V
Junction Temperature(3)			150	°C
Soldering Information	Infrared or Convection (20 sec.)		235	°C
	Wave Soldering (10 sec.)		260	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature at 150°C.
(3) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{θJA}$ and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} − T_A)/R_{θJA}$. All numbers apply for packages soldered directly onto a PC board.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		−65	150	°C
$V_{(ESD)}$	Electrostatic discharge(1)	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(2)		2000	V
		Machine model (MM)(3)		200	

(1) Human body model, 1.5 kΩ in series with 100 pF. Machine model: 0Ω in series with 100 pF.
(2) JEDEC document JEP155 states that 2000-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 200-V MM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions(1)

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply Voltage (V^+ - $V^−$)	±2.5		±6.0	V
Operating Temperature Range	−40		85	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics Table.

6.4 Thermal Information

THERMAL METRIC(1)		SOIC (D)	VSSOP (DGK)	SOT-23 (D)	UNIT
		8 PINS	8 PINS	5 PINS	
$R_{θJA}$	Junction-to-ambient thermal resistance	172	235	265	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 ±5V Electrical Characteristics

Unless otherwise specified, all limits ensured for V^+ = +5V, V^- = −5V, V_{CM} = 0V, A_V = +1, R_F = 25Ω for gain = +1, R_F = 402Ω for gain ≥ +2, and R_L = 100Ω. **Boldface** limits apply at the temperature extremes.

PARAMETER		TEST CONDITIONS	MIN [1]	TYP [2]	MAX [1]	UNIT
DYNAMIC PERFORMANCE						
f_{CL}	Close Loop Bandwidth	A_V = +1		250		MHz
		A_V = +2		130		
		A_V = +5		52		
		A_V = +10		26		
GBWP	Gain Bandwidth Product	A_V ≥ +5		260		MHz
	Bandwidth for 0.1 dB Flatness	A_V +1		18		MHz
φm	Phase Margin			50		deg
SR	Slew Rate [3]	A_V = +1, V_{IN} = 2 V_{PP}		200		V/µs
t_S	Settling Time 0.01%	A_V = +1, 2V Step		25		ns
	0.1%			15		ns
t_r	Rise Time	A_V = +1, 0.2V Step		1.4		ns
t_f	Fall Time	A_V = +1, 0.2V Step		1.2		ns
DISTORTION and NOISE RESPONSE						
e_n	Input Referred Voltage Noise	f ≥ 0.1 MHz		4.5		nV/√Hz
i_n	Input-Referred Current Noise	f ≥ 0.1 MHz		1.7		pA/√Hz
	Second Harmonic Distortion	A_V = +1, f = 5 MHz		−80		dBc
	Third Harmonic Distortion	V_O = 2 V_{PP}, R_L = 100Ω		−85		
X_t	Crosstalk (for LMH6655 only)	Input Referred, 5 MHz, Channel-to-Channel		−80		dB
DG	Differential Gain	A_V = +2, NTSC, R_L = 150Ω		0.01%		
DP	Differential Phase	A_V = +2, NTSC, R_L = 150Ω		0.025		deg
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	V_{CM} = 0V	−3 **−4**	±1	3 **4**	mV
TC V_{OS}	Input Offset Average Drift	V_{CM} = 0V [4]		6		µV/°C
I_B	Input Bias Current	V_{CM} = 0V		5	12 **18**	µA
I_{OS}	Input Offset Current	V_{CM} = 0V	−1 **−2**	0.3	1 **2**	µA
R_{IN}	Input Resistance	Common Mode		4		MΩ
		Differential Mode		20		kΩ
C_{IN}	Input Capacitance	Common Mode		1.8		pF
		Differential Mode		1		
CMRR	Common Mode Rejection Ration	Input Referred, V_{CM} = 0V to −5V	70 **68**	90		dB
CMVR	Input Common- Mode Voltage Range	CMRR ≥ 50 dB		−5.15	−5.0	V
			3.5	3.7		
TRANSFER CHARACTERISTICS						
A_{VOL}	Large Signal Voltage Gain	V_O = 4 V_{PP}, R_L = 100Ω	60 **58**	67		dB

(1) All limits are specified by testing or statistical analysis.
(2) Typical Values represent the most likely parametric norm.
(3) Slew rate is the slower of the rising and falling slew rates. Slew rate is rate of change from 10% to 90% of output voltage step.
(4) Offset voltage average drift is determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

±5V Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for V^+ = +5V, V^- = −5V, V_{CM} = 0V, A_V = +1, R_F = 25Ω for gain = +1, R_F = 402Ω for gain ≥ +2, and R_L = 100Ω. **Boldface** limits apply at the temperature extremes.

PARAMETER		TEST CONDITIONS	MIN (1)	TYP (2)	MAX (1)	UNIT
OUTPUT CHARACTERISTICS						
V_O	Output Swing High	No Load	3.4 **3.2**	3.6		V
	Output Swing Low	No Load		−3.9	−3.7 **−3.5**	
	Output Swing High	R_L = 100Ω	3.2 **3.0**	3.4		
	Output Swing Low	R_L = 100Ω		−3.6	−3.4 **−3.2**	
I_{SC}	Short Circuit Current (5)	Sourcing, V_O = 0V ΔV_{IN} = 200 mV	145 **130**	280		mA
		Sinking, V_O = 0V ΔV_{IN} = 200 mV	100 **80**	185		
I_{OUT}	Output Current	Sourcing, V_O = +3V		80		mA
		Sinking, V_O = −3V		120		
R_O	Output Resistance	A_V = +1, f <100 kHz		0.08		Ω
POWER SUPPLY						
PSRR	Power Supply Rejection Ratio	Input Referred, V_S = ±5V to ±6V	60	76		dB
I_S	Supply Current (per channel)			4.5	6 **7**	mA

(5) Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature at 150°C.

6.6 5V Electrical Characteristics

Unless otherwise specified, all limits ensured for V^+ = +5V, V^- = −0V, V_{CM} = 2.5V, A_V = +1, R_F = 25 Ω for gain = +1, R_F = 402Ω for gain ≥ +2, and R_L = 100Ω to $V^+/2$. **Boldface** limits apply at the temperature extremes.

PARAMETER		TEST CONDITIONS	MIN (1)	TYP (2)	MAX (1)	UNIT
DYNAMIC PERFORMANCE						
f_{CL}	Close Loop Bandwidth	A_V = +1		230		MHz
		A_V = +2		120		MHz
		A_V = +5		50		MHz
		A_V = +10		25		MHz
GBWP	Gain Bandwidth Product	A_V ≥ +5		250		MHz
	Bandwidth for 0.1 dB Flatness	A_V = +1		17		MHz
φm	Phase Margin			48		deg
SR	Slew Rate (3)	A_V = +1, V_{IN} = 2 V_{PP}		190		V/µs
t_S	Settling Time 0.01%	A_V = +1, 2V Step		30		ns
	0.1%			20		ns
t_r	Rise Time	A_V = +1, 0.2V Step		1.5		ns
t_f	Fall Time	A_V = +1, 0.2V Step		1.35		ns
DISTORTION and NOISE RESPONSE						
e_n	Input Referred Voltage Noise	f ≥ 0.1 MHz		4.5		nV/√Hz
i_n	Input Referred Current Noise	f ≥ 0.1 MHz		1.7		pA/√Hz
	Second Harmonic Distortion	A_V = +1, f = 5 MHz		−65		dBc
	Third Harmonic Distortion	V_O = 2 V_{PP}, R_L = 100Ω		−70		dBc
X_t	Crosstalk (for LMH6655 only)	Input Referred, 5 MHz		−78		dB
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	V_{CM} = 2.5V	−5 **−6.5**	±2	5 **6.5**	mV
TC V_{OS}	Input Offset Average Drift	V_{CM} = 2.5V (4)		**6**		µV/°C
I_B	Input Bias Current	V_{CM} = 2.5V		6	12 **18**	µA
I_{OS}	Input Offset Current	V_{CM} = 2.5V	−2 **−3**	0.5	2 **3**	µA
R_{IN}	Input Resistance	Common Mode		4		MΩ
		Differential Mode		20		kΩ
C_{IN}	Input Capacitance	Common Mode		1.8		pF
		Differential Mode		1		pF
CMRR	Common Mode Rejection Ration	Input Referred, V_{CM} = 0V to −2.5V	70 **68**	90		dB
CMVR	Input Common Mode Voltage Range	CMRR ≥ 50 dB		−0.15	0	V
			3.5	3.7		V
TRANSFER CHARACTERISTICS						
A_{VOL}	Large Signal Voltage Gain	V_O = 1.6 V_{PP}, R_L = 100Ω	58 **55**	64		dB

(1) All limits are specified by testing or statistical analysis.
(2) Typical Values represent the most likely parametric norm.
(3) Slew rate is the slower of the rising and falling slew rates. Slew rate is rate of change from 10% to 90% of output voltage step.
(4) Offset voltage average drift is determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

5V Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for $V^+ = +5V$, $V^- = -0V$, $V_{CM} = 2.5V$, $A_V = +1$, $R_F = 25\ \Omega$ for gain = +1, $R_F = 402\Omega$ for gain ≥ +2, and $R_L = 100\Omega$ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
OUTPUT CHARACTERISTICS						
V_O	Output Swing High	No Load	3.6 **3.4**	3.75		V
	Output Swing Low	No Load		0.9	1.1 **1.3**	
	Output Swing High	$R_L = 100\Omega$	3.5 **3.35**	3.70		
	Output Swing Low	$R_L = 100\Omega$		1	1.3 **1.45**	
I_{SC}	Short Circuit Current (5)	Sourcing , $V_O = 2.5V$ $\Delta V_{IN} = 200$ mV	90 **80**	170		mA
		Sinking, $V_O = 2.5V$ $\Delta V_{IN} = 200$ mV	70 **60**	140		
I_{OUT}	Output Current	Sourcing, $V_O = +3.5V$		30		mA
		Sinking, $V_O = 1.5V$		60		
R_O	Output Resistance	$A_V = +1$, f <100 kHz		.08		Ω
POWER SUPPLY						
PSRR	Power Supply Rejection Ratio	Input Referred , $V_S = \pm 2.5V$ to $\pm 3V$	60	75		dB
I_S	Supply Current (per channel)			4.5	6 **7**	mA

(5) Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature at 150°C.

6.7 Typical Characteristics

25°C, $V^+ = \pm 5$ V, $V^- = -5$, $R_F = 25\ \Omega$ for gain = +1, $R_F = 402\ \Omega$ for gain ≥ +2 and $R_L = 100\ \Omega$, unless otherwise specified.

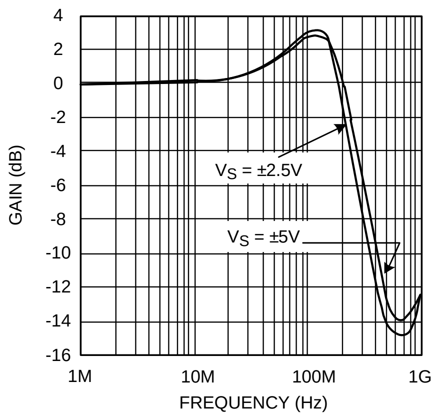


Figure 2. Closed Loop Bandwidth (G = +1)

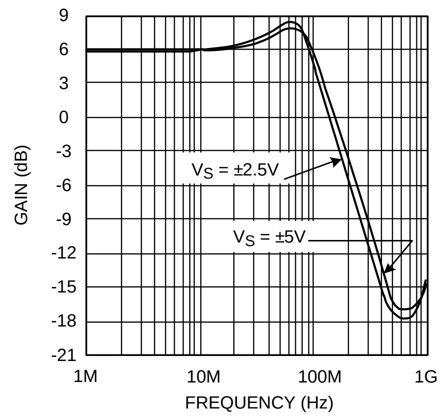


Figure 3. Closed Loop Bandwidth (G = +2)

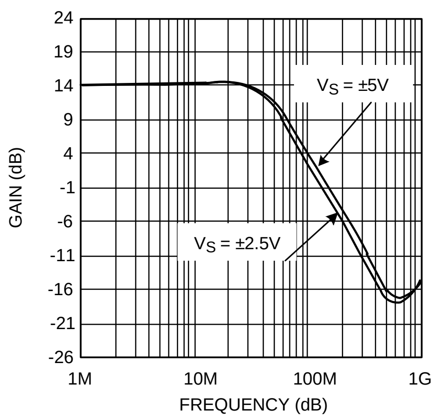


Figure 4. Closed Loop Bandwidth (G = +5)

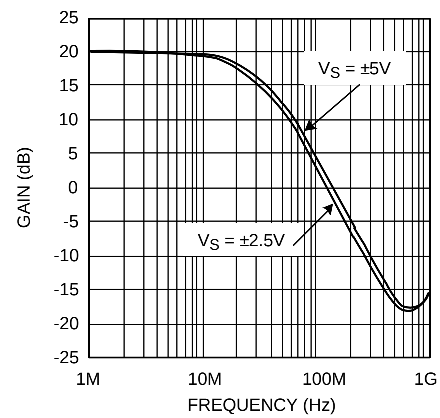


Figure 5. Closed Loop Bandwidth (G = +10)

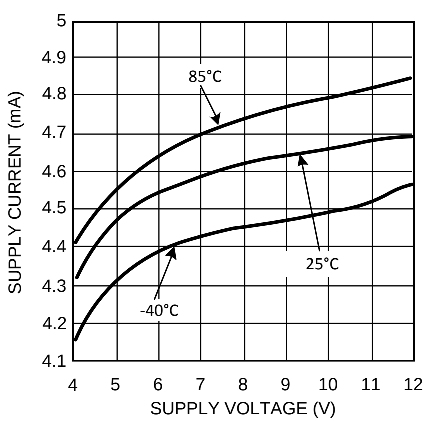


Figure 6. Supply Current per Channel vs. Supply Voltage

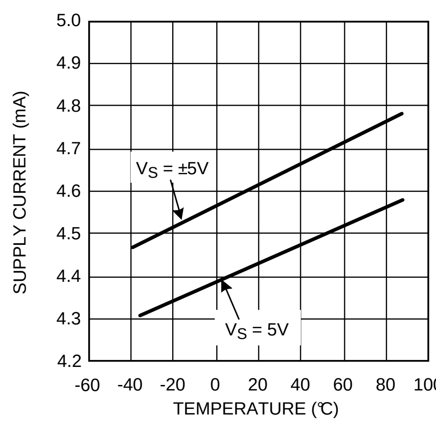


Figure 7. Supply Current per Channel vs. Temperature

Typical Characteristics (continued)

25°C, $V^+ = \pm 5$ V, $V^- = -5$, $R_F = 25\ \Omega$ for gain = +1, $R_F = 402\ \Omega$ for gain ≥ +2 and $R_L = 100\ \Omega$, unless otherwise specified.

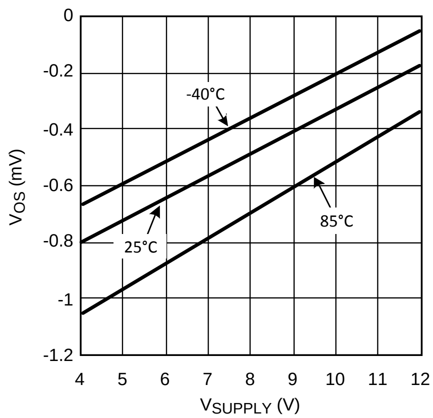


Figure 8. Offset Voltage vs. Supply Voltage (V_{CM} = 0V)

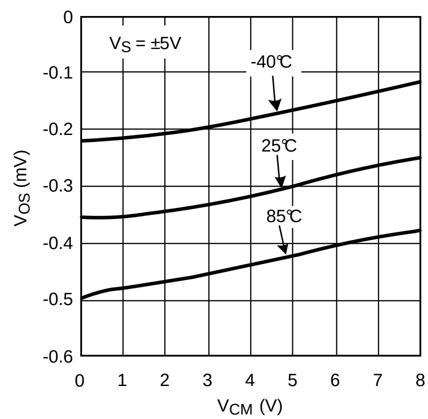


Figure 9. Offset Voltage vs. Common Mode

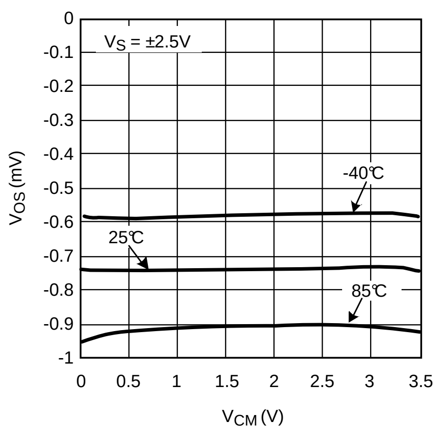


Figure 10. Offset Voltage vs. Common Mode

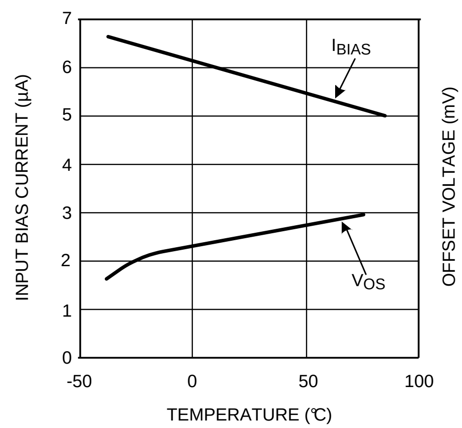


Figure 11. Bias Current and Offset Voltage vs. Temperature

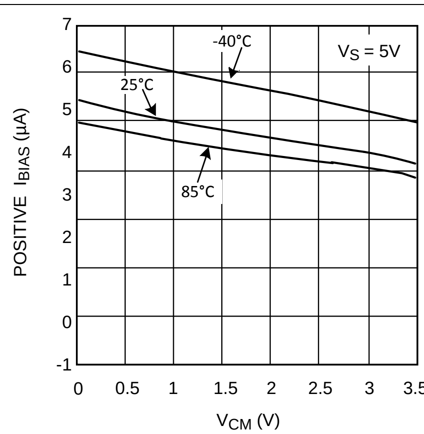


Figure 12. Bias Current vs. Common Mode Voltage

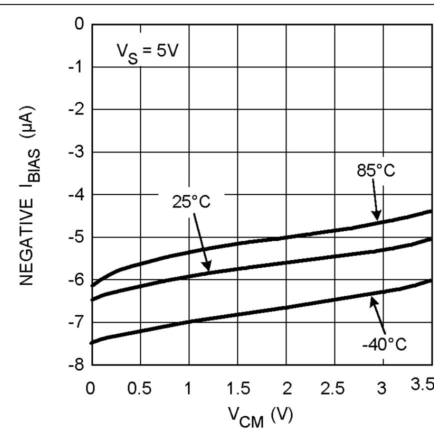


Figure 13. Bias Current vs. Common Mode Voltage

Typical Characteristics (continued)

25°C, V^{+} = ±5 V, V^{-} = −5, R_F = 25 Ω for gain = +1, R_F = 402 Ω for gain ≥ +2 and R_L = 100 Ω, unless otherwise specified.

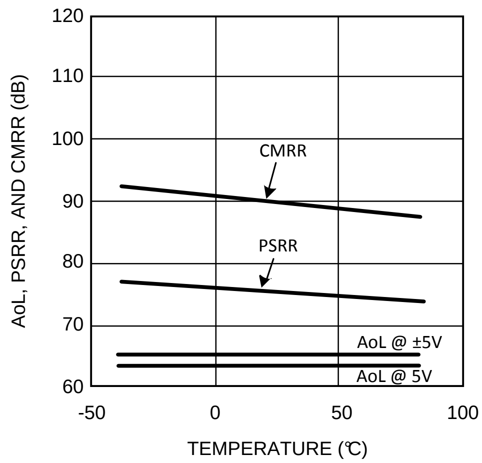


Figure 14. A_{OL}, PSRR and CMRR vs. Temperature

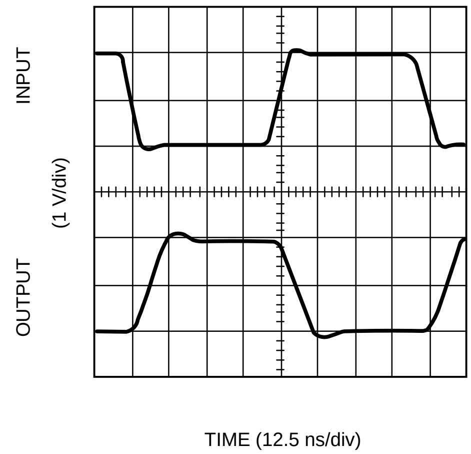


Figure 15. Inverting Large Signal Pulse Response (V_S = 5V)

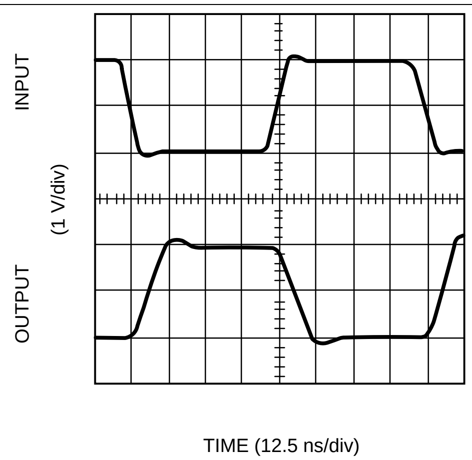


Figure 16. Inverting Large Signal Pulse Response (V_S = ±5V)

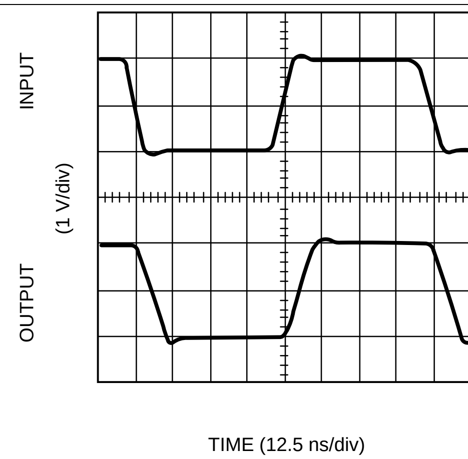


Figure 17. Non-Inverting Large Signal Pulse Response (V_S = 5V)

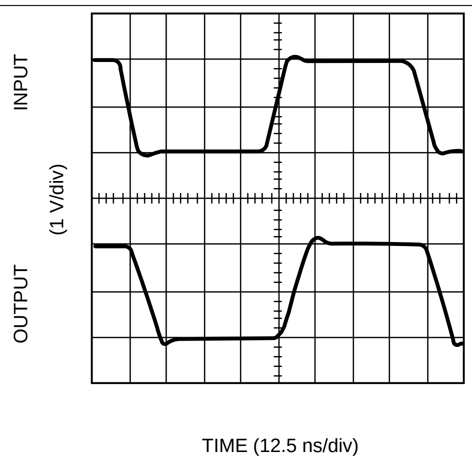


Figure 18. Non-Inverting Large Signal Pulse Response (V_S = ±5V)

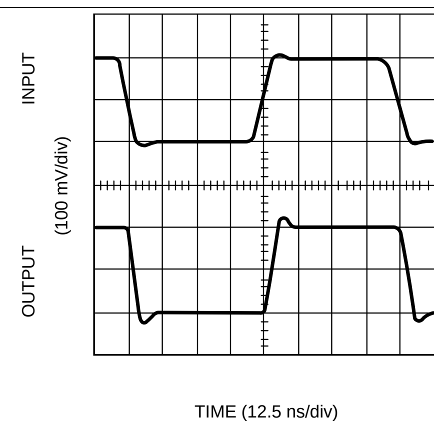


Figure 19. Non-Inverting Small Signal Pulse Response (V_S = 5V)

Typical Characteristics (continued)

25°C, $V^+ = \pm 5$ V, $V^- = -5$, $R_F = 25\ \Omega$ for gain = +1, $R_F = 402\ \Omega$ for gain ≥ +2 and $R_L = 100\ \Omega$, unless otherwise specified.

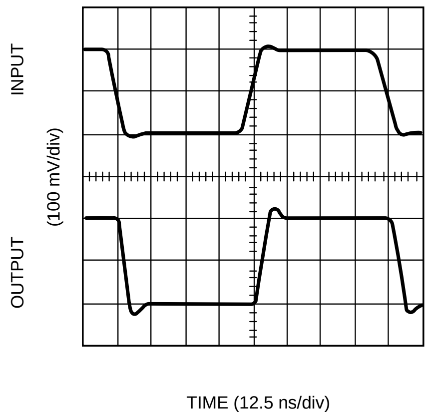


Figure 20. Non-Inverting Small Signal Pulse Response ($V_S = \pm 5V$)

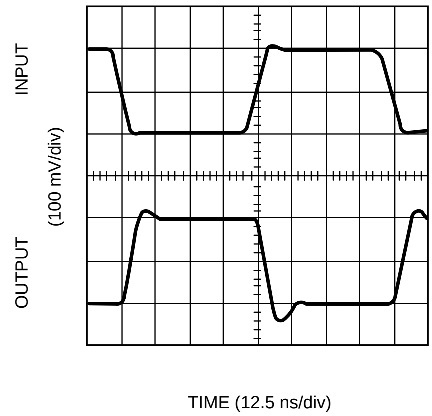


Figure 21. Inverting Small Signal Pulse Response ($V_S = 5V$)

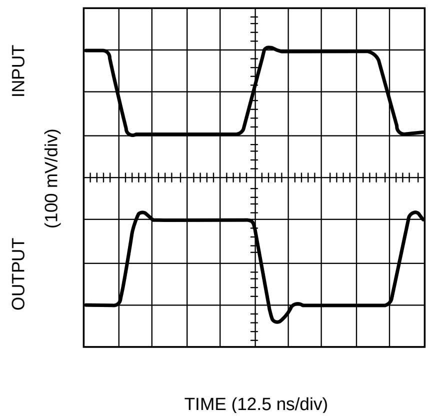


Figure 22. Inverting Small Signal Pulse Response ($V_S = \pm 5V$)

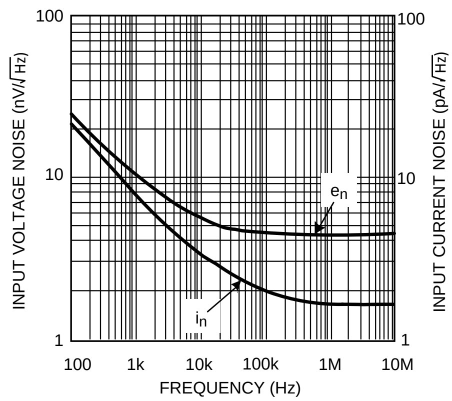


Figure 23. Input Voltage and Current Noise vs. Frequency ($V_S = 5V$)

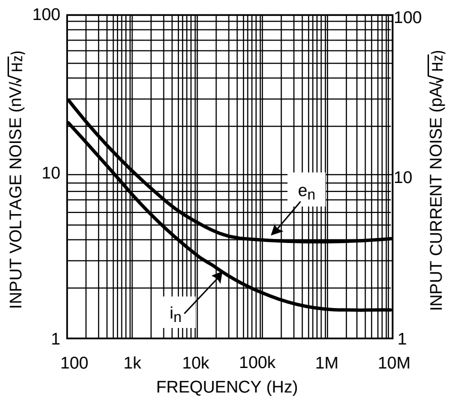


Figure 24. Input Voltage and Current Noise vs. Frequency ($V_S = \pm 5V$)

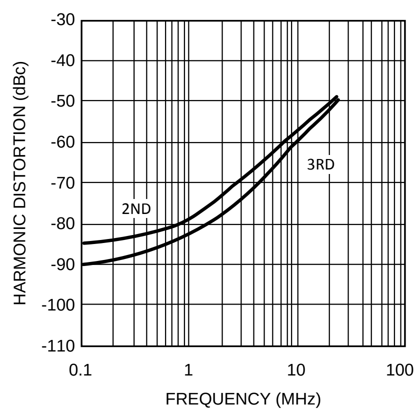


Figure 25. Harmonic Distortion vs. Frequency G = +1, $V_O = 2\ V_{PP}$, $V_S = 5V$

Typical Characteristics (continued)

25°C, V^+ = ±5 V, V^- = −5, R_F = 25 Ω for gain = +1, R_F = 402 Ω for gain ≥ +2 and R_L = 100 Ω, unless otherwise specified.

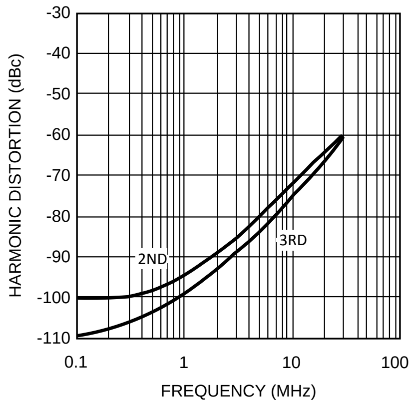


Figure 26. Harmonic Distortion vs. Frequency G = +1, V_O = 2 V_{PP}, V_S = ±5V

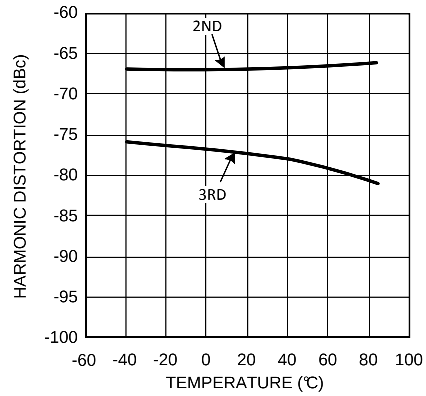


Figure 27. Harmonic Distortion vs. Temperature V_S = 5V, f = 5 MHz, V_O = 2 V_{PP}

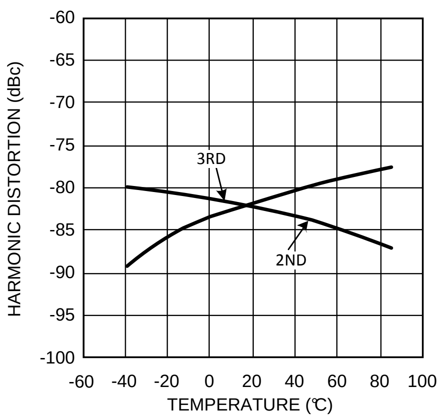


Figure 28. Harmonic Distortion vs. Temperature V_S = ±5V, f = 5 MHz, V_O = 2 V_{PP}

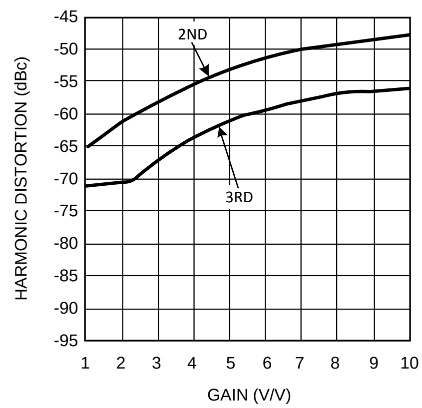


Figure 29. Harmonic Distortion vs. Gain V_S = 5V, f = 5 MHz, V_O = 2 V_{PP}

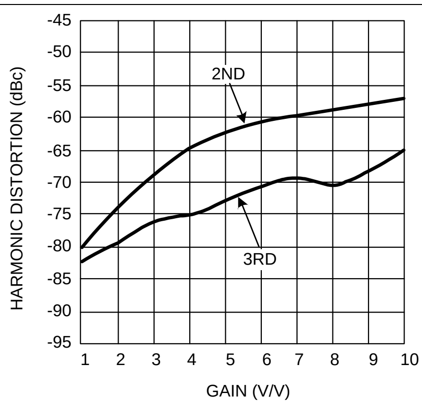


Figure 30. Harmonic Distortion vs. Gain V_S = ±5V, f = 5 MHz, V_O = 2 V_{PP}

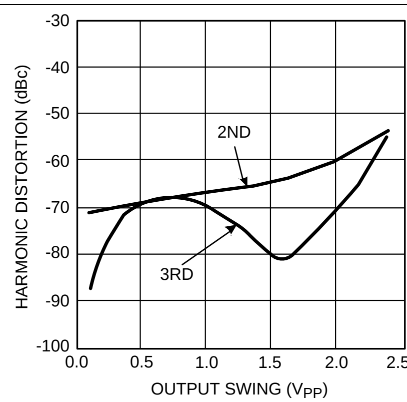


Figure 31. Harmonic Distortion vs. Output Swing (G = +2, V_S = 5V, f = 5 MHz)

Typical Characteristics (continued)

25°C, V^+ = ±5 V, V^- = −5, R_F = 25 Ω for gain = +1, R_F = 402 Ω for gain ≥ +2 and R_L = 100 Ω, unless otherwise specified.

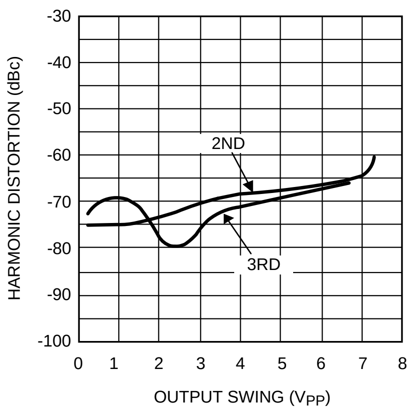


Figure 32. Harmonic Distortion vs. Output Swing (G = +2, V_S = ±5V, f = 5 MHz)

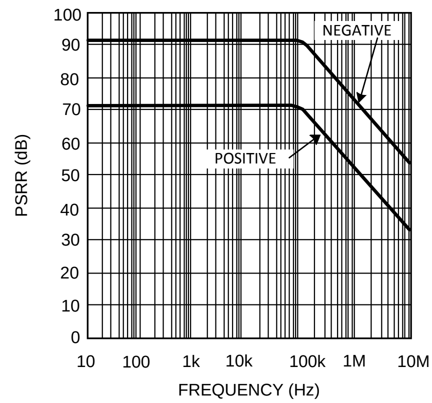


Figure 33. PSRR vs. Frequency

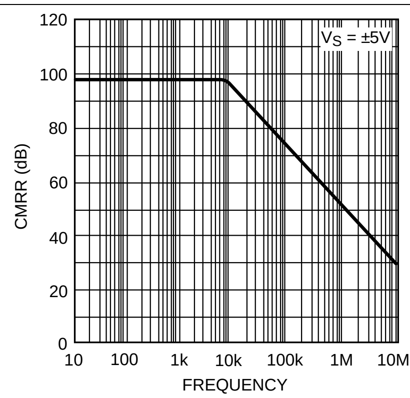


Figure 34. CMRR vs. Frequency

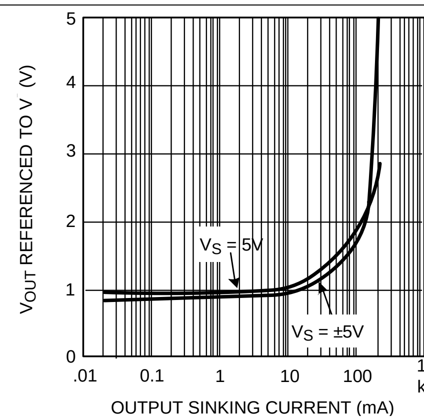


Figure 35. Output Sinking Current

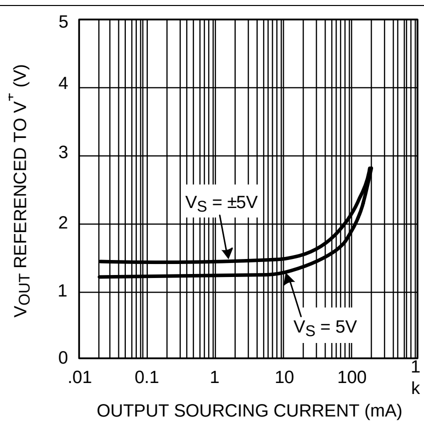


Figure 36. Output Sourcing Current

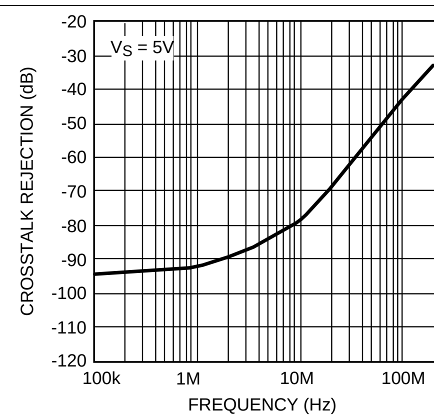


Figure 37. CrossTalk vs. Frequency (LMH6655 only)

Typical Characteristics (continued)

25°C, $V^+ = \pm 5$ V, $V^- = -5$, $R_F = 25\ \Omega$ for gain = +1, $R_F = 402\ \Omega$ for gain ≥ +2 and $R_L = 100\ \Omega$, unless otherwise specified.

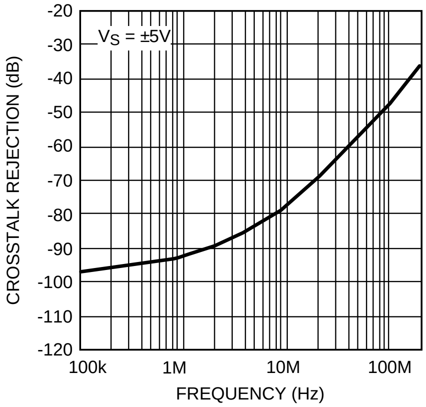


Figure 38. CrossTalk vs. Frequency (LMH6655 only)

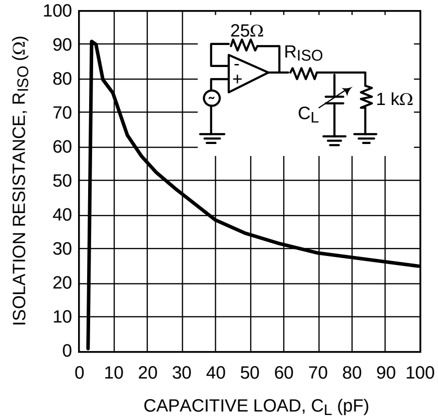


Figure 39. Isolation Resistance vs. Capacitive Load

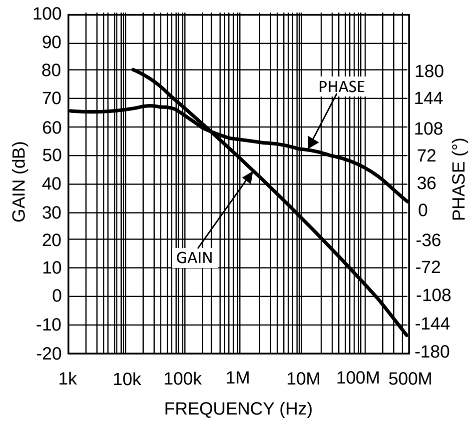


Figure 40. Open Loop Gain and Phase vs. Frequency

7 Application and Implementation

7.1 Application Information

The LMH6654 single and LMH6655 dual high speed, voltage feedback amplifiers are manufactured on TI's new VIP10™ (Vertically Integrated PNP) complementary bipolar process. These amplifiers can operate from ±2.5 V to ±6 V power supply. They offer low supply current, wide bandwidth, very low voltage noise and large output swing. Many of the typical performance plots found in the datasheet can be reproduced if 50 Ω coax and 50 Ω R_{IN}/R_{OUT} resistors are used.

7.2 Typical Application

7.2.1 Design Requirements

7.2.1.1 Components Selection and Feedback Resistor

It is important in high-speed applications to keep all component leads short since wires are inductive at high frequency. For discrete components, choose carbon composition axially leaded resistors and micro type capacitors. Surface mount components are preferred over discrete components for minimum inductive effect. Never use wire wound type resistors in high frequency applications.

Large values of feedback resistors can couple with parasitic capacitance and cause undesired effects such as ringing or oscillation in high-speed amplifiers. Keep resistors as low as possible consistent with output loading consideration. For a gain of 2 and higher, 402 Ω feedback resistor used for the typical performance plots gives optimal performance. For unity gain follower, a 25 Ω feedback resistor is recommended rather than a direct short. This effectively reduces the Q of what would otherwise be a parasitic inductance (the feedback wire) into the parasitic capacitance at the inverting input.

7.2.2 Detailed Design Procedure

7.2.2.1 Driving Capacitive Loads

Capacitive loads decrease the phase margin of all op amps. The output impedance of a feedback amplifier becomes inductive at high frequencies, creating a resonant circuit when the load is capacitive. This can lead to overshoot, ringing and oscillation. To eliminate oscillation or reduce ringing, an isolation resistor can be placed as shown in Figure 41 below. At frequencies above

$$F = \frac{1}{2\pi R_{ISO} C_{LOAD}} \quad (1)$$

the load impedance of the Amplifier approaches R_{ISO}. The desired performance depends on the value of the isolation resistor. The isolation resistance vs. capacitance load graph in the typical performance characteristics provides the means for selection of the value of R_S that provides ≤ 3 dB peaking in closed loop $A_V = 1$ response. In general, the bigger the isolation resistor, the more damped the pulse response becomes. For initial evaluation, a 50Ω isolation resistor is recommended.

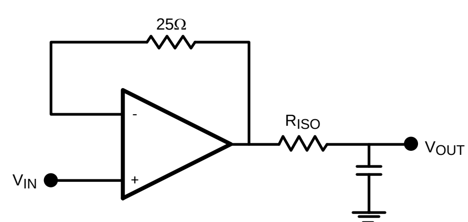


Figure 41. Isolation Resistor Placement

Typical Application (continued)

7.2.2.2 Bias Current Cancellation

In order to cancel the bias current errors of the non-inverting configuration, the parallel combination of the gain setting R_g and feedback R_f resistors should equal the equivalent source resistance R_{seq} as defined in Figure 42. Combining this constraint with the non-inverting gain equation, allows both R_f and R_g to be determined explicitly from the following equations:

$$R_f = A_V R_{seq} \text{ and } R_g = R_f/(A_V - 1) \quad (2)$$

For inverting configuration, bias current cancellation is accomplished by placing a resistor R_b on the non-inverting input equal in value to the resistance seen by the inverting input (R_f//(R_g+R_s). The additional noise contribution of R_b can be minimized through the use of a shunt capacitor.

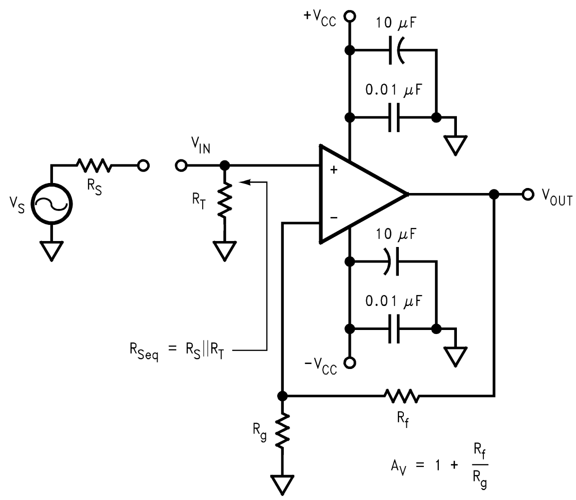


Figure 42. Non-Inverting Amplifier Configuration

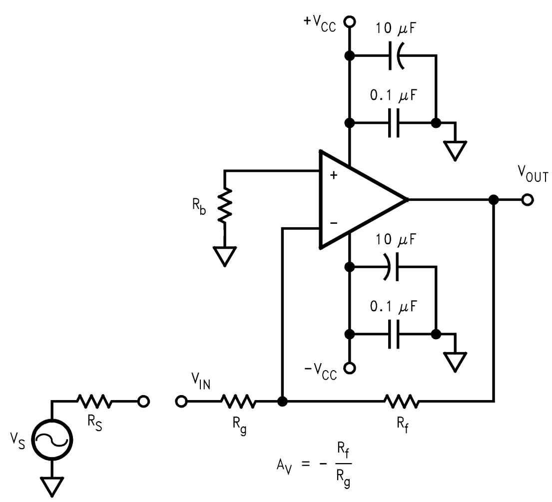


Figure 43. Inverting Amplifier Configuration

Typical Application (continued)

7.2.2.3 Total Input Noise vs. Source Resistance

The noise model for the non-inverting amplifier configuration showing all noise sources is described in Figure 44. In addition to the intrinsic input voltage noise (e_n) and current noise ($i_n = i_{n+} = i_{n-}$) sources, there also exits thermal voltage noise $e_t = \sqrt{4kTR}$ associated with each of the external resistors. Equation 3 provides the general form for total equivalent input voltage noise density (e_{ni}). Equation 4 is a simplification of Equation 3 that assumes $R_f \parallel R_g = R_{seq}$ for bias current cancellation. Figure 45 illustrates the equivalent noise model using this assumption. The total equivalent output voltage noise (e_{no}) is e_{ni} * A_V.

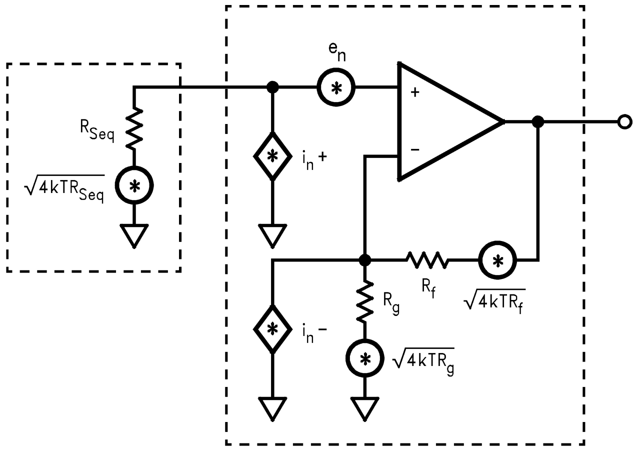


Figure 44. Non-Inverting Amplifier Noise Model

$$e_{ni} = \sqrt{e_n^2 + (i_{n+} \cdot R_{Seq})^2 + 4kTR_{Seq} + (i_{n-} \cdot (R_f \parallel R_g))^2 + 4kT(R_f \parallel R_g)} \quad (3)$$

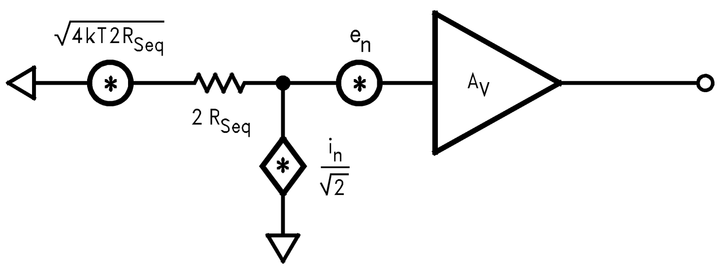


Figure 45. Noise Model with $R_f \parallel R_g = R_{seq}$

$$e_{ni} = \sqrt{e_n^2 + 2\,(i_n \cdot R_{Seq})^2 + 4kT\,(2R_{Seq})} \quad (4)$$

If bias current cancellation is not a requirement, then $R_f \parallel R_g$ does not need to equal R_{seq}. In this case, according to Equation 3, R_f and R_g should be as low as possible in order to minimize noise. Results similar to Equation 3 are obtained for the inverting configuration on if R_{seq} is replaced by $R_b \parallel R_g$ is replaced by $R_g + R_s$. With these substitutions, Equation 3 will yield an e_{ni} referred to the non-inverting input. Referring e_{ni} to the inverting input is easily accomplished by multiplying e_{ni} by the ratio of non-inverting to inverting gains.

Typical Application (continued)

7.2.2.3.1 Noise Figure

Noise Figure (NF) is a measure of the noise degradation caused by an amplifier.

$$NF = 10LOG\left[\frac{S_i/N_i}{S_o/N_o}\right] = 10LOG\left[\frac{e_{ni}^2}{e_t^2}\right] \quad (5)$$

The noise figure formula is shown in Equation 5. The addition of a terminating resistor R_T, reduces the external thermal noise but increases the resulting NF.

The NF is increased because the R_T reduces the input signal amplitude thus reducing the input SNR.

$$\left[\frac{e_n^2 + i_n^2 (R_{Seq} + (R_f \parallel R_g))^2 + 4KTR_{Seq} + 4kt (R_f \parallel R_g)}{4kTR_{Seq}}\right] \quad (6)$$

The noise figure is related to the equivalent source resistance (R_{seq}) and the parallel combination of R_f and R_g. To minimize noise figure, the following steps are recommended:

1. Minimize $R_f||R_g$
2. Choose the Optimum R_s (R_{OPT})

R_{OPT} is the point at which the NF curve reaches a minimum and is approximated by:

$R_{OPT} \approx (e_n/i_n)$

8 Power Supply Recommendations

8.1 Power Dissipation

The package power dissipation should be taken into account when operating at high ambient temperature and/or high power dissipative conditions. In determining maximum operable temperature of the device, make sure the total power dissipation of the device is considered; this power dissipated in the device with a load connected to the output as well as the nominal dissipation of the op amp.

9 Layout

9.1 Layout Guidelines

With all high frequency devices, board layouts with stray capacitance have a strong influence on the AC performance. The LMH6654/LMH6655 are not exception and the inverting input and output pins are particularly sensitive to the coupling of parasitic capacitance to AC ground. Parasitic capacitances on the inverting input and output nodes to ground could cause frequency response peaking and possible circuit oscillation. Therefore, the power supply, ground traces and ground plan should be placed away from the inverting input and output pins. Also, it is very important to keep the parasitic capacitance across the feedback to an absolute minimum.

The PCB should have a ground plane covering all unused portion of the component side of the board to provide a low impedance path. All trace lengths should be minimized to reduce series inductance.

Supply bypassing is required for the amplifiers performance. The bypass capacitors provide a low impedance return current path at the supply pins. They also provide high frequency filtering on the power supply traces. It is recommended that a ceramic decoupling capacitor 0.1 µF chip should be placed with one end connected to the ground plane and the other side as close as possible to the power pins. An additional 10 µF tantalum electrolytic capacitor should be connected in parallel, to supply current for fast large signal changes at the output.

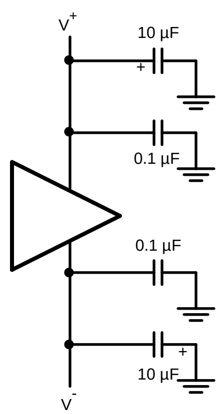


Figure 46. Supply Bypass Capacitors

9.1.1 Evaluation Boards

TI provides the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization.

DEVICE	PACKAGE	EVALUATION BOARD PN
LMH6654MF	5-Pin SOT-23	LMH730216
LMH6654MA	8-Pin SOIC	LMH730227
LMH6655MA	8-Pin SOIC	LMH730036
LMH6655MM	8-Pin VSSOP (DGK)	LMH730123

Components Needed to Evaluate the LMH6654 on the LMH730227 Evaluation Board:

- R_f, R_g use the datasheet to select values.
- R_{IN}, R_{OUT} typically 50 Ω (Refer to the Basic Operation section of the evaluation board datasheet for details)
- R_f is an optional resistor for inverting again configurations (select R_f to yield desired input impedance = $R_g||R_f$)
- C_1, C_2 use 0.1 µF ceramic capacitors
- C_3, C_4 use 10 µF tantalum capacitors

Components not used:

1. C_5, C_6, C_7, C_8
2. R1 thru R8

The evaluation boards are designed to accommodate dual supplies. The board can be modified to provide single operation. For best performance;

1) Do not connect the unused supply.

2) Ground the unused supply pin.

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

10.1.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LMH6654	Click here	Click here	Click here	Click here	Click here
LMH6655	Click here	Click here	Click here	Click here	Click here

10.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

10.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMH6654MA/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMH66 54MA
LMH6654MA/NOPB.A	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMH66 54MA
LMH6654MAX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMH66 54MA
LMH6654MAX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMH66 54MA
LMH6654MF/NOPB	Active	Production	SOT-23 (DBV) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A66A
LMH6654MF/NOPB.A	Active	Production	SOT-23 (DBV) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A66A
LMH6654MFX/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A66A
LMH6654MFX/NOPB.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A66A
LMH6655MA/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMH66 55MA
LMH6655MA/NOPB.A	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMH66 55MA
LMH6655MAX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMH66 55MA
LMH6655MAX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMH66 55MA
LMH6655MM/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A67A
LMH6655MM/NOPB.A	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A67A
LMH6655MMX/NOPB	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A67A
LMH6655MMX/NOPB.A	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A67A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[4] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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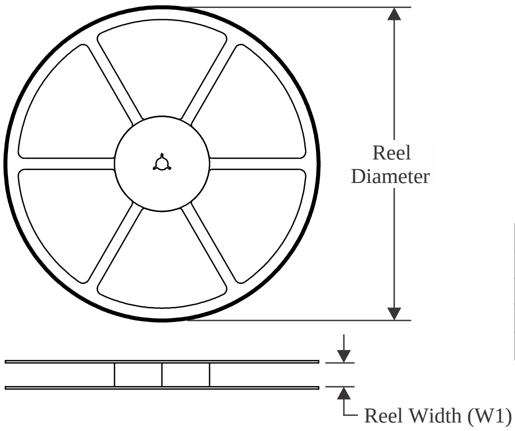
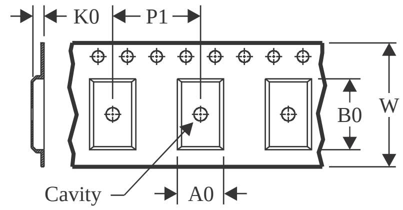
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

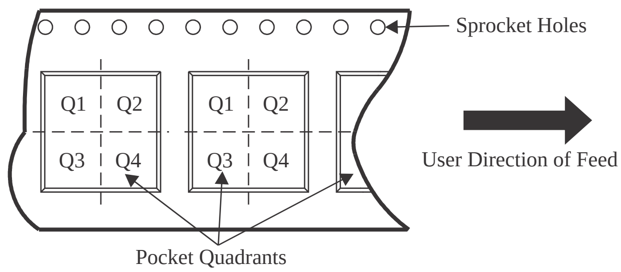


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

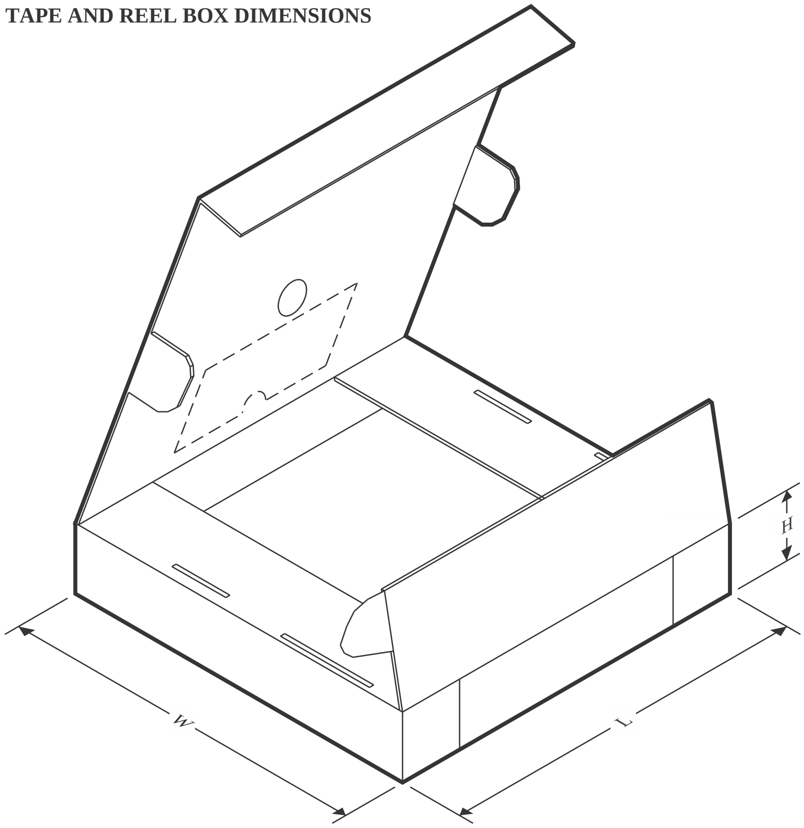
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6654MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6654MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6654MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6655MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6655MM/NOPB	VSSOP	DGK	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMH6655MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

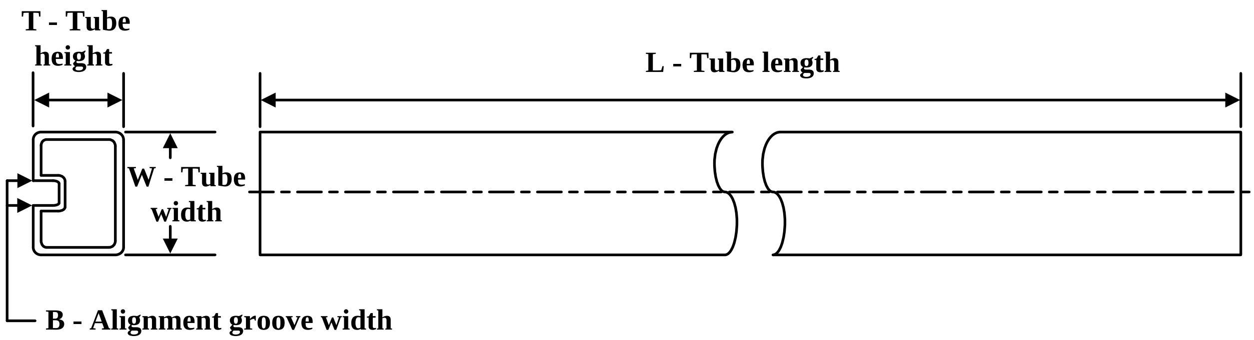
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

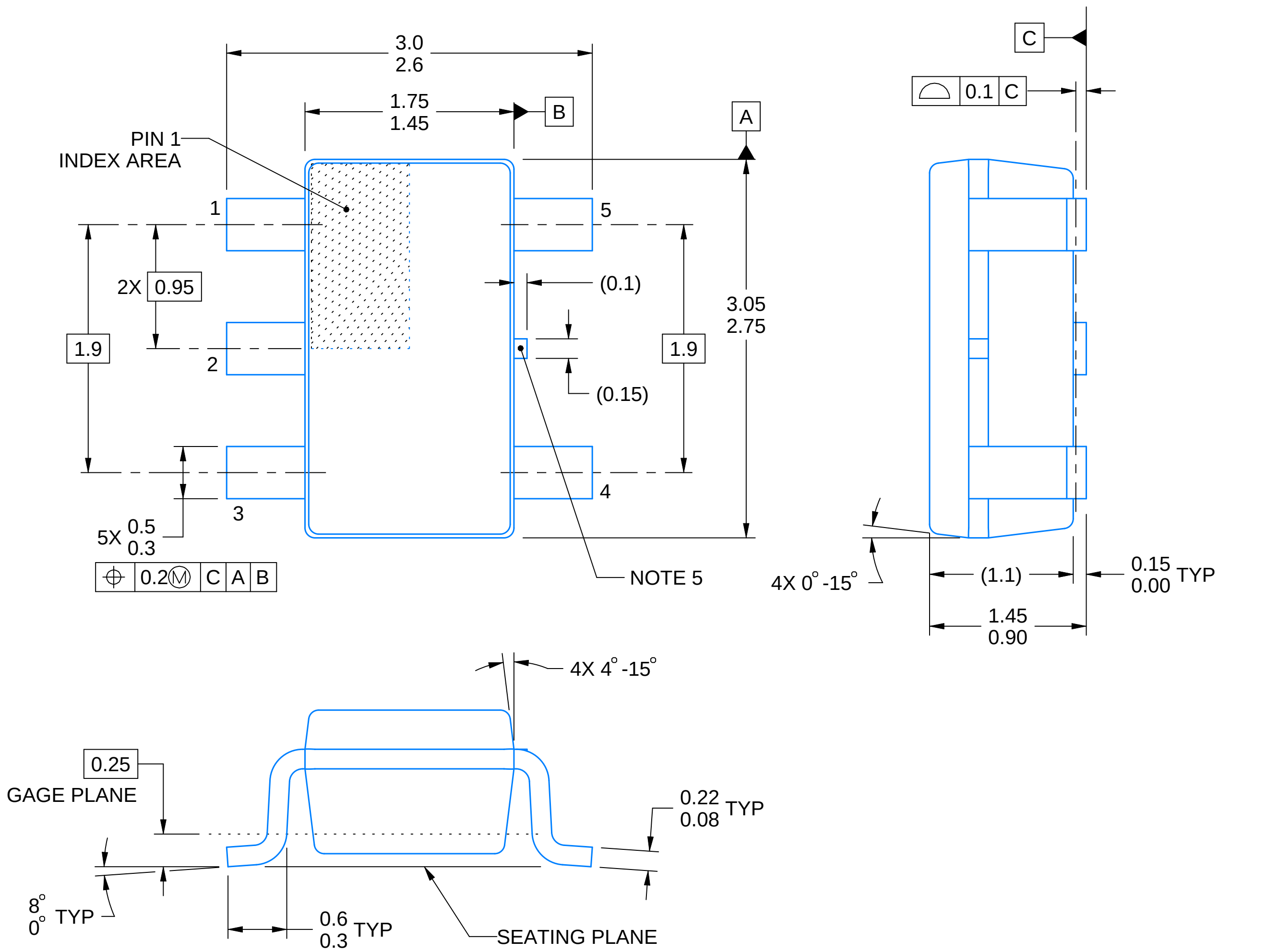
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6654MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMH6654MF/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LMH6654MFX/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LMH6655MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMH6655MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LMH6655MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

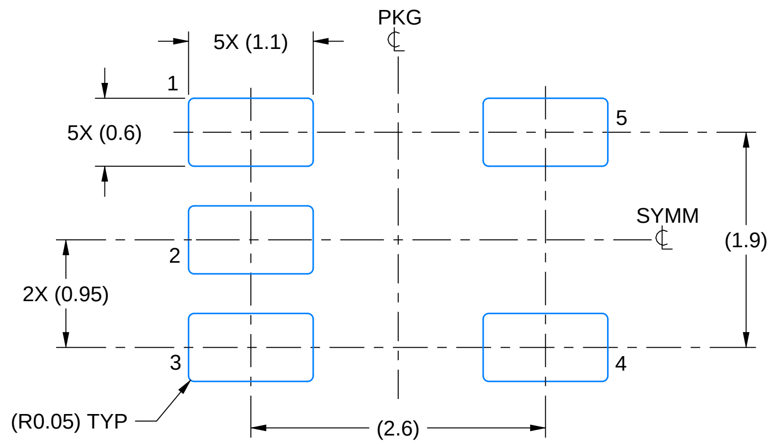
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMH6654MA/NOPB	D	SOIC	8	95	495	8	4064	3.05
LMH6654MA/NOPB.A	D	SOIC	8	95	495	8	4064	3.05
LMH6655MA/NOPB	D	SOIC	8	95	495	8	4064	3.05
LMH6655MA/NOPB.A	D	SOIC	8	95	495	8	4064	3.05



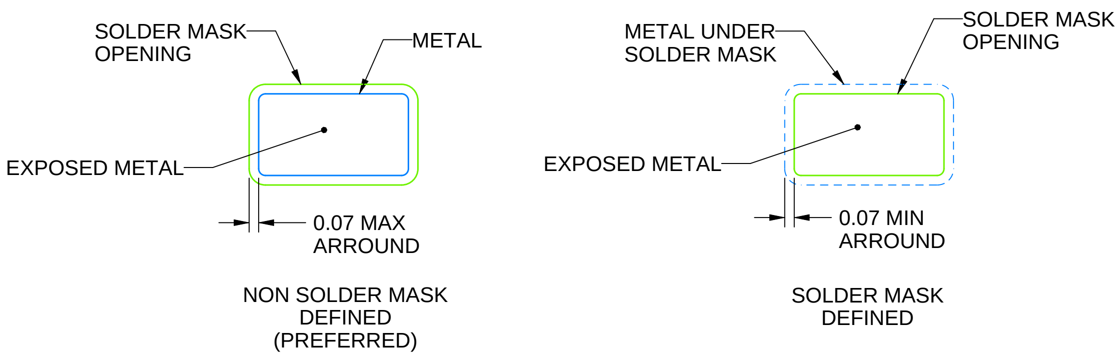
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

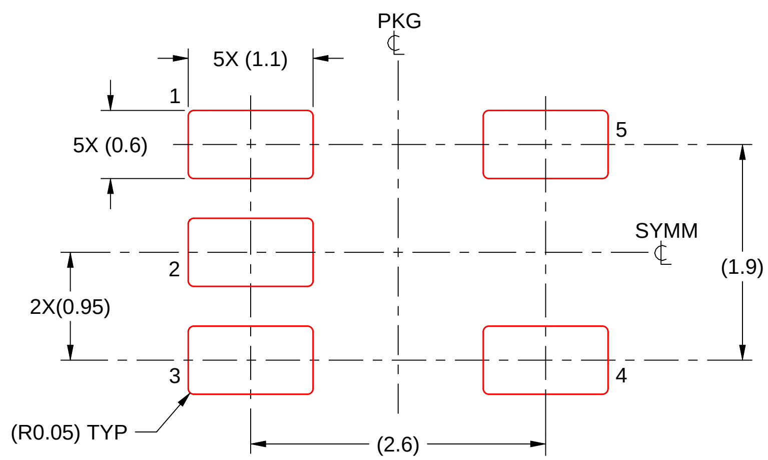


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



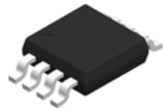
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

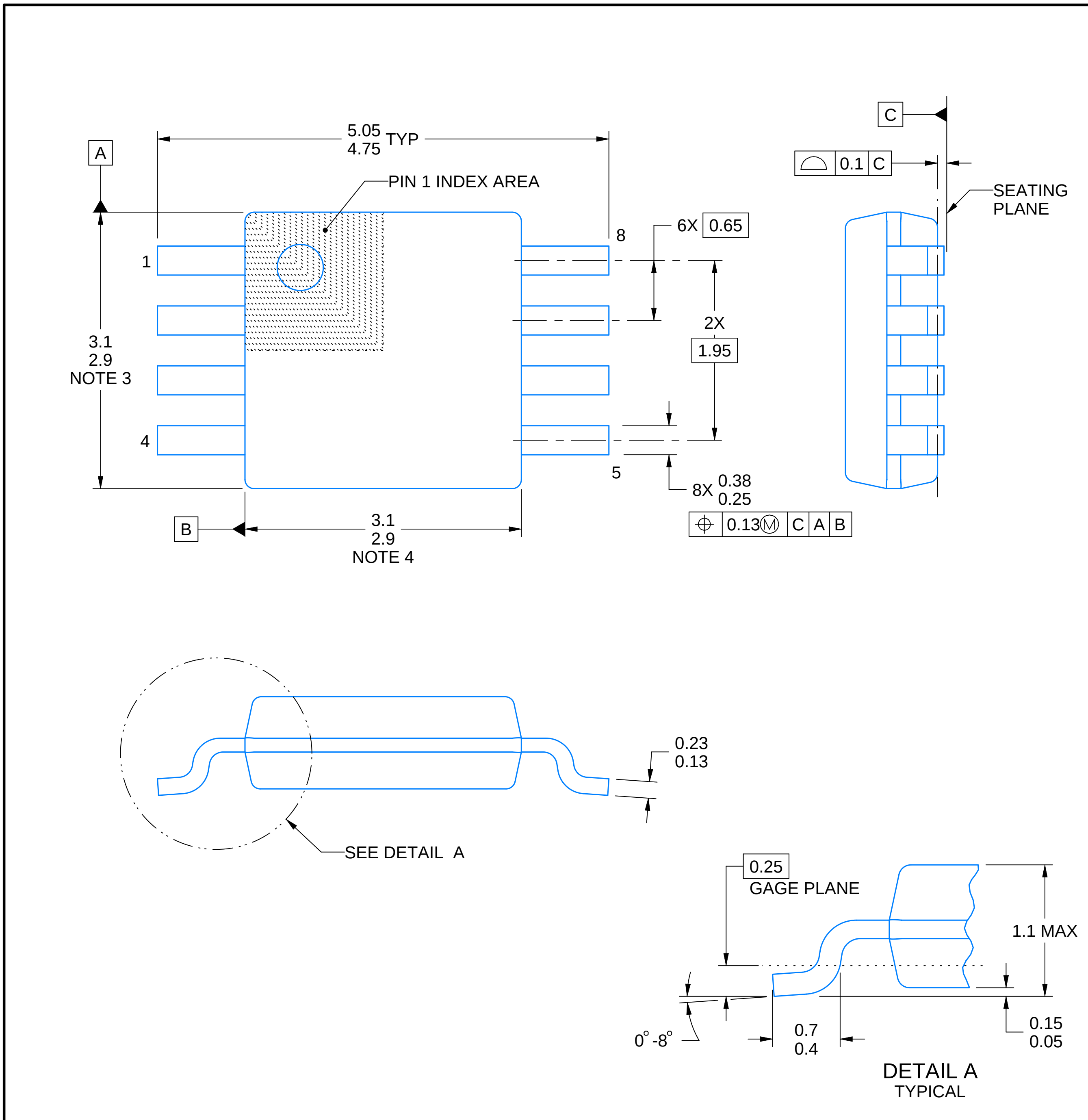
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK0008A



VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

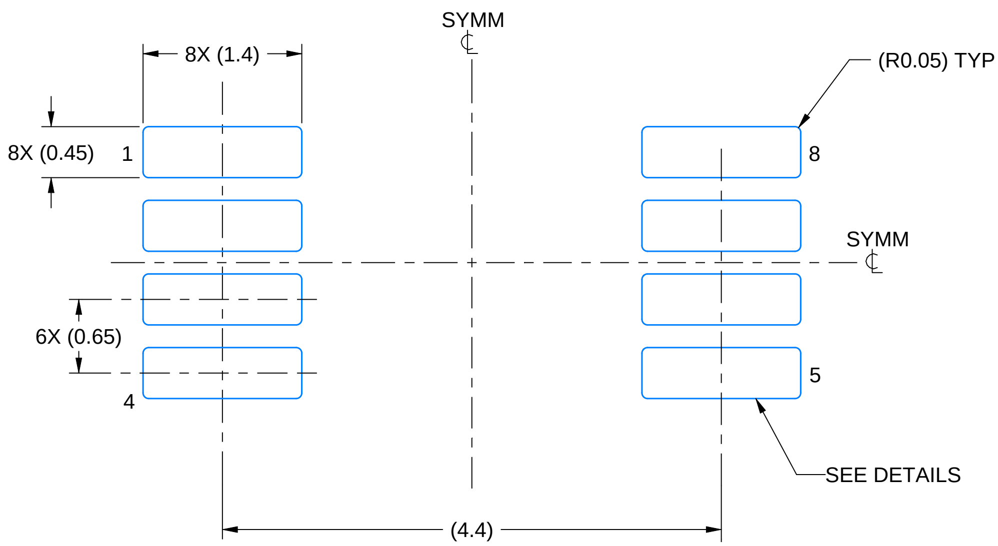


4214862/A 04/2023

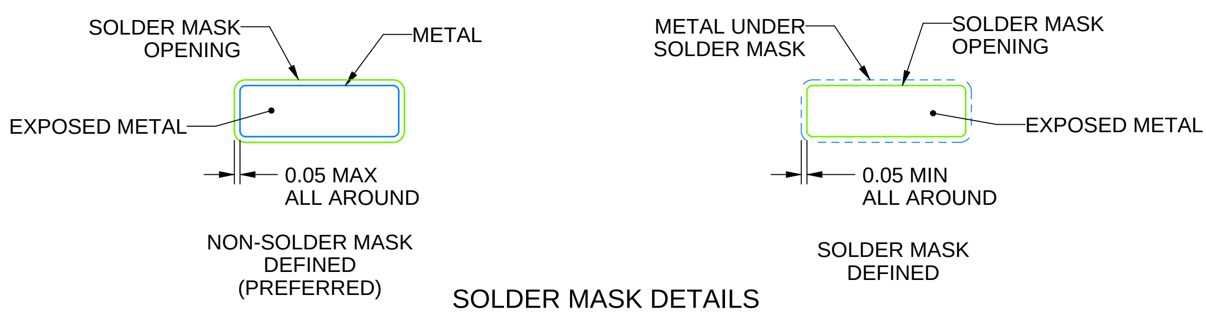
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

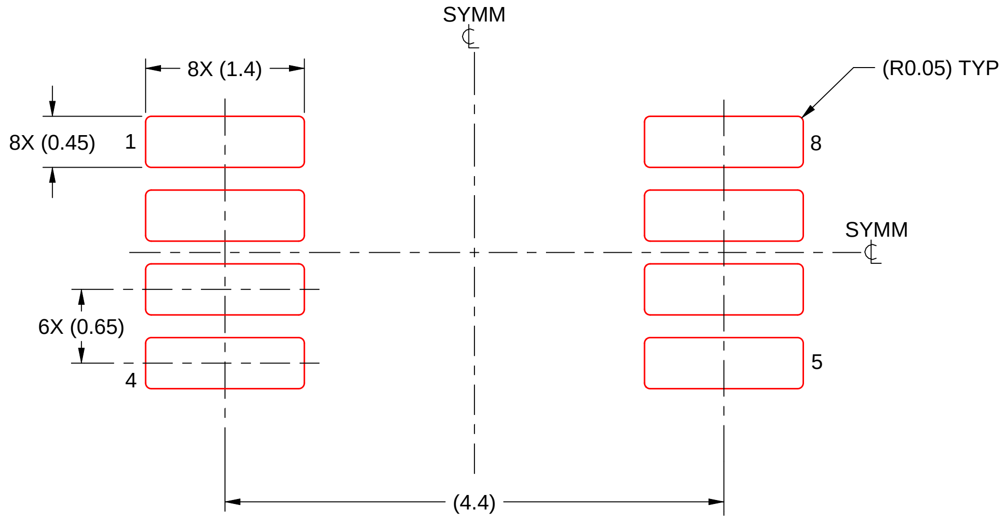


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

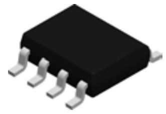


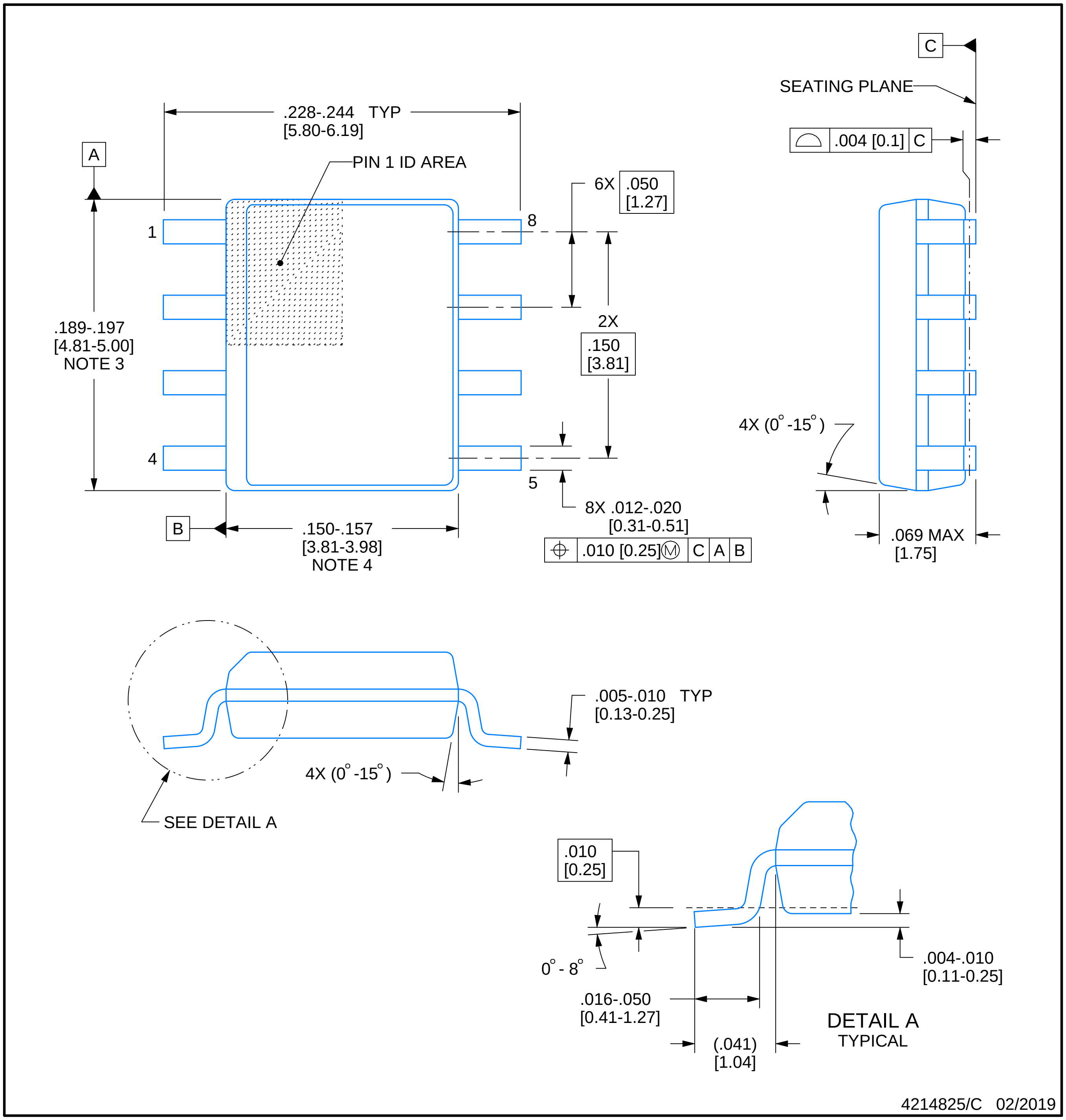
SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

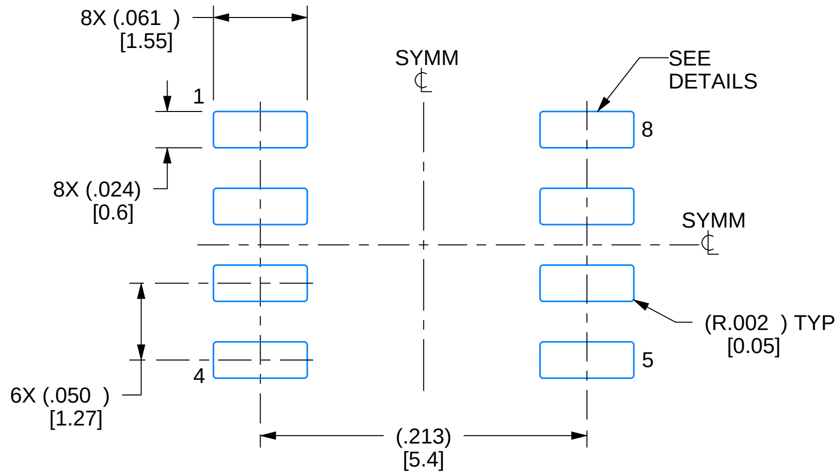
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



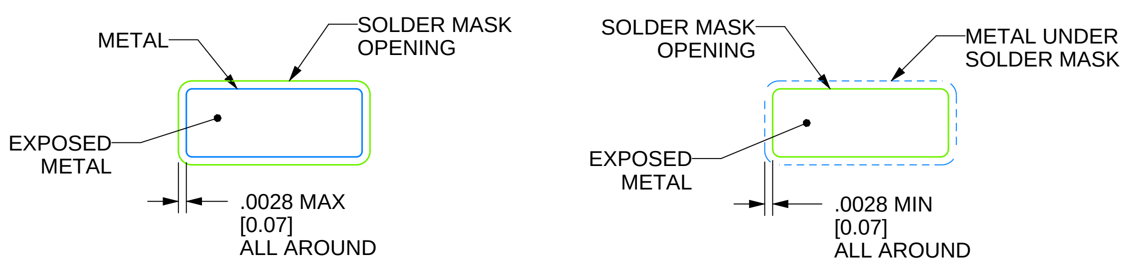


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED

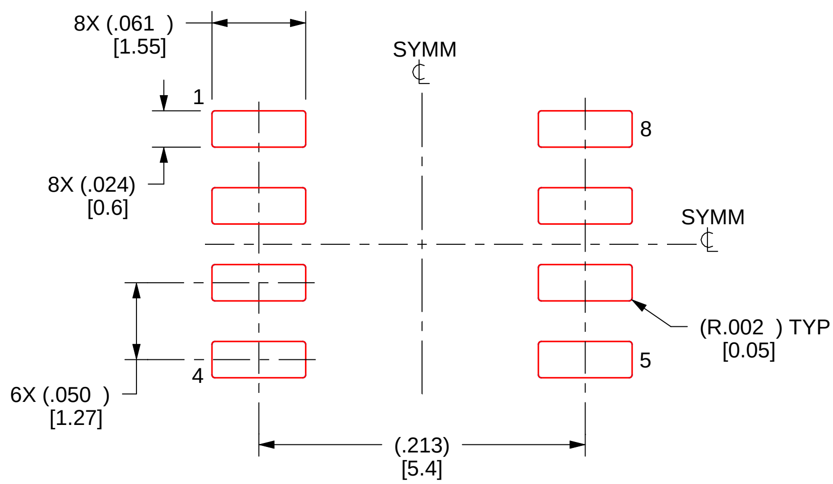
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.