











LMH6570

SNCS104D - APRIL 2005 - REVISED DECEMBER 2014

LMH6570 2:1 High Speed Video Multiplexer

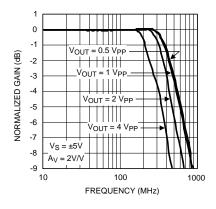
Features

- 500 MHz, 500 mV_{PP}, -3 dB Bandwidth, $A_V=2$
- 400 MHz, $2V_{PP}$, -3 dB Bandwidth, $A_V=2$
- 8 ns Channel Switching Time
- 70 dB Channel to Channel Isolation @ 10 MHz
- 0.02%, 0.05° Diff. Gain, Diff. Phase
- 0.1 dB Gain Flatness to 150 MHz
- 2200 V/µs Slew Rate
- Wide Supply Voltage Range: 6 V (±3 V) to 12 V (±6 V)
- -68 dB HD2 @ 5 MHz
- -84 dB HD3 @ 5 MHz

Applications

- Video Router
- Multi Input Video Monitor
- Instrumentation / Test Equipment
- Receiver IF Diversity Switch
- Multi Channel A/D Driver
- Picture in Picture Video Switch

Frequency Response vs. Vout



3 Description

The LMH6570 is a high performance analog multiplexer optimized for professional grade video and other high fidelity, high bandwidth analog applications. The output amplifier selects one of two buffered input signals based on the state of the SEL pin. The LMH6570 provides a 400 MHz bandwidth at . 2-V_{PP} output signal levels. Multimedia and high definition television (HDTV) applications can benefit from the 0.1-dB bandwidth of 150 MHz and the 2200-V/µs slew rate of LMH6570.

The LMH6570 supports composite video applications with its 0.02% and 0.05° differential gain and phase errors for NTSC and PAL video signals while driving a single, back terminated 75-Ω load. An 80-mA linear output current is available for driving multiple video load applications.

The LMH6570 gain is set by external feedback and gain set resistors for maximum flexibility.

The LMH6570 is available in the 8-pin SOIC package.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMH6570	SOIC (8)	4.9 mm × 3.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Frequency Response vs. Gain

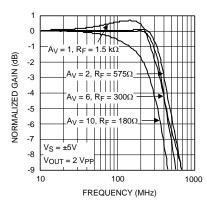




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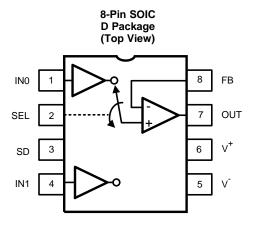
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (May 2013) to Revision D	Page
Added the following sections: Device Information Table; Power Supply Recommendations; Layout, Device and Documentation Support, Mechanical, Packaging, and Ordering Information	
Revised text in Application and Implementation section, formerly titled "Application Notes"	12
Revised text in <i>Multiplexer Expansion</i> section. Added Figure 27, Figure 28, and Figure 29	14
Changes from Revision B (April 2013) to Revision C	Page
Changed layout of National Data Sheet to TI format	18



5 Pin Configuration and Functions



Pin Functions

Р	IN	1/0	DESCRIPTION
NO.	NAME	I/O	Input Channel 0 Select Pin Shutdown Input Channel 1 V* Supply V* Supply Output
1	IN0	I	Input Channel 0
2	SEL	I	Select Pin
3	SD	I	Shutdown
4	IN1	I	Input Channel 1
5	V-	I	V ⁻ Supply
6	V ⁺	I	V ⁺ Supply
7	OUT	0	Output
8	FB	I	Feedback

Truth Table

SEL	SD	OUTPUT
1	0	IN1 * (1+RF/RG)
0	0	IN0 * (1+RF/RG)
X	1	Shutdown



6 Specifications

6.1 Absolute Maximum Ratings⁽¹⁾⁽²⁾

		MIN	MAX	UNIT
Supply Voltage (V ⁺ - V ⁻)			13.2	٧
I _{OUT} ⁽³⁾			130	mA
Signal & Logic Input Pin Voltage			$\pm (V_S + 0.6)$	٧
Signal & Logic Input Pin Current			±20	mA
Maximum Junction Temperature			+150	°C
Storage Temperature		-65	+150	ů
<u> </u>	Infrared or Convection (20 sec)		235	°C
Soldering Information	Wave Soldering (10 sec)		260	°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For specifications, see the Electrical Characteristics tables.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) The maximum output current (I_{OUT}) is determined by the device power dissipation limitations (The junction temperature cannot be allowed to exceed 150°C). See *Power Dissipation* for more details. A short circuit condition should be limited to 5 seconds or less.

6.2 ESD Ratings

			VALUE	UNIT
V	Electrostatic	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	\/
V _(ESD)	discharge	Machine model (MM) ⁽²⁾	±200	V

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance. Human body model, 1.5kΩ in series with 100 pF.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM MAX	UNIT
Operating Temperature	-40	85	°C
Supply Voltage	6	12	V

6.4 Thermal Information

	THERMAL METRIC ⁽¹⁾		UNIT	
	I THERMAL METRIC (**)	8 PINS	UNIT	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	150	°C /\/	
R ₀ JC(top)	Junction-to-case (top) thermal resistance	50	°C/W	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

⁽²⁾ Machine model, 0 Ω In series with 200 pF



6.5 Electrical Characteristics ±5V

 $V_S = \pm 5$ V, $R_L = 100$ Ω , $R_F = 576$ Ω , $A_V = 2$ V/V, $T_J = 25$ °C, unless otherwise specified.

	PARAMETER	TEST CONI	DITIONS ⁽¹⁾	MIN ⁽²⁾ TYP	3) MAX ⁽²⁾	UNIT
FREQUEN	CY DOMAIN PERFORMANCE					
SSBW	-3 dB Bandwidth	$V_{OUT} = 0.5 V_{PP}$		50	0	MHz
LSBW	-3 dB Bandwidth	$V_{OUT} = 2 V_{PP}^{(4)}$		40	0	MHz
.1 dBBW	0.1 dB Bandwidth	$V_{OUT} = 0.25 V_{PP}$		15	0	MHz
DG	Differential gain	$R_L = 150 \Omega$, $f = 4.43 MHz$		0.029	%	
DP	Differential phase	$R_L = 150 \Omega$, $f = 4.43 MHz$		0.0	5	deg
XTLK	Channel to channel crosstalk	All Hostile, f = 5 MHz	All Hostile, f = 5 MHz		0	dBc
TIME DOM	AIN RESPONSE					
T _{RS}	Channel to channel switching time	Logic transition to 90% or	utput		8	ns
	Enable and disable times	Logic transition to 90% or	10% output.	1	0	ns
T _{RL}	Rise and fall time	4 V Step		2.4		ns
T _{SS}	Settling time to 0.05%	2 V Step 17			ns	
OS	Overshoot	2 V Step		5'	%	
SR	Slew rate	4 V Step ⁽⁴⁾⁽⁵⁾		220	10	V/µs
DISTORTIO	NC					
HD2	2 nd Harmonic distortion	2 V _{PP} , 5 MHz		-6	8	dBc
HD3	3 rd Harmonic distortion	2 V _{PP} , 5 MHz		-84		dBc
IMD	3 rd Order intermodulation products	10 MHz, Two tones 2 Vpp	at output	-8	0	dBc
EQUIVALE	ENT INPUT NOISE	1	-			
VN	Voltage	>1 MHz, Input Referred			5	nV√ HZ
ICN	Current	>1 MHz, Input Referred			5	pA/√ Hz
STATIC, D	C PERFORMANCE	•	•			
CHOM	Channel to channel gain	DC, Difference in gain		±0.005	% ±0.034%	
CHGM	difference	between channels	-40°C ≤ T _J ≤ 85°C		±0.036%	
V	land offert veltere	V 0.V			1 ±15	mV
V_{IO}	Input offset voltage	$V_{IN} = 0 V$	-40°C ≤ T _J ≤ 85°C		±21	
DVIO	Offset voltage drift ⁽⁶⁾			3	30	μV/°C
IDNI	land him administration (7)	V 0.V		-	·3 ±8	μA
IBN	Input bias current ⁽⁷⁾	$V_{IN} = 0 V$	-40°C ≤ T _J ≤ 85°C		±10	
DIBN	Bias current drift ⁽⁶⁾			1	1	nA/°C

- (1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where T_J > T_A. See Thermal Information for information on temperature de-rating of this device. Min/Max ratings are based on product testing, characterization and simulation. Individual parameters are tested as noted.
- (2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods.
- (3) Typical numbers are the most likely parametric norm.
- (4) Parameter ensured by design.
- (5) Slew Rate is the average of the rising and falling edges.
- (6) Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.

(7) Positive Value is current into device.



Electrical Characteristics ±5V (continued)

 $V_S = \pm 5$ V, $R_L = 100$ Ω , $R_F = 576$ Ω , $A_V = 2$ V/V, $T_J = 25$ °C, unless otherwise specified.

	PARAMETER	TEST CONDI	TIONS ⁽¹⁾	MIN ⁽²⁾	TYP ⁽³⁾	MAX ⁽²⁾	UNIT
		Pin 8, Feedback point,			-3	±18	uA
l _{BI}	Inverting input bias current ⁽⁷⁾	$V_{IN} = 0 V$	-40°C ≤ T _J ≤ 85°C			±22	
DCDD	Davis a complete acidatica actic	DC Innut referred		48	50		dB
PSRR	Power supply rejection ratio	DC, Input referred	-40°C ≤ T _J ≤ 85°C	46			
ICC	Cumply ourrent	No Load, Shutdown Pin			13.8	15	mA
icc	Supply current	(SD) > 0.8 V	-40°C ≤ T _J ≤ 85°C			16	
	Supply current shutdown	Shutdown Pin (SD) > 2 V			1.1	1.3	mA
	Supply current shutdown	Shuldown Fill (SD) > 2 V	-40°C ≤ T _J ≤ 85°C			1.4	
V _{IH}	Logic high threshold	Select Pin & Shutdown pin	(SEL, SD)	2.0			V
V_{IL}	Logic low threshold	Select Pin & Shutdown pin	(SEL, SD)			0.8	V
		Logic Input = 0 V Select		-8	-1		μΑ
l _{iL}	Logic pin input current low ⁽⁷⁾	Pin & Shutdown Pin (SEL, SD)	-40°C ≤ T _J ≤ 85°C	-10			
	(7)	Logic Input = 5.0 V, Select			57	68	μΑ
l _{іН}	Logic pin input current high ⁽⁷⁾	Pin & Shutdown Pin (SEL, SD)	-40°C ≤ T _J ≤ 85°C			75	
MISCELI	LANEOUS PERFORMANCE	•					
RIN+	Input resistance				5		kΩ
CIN	Input capacitance				0.8		pF
R _{OUT}	Output resistance	Output Active, (SD < 0.8 V))		0.04		Ω
R _{OUT}	Output resistance	Output Disabled, (SD > 2 V	")		3000		Ω
C _{OUT}	Output capacitance	Output Disabled, (SD > 2 V	")		3.1		pF
.,		No Load		±3.51	±3.7		V
Vo	— Output voltage range	NO LOAU	-40°C ≤ T _J ≤ 85°C	±3.50			
V _a .	Output voltage range	R ₁ = 100 Ω		±3.16	±3.5		V
V _{OL}		17[- 100 72	-40°C ≤ T _J ≤ 85°C	±3.15			
CMIR	Input voltage range			±2.5	±2.6		V
				+60	±80		mA
lo	Linear output current(7)	$V_{IN} = 0 V$		-70			
			-40°C ≤ T _J ≤ 85°C	±55			
I _{SC}	Short circuit current ⁽⁸⁾	V _{IN} = ±2 V, Output shorted	to ground		±230		mA

⁽⁸⁾ The maximum output current (I_{OUT}) is determined by the device power dissipation limitations (The junction temperature cannot be allowed to exceed 150°C). See *Power Dissipation* for more details. A short circuit condition should be limited to 5 seconds or less.



6.6 Electrical Characteristics ±3.3V

 $V_S = \pm 3.3 \text{ V}$, $R_L = 100 \Omega$, $R_F = 576 \Omega$, $A_V = 2 \text{ V/V}$, unless otherwise specified.

	PARAMETER	TEST CONDITIONS ⁽¹⁾	MIN ⁽²⁾ TYP ⁽³⁾ N	MAX ⁽²⁾	UNIT
FREQUEN	CY DOMAIN PERFORMANCE				
SSBW	-3 dB Bandwidth	V _{OUT} = 0.5 V _{PP}	475		MHz
LSBW	-3 dB Bandwidth	V _{OUT} = 2.0 V _{PP}	375		MHz
0.1 dBBW	0.1 dB Bandwidth	V _{OUT} = 0.5 V _{PP}	100		MHz
GFP	Peaking	DC to 200 MHz	0.4		dB
XTLK	Channel to channel crosstalk	All Hostile, f = 5 MHz	-70		dBc
TIME DOM	AIN RESPONSE		•	•	
T _{RL}	Rise and Fall time	2 V Step	2		ns
T _{SS}	Settling time to 0.05%	2 V Step	20		ns
OS	Overshoot	2 V Step	5%		
SR	Slew rate	2 V Step	1400		V/µs
DISTORTIO	ON				
HD2	2 nd Harmonic distortion	2 V _{PP} , 10 MHz	-67		dBc
HD3	3 rd Harmonic distortion	2 V _{PP} , 10 MHz	-87		dBc
STATIC, D	C PERFORMANCE			·	
V _{IO}	Input offset voltage	V _{IN} = 0 V	1		mV
IBN	Input bias current ⁽⁴⁾	V _{IN} = 0 V	-3		μΑ
PSRR	Power supply rejection ratio	DC, Input Referred	49		dB
ICC	Supply current	No Load	12.5		mA
V _{IH}	Logic high threshold	Select Pin & Shutdown pin (SEL, SD), $V_{IH} \cong V^{+*} 0.4$	1.3		V
V _{IL}	Logic low threshold	Select Pin & Shutdown pin (SEL, SD), V _{IL} ≅ V ⁺ * 0.12	0.4		V
MISCELLA	NEOUS PERFORMANCE				
R _{IN+}	Input resistance		5		kΩ
C _{IN}	Input capacitance		0.8		pF
R _{OUT}	Output resistance		0.06		Ω
Vo	Output valtage range	No Load	±2		V
V _{OL}	Output voltage range	R _L = 100 Ω	±1.8		V
CMIR	Input voltage range		±1.2		V
I _O	Linear output current ⁽⁵⁾	V _{IN} = 0 V	±60		mA
I _{SC}	Short circuit current ⁽⁵⁾	V _{IN} = ±1 V, Output shorted to ground	±150		mA

⁽¹⁾ Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where T_J > T_A. See Thermal Information for information on temperature de-rating of this device. Min/Max ratings are based on product testing, characterization and simulation. Individual parameters are tested as noted.

⁽²⁾ Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods.

⁽³⁾ Typical numbers are the most likely parametric norm.

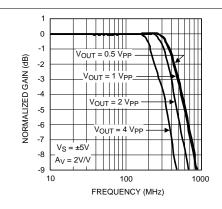
⁽⁴⁾ Positive Value is current into device.

⁽⁵⁾ The maximum output current (I_{OUT}) is determined by the device power dissipation limitations (The junction temperature cannot be allowed to exceed 150°C). See *Power Dissipation* for more details. A short circuit condition should be limited to 5 seconds or less.

TEXAS INSTRUMENTS

6.7 Typical Performance Characteristics

 V_s = ±5 V, R_L = 100 Ω , A_V = 2, R_F = R_G = 576 Ω , unless otherwise specified.



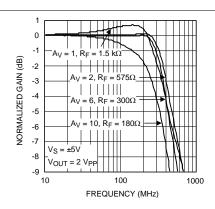


Figure 1. Frequency Response vs. $V_{\rm OUT}$

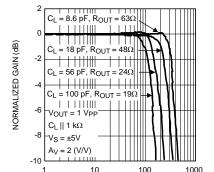


Figure 2. Frequency Response vs. Gain

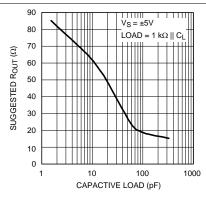


Figure 3. Frequency Response vs. Capacitive Load

FREQUENCY (MHz)

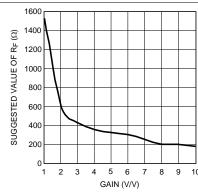


Figure 4. Suggested R_{OUT} vs. Capacitive Load

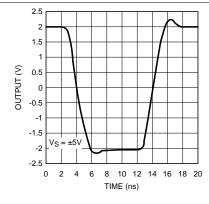


Figure 5. Suggested Value of $R_{\text{\scriptsize F}}$ vs. Gain

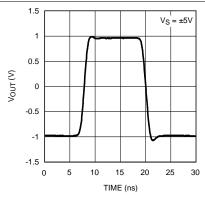
Figure 6. Pulse Response $4V_{PP}$

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Typical Performance Characteristics (continued)

 $V_s = \pm 5$ V, $R_L = 100$ Ω , $A_V = 2$, $R_F = R_G = 576$ Ω , unless otherwise specified.



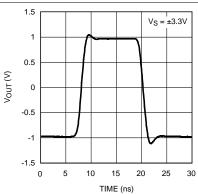
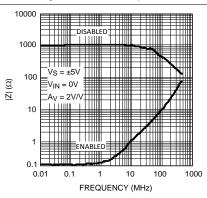


Figure 7. Pulse Response 2VPP





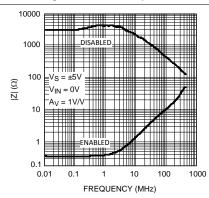
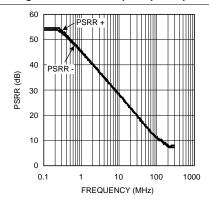


Figure 9. Closed Loop Output Impedance

Figure 10. Closed Loop Output Impedance



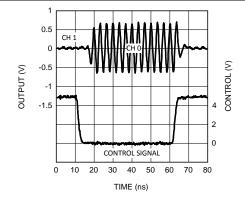


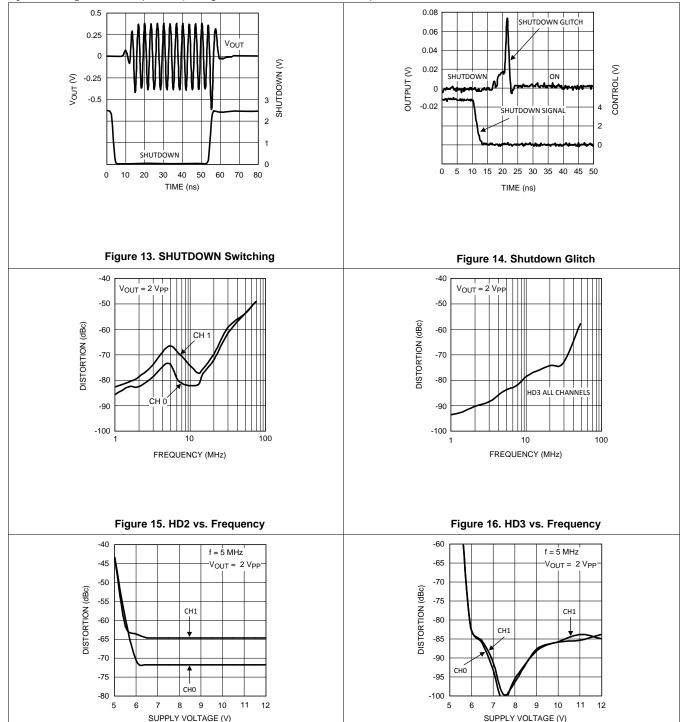
Figure 11. PSRR vs. Frequency

Figure 12. Channel Switching

TEXAS INSTRUMENTS

Typical Performance Characteristics (continued)

 $\rm V_s=\pm 5~V,~R_L=100~\Omega,~A_V=2,~R_F=R_G=576~\Omega,$ unless otherwise specified.



Product Folder Links: LMH6570

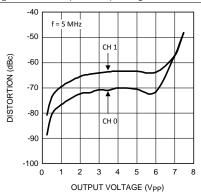
Figure 17. HD2 vs. V_S

Figure 18. HD3 vs. V_S



Typical Performance Characteristics (continued)

 $\rm V_s=\pm 5~V,~R_L=100~\Omega,~A_V=2,~R_F=R_G=576~\Omega,$ unless otherwise specified.



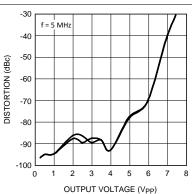
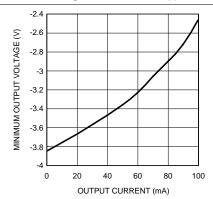


Figure 19. HD2 vs. V_{OUT}



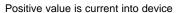
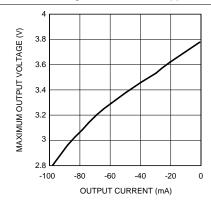


Figure 20. HD3 vs. V_{OUT}



Positive value is current into device

Figure 21. Minimum V_{OUT} vs. I_{OUT}

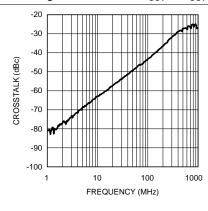
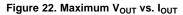


Figure 23. Crosstalk vs. Frequency



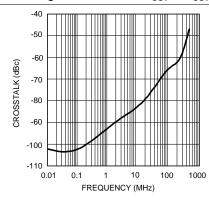


Figure 24. Off Isolation

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7 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

The LMH6570 is a high-speed 2:1 analog multiplexer, optimized for very high speed and low distortion. With selectable gain and excellent AC performance, the LMH6570 is ideally suited for switching high resolution, presentation grade video signals. The LMH6570 has no internal ground reference. Single or split supply configurations are both possible, however, all logic functions are referenced to the mid supply point. The LMH6570 features very high speed channel switching and disable times. When disabled the LMH6570 output is high impedance making MUX expansion possible by combining multiple devices. See *Multiplexer Expansion*. The LMH6570 SEL defaults to logic low (IN0 active). The default state for the SD pin is also logic low (device enabled). Both pins can be left floating if the default state is desired.

7.2 Typical Application

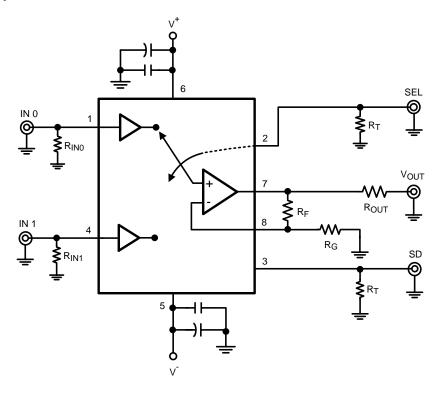


Figure 25. Typical Application

7.2.1 Video Performance

The LMH6570 has been designed to provide excellent performance with production quality video signals in a wide variety of formats such as HDTV and High Resolution VGA. Best performance will be obtained with back-terminated loads. The back termination reduces reflections from the transmission line and effectively masks transmission line and other parasitic capacitances from the amplifier output stage. Figure 25 shows a typical configuration for driving a 75- Ω cable. The output buffer is configured for a gain of 2, so using back terminated loads will give a net gain of 1.



7.2.2 Feedback Resistor Selection

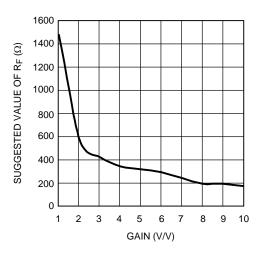


Figure 26. Suggested R_F vs. Gain

The LMH6570 has a current feedback output buffer with gain determined by external feedback (R_F) and gain set (R_G) resistors. With current feedback amplifiers, the closed loop frequency response is a function of R_F . For a gain of 2 V/V, the recommended value of R_F is 576 Ω . For other gains, see Figure 26. Generally, lowering R_F from the recommended value will peak the frequency response and extend the bandwidth while increasing the value of R_F will cause the frequency response to roll off faster. Reducing the value of R_F too far below the recommended value will cause overshoot, ringing and, eventually, oscillation.

Since all applications are slightly different, it is worth some experimentation to find the optimal R_F for a given circuit. For more information see *Current Feedback Loop Gain Analysis and Performance Enhancement*, Application Note OA-13 (SNOA366), which describes the relationship between R_F and closed-loop frequency response for current feedback operational amplifiers. The impedance looking into pin 8 is approximately 20 Ω . This allows for good bandwidth at gains up to 10 V/V. When used with gains over 10 V/V, the LMH6570 will exhibit a "gain bandwidth product" similar to a typical voltage feedback amplifier. For gains of over 10 V/V consider selecting a high performance video amplifier like the LMH6720 to provide additional gain.



7.2.3 Multiplexer Expansion

It is possible to use multiple LMH6570 devices to expand the number of inputs that can be selected for output. Figure 27 shows a 4:1 MUX using two LMH6570 devices.

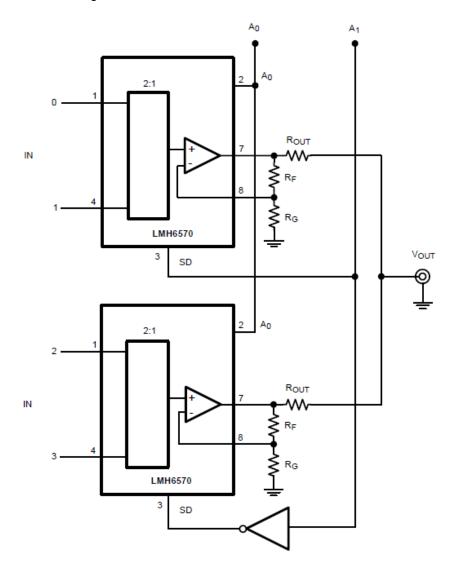


Figure 27. 4:1 MUX Using Two LMH6570 Devices

In such an application, the output settling may be longer than the LMH6570 switching specifications (~20 ns), while switching between two separate LMH6570 devices. The switching time limiting factor occurs when one LMH6570 is turned off and another one is turned on, using the SD (shutdown) pin. The output settling time consists of the time needed for the first LMH6570 to enter high impedance state plus the time required for the second LMH6570 output to dissipate left-over output charge of the first device (limited by the output current capability of the second device) and the time needed to settle to the final voltage value.



While Figure 27 MUX expansion benefits from more isolation, originating from the parasitic loading of the unselected channels on the selected channel, afforded by individual R_{OUT} on each multiplexer output, this configuration does not produce the fastest transition between individual LMH6570 devices. For fastest transition between LMH6570 devices, the configuration of Figure 28 can be used where the LMH6570 output pins are all shorted together.

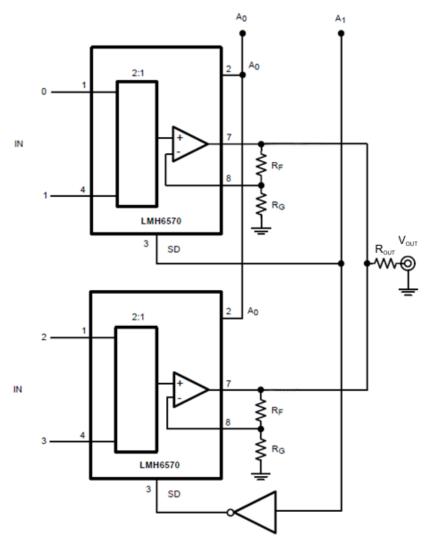


Figure 28. Alternate 4:1 MUX Expansion Schematic (for Faster SD Switching)

Figure 29 shows typical transition waveforms and shows that SD pin switching settles in less than 145 ns.

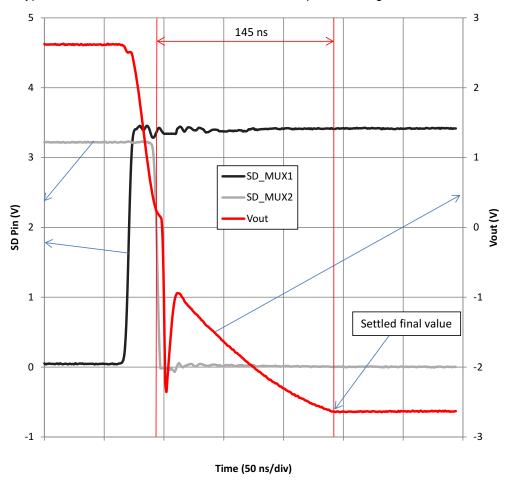


Figure 29. SD pin Switching Waveform and Output Settling

If it is important in the end application to make sure that no two inputs are presented to the output at the same time, an optional delay block can be added, to drive the SHUTDOWN pin of each device. Figure 30 shows one possible approach to this delay circuit. The delay circuit shown will delay H to L transitions of SHUTDOWN (R1 and C1 decay) but will not delay its L to H transition. R2 should be kept small compared to R1 in order to not reduce the SHUTDOWN voltage and to produce little or no delay to SHUTDOWN.

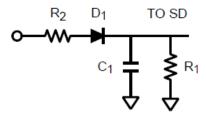


Figure 30. Delay Circuit Implementation



With the SHUTDOWN pin putting the output stage into a high impedance state, several LMH6570 devices can be tied together to form a larger input MUX. However, there is a loading effect on the active output caused by the unselected devices. The circuit in Figure 31 shows how to compensate for this effect. For the 8:1 MUX function shown in Figure 31, the gain error would be about 0.7% or -0.06dB. In the circuit in Figure 31, resistor ratios have been adjusted to compensate for this gain error. By adjusting the gain of each multiplexer circuit the error can be reduced to the tolerance of the resistors used (1% in this example).

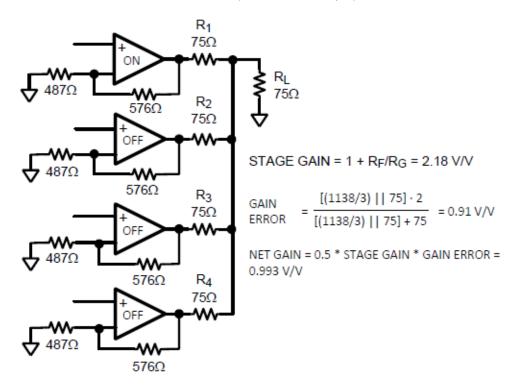


Figure 31. Multiplexer Gain Compensation

NOTE

Disabling of the LMH6570 using the EN pin is not recommended for use when doing multiplexer expansion. While disabled, If the voltage between the selected input and the chip output exceeds approximately 2 V the device will begin to enter a soft breakdown state. This will show up as reduced input to output isolation. The signal on the non-inverting input of the output driver amplifier will leak through to the inverting input, and then to the output through the feedback resistor. The worst case is a gain of 1 configuration where the non-inverting input follows the active input buffer and (through the feedback resistor) the inverting input follows the voltage driving the output stage. The solution for this is to use shutdown mode for multiplexer expansion.

7.2.4 Other Applications

The LMH6570 could support a dual antenna receiver with two physically separate antennas. Monitoring the signal strength of the active antenna and switching to the other antenna when a fade is detected is a simple way to achieve spacial diversity. This method gives about a 3 dB boost in average signal strength and is the least expensive method for combining signals.



7.2.5 Driving Capacitive Loads

Capacitive output loading applications will benefit from the use of a series output resistor R_{OUT} . Figure 32 shows the use of a series output resistor, R_{OUT} , to stabilize the amplifier output under capacitive loading. Capacitive loads of 5 to 120 pF are the most critical, causing ringing, frequency response peaking and possible oscillation. Figure 33 gives a recommended value for selecting a series output resistor for mitigating capacitive loads. The values suggested in the charts are selected for 0.5 dB or less of peaking in the frequency response. This gives a good compromise between settling time and bandwidth. For applications where maximum frequency response is needed and some peaking is tolerable, the value of R_{OUT} can be reduced slightly from the recommended values.

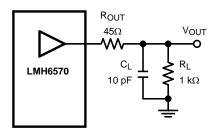
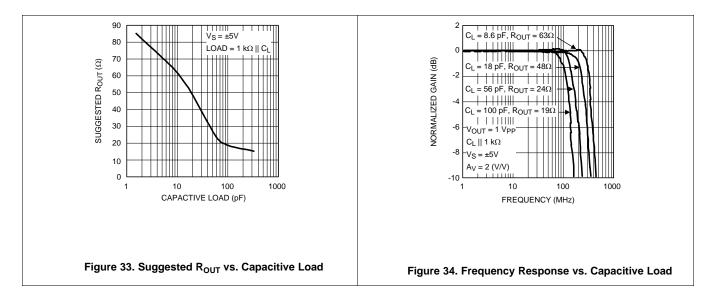


Figure 32. Decoupling Capacitive Loads



7.2.6 ESD Protection

The LMH6570 is protected against electrostatic discharge (ESD) on all pins. The LMH6570 will survive 2000-V Human Body model and 200-V Machine model events. Under normal operation the ESD diodes have no effect on circuit performance. However, there are occasions when the ESD diodes will be evident. If the LMH6570 is driven by a large signal while the device is powered down, the ESD diodes will conduct. The current that flows through the ESD diodes will either exit the chip through the supply pins or will flow through the device. Therefore, it is possible to power up a chip with a large signal applied to the input pins. Using the shutdown mode is one way to conserve power and still prevent unexpected operation.



8 Power Supply Recommendations

8.1 Power Dissipation

The LMH6570 is optimized for maximum speed and performance in the small form factor of the standard SOIC package. To ensure maximum output drive and highest performance, thermal shutdown is not provided. Therefore, it is of utmost importance to make sure that the T_{JMAX} is never exceeded due to the overall power dissipation.

Follow these steps to determine the maximum power dissipation for the LMH6570:

1. Calculate the quiescent (no-load) power:

$$P_{AMP} = I_{CC}^* (V_S),$$

where

•
$$V_S = V^+ - V^-$$
 (1)

2. Calculate the RMS power dissipated in the output stage:

$$P_D$$
 (rms) = rms (($V_S - V_{OUT}$) * I_{OUT})

where

- V_{OUT} and I_{OUT} are the voltage across
- The current through the external load and V_S is the total supply voltage

(2)

3. Calculate the total RMS power:

$$P_{T} = P_{AMP} + P_{D} \tag{3}$$

The maximum power that t-he LMH6570 package can dissipate at a given temperature can be derived with the following equation:

$$P_{MAX} = (150^{\circ} - T_{AMB})/R_{\theta JA}$$

where

- T_{AMB} = Ambient temperature (°C)
- R_{θJA} = Thermal resistance, from junction to ambient, for a given package (°C/W)
- For the SOIC package R_{BJA} is 150 °C/W (4)

9 Layout

9.1 Layout Guidelines

To reduce parasitic capacitances, ground and power planes should be removed near the input and output pins. For long signal paths controlled impedance lines should be used, along with impedance matching elements at both ends. Bypass capacitors should be placed as close to the device as possible. Bypass capacitors from each rail to ground are applied in pairs. The larger electrolytic bypass capacitors can be located farther from the device, whereas the smaller ceramic capacitors should be placed as close to the device as possible. In Figure 25, the capacitor between V^+ and V^- is optional, but is recommended for best second harmonic distortion. Another way to enhance performance is to use pairs of 0.01 μ F and 0.1 μ F ceramic capacitors for each supply bypass.



10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Current Feedback Loop Gain Analysis and Performance Enhancement, Application Note OA-13 (SNOA366)
- IC Package Thermal Metrics Application Report (SPRA953)

10.2 Trademarks

All trademarks are the property of their respective owners.

10.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

10.4 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

www.ti.com 10-Nov-2025

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
LMH6570MA/NOPB	Active	Production	SOIC (D) 8	95 TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMH65 70MA
LMH6570MA/NOPB.A	Active	Production	SOIC (D) 8	95 TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMH65 70MA
LMH6570MAX/NOPB	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMH65 70MA
LMH6570MAX/NOPB.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMH65 70MA

⁽¹⁾ Status: For more details on status, see our product life cycle.

- (3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
- (4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.



PACKAGE OPTION ADDENDUM

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	_	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6570MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

www.ti.com 23-May-2025



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
LMH6570MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0	

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMH6570MA/NOPB	D	SOIC	8	95	495	8	4064	3.05
LMH6570MA/NOPB.A	D	SOIC	8	95	495	8	4064	3.05



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

- 1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- 4. This dimension does not include interlead flash.
- 5. Reference JEDEC registration MS-012, variation AA.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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