LMH5485-SP Radiation Hardened Assured, Negative Rail Input, Rail-to-Rail Output, Precision, 850MHz Fully Differential Amplifier

1 Features

- QMLV (QML class V) MIL-PRF-38535 qualified, SMD 5962R1920401VXC
  - TID assured for every wafer lot up to 100krad (Si)
  - Single event latch-up (SEL) immune to LET = 77MeV-cm2/mg
  - Qualified over the military temperature range: –55°C to +125°C
- Gain bandwidth product (GBWP): 850MHz
- Slew rate: 1400V/µs
- HD2, HD3: –111dBc, –149dBc (100kHz, $2V_{PP}$)
- Input voltage noise: 2.4nV/√Hz
- Low offset drift: ±0.5µV/°C (typical)
- Negative rail input (NRI), rail-to-rail output (RRO)
- Power supply:
  - Supply voltage range: 2.7V to 5.4V
  - Quiescent current: 10.1mA
  - Power-down capability: 2µA (typical)

2 Applications

- Low-power, high-performance ADC driver:
  - SAR, ΔΣ, and pipeline
- Differential DAC output driver
- Command and data handling
- Launch vehicle systems
- Space imaging systems:
  - Optical imaging payload
  - Radar imaging payload
  - Thermal imaging cameras

3 Description

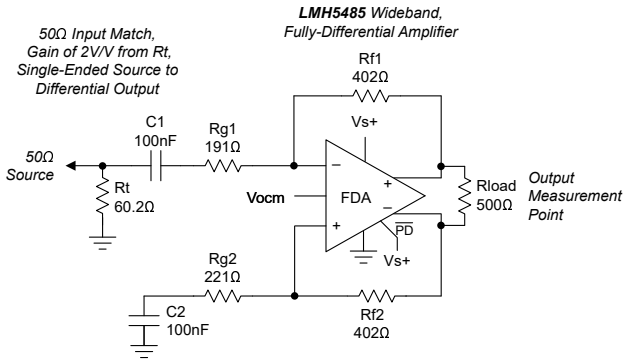
The LMH5485-SP is a radiation-hardened assured, low-power, voltage-feedback, fully differential amplifier (FDA). This device is able to achieve a high gain bandwidth product (GBWP) of 850MHz to maintain excellent distortion performance over a wide range of frequencies. This wide bandwidth range is also achieved with a relatively low power consumption of 10.1mA and broadband voltage noise of 2.4nV/√Hz. These features make the LMH5485-SP an excellent choice for power-sensitive data acquisition systems with frequencies > 10MHz that require both the best signal-to-noise ratio (SNR) and spurious-free dynamic range (SFDR).

The LMH5485-SP features the negative-rail input required when interfacing with a dc-coupled, ground-centered source signal. This negative-rail input with a rail-to-rail output allows for easy interface between single-ended, ground-referenced, bipolar signal sources and a wide variety of successive approximation register (SAR), delta-sigma (ΔΣ), or pipeline ADCs using only a single 2.7V to 5.4V power supply. The LMH5485-SP also features a low offset voltage drift of ±0.5µV/°C to maintain excellent dc performance over a wide temperature range of –55°C to +125°C.

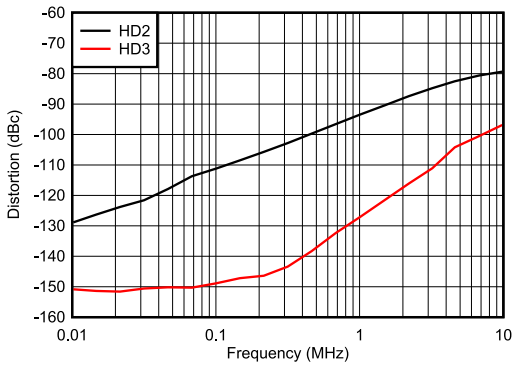
Device Information

PART NUMBER(1)	GRADE(2)	PACKAGE
5962R1920401VXC(4)	Radiation hardened assured (RHA)	Ceramic CFP HKX (8) 6.5mm × 6.5mm
LMH5485HKX/EM	Engineering samples(3)	

(1) See *Section 4*.
(2) For more information, see Section 12.
(3) These units are intended for engineering evaluation only. These units are processed to a non-compliant flow. These units are not designed for qualification, production, radiation testing or flight use. Parts are not warranted for performance over the full MIL specified temperature range of –55°C to +125°C or operating life.
(4) Product preview.



Simplified Schematic



Harmonic Distortion vs Frequency

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4 Related Products

DEVICE	RAD TOLERANCE	GBWP (MHz)	I_Q (mA)	HD2 / HD3 (dBc) $2V_{PP}$ AT 10MHz	INPUT NOISE (nV/√Hz)	RAIL-TO-RAIL
LMH5485-SP	100kRad TID	850	10.1	–79 / –97	2.4	Negative rail input/Output
LMH5485-SEP	30kRad TID	850	10.1	–90 / –102	2.4	Negative rail input/Output
THS4513-SP	150kRad TID	3000	37.7	–106 / –108	2.2	No
LMH5401-SP	100kRad TID	6500	60	–99 / –100	1.25	No

5 Pin Configuration and Functions

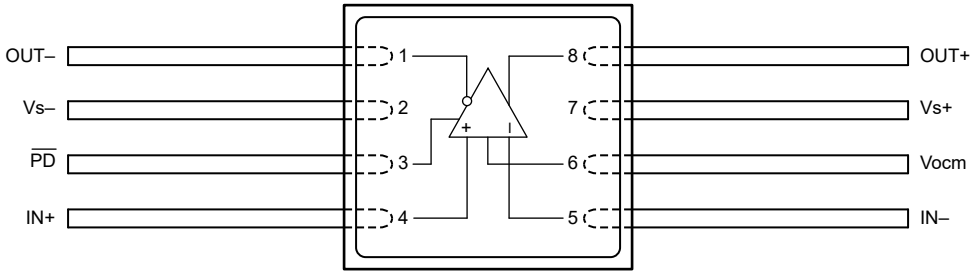


Figure 5-1. HKX Package, 8-Pin CFP (Top View)

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
IN+	4	Input	Noninverting (positive) amplifier input
IN–	5	Input	Inverting (negative) amplifier input
OUT+	8	Output	Noninverting (positive) amplifier output
OUT–	1	Output	Inverted (negative) amplifier output
$\overline{PD}$	3	Input	Power down. $\overline{PD}$ = logic low = power-down mode; $\overline{PD}$ = logic high = normal operation.
Vocm	6	Input	Common-mode voltage input
Vs+	7	Power	Positive power-supply input
Vs–	2	Power	Negative power-supply input

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage (Vs+) – (Vs–)	$\overline{PD}$ = logic high		5.5	V
		$\overline{PD}$ = logic low		5.25	
V_{IN}	Input voltage		(Vs–) – 0.5	(Vs+) + 0.5	V
V_{OUT}	Output voltage		(Vs–) – 0.5	(Vs+) + 0.5	V
V_{ID}	Differential input voltage			±1	V
I_I	Continuous input current			±20	mA
I_O	Continuous output current			±80	mA
	Continuous power dissipation		See *Thermal Information* and *Thermal Analysis* sections		
T_J	Junction temperature			150	°C
T_A	Ambient temperature		–55	125	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±750	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
Vs+	Single-supply voltage	$\overline{PD}$ = logic high	2.7	5	5.4	V
		$\overline{PD}$ = logic low	2.7	5	5.1	V
T_A	Ambient temperature		–55	25	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LMH5485-SP HKX (CFP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	145.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	128.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	61.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	122.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	55.8	°C/W

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics for V_S = 5V

The following specifications correspond to the respectively identified subgroup temperature (see Section 6.7), unless otherwise noted. Vocm = open (defaults midsupply), V_{OUT} = 2V_{PP}, Rf = 402Ω, Rload = 499Ω, 50Ω input match, G = 2V/V, single-ended input, differential output, and $\overline{PD}$ = Vs+, unless otherwise noted. See Section 7.1 for a test circuit with an ac-coupled gain of 2V/V, and Section 7.1 for a dc-coupled gain of a 2V/V.

PARAMETER		TEST CONDITIONS		SUB-GROUP(1)	MIN	TYP	MAX	UNIT
AC PERFORMANCE								
	Small-signal bandwidth	V_{OUT} = 100mV_{PP}	G = 1			530		MHz
			G = 2			490		
			G = 5			240		
			G = 10			125		
GBWP	Gain-bandwidth product	V_{OUT} = 100mV_{PP}, G = 20				1200		MHz
	Large-signal bandwidth	V_{OUT} = 2V_{PP}				315		MHz
	Bandwidth for 0.1dB flatness	V_{OUT} = 2V_{PP}				50		MHz
	Slew rate(2)	V_{OUT} = 2V_{PP}, FPBW				1400		V/µs
	Rise and fall time	V_{OUT} = 2V step, input ≤ 0.5ns t_r				1.4		ns
	Settling time	V_{OUT} = 2V step, t_r = 2ns	To 1%			5.4		ns
			To 0.1%			10		
	Overshoot and undershoot	V_{OUT} = 2V step, input ≤ 0.3ns t_r				24%		
	Harmonic distortion	100kHz, V_{OUT} = 2V_{PP}	HD2			–111		dBc
			HD3			–149		
		10MHz, V_{OUT} = 2V_{PP}	HD2			–79		
			HD3			–97		
	2nd-order intermodulation distortion	f = 10MHz, 100kHz tone spacing, V_{OUT} envelope = 2V_{PP} (1V_{PP} per tone)				–90		dBc
	3rd-order intermodulation distortion					–85		dBc
	Input voltage noise	f > 100kHz				2.4		nV/√Hz
	Input current noise	f > 1MHz				1.9		pA/√Hz
	Overdrive recovery time	2 × output overdrive, either polarity				20		ns
	Closed-loop output impedance	f = 10MHz (differential)				0.1		Ω
DC PERFORMANCE								
A_{OL}	Open-loop voltage gain			[1, 2, 3]	97	119		dB
	Input-referred offset voltage			[1, 2, 3]	–900	±100	900	µV
	Input offset voltage drift(3)				–4	±0.5	4	µV/°C
	Input bias current	Positive out of node		[1, 2, 3]	0.4	10	15	µA
	Input bias current drift(3)					6	15	nA/°C
	Input offset current			[1, 2, 3]	–1200	±150	1200	nA
	Input offset current drift(3)				–1.5	±0.3	1.5	nA/°C
INPUT								
	Common-mode input low	< 3dB degradation in CMRR from midsupply		[1, 2, 3]		(Vs–) – 0.2	Vs–	V
	Common-mode input high	< 3dB degradation in CMRR from midsupply		[1, 2, 3]	(Vs+) – 1.3	(Vs+) –1.2		V
	Common-mode rejection ratio	Input pins at midsupply		[1, 2, 3]	82	100		dB
	Input impedance differential mode	Input pins at midsupply				110 || 1.25		kΩ || pF

6.5 Electrical Characteristics for V_S = 5V (continued)

The following specifications correspond to the respectively identified subgroup temperature (see Section 6.7), unless otherwise noted. Vocm = open (defaults midsupply), V_{OUT} = $2V_{PP}$, Rf = 402Ω, Rload = 499Ω, 50Ω input match, G = 2V/V, single-ended input, differential output, and $\overline{PD}$ = Vs+, unless otherwise noted. See Section 7.1 for a test circuit with an ac-coupled gain of 2V/V, and Section 7.1 for a dc-coupled gain of a 2V/V.

PARAMETER		TEST CONDITIONS		SUB-GROUP(1)	MIN	TYP	MAX	UNIT
OUTPUT								
	Output voltage low			[1, 2, 3]		(Vs–) + 0.2	(Vs–) + 0.25	V
	Output voltage high			[1, 2, 3]	(Vs+) – 0.25	(Vs+) – 0.2		V
	Output current drive			[1, 2, 3]	±70	±100		mA
POWER SUPPLY								
	Quiescent operating current			[1, 2, 3]	9.2	10.1	11	mA
PSRR	Power-supply rejection ratio	Either supply pin to differential V_{OUT}		[1, 2, 3]	82	100		dB
POWER DOWN								
	Enable voltage threshold			[1, 2, 3]	(Vs–) + 1.7			V
	Disable voltage threshold			[1, 2, 3]			(Vs–) + 0.7	V
	Disable pin bias current	$\overline{PD}$ = Vs– → Vs+		[1, 2, 3]		20	50	nA
	Power-down quiescent current	$\overline{PD}$ = (Vs–) + 0.7V	T_A = 25°C	[1, 2, 3]		6	30	µA
			T_A = –40°C to +125°C				100	
		$\overline{PD}$ = Vs–	T_A = 25°C	[1, 2, 3]		2	8	
			T_A = –40°C to +125°C				30	
	Turn-on delay	Time from $\overline{PD}$ = low to V_{OUT} = 90% of final value				100		ns
	Turn-off delay	Time from $\overline{PD}$ = low to V_{OUT} = 10% of final value				60		ns
OUTPUT COMMON-MODE VOLTAGE CONTROL(4)								
	Small-signal bandwidth	Vocm = $100mV_{PP}$				150		MHz
	Slew rate(2)	Vocm = 2V step				400		V/µs
	Gain			[1, 2, 3]	0.975	0.982	0.995	V/V
	Input bias current	Considered positive out of node		[1, 2, 3]	–0.9	0.1	0.9	µA
	Input impedance	Vocm pin driven to midsupply				47 || 1.2		kΩ || pF
	Default voltage offset from midsupply	Vocm pin open		[1, 2, 3]	–50	±8	50	mV
CM V_{OS}	Common-mode offset voltage	Vocm pin driven to midsupply		[1, 2, 3]	–8	±2	8	mV
	CM V_{OS} drift(3)	Vocm pin driven to midsupply			–20	±4	+20	µV/°C
	Common-mode loop supply headroom to negative supply	< ±15mV shift from midsupply CM V_{OS}		[1, 2, 3]	0.94			V
	Common-mode loop supply headroom to positive supply	< ±15mV shift from midsupply CM V_{OS}		[1, 2, 3]	1.2			V

(1) For subgroup definitions, see Section 6.7
(2) This slew rate is the average of the rising and falling time estimated from the large-signal bandwidth as: $(V_P / \sqrt{2}) \times 2\pi \times f_{-3dB}$.
(3) Input offset voltage drift, input bias current drift, input offset current drift, and Vocm drift are average values calculated by taking data at the maximum-range ambient-temperature end-points, computing the difference, and dividing by the temperature range.
(4) Specifications are from the input Vocm pin to the differential output average voltage.

6.6 Electrical Characteristics for V_S = 3V

The following specifications correspond to the respectively identified subgroup temperature (see Section 6.7), unless otherwise noted. Vocm = open (defaults midsupply), V_{OUT} = 2V_{PP}, Rf = 402Ω, Rload = 499Ω, 50Ω input match, G = 2V/V, single-ended input, differential output, and $\overline{PD}$ = Vs+, unless otherwise noted. See Section 7.1 for a test circuit with an ac-coupled gain of 2V/V, and Section 7.1 for a dc-coupled gain of 2V/V.

PARAMETER		TEST CONDITIONS		SUB-GROUP[1]	MIN	TYP	MAX	UNIT
AC PERFORMANCE								
	Small-signal bandwidth	V_{OUT} = 100mV_{PP}	G = 1			510		MHz
			G = 2			475		
			G = 5			240		
GBWP	Gain-bandwidth product	V_{OUT} = 100mV_{PP}, G = 20				850		MHz
	Large-signal bandwidth	V_{OUT} = 2V_{PP}				300		MHz
	Bandwidth for 0.1dB flatness	V_{OUT} = 2V_{PP}				50		MHz
	Slew rate[2]	V_{OUT} = 2V step, FPBW				1200		V/µs
	Rise and fall time	V_{OUT} = 2V step, input ≤ 0.5ns t_r				1.6		ns
	Settling time	V_{OUT} = 2V step, t_r = 2ns	To 1%			5		ns
			To 0.1%			9		
	Overshoot and undershoot	V_{OUT} = 2V step, input ≤ 0.3ns t_r				25%		
	Harmonic distortion	100kHz, V_{OUT} = 2V_{PP}	HD2			–111		dBc
			HD3			–150		
		10MHz, V_{OUT}= 2V_{PP}	HD2			–80		
			HD3			–96		
	2nd-order intermodulation distortion	f = 10MHz, 100kHz tone spacing, V_{OUT} envelope = 2V_{PP} (1V_{PP} per tone)				–89		dBc
	3rd-order intermodulation distortion					–87		dBc
	Input voltage noise	f > 100kHz				2.4		nV/√Hz
	Input current noise	f > 1MHz				1.9		pA/√Hz
	Overdrive recovery time	2 × output overdrive, either polarity				20		ns
	Closed-loop output impedance	f = 10MHz (differential)				0.1		Ω
DC PERFORMANCE								
A_{OL}	Open-loop voltage gain			[1, 2, 3]	97	119		dB
	Input-referred offset voltage			[1, 2, 3]	–900	±100	900	µV
	Input offset voltage drift[3]				–4	±0.5	4	µV/°C
	Input bias current	Positive out of node		[1, 2, 3]	0.4	9	15	µA
	Input bias current drift[3]					5	15	nA/°C
	Input offset current			[1, 2, 3]	–1200	±150	1200	nA
	Input offset current drift[3]				–4	±0.3	4	nA/°C
INPUT								
	Common-mode input low	< 3dB degradation in CMRR from midsupply		[1, 2, 3]		(Vs–) – 0.2	Vs–	V
	Common-mode input high	< 3dB degradation in CMRR from midsupply		[1, 2, 3]	(Vs+) – 1.3	(Vs+) –1.2		V
	Common-mode rejection ratio	Input pins at midsupply		[1, 2, 3]	82	100		dB
	Input impedance differential mode	Input pins at midsupply				110 || 1.25		kΩ || pF

6.6 Electrical Characteristics for V_S = 3V (continued)

The following specifications correspond to the respectively identified subgroup temperature (see Section 6.7), unless otherwise noted. Vocm = open (defaults midsupply), V_{OUT} = $2V_{PP}$, Rf = 402Ω, Rload = 499Ω, 50Ω input match, G = 2V/V, single-ended input, differential output, and $\overline{PD}$ = Vs+, unless otherwise noted. See Section 7.1 for a test circuit with an ac-coupled gain of 2V/V, and Section 7.1 for a dc-coupled gain of 2V/V.

PARAMETER		TEST CONDITIONS	SUB-GROUP(1)	MIN	TYP	MAX	UNIT
OUTPUT							
	Output voltage low		[1, 2, 3]		(Vs–) + 0.2	(Vs–) + 0.25	V
	Output voltage high		[1, 2, 3]	(Vs+) – 0.25	(Vs+) – 0.2		V
	Output current drive		[1, 2, 3]	±49	±60		mA
POWER SUPPLY							
	Quiescent operating current		[1, 2, 3]	8.9	9.7	10.6	mA
PSRR	Power-supply rejection ratio	Either supply pin to differential V_{OUT}	[1, 2, 3]	82	100		dB
POWER DOWN							
	Enable voltage threshold		[1, 2, 3]	(Vs–) + 1.7			V
	Disable voltage threshold		[1, 2, 3]			(Vs–) + 0.7	V
	Disable pin bias current	$\overline{PD}$ = Vs– → Vs+	[1, 2, 3]		20	50	nA
	Power-down quiescent current	$\overline{PD}$ = (Vs–) + 0.7V	[1, 2, 3]		2	33	µA
		$\overline{PD}$ = Vs–	[1, 2, 3]		1	8	µA
	Turn-on delay	Time from $\overline{PD}$ = low to V_{OUT} = 90% of final value			100		ns
	Turn-off delay	Time from $\overline{PD}$ = low to V_{OUT} = 10% of final value			60		ns
OUTPUT COMMON-MODE VOLTAGE CONTROL(4)							
	Small-signal bandwidth	Vocm = $100mV_{PP}$			140		MHz
	Slew rate(2)	Vocm = 1V step			350		V/µs
	Gain		[1, 2, 3]	0.975	0.987	0.991	V/V
	Input bias current	Considered positive out of node	[1, 2, 3]	–0.8	0.1	0.8	µA
	Input impedance	Vocm pin driven to midsupply			47 || 1.2		kΩ || pF
	Default voltage offset from midsupply	Vocm pin open	[1, 2, 3]	–50	±10	50	mV
CM V_{OS}	Common-mode offset voltage	Vocm pin driven to midsupply	[1, 2, 3]	–8	±2	8	mV
	CM V_{OS} drift(3)	Vocm pin driven to midsupply		–22	±4	22	µV/°C
	Common-mode loop supply headroom to negative supply	< ±15mV shift from midsupply CM V_{OS}	[1, 2, 3]	0.94			V
	Common-mode loop supply headroom to positive supply	< ±15mV shift from midsupply CM V_{OS}	[1, 2, 3]	1.2			V

(1) For subgroup definitions, see Section 6.7
(2) This slew rate is the average of the rising and falling time estimated from the large-signal bandwidth as: $(V_P / \sqrt{2}) \times 2\pi \times f_{-3dB}$.
(3) Input offset voltage drift, input bias current drift, input offset current drift, and Vocm drift are average values calculated by taking data at the at the maximum-range ambient-temperature end-points, computing the difference, and dividing by the temperature range. Maximum drift set by distribution of a large sampling of devices. Drift is not specified by test or QA sample test.
(4) Specifications are from input Vocm pin to differential output average voltage.

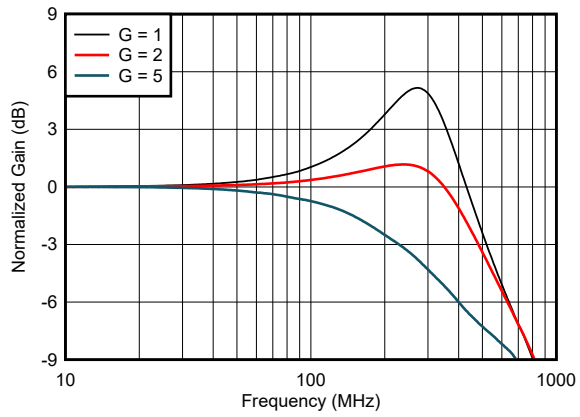
6.7 Quality Conformance Inspection

MIL-STD-883, Method 5005 - Group A

SUBGROUP	DESCRIPTION	TEMPERATURE (°C)
1	Static tests at	25
2	Static tests at	125
3	Static tests at	–55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	–55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	–55

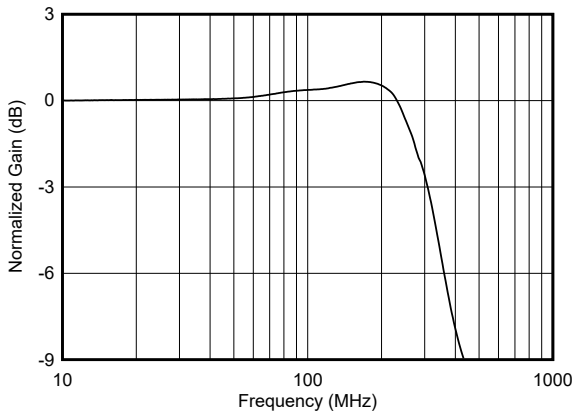
6.8 Typical Characteristics: 5V Single Supply

at Vs+ = 5V, Vs– = GND, R_F = 402Ω, Vocm is open, 50Ω single-ended input to differential output, gain = 2V/V, Rload = 500Ω, and T_A ≅ 25°C (unless otherwise noted)



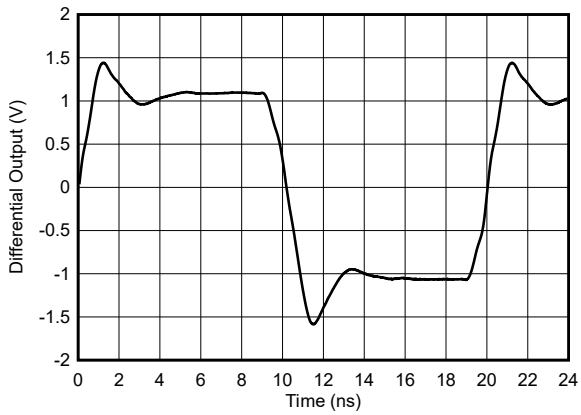
V_{OUT} = 100mV_{PP}

Figure 6-1. Small-Signal Frequency Response vs Gain



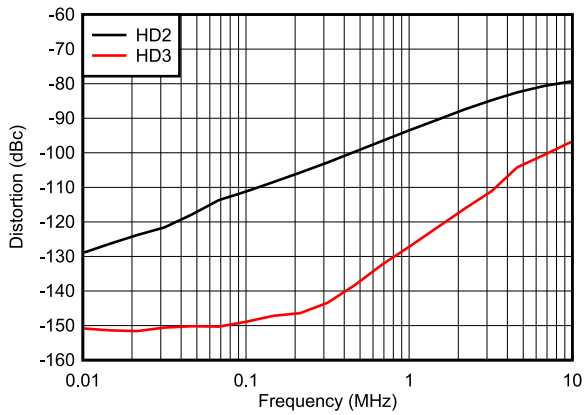
V_{OUT} = 2V_{PP}

Figure 6-2. Large-Signal Frequency Response



50MHz input, 0.5ns input edge rate, single-ended to differential output, split supply, dc-coupled, see Figure 7-2

Figure 6-3. Large-Signal Step Response

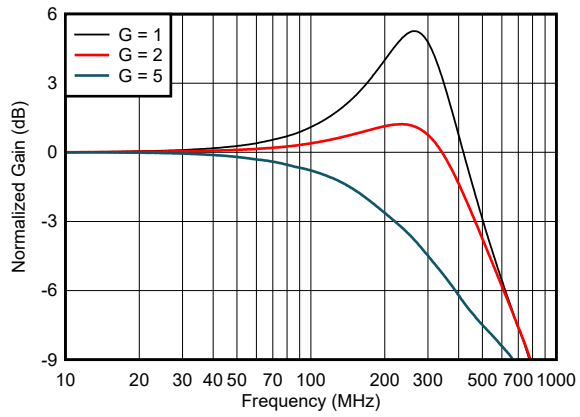


2V_{PP} output, see Figure 7-1

Figure 6-4. Harmonic Distortion Over Frequency

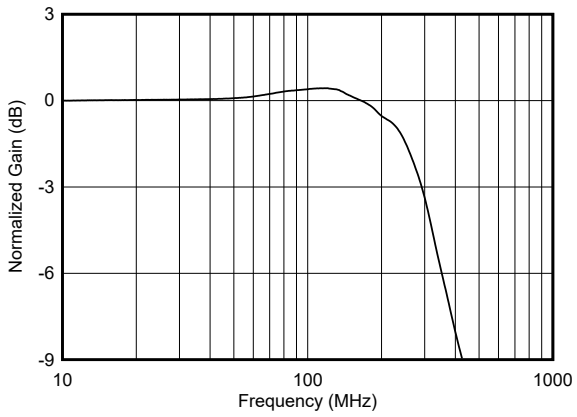
6.9 Typical Characteristics: 3V Single Supply

at Vs+ = 3V, Vs– = GND, Vocm is open, 50Ω single-ended input to differential output, gain = 2V/V, Rload = 500Ω, and T_A ≅ 25°C (unless otherwise noted)



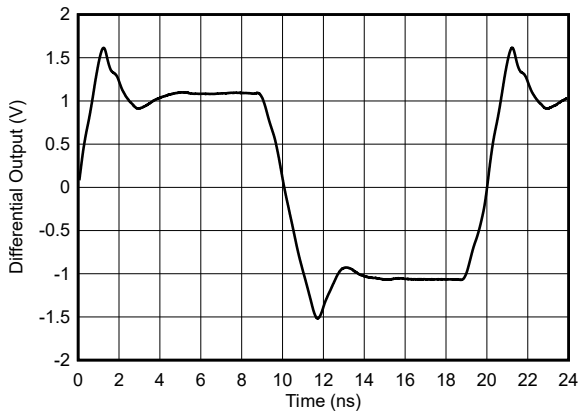
Rf = 402Ω, V_{OUT} = 100mV_{PP}

Figure 6-5. Small-Signal Frequency Response vs Gain



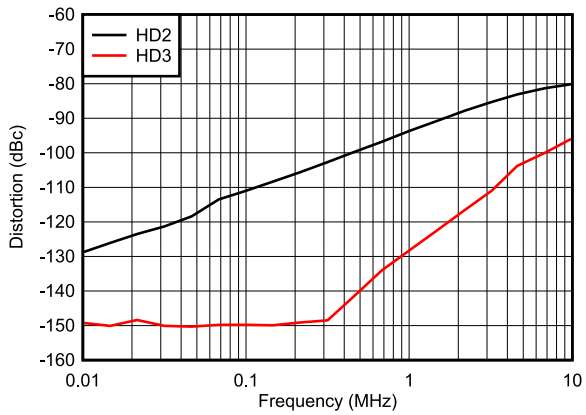
Rf = 402Ω, V_{OUT} = 2V_{PP}

Figure 6-6. Large-Signal Frequency Response



50MHz input, 0.5ns input edge rate, single-ended input to differential output, split supply, DC coupled, see Figure 7-2

Figure 6-7. Large-Signal Step Response



2V_{PP} output, see Figure 7-1 with Vs+ = 3V, Vocm = 1.5V

Figure 6-8. Harmonic Distortion Over Frequency

6.10 Typical Characteristics: 3V to 5V Supply Range

at Vs+ = 3V and 5V, Vs– = GND, Vocm is open, 50Ω single-ended input to differential output, gain = 2V/V, Rload = 500Ω, and T_A ≅ 25°C (unless otherwise noted)

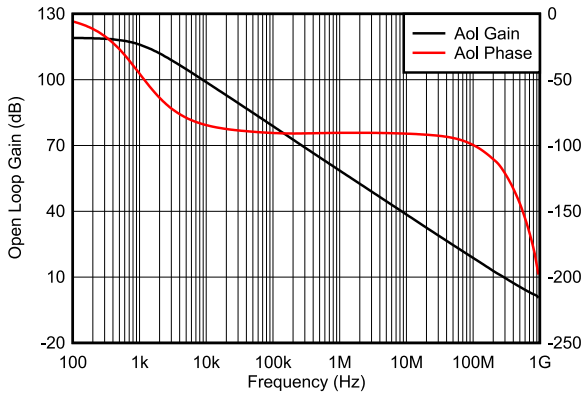
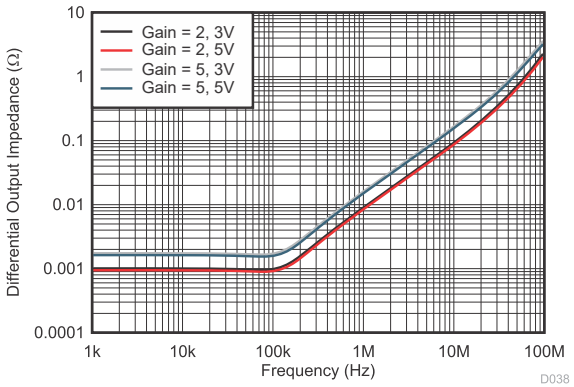


Figure 6-9. Main Amplifier Differential Open-Loop Gain and Phase vs Frequency



Single-ended input to differential output, simulated differential output impedance, see Figure 7-1

Figure 6-10. Closed-Loop Output Impedance

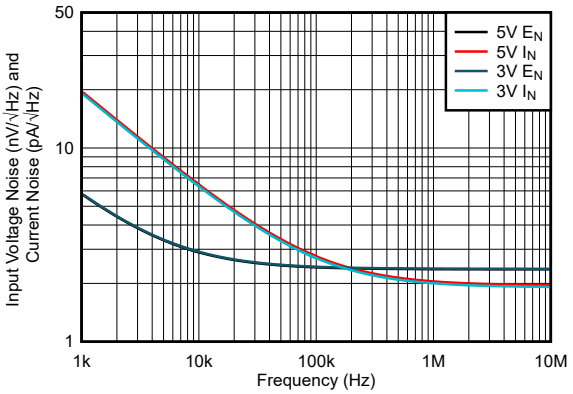
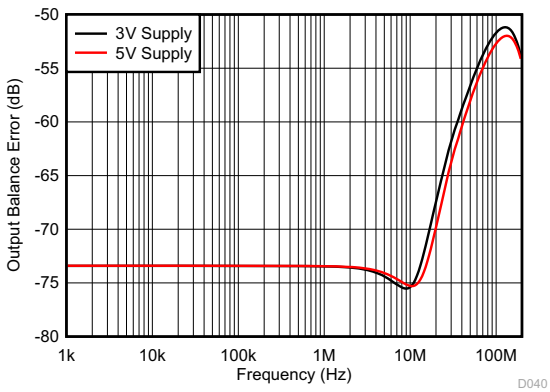
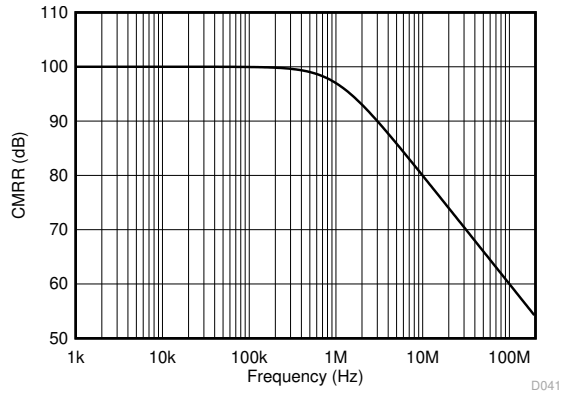


Figure 6-11. Input Spot Noise Over Frequency



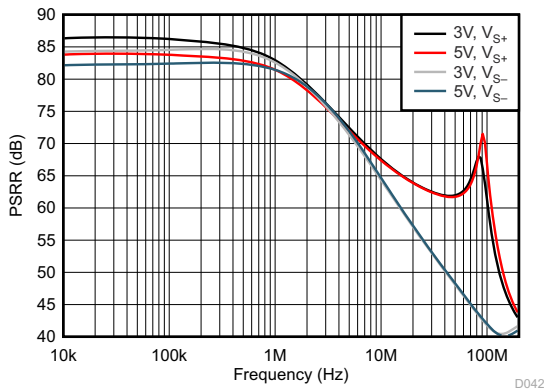
Single-ended input to differential output, gain of 2 (see Figure 7-1), simulated with 1% resistor, worst-case mismatch

Figure 6-12. Output Balance Error Over Frequency



Common-mode in to differential out, gain of 2 simulation

Figure 6-13. CMRR Over Frequency

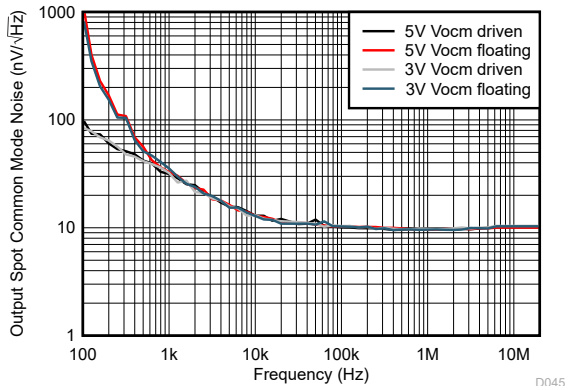


Single-ended to differential, gain of 2 (see Figure 7-1) PSRR simulated to differential output

Figure 6-14. PSRR Over Frequency

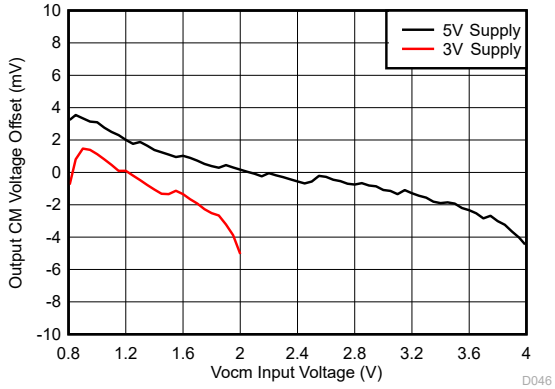
6.10 Typical Characteristics: 3V to 5V Supply Range (continued)

at Vs+ = 3V and 5V, Vs– = GND, Vocm is open, 50Ω single-ended input to differential output, gain = 2V/V, Rload = 500Ω, and T_A ≅ 25°C (unless otherwise noted)



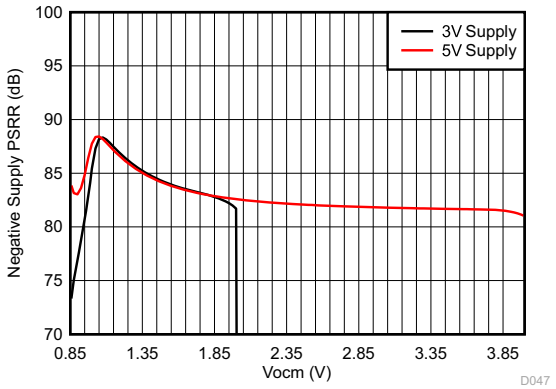
Vocm input either driven to midsupply by low impedance source, or allowed to float and default to midsupply

Figure 6-15. Output Common-Mode Noise



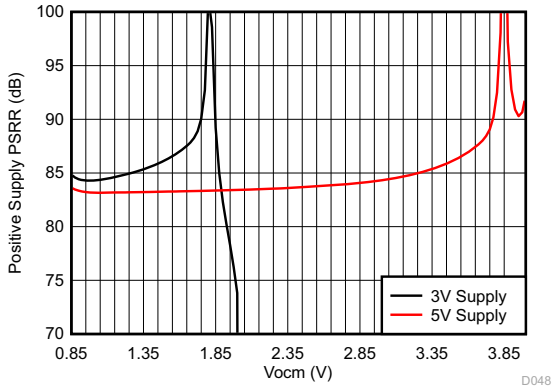
Average Vocm output offset of 37 units, standard deviation < 2.5mV, see Figure 7-2

Figure 6-16. Vocm Offset vs Vocm Setting



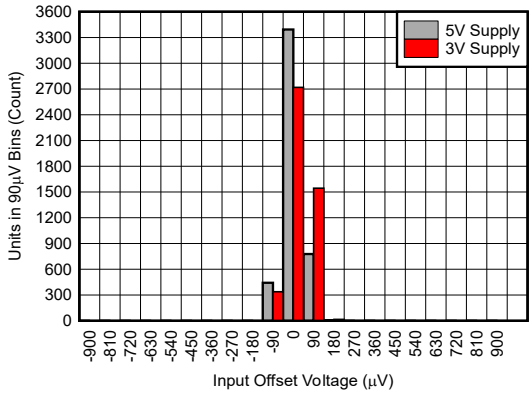
Single-ended to differential gain of 2 (see Figure 7-1), PSRR for negative supply to differential output (1kHz simulation)

Figure 6-17. –PSRR vs Vocm Approaching Vs–



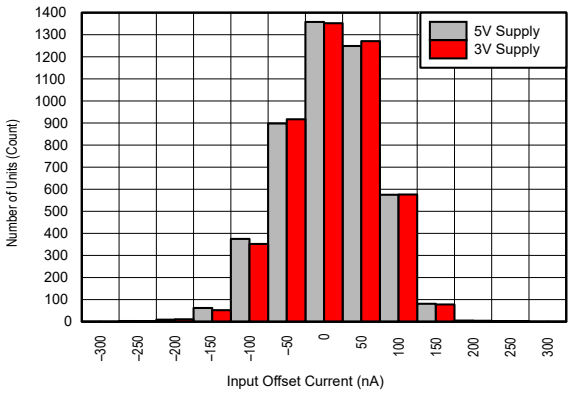
Single-ended to differential gain of 2 (see Figure 7-1), PSRR for positive supply to differential output (1kHz simulation)

Figure 6-18. +PSRR vs Vocm Approaching Vs+



Total of 4618 units for each supply.
For Vs = 5V: µ = -35.1µV, σ = 38.9µV

Figure 6-19. Input Offset Voltage

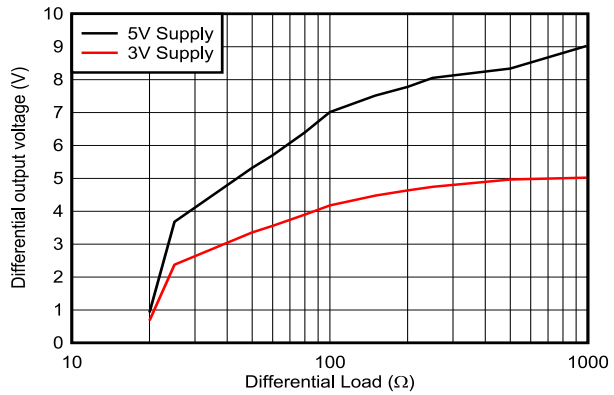


Total of 4618 units for each supply.
For Vs = 5V: µ = 16.7nA, σ = 62.3nA

Figure 6-20. Input Offset Current

6.10 Typical Characteristics: 3V to 5V Supply Range (continued)

at Vs+ = 3V and 5V, Vs– = GND, Vocm is open, 50Ω single-ended input to differential output, gain = 2V/V, Rload = 500Ω, and T_A ≅ 25°C (unless otherwise noted)



Maximum differential output swing, Vocm at midsupply

Figure 6-21. Differential Output Voltage vs Rload

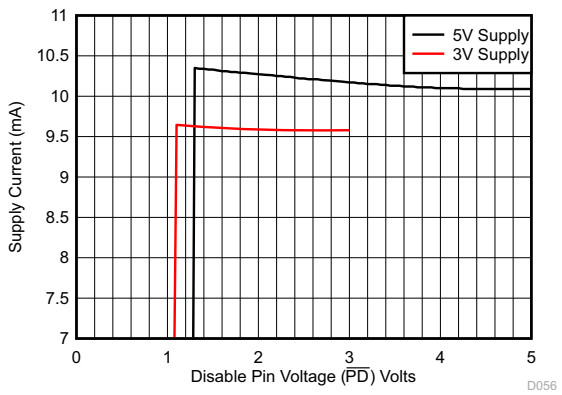
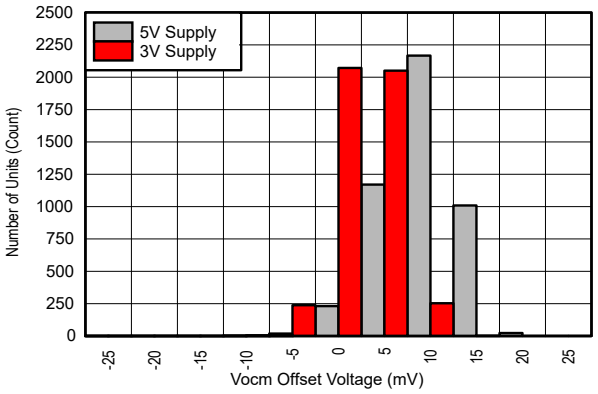
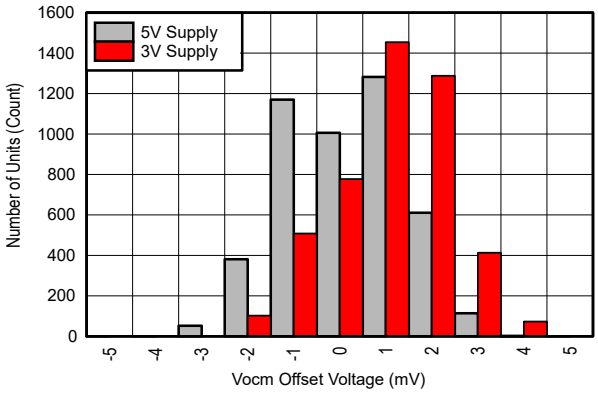


Figure 6-22. Supply Current vs $\overline{PD}$ Voltage



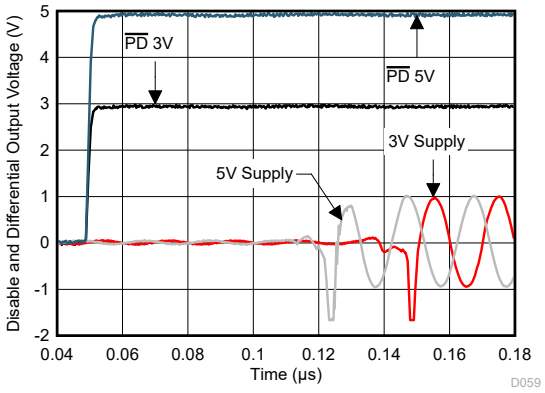
Vocm input floating. Total of 4618 units for each supply,
For Vs = 5V: μ = 6.8mV, σ = 3.9mV

Figure 6-23. Common-Mode Output Offset from Vs+ / 2 Default Value



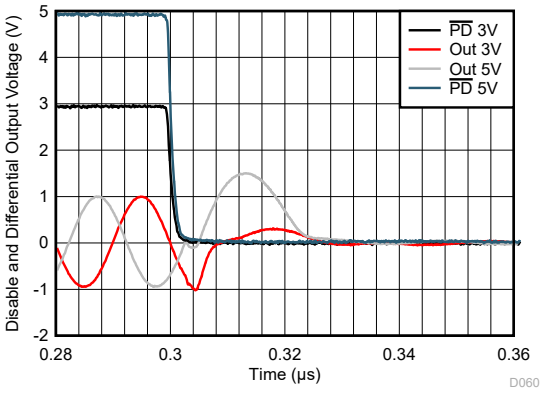
Total of 4618 units for each supply,
For Vs = 5V: μ = 0.3mV, σ = 1.3mV

Figure 6-24. Common-Mode Output Offset from Driven Vocm



10MHz, 1V_{PP} input single to differential gain of 2,
see Figure 7-2

Figure 6-25. $\overline{PD}$ Turn-On Waveform



10MHz, 1V_{PP} input single to differential gain of 2,
see Figure 7-2

Figure 6-26. $\overline{PD}$ Turn-Off Waveform

7 Parameter Measurement Information

7.1 Example Characterization Circuits

The LMH5485-SP offers the advantages of a fully differential amplifier (FDA) design, with the trimmed input offset voltage of a precision op amp. The FDA is an extremely flexible device that provides a purely differential output signal centered on a settable output common-mode level. The primary options revolve around the choices of single-ended or differential inputs, ac-coupled or dc-coupled signal paths, gain targets, and resistor Value selections. Differential sources can certainly be supported and are often simpler to both implement and analyze. Figure 7-1 and Figure 7-2 show examples of both ac and dc coupled single-ended to differential circuits.

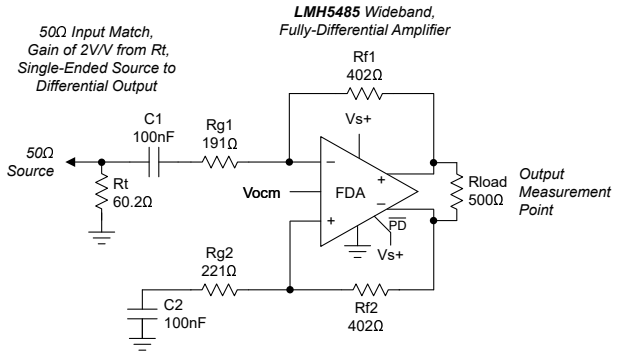


Figure 7-1. AC-Coupled, Single-Ended Source to a Differential Gain of a 2V/V Test Circuit

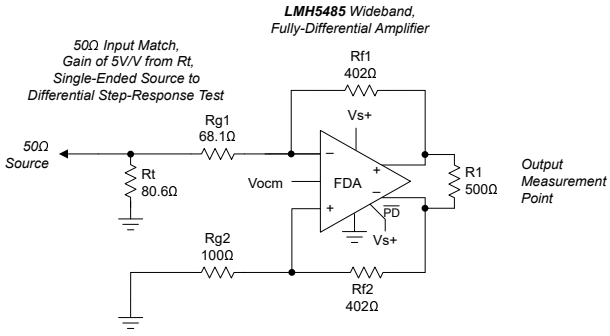


Figure 7-2. DC-Coupled, Single-Ended-to-Differential, Basic Test Circuit Set for a Gain of 5V/V

Most lab equipment is single-ended; therefore, the characterization circuits typically operate with a single-ended, matched, 50Ω input termination to a differential output at the FDA output pins. That output is then translated back to single-ended through a variety of baluns (or transformers) depending on the test and frequency range. DC-coupled, step-response testing uses two 50Ω scope inputs with trace math.

Figure 7-1 shows how most characterization plots fix the R_f value at 402Ω. This value is completely flexible in application, but the 402Ω provides a good compromise for the issues linked to this value, specifically:

- Added output loading. The FDA appears like an inverting op amp design with both feedback resistors as an added load across the outputs (approximate total differential load in Figure 7-1 is 500Ω || 804Ω = 308Ω).
- Noise contributions because of the resistor values. The resistors contribute both a 4kTR term and provide gain for the input current noise.
- Parasitic feedback pole at the input summing nodes. This pole created by the feedback R value and the 1.25pF differential input capacitance (as well as any board layout parasitic) introduces a zero in the noise gain, decreasing the phase margin in most situations. This effect must be managed for best frequency response flatness or step response overshoot. The 402Ω value selected does degrade the phase margin slightly over a lower value, but does not decrease the loading significantly from the nominal 500Ω value across the output pins.

8 Detailed Description

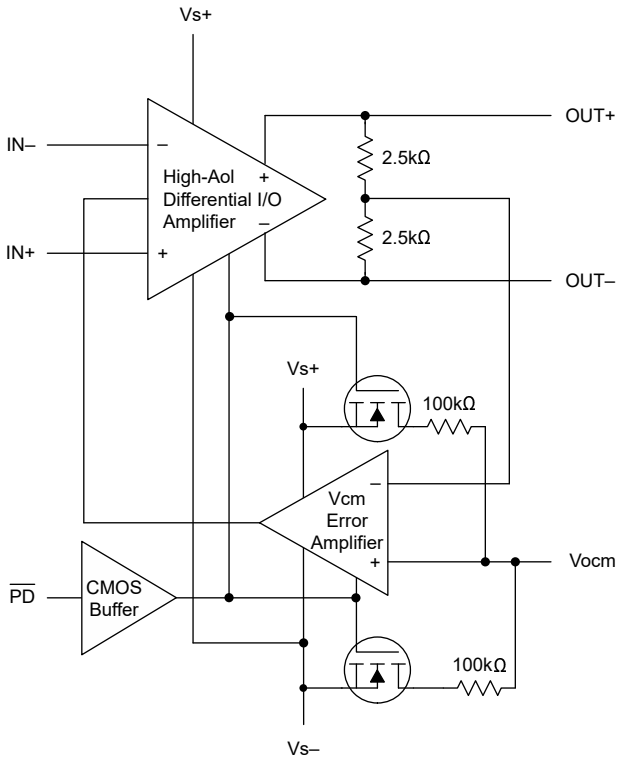
8.1 Overview

The LMH5485-SP is a voltage-feedback-based, fully-differential amplifier (FDA) with a trimmed supply current and input offset voltage. The core differential amplifier is a slightly decompensated voltage-feedback design with a high slew-rate, precision input stage. This design gives a 490MHz, gain of 2V/V, small-signal bandwidth shown in the characterization curves, with a 1400V/µs slew rate, yielding approximately a 315MHz, $2V_{PP}$, large-signal bandwidth in the same circuit configuration.

The outputs offer near rail-to-rail output swing (0.2V headroom to either supply), while the device inputs are negative rail inputs with approximately 1.2V of headroom required to the positive supply. Figure 7-2 shows how this negative rail input directly supports a bipolar input around ground in a dc-coupled, single-supply design. Similar to all FDA devices, the output average voltage (common-mode) is controlled by a separate common-mode loop. The target for this output average is set by the Vocm input pin that can be either floated to default near midsupply or driven to a desired output common-mode voltage. The Vocm range extends from a very low 0.91V above the negative supply to 1.1V below the positive supply, supporting a wide range of modern analog-to-digital converter (ADC) input common-mode requirements using a single 2.7V to 5.4V supply range for the LMH5485-SP.

A power-down pin ($\overline{PD}$) is included. Pull the $\overline{PD}$ pin voltage to the negative supply to turn the device off, putting the LMH5485-SP into a very-low quiescent current state. To use the full supply range of the device, keep the device in normal operation by keeping the $\overline{PD}$ pin asserted high. When the device is disabled, remember that the signal path is still present through the passive external resistors. Input signals applied to a disabled LMH5485-SP, as with any disabled FDA device, still appear at the outputs at some level through this passive resistor path.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Differential I/O

The LMH5485-SP combines a core differential I/O, high-gain block with an output common-mode sense that is compared to a reference voltage and then fed back into the main amplifier block to control the average output to that reference. The differential I/O block is a classic, high open-loop gain stage with a dominant pole at approximately 900Hz. This voltage feedback structure projects a single-pole, unity-gain A_{OL} at 850MHz (gain bandwidth product). The high-speed differential outputs include an internal averaging resistor network to sense the output common-mode voltage. This voltage is compared by a separate Vcm error amplifier to the voltage on the Vocm pin. If floated, this reference is at half the total supply voltage across the device using two 100kΩ resistors. This Vcm error amplifier transmits a correction signal into the main amplifier to force the output average voltage to meet the target voltage on the Vocm pin. The bandwidth of this error amplifier is approximately the same bandwidth as the main differential I/O amplifier.

The differential outputs are collector outputs to obtain the rail-to-rail output swing. These outputs are relatively high-impedance, open-loop sources; however, closing the loop provides a very low output impedance for load driving. No output current limit or thermal shutdown features are provided in this lower-power device. The differential inputs are PNP inputs to provide a negative-rail input range.

To operate the LMH5485-SP connect the OUT– pin to the IN+ pin through an Rf, and the OUT+ pin to the IN– pin through the same value of Rf. Bring in the inputs through additional resistors to the IN+ and IN– pins. The differential I/O op amp operates similarly to an inverting op amp structure where the source must drive the input resistor and the gain is the ratio of the feedback to the input resistor.

8.3.2 Power-Down Control Pin ($\overline{PD}$)

The LMH5485-SP includes a power-down control pin, $\overline{PD}$. This pin must be asserted high for correct amplifier operation. The $\overline{PD}$ pin cannot be floated because there is no internal pullup or pull-down resistor on this pin to reduce disabled power consumption. Asserting this pin low (within 0.7V of the negative supply) puts the LMH5485-SP into a very low quiescent state (approximately 2µA). Switches in the default Vocm resistor string open to eliminate the fixed bias current (25µA) across the supply in this 200kΩ voltage divider to mid-supply.

8.3.2.1 Operating the Power Shutdown Feature

When the $\overline{PD}$ pin is asserted high, close to the positive supply, the device is in normal active mode of operation. To disable the device for reduced power consumption, assert the $\overline{PD}$ low, close to the negative supply. Figure 6-22 shows the $\overline{PD}$ pin voltage and the corresponding quiescent current drawn. For applications that require the device to only be powered on when the supplies are present, tie the $\overline{PD}$ pin to the positive supply voltage.

The disable operation is referenced from the negative supply (normally, ground). For split-supply operation, with the negative supply below ground, a disable control voltage below ground is required to turn the LMH5485-SP off when the negative supply exceeds –0.7V.

For single-supply operation, a minimum of 1.7V greater than the negative supply (ground, in this case) is required for proper operation. This minimum logic-high level allows for direct operation from 1.8V supply logic.

8.3.3 Input Overdrive Operation

The LMH5485-SP input stage architecture is intrinsically robust to input overdrives with the series input resistor required by all applications. High input overdrives cause the outputs to limit the maximum swings with the remaining input current through the Rg resistors absorbed by internal, back-to-back protection diodes across the two inputs. These diodes are normally off in application, and only turn on to absorb the currents that a large input overdrive can produce through the source impedance and or the series Rg elements required by all designs.

The internal input diodes can safely absorb up to ±15mA in an overdrive condition. For designs that require more current to be absorbed, consider adding an external protection diode.

8.4 Device Functional Modes

This wideband FDA requires external resistors for correct signal-path operation. When configured for the desired input impedance and gain setting with these external resistors, the amplifier can be either *on* with the $\overline{PD}$ pin asserted to a voltage greater than (Vs–) + 1.7V or turned *off* by asserting $\overline{PD}$ low. Disabling the amplifier shuts off the quiescent current and stops the correct amplifier operation. The signal path is still present for the source signal through the external resistors.

The Vocm control pin sets the output average voltage. Left open, Vocm defaults to an internal midsupply value. Driving this high-impedance input with a voltage reference within the valid range sets a target for the internal Vcm error amplifier.

8.4.1 Operation from Single-Ended Sources to Differential Outputs

One of the most useful features supported by the FDA device is an easy conversion from a single-ended input to a differential output centered on a user-controlled, common-mode level. While the output side is relatively straightforward, the device input pins move in a common-mode sense with the input signal. This common-mode voltage at the input pins moving with the input signal acts to increase the apparent input impedance to be greater than the Rg value. This input active impedance issue applies to both ac- and dc-coupled designs, and requires somewhat more complex solutions for the resistors to account for this active impedance, and is shown in the following subsections.

8.4.1.1 AC-Coupled Signal Path Considerations for Single-Ended Input to Differential Output Conversion

When the signal path can be ac-coupled, the dc biasing for the LMH5485-SP becomes a relatively simple task. In all designs, start by defining the output common-mode voltage. The ac-coupling issue can be separated for the input and output sides of an FDA design. In any case, the design starts by setting the desired Vocm. When an ac-coupled path follows the output pins, the best linearity is achieved by operating Vocm at mid-supply. The Vocm voltage must be within the linear range for the common-mode loop, as specified in the headroom specifications (approximately 0.91V greater than the negative supply and 1.1V less than the positive supply). If the output path is also ac coupled, simply letting the Vocm control pin float is typically preferred to get a midsupply default Vocm bias with minimal elements. To limit noise, place a 0.1µF decoupling capacitor on the Vocm pin to ground.

After Vocm is defined, check the target output voltage swing and ensure that the Vocm plus the positive or negative output swing on each side does not clip into the supplies. Check that Vocm ±Vp does not exceed the absolute supply rails for this rail-to-rail output (RRO) device.

Going to the device input pins side, because both the source and balancing resistor on the nonsignal input side are dc blocked (see Figure 7-1), no common-mode current flows from the output common-mode voltage, thus setting the input common-mode equal to the output common-mode voltage.

This input headroom also sets a limit for higher Vocm voltages. Because the input Vicm is the output Vocm for ac-coupled sources, the 1.2V minimum headroom for the input pins to the positive supply overrides the 1.1V headroom limit for the output Vocm. The input signal also moves this input Vicm around the dc bias point.

8.4.1.2 DC-Coupled Input Signal Path Considerations for Single-Ended to Differential Conversion

The output considerations remain the same as for the ac-coupled design. Again, the input can be dc-coupled while the output is ac-coupled. A dc-coupled input with an ac-coupled output can have some advantages to move the input Vicm down if the source is ground referenced. Figure 7-2 shows how when the source is dc-coupled into the LMH5485-SP, both sides of the input circuit must be dc coupled to retain differential balance. Normally, the nonsignal input side has an Rg element biased to whatever the source midrange is expected to be. Providing this midscale reference gives a balanced differential swing around Vocm at the outputs.

One significant consideration for a dc-coupled input is that Vocm sets up a common-mode bias current from the output back through Rf and Rg to the source on both sides of the feedback. Without input balancing networks, the source must sink or source this dc current. After the input signal range and biasing on the other Rg element is set, check that the voltage divider from Vocm to V_{IN} through Rf and Rg (and possibly Rs) establishes an input Vicm at the device input pins that is in range. If the average source is at ground, the negative rail input stage for

the LMH5485-SP is in range for applications using a single positive supply and a positive output Vocm setting because this dc current lifts the average FDA input summing junctions up off of ground to a positive voltage (the average of the V+ and V– input pin voltages on the FDA).

8.4.2 Differential-Input to Differential-Output Operation

In many ways, this method is a much simpler way to operate the FDA from a design equations perspective. Assuming the two sides of the circuit are balanced with equal Rf and Rg elements, the differential input impedance is the sum of the two Rg elements to a differential inverting summing junction. In these designs, the input common-mode voltage at the summing junctions does not move with the signal, but must be DC biased in the allowable range for the input pins with consideration given to the voltage headroom required from each supply. Slightly different considerations apply to AC- or DC-coupled, differential-in to differential-out designs, as described in the following sections.

8.4.2.1 AC-Coupled, Differential-Input to Differential-Output Design Issues

There are two typical ways to use the LMH5485-SP with an ac-coupled differential source. In the first method, the source is differential and can be coupled in through two blocking capacitors. The second method uses either a single-ended or a differential source and couples in through a transformer (or balun). Figure 8-1 shows a typical blocking capacitor approach to a differential input. An optional input differential termination resistor (Rm) is included in this design. This Rm element allows the input Rg resistors to be scaled up while still delivering lower differential input impedance to the source. In this example, the Rg elements sum to show a 200Ω differential impedance, while the Rm element combines in parallel to give a net 100Ω, ac-coupled, differential impedance to the source. Again, the design proceeds by selecting the Rf element values, then the Rg to set the differential gain, then an Rm element (if needed) to achieve a target input impedance. Alternatively, the Rm element can be eliminated, the Rg elements set to the desired input impedance, and Rf set to the get the differential gain (= Rf / Rg).

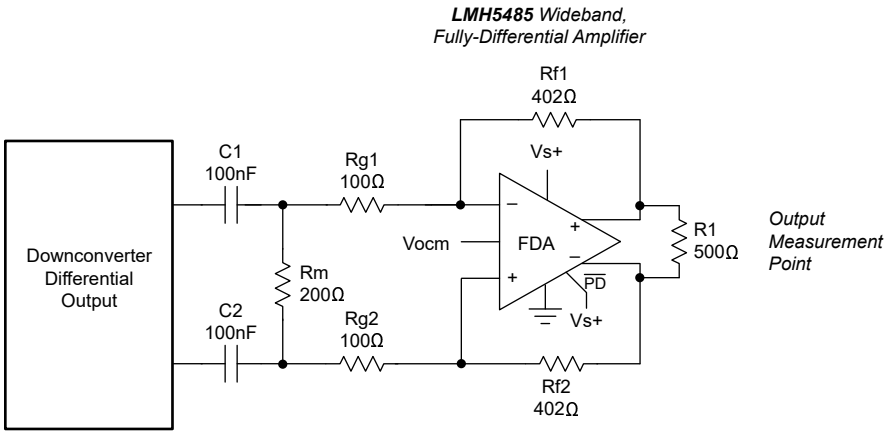


Figure 8-1. Down-Converting Mixer Delivering an AC-Coupled Differential Signal to the LMH5485-SP

The dc biasing here is very simple. The output Vocm is set by the input control voltage. Because there is no dc current path for the output common-mode voltage, that dc bias also sets the input pins common-mode operating points.

Transformer input coupling allows either a single-ended or differential source to be coupled into the LMH5485-SP, which also improves the input-referred noise figure. These designs assume a source impedance that must be matched in the balun interface. Figure 8-2 shows the simplest approach where an example 1:2 turns ratio step-up transformer is used from a 50Ω source.

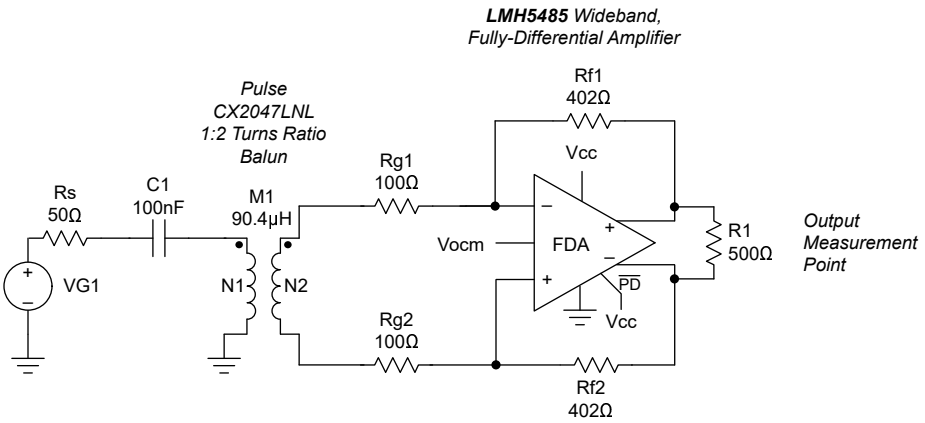


Figure 8-2. Input Balun Interface Delivers a Differential Input to the LMH5485-SP

In this example, this 1:2 turns ratio step-up transformer provides a source and load match from the 50Ω source if the secondary is terminated in 200Ω (turns-ratio squared is the impedance ratio across a balun). The two Rg elements provide that termination as these resistors sum to the differential virtual ground at the FDA summing junctions. The input blocking cap (C1) is optional and included only to eliminate dc shorts to ground from the source. This implementation often improves the total noise figure compared to using just the FDA, as this configuration allows for reduction of the amplifier noise gain.

8.4.2.2 DC-Coupled, Differential-Input to Differential-Output Design Issues

Operating the LMH5485-SP with a dc-coupled differential input source is very simple and only requires that the input pins stay in range of the dc common-mode operating voltage. One example is a dc-to-50MHz quadrature down-converter output. These outputs typically sit on a dc level with some internal source impedance to the external loads. The example of Figure 8-3 shows a design using the LMH5485-SP with a simple, passive RLC filter to the inputs (the Rg elements act as the differential termination for the filter design). From the original source behind the internal 250Ω outputs, this circuit is a gain of 1 to the LMH5485-SP output pins. The DC common-mode operating voltage level shifts from the 1.2V internal, to the mixer, to an output at the ADC Vcm voltage of 0.95V. In this case, a simple average of the two dc voltages in the gain of 1 stage gives a 1.08V input pin common-mode result that is well within range.

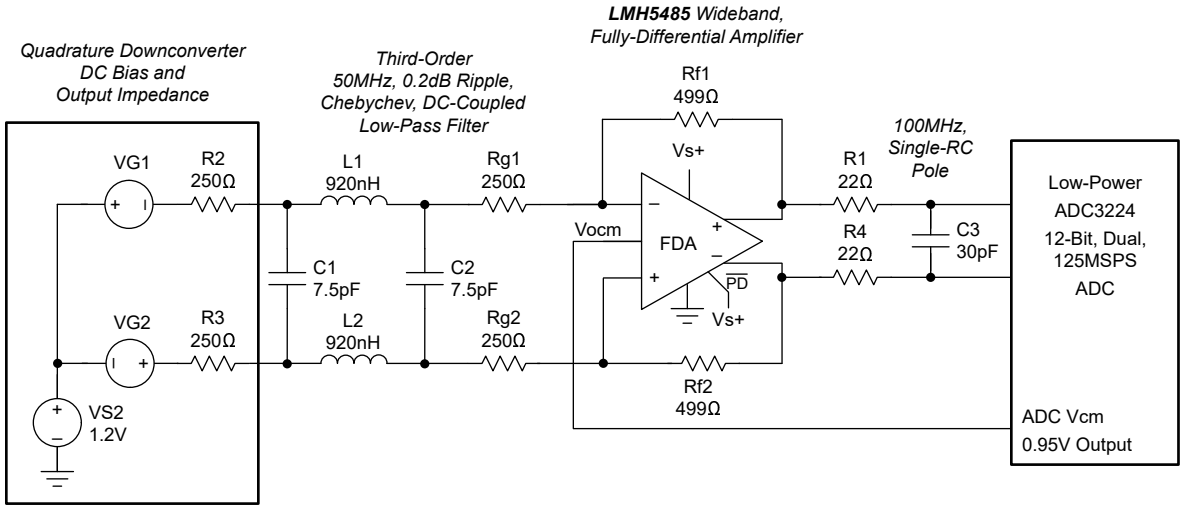


Figure 8-3. Example DC-Coupled, Differential I/O Design From a Quadrature Mixer to an ADC

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The LMH5485-SP is an effective ADC driver over a broad range of applications. In this example the LMH5485-SP is in a gain of 2V/V, matched input of 50Ω to an output set to 0.95V common-mode followed by a third-order Bessel filter with approximately 20MHz of bandwidth, designed for interfacing with a high-speed ADC.

9.2 Typical Applications

9.2.1 Interfacing to High-Performance ADCs

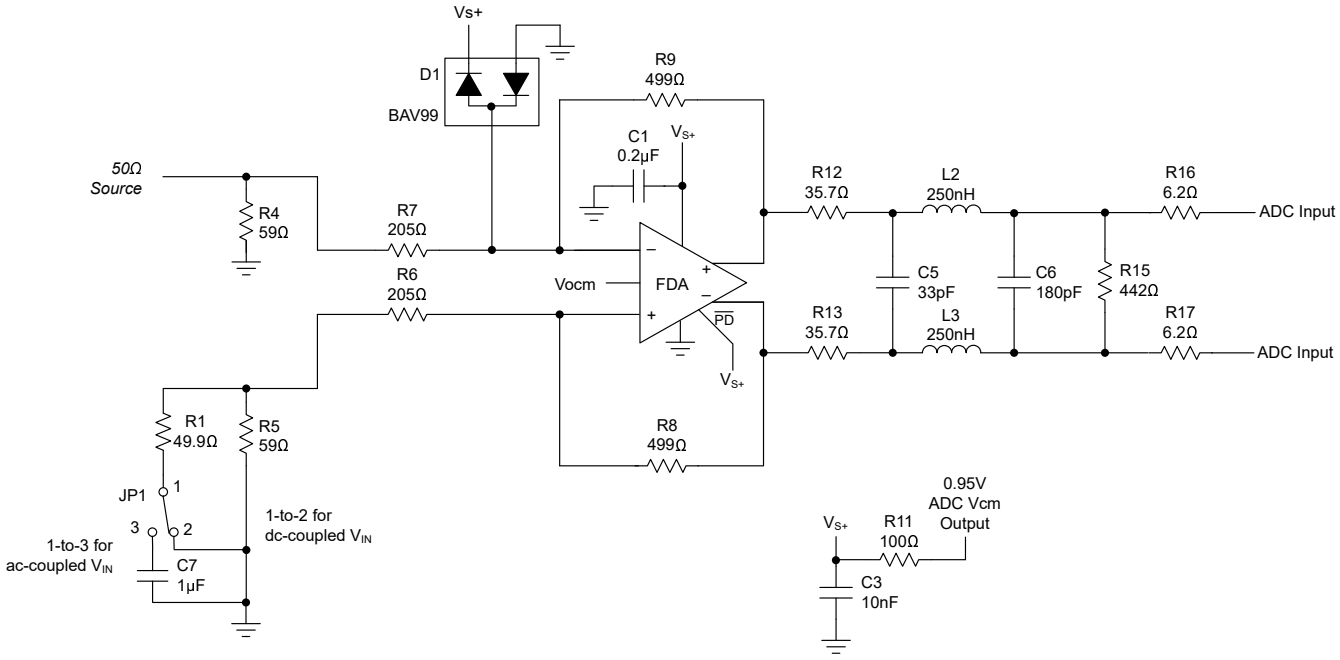


Figure 9-1. DC-Coupled, Bipolar Input Gain of 2V/V Single-Ended to Differential Interface to ADC

9.2.1.1 Design Requirements

In this example design, an impedance matched input assuming a 50Ω source is implemented with a dc-coupled gain of 2V/V to the ADC. This configuration effectively reduces the required full-scale input to ±0.5V for a $2V_{PP}$ full-scale input ADC. Add a low insertion-loss interstage filter to the ADC to control the broadband noise where the goal is to show minimal SNR reduction in the FFT, as well as minimal degradation in SFDR performance.

9.2.1.2 Detailed Design Procedure

The LMH5485-SP provides a simple interface to a wide variety of precision SAR, ΔΣ, or higher-speed pipeline ADCs. To deliver the exceptional distortion at the output pins, considerably wider bandwidth than typically required in the signal path to the ADC inputs is provided by the LMH5485-SP. For instance, the gain-of-2, single-ended-to-differential design example provides approximately a 500MHz, small-signal bandwidth. Even if the source signal is Nyquist bandlimited, this broad bandwidth can possibly integrate enough LMH5485-SP noise to degrade the SNR through the ADC if the broadband noise is not bandlimited between the amplifier and ADC. Figure 9-1 shows an example dc-coupled, gain-of-2 interface with a controlled, interstage-bandwidth filter.

Designed for a DC-coupled 50Ω input match, this design starts with a 499Ω feedback resistor, and provides a gain of 2.35V/V to the LMH5485-SP output pins. The third-order interstage, low-pass filter provides a 20MHz Bessel response with a 0.85V/V insertion loss to the ADC, providing a net gain of 2V/V from board edge to the ADC inputs. Although the LMH5485-SP can absorb overdrives, an external protection element is added using the BAV99 low-capacitance device (see also Figure 9-1). For dc-coupled testing, pins 1 and 2 of JP1 are jumpered together. When the source is an ac-coupled, 50Ω source, pins 2 and 3 of JP1 are jumpered to maintain differential balance.

9.2.1.3 Application Curve

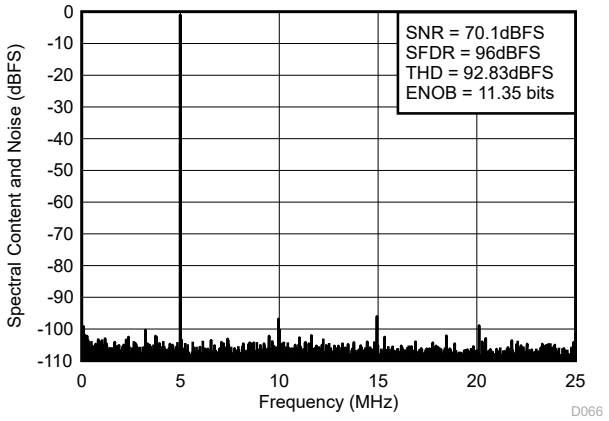


Figure 9-2. 5MHz FFT, 50MSPS Test for the Gain of 2 Interface

9.3 Power Supply Recommendations

The LMH5485-SP is principally intended to operate with a nominal single-supply voltage of 3V to 5V. Supply decoupling is required, as described in *Section 9.4.1*. The amplifier signal path is flexible for single or split-supply operation. Most applications are intended to be single supply, but any split-supply design can be used, as long as the total supply across the LMH5485-SP is less than 5.25V and the required input, output, and common-mode pin headroom to each supply are observed. Left open, the V_{OCM} pin defaults to near midsupply for any combination of split or single supplies used. The disable pin is negative-rail referenced. Using a negative supply requires the disable pin to be pulled down to within 0.7V of the negative supply to disable the amplifier.

9.4 Layout

9.4.1 Layout Guidelines

Similar to all high-speed devices, best system performance is achieved with a close attention to board layout. The LMH5485-SP evaluation module (EVM) shows a good example of high frequency layout techniques as a reference. This EVM includes numerous extra elements and features for characterization purposes that do not apply to some applications. General high-speed, signal-path layout suggestions include the following:

- Continuous ground planes are preferred for signal routing with matched impedance traces for longer runs; however, ensure that ground and power planes around the capacitive sensitive input and output device pins are open. After the signal is sent into a resistor, the parasitic capacitance becomes more of a band-limiting issue and less of a stability issue.
- Use good, high-frequency decoupling capacitors (0.1µF) on the ground plane at the device power pins. Higher value capacitors (2.2µF) are required, but can be placed further from the device power pins and shared among devices. Also, add a supply-decoupling capacitor across the two power supplies (for bipolar operation). For best high-frequency decoupling, consider X2Y supply-decoupling capacitors that offer a much higher self-resonance frequency over standard capacitors.
- For each LMH5485-SP, attach a separate 0.1µF capacitor to a nearby ground plane. With cascaded or multiple parallel channels, including ferrite beads from the larger capacitor is often useful to the local high-frequency decoupling capacitor.
- When using differential signal routing over any appreciable distance, use microstrip layout techniques with matched impedance traces.
- The input summing junctions are very sensitive to parasitic capacitance. Connect any Rg elements into the summing junction with minimal trace length to the device pin side of the resistor. The other side of the Rg elements can have more trace length if needed to the source or to ground.

9.4.2 Layout Example

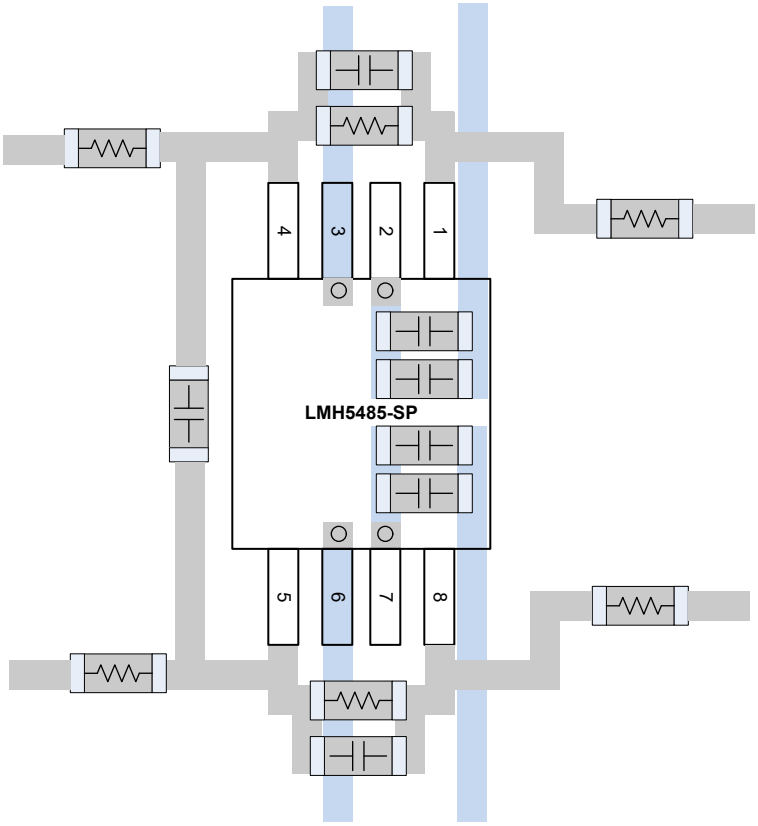


Figure 9-3. Layout Example

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Design for a Wideband, Differential Transimpedance DAC Output* application report
- Texas Instruments, *Extending Rail-to-Rail Output Range for Fully Differential Amplifiers to Include True Zero Volts* reference guide
- Texas Instruments, *LMH6554 2.8GHz Ultra Linear Fully Differential Amplifier* data sheet
- Texas Instruments, *LMH5485-SP-EVM* user's guide
- Texas Instruments, *Maximizing the dynamic range of analog front ends having a transimpedance amplifier* technical brief
- Texas Instruments, *Fully Differential Amplifiers* application note
- Texas Instruments, *Maximizing Signal Chain Distortion Performance Using High Speed Amplifiers* app note
- Texas Instruments, TI Precision Labs - Fully Differential Amplifiers video series

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.4 Trademarks

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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (November 2025) to Revision C (June 2026)	Page
• Added preview note to 5962R1920401VXC device	1

Changes from Revision A (December 2021) to Revision B (November 2025)	Page
• Changed data sheet status from advanced information (preview) to production data (active)	1

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMH5485HKX/EM	Active	Production	CFP (HKX) | 8	1 | TUBE	Yes	NIAU	N/A for Pkg Type	25 to 25	LMH5485/EM

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

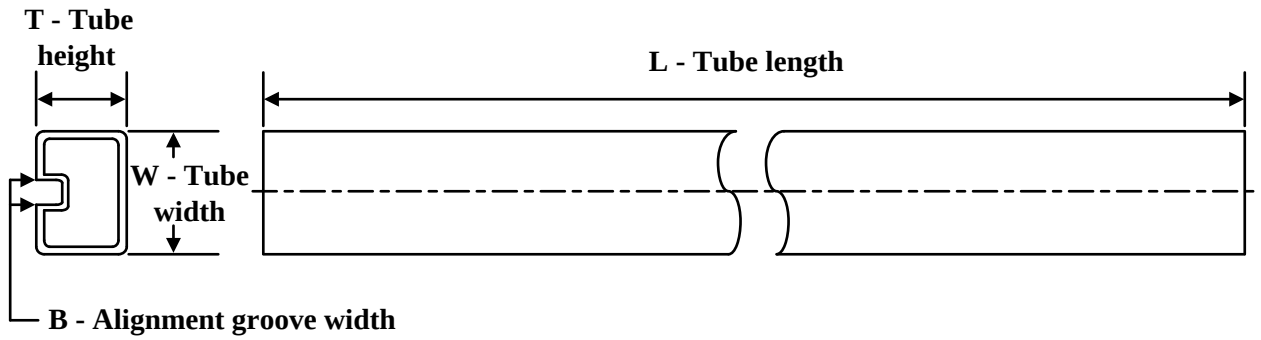
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMH5485HKX/EM	HKX	CFP (HSL)	8	1	506.98	26.16	6220	NA

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