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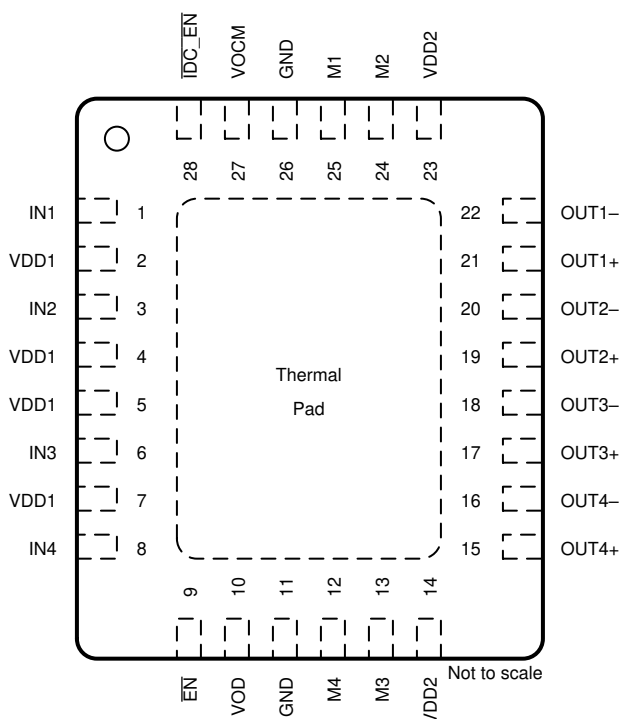
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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision * (December 2020) to Revision A (November 2021)</b>	<b>Page</b>
• Change the status of the data sheet from: <i>Advanced Information</i> to: <i>Production Data</i> .....	<b>1</b>

## 5 Pin Configuration and Functions



**Figure 5-1. RHF Package, 28-Pin VQFN, (Top View)**

**Table 5-1. Pin Functions**

PIN		TYPE <sup>(2)</sup>	DESCRIPTION
NAME	NO.		
$\overline{\text{EN}}$	9	I	Device enable pin. $\overline{\text{EN}}$ = logic low = normal operation (default); $\overline{\text{EN}}$ = logic high = low power mode. <sup>(1)</sup>
GND	11, 26	I	Amplifier ground.
$\overline{\text{IDC\_EN}}$	28	I	Ambient light cancellation loop enable. $\overline{\text{IDC\_EN}}$ = logic low = enable DC cancellation (default); $\overline{\text{IDC\_EN}}$ = logic high = disable DC cancellation. <sup>(1)</sup>
IN1	1	I	Transimpedance amplifier input - Channel 1.
IN2	3	I	Transimpedance amplifier input - Channel 2.
IN3	6	I	Transimpedance amplifier input - Channel 3.
IN4	8	I	Transimpedance amplifier input - Channel 4.
M1	25	I	Select Channel 1. M1 = logic high = Channel 1 operational and output switches closed. M1 = logic low (default) = Channel 1 in standby power mode and output switches open. <sup>(1)</sup>
M2	24	I	Select Channel 2. M2 = logic high = Channel 2 operational and output switches closed. M2 = logic low (default) = Channel 2 in standby power mode and output switches open. <sup>(1)</sup>
M3	13	I	Select Channel 3. M3 = logic high = Channel 3 operational and output switches closed. M3 = logic low (default) = Channel 3 in standby power mode and output switches open. <sup>(1)</sup>
M4	12	I	Select Channel 4. M4 = logic high = Channel 4 operational and output switches closed. M4 = logic low (default) = Channel 4 in standby power mode and output switches open. <sup>(1)</sup>
OUT1–	22	O	Channel 1 inverting amplifier output. When light is incident on the photodiode the output pin transitions in a negative direction from the no light condition.
OUT1+	21	O	Channel 1 noninverting amplifier output. When light is incident on the photodiode the output pin transitions in a positive direction from the no light condition.
OUT2–	20	O	Channel 2 inverting amplifier output. When light is incident on the photodiode the output pin transitions in a negative direction from the no light condition.
OUT2+	19	O	Channel 2 noninverting amplifier output. When light is incident on the photodiode the output pin transitions in a positive direction from the no light condition.

**Table 5-1. Pin Functions (continued)**

PIN		TYPE <sup>(2)</sup>	DESCRIPTION
NAME	NO.		
OUT3–	18	O	Channel 3 inverting amplifier output. When light is incident on the photodiode the output pin transitions in a negative direction from the no light condition.
OUT3+	17	O	Channel 3 noninverting amplifier output. When light is incident on the photodiode the output pin transitions in a positive direction from the no light condition.
OUT4–	16	O	Channel 4 inverting amplifier output. When light is incident on the photodiode the output pin transitions in a negative direction from the no light condition.
OUT4+	15	O	Channel 4 noninverting amplifier output. When light is incident on the photodiode the output pin transitions in a positive direction from the no light condition.
VDD1	2, 4, 5, 7	I	Positive power supply for the transimpedance amplifier stage. Each pin should be tied to the same power supply with independent power-supply bypassing.
VDD2	14, 23	I	Positive power supply for the differential amplifier stage. Tie VDD1 and VDD2 to the same power supply with independent power-supply bypassing.
VOCM	27	I	Differential amplifier common-mode output control.
VOD	10	I	Differential amplifier differential output offset control.
Thermal pad		—	Connect the thermal pad to the same potential as pin 11 and 26 (GND).

- (1) TI recommends driving a digital pin with a low-impedance source rather than leaving the pin floating because fast-moving transients can couple into the pin and inadvertently change the logic level.
- (2) I = input, O = output

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>DD1</sub> , V <sub>DD2</sub>	Total supply voltage, (V <sub>DD</sub> ) <sup>(2)</sup>		3.65	V
	Voltage at Output pins	0	V <sub>DD</sub>	V
	Voltage at Logic pins	–0.2	V <sub>DD</sub>	V
I <sub>IN</sub>	Continuous current into IN		25	mA
I <sub>OUT</sub>	Continuous output current		35	mA
T <sub>J</sub>	Junction temperature		150	°C
T <sub>A</sub>	Operating free-air temperature	–40	125	°C
T <sub>stg</sub>	Storage temperature	–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) VDD1 and VDD2 should always be tied to the same supply and have separate power-supply bypass capacitors.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±1500	V
		Charged device model (CDM), per AEC Q100-011	±1000	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>DD</sub>	Total supply voltage	3	3.3	3.45	V
T <sub>A</sub>	Operating free-air temperature	–40		125	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		LMH32404-Q1	UNIT
		RHF (VQFN)	
		28 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	39.7	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	31.5	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	17.8	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.8	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	17.8	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	6.0	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

$V_{DD} = 3.3\text{ V}$ ,  $V_{OCM} = \text{Open}$ ,  $V_{OD} = 0\text{ V}$ ,  $C_{PD}^{(1)} = 1\text{ pF}$ ,  $\overline{EN} = 0\text{ V}$ ,  $\overline{IDC\_EN} = 3.3\text{ V}$ ,  $R_L = 100\text{ }\Omega$  (differential load between OUT+ and OUT-), and  $T_A = 25^\circ\text{C}$ . (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal bandwidth	V <sub>OUT</sub> = 100 mV <sub>PP</sub>		350		MHz
LSBW	Large-signal bandwidth	V <sub>OUT</sub> = 1 V <sub>PP</sub>		300		MHz
t <sub>R</sub> , t <sub>F</sub>	Rise and fall time	V <sub>OUT</sub> = 100 mV <sub>PP</sub> , Pulse width = 10 ns		1.25		ns
	Slew Rate <sup>(4)</sup>	V <sub>OUT</sub> = 1 V <sub>PP</sub> , Pulse width = 10 ns		750		V/μs
	Overload recovery time (1% settling)	I <sub>IN</sub> = 100 mA, Pulse width = 10 ns		12		ns
	Overload pulse width extension <sup>(5)</sup>	I <sub>IN</sub> = 100 mA, Pulse width = 10 ns		5		ns
i <sub>IN</sub>	Integrated input current noise	f = 250 MHz		56		nA <sub>RMS</sub>
	Adjacent channel crosstalk	f = 100 MHz		-49		dBc
	Non adjacent channel crosstalk	f = 100 MHz		-58		dBc
	All hostile channels crosstalk	f = 100 MHz		-39		dBc
DC PERFORMANCE						
Z <sub>21</sub>	Small-signal transimpedance gain <sup>(6)</sup>		17	20	23	kΩ
	Channel-to-channel gain matching			±0.1		%
V <sub>OD</sub>	Differential output offset voltage (V <sub>OUT-</sub> – V <sub>OUT+</sub> )		–20	±5	20	mV
	Differential output offset voltage drift, ΔV <sub>OD</sub> /ΔT <sub>A</sub>			±20		μV/°C
INPUT PERFORMANCE						
V <sub>IN</sub>	Default input bias voltage	Input pin floating	2.42	2.47	2.52	V
	Default input bias voltage drift, ΔV <sub>IN</sub> /ΔT <sub>A</sub>	Input pin floating		1.1		mV/°C
I <sub>IN</sub>	DC Input current range	Z <sub>21</sub> < 3-dB degradation from I <sub>IN</sub> = 5 μA	60	72		μA
OUTPUT PERFORMANCE						
V <sub>OH</sub>	Single-sided output voltage swing (high) <sup>(2)</sup>		2.85	2.9		V
V <sub>OL</sub>	Single-sided output voltage swing (low) <sup>(2)</sup>			0.36	0.39	V
I <sub>OUT</sub>	Linear output drive (sink and source)	T <sub>A</sub> = 25°C, I <sub>IN</sub> = 50 μA, R <sub>L</sub> = 25 Ω	24	26.6	32	mA
		T <sub>A</sub> = –40°C, I <sub>IN</sub> = 50 μA, R <sub>L</sub> = 25 Ω		27.1		
		T <sub>A</sub> = 125°C, I <sub>IN</sub> = 50 μA, R <sub>L</sub> = 25 Ω		25.1		
I <sub>SC</sub>	Output short-circuit current (differential) <sup>(3)</sup>			70		mA
Z <sub>OUT</sub>	DC differential output impedance	M <sub>X</sub> = high	18	21	24	Ω
		M <sub>X</sub> = low		1		MΩ
OUTPUT COMMON-MODE CONTROL (V <sub>OCM</sub> ) PERFORMANCE						
SSBW	Small-signal bandwidth	V <sub>OCM</sub> = 100 mV <sub>PP</sub> at V <sub>OCM</sub> pin		375		MHz
LSBW	Large-signal bandwidth	V <sub>OCM</sub> = 1 V <sub>PP</sub> at V <sub>OCM</sub> pin		120		MHz
e <sub>N</sub>	Output common-mode noise	f = 10 MHz, 1 nF capacitor to GND on V <sub>OCM</sub> pin		15		nV/√Hz
A <sub>V</sub>	Gain, (ΔV <sub>OCM</sub> /ΔV <sub>OCM</sub> )	I <sub>N</sub> floating, V <sub>OCM</sub> = 1.1 V (driven)		1		V/V
	Gain Error	T <sub>A</sub> = 25°C, V <sub>OCM</sub> = 0.7 V to 2.3 V	–2%	0.5%	2%	
		T <sub>A</sub> = –40°C to 125°C, V <sub>OCM</sub> = 0.7 V to 2.3 V		±1%		
	Input impedance			17		kΩ
V <sub>OCM</sub>	V <sub>OCM</sub> pin default offset from 1.1 V	V <sub>OCM</sub> floating, (V <sub>OCM</sub> - 1.1 V)	–25	8	45	mV
	V <sub>OCM</sub> error vs Input current, ΔV <sub>OCM</sub> /ΔI <sub>IN</sub>	V <sub>OCM</sub> driven to 1.1 V		10		V/A
V <sub>OCM</sub>	Output common-mode voltage, (V <sub>OUT+</sub> + V <sub>OUT-</sub> )/2	T <sub>A</sub> = 25°C, V <sub>OCM</sub> floating	1	1.1	1.2	V

## 6.5 Electrical Characteristics (continued)

$V_{DD} = 3.3\text{ V}$ ,  $V_{OCM} = \text{Open}$ ,  $V_{OD} = 0\text{ V}$ ,  $C_{PD}^{(1)} = 1\text{ pF}$ ,  $\overline{EN} = 0\text{ V}$ ,  $\overline{IDC\_EN} = 3.3\text{ V}$ ,  $R_L = 100\ \Omega$  (differential load between OUT+ and OUT-), and  $T_A = 25^\circ\text{C}$ . (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Output common-mode voltage drift, $(\Delta V_{OCM}/\Delta T_A)$	$T_A = -40^{\circ}\text{C}$ to $125^{\circ}\text{C}$ , $V_{OCM}$ floating		300		$\mu\text{V}/^{\circ}\text{C}$
$V_{OCM}$	Output common-mode voltage, $(V_{OUT+} + V_{OUT-})/2$	$T_A = 25^{\circ}\text{C}$ , $V_{OCM}$ driven to 1.1V	1.05	1.1	1.15	V
	Output common-mode voltage drift, $(\Delta V_{OCM}/\Delta T_A)$	$T_A = -40^{\circ}\text{C}$ to $125^{\circ}\text{C}$ , $V_{OCM}$ driven to 1.1V		-10		$\mu\text{V}/^{\circ}\text{C}$
	VOCM headroom to positive supply voltage	$T_A = 25^{\circ}\text{C}$ , $V_{OCM}$ offset shift from $V_{OCM} = 1.1\text{ V}$ (driven) < 10-mV		1.2	1.3	V
		$T_A = -40^{\circ}\text{C}$ to $125^{\circ}\text{C}$ , $V_{OCM}$ offset shift from $V_{OCM} = 1.1\text{ V}$ (driven) < 10-mV		1		V
	VOCM headroom to negative supply voltage	$T_A = 25^{\circ}\text{C}$ , $V_{OCM}$ offset shift from $V_{OCM} = 1.1\text{ V}$ (driven) < 10-mV		0.2	0.65	V
		$T_A = -40^{\circ}\text{C}$ to $125^{\circ}\text{C}$ , $V_{OCM}$ offset shift from $V_{OCM} = 1.1\text{ V}$ (driven) < 10-mV		0.25		V
OUTPUT DIFFERENTIAL OFFSET ( $V_{OD}$ ) PERFORMANCE						
SSBW	Small-signal bandwidth	$V_{OD} = 100\text{ mV}_{PP}$		45		MHz
LSBW	Large-signal bandwidth	$V_{OD} = 1\text{ V}_{PP}$		17		MHz
$V_{OD}$	Default VOD pin voltage			0.5		V
$V_{OS\_D}$	Differential output offset, $V_{OUT} = (V_{OUT-} - V_{OUT+})$	IN floating, $V_{OD} = 0.5\text{ V}$	470	500	530	mV
	Differential output offset drift, $\Delta V_{OS\_D}/\Delta T_A$	IN floating, $V_{OD} = 0.5\text{ V}$		0.03		mV/ $^{\circ}\text{C}$
$V_{OS\_D}$	Differential output offset, $V_{OUT} = (V_{OUT-} - V_{OUT+})$	IN floating, $V_{OD}$ floating	470	500	530	mV
	Differential output offset drift, $\Delta V_{OS\_D}/\Delta T_A$	IN floating, $V_{OD}$ floating		0.05		mV/ $^{\circ}\text{C}$
$A_V$	Gain, $(\Delta V_{OUT}/\Delta V_{OD})$ , where $V_{OUT} = (V_{OUT-} - V_{OUT+})$	IN floating, $V_{OCM} = 1.1\text{ V}$ (driven)		-1.01		V/V
	Gain Error	$T_A = 25^{\circ}\text{C}$ , $V_{OD} = 0.3\text{ V}$ to $1.2\text{ V}$	-5%	$\pm 0.8\%$	5%	
		$T_A = -40^{\circ}\text{C}$ to $125^{\circ}\text{C}$ , $V_{OD} = 0.3\text{ V}$ to $1.2\text{ V}$		$\pm 1.5\%$		
	Input impedance			2.5		k $\Omega$
AMBIENT LIGHT CANCELLATION PERFORMANCE ( $\overline{IDC\_EN} = 0\text{ V}$ ) <sup>(7)</sup>						
	Settling time, 1% (2 mV) of settled $V_{OS}$	$I_{IN} = 0\text{ }\mu\text{A} \rightarrow 10\text{ }\mu\text{A}$		20		$\mu\text{s}$
		$I_{IN} = 10\text{ }\mu\text{A} \rightarrow 0\text{ }\mu\text{A}$		60		
	Ambient light current cancellation range	Differential output offset ( $V_{OUT-} - V_{OUT+}$ ) shift from $I_{DC} = 10\text{ }\mu\text{A}$ < 10 mV	1.8	2.5		mA
POWER SUPPLY						
$I_Q$	Quiescent current, per channel, $(V_{DD1} + V_{DD2})$	$M_X = 3.3\text{ V}$ , $T_A = 25^{\circ}\text{C}$	22.8	27.7	32.5	mA
		$M_X = 0\text{ V}$ , $T_A = 25^{\circ}\text{C}$	8.5	10.4	13.4	
PSRR+	Positive power-supply rejection ratio	$V_{DD1} = V_{DD2}$	54	74		dB
SHUTDOWN						
$I_Q$	Total disabled quiescent current ( $\overline{EN} = V_{DD}$ )	$T_A = 25^{\circ}\text{C}$		2.35	3	mA
		$T_A = -40^{\circ}\text{C}$		2.25		
		$T_A = 125^{\circ}\text{C}$		2.55		

- (1) Input capacitance of photodiode.
- (2) Output slammed to the rail and  $V_{OCM}$  adjusted to achieve output swing.
- (3) Device cannot withstand continuous short-circuit between the differential outputs.
- (4) Average of rising and falling slew rate.
- (5) Pulse width extension measured at 50% of pulse height of a square wave.
- (6) Gain measured at the amplifier output pins when driving a 100- $\Omega$  resistive load. At higher resistor loads the gain will increase.

- (7) Enabling the ambient light cancellation loop will add noise to the system.



## 6.6 Electrical Characteristics: Logic Threshold and Switching Characteristics

$V_{DD} = 3.3\text{ V}$ ,  $V_{OCM} = \text{Open}$ ,  $V_{OD} = 0\text{ V}$ ,  $C_{PD}^{(1)} = 1\text{ pF}$ ,  $\overline{EN} = 0\text{ V}$ ,  $\overline{IDC\_EN} = 3.3\text{ V}$ ,  $R_L = 100\ \Omega$  (differential load between OUT+ and OUT-), and  $T_A = 25^\circ\text{C}$ . (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>LOGIC THRESHOLD PERFORMANCE</b>						
	Logic pin bias current			75	120	$\mu\text{A}$
	$\overline{EN}$ , $\overline{IDC\_EN}$ , disable threshold voltage	Disabled above this voltage		1.5	2	V
	$\overline{EN}$ , $\overline{IDC\_EN}$ , enable threshold voltage	Enabled below this voltage	0.8	1		V
	$M_X$ control, enable threshold voltage	Switch closed above this voltage		1.5	2	V
	$M_X$ control, disable threshold voltage	Switch open below this voltage	0.8	1.0		V
<b>EN CONTROL TRANSIENT PERFORMANCE</b>						
	Enable transition-time (1% settling)	Ambient loop disabled, $f_{IN} = 25\text{ MHz}$ , $V_{OUT} = 1\text{ V}_{PP}$ , $I_{DC} = 0\ \mu\text{A}$		250		ns
	Disable transition-time (1% settling)	Ambient loop disabled, $f_{IN} = 25\text{ MHz}$ , $V_{OUT} = 1\text{ V}_{PP}$ , $I_{DC} = 0\ \mu\text{A}$		8		ns
	Enable transition-time (1% settling)	Ambient loop enabled, $f_{IN} = 25\text{ MHz}$ , $V_{OUT} = 1\text{ V}_{PP}$ , $I_{DC} = 100\ \mu\text{A}$		4		$\mu\text{s}$
	Disable transition-time (1% settling)	Ambient loop enabled, $f_{IN} = 25\text{ MHz}$ , $V_{OUT} = 1\text{ V}_{PP}$ , $I_{DC} = 100\ \mu\text{A}$		3		ns
<b>MULTIPLEXER CONTROL TRANSIENT PERFORMANCE</b>						
	Channel to Channel transition-time (1% settling)	Ambient loop disabled, $0 \rightarrow 0.5\text{V}$ transition at $V_{OUT}$ .		10		ns
	Disable transition-time (1% settling)	Ambient loop disabled, $f_{IN} = 25\text{ MHz}$ , $V_{OUT} = 1\text{ V}_{PP}$ , $I_{DC} = 0\ \mu\text{A}$		8		ns

(1) Input capacitance of photodiode.

## 6.7 Typical Characteristics

At  $V_{DD} = 3.3\text{ V}$ ,  $V_{OCM} = \text{open}$ ,  $V_{OD} = 0\text{ V}$ ,  $C_{PD} = 1\text{ pF}$ ,  $\overline{\text{EN}} = 0\text{ V}$  (enabled),  $\overline{\text{IDC\_EN}} = 3.3\text{ V}$  (disabled),  $R_L = 100\ \Omega$  (differential load between  $\text{OUT+}$  and  $\text{OUT-}$ ), and  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

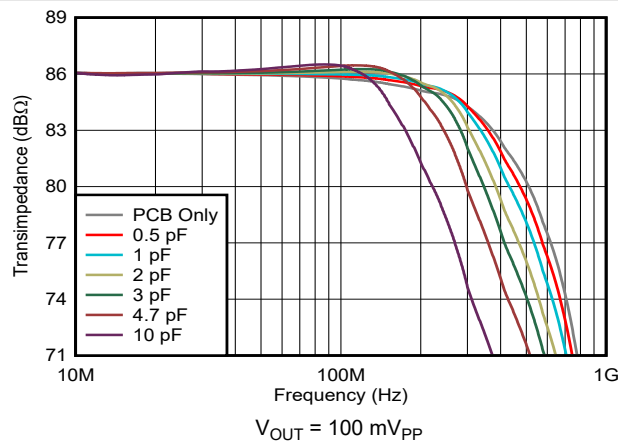


Figure 6-1. Small Signal Response vs Input Capacitance

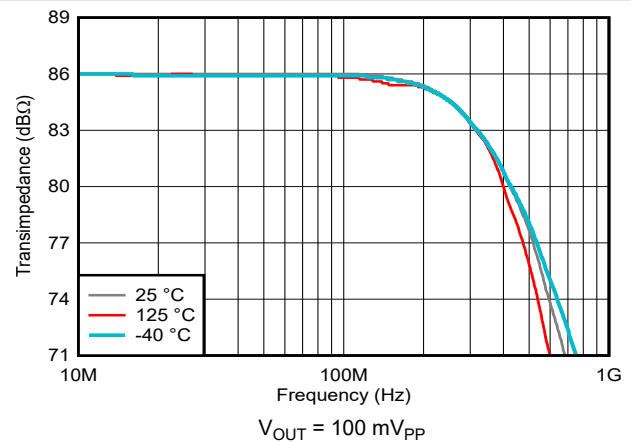


Figure 6-2. Small Signal Response vs Ambient Temperature

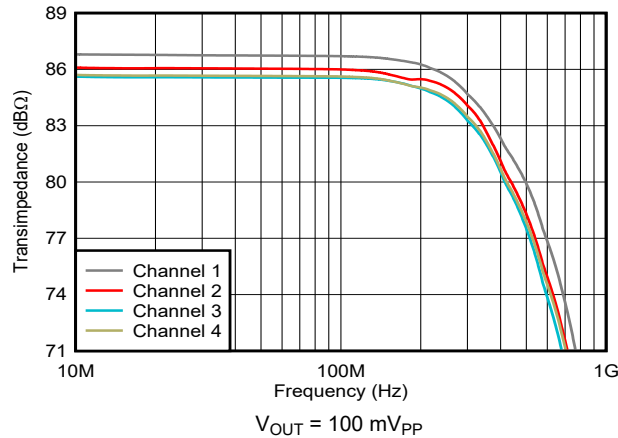


Figure 6-3. Small Signal Response vs Channels

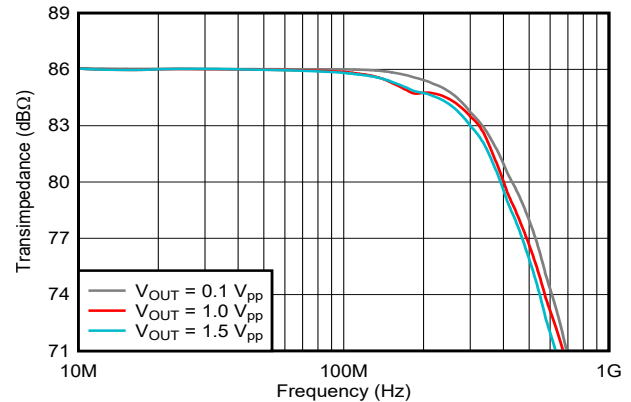


Figure 6-4. Frequency Response vs Output Swing

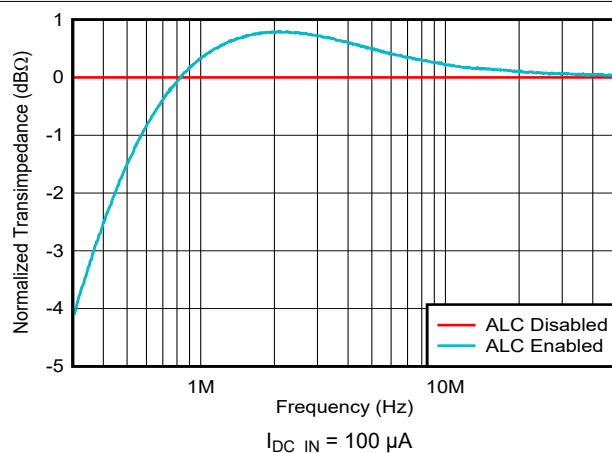


Figure 6-5. Low-Side Frequency Response vs Ambient Light Cancellation

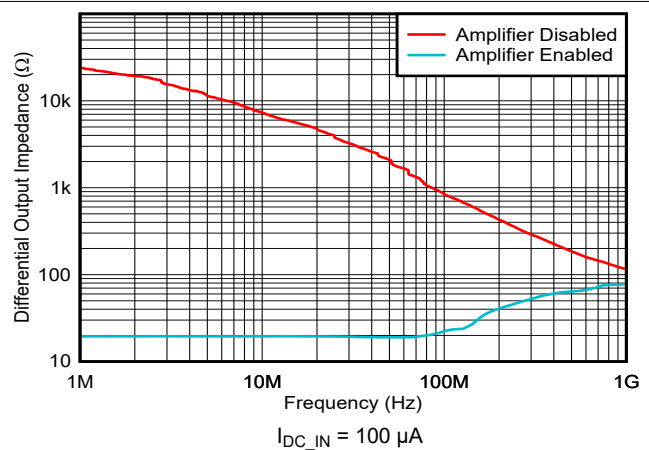
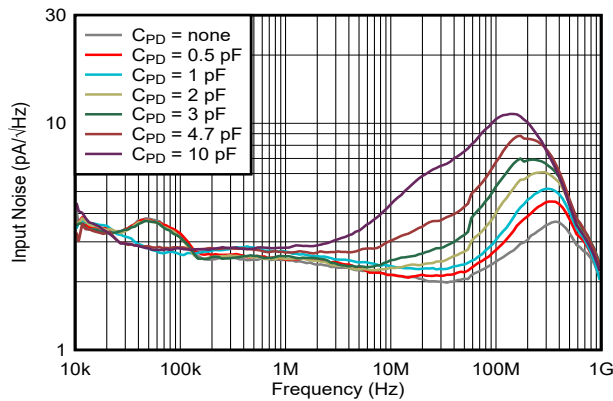


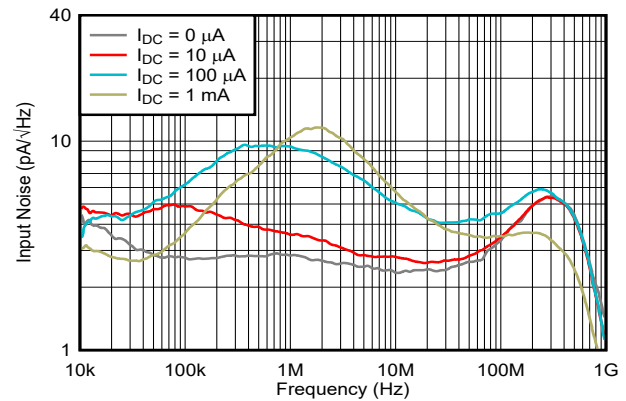
Figure 6-6. Closed-Loop Output Impedance vs Frequency

## 6.7 Typical Characteristics (continued)

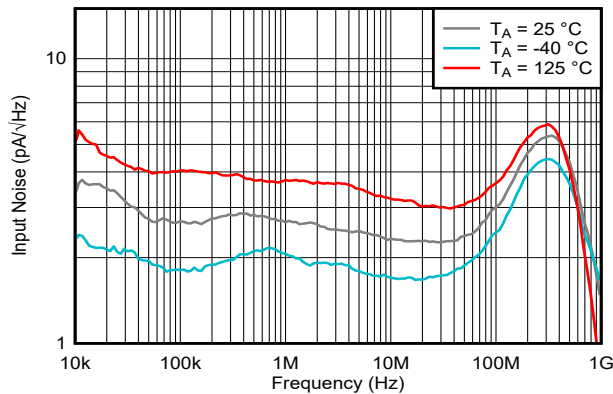
At  $V_{DD} = 3.3\text{ V}$ ,  $V_{OCM} = \text{open}$ ,  $V_{OD} = 0\text{ V}$ ,  $C_{PD} = 1\text{ pF}$ ,  $\overline{EN} = 0\text{ V}$  (enabled),  $\overline{IDC\_EN} = 3.3\text{ V}$  (disabled),  $R_L = 100\ \Omega$  (differential load between  $OUT+$  and  $OUT-$ ), and  $T_A = 25^\circ\text{C}$  (unless otherwise noted)



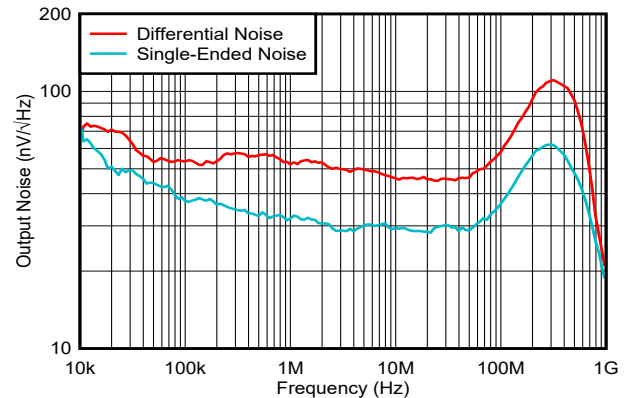
**Figure 6-7. Input Noise Density vs Input Capacitance**



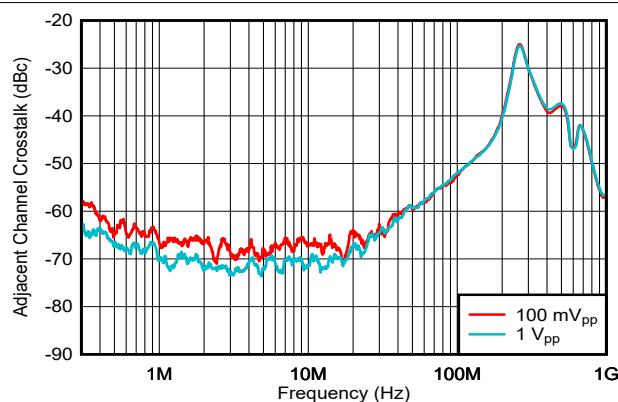
**Figure 6-8. Input Noise Density vs Ambient Light DC Current**



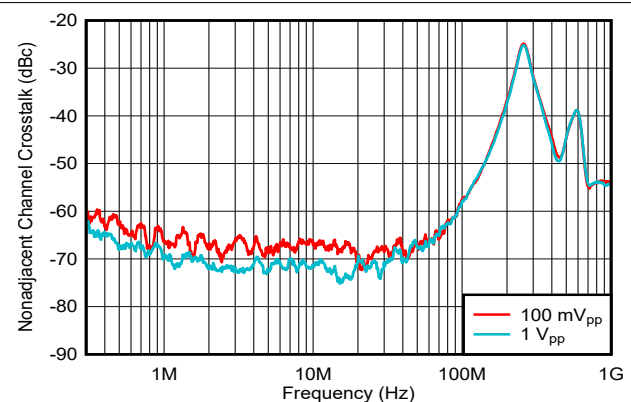
**Figure 6-9. Input Noise Density vs Ambient Temperature**



**Figure 6-10. Output Noise Density vs Output Configuration**



**Figure 6-11. Adjacent Channel Crosstalk**



**Figure 6-12. Non-Adjacent Channel Crosstalk**

## 6.7 Typical Characteristics (continued)

At  $V_{DD} = 3.3\text{ V}$ ,  $V_{OCM} = \text{open}$ ,  $V_{OD} = 0\text{ V}$ ,  $C_{PD} = 1\text{ pF}$ ,  $\overline{\text{EN}} = 0\text{ V}$  (enabled),  $\overline{\text{IDC\_EN}} = 3.3\text{ V}$  (disabled),  $R_L = 100\ \Omega$  (differential load between  $\text{OUT+}$  and  $\text{OUT-}$ ), and  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

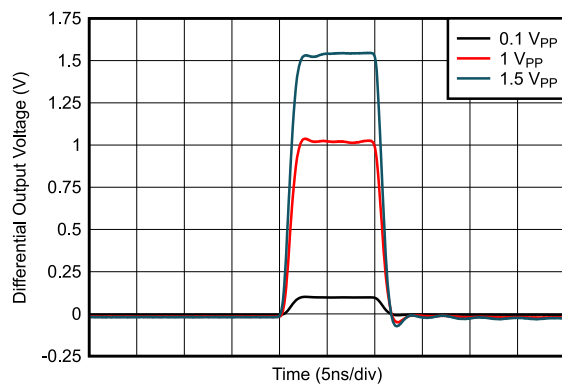


Figure 6-13. Pulse Response vs Output Swing

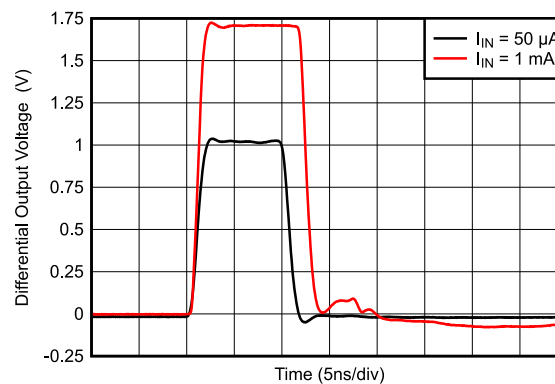


Figure 6-14. Overloaded Pulse Response

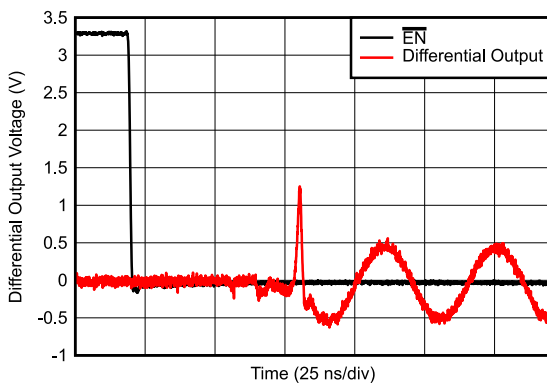


Figure 6-15. Turn-On Time

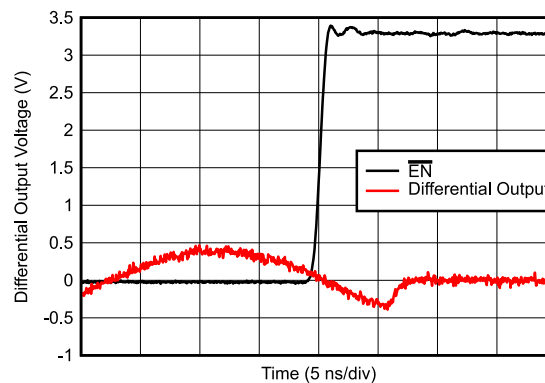
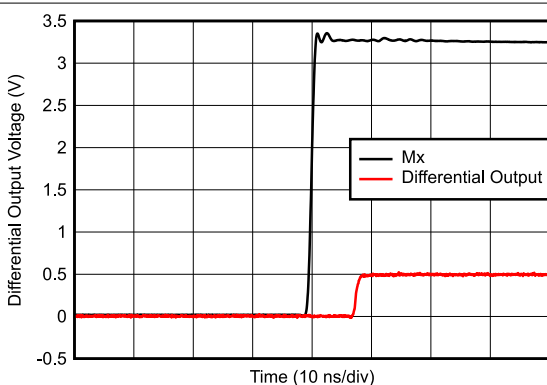


Figure 6-16. Turn-Off Time



0 → 0.5V transition at  $V_{OUT}$  (1% settling)

Figure 6-17. Channel Turn-On Response

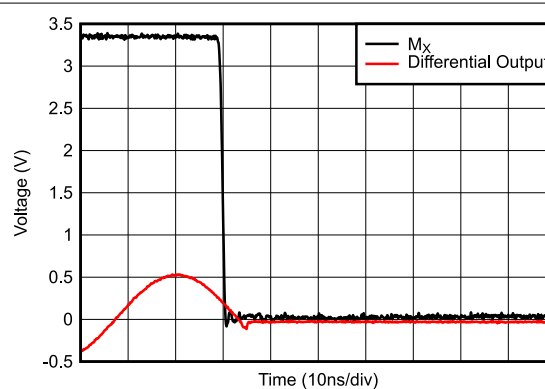
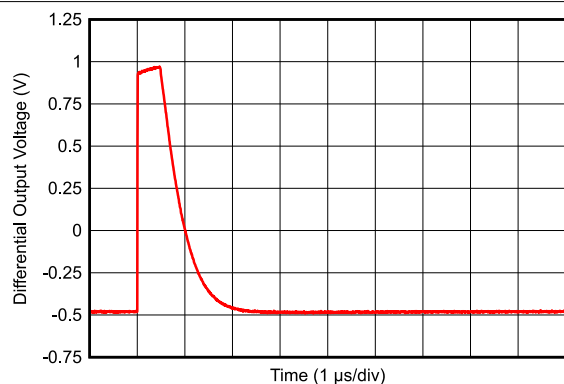


Figure 6-18. Channel Turn-Off Response

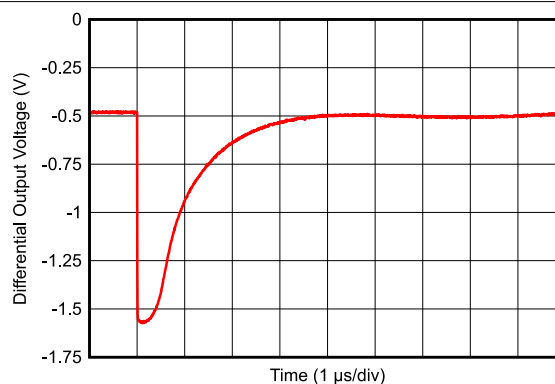
## 6.7 Typical Characteristics (continued)

At  $V_{DD} = 3.3\text{ V}$ ,  $V_{OCM} = \text{open}$ ,  $V_{OD} = 0\text{ V}$ ,  $C_{PD} = 1\text{ pF}$ ,  $\overline{\text{EN}} = 0\text{ V}$  (enabled),  $\overline{\text{IDC\_EN}} = 3.3\text{ V}$  (disabled),  $R_L = 100\ \Omega$  (differential load between  $\text{OUT+}$  and  $\text{OUT-}$ ), and  $T_A = 25^\circ\text{C}$  (unless otherwise noted)



$I_{DC\_IN} = 0\ \mu\text{A} \rightarrow 100\ \mu\text{A}$ ,  $V_{OD} = 0.5\text{ V}$

Figure 6-19. Ambient Loop Cancellation Settling Time <sup>(1)</sup>



$I_{DC\_IN} = 100\ \mu\text{A} \rightarrow 0\ \mu\text{A}$ ,  $V_{OD} = 0.5\text{ V}$

Figure 6-20. Ambient Loop Cancellation Settling Time <sup>(1)</sup>

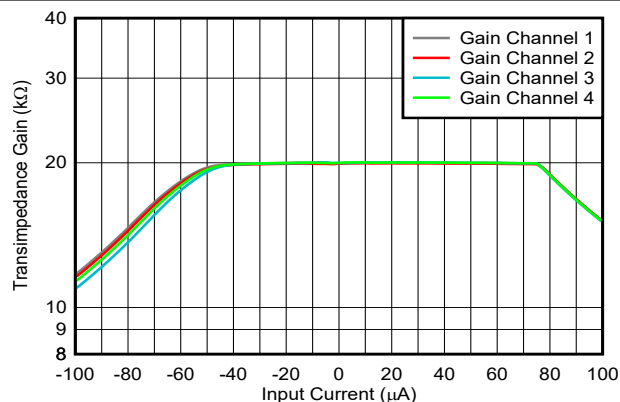


Figure 6-21. Transimpedance Gain vs Input Current

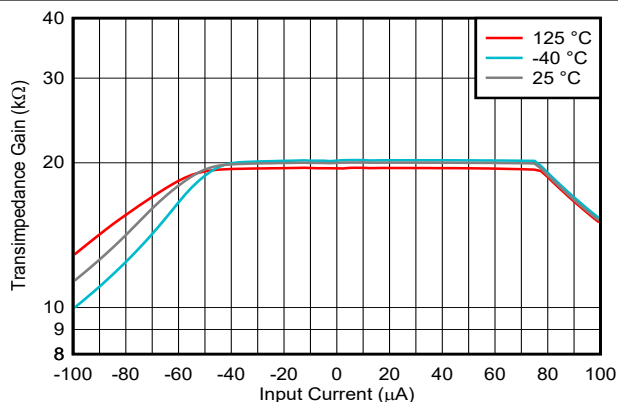


Figure 6-22. Transimpedance Gain vs Ambient Temperature

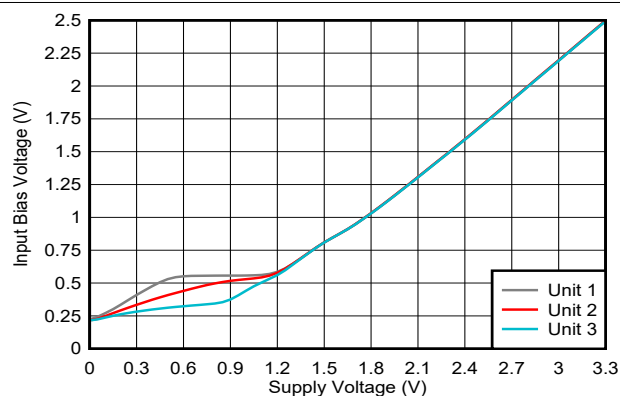


Figure 6-23. Input Bias Voltage vs Supply Voltage <sup>(2)</sup>

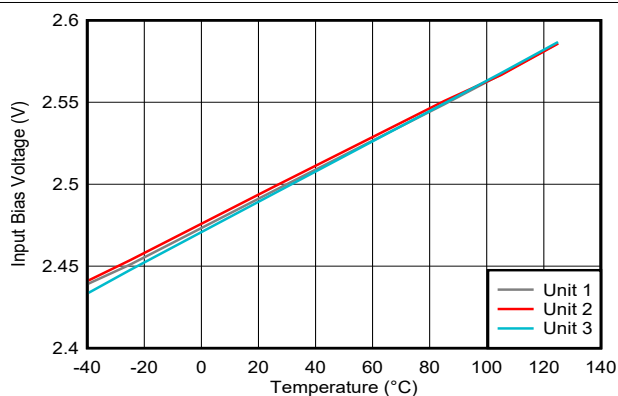


Figure 6-24. Input Bias Voltage vs Ambient Temperature <sup>(2)</sup>

<sup>1</sup> Differential Output Voltage = ( $V_{out+}$  -  $V_{out-}$ ).

<sup>2</sup> Typical units from different lots.

## 6.7 Typical Characteristics (continued)

At  $V_{DD} = 3.3\text{ V}$ ,  $V_{OCM} = \text{open}$ ,  $V_{OD} = 0\text{ V}$ ,  $C_{PD} = 1\text{ pF}$ ,  $\overline{\text{EN}} = 0\text{ V}$  (enabled),  $\overline{\text{IDC\_EN}} = 3.3\text{ V}$  (disabled),  $R_L = 100\ \Omega$  (differential load between  $\text{OUT+}$  and  $\text{OUT-}$ ), and  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

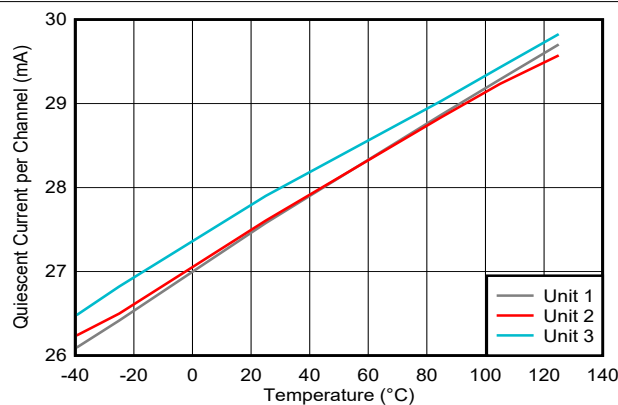


Figure 6-25. Quiescent Current (Per Channel) vs Ambient Temperature <sup>(2)</sup>

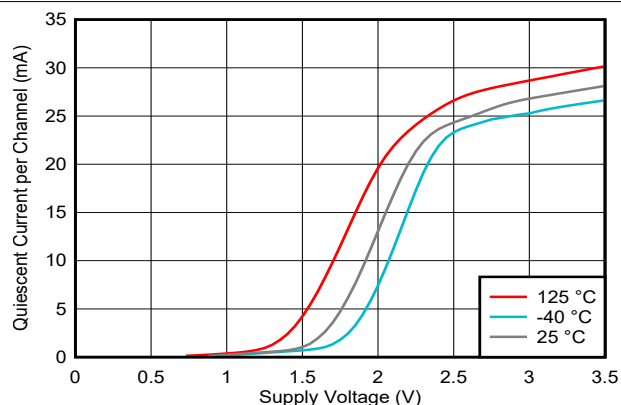


Figure 6-26. Quiescent Current (Per Channel) vs Supply Voltage

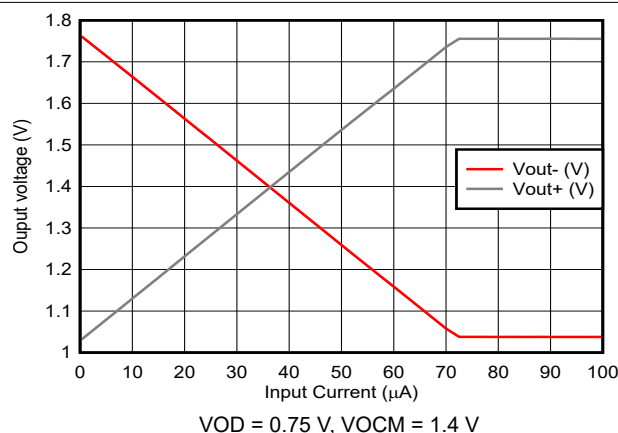


Figure 6-27. High-Side Swing vs Input Current

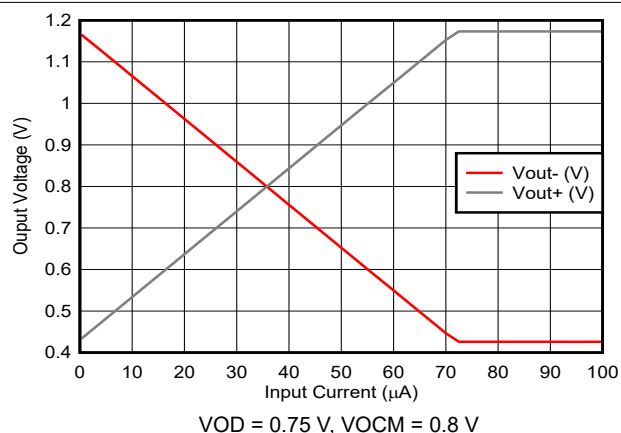


Figure 6-28. Low-Side Swing vs Input Current

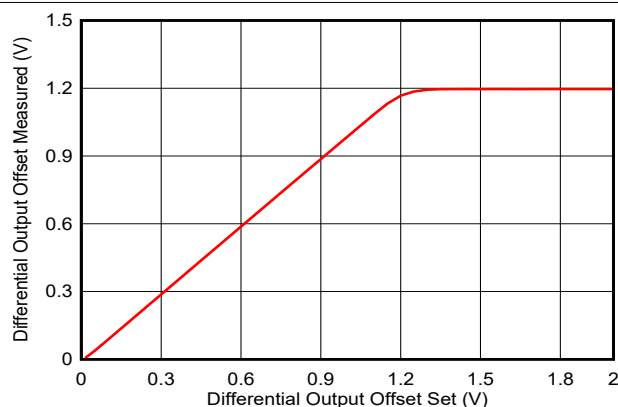


Figure 6-29. Differential Output Offset Gain

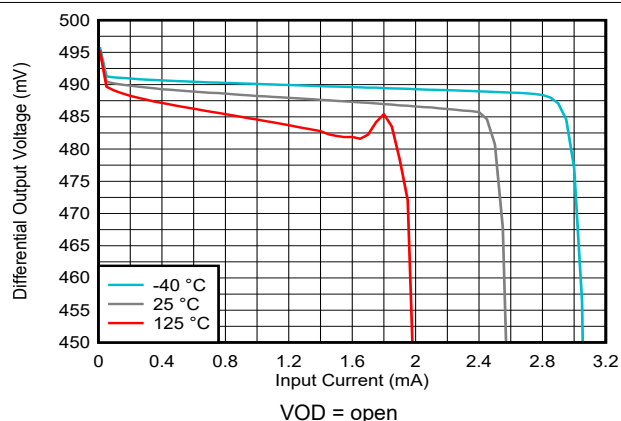
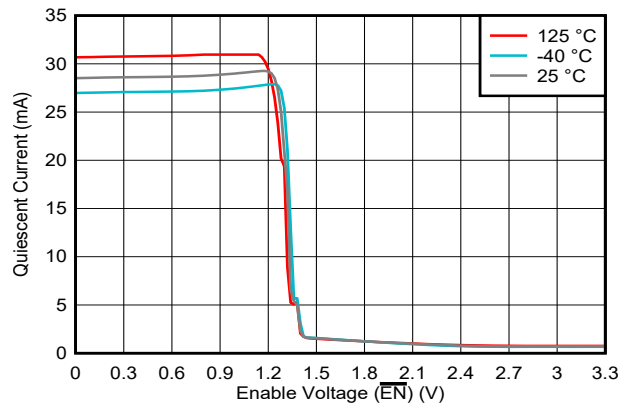


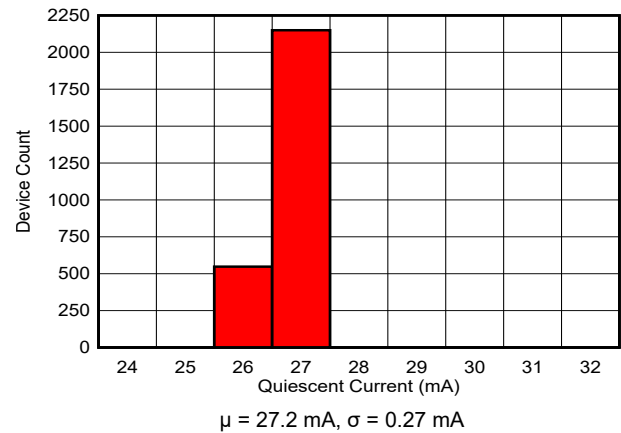
Figure 6-30. Ambient Light Cancellation Range vs Ambient Temperature

## 6.7 Typical Characteristics (continued)

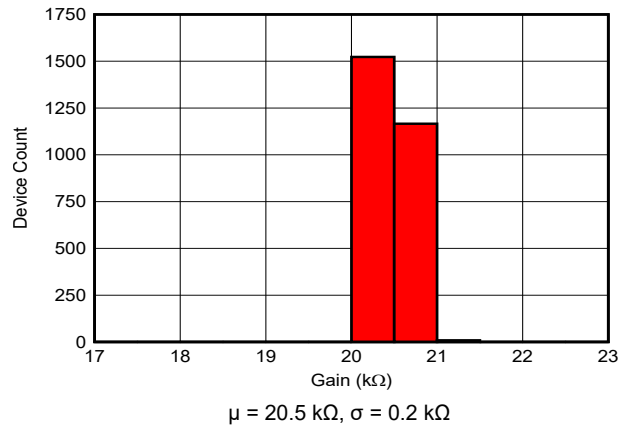
At  $V_{DD} = 3.3\text{ V}$ ,  $V_{OCM} = \text{open}$ ,  $V_{OD} = 0\text{ V}$ ,  $C_{PD} = 1\text{ pF}$ ,  $\overline{\text{EN}} = 0\text{ V}$  (enabled),  $\overline{\text{IDC\_EN}} = 3.3\text{ V}$  (disabled),  $R_L = 100\ \Omega$  (differential load between  $\text{OUT+}$  and  $\text{OUT-}$ ), and  $T_A = 25^\circ\text{C}$  (unless otherwise noted)



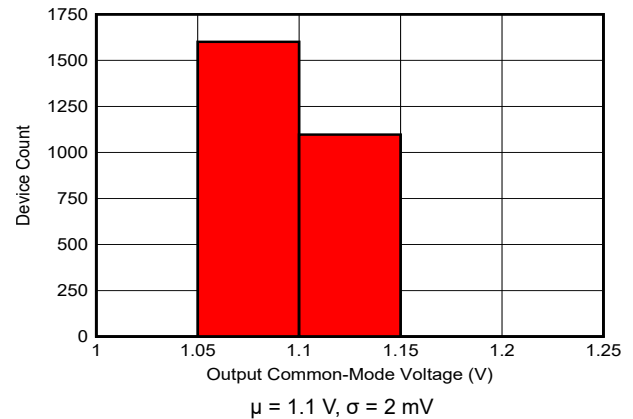
**Figure 6-31. Logic Threshold vs Ambient Temperature**



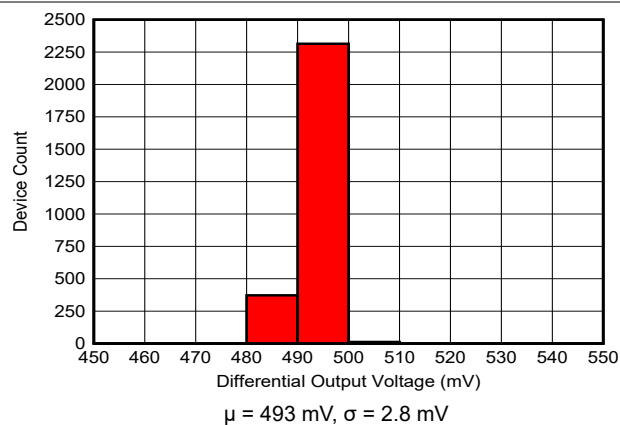
**Figure 6-32. Quiescent Current Distribution**



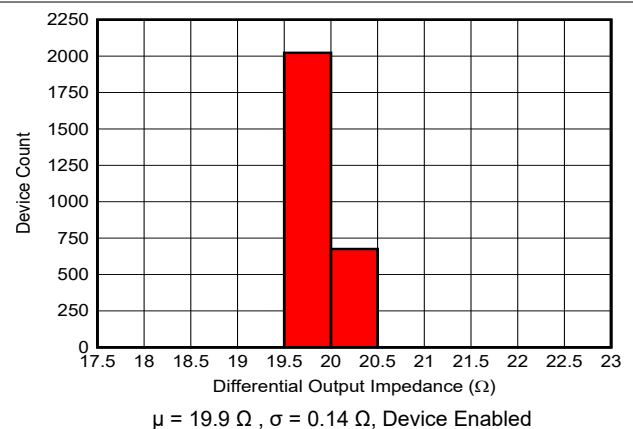
**Figure 6-33. Transimpedance Gain Distribution**



**Figure 6-34. Output Common-Mode Voltage ( $V_{OCM}$ ) Distribution**



**Figure 6-35. Differential Output Offset Voltage ( $V_{OD}$ ) Distribution**



**Figure 6-36. Differential Output Impedance ( $Z_{OUT}$ ) Distribution**

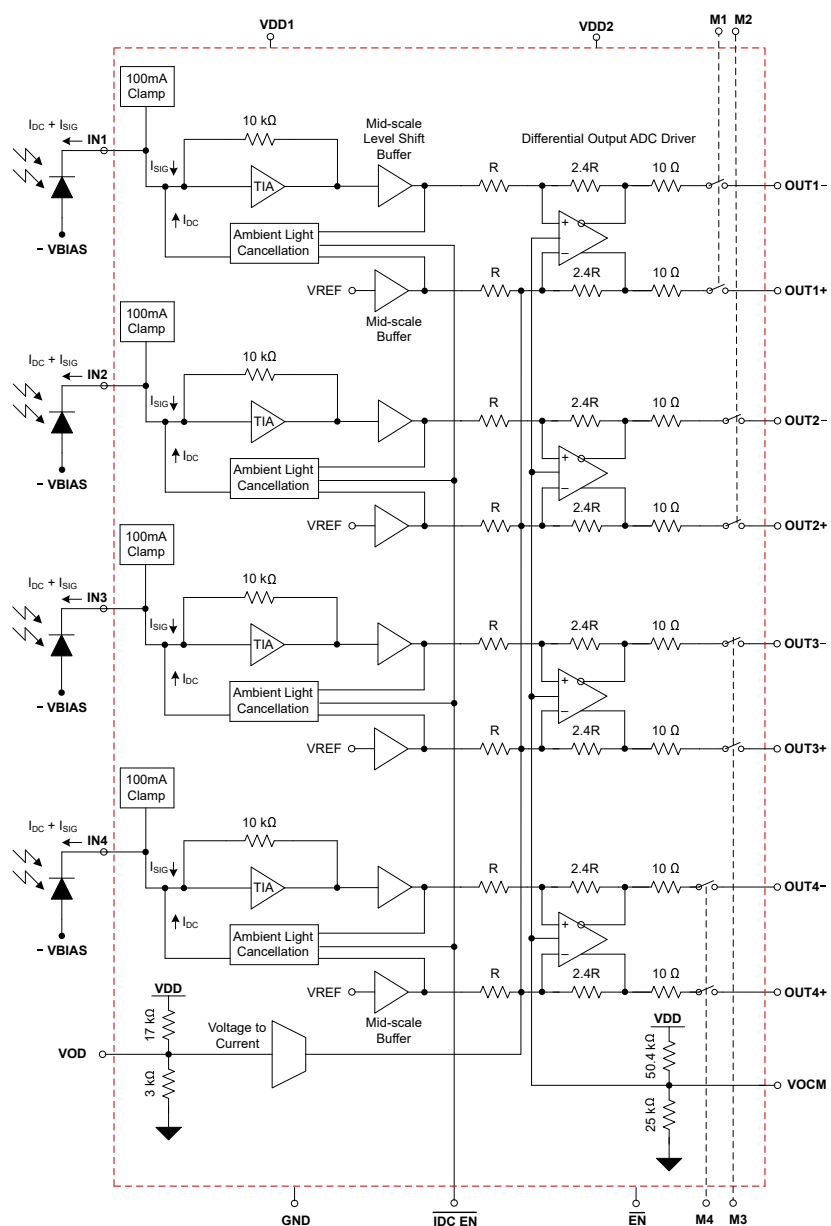
## 7 Detailed Description

### 7.1 Overview

The LMH32404-Q1 is a quad-channel, differential output, high-speed transimpedance amplifier (TIA) geared towards light detection and ranging (LIDAR) and laser distance measurement systems. Each LMH32404-Q1 channel has integrated switches on the output to disconnect the differential output amplifier from the output pins. This enables the LMH32404-Q1 to be highly configurable in a multi-channel LIDAR system. The LMH32404-Q1 device is designed to work with photodiodes (PDs), for example avalanche photodiodes (APDs), connected in configurations that can source or sink the current. When the photodiode sinks the photocurrent (anode is biased to a negative voltage and cathode is tied to the amplifier input) the fast recovery clamp activates when the amplifier input is overloaded. When the photodiode sources the photocurrent (cathode is biased to a positive voltage and anode is tied to the amplifier input) a soft clamp activates when the amplifier input is overloaded. When the soft clamp activates the amplifier takes longer to recover. The recovery time depends on the level of input overload. The LMH32404-Q1 is offered in a space-saving 5-mm × 4-mm, 28-pin VQFN package and is rated over a temperature range from –40°C to +125°C.



## 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Clamping and Input Protection

The LMH32404-Q1 device is optimized to work with photodiodes (PD) configurations that can source or sink current; however, the LMH32404-Q1 is optimized for a sinking current configuration. It is assumed that the LMH32404-Q1 device is being used with a PD that is configured with its cathode tied to the amplifier input and the anode tied to a negative supply voltage, unless stated otherwise.

The LMH32404-Q1 features two internal clamps, a fast recovery clamp and a soft clamp. The fast recovery clamp is the active clamp when the photodiode is sinking a photocurrent. The soft clamp is the active clamp when the photodiode is sourcing a photocurrent. Stray reflections from nearby objects with high reflectivity can produce large output current pulses from the PD. The linear input range of the LMH32404-Q1 is approximately 65  $\mu$ A. Input currents in excess of the linear current range will cause the internal nodes of the amplifier to saturate, which increases the amplifier recovery time. The end result broadens the output pulse, which leads to blind zones.

To protect against this condition, the LMH32404-Q1 features an integrated fast recovery clamp that absorbs and diverts the excess current to the positive supply ( $V_{DD1}$ ) when the amplifier detects its nodes entering a saturated condition. The integrated clamp minimizes the pulse extension to less than a few nanoseconds for input pulses up to 100 mA. The power-supply pins ( $V_{DD1}$  and  $V_{DD2}$ ) must have their own bypass capacitors to prevent large input pulses from affecting the differential output stage. The clamp circuitry is active when the amplifier is in standby mode and low-power mode, thereby protecting the TIA input.

### 7.3.2 ESD Protection

All LMH32404-Q1 IO pins (excluding  $V_{DD1}$ ,  $V_{DD2}$ , and GND) have an internal electrostatic discharge (ESD) protection diode to the positive and negative supply rails to protect the amplifier from ESD events.

### 7.3.3 Differential Output Stage

Each channel of the LMH32404-Q1 has a differential output stage that performs two functions that are common across all differential amplifiers. This stage does the following:

1. Converts the single-ended output from the TIA stage to a differential output.
2. Performs a common-mode output shift to match the specified ADC input common-mode voltage.

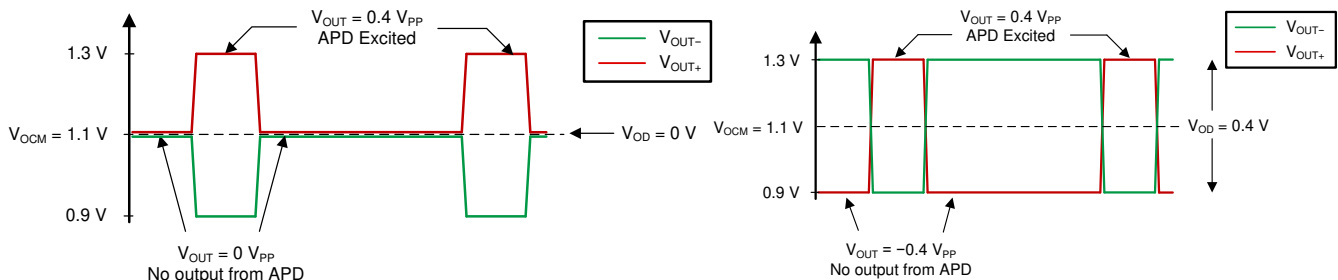
The VOD pin is functional only when the LMH32404-Q1 device is used with a PD that sinks the photocurrent. Set  $V_{OD} = 0$  V when the LMH32404-Q1 device is interfaced with a PD that sources the photocurrent. The differential output stage has two 10- $\Omega$  series resistors on its output to isolate the amplifier output stage transistors from the package bond-wire inductance and printed circuit board (PCB) capacitance. The net gain of the LMH32404-Q1 (TIA plus the output stage) is 20 k $\Omega$  per channel when driving an external 100- $\Omega$  resistor. When the external load resistor is increased above 100  $\Omega$ , the effective gain from the IN pin to the differential output pin increases. Consequently, when the external load resistor is decreased to less than 100  $\Omega$ , the effective gain from the IN pin to the differential output pin decreases as a result of the larger voltage drop across the two internal 10- $\Omega$  resistors. The effective TIA gain is 24 k $\Omega$  when there is no load resistor between the OUT+ and OUT– pins.

The output common-mode voltage of the LMH32404-Q1 can be set externally through the VOCM pin. A resistor divider internal to the amplifier, between  $V_{DD2}$  and ground sets the default voltage to 1.1 V. The internal resistors generate common-mode noise that is typically rejected by the CMRR of the subsequent ADC stage. To maximize the amplifier SNR, place an external noise bypass capacitor to ground on the VOCM pin. In single-ended signal chains, such as ToF systems that use time-to-digital converters (TDCs), only a single output per channel of the LMH32404-Q1 is needed. In such situations, terminate the unused differential output in the same manner as the used output to maintain balance and symmetry. The signal swing of the single-ended output is half the available differential output swing. Additionally, the common-mode noise of the output stage, which is typically rejected by the differential input ADC, is now added to the total noise, further degrading SNR.

The output stage of the LMH32404-Q1 has an additional VOD input that sets the differential output between OUT– and OUT+. Figure 7-1 shows how each output pin of the LMH32404-Q1 is at the voltage set by the VOD pin (default = 1.1 V) when the photodiode output current is zero and the VOD input is set to 0 V. When the VOD pin is driven to a voltage of X volts, the two output pins are separated by X volts when the photodiode current is zero. The average voltage is still equal to VOD. For example, Figure 7-2 shows how if VOD is set to 1.1 V and VOD is set to 0.4 V, then OUT– = 1.1 V + 0.2 V = 1.3 V and OUT+ = 1.1 V – 0.2 V = 0.9 V.

The VOD output offset feature is included in the LMH32404-Q1 because the output current of a photodiode is unipolar. Depending on the reverse bias configuration, a photodiode can either sink or source current, but cannot do both at the same time. With the anode connected to a negative bias and the cathode connected to the TIA stage input, the photodiode can only sink current, which implies that the TIA stage output swings in a positive direction above its default input bias voltage. Subsequently, OUT– only swings below VOD and OUT+ only swings above VOD. Figure 7-1 shows how the with VOD = 0 V, the LMH32404-Q1 only uses half its output swing range ( $V_{OUT} = V_{OUT+} - V_{OUT-}$ ), because one output never swings below VOD and the other output never goes above VOD. The signal dynamic range in this case is  $0.4 V_{PP} - 0 V = 0.4 V_{PP}$ .

Figure 7-2 shows how the VOD pin voltage allows OUT– to be level-shifted above VOD, and OUT+ to be level-shifted below VOD to maximize the output swing capabilities of the amplifier. The signal dynamic range in this case is  $0.4 V_{PP} - (-0.4 V_{PP}) = 0.8 V_{PP}$ .



**Figure 7-1. Single-Ended Outputs With VOD = 0 V** **Figure 7-2. Single-Ended Outputs With VOD = 0.4 V**

When the LMH32404-Q1 drives a 100-Ω load, the voltage set at the VOD pin is equal to the differential output offset ( $V_{OUT} = V_{OUT+} - V_{OUT-}$ ) when the input signal current is zero. Use Equation 1 to calculate the differential output offset under other load conditions.

$$V_{OD} = 1.2 \times VOD \times \frac{R_L}{(R_L + 20 \Omega)} \quad (1)$$

where

- VOD = Voltage applied at pin 10
- $V_{OD} = (V_{OUT-} - V_{OUT+})$
- $R_L$  = External load resistance

## 7.4 Device Functional Modes

### 7.4.1 Ambient Light Cancellation (ALC) Mode

The LMH32404-Q1 has an integrated DC cancellation loop that cancels and voltage offsets from incidental ambient light. The ALC mode only works when the PD is sinking the photocurrent. The DC cancellation loop is enabled by setting  $\overline{\text{IDC\_EN}}$  low. Incident ambient light on a photodiode produces a DC current resulting in an offset voltage at the output of the TIA stage.

If the photodiode produces a DC output current resulting from ambient light, the output of the level-shift buffer stage is offset from the reference voltage  $V_{\text{REF}}$ . The ALC loop detects this offset and produces an opposing DC current to compensate for the differential offset voltage at its input. The loop has a high-pass cutoff frequency of 400 kHz. The ambient light cancellation loop is disabled when the amplifier is placed in low-power mode.

The shot noise current introduced by the DC cancellation loop increases the overall amplifier noise; so, if the ambient light level is negligible, then disable the loop to improve SNR. The cancellation loop helps save PCB space and system costs by eliminating the need for external AC coupling passive components. Additionally, the extra trace inductance and PCB capacitance introduced by using external AC coupling components degrades the LMH32404-Q1 dynamic performance.

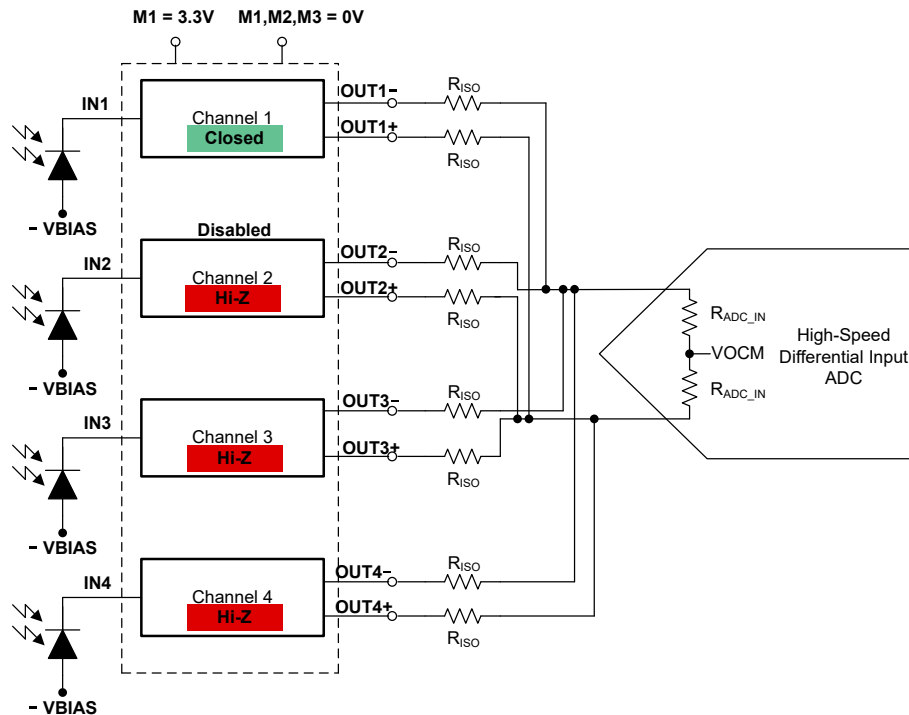
The ambient light cancellation loop is active (depending on  $\overline{\text{IDC\_EN}}$  configuration) when one or more of the channels is in standby mode. The ambient light cancellation loop is disabled when the amplifier is placed in low-power mode. When the LMH32404-Q1 is brought out of low-power operation the ambient light cancellation loop requires several time constants to settle. The time constant is based on the 400-kHz cutoff frequency of the loop. When in standby mode, the ALC loop is still active depending on  $\overline{\text{IDC\_EN}}$  configuration.

### 7.4.2 Channel Multiplexer Mode

The LMH32404-Q1 is a highly integrated transimpedance amplifier device with four independent channels. Each channel has its own single-ended input, differential output stage and multiplexing switch. The integrated switch can be used to disconnect the differential output amplifier from the output pin, thereby enabling high-impedance output for the respective channel.

Figure 7-4 shows how this device feature can further save board space and cost by eliminating the need for discrete high-speed multiplexer in a system that consists of several amplifier channels multiplexed to a single ADC channel. When switching between different channels, the LMH32404-Q1 has a transition time of 10 ns (typical). The disabled channel outputs are high-impedance so multiple amplifier outputs can be directly shorted to each other. If one channel is enabled and other channels are disabled, the disabled channels will not load the enabled channel. This further makes the LMH32404-Q1 easy to use in photodiode array applications.

Set Mx (M1, M2, M3, or M4) high for the corresponding channel to be enabled and output switches closed. Set Mx to logic low (default state) for the corresponding channel to be disabled (standby mode) and output switches open. When the channel is in its standby power mode, the clamp circuitry is still active thereby protecting the TIA input. Also, when in standby mode, the ALC loop is still active depending on  $\overline{\text{IDC\_EN}}$  configuration.



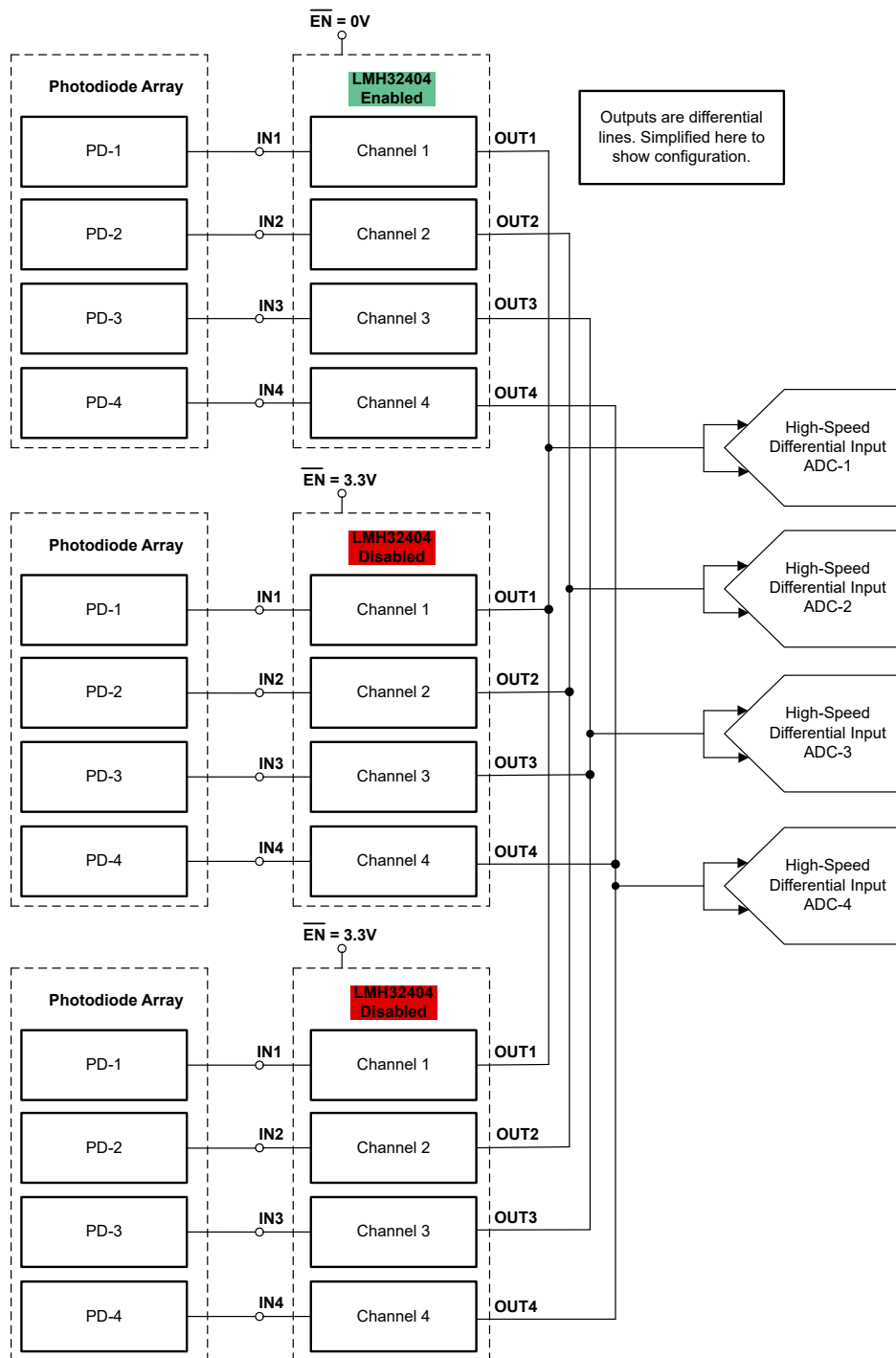
**Figure 7-3. Configuring LMH32404-Q1 in Channel Multiplexer Mode to Drive a Single ADC**

### 7.4.3 Low-Power Mode

The LMH32404-Q1 can be placed in low-power mode by setting  $\overline{\text{EN}}$  high, which helps in saving system power. Enabling low-power mode puts the outputs of the internal amplifiers in the LMH32404-Q1, including the differential outputs, in a high-impedance state.

If a system consists of high number of amplifier channels multiplexed to a few ADC channels. Figure 7-4 shows how this device feature can further save board space and cost by eliminating the need for a discrete high-speed multiplexer. The disabled LMH32404-Q1 outputs are high-impedance so multiple LMH32404-Q1 device outputs can be directly shorted to each other. If one LMH32404-Q1 device is enabled and others are disabled, the disabled devices will not load the enabled device. This further makes the LMH32404-Q1 easy to use in photodiode array applications.

When the amplifier is in its low-power mode, the clamp circuitry is still active thereby protecting the TIA input. The ambient light cancellation loop is disabled when the amplifier is placed in low-power mode. When the LMH32404-Q1 is brought out of low-power operation the ambient light cancellation loop requires several time constants to settle. The time constant is based on the 400-kHz cutoff frequency of the loop.



**Figure 7-4. Configuring Three LMH32404-Q1 Devices to Drive Four ADC Channels**

## Note

## 8.1 Application Information

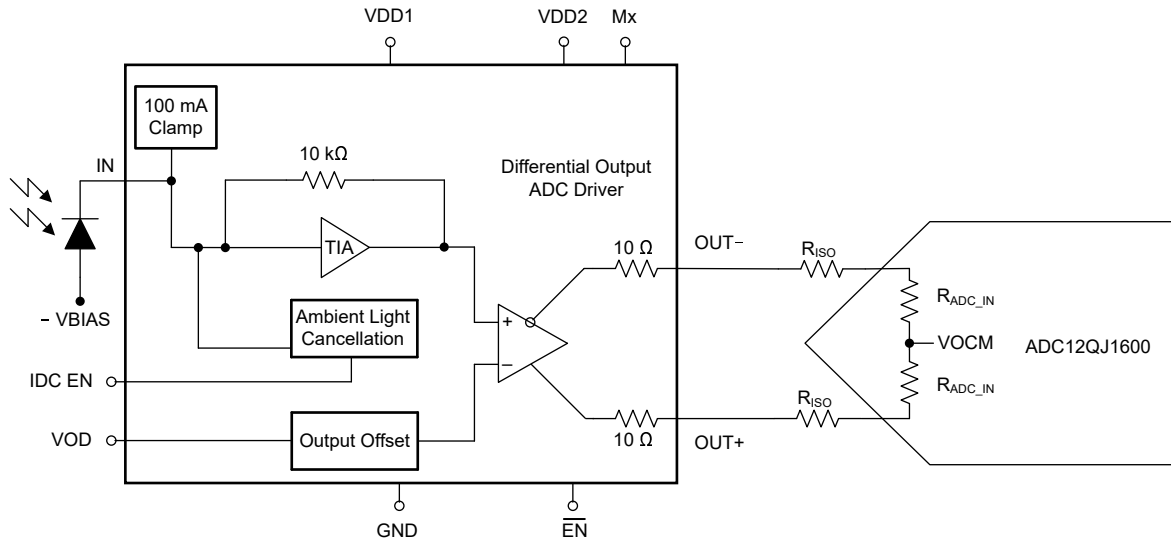
### Figure 8-1. LMH32404-Q1 (Single Channel) to ADC Interface

$$A_v = 20 \text{ k}\Omega \times 1.2 \times \frac{2 \times R_{\text{ADC\_IN}}}{(2 \times R_{\text{ADC\_IN}} + 20 \text{ }\Omega)} \quad (2)$$

where

- $A_V$  = Differential gain from the TIA input to the ADC input
- $R_{ADC\_IN}$  = Input resistance of the ADC

Figure 8-2 shows that in some designs a matching resistor network can be inserted between the LMH32404-Q1 output and the ADC inputs. Equation 3 gives the effective gain from the TIA input to the ADC input when using a matching resistor network.



**Figure 8-2. LMH32404-Q1 (Single Channel) to ADC Interface With a Matching Resistor Network**

$$A_V = 20 \text{ k}\Omega \times 1.2 \times \frac{2 \times R_{\text{ADC\_IN}}}{(2 \times R_{\text{ADC\_IN}} + 2 \times R_{\text{ISO}} + 20 \Omega)} \quad (3)$$

where

- $A_V$  = Gain from the TIA input to the ADC input
- $R_{\text{ADC\_IN}}$  = Differential input resistance of the ADC
- $R_{\text{ISO}}$  = Series resistance between the TIA and ADC

Equation 4 gives the voltage to be applied at the VOD pin (pin 10) if a certain differential offset voltage ( $V_{\text{OD}}$ ) is needed at the ADC input for the circuit in Figure 8-2.

$$V_{\text{OD}} = V_{\text{OD}} \times \left( \frac{1}{1.2} \right) \times \frac{(2 \times R_{\text{ADC\_IN}} + 2 \times R_{\text{ISO}} + 20 \Omega)}{(2 \times R_{\text{ADC\_IN}})} \quad (4)$$

where

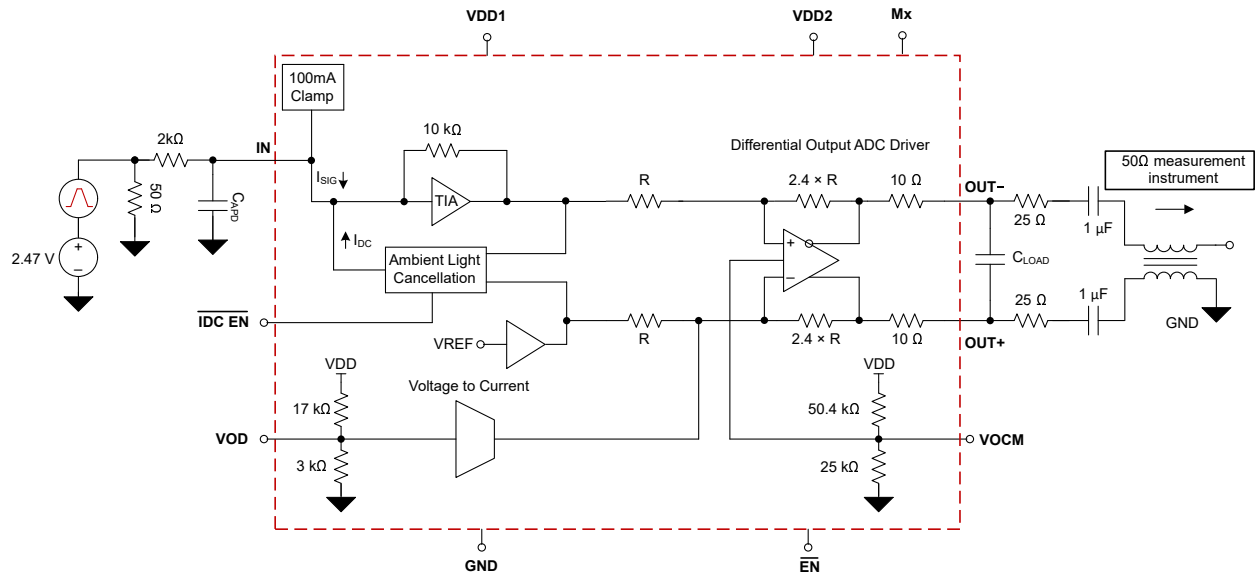
- $V_{\text{OD}}$  = Voltage applied at pin 10
- $V_{\text{OD}}$  = Desired differential offset voltage at the ADC input
- $R_{\text{ADC\_IN}}$  = Differential input resistance of the ADC
- $R_{\text{ISO}}$  = Series resistance between the TIA and ADC



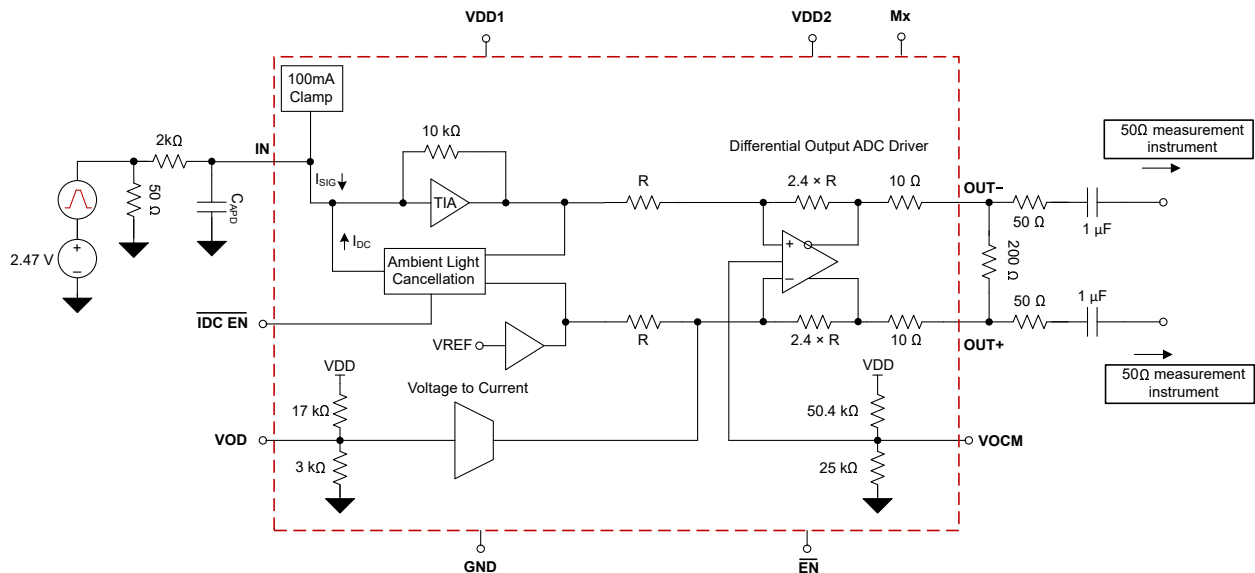
## 8.2 Typical Application

### 8.2.1 Standard TIA Application

Figure 8-3 and Figure 8-4 shows the circuit used to test the LMH32404-Q1 with a voltage source.



**Figure 8-3. LMH32404-Q1 Single Channel Test Circuit for Single-Ended Measurement**



**Figure 8-4. LMH32404-Q1 Single Channel Test Circuit for Differential Measurement**

#### 8.2.1.1 Design Requirements

The objective is to design a low-noise, wideband differential output transimpedance amplifier. The design requirements are:

- Amplifier supply voltage: 3.3 V
- Transimpedance gain: 20 kΩ
- Photodiode capacitance:  $C_{APD} = 1$  pF
- Target bandwidth: > 300 MHz
- Multiple channels for array applications

### 8.2.1.2 Detailed Design Procedure

Figure 8-3 and Figure 8-4 shows the LMH32404-Q1 test circuit used to measure its bandwidth, noise and transient response. The voltage source is DC biased close to the input bias voltage of the LMH32404-Q1. The LMH32404-Q1 internal design is optimized to only source current out of the input pin (INx). When testing the LMH32404-Q1 with a network analyzer or sinusoidal source, set the DC bias such that sum of the input AC and DC component does not result in a sourcing current into the amplifier input. Only use the LMH32404-Q1 with avalanche photodiodes (APDs) that sink current. An anode-biased APD satisfies this requirement.

Figure 8-5 shows the measured results for bandwidth of LMH32404-Q1 for all four channels.

Figure 8-6 shows the output noise spectral density of the LMH32404-Q1 with  $C_{APD} = 1$  pF and no photodiode capacitance.

Figure 8-7 shows the turn-on time of the LMH32404-Q1 channel when the Mx pin is toggled from logic low to high. When the amplifier is off, the output is in a high-impedance state. When the amplifier turns on, the output settles and starts tracking the input within a few nanoseconds.

Figure 8-8 shows the turn-off time of the LMH32404-Q1 channel when the Mx pin is toggled from logic high to low. When the amplifier is off, the output is in a high-impedance state.

### 8.2.1.3 Application Curves

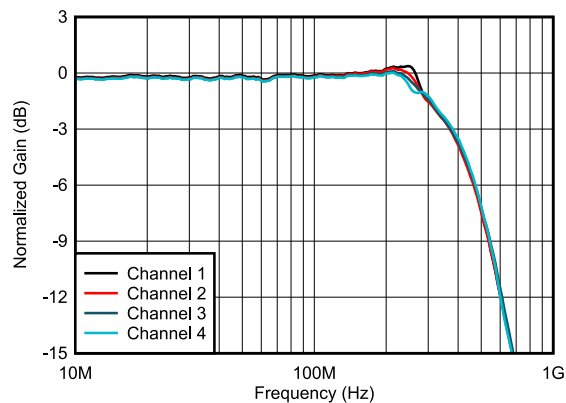


Figure 8-5. Transimpedance Bandwidth

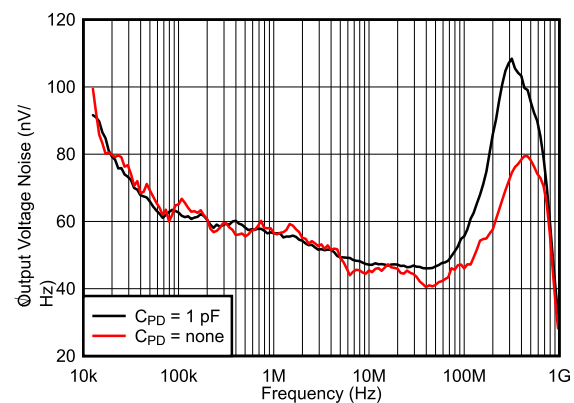


Figure 8-6. Output Noise Spectral Density

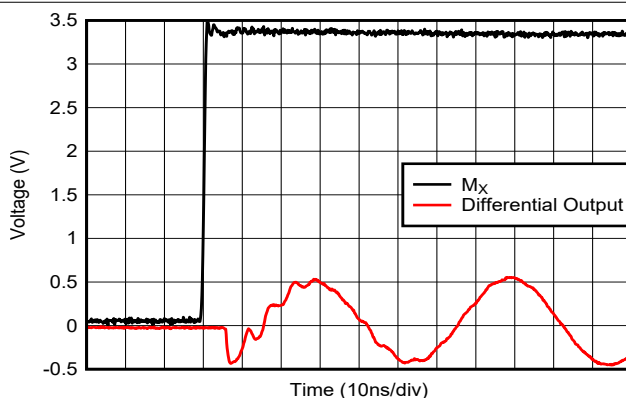


Figure 8-7. Channel Turn-On Response

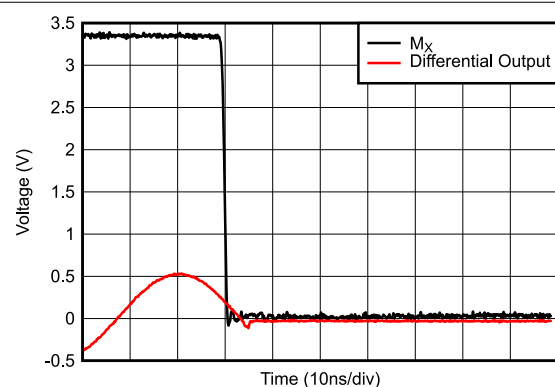


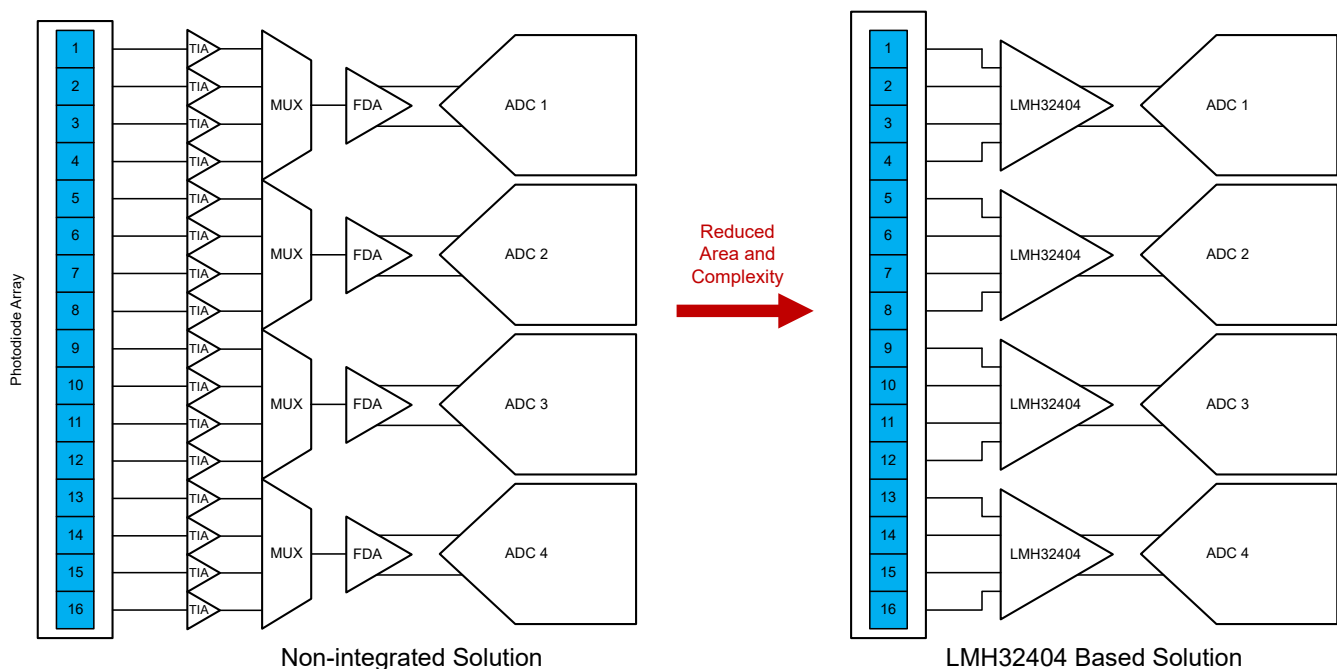
Figure 8-8. Channel Turn-Off Response

## 8.2.2 Increase Channel Density for Optical Front-End Systems

Modern LiDAR systems are moving towards solid state configurations with multi-channel photodiode arrays. For optical front-end designs it is impractical to have single transimpedance amplifiers (TIA) connected to each diode output along with additional multiplexers or other switching solutions to connect to the digitizer. This approach causes increased solution size, complexity and signal degradation.

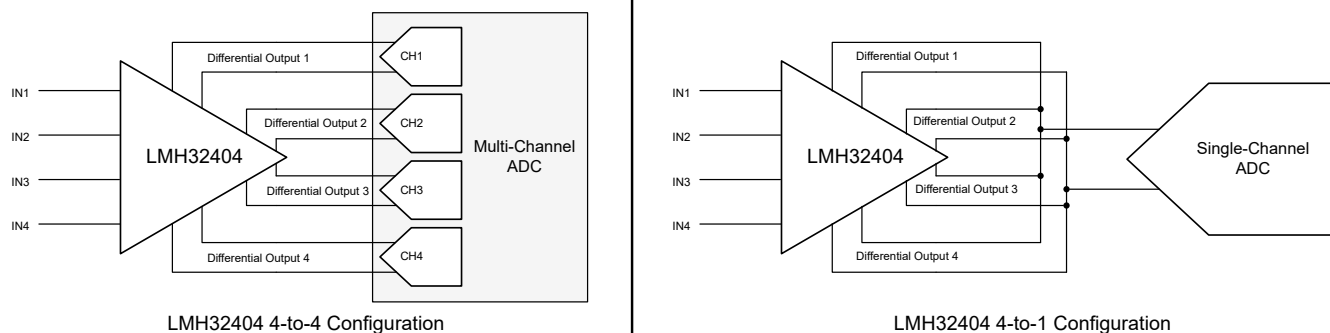
The LMH32404-Q1 resolves this problem in two ways, by providing higher integration within the device and by allowing user configured output multiplexing for independent output control.

Figure 8-9 shows a comparison of a non-integrated front end using individual amplifiers, a multiplexer, and fully-differential amplifier (FDA) to connect to the differential input ADC. In comparison, the front end using the LMH32404-Q1 is able to connect four channels per amplifier to each ADC or set of ADC differential inputs. Figure 8-9 shows how the LMH32404-Q1 improves solution size and system complexity compared to a non-integrated solution. With the additional features like input current clamps and ambient light cancellation, LMH32404-Q1 also improves system design and eliminates need for additional circuitry.



**Figure 8-9. Solution Size Comparison**

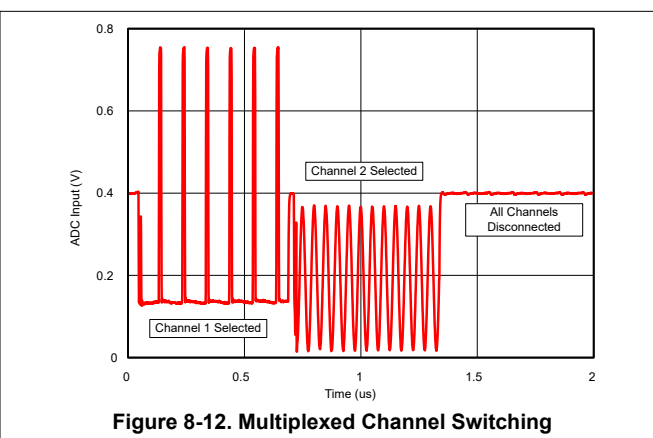
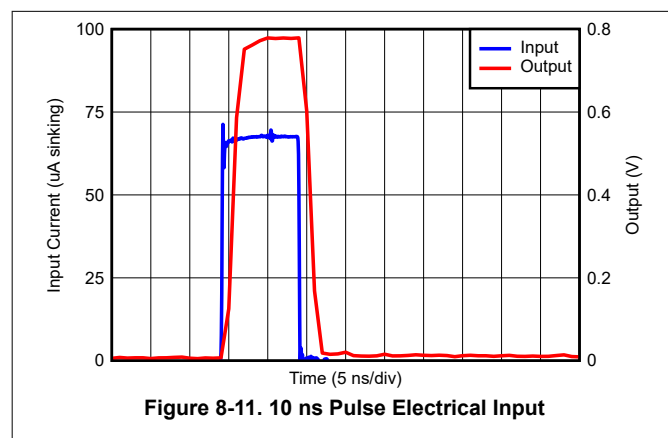
LMH32404-Q1 is a quad-channel device and each channel has an independent differential output stage and multiplexing switch. Figure 8-10 shows two common output configurations. In a four-to-four configuration the LMH32404-Q1 operates with no output multiplexing with each input and corresponding differential output active. This configuration is useful when the user needs to be able to capture data from four optical sensors simultaneously. In a four-to-one configuration, the LMH32404-Q1 internally multiplexes all four differential outputs into a single differential output. The LMH32404-Q1 outputs can be configured in any permutation such as one channel operating in one-to-one mode with the other three channels multiplexed in a three-to-one configuration. This independent control and multiplexing feature significantly increases channel density for systems that do not need to record all inputs simultaneously.



**Figure 8-10. LMH32404 Multiplexing Configuration Examples**

To show the front-end design integration and multiplexing capability, the LMH32404-Q1 performance was measured with the ADC12QJ1600-Q1 quad channel analog to digital converter. [Figure 8-11](#) shows the data measured from the ADC12QJ1600-Q1 using a 10 ns electrical input pulse on a single channel of the LMH32404-Q1. These pulses are similar to outputs seen in a typical LiDAR application. [Figure 8-12](#) shows the data from the ADC12QJ1600-Q1 when the LMH32404-Q1 outputs multiplex between different channels. The initial output shows a 10ns duration pulse train on channel 1, followed by a 20 MHz sinusoidal signal on channel 2 and then the output with all channels turned off but the input signals still present. Details on these measurements and application are discussed in the application brief, [How to Increase the Channel Density of LiDAR Systems with the 4-Channel LMH32404 Transimpedance Amplifier](#).

### 8.2.2.1 Application Curves



## 9 Power Supply Recommendations

The LMH32404-Q1 operates on 3.3-V supplies. The VDD1 and VDD2 pins must always be driven from the same supply source and individually bypassed. Use multiple bypass capacitors in parallel, because a low power-supply source impedance must be maintained across frequency. Place the bypass capacitors as close to the supply pins as possible. Place the smallest capacitor on the same side of the PCB as the LMH32404-Q1. Placing the larger valued bypass capacitors on the same side of the PCB is preferable as well; if there are space constraints however, the capacitors can be moved to the opposite side of the PCB using multiple vias to reduce the series inductance resulting from the vias. The LMH32404-Q1 can be run on bipolar supplies by connecting pins 11 and 26 to the negative supply. The thermal pad must always be connected to the most negative supply. The digital pin threshold voltages must be appropriately level shifted as they are referred to voltages at pins 11 and 26.

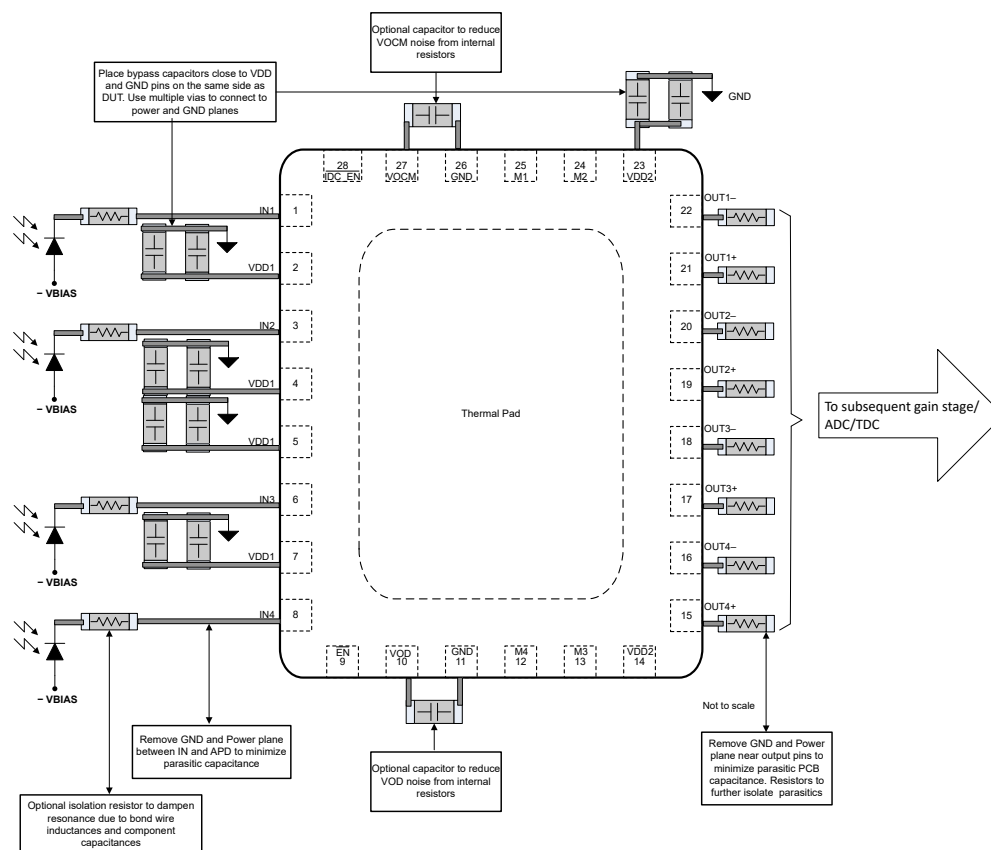
## 10 Layout

### 10.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier such as the LMH32404-Q1 requires careful attention to board layout parasitics and external component types. Recommendations that optimize performance include:

- **Minimize parasitic capacitance from the signal I/O pins to ac ground.** Parasitic capacitance on the output pins can cause instability, whereas parasitic capacitance on the input pin reduces the amplifier bandwidth. Cut out the power and ground traces under the signal input and output pins to reduce unwanted capacitance. Otherwise, ground and power planes must be unbroken elsewhere on the board.
- **Minimize the distance from the power-supply pins to high-frequency bypass capacitors.** Use low inductance ceramic capacitors as decoupling capacitors with voltage ratings at least three times greater than the amplifiers maximum power supplies. Place a combination of 100 pF (or higher) and 33 nF (or higher) capacitors on the same side as the DUT. If space constraints force the larger value bypass capacitors to be placed on the opposite side of the PCB, use multiple vias on the supply and ground side of the capacitors. This configuration makes sure that there is a low-impedance path to the amplifiers power-supply pins across the amplifiers gain bandwidth specification. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. Larger (2.2- $\mu$ F to 6.8- $\mu$ F) decoupling capacitors that are effective at lower frequency must be used on the supply pins. Place these decoupling capacitors further from the device. Share the decoupling capacitors among several devices in the same area of the printed circuit board (PCB).
- For more information on board design and layout, see the evaluation module user guide, [LMH32404 Evaluation Module User's Guide](#).

### 10.2 Layout Example



**Figure 10-1. Layout Recommendation**

## 11 Device and Documentation Support

### 11.1 Device Support

#### 11.1.1 Development Support

- Texas Instruments, [LIDAR-Pulsed Time-of-Flight Reference Design design guide](#)
- Texas Instruments, [LIDAR-Pulsed Time-of-Flight Reference Design: Using High-Speed Data Converters design guide](#)
- Texas Instruments, [Optical Front-End System Reference Design design guide](#)

### 11.2 Documentation Support

#### 11.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [LMH32404 Evaluation Module user's guide](#)
- Texas Instruments, [Training Video: High speed TIAs for optical time of flight and LIDAR systems](#)
- Texas Instruments, [Training Video: Multi-channel optical front-end reference design overview](#)
- Texas Instruments, [Training Video: How to Convert a TINA-TI Model into a Generic SPICE Model](#)
- Texas Instruments, [Transimpedance Considerations for High-Speed Amplifiers application report](#)
- Texas Instruments, [What You Need To Know About Transimpedance Amplifiers – Part 1 blog](#)
- Texas Instruments, [What You Need To Know About Transimpedance Amplifiers – Part 2 blog](#)

### 11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMH32404QWRHFRQ1	Active	Production	VQFN (RHF)   28	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	32404Q
LMH32404QWRHFRQ1.B	Active	Production	VQFN (RHF)   28	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	32404Q

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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### OTHER QUALIFIED VERSIONS OF LMH32404-Q1 :

- Catalog : [LMH32404](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product



## TAPE AND REEL INFORMATION



\*All dimensions are nominal

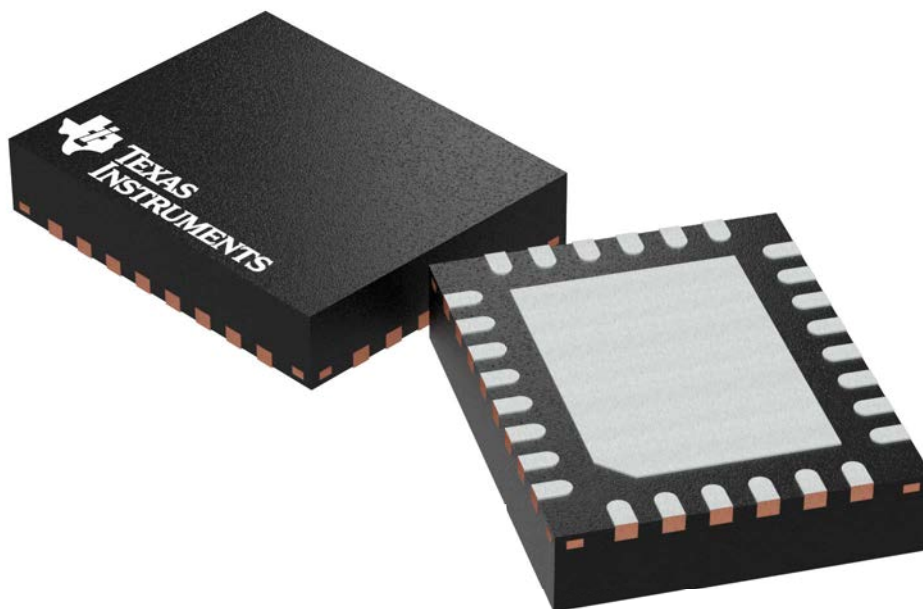
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH32404QWRHFRQ1	VQFN	RHF	28	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS

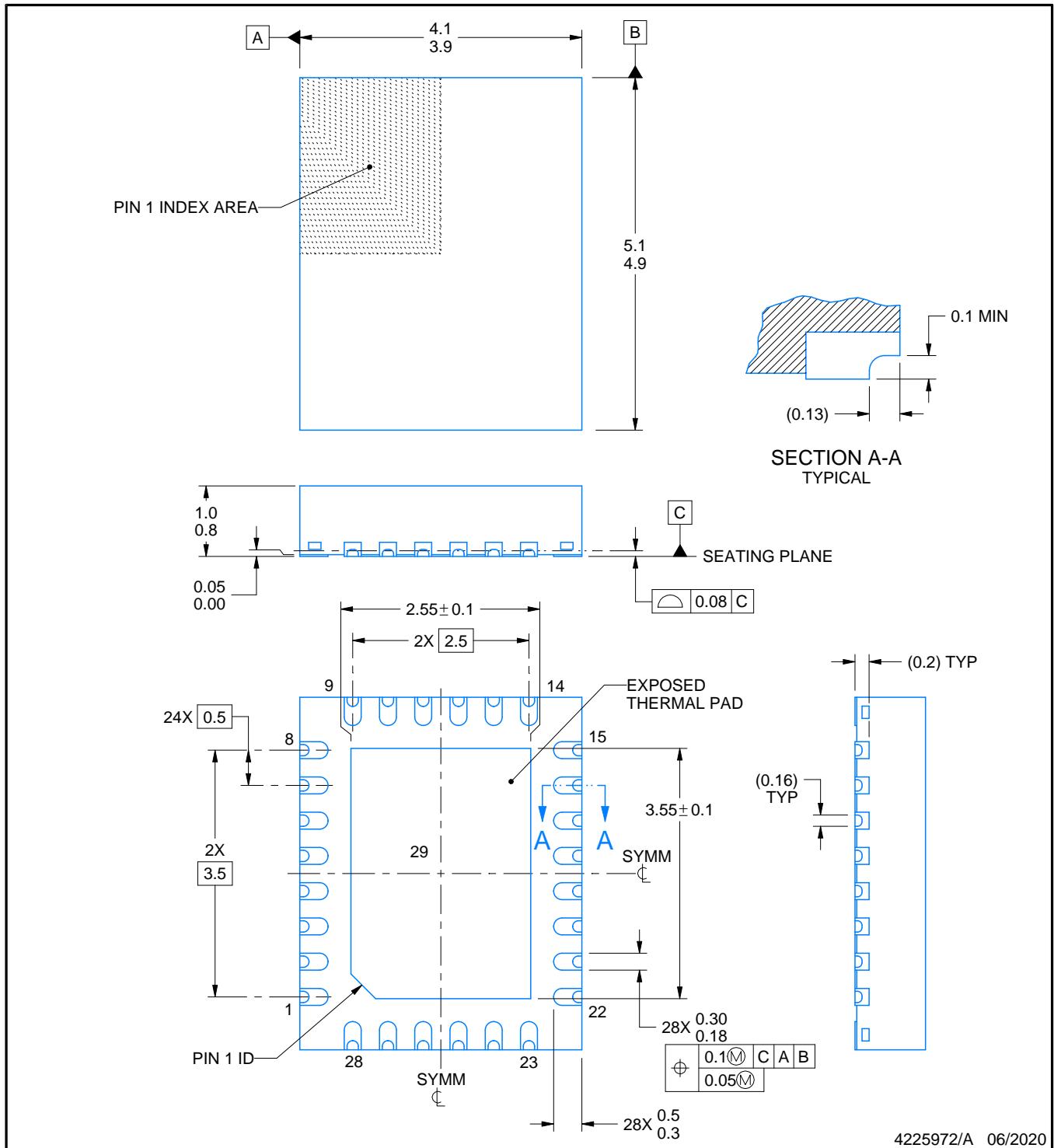
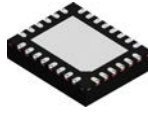


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH32404QWRHFRQ1	VQFN	RHF	28	3000	367.0	367.0	35.0



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



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## NOTES:

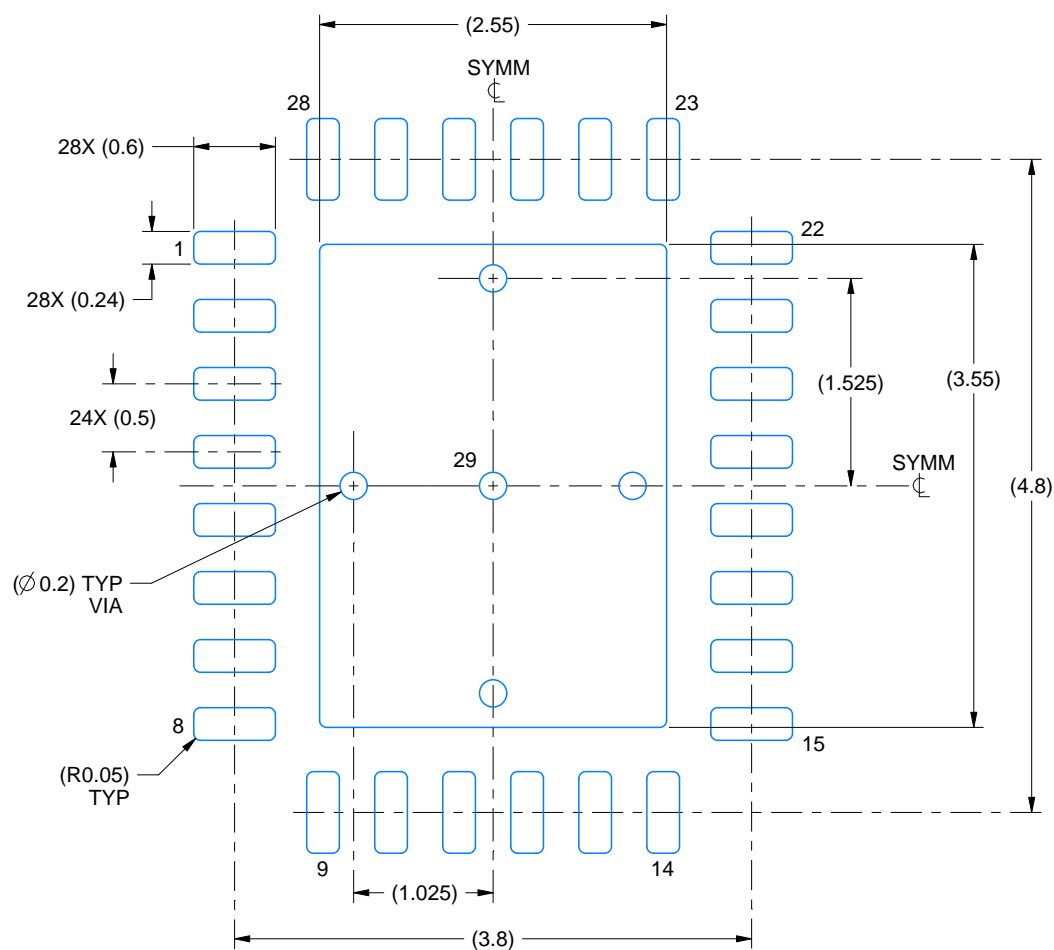
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

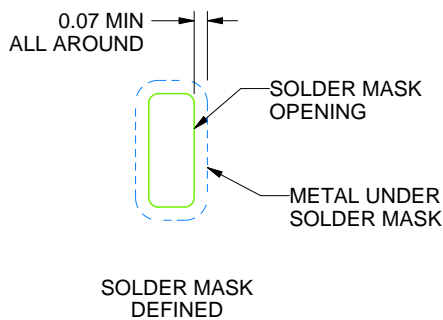
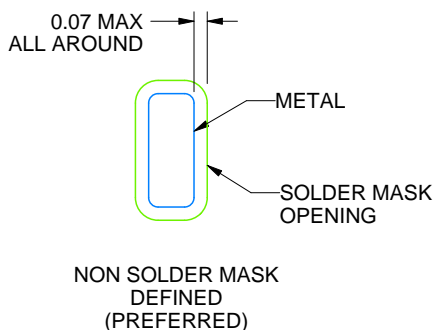
RHF0028B

VQFN - 1.0 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:18X



SOLDER MASK DETAILS

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NOTES: (continued)

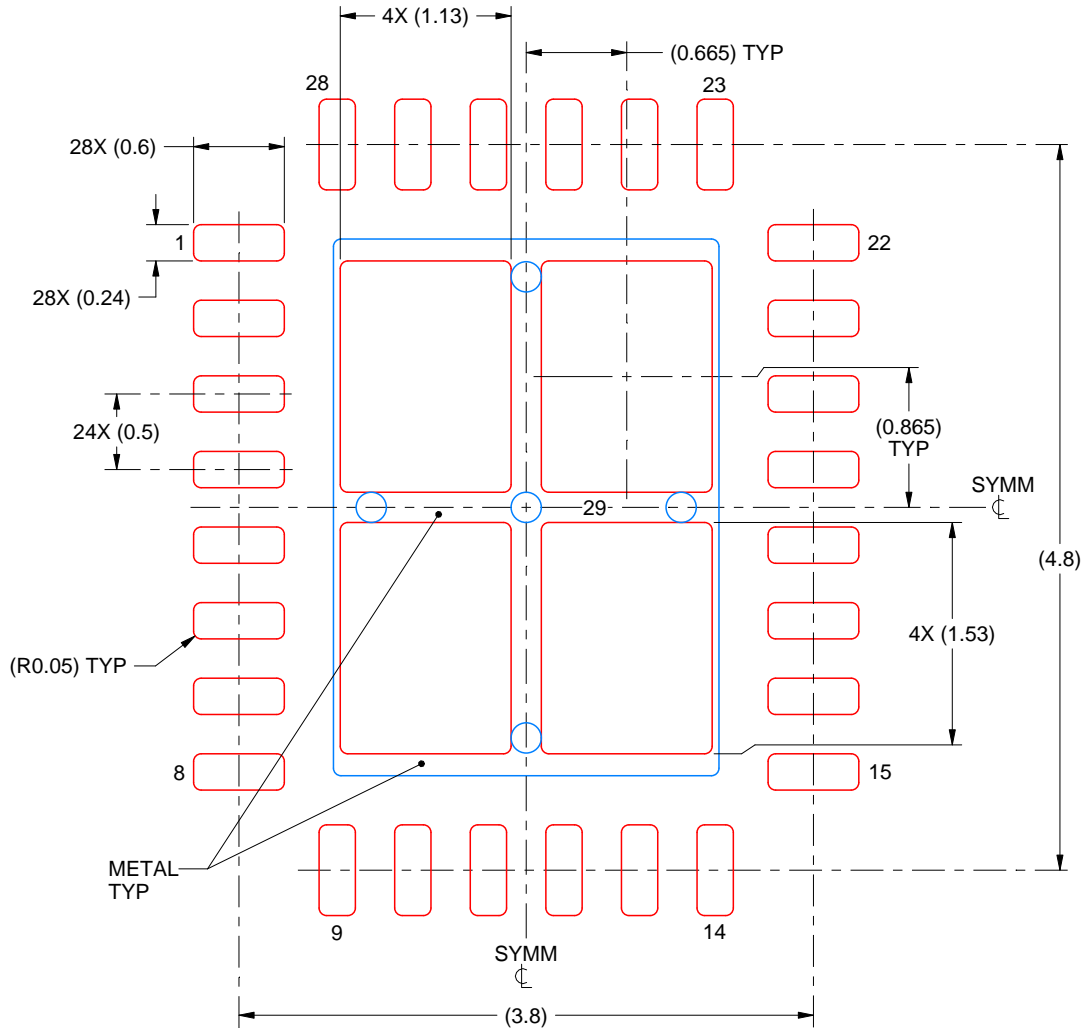
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RHF0028B

VQFN - 1.0 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 29  
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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