LMH1228 12G UHD-SDI Dual Output Cable Driver With Integrated Reclocker

1 Features

- Supports ST-2082-1 (12G), ST-2081-1 (6G), ST-424 (3G), ST-292 (HD), and ST-259 (SD)
- Compatible with DVB-ASI and AES10 (MADI)
- Integrated reclocker locks to SMPTE rates of 11.88 Gbps, 5.94 Gbps, 2.97 Gbps, 1.485 Gbps or divide-by-1.001 sub-rates and 270 Mbps
- Integrated Eye Opening Monitor (EOM)
- Dual differential output cable drivers
- On-chip 75-Ω termination and return loss compensation network
- Adaptive PCB input equalizer
- Reclocked 100-Ω loop-back output
- Automatic slew rate control on 75-Ω outputs
- Automatic pre-emphasis and output amplitude on 75-Ω outputs
- Programmable de-emphasis and output amplitude on 100-Ω output
- Polarity inversion on 75-Ω and 100-Ω outputs
- Automatic power save in absence of input signal
  - Power Consumption: 25 mW (Typical)
- Power-Down Control Through ENABLE Pin
- Single 2.5-V Supply
  - Power consumption: 305 mW (typical)
- Programmable through pins, SPI, or SMBus interface
- –40°C to +85°C operating temperature range
- 5-mm × 5-mm, 32-pin WQFN package

2 Applications

- SMPTE compatible serial digital interface
- UHDTV/4K/8K/HDTV/SDTV video
- Broadcast video routers, switchers, distribution amplifiers, and monitors
- Digital video processing and editing

3 Description

LMH1228 device is a 12G UHD-SDI low power dual output cable driver with integrated reclocker. It supports SMPTE video rates up to 11.88 Gbps, enabling UHD video for 4K/8K applications. With a wide range clock-and-data recovery (CDR) circuit, the on-chip reclocker automatically detects and locks to all SMPTE video rates up to 11.88 Gbps. The additional reclocked 100-Ω driver output on the host-side can be used for monitoring or signal distribution purposes.

The on-chip reclocker attenuates high-frequency jitter and fully regenerates the data using a clean, low-jitter clock. The reclocker has a built-in loop filter and does not require any input reference clock. The LMH1228 also has an internal eye opening monitor and a programmable pin for CDR lock indication, input signal detect, or hardware interrupts to support system diagnostics and board bring-up.

The LMH1228 is powered from a single 2.5-V supply. It is offered in a small footprint 5 mm × 5 mm 32-pin WQFN package. The LMH1228 is pin compatible with the LMH1208 (12G Dual Cable Driver).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMH1228	WQFN (32)	5.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Block Diagram

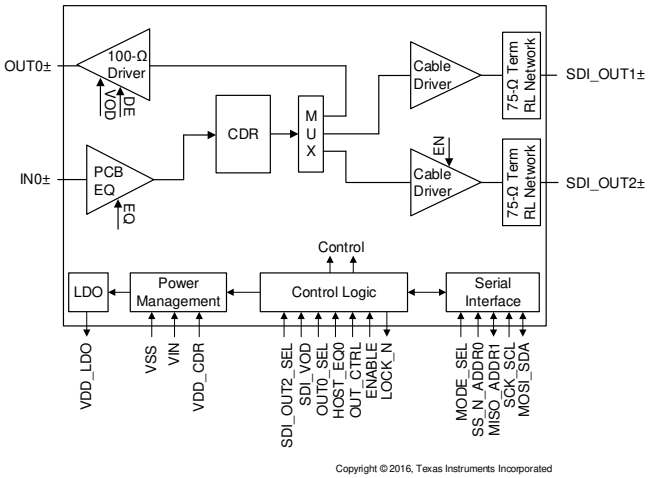


Table of Contents

4 Revision History

Changes from Revision C (October 2019) to Revision D **Page**

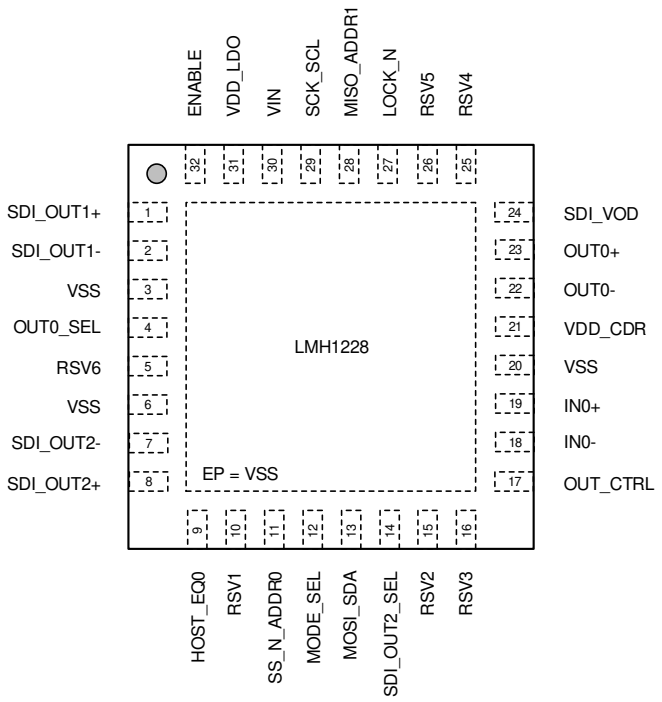
- Changed HBM ESD rating and added pin 27 description ... 5

Changes from Revision B (September 2017) to Revision C **Page**

- Initial Public Release ... 1

5 Pin Configuration and Functions

RTV Package
32-Pin WQFN
Top View



Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
HIGH-SPEED DIFFERENTIAL I/OS			
SDI_OUT1+	1	I/O, Analog	Single-ended complementary outputs with on-chip 75-Ω termination at SDI_OUT1+ and SDI_OUT1–. SDI_OUT1± include integrated return loss networks designed to meet the SMPTE output return loss requirements. Connect SDI_OUT1+ to a BNC through a 4.7-µF, AC-coupling capacitor. SDI_OUT1– should be similarly AC-coupled and terminated with an external 4.7-µF capacitor and 75-Ω resistor to GND.
SDI_OUT1–	2	I/O, Analog	
SDI_OUT2+	8	O, Analog	Single-ended complementary outputs with on-chip 75-Ω termination at SDI_OUT2+ and SDI_OUT2–. SDI_OUT2± include integrated return loss networks designed to meet the SMPTE output return loss requirements. SDI_OUT2± is used as a second cable driver. Connect SDI_OUT2+ to a BNC through a 4.7-µF, AC-coupling capacitor. SDI_OUT2– should be similarly AC-coupled and terminated with an external 4.7-µF capacitor and 75-Ω resistor to GND.
SDI_OUT2–	7	O, Analog	
IN0+	19	I, Analog	Differential inputs from host video processor. On-chip 100-Ω differential termination. Requires external 4.7-µF, AC-coupling capacitors for SMPTE applications.
IN0–	18	I, Analog	
OUT0+	23	O, Analog	Differential outputs to host video processor. On-chip 100-Ω differential termination. Requires external 4.7-µF, AC-coupling capacitors for SMPTE applications.
OUT0–	22	O, Analog	
CONTROL PINS			
OUT0_SEL	4	I, LVCMOS	OUT0_SEL enables the use of the 100-Ω host-side output driver at OUT0±. See Table 2 for details. OUT0_SEL is internally pulled high by default (OUT0 disabled).
HOST_EQ0	9	I, 4-LEVEL	HOST_EQ0 selects the equalizer setting for IN0±. See Table 4 for details.
MODE_SEL	12	I, 4-LEVEL	MODE_SEL enables the SPI or SMBus serial control interface. See Table 9 for details.
SDI_OUT2_SEL	14	I, LVCMOS	SDI_OUT2_SEL enables the use of the 75-Ω output driver at SDI_OUT2±. See Table 2 for details. SDI_OUT2_SEL is internally pulled high by default (SDI_OUT2 disabled).

(1) I = Input, O = Output, I/O = Input or Output, OD = Open Drain, LVCMOS = 2-State Logic, 4-LEVEL = 4-State Logic

Pin Functions (continued)

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
OUT_CTRL	17	I, 4-LEVEL	OUT_CTRL selects the signal being routed to the output. It is used to enable or bypass the reclocker. See Table 6 for details.
SDI_VOD	24	I, 4-LEVEL	SDI_VOD selects one of four output amplitudes for the cable drivers at SDI_OUT1± and SDI_OUT2±. See Table 7 for details.
LOCK_N	27	O, LVCMOS, OD	LOCK_N is the reclocker lock indicator. LOCK_N is pulled low when the reclocker has acquired lock condition. LOCK_N is a 3.3-V tolerant, open-drain output. It requires an external resistor to a logic supply. LOCK_N can be reconfigured to indicate Signal Detector (SD_N) or Interrupt (INT_N) through register programming. See *Status Indicators and Interrupts*.
ENABLE	32	I, LVCMOS	A logic-high at ENABLE enables normal operation for the LMH1228. A logic-low at ENABLE places the LMH1228 in Power-Down Mode. ENABLE is internally pulled high by default.
SPI SERIAL CONTROL INTERFACE, MODE_SEL = F (FLOAT)			
SS_N	11	I, LVCMOS	SS_N is the Slave Select. When SS_N is at logic Low, it enables SPI access to the LMH1228 slave device. SS_N is a 2.5-V LVCMOS input and is internally pulled high by default.
MOSI	13	I, LVCMOS	MOSI is the SPI serial control data input to the LMH1228 slave device when the SPI bus is enabled. MOSI is a 2.5-V LVCMOS input. An external pullup resistor is recommended.
MISO	28	O, LVCMOS	MISO is the SPI serial control data output from the LMH1228 slave device. MISO is a 2.5-V LVCMOS output.
SCK	29	I, LVCMOS	SCK is the SPI serial input clock to the LMH1228 slave device when the SPI interface is enabled. SCK is a 2.5-V LVCMOS input. An external pullup resistor is recommended.
SMBUS SERIAL CONTROL INTERFACE, MODE_SEL = L (1 KΩ TO VSS)			
ADDR0	11	Strap, 4-LEVEL	ADDR[1:0] are 4-level straps, read into the device at power up. They are used to select one of the 16 supported SMBus addresses when SMBus is enabled. See Table 10 for details.
SDA	13	I/O, LVCMOS, OD	SDA is the SMBus bidirectional data line to or from the LMH1228 slave device when SMBus is enabled. SDA is an open-drain I/O and requires an external pullup resistor to the SMBus termination voltage. SDA is 3.3-V tolerant.
ADDR1	28	Strap, 4-LEVEL	ADDR[1:0] are 4-level straps, read into the device at power up. They are used to select one of the 16 supported SMBus addresses when SMBus is enabled. See Table 10 for details.
SCL	29	I/O, LVCMOS, OD	SCL is the SMBus input clock to the LMH1228 slave device when SMBus is enabled. It is driven by a LVCMOS open-drain driver from the SMBus master. SCL requires an external pullup resistor to the SMBus termination voltage. SCL is 3.3-V tolerant.
RESERVED			
RSV1 RSV2 RSV3 RSV4 RSV5	10 15 16 25 26	—	Reserved pins. Do not connect.
RSV6	5	I, LVCMOS	Reserved pin. This input must be tied high with 1-kΩ resistor to VIN. Alternatively, this pin setting can be overridden by register control. Refer to the *LMH1228 and LMH1208 Programming Guide* (SNAU206) for more details.
POWER			
VSS	3, 6, 20	I, Ground	Ground reference.
VDD_CDR	21	I, Power	VDD_CDR powers the reclocker circuitry. It is connected to the same 2.5-V ± 5% supply as VIN.
VIN	30	I, Power	VIN is connected to an external 2.5-V ± 5% power supply.
VDD_LDO	31	O, Power	VDD_LDO is the output of the internal 1.8-V LDO regulator. VDD_LDO output requires an external 1-µF and 0.1-µF bypass capacitor to VSS. The internal LDO is designed to power internal circuitry only.
EP	—	I, Ground	EP is the exposed pad at the bottom of the RTV package. The exposed pad should be connected to the VSS plane through a 3 × 3 via array.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage (VIN, VDD_CDR)	–0.5	2.75	V
Input voltage for 4-level pins	–0.5	2.75	V
Input/output voltage for 2-level control pins	–0.5	2.75	V
SMBus input/output voltage (SDA, SCL)	–0.5	4	V
SPI input/output voltage (SS_N, MISO, MOSI, and SCK)	–0.5	2.75	V
High-speed input/output voltage (IN0±, SDI_OUT1±, OUT0±, SDI_OUT2±)	–0.5	2.75	V
Input current (IN0±)	–30	30	mA
Operating junction temperature		125	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins except 13, 27, and 29	±6000	V
		Pins 13, 27, and 29	±5000	
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
	Supply voltage	VIN, VDD_CDR to VSS	2.375	2.5	2.625	V
VDD_{SMBUS}	SMBus: SDA, SCL open-drain termination voltage		2.375		3.6	V
V_{IN0_LAUNCH}	Source differential launch amplitude	Before 5-inch board trace to IN0±	300		850	mVp-p
		Before 20-inch board trace to IN0±	650		1000	
$T_{JUNCTION}$	Operating junction temperature				110	°C
$T_{AMBIENT}$	Ambient temperature		–40	25	85	°C
$NTps_{max}$	Maximum supply noise(1)	50 Hz to 1 MHz, sinusoidal		< 20		mVp-p
		1.1 MHz to 50 MHz, sinusoidal		< 10		

(1) The sum of the DC supply voltage and AC supply noise should not exceed the recommended supply voltage range.

6.4 Thermal Information

THERMAL METRIC[1]		LMH1228 RTV (WQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	6.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER						
PD	Power dissipation, Measured with PRBS10, CDR Locked to 11.88 Gbps, VOD = default, HEO/VEO lock monitor disabled	SDI_OUT1± enabled SDI_OUT2± disabled OUT0± disabled		305		mW
		SDI_OUT1± enabled SDI_OUT2± disabled OUT0± enabled		350		mW
		SDI_OUT1± enabled SDI_OUT2± enabled OUT0± disabled		442		mW
		SDI_OUT1± enabled SDI_OUT2± enabled OUT0± enabled		485		mW
PD_Z	Power dissipation, Power Save Mode	Power Save Mode, ENABLE = H, no signal applied at IN0±		25		mW
IDD	Current consumption, Measured with PRBS10, CDR Locked to 11.88 Gbps, VOD = default, HEO/VEO lock monitor disabled	SDI_OUT1± enabled SDI_OUT2± disabled OUT0± disabled		122	146	mA
		SDI_OUT1± enabled SDI_OUT2± disabled OUT0± enabled		140	166	mA
		SDI_OUT1± enabled SDI_OUT2± enabled OUT0± disabled		177	211	mA
		SDI_OUT1± enabled SDI_OUT2± enabled OUT0± enabled		194	230	mA
IDD_Z	Current consumption, Power Save Mode	Power Save Mode, ENABLE = H, no signal applied at IN0±		10		mA
IDD_{Z_PD}	Current consumption, Power-Down Mode	Power-Down Mode, ENABLE = L, no signal applied at IN0±		10	30	mA

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IDD_{TRANS}	Current consumption, CDR acquiring lock to 11.88 Gbps, VOD = default, HEO/VEO lock monitor enabled	SDI_OUT1± enabled SDI_OUT2± disabled OUT0± disabled			200	mA
		SDI_OUT1± enabled SDI_OUT2± disabled OUT0± enabled			225	mA
		SDI_OUT1± enabled SDI_OUT2± enabled OUT0± disabled			271	mA
		SDI_OUT1± enabled SDI_OUT2± enabled OUT0± enabled			290	mA
LVCMOS DC SPECIFICATIONS						
V_{IH}	Logic high input voltage	2-level input (SS_N, SCK, MOSI, SDI_OUT2_SEL, OUT0_SEL, ENABLE)	0.72 × VIN		VIN + 0.3	V
		2-level input (SCL, SDA)	0.7 × VIN		3.6	V
V_{IL}	Logic low input voltage	2-level input (SS_N, SCK, MOSI, SDI_OUT2_SEL, OUT0_SEL, ENABLE, SCL, SDA)	0		0.3 × VIN	V
V_{OH}	Logic high output voltage	IOH = –2 mA, (MISO)	0.8 × VIN		VIN	V
V_{OL}	Logic low output voltage	IOL = 2 mA, (MISO)	0		0.2 × VIN	V
		IOL = 3 mA, (LOCK_N, SDA)			0.4	V
I_{IH}	Input high leakage current (Vinput = VIN)	LVCMOS (SDI_OUT2_SEL, ENABLE)			15	µA
		LVCMOS (OUT0_SEL)			65	µA
		LVCMOS (LOCK_N)			10	µA
		SPI mode: LVCMOS (SS_N, SCK, MOSI)			15	µA
		SMBus mode: LVCMOS (SCL, SDA)			10	µA
I_{IL}	Input low leakage current (Vinput = GND)	LVCMOS (SDI_OUT2_SEL, ENABLE)	–50			µA
		LVCMOS (OUT0_SEL)	–15			µA
		LVCMOS (LOCK_N)	–10			µA
		SPI mode: LVCMOS (SCK, MOSI)	–15			µA
		SPI mode: LVCMOS (SS_N)	–50			µA
		SMBus mode: LVCMOS (SCL, SDA)	–10			µA

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
4-LEVEL LOGIC DC SPECIFICATIONS (APPLY TO ALL 4-LEVEL INPUT CONTROL PINS)						
V_{LVL_H}	LEVEL-H input voltage	Measured voltage at 4-level pin with external 1 kΩ to VIN		VIN		V
V_{LVL_F}	LEVEL-F default voltage	Measured voltage 4-level pin at default		2/3 × VIN		V
V_{LVL_R}	LEVEL-R input voltage	Measured voltage at 4-level pin with external 20 kΩ to VSS		1/3 × VIN		V
V_{LVL_L}	LEVEL-L input voltage	Measured voltage at 4-level pin with external 1 kΩ to VSS		0		V
I_{IH}	Input high leakage current (Vinput = VIN)	4-levels (HOST_EQ0, MODE_SEL, OUT_CTRL, SDI_VOD)	20	45	80	µA
		SMBus mode: 4-levels (ADDR0, ADDR1)	20	45	80	µA
I_{IL}	Input low leakage current (Vinput = GND)	4-levels (HOST_EQ0, MODE_SEL, OUT_CTRL, SDI_VOD)	–160	–93	–40	µA
		SMBus mode: 4-levels (ADDR0, ADDR1)	–160	–93	–40	µA
RECEIVER SPECIFICATIONS (IN0±)						
R_{IN0_TERM}	DC input differential termination	Measured across IN0+ to IN0–	80	100	120	Ω
RL_{IN0_SDD11}	Input differential return loss(1)	SDD11, 10 MHz – 2.8 GHz		–22		dB
		SDD11, 2.8 GHz – 6 GHz		–16		dB
		SDD11, 6 GHz – 11.1 GHz		–10		dB
RL_{IN0_SCD11}	Differential to common-mode input conversion(1)	SCD11, 10 MHz to 11.1 GHz		–21		dB
V_{IN0_CM}	DC common-mode voltage	Input common-mode voltage at IN0+ or IN0– to GND		2.06		V
CD_{ON_IN0}	Signal detect (default) Assert ON threshold level for IN0±	11.88 Gbps, EQ and PLL pathological pattern		20		mVp-p
CD_{OFF_IN0}	Signal detect (default) Deassert OFF threshold level for IN0±	11.88 Gbps, EQ and PLL pathological pattern		18		mVp-p
DRIVER OUTPUT (SDI_OUT1+ AND SDI_OUT2+)						
R_{OUT_TERM}	DC output single-ended termination	SDI_OUT1+ and SDI_OUT1–, SDI_OUT2+ and SDI_OUT2– to VIN	63	75	87	Ω
VOD_{CD_OUTP}	Output single-ended output voltage	Measure AC signal at SDI_OUT1+ and SDI_OUT2+, with SDI_OUT1– and SDI_OUT2– AC terminated with 75 Ω SDI_VOD = H		840		mVp-p
		SDI_VOD = F	720	800	880	mVp-p
		SDI_VOD = R		880		mVp-p
		SDI_VOD = L		760		mVp-p
VOD_{CD_OUTN}	Output single-ended output voltage	Measure AC signal at SDI_OUT1– and SDI_OUT2-, with SDI_OUT1+ and SDI_OUT2+ AC terminated with 75 Ω SDI_VOD = H		840		mVp-p
		SDI_VOD = F	720	800	880	mVp-p
		SDI_VOD = R		880		mVp-p
		SDI_VOD = L		760		mVp-p
PRE_{CD_OUTP}	Output pre-emphasis	Output pre-emphasis boost amplitude at SDI_OUT1+ and SDI_OUT2+, programmed to maximum setting through register, measured at SDI_VOD = F		2		dB

(1) This parameter is measured with the LMH1297EVM (Evaluation board for LMH1228).

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PRE_{CD_OUTN}	Output pre-emphasis	Output pre-emphasis boost amplitude at SDI_OUT1– and SDI_OUT2–, programmed to maximum setting through register, measured at SDI_VOD = F		2		dB
$t_{R\_F\_SDI}$	Output rise and fall time(1)	Measured with PRBS10 pattern, default VOD at 20% – 80% amplitude, default pre-emphasis enabled 11.88 Gbps		34	42	ps
		5.94 Gbps		36	43	ps
		2.97 Gbps		59	67	ps
		1.485 Gbps		60	73	ps
		270 Mbps	400	550	700	ps
$t_{R\_F\_DELTA}$	Output rise and fall time mismatch(1)	Measured with PRBS10 pattern, default VOD at 20% – 80% amplitude, default pre-emphasis enabled 11.88 Gbps		3	18	ps
		5.94 Gbps		2.7	12	ps
		2.97 Gbps		0.8	11	ps
		1.485 Gbps		0.8	12	ps
		270 Mbps		72	150	ps
$V_{OVERSHOOT}$	Output overshoot or undershoot (1)	Measured with PRBS10 pattern, default VOD, default pre-emphasis enabled(2) 12G/6G/3G/HD/SD		5%		
V_{DC_OFFSET}	DC offset	12G/6G/3G/HD/SD		±0.2		V
V_{DC_WANDER}	DC wander	12G/6G/3G/HD/SD with EQ pathological pattern		20		mV
RL_{CD_S22}	Output return loss at SDI_OUT1+ and SDI_OUT2+ reference to 75 Ω(1)	S22, 5 MHz to 1.485 GHz		–25		dB
		S22, 1.485 GHz to 3 GHz		–22		dB
		S22, 3 GHz to 6 GHz		–12		dB
		S22, 6 GHz to 12 GHz		–8		dB

(2) $V_{OVERSHOOT}$ overshoot/undershoot maximum measurements are largely affected by the PCB layout and input test pattern. The maximum value specified in *Electrical Characteristics* for $V_{OVERSHOOT}$ is based on bench evaluation across temperature and supply voltages with the LMH1297EVM.

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DRIVER OUTPUT (OUT0±)						
R_{OUT0_TERM}	DC output differential termination	Measured across OUT0+ and OUT0–	80	100	120	Ω
VOD_{OUT0}	Output differential voltage at OUT0±	Measured with 8T pattern HOST_EQ0 = H		410		mVp-p
		HOST_EQ0 = F	485	560	620	mVp-p
		HOST_EQ0 = R		635		mVp-p
		HOST_EQ0 = L		810		mVp-p
VOD_{OUT0_DE}	De-emphasized output differential voltage at OUT0±	Measured with 8T pattern HOST_EQ0 = H		410		mVp-p
		HOST_EQ0 = F		550		mVp-p
		HOST_EQ0 = R		545		mVp-p
		HOST_EQ0 = L		532		mVp-p
t_R/t_F	Output rise and fall time	Measured with 8T Pattern, 20% – 80% amplitude		45		ps
$RL_{OUT0-SDD22}$	Output differential return loss(1)	Measured with the device powered up and outputs a 10-MHz clock signal SDD22, 10 MHz – 2.8 GHz		–24		dB
		SDD22, 2.8 GHz – 6 GHz		–16		dB
		SDD22, 6 GHz – 11.1 GHz		–15		dB
$RL_{OUT0-SCC22}$	Output common-mode return loss(1)	Measured with the device powered up and outputs a 10-MHz clock signal. SCC22, 10 MHz – 4.75 GHz		–12		dB
		SCC22, 4.75 GHz – 11.1 GHz		–9		dB
V_{OUT0_CM}	AC common-mode voltage on OUT0±(1)	Default setting, PRBS31, 11.88 Gbps		8		mV (rms)
RECLOCKER OUTPUT JITTER						
AJ_{CD}	Alignment jitter(1)	Measured at SDI_OUT1+ and SDI_OUT2+, OUT0± disabled PRBS10, 3G/HD/SD12G/6G/3G/HD/SD		0.1	0.14	UI
TMJ_{CD}	Timing jitter(1)	Measured at SDI_OUT1+ and SDI_OUT2+, OUT0± disabled PRBS10, 12G/6G/3G/HD/SD		0.45		UI
RECLOCKER SPECIFICATIONS						
$LOCK_{RATE}$	Reclocker lock data rates	SMPTE 12G, /1		11.88		Gbps
		SMPTE 12G, /1.001		11.868		Gbps
		SMPTE 6G, /1		5.94		Gbps
		SMPTE 6G, /1.001		5.934		Gbps
		SMPTE 3G, /1		2.97		Gbps
		SMPTE 3G, /1.001		2.967		Gbps
		SMPTE HD, /1		1.485		Gbps
		SMPTE HD, /1.001		1.4835		Gbps
		SMPTE SD, /1		270		Mbps
$BYPASS_{RATE}$	Reclocker automatically goes to bypass	MADI		125		Mbps

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BW_{PLL}	PLL bandwidth	Applied 0.2 UI input sinusoidal jitter, measure –3-dB bandwidth on input-to-output jitter transfer 11.88 Gbps		13		MHz
		5.94 Gbps		7		MHz
		2.97 Gbps		5		MHz
		1.485 Gbps		3		MHz
		270 Mbps		1		MHz
$J_{PEAKING}$	PLL jitter peaking	11.88 Gbps, 5.94 Gbps, 2.97 Gbps, 1.485 Gbps, 270 Mbps		<0.3		dB
T_{LOCK}	Lock time	SMPTE supported data rates, disable HEO/VEO monitor, CTLE in AM0 Manual Mode		5		ms
$TEMP_{LOCK}$	VCO temperature lock range	Measured with temperature ramp of 5°C per min, ramp up and down, –40°C to 85°C operating range at 11.88 Gbps		125		°C
TLAT	Reclocker latency	Measured from IN0± to SDI_OUT1+, 11.88 Gbps		1.5 UI + 175		ps
		Measured from IN0± to SDI_OUT2+, 11.88 Gbps		1.6 UI + 130		ps

6.6 Recommended SMBus Interface Timing Specifications

over recommended operating supply and temperature ranges unless otherwise specified(1)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
F_{SCL}	SMBUS SCL frequency		10		400	kHz
T_{BUF}	Bus free time between stop and start condition	See Figure 1.	1.3			µs
$T_{HD:STA}$	Hold time after (repeated) start condition.	After this period, the first clock is generated.	0.6			µs
$T_{SU:STA}$	Repeated start condition setup time	See Figure 1.	0.6			µs
$T_{SU:STO}$	Stop condition setup time	See Figure 1.	0.6			µs
$T_{HD:DAT}$	Data hold time	See Figure 1.	0			ns
$T_{SU:DAT}$	Data setup time	See Figure 1.	100			ns
T_{LOW}	Clock low period	See Figure 1.	1.3			µs
T_{HIGH}	Clock high period	See Figure 1.	0.6			µs
T_R	Clock and data rise time	See Figure 1.			300	ns
T_F	Clock and data fall time	See Figure 1.			300	ns
T_{POR}	SMBus ready time after POR	Time from minimum VDDIO to SMBus valid write or read access			50	ms

(1) These parameters support SMBus 2.0 specifications.

6.7 Serial Parallel Interface (SPI) Timing Specifications

over recommended operating supply and temperature ranges unless otherwise specified(1)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
F_{SCK}	SPI SCK frequency				20	MHz
T_{PH}	SCK pulse width high	See Figure 17 and Figure 18	40			% SCK period
T_{PL}	SCK pulse width low		40			% SCK period
T_{SU}	MOSI setup time	See Figure 17 and Figure 18	4			ns
T_{H}	MOSI hold time		4			ns
T_{SSSU}	SS setup time	See Figure 17 and Figure 18	14			ns
T_{SSH}	SS hold time		4			ns
T_{SSOF}	SS off time		1			µs
T_{ODZ}	MISO driven-to-tristate time	See Figure 17 and Figure 18		20		ns
T_{OZD}	MISO tristate-to-driven time			10		ns
T_{OD}	MISO output delay time			15		ns

(1) Typical SPI load capacitance is 2 pF.

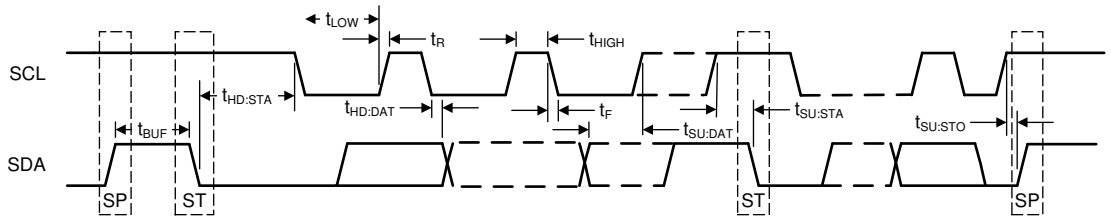


Figure 1. SMBus Timing Parameters

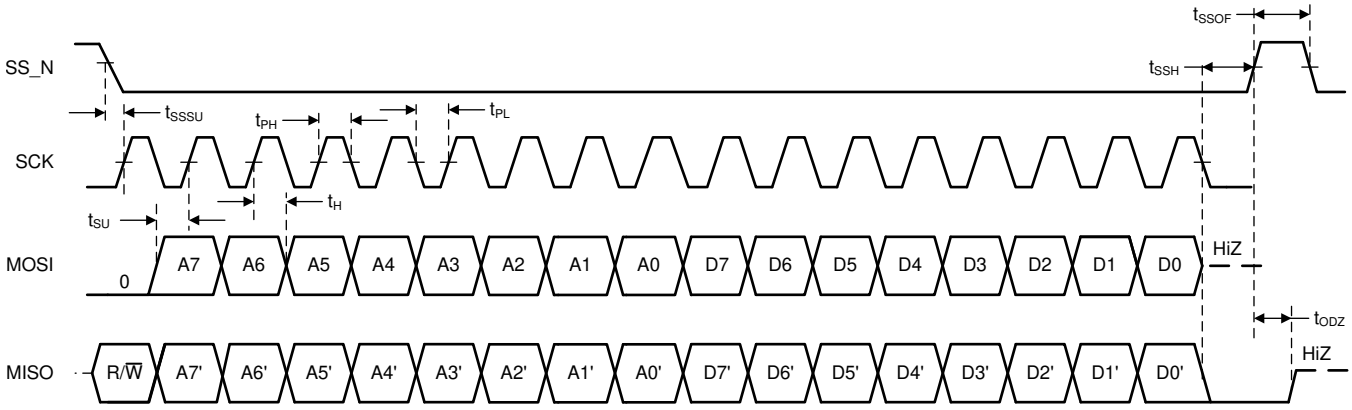


Figure 2. SPI Timing Parameters (Write Operation)

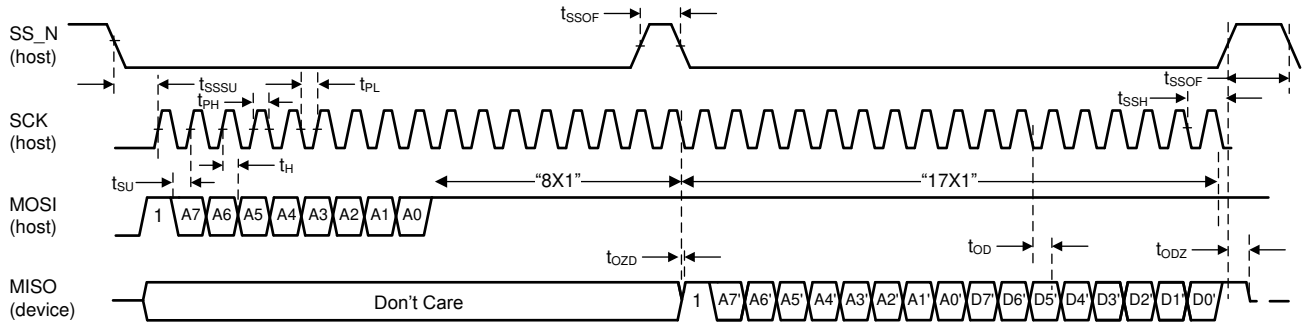


Figure 3. SPI Timing Parameters (Read Operation)

6.8 Typical Characteristics

T_A = 25°C and VIN = VDD_CDR = 2.5 V (unless otherwise noted)

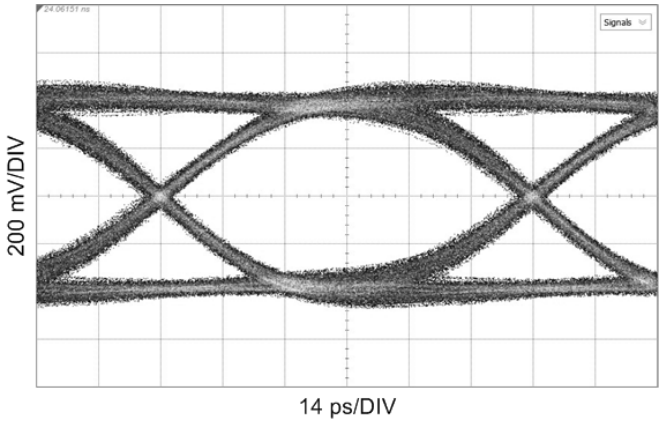


Figure 4. Output at 11.88 Gbps, Measured at SDI_OUT1+, 20-in. FR4 Before IN0±

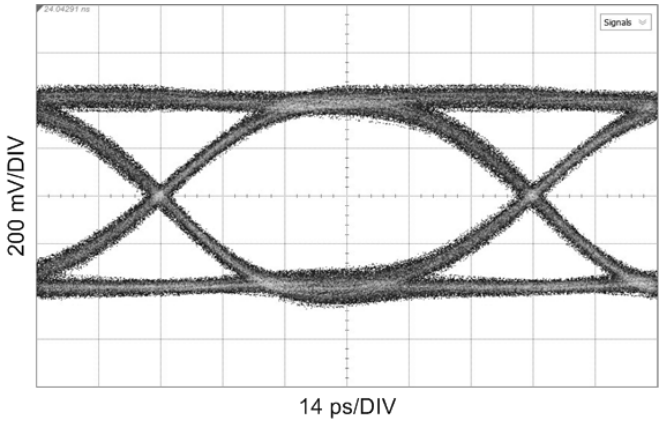


Figure 5. Output at 11.88 Gbps, Measured at SDI_OUT2+, 20-in. FR4 Before IN0±

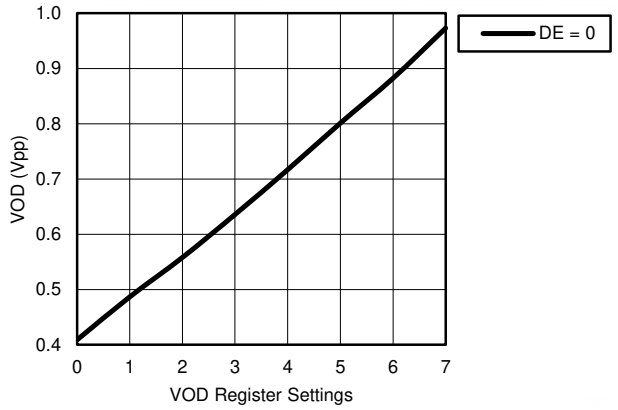


Figure 6. OUT0 VOD vs. OUT0 VOD and DE Register Settings

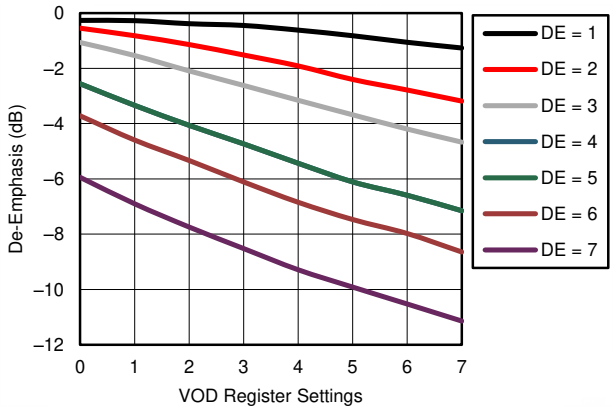
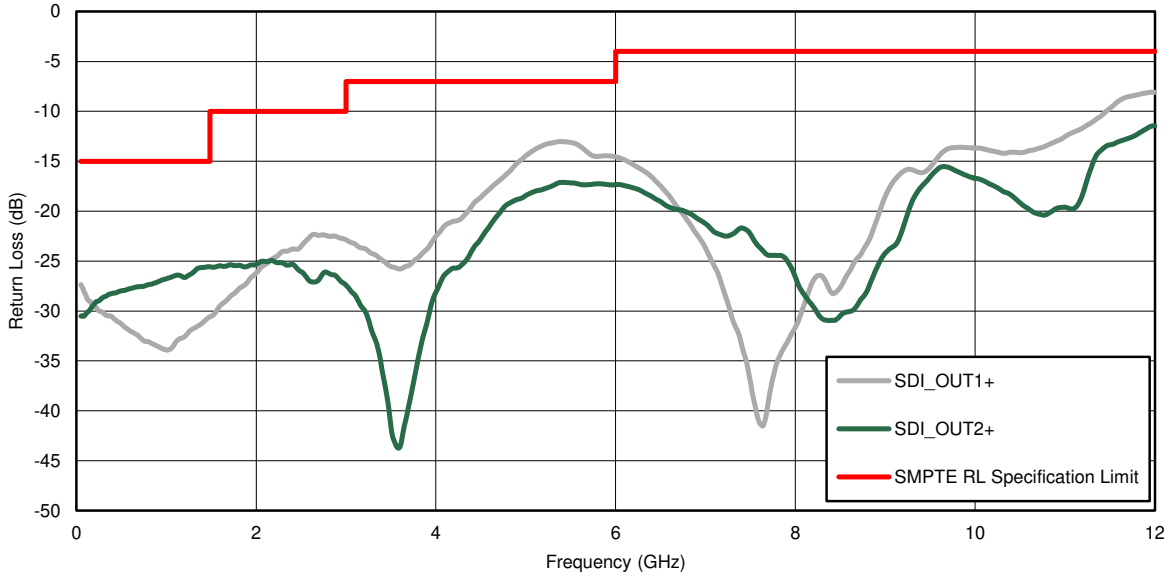


Figure 7. OUT0 De-Emphasis vs. OUT0 VOD and DE Register Settings



Measured with LMH1297EVM

Figure 8. Return Loss (RL) vs Frequency

7 Detailed Description

7.1 Overview

The LMH1228 is a 12G UHD-SDI dual output cable driver with integrated reclocker. From the host-side input at IN0±, the signal is equalized, reclocked, and routed to 75-Ω cable driver outputs at SDI_OUT1+ and SDI_OUT2+. The 100-Ω driver at OUT0± can be used as a host-side loop-back output for monitoring purposes.

7.2 Functional Block Diagram

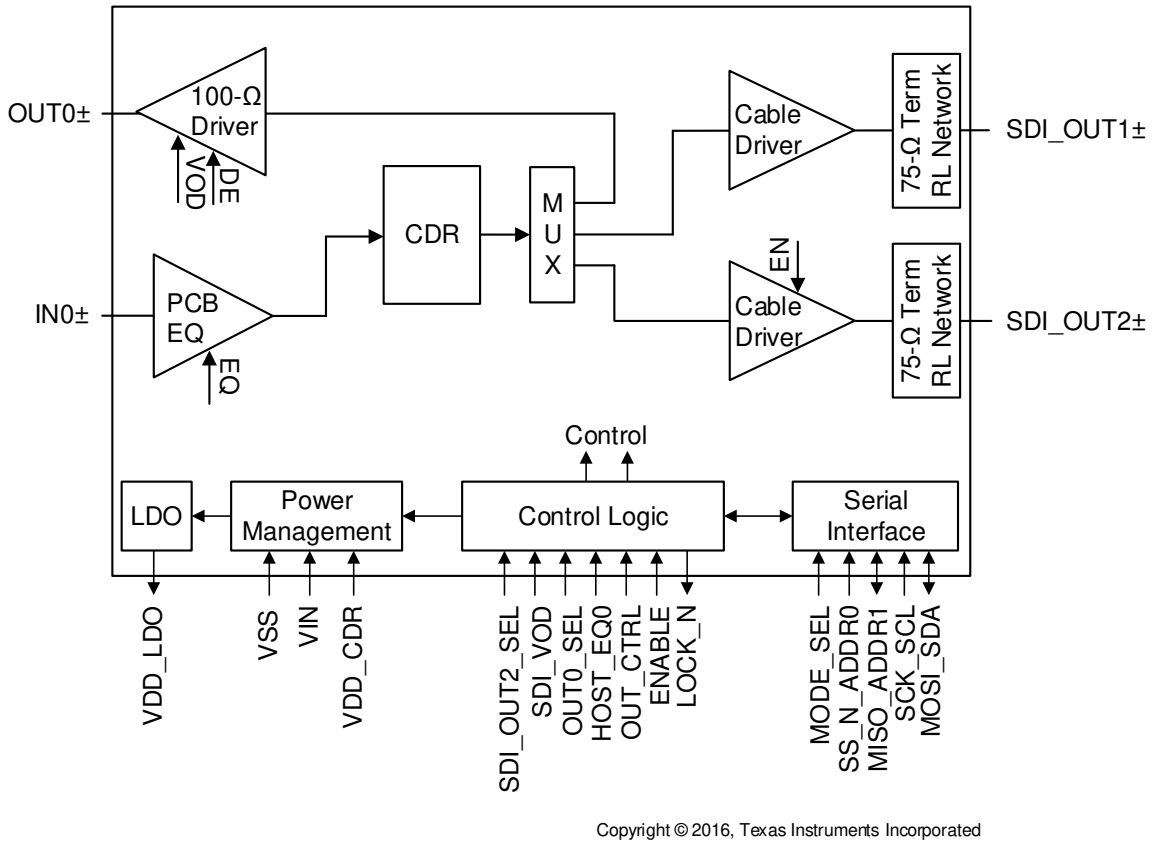


Figure 9. LMH1228 Block Diagram Overview

7.3 Feature Description

The LMH1228 data path consists of several key blocks as shown in the functional block diagram. These key blocks are:

- *4-Level Input Pins and Thresholds*
- *OUT0_SEL and SDI_OUT2_SEL Control*
- *Input Signal Detect*
- *Continuous Time Linear Equalizer (CTLE)*
- *Clock and Data (CDR) Recovery*
- *Internal Eye Opening Monitor (EOM)*
- *Output Function Control*
- *Output Driver Control*
- *Status Indicators and Interrupts*

7.3.1 4-Level Input Pins and Thresholds

The 4-level input configuration pins use a resistor divider to provide four logic states for each control pin. There is an internal 30-kΩ pullup and a 60-kΩ pulldown connected to the control pin that sets the default voltage at 2/3 × VIN. These resistors, together with the external resistor, combine to achieve the desired voltage level. By using the 1-kΩ pulldown, 20-kΩ pulldown, no connect, and 1-kΩ pullup, the optimal voltage levels for each of the four input states are achieved as shown in Table 1.

Table 1. 4-Level Control Pin Settings

LEVEL	SETTING	NOMINAL PIN VOLTAGE
H	Tie 1 kΩ to VIN	VIN
F	Float (leave pin open)	2/3 × VIN
R	Tie 20 kΩ to VSS	1/3 × VIN
L	Tie 1 kΩ to VSS	0

Typical 4-Level Input Thresholds:

- Internal Threshold between L and R = 0.2 × VIN
- Internal Threshold between R and F = 0.5 × VIN
- Internal Threshold between F and H = 0.8 × VIN

7.3.2 OUT0_SEL and SDI_OUT2_SEL Control

The OUT0_SEL and SDI_OUT2_SEL pins select the LMH1228 data-path routes. Table 2 shows all possible signal path combinations and typical use cases for each configuration.

Table 2. LMH1228 Signal Path Combinations

OUT0_SEL	SDI_OUT2_SEL	INPUT	MAIN OUTPUT	LINE SIDE SECONDARY OUTPUT	HOST SIDE LOOP-BACK OUTPUT	TYPICAL APPLICATION
H	H	IN0±	SDI_OUT1±			Single cable driver
H	L	IN0±	SDI_OUT1±	SDI_OUT2±		Dual cable drivers
L	H	IN0±	SDI_OUT1±		OUT0±	Single cable driver with host-side loop-back enabled
L	L	IN0±	SDI_OUT1±	SDI_OUT2±	OUT0±	Dual cable drivers with host-side loop-back enabled

7.3.3 Input Signal Detect

IN0 has a signal detect circuit to monitor the presence or absence of an input signal. When the input signal amplitude for the selected input exceeds the signal detect assert threshold, the LMH1228 operates in normal operation mode.

In the absence of an input signal, the LMH1228 automatically goes into Power Save Mode to conserve power dissipation. When a valid signal is detected, the LMH1228 automatically exits Power Save Mode and returns to the normal operation mode. If the ENABLE pin is pulled low, the LMH1228 is forced into Power-Down Mode. In Power Save Mode, both the signal detect circuit and the serial interface remain active. In Power-Down Mode, only the serial interface remains active.

Users can monitor the status of the signal detect through register programming. This can be done either by configuring the LOCK_N pin to output the SD_N status or by monitoring the signal detect status register.

Table 3. Input Signal Detect Modes of Operation

ENABLE	SIGNAL INPUT	OPERATING MODE
H	100-Ω signal input at IN0±	Normal operation Signal Detector at IN0± Serial interface active
H	No signal at IN0±	Power Save Mode Signal Detector at IN0± Serial interface active
L	Input signal ignored	Power-Down Mode Forced device power down Serial interface active

7.3.4 Continuous Time Linear Equalizer (CTLE)

The LMH1228 has a continuous time linear equalizer (CTLE) block for IN0. The CTLE compensates for frequency-dependent loss due to the transmission media prior to the device input. The CTLE accomplishes this by applying variable gain to the input signal, thereby boosting higher frequencies more than lower frequencies. The CTLE block extends the signal bandwidth, restores the signal amplitude, and reduces ISI caused by the transmission medium.

IN0 has an on-chip 100-Ω termination and is designed for AC coupling, requiring a 4.7-µF, AC-coupling capacitor for minimizing base-line wander. The PCB equalizer can compensate up to 20 inches of board trace at data rates up to 11.88 Gbps. There are two adapt modes for IN0: AM0 manual mode and AM1 adaptive mode. In AM0 manual mode, fixed EQ boost settings are applied through user-programmable control. In AM1 adaptive mode, state machines automatically find the optimal EQ boost from a set of 16 predetermined settings defined in Registers 0x40-0x4F.

The HOST_EQ0 pin determines the IN0 adapt mode and EQ boost level. For normal operation, HOST_EQ0 = F is recommended. HOST_EQ0 pin logic settings are shown in Table 4. These HOST_EQ0 pin settings can be overridden by register control. For more information, refer to the *LMH1228 and LMH1208 Programming Guide* (SNAU206).

Table 4. HOST_EQ0 Pin EQ Settings

HOST_EQ0 (1)	IN0± EQ BOOST	RECOMMENDED BOARD TRACE IN0± (2)
H	All Rates: AM0 Manual Mode, EQ=0x00	< 1 inch
F	**Normal Operation** 12G to 3G Rates: AM1 Adaptive Mode 1.5G, 270M Rates: AM0 Manual Mode, EQ= 0x00	0-20 inches
R	All Rates: AM0 Manual Mode, EQ=0x80	10-15 inches
L	All Rates: AM0 Manual Mode, EQ=0x90	20 inches

(1) The HOST_EQ0 pin is also used to set OUT0 VOD and de-emphasis values. See *Host-Side 100-Ω Output Driver (OUT0±)* for more information.
(2) Recommended board trace at 11.88 Gbps.

7.3.5 Clock and Data (CDR) Recovery

After the input signal passes through the CTLE, the equalized data is fed into the clock and data recovery (CDR) block. Using an internal PLL, the CDR locks to the incoming equalized data and recovers a clean internal clock to re-sample the equalized data. The LMH1228 CDR is able to tolerate high input jitter, tracking low-frequency input jitter below the PLL bandwidth while reducing high-frequency input jitter above the PLL bandwidth. The supported data rates are listed in Table 5.

Table 5. Supported Data Rates

INPUT	DATA RATE	RECLOCKER
IN0±	11.88 Gbps, 5.94 Gbps, 2.97 Gbps, 1.485 Gbps, 270 Mbps(1)	Enable
	125 Mbps	Bypass

(1) The LMH1228 supports divide-by-1.001 lock rates for 11.88 Gbps, 5.94 Gbps, 2.97 Gbps, and 1.485 Gbps.

7.3.6 Internal Eye Opening Monitor (EOM)

The LMH1228 has an on-chip eye opening monitor (EOM) that can be used to analyze, monitor, and diagnose the post-equalized waveform, just prior to the CDR reclocker. The EOM is operational for 2.97 Gbps and higher data rates.

The EOM monitors the post-equalized waveform in a time window that spans one unit interval and a configurable voltage range that spans up to ±400 mV. The time window and voltage range are divided into 64 steps, so the result of the eye capture is a 64 × 64 matrix of hits, where each point represents a specific voltage and phase offset relative to the main data sampler. The number of hits registered at each point needs to be taken in context with the total number of bits observed at that voltage and phase offset to determine the corresponding probability for that point.

The resulting 64 × 64 matrix produced by the EOM can be processed by software and visualized in a number of ways. Two common ways to visualize this data are shown in Figure 10 and Figure 11. These diagrams depict examples of eye monitor plots implemented by software. The first plot is an example using the EOM data to plot a basic eye using ASCII characters, which can be useful for diagnostic software. The second plot shows the first derivative of the EOM data, revealing the density of hits and the actual waveforms and crossings that comprise the eye.

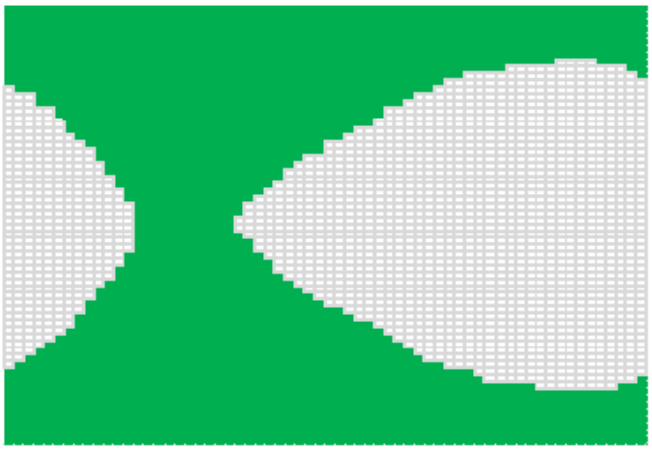


Figure 10. Internal Input Eye Monitor Plot

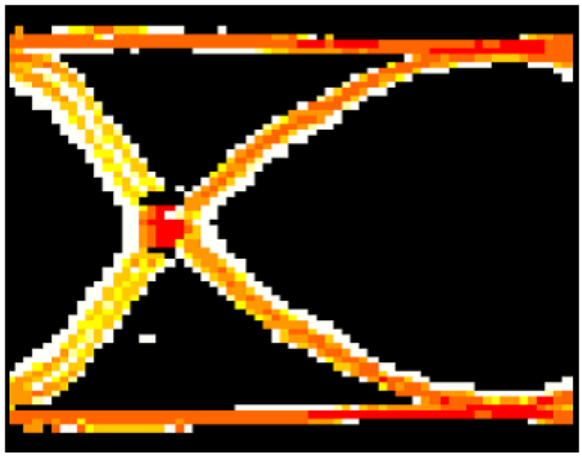


Figure 11. Internal Eye Monitor Hit Density Plot

A common measurement performed by the EOM is the horizontal and vertical eye opening. The horizontal eye opening (HEO) represents the width of the post-equalized eye at 0-V differential amplitude, measured in unit intervals or picoseconds (ps). The vertical eye opening (VEO) represents the height of the post-equalized eye, measured midway between the mean zero crossing of the eye. This position in time approximates the CDR sampling phase. HEO and VEO measurements can be read back through register control.

7.3.7 Output Function Control

The LMH1228 output function control for data routed to outputs SDI_OUT1, SDI_OUT2, and OUT0 is configured by the OUT_CTRL pin. The OUT_CTRL pin determines whether to bypass the reclocker. In normal operation (OUT_CTRL = F), the reclocker is enabled.

OUT_CTRL pin logic settings are shown in Table 6. These settings can be overridden through register control by applying the appropriate override bit values. For more information, refer to the *LMH1228 and LMH1208 Programming Guide* (SNAU206).

Table 6. OUT_CTRL Settings for Bypass Modes(1)

OUT_CTRL	IN0± PCB EQUALIZER	RECLOCKER	SUMMARY
H, F	Enable	Enable	Normal operation Input IN0 equalizer enabled Reclocker enabled
R, L	Enable	Bypass	Input IN0 equalizer enabled in AM0 manual mode. IN0 EQ settings configurable by HOST_EQ0 pin. Reclocker bypassed

(1) Regardless of OUT_CTRL pin setting, IN0 CTLE is always enabled.

7.3.8 Output Driver Control

7.3.8.1 Line-Side Output Cable Driver (SDI_OUT1+, SDI_OUT2+)

The LMH1228 has two output cable driver (CD) blocks, one for SDI_OUT1 and another for SDI_OUT2. These SDI outputs are designed to drive 75-Ω single-ended coaxial cables at data rates up to 11.88 Gbps. Both SDI_OUT1 and SDI_OUT2 feature an integrated 75-Ω termination and return loss compensation network for meeting stringent SMPTE return loss requirements (see Figure 8). The cable drivers are designed for AC coupling, requiring a 4.7-µF, AC-coupling capacitor for minimizing base-line wander due to the rare-occurring pathological bit pattern.

7.3.8.1.1 Output Amplitude (VOD)

SDI_OUT1 and SDI_OUT2 are designed for transmission across 75-Ω single-ended impedance. The nominal SDI cable driver output amplitude (VOD) is 800 mVp-p single-ended. In the presence of long output cable lengths or crosstalk, the SDI_VOD pin can be used to optimize the cable driver output with respect to the nominal amplitude. Table 7 details VOD settings that can be applied to both SDI_OUT1 and SDI_OUT2. The SDI_VOD pin can be overridden through register control. In addition, the nominal VOD amplitude can be changed by register control. For more information, refer to the *LMH1228 and LMH1208 Programming Guide* (SNAU206).

Table 7. SDI_VOD Settings for Line-Side Output Amplitude

SDI_VOD	DESCRIPTION
H	about +5% of nominal
F	800 mVp-p (nominal)
R	about +10% of nominal
L	about –5% of nominal

7.3.8.1.2 Output Pre-Emphasis

In addition to SDI cable driver VOD control, the LMH1228 can add pre-emphasis on the cable driver output to improve output signal integrity when the reclocker recovers a UHD (12G, 6G) or HD (3G, 1.5G) input data rate. By default, the LMH1228 automatically enables pre-emphasis on SDI_OUT1 and SDI_OUT2 at UHD (12G, 6G) rates, and pre-emphasis is disabled for all other data rates. When enabled, the amount of pre-emphasis applied to the cable driver outputs is determined by register control. If the reclocker is bypassed or if the user desires to disable automatic pre-emphasis, pre-emphasis can be enabled manually through register control. For more information, refer to the *LMH1228 and LMH1208 Programming Guide* (SNAU206).

7.3.8.1.3 Output Slew Rate

SMPTE specifications require different output driver rise and fall times depending on the operating data rate. To meet these requirements, the output edge rate of SDI_OUT1 and SDI_OUT2 is automatically programmed according to the signal recovered by the reclocker. Typical edge rates at the cable driver output are shown in Table 8.

Table 8. SDI_OUT1 and SDI_OUT2 Output Edge Rate

DETECTED DATA RATE	CABLE DRIVER OUTPUT EDGE RATE (TYP)
11.88 Gbps	34 ps
5.94 Gbps	36 ps
2.97 Gbps	59 ps
1.485 Gbps	60 ps
270 Mbps	550 ps

If the reclocker is bypassed, users must program the desired edge rate manually through register control. For more information, refer to the *LMH1228 and LMH1208 Programming Guide* (SNAU206).

7.3.8.1.4 Output Polarity Inversion

Polarity inversion is supported on both SDI_OUT1 and SDI_OUT2 outputs through register control.

7.3.8.2 Host-Side 100-Ω Output Driver (OUT0±)

OUT0 is a 100-Ω driver output. OUT0 serves as a host-side loop-back output. OUT0 also supports polarity inversion.

The driver offers users the capability to select higher output amplitude and de-emphasis levels for longer board trace that connects the drivers to their downstream receivers. Driver de-emphasis provides transmitter equalization to reduce the ISI caused by the board trace.

The VOD and de-emphasis levels for OUT0 are set by default to 570 mVp-p and –0.4 dB, and these values are recommended for driving 1-2 inches of board trace from OUT0± at 11.88 Gbps. These settings can be changed through register control if desired. When these parameters are controlled by registers, the VOD and de-emphasis levels can be programmed independently. For more information, refer to the *LMH1228 and LMH1208 Programming Guide* (SNAU206).

7.3.9 Status Indicators and Interrupts

The LOCK_N pin is a 3.3-V tolerant, active-low, open-drain output. An external resistor to the logic supply is required. The LOCK_N pin can be configured to indicate reclocker lock, input signal detect, or an interrupt event.

7.3.9.1 LOCK_N (Lock Indicator)

By default, LOCK_N is the reclocker lock indicator, and this pin asserts low when the LMH1228 achieves lock to a valid SMPTE data rate. The LOCK_N pin functionality can also be configured through register control to indicate SD_N (signal detect) or INT_N (interrupt) events. For more information about how to reconfigure the LOCK_N pin functionality, refer to the *LMH1228 and LMH1208 Programming Guide* (SNAU206).

7.3.9.2 SD_N (Signal Detect)

The LOCK_N pin can be reconfigured through register control to indicate a SD_N (signal detect) event. When configured as a SD_N output, the pin asserts low at the end of adaptation after a valid signal is detected by the IN0 signal detect circuit. For more information about how to configure the LOCK_N pin for SD_N functionality, refer to the *LMH1228 and LMH1208 Programming Guide* (SNAU206).

7.3.9.3 INT_N (Interrupt)

The LOCK_N pin can be configured to indicate an INT_N (interrupt) event. When configured as an INT_N output, the pin asserts low when an interrupt occurs, according to the programmed interrupt masks. Five separate masks can be programmed through register control as interrupt sources:

- If there is a loss of signal (LOS) event on IN0 (2 separate masks).
- If HEO or VEO falls below a certain threshold after CDR is locked (1 mask).
- If a CDR Lock event has occurred (2 separate masks).

INT_N is a sticky bit, meaning that it will flag after an interrupt occurs and will not clear until read-back. Once the Interrupt Status Register is read, the INT_N pin will assert high again. For more information about how to configure the LOCK_N pin for INT_N functionality, refer to the *LMH1228 and LMH1208 Programming Guide* (SNAU206).

7.4 Device Functional Modes

The LMH1228 operates in one of two modes: System Management Bus (SMBus) or Serial Peripheral Interface (SPI) mode. To determine the mode of operation, the proper setting must be applied to the MODE_SEL pin at power up, as detailed in Table 9.

Table 9. MODE_SEL Pin Settings

LEVEL	DESCRIPTION
H	Reserved for factory testing – do not use
F	Selects SPI Interface for register access
R	Reserved for factory testing – do not use
L	Selects SMBus Interface for register access

7.4.1 System Management Bus (SMBus) Mode

The SMBus interface can also be used to control the device. If MODE_SEL = Low (1 kΩ to VSS), Pins 13 and 29 are configured as SDA and SCL. Pins 11 and 28 are address straps ADDR0 and ADDR1 during power up. The maximum operating speed supported on the SMBUS pins is 400 kHz.

Table 10. SMBus Device Slave Addresses(1)

ADDR0 (LEVEL)	ADDR1 (LEVEL)	7-BIT SLAVE ADDRESS [HEX]	8-BIT WRITE COMMAND [HEX]
L	L	2D	5A
L	R	2E	5C
L	F	2F	5E
L	H	30	60
R	L	31	62
R	R	32	64
R	F	33	66
R	H	34	68
F	L	35	6A
F	R	36	6C
F	F	37	6E
F	H	38	70
H	L	39	72
H	R	3A	74
H	F	3B	76
H	H	3C	78

(1) The 8-bit write command consists of the 7-bit slave address (Bits 7:1) with 0 appended to the LSB to indicate an SMBus write. For example, if the 7-bit slave address is 0x2D (010 1101'b), the 8-bit write command is 0x5A (0101 1010'b).

7.4.1.1 SMBus Read and Write Transaction

SMBus is a two-wire serial interface through which various system component chips can communicate with the master. Slave devices are identified by having a unique device address. The two-wire serial interface consists of SCL and SDA signals. SCL is a clock output from the master to all of the slave devices on the bus. SDA is a bidirectional data signal between the master and slave devices. The LMH1228 SMBus SCL and SDA signals are open-drain and require external pullup resistors.

Start and Stop:

The master generates Start and Stop patterns at the beginning and end of each transaction.

- Start: High-to-low transition (falling edge) of SDA while SCL is high.
- Start: High-to-low transition (falling edge) of SDA while SCL is high.

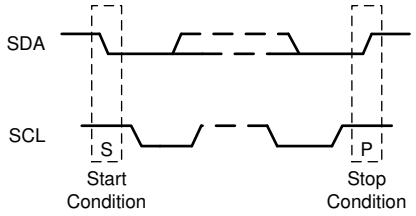


Figure 12. Start and Stop Conditions

The master generates nine clock pulses for each byte transfer. The 9th clock pulse constitutes the ACK cycle. The transmitter releases SDA to allow the receiver to send the ACK signal. An ACK is recorded when the device pulls SDA low, while a NACK is recorded if the line remains high.

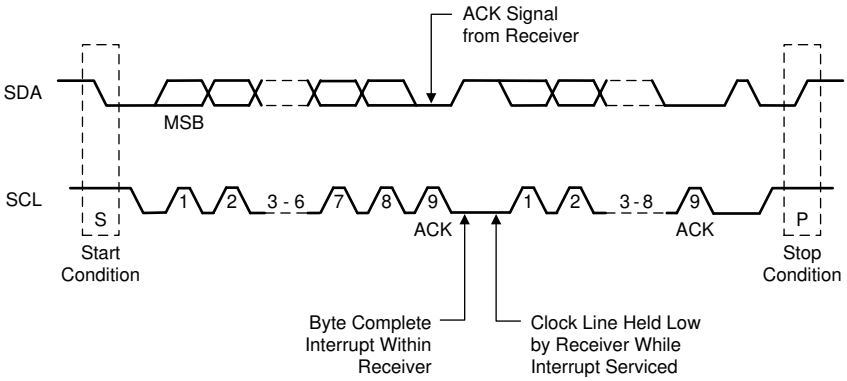


Figure 13. Acknowledge (ACK)

7.4.1.1.1 SMBus Write Operation Format

Writing data to a slave device consists of three parts, as illustrated in Figure 14:

1. The master begins with a start condition followed by the slave device address with the R/$\overline{W}$ bit set to 0'b.
2. After an ACK from the slave device, the 8-bit register word address is written.
3. After an ACK from the slave device, the 8-bit data is written, followed by a stop condition.

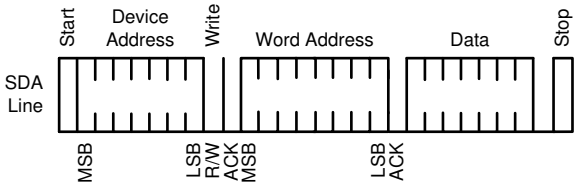


Figure 14. SMBus Write Operation

7.4.1.1.2 SMBus Read Operation Format

SMBus read operation consists of four parts, as illustrated in Figure 15:

1. The master begins with a start condition, followed by the slave device address with the R/$\overline{W}$ bit set to 0'b.
2. After an ACK from the slave device, the 8-bit register word address is written.
3. After an ACK from the slave device, the master initiates a restart condition, followed by the slave address with the R/$\overline{W}$ bit set to 1'b.
4. After an ACK from the slave device, the 8-bit data is read-back. The last ACK is high if there are no more bytes to read, and the last read is followed by a stop condition.

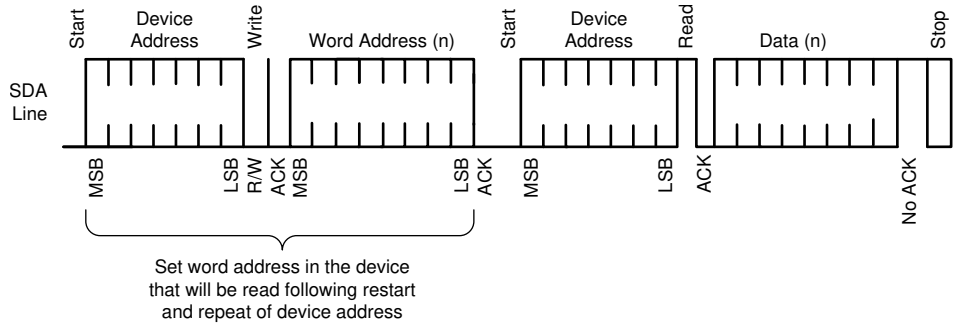


Figure 15. SMBus Read Operation

7.4.2 Serial Peripheral Interface (SPI) Mode

If MODE_SEL = F or H, the LMH1228 is in SPI mode. In SPI mode, the following pins are used for SPI bus communication:

- MOSI (Pin 13): Master Output Slave Input
- MISO (Pin 28): Master Input Slave Output
- SS_N (Pin 11): Slave Select (Active Low)
- SCK (Pin 29): Serial Clock (Input to the LMH1228 Slave Device)

7.4.2.1 SPI Read and Write Transactions

Each SPI transaction to a single device is 17 bits long and is framed by SS_N when asserted low. The MOSI input is ignored, and the MISO output is floated whenever SS_N is deasserted (high).

The bits are shifted in left-to-right. The first bit is R/$\overline{W}$, which is 1'b for *read* and 0'b for *write*. Bits A7-A0 are the 8-bit register address, and bits D7-D0 are the 8-bit read or write data. The previous SPI command, address, and data are shifted out on MISO as the current command, address, and data are shifted in on MOSI. In all SPI transactions, the MISO output signal is enabled asynchronously when SS_N asserts low. The contents of a single MOSI or MISO transaction frame are shown in Figure 16.

Figure 16. 17-Bit Single SPI Transaction Frame

R/W	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

7.4.2.2 SPI Write Transaction Format

For SPI writes, the R/W bit is 0'b. SPI write transactions are 17 bits per device, and the command is executed on the rising edge of SS_N. The SPI transaction always starts on the rising edge of the clock.

The signal timing for a SPI Write transaction is shown in Figure 17. The *prime* values on MISO (for example, A7') reflect the contents of the shift register from the previous SPI transaction and are listed as don't-care for the current transaction.

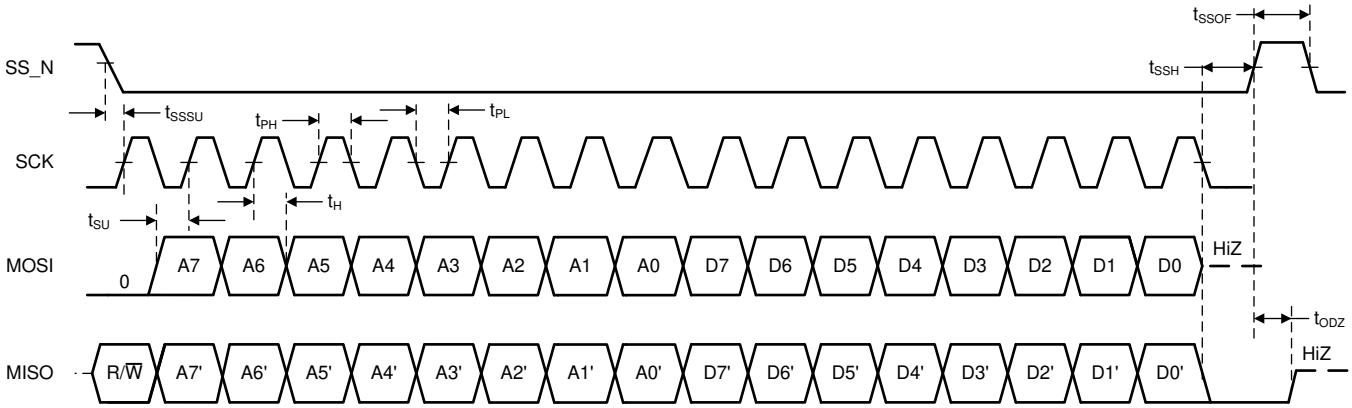


Figure 17. Signal Timing for a SPI Write Transaction

7.4.2.3 SPI Read Transaction Format

A SPI read transaction is 34 bits per device and consists of two 17-bit frames. The first 17-bit read transaction frame shifts in the address to be read, followed by a dummy transaction second frame to shift out 17-bit read data. The R/W bit is 1'b for the read transaction, as shown in Figure 18.

The first 17 bits from the read transaction specifies 1-bit of R/W and 8-bits of address A7-A0 in the first 8 bits. The eight 1's following the address are ignored. The second dummy transaction acts like a read operation on address 0xFF and needs to be ignored. However, the transaction is necessary to shift out the read data D7-D0 in the last 8 bits of the MISO output. As with the SPI Write, the *prime* values on MISO during the first 16 clocks are listed as don't care for this portion of the transaction. The values shifted out on MISO during the last 17 clocks reflect the read address and 8-bit read data for the current transaction.

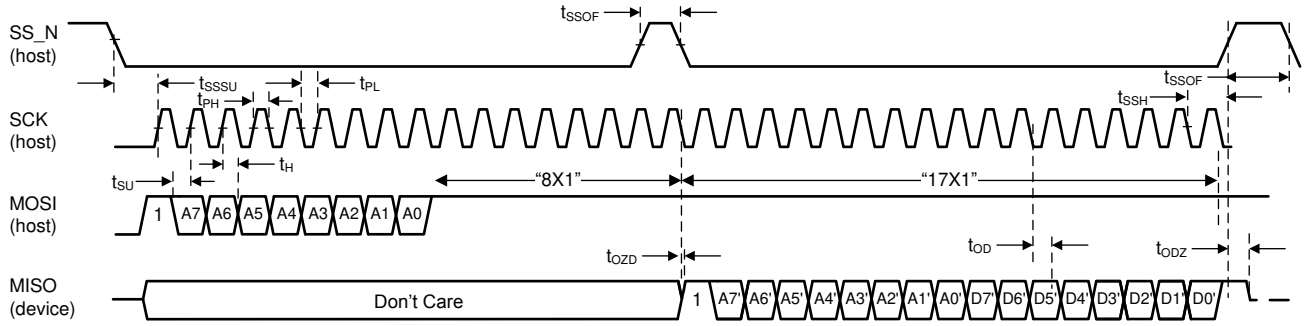


Figure 18. Signal Timing for a SPI Read Transaction

7.4.2.4 SPI Daisy Chain

The LMH1228 supports SPI daisy-chaining among multiple devices, as shown in Figure 19.

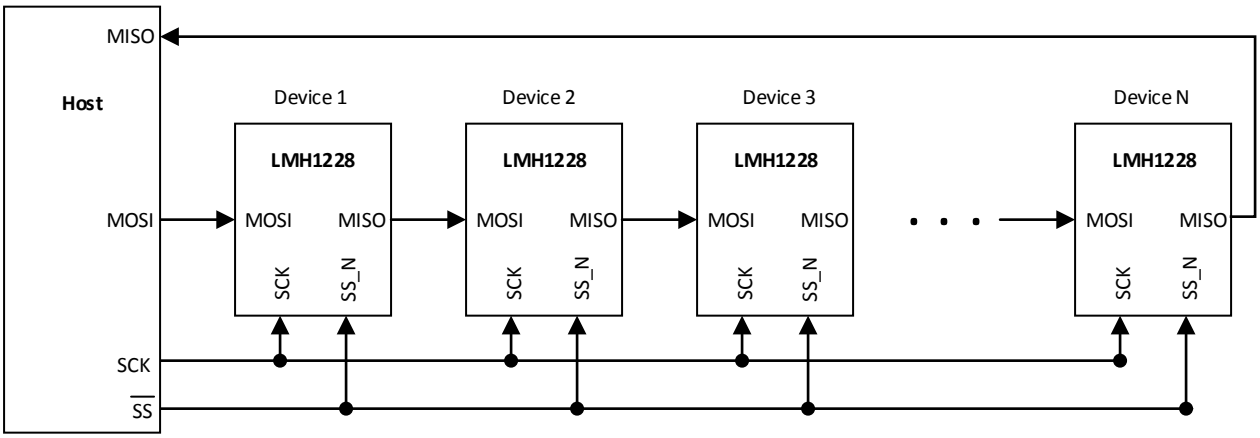


Figure 19. Daisy-Chain Configuration

Each LMH1228 device is directly connected to the SCK and SS_N pins of the host. The first LMH1228 device in the chain is connected to the host's MOSI pin, and the last device in the chain is connected to the host's MISO pin. The MOSI pin of each intermediate LMH1228 device in the chain is connected to the MISO pin of the previous LMH1228 device, thereby creating a serial shift register. In a daisy-chain configuration of N × LMH1228 devices, the host conceptually sees a shift register of length 17 × N for a basic SPI transaction, during which SS_N is asserted low for 17 × N clock cycles.

7.5 Register Maps

The LMH1228 register map is divided into three register pages. These register pages are used to control different aspects of the LMH1228 functionality. A brief summary of the pages is shown below:

1. **Share Register Page:** This page corresponds to global parameters, such as LMH1228 device ID and LOCK_N status configuration. This is the default page at start-up. Access this page by setting Reg 0xFF[2:0] = 000'b.
2. **CTLE/CDR Register Page:** This page corresponds to IN0 PCB CTLE, output mux settings, CDR settings, and output interrupt overrides. Access this page by setting Reg 0xFF[2:0] = 100'b.
3. **Driver Register Page:** This page corresponds to OUT0, SDI_OUT1, and SDI_OUT2 driver output settings. Access this page by setting Reg 0xFF[2:0] = 101'b.

For the complete register map, typical device configurations, and proper register reset sequencing, refer to the *LMH1228 and LMH1208 Programming Guide* (SNAU206).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 SMPTE Requirements and Specifications

SMPTE specifies several key requirements for the Serial Digital Interface to transport digital video over coaxial cables. Such requirements include return loss, AC coupling, and data rate dependency with rise and fall times.

1. **Return Loss:** This specification details how closely the port resembles 75-Ω impedance across a specified frequency band. The LMH1228 features a built-in 75-Ω return-loss network on SDI_OUT1 and SDI_OUT2 to minimize parasitics and improve overall signal integrity.
2. **AC Coupling:** AC-coupling capacitors are required for transporting uncompressed serial data streams with heavy low-frequency content. The use of 4.7-µF, AC-coupling capacitors is recommended to avoid low-frequency DC wander.
3. **Rise/Fall Time:** Output 75-Ω signals are required to meet certain rise and fall timing depending on the data rate. This improves the eye opening observed for the receiving device. The LMH1228 SDI_OUT1 and SDI_OUT2 cable drivers feature automatic edge rate adjustment to meet SMPTE rise and fall time requirements.

TI recommends placing the LMH1228 as close as possible to the 75-Ω BNC ports to meet SMPTE specifications.

8.1.2 Low-Power Optimization

The LMH1228 IN0 CTLE operates in either AM1 Adaptive Mode or AM0 Manual Mode. When operating in AM1, the LMH1228 uses HEO/VEO Lock Monitoring as a key parameter to achieve lock. HEO/VEO Lock Monitoring determines the CTLE boost setting that produces the best horizontal and vertical eye opening after the CTLE. Once AM1 adaptation is complete and the LMH1228 asserts CDR lock at the optimal IN0 CTLE setting, HEO/VEO Lock Monitoring is no longer required to maintain lock. Therefore, HEO/VEO Lock Monitoring can be disabled by setting CTLE/CDR Reg 0x3E[7] = 0'b **after** lock is declared. Disabling HEO/VEO Lock Monitoring optimizes power dissipation, reducing the overall power by approximately 25 mW.

When operating in AM0, the LMH1228 does not use HEO/VEO Lock Monitoring, because the IN0 CTLE setting is set manually by the user. In AM0, HEO/VEO Lock Monitoring can be disabled at any time.

8.1.3 Optimized Loop Bandwidth Settings for Arria 10 FPGA Applications

The LMH1228 default loop bandwidth setting is optimized for a wide variety of applications. For applications using the Intel Arria 10 FPGA, further optimization of the loop bandwidth may be required. Refer to the *LMH1228 and LMH1208 Programming Guide* (SNAU206) for detailed register settings when using the LMH1228 with an Arria 10 FPGA.

8.2 Typical Applications

The LMH1228 is a dual cable driver with integrated reclocker that supports SDI data rates up to 11.88 Gbps. Figure 20 shows a typical application circuit for the LMH1228.

Specific examples of typical applications for the LMH1228 as a dual cable driver and distribution amplifier are detailed in the following subsections.

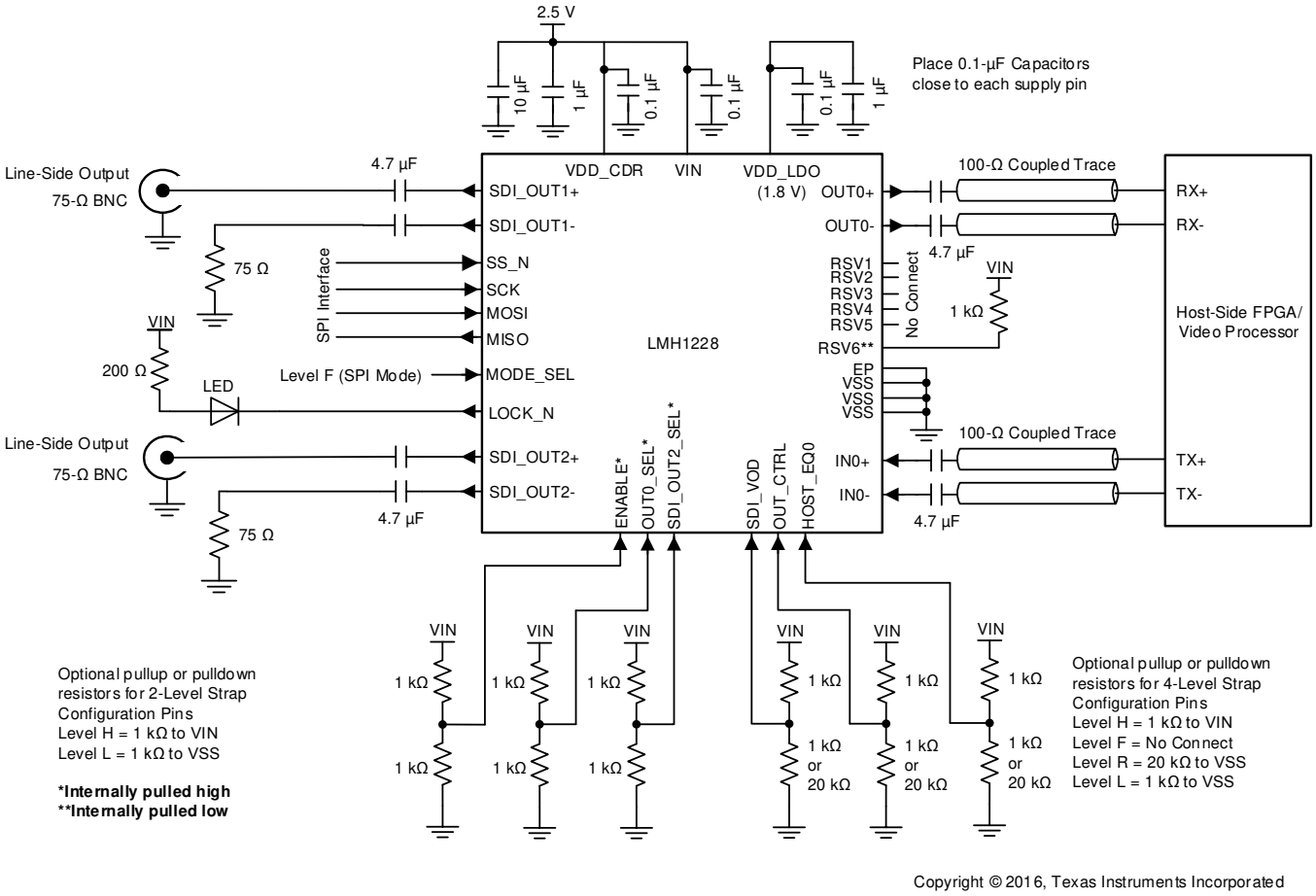


Figure 20. LMH1228 Typical Application Circuit

Typical Applications (continued)

8.2.1 Dual Cable Driver

The LMH1228 can be configured as a dual cable driver to route the same SDI output signal to multiple receivers. In this configuration, the LMH1228 adaptively equalizes 100-Ω SDI input data at IN0 and uses the dual cable drivers at SDI_OUT1 and SDI_OUT2 to drive out the SDI signal.

Figure 21 shows a typical application of an LMH1228 as a dual cable driver output. In this example, the LMH1219 Cable EQ with Integrated Reclocker provides an SDI input to the SDI FPGA. The FPGA then sends post-processed SDI data to the IN0 of the LMH1228, which drives the data on cable driver outputs SDI_OUT1 and SDI_OUT2.

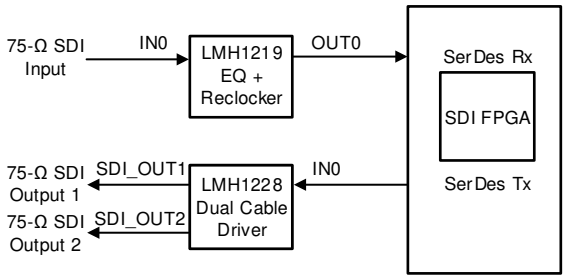


Figure 21. LMH1228 Dual Cable Driver Application

8.2.1.1 Design Requirements

For general LMH1228 design requirements, reference the guidelines in Table 11.

For dual cable driver application-specific requirements, reference the guidelines in Table 12.

Table 11. LMH1228 General Design Requirements

DESIGN PARAMETER	REQUIREMENTS
SDI_OUT1+, SDI_OUT2+ AC-coupling capacitors	4.7-µF capacitors recommended
SDI_OUT1–, SDI_OUT2– AC-coupling capacitors	4.7-µF capacitors recommended, AC terminated with 75 Ω to VSS.
IN0± and OUT0± AC-coupling capacitors	4.7-µF capacitors recommended
Input and Output Terminations	Input and output terminations provided internally. Do **not** add external terminations.
DC power supply decoupling capacitors	10-µF and 1-µF bulk capacitors; place close to each device. 0.1-µF capacitor; place close to each supply pin.
VDD_LDO decoupling capacitors	1-µF and 0.1-µF capacitors; place as close as possible to the device VDD_LDO pin.
MODE_SEL Pin	SPI: Leave MODE_SEL unconnected (Level F) SMBus: Connect 1 kΩ to VSS (Level L)
Input Reclocked Data Rate	11.88 Gbps, 5.94 Gbps, 2.97 Gbps, 1.485 Gbps, or Divide-by-1.001 sub-rates and 270 Mbps. For all other input data rates, the reclocker is automatically bypassed.

Table 12. LMH1228 Dual Cable Driver Requirements

DESIGN PARAMETER	REQUIREMENTS
OUT0_SEL Pin	1 kΩ to VIN (Level H) to disable the OUT0 loop-back output
SDI_OUT2_SEL Pin	1 kΩ to VSS (Level L) to enable SDI_OUT2 as secondary cable output

8.2.1.2 Detailed Design Procedure

The design procedure for dual cable driver applications is as follows:

1. Select a power supply that meets the DC and AC requirements in *Recommended Operating Conditions*.
2. Choose a small 0402 surface mount ceramic capacitor for AC-coupling capacitors to maintain characteristic impedance.
3. Choose a high-quality, 75-Ω BNC connector that is capable of supporting 11.88-Gbps applications. Consult a BNC supplier regarding insertion loss, impedance specifications, and recommended footprint for meeting SMPTE return loss.
4. Follow detailed high-speed layout recommendations provided in *Layout Guidelines* to ensure optimal signal quality when interconnecting 75-Ω and 100-Ω signals to the LMH1228.
5. Determine whether SPI or SMBus communication is necessary. If the LMH1228 must be programmed with settings other than what is offered by pin control, users must use SPI or SMBus Mode for additional programming.
6. Configure OUT0_SEL and SDI_OUT2_SEL pins according to the desired default use case.
7. Tune the SDI_VOD output amplitude control pin for optimal signal quality depending on the cable length attached at SDI_OUT1+ and SDI_OUT2+. Use register control for more tuning options if necessary.

8.2.1.3 Application Curves

The LMH1228 performance on SDI_OUT1+ and SDI_OUT2+ was measured with the test setups shown in Figure 22 and Figure 23.

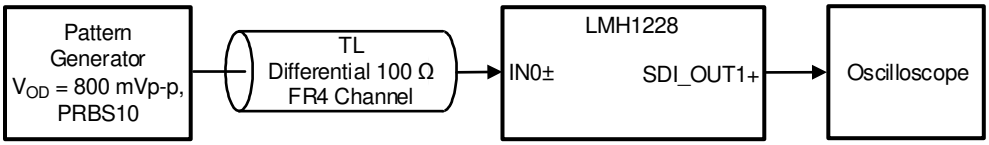


Figure 22. Test Setup for LMH1228 to SDI_OUT1+

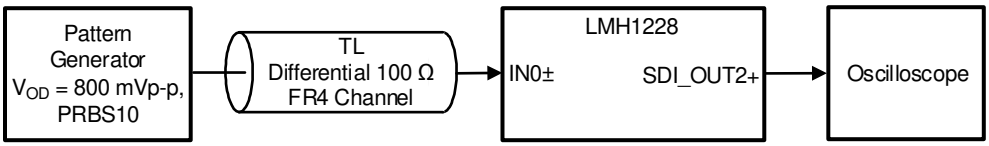
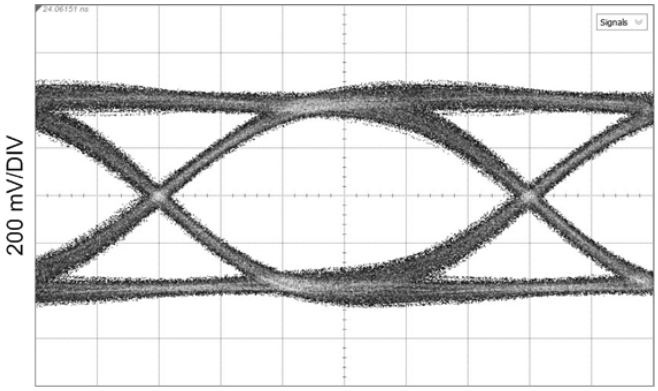


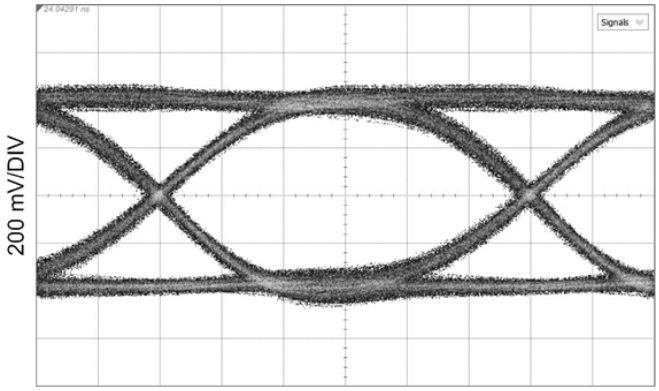
Figure 23. Test Setup for LMH1228 to SDI_OUT2+

The eye diagrams in this subsection show how the LMH1228 improves overall signal integrity in the data path for 100-Ω differential FR4 PCB trace at IN0±.



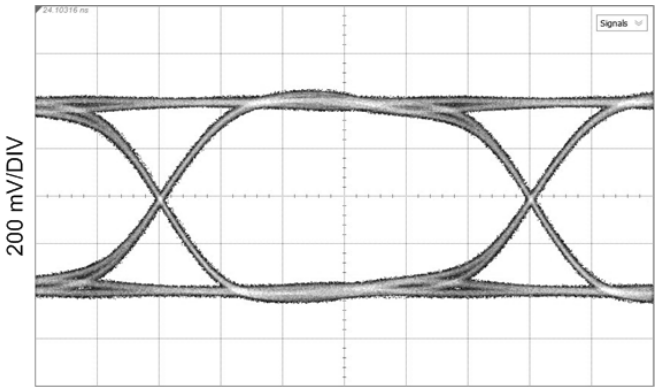
Measured at SDI_OUT1+
HOST_EQ0 = F, SDI_OUT2_SEL = L, OUT_CTRL = F

Figure 24. 11.88 Gbps, TL = 20" FR4, Reclocked



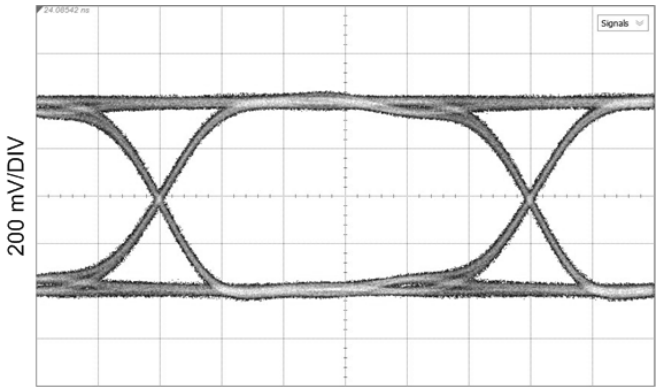
Measured at SDI_OUT2+
HOST_EQ0 = F, SDI_OUT2_SEL = L, OUT_CTRL = F

Figure 25. 11.88 Gbps, TL = 20" FR4, Reclocked



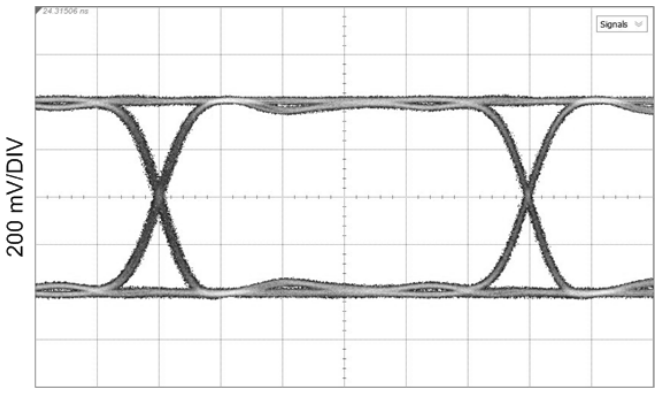
Measured at SDI_OUT1+
HOST_EQ0 = F, SDI_OUT2_SEL = L, OUT_CTRL = F

Figure 26. 5.94 Gbps, TL = 20" FR4, Reclocked



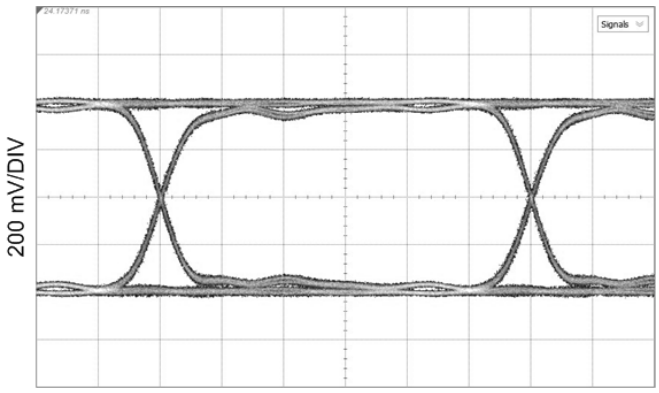
Measured at SDI_OUT2+
HOST_EQ0 = F, SDI_OUT2_SEL = L, OUT_CTRL = F

Figure 27. 5.94 Gbps, TL = 20" FR4, Reclocked



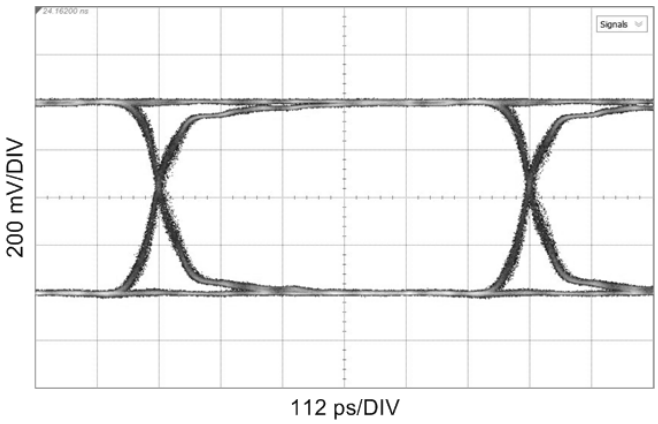
Measured at SDI_OUT1+
HOST_EQ0 = F, SDI_OUT2_SEL = L, OUT_CTRL = F

Figure 28. 2.97 Gbps, TL = 20" FR4, Reclocked



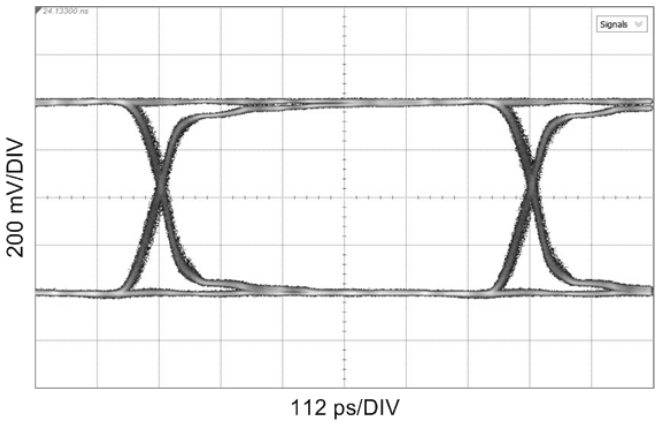
Measured at SDI_OUT2+
HOST_EQ0 = F, SDI_OUT2_SEL = L, OUT_CTRL = F

Figure 29. 2.97 Gbps, TL = 20" FR4, Reclocked



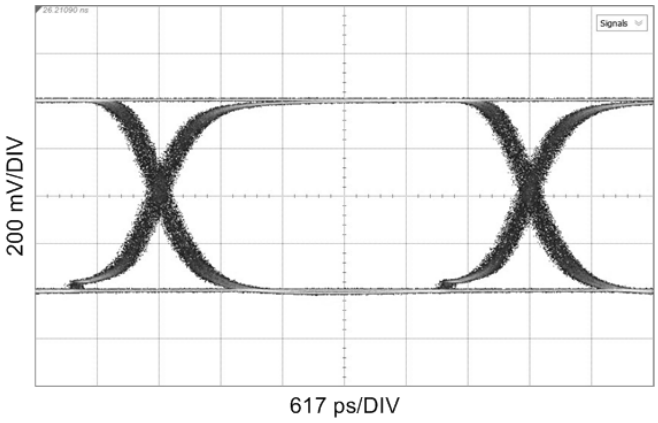
Measured at SDI_OUT1+
HOST_EQ0 = F, SDI_OUT2_SEL = L, OUT_CTRL = F

Figure 30. 1.485 Gbps, TL = 20" FR4, Reclocked



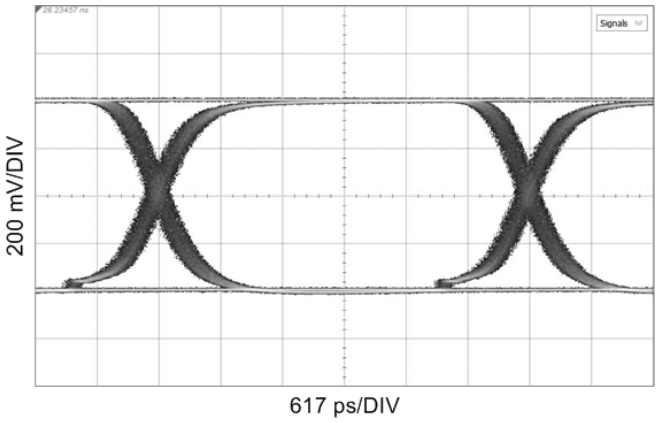
Measured at SDI_OUT2+
HOST_EQ0 = F, SDI_OUT2_SEL = L, OUT_CTRL = F

Figure 31. 1.485 Gbps, TL = 20" FR4, Reclocked



Measured at SDI_OUT1+
HOST_EQ0 = F, SDI_OUT2_SEL = L, OUT_CTRL = F

Figure 32. 270 Mbps, TL = 20" FR4, Reclocked



Measured at SDI_OUT2+
HOST_EQ0 = F, SDI_OUT2_SEL = L, OUT_CTRL = F

Figure 33. 270 Mbps, TL = 20" FR4, Reclocked

8.2.2 Distribution Amplifier

The LMH1228 can be configured as a distribution amplifier to distribute the same SDI input signal to multiple cable driver outputs. In this configuration, the LMH1228 uses the dual cable drivers at SDI_OUT1 and SDI_OUT2 to drive out the SDI signal seen at IN0. Meanwhile, the loop-back output on OUT0 is daisy-chained as a duplicate input to IN0 of the next LMH1228.

Figure 34 shows a typical application where four LMH1228s are used in combination with an LMH1219 Cable EQ with Integrated Reclocker to form a 1:8 distribution amplifier network.

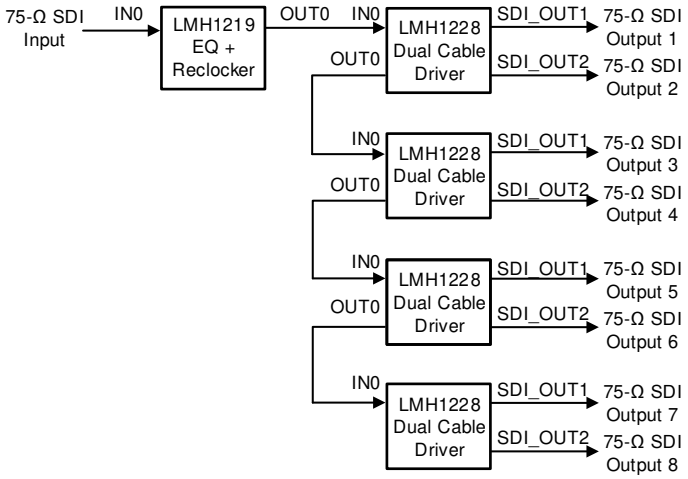


Figure 34. LMH1228 Distribution Amplifier Application

8.2.2.1 Design Requirements

See Table 11 in *Dual Cable Driver Design Requirements* for general LMH1228 design requirements.

For distribution amplifier application-specific requirements, reference the guidelines in Table 13.

Table 13. LMH1228 Distribution Amplifier Requirements

DESIGN PARAMETER	REQUIREMENTS
OUT0_SEL Pin	1 kΩ to VSS (Level L) to enable OUT0 as a loop-back output to the next LMH1228 IN0 input
SDI_OUT2_SEL Pin	1 kΩ to VSS (Level L) to enable SDI_OUT2 as secondary cable output

8.2.2.2 Detailed Design Procedure

See *Dual Cable Driver Detailed Design Procedure* and follow Steps 1 through 5. Refer to the additional steps below for distribution amplifier applications.

1. Configure OUT0_SEL and SDI_OUT2_SEL pins according to the desired default use case.
2. Tune the output VOD and de-emphasis level for the 100-Ω driver prior to each LMH1228 IN0±. In the distribution amplifier example shown in Figure 34, this step applies to the LMH1219 OUT0± driver and all LMH1228 OUT0± drivers that are daisy-chained to a subsequent LMH1228 IN0±. If OUT0± is located within 1-2 inches of IN0±, then use a lower VOD setting and no de-emphasis. If the OUT0± is located many inches away from IN0±, some VOD gain and de-emphasis may be required at OUT0± for the IN0 CTLE to equalize optimally. Use register control for more tuning options if necessary.
3. Tune the SDI_VOD output amplitude control pin for optimal signal quality depending on the cable length attached at SDI_OUT1+ and SDI_OUT2+ for each LMH1228. Use register control for more tuning options if necessary.

8.2.2.3 Application Curves

The LMH1228 performance on OUT0± was measured with the test setup shown in Figure 22.

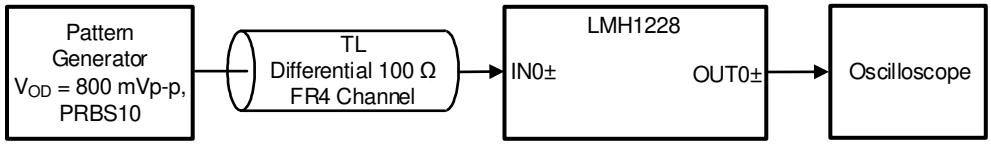
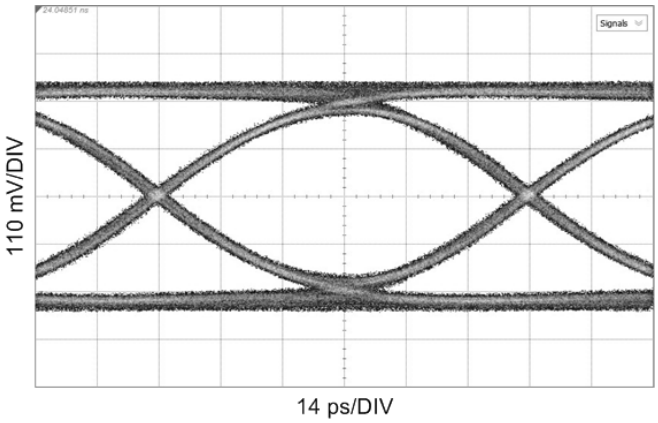


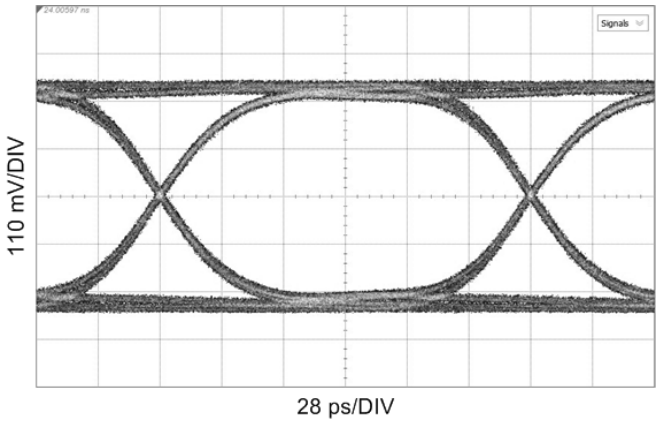
Figure 35. Test Setup for LMH1228 to OUT0±

The eye diagrams in this subsection show how the LMH1228 improves overall signal integrity in the data path for 100-Ω differential FR4 PCB trace at IN0±.



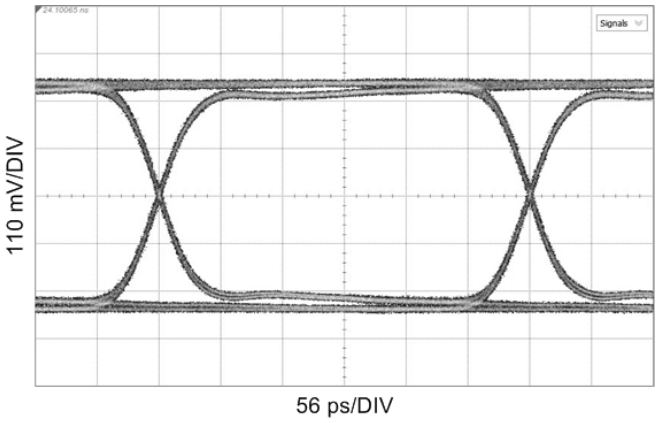
Measured at OUT0±
HOST_EQ0 = F, SDI_OUT2_SEL = L, OUT_CTRL = F

Figure 36. 11.88 Gbps, TL = 20" FR4, Reclocked



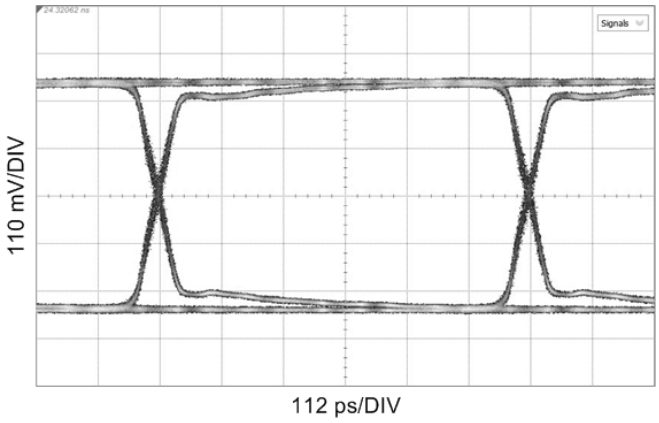
Measured at OUT0±
HOST_EQ0 = F, SDI_OUT2_SEL = L, OUT_CTRL = F

Figure 37. 5.94 Gbps, TL = 20" FR4, Reclocked



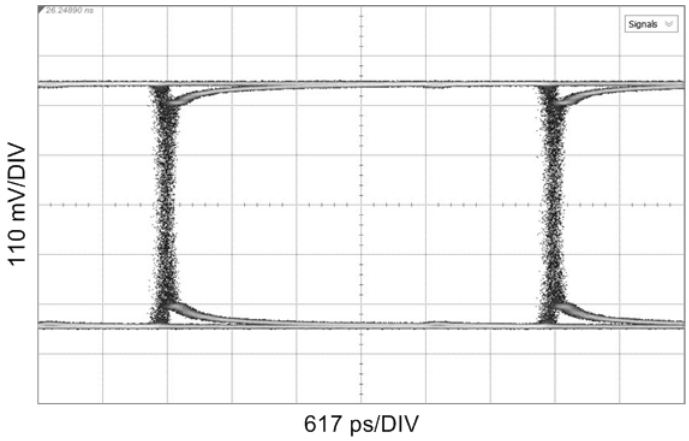
Measured at OUT0±
HOST_EQ0 = F, SDI_OUT2_SEL = L, OUT_CTRL = F

Figure 38. 2.97 Gbps, TL = 20" FR4, Reclocked



Measured at OUT0±
HOST_EQ0 = F, SDI_OUT2_SEL = L, OUT_CTRL = F

Figure 39. 1.485 Gbps, TL = 20" FR4, Reclocked



Measured at OUT0±
HOST_EQ0 = F, SDI_OUT2_SEL = L, OUT_CTRL = F

Figure 40. 270 Mbps, TL = 20" FR4, Reclocked

9 Power Supply Recommendations

The LMH1228 requires decoupling capacitors to ensure a stable power supply. For power supply decoupling, 0.1-μF surface-mount ceramic capacitors must be placed close to each VDD_CDR, VDD_LDO, and VIN supply pin to VSS. Larger bulk capacitors (for example, 10 μF and 1 μF) are recommended for VDD_CDR and VIN.

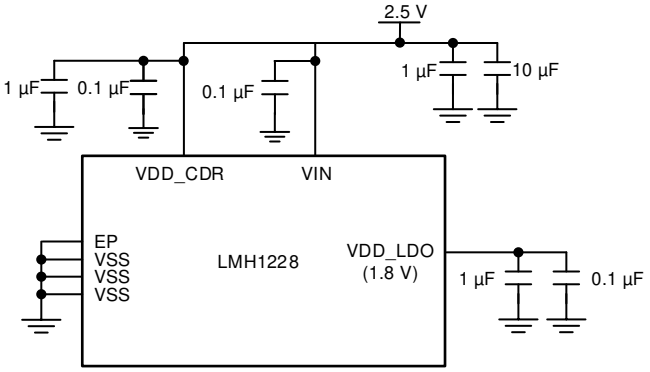


Figure 41. Recommended Power Supply Decoupling

Good supply bypassing requires low inductance capacitors. This can be achieved through an array of multiple small body size surface-mount bypass capacitors to keep low supply impedance. Better results can be achieved through the use of a buried capacitor formed by a VDD and VSS plane separated by 2 to 4 mil dielectric in a printed-circuit board.

10 Layout

10.1 Layout Guidelines

The following guidelines are recommended to optimize the board layout for the LMH1228.

10.1.1 Board Stack-Up and Ground References

- Choose a suitable board stack-up that supports 75-Ω single-ended trace and 100-Ω differential trace routing on the top layer of the board. This is typically done with a Layer-2 ground plane reference for the 100-Ω differential traces and a Layer-3 ground plane reference for the 75-Ω single-end traces.
- Maintain a distance of at least 5 times the trace width between signal trace and ground reference if they are on the same layer. This prevents unwanted changes in the characteristic impedance.
- Maintain a consistent ground plane reference for each high-speed trace from source to end-point. Ground reference discontinuities lead to characteristic impedance mismatch.

10.1.2 High-Speed PCB Trace Routing and Coupling

Observe the following general high-speed recommendations for high-speed trace routing:

- For differential pairs, maintain a uniform width and gap for each differential pair where possible. When traces must diverge (for example, due to AC-coupling capacitors), ensure that the traces branch out or merge uniformly.
- To prevent reflections due to trace routing, ensure that trace bends are at most 45°. Right angle bends should be implemented with at least two 45° corners. Radial bends are ideal.
- Avoid using signal vias. If signal vias must be used, a return path (GND) via must be placed near the signal via to provide a consistent ground reference and minimize impedance discontinuities.
- Avoid via stubs by back-drilling as necessary.

Layout Guidelines (continued)

10.1.2.1 SDI_OUT1± and SDI_OUT2±:

- Use an uncoupled trace with 75-Ω single-ended impedance for signal routing to SDI_OUT1± and SDI_OUT2±.
- The trace width is typically 8 to 10 mils with reference to a Layer-3 ground plane.

10.1.2.2 IN0± and OUT0±:

- Use coupled traces with 100-Ω differential impedance for signal routing to IN0± and OUT0±.
- The trace width is typically 5 to 8 mils with reference to a Layer-2 ground plane.

10.1.3 Anti-Pads

- Place anti-pads (ground relief) on the power and ground planes directly under the 4.7-µF, AC-coupling capacitor and IC landing pads to minimize parasitic capacitance. The size of the anti-pad and the number of layers to use the anti-pad depend on the board stack-up and can be determined by a 3-dimension electromagnetic simulation tool.

10.1.4 BNC Connector Layout and Routing

- Use a well-designed BNC footprint to ensure the BNC's signal landing pad achieves 75-Ω characteristic impedance. BNC suppliers usually provide recommendations on BNC footprint for best results.
- Keep trace length short between the BNC and SDI_OUT1±. The trace routing for SDI_OUT1+ and SDI_OUT1– should be as symmetrical as possible, with approximately equal lengths and equal loading. The same is true for SDI_OUT2+ and SDI_OUT2–.

10.1.5 Power Supply and Ground Connections

- Connect each supply pin (VDD_CDR, VIN, VDD_LDO) directly to the power or ground planes with a short via. The via is usually placed tangent to the supply pins' landing pads with the shortest trace possible.
- Power supply decoupling capacitors should be a small physical size (0402 or smaller) and placed close to the supply pins to minimize inductance. The capacitors are commonly placed on the bottom layer and share the ground of the EP (Exposed Pad).

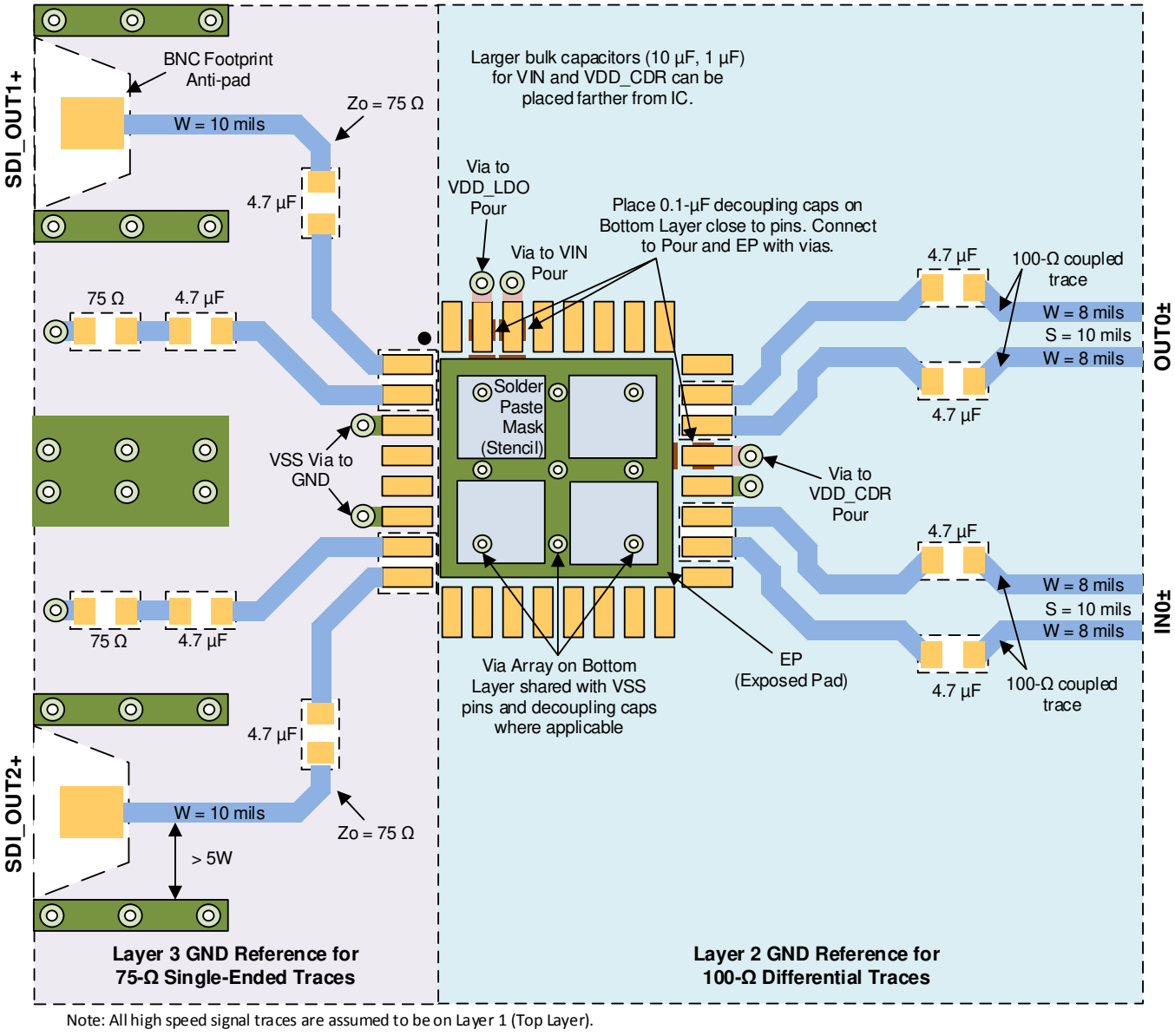
10.1.6 Footprint Recommendations

- Stencil parameters for the EP (Exposed Pad) such as aperture area ratio and the fabrication process have a significant impact on paste deposition. Inspection of the stencil prior to placement of the WQFN package is highly recommended to improve board assembly yields. If the via and aperture openings are not carefully monitored, the solder may flow unevenly through the EP. Stencil parameters for aperture opening and via locations are shown in the RTV package drawing in *Mechanical, Packaging, and Orderable Information*.
- The EP of the package must be connected to the ground plane through a 3 × 3 via array. These vias are solder-masked to avoid solder flowing into the plated-through holes during the board manufacturing process. Details about via dimensions are also shown in the RTV package drawing in *Mechanical, Packaging, and Orderable Information*.

More information on the WQFN style package is provided in *WQFN/SON PCB Attachment Application Report* (SLUA271).

10.2 Layout Example

The example shown in Figure 42 demonstrates the LMH1228 layout guidelines highlighted in *Layout Guidelines*.



Note: All high speed signal traces are assumed to be on Layer 1 (Top Layer).

Figure 42. LMH1228 High-Speed Trace Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

QFN/SON PCB Attachment Application Report (SLUA271)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from Disclosing party under this Agreement, or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMH1228RTVR	Active	Production	WQFN (RTV) | 32	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	L1228
LMH1228RTVR.A	Active	Production	WQFN (RTV) | 32	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	L1228
LMH1228RTVR.B	Active	Production	WQFN (RTV) | 32	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	L1228
LMH1228RTVT	Active	Production	WQFN (RTV) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	L1228
LMH1228RTVT.A	Active	Production	WQFN (RTV) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	L1228
LMH1228RTVT.B	Active	Production	WQFN (RTV) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	L1228
LMH1228RTVTG4	Active	Production	WQFN (RTV) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	L1228
LMH1228RTVTG4.A	Active	Production	WQFN (RTV) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	L1228
LMH1228RTVTG4.B	Active	Production	WQFN (RTV) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	L1228

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

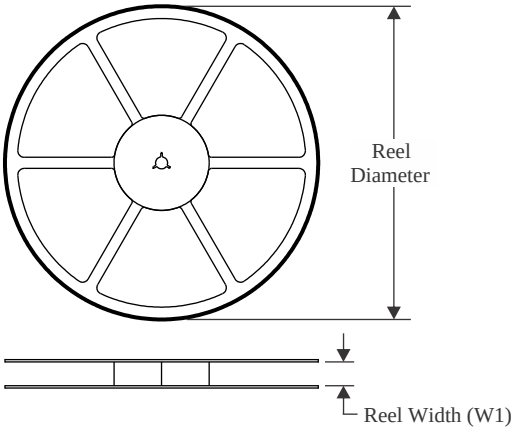
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

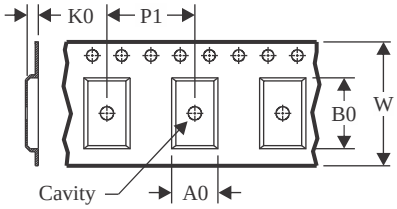
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

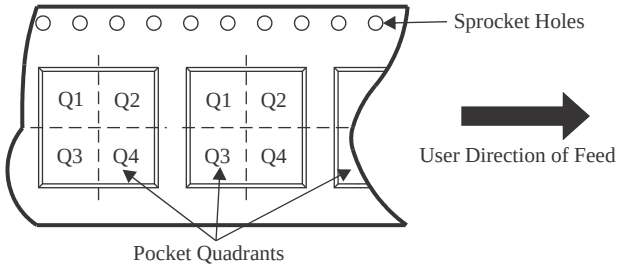


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

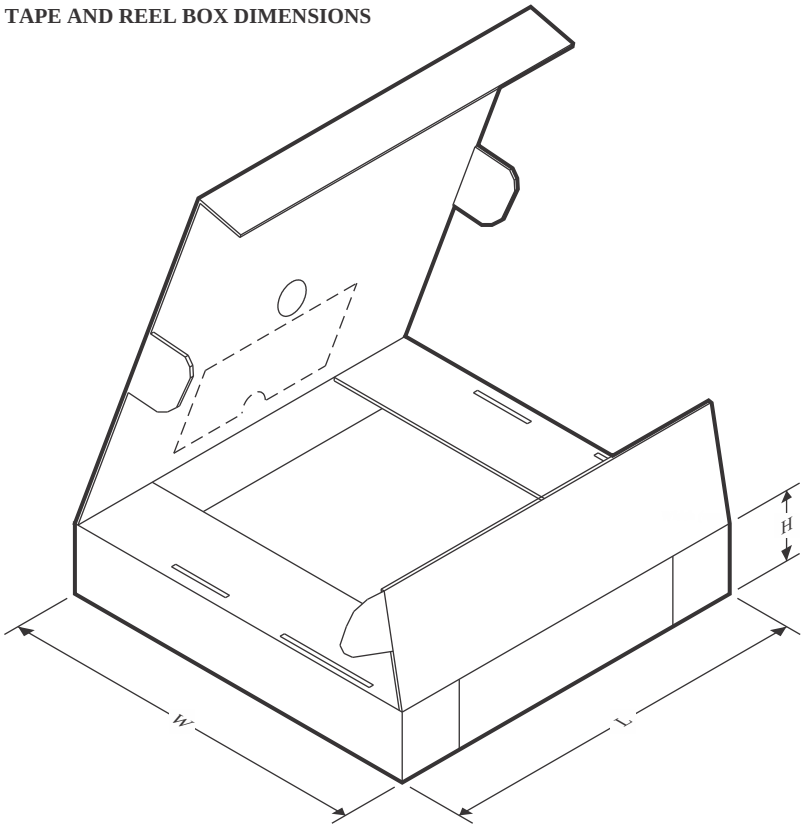
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH1228RTVR	WQFN	RTV	32	1000	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
LMH1228RTVT	WQFN	RTV	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
LMH1228RTVTG4	WQFN	RTV	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

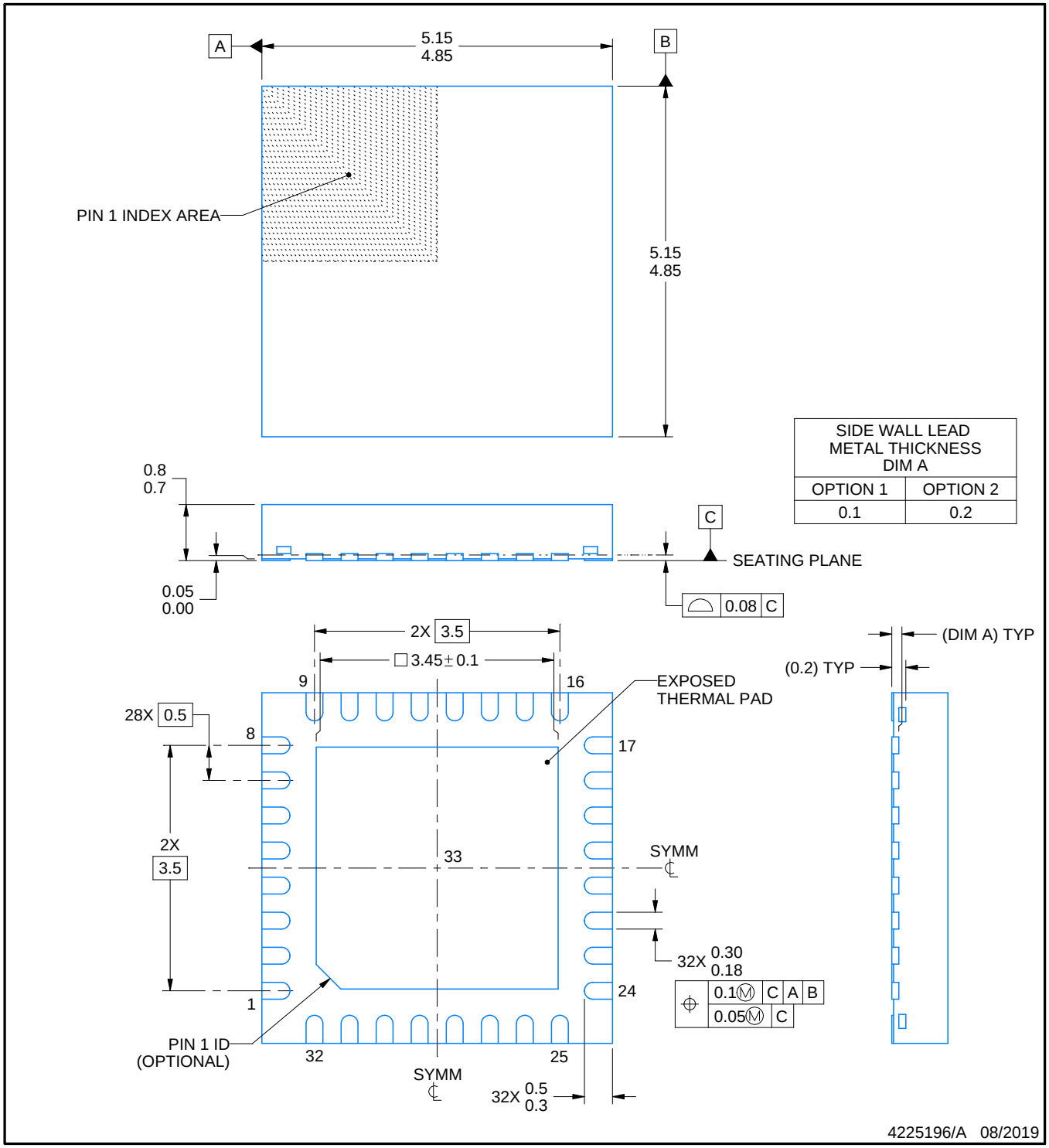
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH1228RTVR	WQFN	RTV	32	1000	182.0	182.0	20.0
LMH1228RTVT	WQFN	RTV	32	250	182.0	182.0	20.0
LMH1228RTVTG4	WQFN	RTV	32	250	182.0	182.0	20.0

RTV0032E

PACKAGE OUTLINE

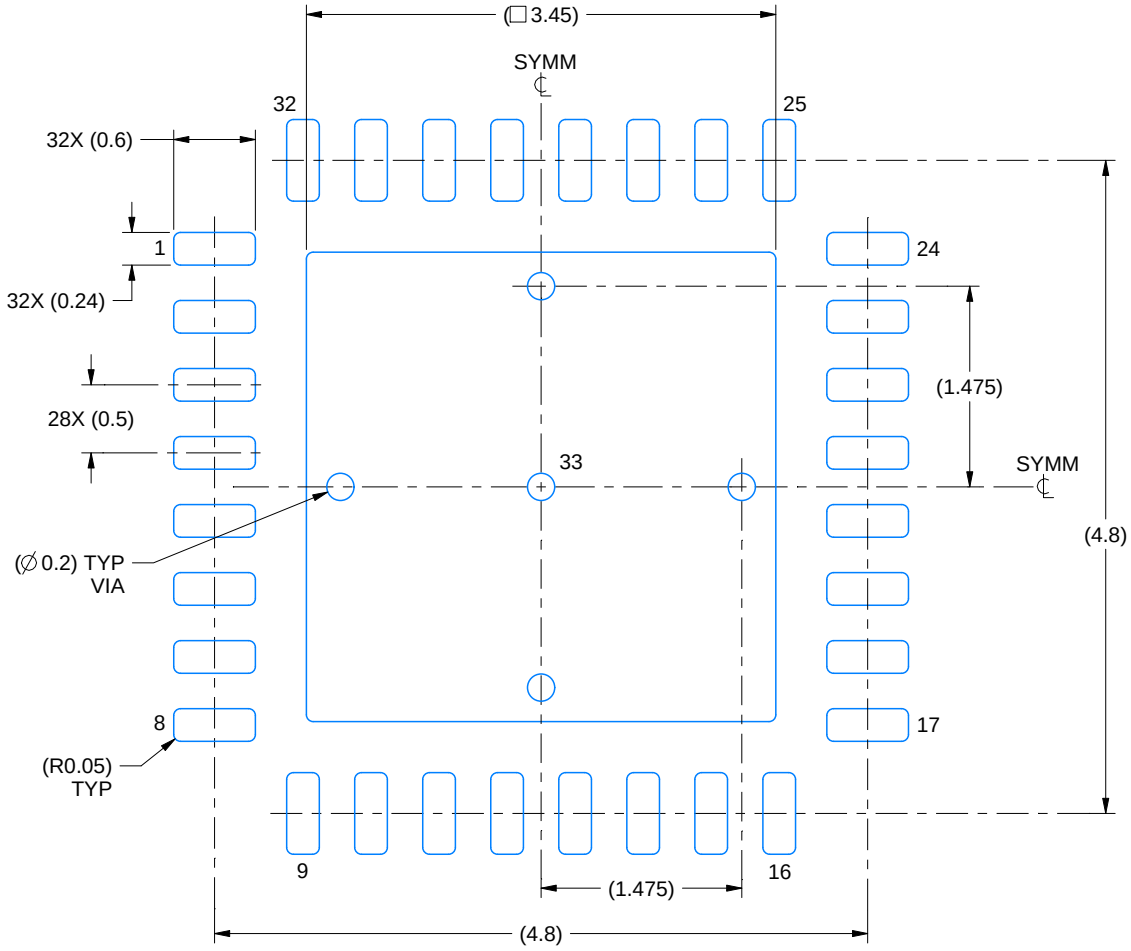
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

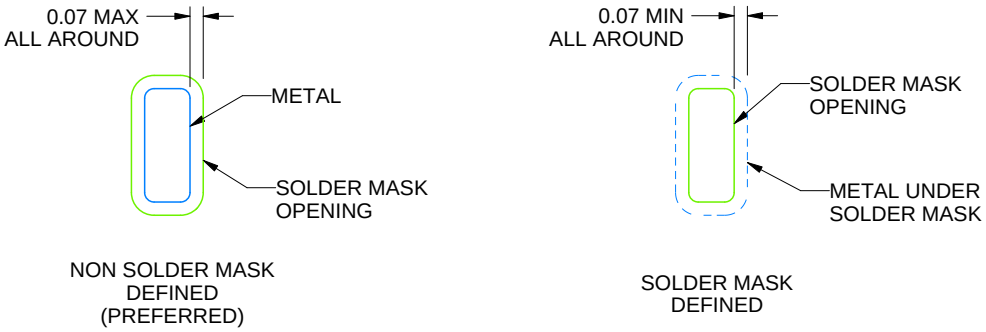


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X

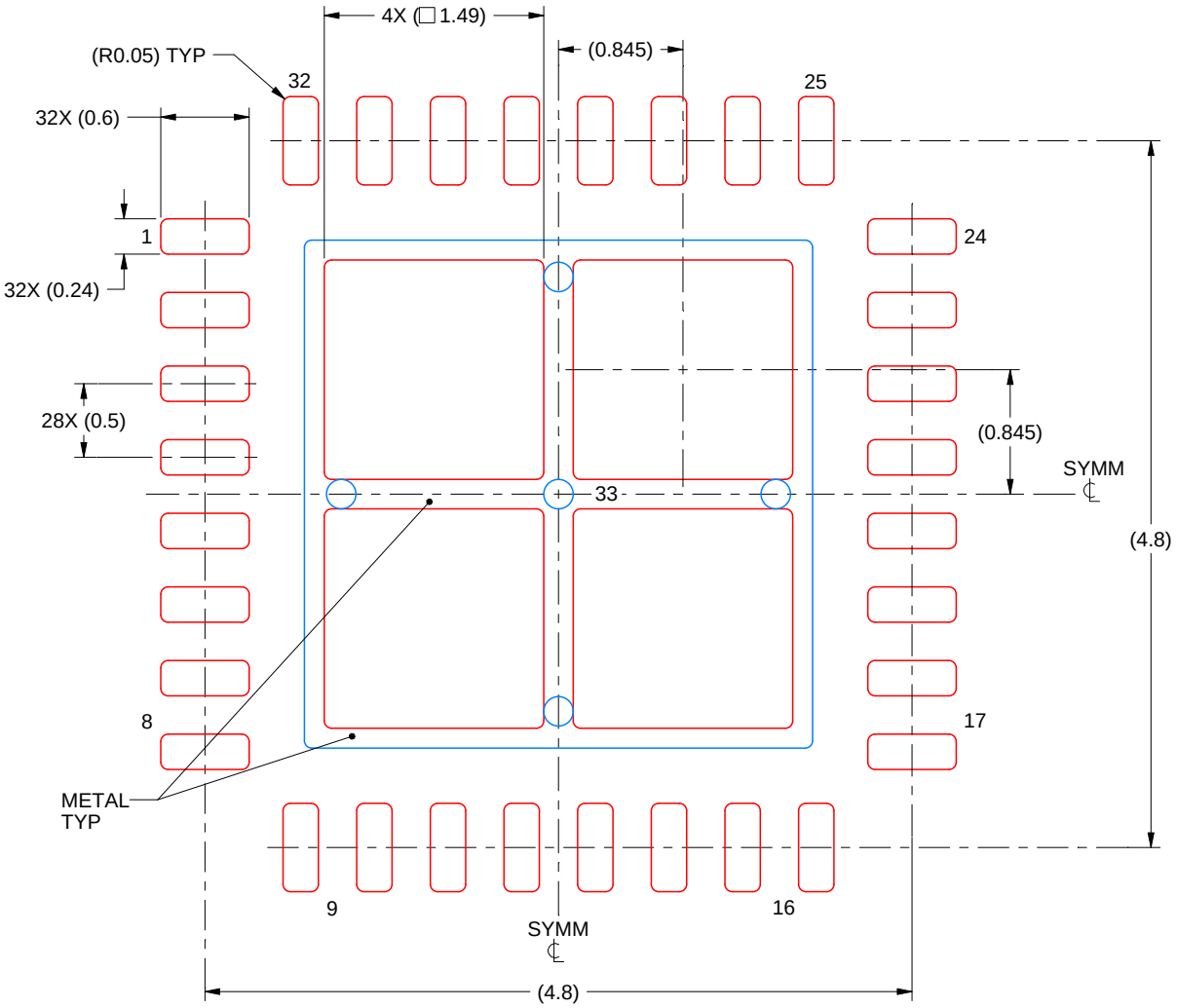


SOLDER MASK DETAILS

4225196/A 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4225196/A 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265