

# LME49721 High-Performance, High-Fidelity Rail-to-Rail Input/Output Audio Operational Amplifier

Check for Samples: LME49721

### **FEATURES**

- Rail-to-Rail Input and Output
- Easily Drives 10kΩ Loads to Within 10mV of Each Power Supply Voltage
- Optimized for Superior Audio Signal Fidelity
- Output Short Circuit Protection

### **APPLICATIONS**

- Ultra High-Quality Portable Audio Amplification
- · High-Fidelity Preamplifiers
- · High-Fidelity Multimedia
- State-of-the-Art Phono Pre Amps
- High-Performance Professional Audio
- High-Fidelity Equalization and Crossover Networks
- High-Performance Line Drivers
- High-Performance Line Receivers
- High-Fidelity Active Filters
- DAC I–V Converter
- ADC Front-End Signal Conditioning

### **KEY SPECIFICATIONS**

- Power Supply Voltage Range: 2.2V to 5.5V
- Quiescent Current: 2.15mA (typ)
- THD+N ( $A_V = 2$ ,  $V_{OUT} = 4V_{p-p}$ ,  $f_{IN} = 1$ kHz)
  - $R_L = 2k\Omega$ : 0.00008% (typ) -  $R_L = 600\Omega$ : 0.0001% (typ)
- Input Noise Density: 4nV/√Hz (typ), @ 1kHz
- Slew Rate: ±8.5V/µs (typ)
- Gain Bandwidth Product: 20MHz (typ)
- Open Loop Gain ( $R_L = 600\Omega$ ): 118dB (typ)
- Input Bias Current: 40fA (typ)Input Offset Voltage: 0.3mV (typ)
- PSRR: 103dB (typ)

### DESCRIPTION

The LME49721 is a low-distortion, low-noise Rail-to-Rail Input/Output operational amplifier optimized and fully specified for high-performance, high-fidelity applications. Combining advanced leading-edge technology with state-of-the-art circuit process design, the LME49721 Rail-to-Rail Input/Output operational amplifier delivers superior amplification for outstanding performance. The LME49721 combines a very high slew rate with low THD+N to easily satisfy demanding applications. To ensure that the most challenging loads are driven without compromise, the LME49721 has a high slew rate of ±8.5V/µs and an output current capability of ±9.7mA. Further, dynamic range is maximized by an output stage that drives 10kΩ loads to within 10mV of either power supply voltage.

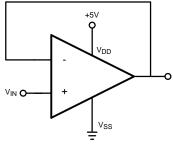
The LME49721 has a wide supply range of 2.2V to 5.5V. Over this supply range the LME49721's input circuitry maintains excellent common-mode and power supply rejection, as well as maintaining its low input bias current. The LME49721 is unity gain stable.

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Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



#### TYPICAL CONNECTION AND PINOUT





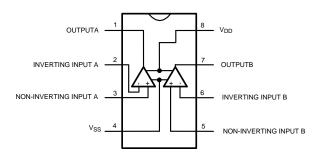


Figure 2. 8-Pin SOIC (D Package)



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### **ABSOLUTE MAXIMUM RATINGS**(1)(2)(3)

| Power Supply Voltage (V <sub>S</sub> = V <sup>+</sup> - V <sup>-</sup> ) | 6V                            |
|--|-------------------------------|
| Storage Temperature  | −65°C to 150°C                |
| Input Voltage  | (V-) - 0.7V to (V+) + 0.7V    |
| Output Short Circuit <sup>(4)</sup>                                      | Continuous                    |
| Power Dissipation  | Internally Limited            |
| ESD Rating <sup>(5)</sup>  | 2000V                         |
| ESD Rating <sup>(6)</sup>  | 200V                          |
| Junction Temperature   | 150°C                         |
| Thermal Resistance, θ <sub>JA</sub> (SOIC)                               | 165°C/W                       |
| Temperature Range, T <sub>MIN</sub> ≤ T <sub>A</sub> ≤ T <sub>MAX</sub>  | -40°C ≤ T <sub>A</sub> ≤ 85°C |
| Supply Voltage Range   | $2.2V \le V_S \le 5.5V$       |

- (1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified
- (2) The Electrical Characteristics table lists ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
- (3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- (4) The maximum power dissipation must be derated at elevated temperatures and is dictated by T<sub>JMAX</sub>, θ<sub>JA</sub>, and the ambient temperature, T<sub>A</sub>. The maximum allowable power dissipation is P<sub>DMAX</sub> = (T<sub>JMAX</sub> T<sub>A</sub>) / θ<sub>JA</sub> or the number given in Absolute Maximum Ratings, whichever is lower.
- (5) Human body model, applicable std. JESD22-A114C.
- (6) Machine model, applicable std. JESD22-A115-A.



### **ELECTRICAL CHARACTERISTICS FOR THE LME49721**

The following specifications apply for the circuit shown in Figure 1.  $V_S = 5V$ ,  $R_L = 10k\Omega$ ,  $R_{SOURCE} = 10\Omega$ ,  $f_{IN} = 1kHz$ , and  $T_A = 25^{\circ}C$ , unless otherwise specified.

| Symbol                  | Parameter   | Conditions  |                        | 49721                    | Units                      |
|-------------------------|---|---|------------------------|--------------------------|----------------------------|
| Cymbol                  | 1 didileter   | Conditions  | Typical <sup>(1)</sup> | Limit <sup>(2)</sup>     | (Limits)                   |
| THD+N                   | Total Harmonic Distortion + Noise                             | $\label{eq:local_control_control} \begin{split} A_V &= +1, \ V_{OUT} = 2V_{p\text{-}p}, \\ R_L &= 2k\Omega \\ R_L &= 600\Omega \end{split}$ | 0.0002<br>0.0002       | 0.001                    | % (max)                    |
| IMD                     | Intermodulation Distortion                                    | $A_V = +1$ , $V_{OUT} = 2V_{p-p}$ ,<br>Two-tone, 60Hz & 7kHz 4:1  | 0.0004                 |                          | %                          |
| GBWP                    | Gain Bandwidth Product  |   | 20                     | 15                       | MHz (min)                  |
| SR                      | Slew Rate   | A <sub>V</sub> = +1   | 8.5                    |                          | V/µs (min)                 |
| FPBW                    | Full Power Bandwidth  | V <sub>OUT</sub> = 1V <sub>P-P</sub> , –3dB<br>referenced to output magnitude<br>at f = 1kHz  | 2.2                    |                          | MHz                        |
| t <sub>s</sub>          | Settling time   | A <sub>V</sub> = 1, 4V step<br>0.1% error range   | 800                    |                          | ns                         |
| _                       | Equivalent Input Noise Voltage                                | f <sub>BW</sub> = 20Hz to 20kHz,<br>A-weighted  | .707                   | 1.13                     | μV <sub>P-P</sub><br>(max) |
| e <sub>n</sub>          | Equivalent Input Noise Density                                | f = 1kHz<br>A-weighted  | 4                      | 6                        | nV <b>/</b> √Hz<br>(max)   |
| In                      | Current Noise Density   | f = 10kHz   | 4.0                    |                          | fA <b>/</b> √Hz            |
| Vos                     | Offset Voltage  |   | 0.3                    | 1.5                      | mV (max)                   |
| ΔV <sub>OS</sub> /ΔTemp | Average Input Offset Voltage Drift vs<br>Temperature          | 40°C ≤ T <sub>A</sub> ≤ 85°C  | 1.1                    |                          | μV/°C                      |
| PSRR                    | Average Input Offset Voltage Shift vs<br>Power Supply Voltage |   | 103                    | 85                       | dB (min)                   |
| ISO <sub>CH-CH</sub>    | Channel-to-Channel Isolation                                  | f <sub>IN</sub> = 1kHz  | 117                    |                          | dB                         |
| I <sub>B</sub>          | Input Bias Current  | $V_{CM} = V_S/2$  | 40                     |                          | fA                         |
| ΔI <sub>OS</sub> /ΔTemp | Input Bias Current Drift vs<br>Temperature                    | -40°C ≤ T <sub>A</sub> ≤ 85°C   | 48                     |                          | fA/°C                      |
| Ios                     | Input Offset Current  | $V_{CM} = V_S/2$  | 60                     |                          | fA                         |
| V <sub>IN-CM</sub>      | Common-Mode Input Voltage Range                               |   |                        | (V+) - 0.1<br>(V-) + 0.1 | V (min)                    |
| CMRR                    | Common-Mode Rejection   | V <sub>SS</sub> - 100mV < V <sub>CM</sub> < V <sub>DD</sub> + 100mV   | 93                     | 70                       | dB (min)                   |
|                         | 1/f Corner Frequency  |   | 2000                   |                          | Hz                         |
|                         |   | $V_{SS}$ - 200mV < $V_{OUT}$ < $V_{DD}$ + 200mV   |                        | •                        | ·                          |
| ^                       | Open Lean Veltage Cain  | $R_L = 600\Omega$   | 118                    | 100                      | dB (min)                   |
| A <sub>VOL</sub>        | Open Loop Voltage Gain  | $R_L = 2k\Omega$  | 122                    |                          | dB (min)                   |
|                         |   | $R_L = 10k\Omega$   | 130                    | 115                      | dB (min)                   |
|                         |   | B 6000  | $V_{DD} - 30 mV$       | $V_{DD} - 80 \text{mV}$  | V (min)                    |
|                         | Outrot Valta na Cuina   | $R_L = 600\Omega$   | V <sub>SS</sub> + 30mV | V <sub>SS</sub> + 80mV   | V (min)                    |
| V <sub>OUTMIN</sub>     | Output Voltage Swing  | B 40k0 V 5 0V   | V <sub>DD</sub> – 10mV | V <sub>DD</sub> – 20mV   | V (min)                    |
|                         |   | $R_L = 10k\Omega$ , $V_S = 5.0V$  | V <sub>SS</sub> + 10mV | V <sub>SS</sub> + 20mV   | V (min)                    |
| l <sub>OUT</sub>        | Output Current  | $R_L = 250\Omega, V_S = 5.0V$   | 9.7                    | 9.3                      | mA (min)                   |
| I <sub>OUT-SC</sub>     | Short Circuit Current   |   | 100                    |                          | mA                         |
| R <sub>OUT</sub>        | Output Impedance  | f <sub>IN</sub> = 10kHz<br>Closed-Loop<br>Open-Loop   | 0.01<br>46             |                          | Ω                          |
| I <sub>S</sub>          | Quiescent Current per Amplifier                               | I <sub>OUT</sub> = 0mA  | 2.15                   | 3.25                     | mA (max)                   |

<sup>(1)</sup> Typical values represent most likely parametric norms at  $T_A = +25^{\circ}C$ , and at the Recommended Operation Conditions at the time of product characterization and are not ensured.

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<sup>(2)</sup> Datasheet min/max specification limits are ensured by test or statistical analysis.

### TYPICAL PERFORMANCE CHARACTERISTICS

Graphs were taken in dual supply configuration.

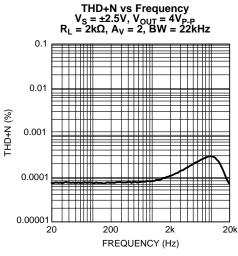


Figure 3.

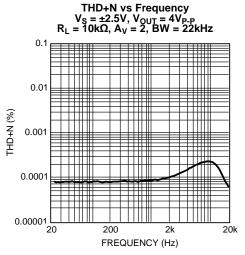


Figure 5.

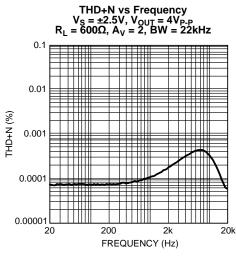


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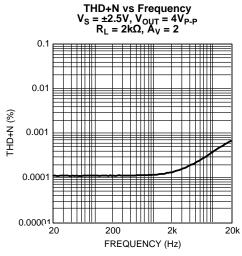


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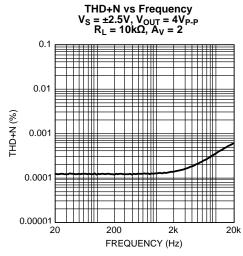


Figure 6.

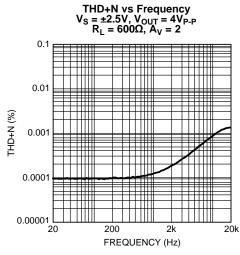


Figure 8.



Graphs were taken in dual supply configuration.

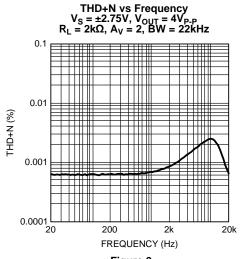


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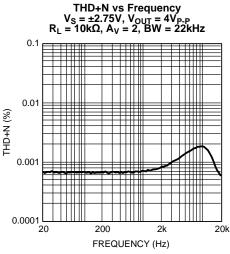
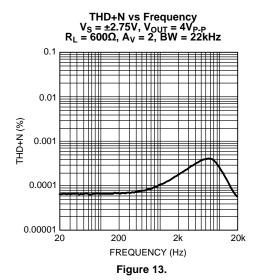


Figure 11.



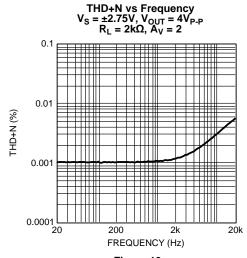


Figure 10.

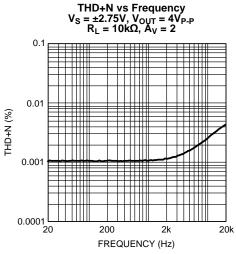


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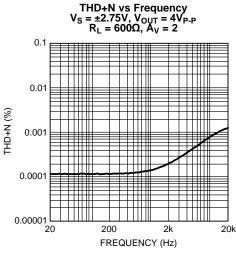


Figure 14.

Graphs were taken in dual supply configuration.

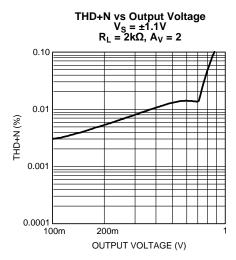


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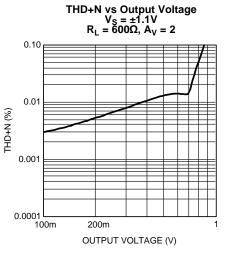
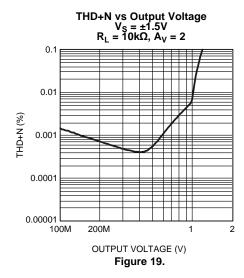


Figure 17.



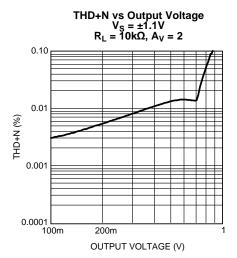


Figure 16.

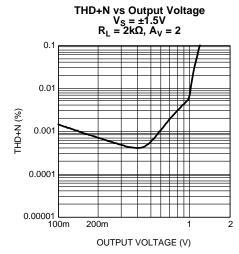
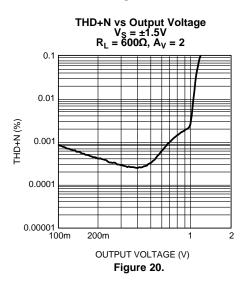
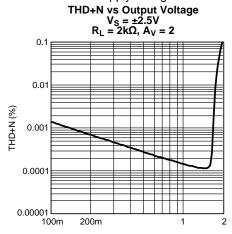


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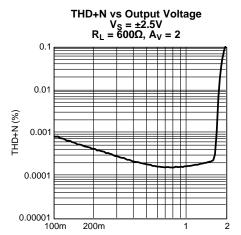




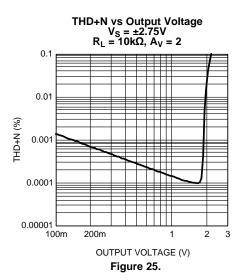
Graphs were taken in dual supply configuration.



OUTPUT VOLTAGE (V) Figure 21.



OUTPUT VOLTAGE (V) Figure 23.



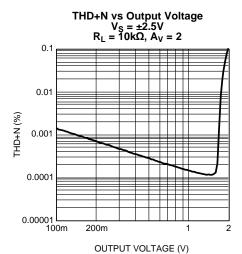
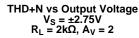
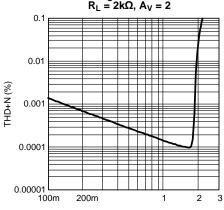


Figure 22.





OUTPUT VOLTAGE (V) Figure 24.

THD+N vs Output Voltage  $V_S = \pm 2.75V$  $R_L = 600\Omega$ ,  $A_V = 2$ 

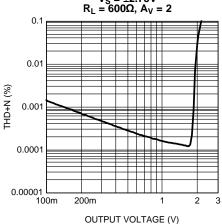
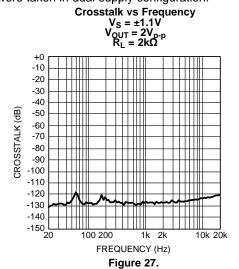
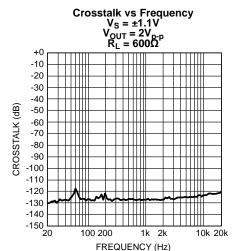


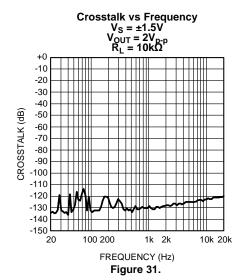
Figure 26.

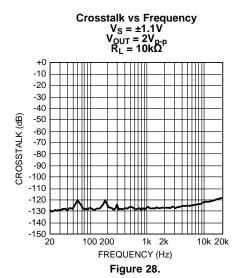
Graphs were taken in dual supply configuration.

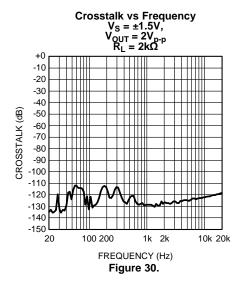


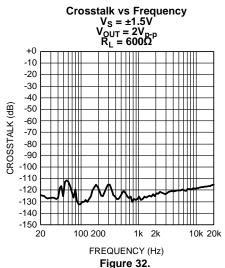














Graphs were taken in dual supply configuration.

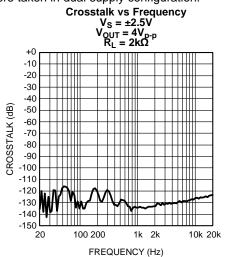
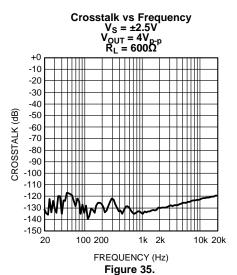
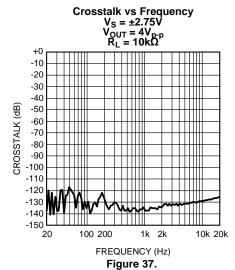
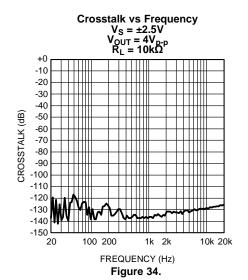
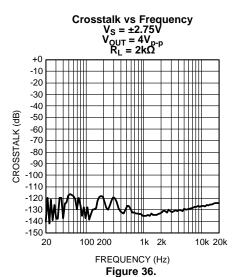


Figure 33.









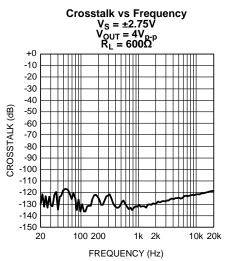


Figure 38.

Product Folder Links: LME49721



Graphs were taken in dual supply configuration.

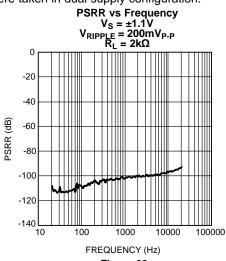


Figure 39.

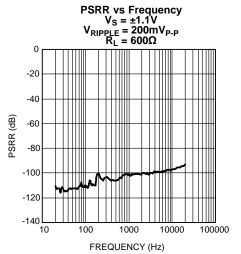
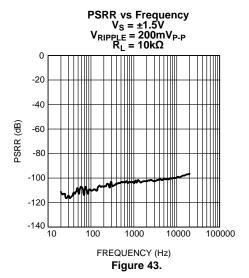
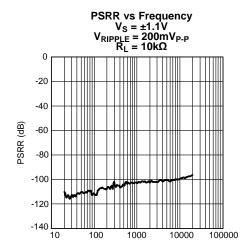


Figure 41.





FREQUENCY (Hz) **Figure 40.** 

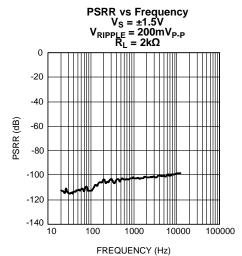


Figure 42.

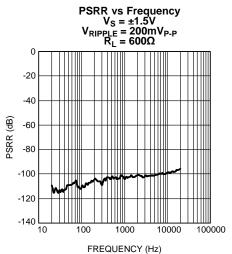


Figure 44.



Graphs were taken in dual supply configuration.

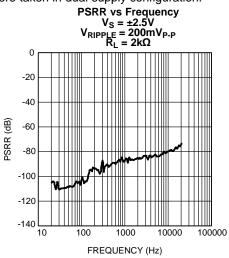


Figure 45.

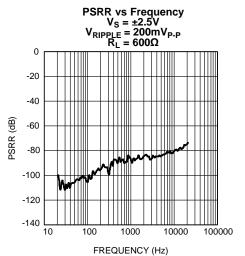
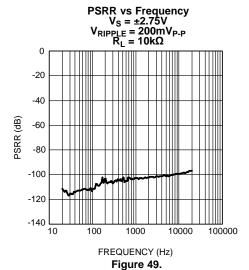
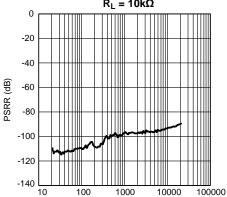


Figure 47.



 $\begin{array}{c} \text{PSRR vs Frequency} \\ \text{V}_{\text{S}} = \pm 2.5 \text{V} \\ \text{V}_{\text{RIPPLE}} = 200 \text{mV}_{\text{P-P}} \\ \text{R}_{\text{L}} = 10 \text{k}\Omega \end{array}$ 



FREQUENCY (Hz) Figure 46.

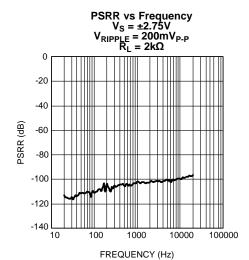


Figure 48.

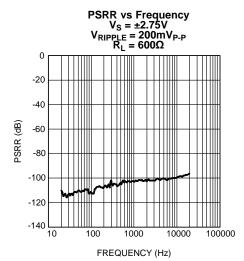
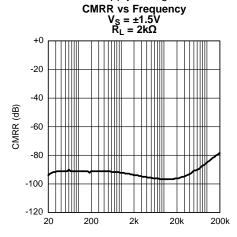


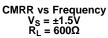
Figure 50.

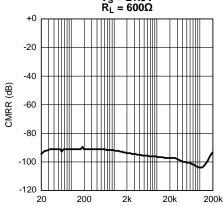


Graphs were taken in dual supply configuration.

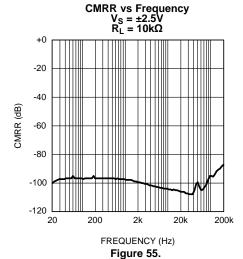


FREQUENCY (Hz) Figure 51.

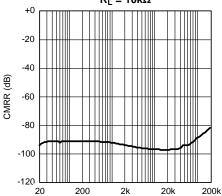




FREQUENCY (Hz) Figure 53.

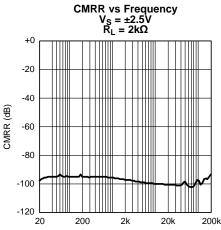


CMRR vs Frequency  $V_S = \pm 1.5V$   $R_L = 10k\Omega$ +0

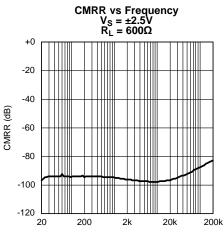


FREQUENCY (Hz)

Figure 52.



FREQUENCY (Hz) Figure 54.



FREQUENCY (Hz)

Figure 56.



Graphs were taken in dual supply configuration.

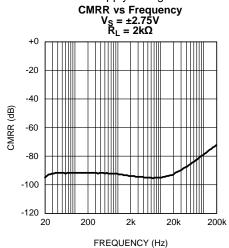
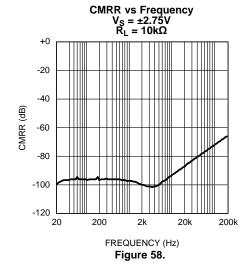


Figure 57.



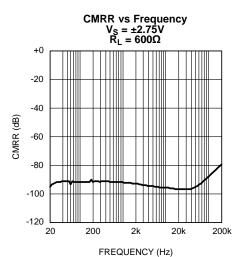
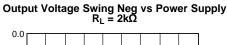


Figure 59.



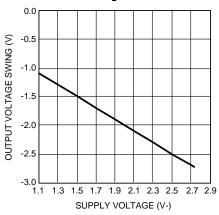


Figure 60.

## Output Voltage Swing Neg vs Power Supply $R_L = 10k\Omega$

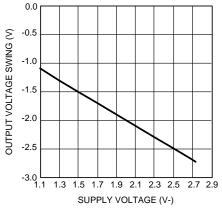


Figure 61.

### Output Voltage Swing Neg vs Power Supply $R_L$ = $600\Omega$

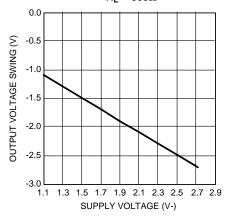


Figure 62.



Graphs were taken in dual supply configuration.

### Output Voltage Swing Pos vs Power Supply $R_L = 2k\Omega$

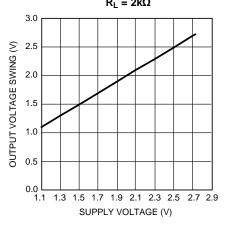


Figure 63.

### Output Voltage Swing Pos vs Power Supply $R_L = 600\Omega$

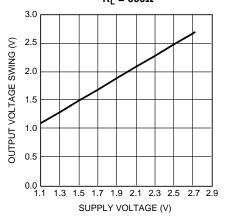
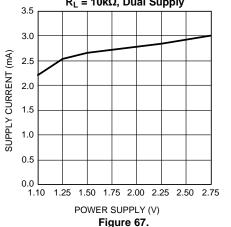


Figure 65.

### Supply Current per amplifier vs Power Supply $R_L$ = 10k $\Omega$ , Dual Supply



### Output Voltage Swing Pos vs Power Supply $R_L = 10k\Omega$

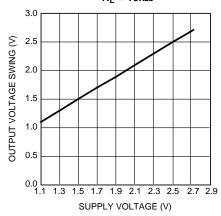


Figure 64.

### Supply Current per amplifier vs Power Supply $R_L = 2k\Omega$ , Dual Supply

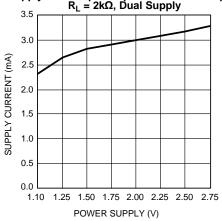


Figure 66.

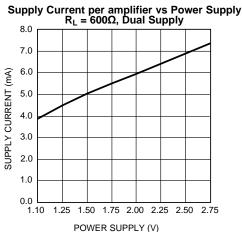


Figure 68.



#### **APPLICATION INFORMATION**

### **DISTORTION MEASUREMENTS**

The vanishingly low residual distortion produced by LME49721 is below the capabilities of all commercially available equipment. This makes distortion measurements just slightly more difficult than simply connecting a distortion meter to the amplifier's inputs and outputs. The solution. however, is quite simple: an additional resistor. Adding this resistor extends the resolution of the distortion measurement equipment.

The LME49721's low residual is an input referred internal error. As shown in Figure 69, adding the  $10\Omega$  resistor connected between a the amplifier's inverting and non-inverting inputs changes the amplifier's noise gain. The result is that the error signal (distortion) is amplified by a factor of 101. Although the amplifier's closed-loop gain is unaltered, the feedback available to correct distortion errors is reduced by 101. To ensure minimum effects on distortion measurements, keep the value of R1 low as shown in Figure 69.

This technique is verified by duplicating the measurements with high closed-loop gain and/or making the measurements at high frequencies. Doing so, produces distortion components that are within equipments capabilities. This datasheet's THD+N and IMD values were generated using the above described circuit connected to an Audio Precision System Two Cascade.

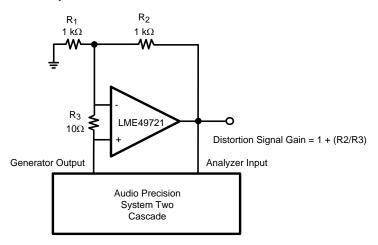


Figure 69. THD+N and IMD Distortion Test Circuit with  $A_V = 2$ 

### **OPERATING RATINGS AND BASIC DESIGN GUIDELINES**

The LME49721 has a supply voltage range from +2.2V to +5.5V single supply or ±1.1 to ±2.75V dual supply.

Bypassed capacitors for the supplies should be placed as close to the amplifier as possible. This will help minimize any inductance between the power supply and the supply pins. In addition to a  $10\mu F$  capacitor, a  $0.1\mu F$  capacitor is also recommended in CMOS amplifiers.

The amplifier's inputs lead lengths should also be as short as possible. If the op amp does not have a bypass capacitor, it may oscillate.

### **BASIC AMPLIFIER CONFIGURATIONS**

The LME49721 may be operated with either a single supply or dual supplies. Figure 70 shows the typical connection for a single supply inverting amplifier. The output voltage for a single supply amplifier will be centered around the common-mode voltage Vcm. Note: the voltage applied to the Vcm insures the output stays above ground. Typically, the Vcm should be equal to  $V_{DD}/2$ . This is done by putting a resistor divider ckt at this node, see Figure 70.

Product Folder Links: LME49721



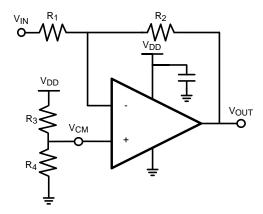


Figure 70. Single-Supply Inverting Op Amp

Figure 71 shows the typical connection for a dual supply inverting amplifier. The output voltage is centered on zero.

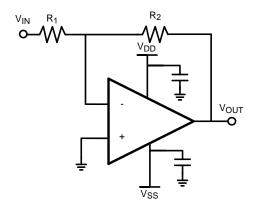


Figure 71. Dual-Supply Inverting Op Amp

Figure 72 shows the typical connection for the Buffer Amplifier or also called a Voltage Follower. A Buffer Amplifier can be used to solve impedance matching problems, to reduce power consumption in the source, or to drive heavy loads. The input impedance of the op amp is very high. Therefore, the input of the op amp does not load down the source. The output impedance on the other hand is very low. It allows the load to either supply or absorb energy to a circuit while a secondary voltage source dissipates energy from a circuit. The Buffer is a unity stable amplifier, 1V/V. Although the feedback loop is tied from the output of the amplifier to the inverting input, the gain is still positive. Note: if a positive feedback is used, the amplifier will most likely drive to either rail at the output.

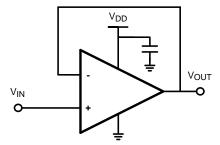


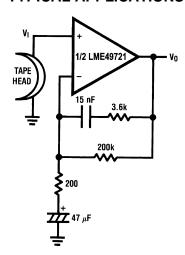
Figure 72. Buffer

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### **TYPICAL APPLICATIONS**



 $A_V = 34.5$  F = 1 kHz  $E_n = 0.38 \text{ }\mu\text{V}$  A Weighted

Figure 73. ANAB Preamp

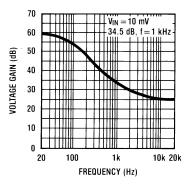
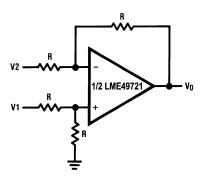


Figure 74. NAB Preamp Voltage Gain vs Frequency



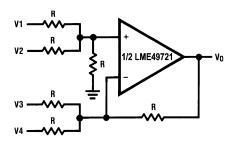
 $V_O = V1-V2$ 

Figure 75. Balanced to Single-Ended Converter

Product Folder Links: LME49721

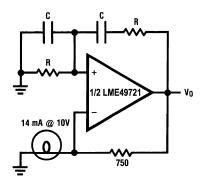
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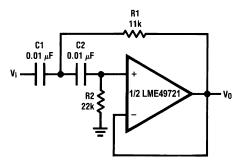
 $V_0 = V1 + V2 - V3 - V4$ 

Figure 76. Adder/Subtracter



$$f_0 = \frac{1}{2\pi RC}$$

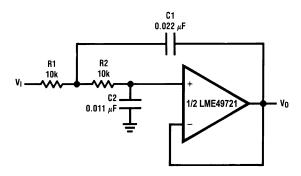
Figure 77. Sine Wave Oscillator



if C1 = C2 = C  $R1 = \frac{\sqrt{2}}{2\omega_0C}$   $R2 = 2 \bullet R1$  Illustration is  $f_0 = 1 \text{ kHz}$ 

Figure 78. Second-Order High-Pass Filter (Butterworth)



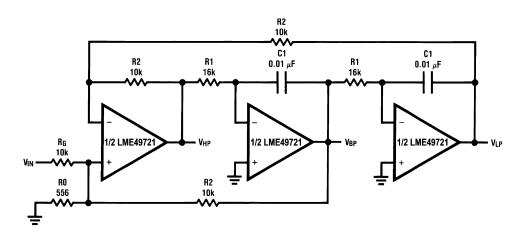


$$C1 = \frac{\sqrt{2}}{\omega_0 B}$$

$$C2 = \frac{C}{2}$$

Illustration is  $f_0 = 1 \text{ kHz}$ 

Figure 79. Second-Order Low-Pass Filter (Butterworth)



$$\begin{split} f_0 &= \frac{1}{2\pi C 1R1}, Q = \frac{1}{2} \left(1 + \frac{R2}{R0} + \frac{R2}{RG}\right), A_{BP} = QA_{LP} = QA_{LH} = \frac{R2}{RG} \end{split}$$
 Illustration is  $f_0 = 1$  kHz,  $Q = 10$ ,  $A_{BP} = 1$ 

Figure 80. State Variable Filter

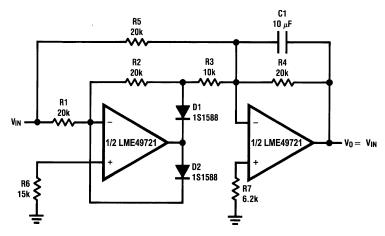


Figure 81. AC/DC Converter



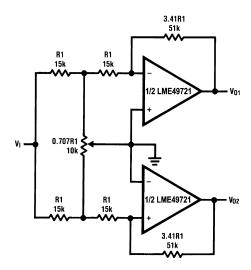


Figure 82. 2-Channel Panning Circuit (Pan Pot)

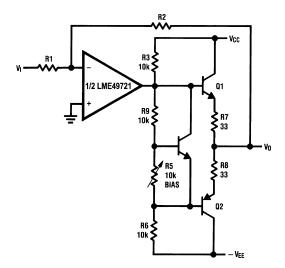
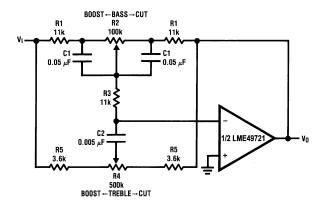


Figure 83. Line Driver





```
\begin{split} f_L &= \frac{1}{2\pi R2C1}, f_{LB} = \frac{1}{2\pi R1C1} \\ f_H &= \frac{1}{2\pi R5C2}, f_{HB} = \frac{1}{2\pi (R1 + R5 + 2R3)C2} \\ Illustration is: \\ f_L &= 32 \ Hz, \ f_{LB} = 320 \ Hz \\ f_H &= 11 \ kHz, \ f_{HB} = 1.1 \ kHz \end{split}
```

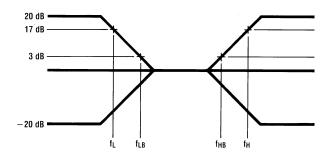
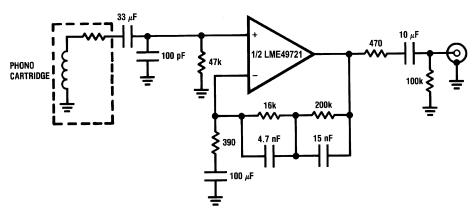


Figure 84. Tone Control

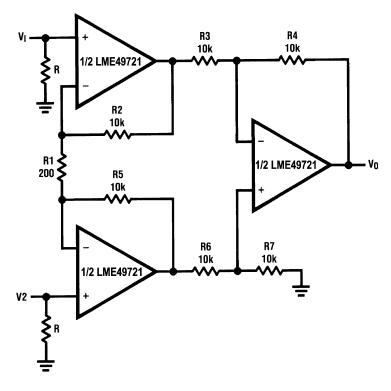


 $\begin{array}{l} A_v = 35 \text{ dB} \\ E_n = 0.33 \text{ } \mu\text{V} \\ \text{S/N} = 90 \text{ dB} \\ \text{f} = 1 \text{ kHz} \\ \text{A Weighted}, \text{ V}_{\text{IN}} = 10 \text{ mV} \\ \text{@f} = 1 \text{ kHz} \end{array}$ 

Figure 85. RIAA Preamp

Product Folder Links: LME49721

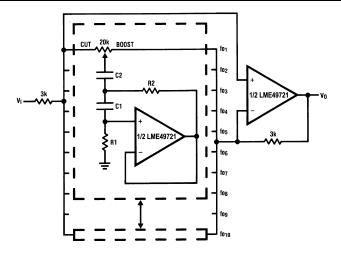




If R2 = R5, R3 = R6, R4 = R7 
$$V0 = \left(1 + \frac{2R2}{R1}\right) \frac{R4}{R3}(V2 - V1)$$
 Illustration is: 
$$V0 = 101(V2 - V1)$$

Figure 86. Balanced Input Mic Amp





A. See Table 1.

Figure 87. 10-Band Graphic Equalizer

Table 1.  $C_1$ ,  $C_2$ ,  $R_1$ , and  $R_2$  Values for Figure 87<sup>(1)</sup>

| fo (Hz) | C <sub>1</sub> | C <sub>2</sub> | R <sub>1</sub> | R <sub>2</sub> |
|---------|----------------|----------------|----------------|----------------|
| 32      | 0.12µF         | 4.7µF          | 75kΩ           | 500Ω           |
| 64      | 0.056µF        | 3.3µF          | 68kΩ           | 510Ω           |
| 125     | 0.033µF        | 1.5µF          | 62kΩ           | 510Ω           |
| 250     | 0.015µF        | 0.82µF         | 68kΩ           | 470Ω           |
| 500     | 8200pF         | 0.39µF         | 62kΩ           | 470Ω           |
| 1k      | 3900pF         | 0.22µF         | 68kΩ           | 470Ω           |
| 2k      | 2000pF         | 0.1µF          | 68kΩ           | 470Ω           |
| 4k      | 1100pF         | 0.056µF        | 62kΩ           | 470Ω           |
| 8k      | 510pF          | 0.022µF        | 68kΩ           | 510Ω           |
| 16k     | 330pF          | 0.012µF        | 51kΩ           | 510Ω           |

(1) At volume of change =  $\pm 12$  dB Q = 1.7



### **REVISION HISTORY**

| Rev | Date     | Description   |
|-----|----------|---|
| 1.0 | 09/26/07 | Initial release.                                    |
| 1.1 | 10/01/07 | Input more info under the Buffer Amplifier.         |
| 1.2 | 04/21/10 | Added the Ordering Information table.               |
| С   | 04/04/13 | Changed layout of National Data Sheet to TI format. |

www.ti.com 11-Nov-2025

#### PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type | Package   Pins | Package qty   Carrier | RoHS | Lead finish/<br>Ball material | MSL rating/<br>Peak reflow | Op temp (°C) | Part marking (6) |
|-----------------------|------------|---------------|----------------|-----------------------|------|-------------------------------|----------------------------|--------------|------------------|
| LME49721MA/NOPB       | Active     | Production    | SOIC (D)   8   | 95   TUBE             | Yes  | SN                            | Level-1-260C-UNLIM         | -40 to 85    | L49721<br>MA     |
| LME49721MA/NOPB.A     | Active     | Production    | SOIC (D)   8   | 95   TUBE             | Yes  | SN                            | Level-1-260C-UNLIM         | -40 to 85    | L49721<br>MA     |
| LME49721MAX/NOPB      | Active     | Production    | SOIC (D)   8   | 2500   LARGE T&R      | Yes  | SN                            | Level-1-260C-UNLIM         | -40 to 85    | L49721<br>MA     |
| LME49721MAX/NOPB.A    | Active     | Production    | SOIC (D)   8   | 2500   LARGE T&R      | Yes  | SN                            | Level-1-260C-UNLIM         | -40 to 85    | L49721<br>MA     |

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

- (3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
- (4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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### **PACKAGE OPTION ADDENDUM**

www.ti.com 11-Nov-2025

### **PACKAGE MATERIALS INFORMATION**

www.ti.com 23-May-2025

### TAPE AND REEL INFORMATION





| A0 | Dimension designed to accommodate the component width     |
|----|---|
| В0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

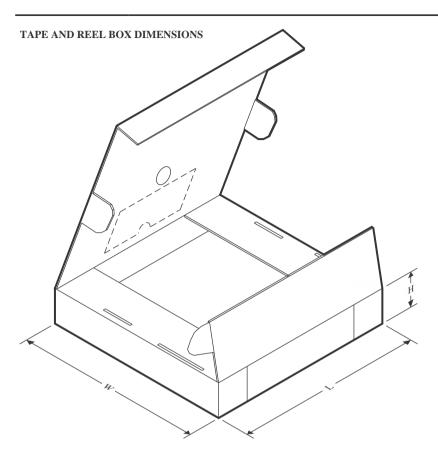
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

| Device           |      | Package<br>Drawing |   | SPQ  | Reel<br>Diameter<br>(mm) | Reel<br>Width<br>W1 (mm) | A0<br>(mm) | B0<br>(mm) | K0<br>(mm) | P1<br>(mm) | W<br>(mm) | Pin1<br>Quadrant |
|------------------|------|--------------------|---|------|--------------------------|--------------------------|------------|------------|------------|------------|-----------|------------------|
| LME49721MAX/NOPB | SOIC | D                  | 8 | 2500 | 330.0                    | 12.4                     | 6.5        | 5.4        | 2.0        | 8.0        | 12.0      | Q1               |

www.ti.com 23-May-2025



### \*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |  |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|--|
| LME49721MAX/NOPB | SOIC         | D               | 8    | 2500 | 367.0       | 367.0      | 35.0        |  |

### **PACKAGE MATERIALS INFORMATION**

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### **TUBE**



### \*All dimensions are nominal

| Device            | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|-------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| LME49721MA/NOPB   | D            | SOIC         | 8    | 95  | 495    | 8      | 4064   | 3.05   |
| LME49721MA/NOPB.A | D            | SOIC         | 8    | 95  | 495    | 8      | 4064   | 3.05   |



SMALL OUTLINE INTEGRATED CIRCUIT



### NOTES:

- 1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- 4. This dimension does not include interlead flash.
- 5. Reference JEDEC registration MS-012, variation AA.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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