LMC8101 Rail-to-Rail Input and Output, 2.7V Op Amp in DSBGA Package With Shutdown

Check for Samples: LMC8101

FEATURES

- V_S = 2.7V, T_A = 25°C, R_L to $V^+/2$, Typical Values Unless Specified.
- Rail-to-Rail Inputs
- Rail-to-Rail Output Swing Within 35mV of Supplies (R_L =2kΩ)
- Packages Offered:
  - DSBGA package 1.39mm x 1.41mm
  - VSSOP package 3.0mm x 4.9mm
- Low Supply Current <1mA (max)
- Shutdown Current 1µA (Max)
- Versatile Shutdown Feature 10µs Turn-On
- Output Short Circuit Current 10mA
- Offset Voltage ±5 mV (max)
- Gain-Bandwidth 1MHz
- Supply Voltage Range 2.7V-10V
- THD 0.18%
- Voltage Noise 36nv/$\sqrt{Hz}$

APPLICATIONS

- Portable Communication (Voice, Data)
- Cellular Phone Power Amp Control Loop
- Buffer AMP
- Active Filters
- Battery Sense
- VCO Loop

DESCRIPTION

The LMC8101 is a Rail-to-Rail Input and Output high performance CMOS operational amplifier. The LMC8101 is ideal for low voltage (2.7V to 10V) applications requiring Rail-to-Rail inputs and output. The LMC8101 is supplied in the die sized DSBGA as well as the 8 pin VSSOP packages. The DSBGA package requires 75% less board space as compared to the SOT-23 package. The LMC8101 is an upgrade to the industry standard LMC7101.

The LMC8101 incorporates a simple user controlled methodology for shutdown. This allows ease of use while reducing the total supply current to 1nA typical. This extends battery life where power saving is mandated. The shutdown input threshold can be set relative to either V^+ or V^- using the SL pin (see Application Notes section for details).

Other enhancements include improved offset voltage limit, three times the output current drive and lower 1/f noise when compared to the industry standard LMC7101 Op Amp. This makes the LMC8101 ideal for use in many battery powered, wireless communication and Industrial applications.

Connection Diagrams

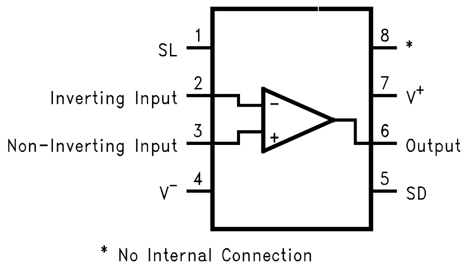

Figure 1. 8-Pin VSSOP Top View

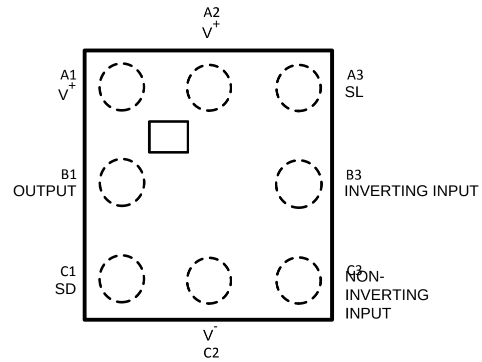

Figure 2. DSBGA Top View

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

ESD Tolerance		2KV(3) 200V(4)
V_{IN} differential		±Supply Voltage
Output Short Circuit Duration		See(5)(6)
Supply Voltage ($V^+ - V^-$)		12V
Voltage at Input/Output pins		V^+ +0.8V, V^- −0.8V
Current at Input Pin		±10mA
Current at Output Pin(5)(6)		±80mA
Current at Power Supply pins		±80mA
Storage Temperature Range		−65°C to +150°C
Junction Temperature(7)		+150°C
Soldering Information	Infrared or Convection (20 sec.)	235°C
	Wave Soldering (10 sec.)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not specified. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human body model, 1.5kΩ in series with 100pF.
(4) Machine Model, 0Ω in series with 200pF.
(5) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature at 150°C. Output currents in excess of 40mA over long term may adversely affect reliability.
(6) Short circuit test is a momentary test. Output short circuit duration is infinite for V_S < 6V. Otherwise, extended period output short circuit may damage the device.
(7) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Operating Ratings

Supply Voltage (V^+ - V^-)		2.7V to 10V
Junction Temperature Range (2)		−40°C to +85°C
Package Thermal Resistance (θ_{JA}) (2)	DSBGA	220°C/W
	VSSOP package 8 pin Surface Mount	230°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not specified. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

2.7V Electrical Characteristics

Unless otherwise specified, all limits specified for T_J = 25°C, V^+ = 2.7V, V^- = 0V, $V_{CM} = V_O = V^+/2$ and R_L > 1 MΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (1)	Limit (2)	Units
V_{OS}	Input Offset Voltage		±0.70	±5 **±7**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		4		µV/°C
I_B	Input Bias Current	See (3)	±1	**±64**	pA max
I_{OS}	Input Offset Current		0.5	**32**	pA max
$R_{in\ CM}$	Input Common Mode Resistance		10		GΩ
$C_{in\ CM}$	Input Common Mode Capacitance		10		pF
CMRR	Common Mode Rejection Ratio	0V < = V_{CM} < = 2.7V	78	60	dB min
		V_S = 3V 0V < = V_{CM} < = 3V	78	64 **60**	
PSRR	Power Supply Rejection Ratio	V_S = 2.7V to 3V	57	50 **48**	dB min
CMVR	Input Common-Mode Voltage Range	V_S = 2.7V CMRR > = 50dB	0.0	0.0	V max
			3.0	2.7	V min
		V_S = 3V CMRR > = 50dB	−0.2	−0.1	V max
			3.2	3.1	V min
A_{VOL}	Large Signal Voltage Gain	Sourcing R_L = 2kΩ to $V^+/2$ V_O = 1.35V to 2.45V	3162	1000 562	V/V min
		Sinking R_L = 2kΩ to $V^+/2$ V_O = 1.35V to 0.25V	3162	804 **562**	
		Sourcing R_L = 10kΩ to $V^+/2$ V_O = 1.35V to 2.65V	4000	1778 **1000**	V/V min
		Sinking R_L = 10kΩ to $V^+/2$ V_O = 1.35V to 0.05V	4000	1778 **1000**	
V_O	Output Swing High	R_L = 2kΩ to $V^+/2$ V_{ID} = 100mV	2.67	2.64 **2.62**	V min
		R_L = 10kΩ to $V^+/2$ V_{ID} = 100mV	2.69	2.68 **2.67**	V min
	Output Swing Low	R_L = 2kΩ to $V^+/2$ V_{ID} = −100mV	32	100 **150**	mV max
		R_L = 10kΩ to $V^+/2$ V_{ID} = −100mV	10	30 **70**	mV max

(1) Typical Values represent the most likely parametric norm.
(2) All limits are specified by testing or statistical analysis.
(3) Positive current corresponds to current flowing into the device.

2.7V Electrical Characteristics (continued)

Unless otherwise specified, all limits specified for T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = V_O = V^+/2 and R_L > 1 MΩ to V^+/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (1)	Limit (2)	Units
I_{SC}	Output Short Circuit Current	Sourcing to V^+/2 V_{ID} = 100mV (4)	20	14 **6**	mA min
		Sinking to V^+/2 V_{ID} = −100mV (4)	10	5 **4**	mA min
I_S	Supply Current	No load, normal operation	0.70	1.0 **1.2**	mA max
		Shutdown mode	0.001	1	µA max
T_{on}	Shutdown Turn-on time	See (5)	10	15	µs
T_{off}	Shutdown Turn-off time	See (5)	1		µs
I_{in}	"SL" and "SD" Input Current (6)		±1	**±64**	pA max
SR	Slew Rate (7)	A_V = +1, R_L = 10kΩ to V^+/2 V_I= $1V_{PP}$	1	0.8	V/µs min
f_u	Unity Gain-Bandwidth	V_I = 10mV, R_L = 2kΩ to V^+/2	750		KHz
GBW	Gain Bandwidth Product	f = 100KHz	1		MHz
e_n	Input-Referred Voltage Noise	f = 10KHz, R_S = 50Ω	36		nV/√Hz
i_n	Input-Referred Current Noise	f = 10KHz	1.5		fA/√Hz
THD	Total Harmonic Distortion	f = 1KHz, AV = +1, V_O = 2.2Vpp, R_L = 600Ω to V^+/2	0.18		%

(4) Short circuit test is a momentary test. Output short circuit duration is infinite for V_S < 6V. Otherwise, extended period output short circuit may damage the device.
(5) Shutdown Turn-on and Turn-off times are defined as the time required for the output to reach 90% and 10%, respectively, of its final peak to peak swing when set for Rail to Rail output swing with a 100KHz sine wave, 2KΩ load, and A_V = +10.
(6) Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.
(7) Slew rate is the slower of the rising and falling slew rates.

±5V Electrical Characteristics

Unless otherwise specified, all limits specified for T_J = 25°C, V^+ =5V, V^- = −5V, V_{CM} = V_O = 0V, and R_L > 1 MΩ to gnd. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (1)	Limit (2)	Units
V_{OS}	Input Offset Voltage		±0.7	±5 **±7**	mV max
TCV_{os}	Input Offset Voltage Average Drift		4		µV/°C
I_B	Input Bias Current	See (3)	±1	**±64**	pA max
I_{OS}	Input Offset Current		0.5	**32**	pA max
$R_{in\ CM}$	Input Common Mode Resistance		10		GΩ
$C_{in\ CM}$	Input Common Mode Capacitance		10		pF
CMRR	Common-Mode Rejection Ratio	−5V < = V_{CM} < = 5V	87	70 **67**	dB min
PSRR	Power Supply Rejection Ratio	V_S = 5V to 10V	80	76 **72**	dB min
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 50 dB	−5.3	−5.2 **−5.0**	V max
			5.3	5.2 **5.0**	V min

(1) Typical Values represent the most likely parametric norm.
(2) All limits are specified by testing or statistical analysis.
(3) Positive current corresponds to current flowing into the device.

±5V Electrical Characteristics (continued)

Unless otherwise specified, all limits specified for T_J = 25°C, V^+ =5V, V^- = −5V, V_{CM} = V_O = 0V, and R_L > 1 MΩ to gnd. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (1)	Limit (2)	Units
A_{VOL}	Large Signal Voltage Gain	Sourcing R_L = 600Ω V_O = 0V to 4V	34.5	17.8 **10**	V/mV min
		Sinking R_L = 600Ω V_O = 0V to −4V	34.5	17.8 **3.16**	
		Sourcing R_L = 2kΩ V_O = 0V to 4.6V	138	31.6 **17.8**	V/mV min
		Sinking R_L = 2kΩ V_O = 0V to −4.6V	138	31.6 **10**	
V_O	Output Swing High	R_L = 600Ω V_{ID} = 100mV	4.73	4.60 **4.54**	V min
		R_L = 2kΩ V_{ID} = 100mV	4.90	4.85 **4.83**	V min
	Output Swing Low	R_L = 600Ω V_{ID} = −100mV	−4.85	−4.75 **−4.65**	V max
		R_L = 2kΩ V_{ID} = −100mV	−4.95	4.90 **−4.84**	V max
I_{SC}	Output Short Circuit Current	Sourcing, V_{ID} = 100mV (4) (5)	49	30 **25**	mA min
		Sinking, V_{ID} = −100mV (4) (5)	90	60 **52**	mA min
I_S	Supply Current	No load, normal operation	1.1	1.7 **1.9**	mA max
		Shutdown mode	0.001	1	µA
T_{on}	Shutdown Turn-on time	See (6)	10	15	µs
T_{off}	Shutdown Turn-off time	See (6)	1		µs
I_{in}	"SL" and "SD" Input Current		±1	**±64**	pA max
SR	Slew Rate (7)	A_V = +10, R_L = 10kΩ, V_O = 10Vpp, C_L = 1000pF	1.2		V/µs
f_u	Unity Gain-Bandwidth	V_I = 10mV R_L = 2kΩ	840		KHz
GBW	Gain Bandwidth Product	f = 10KHz	1.3		MHz
e_n	Input-Referred Voltage Noise	f = 10KHz, R_s = 50Ω	33		nV/√Hz
i_n	Input-Referred Current Noise	f = 10KHz	1.5		fA/√Hz
THD	Total Harmonic Distortion	f = 10KHz, AV = +1, V_O =8Vpp, R_L = 600Ω	0.2		%

(4) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature at 150°C. Output currents in excess of 40mA over long term may adversely affect reliability.
(5) Short circuit test is a momentary test. Output short circuit duration is infinite for V_S < 6V. Otherwise, extended period output short circuit may damage the device.
(6) Shutdown Turn-on and Turn-off times are defined as the time required for the output to reach 90% and 10%, respectively, of its final peak to peak swing when set for Rail to Rail output swing with a 100KHz sine wave, 2KΩ load, and A_V = +10.
(7) Slew rate is the slower of the rising and falling slew rates.

Typical Performance Characteristics

V_S = 2.7V, Single Supply, V_{CM} = V^+/2, T_A = 25°C unless specified

Gain/Phase vs. Frequency (R_L = 2k, V_S = ± 1.35V)

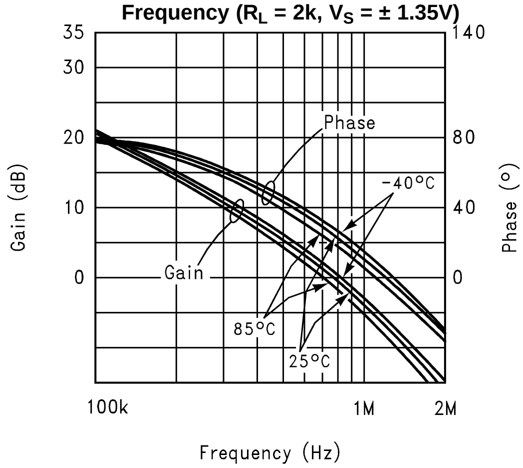

Figure 3.

Gain/Phase vs. Frequency (R_L = 2k, V_S = ± 5V)

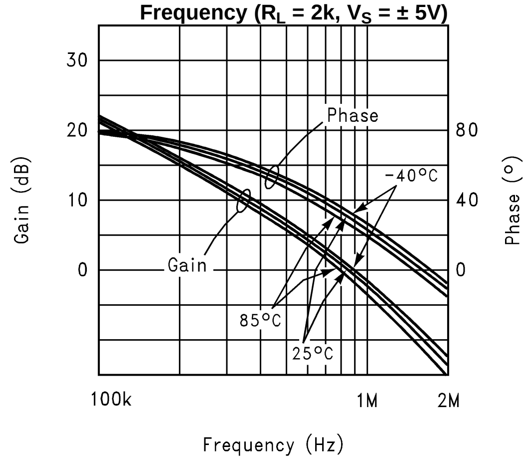

Figure 4.

Gain/Phase vs. Frequency (R_L = Open)

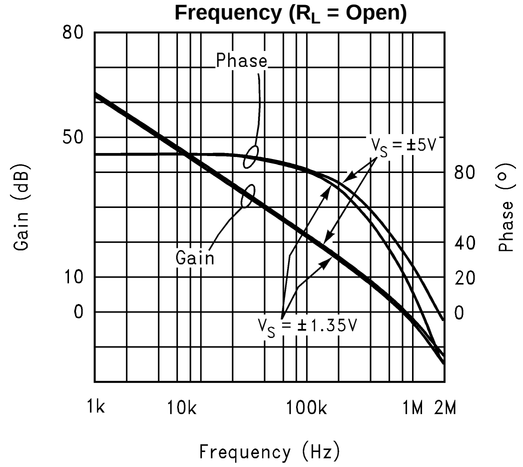

Figure 5.

Gain vs. Phase for various C_L V_S = ±1.35V

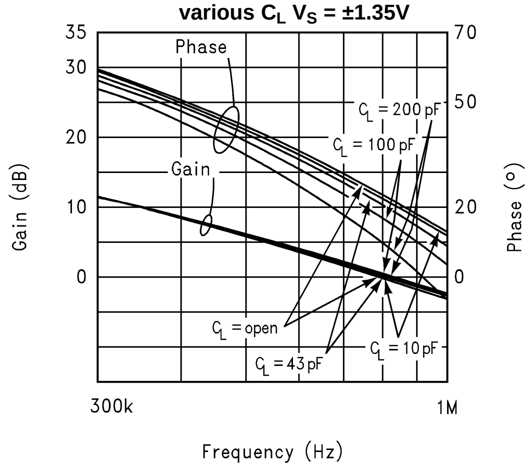

Figure 6.

Unity Gain Frequency vs. Supply Voltage

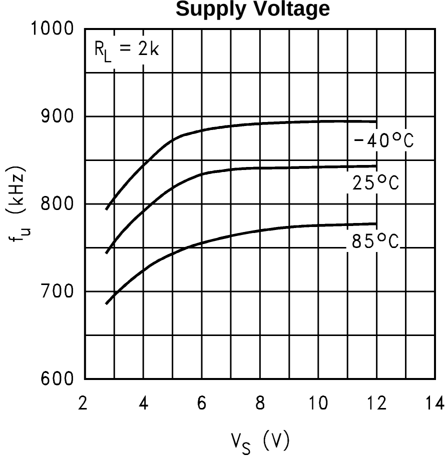

Figure 7.

Phase Margin vs. Supply Voltage

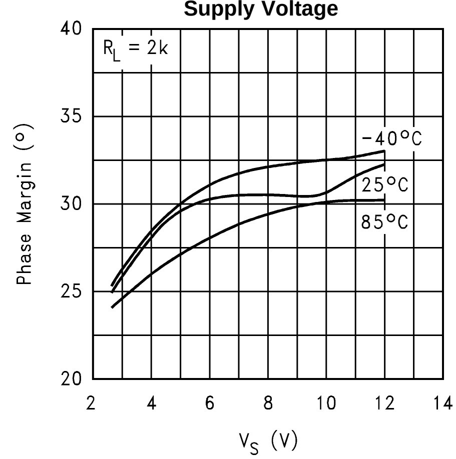

Figure 8.

Typical Performance Characteristics (continued)

V_S = 2.7V, Single Supply, V_{CM} = $V^+/2$, T_A = 25°C unless specified

Unity Gain Frequency and Phase Margin vs. Load

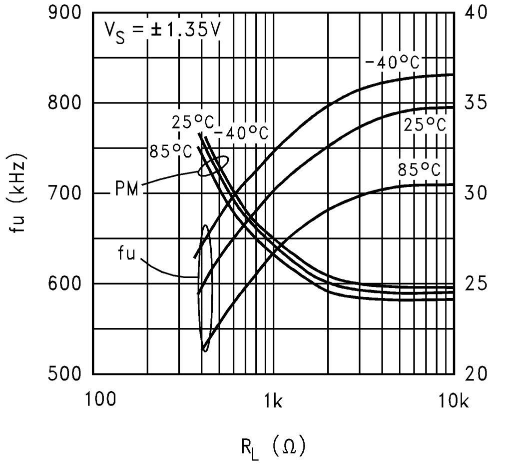

Figure 9.

Unity Gain Frequency and Phase Margin vs. Load

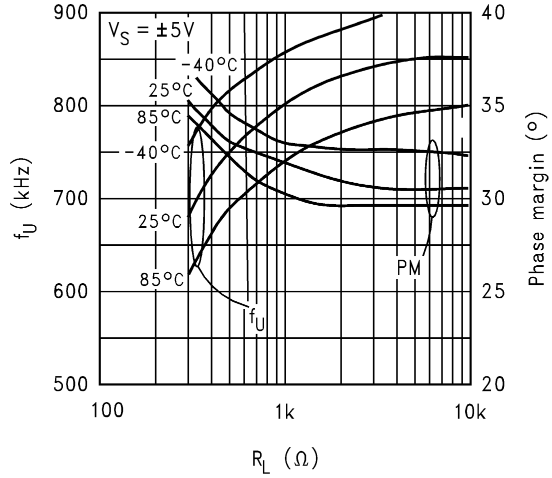

Figure 10.

PSRR vs. Frequency

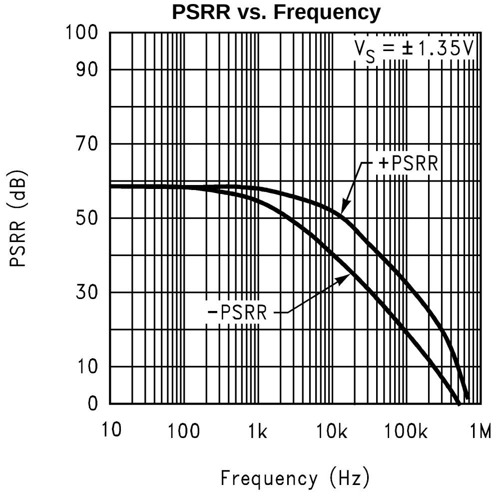

Figure 11.

PSRR vs. Frequency

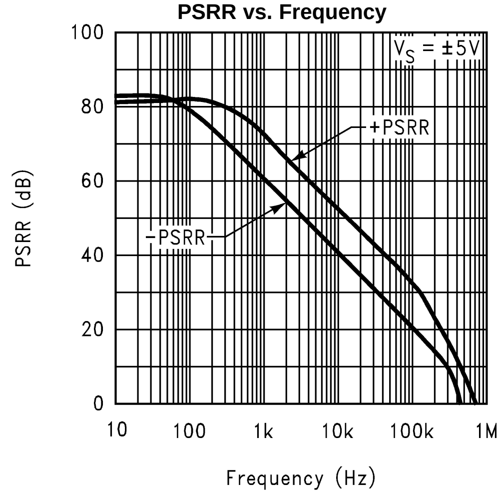

Figure 12.

CMRR vs. Frequency

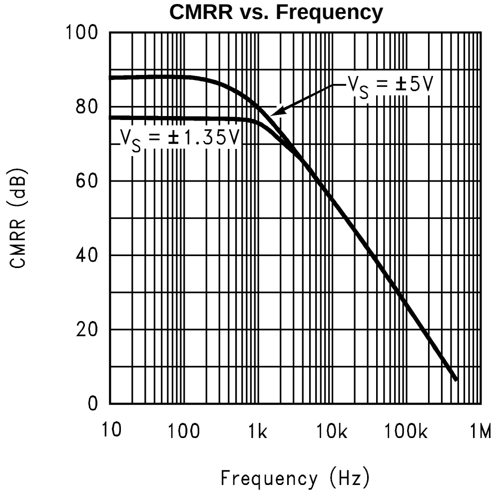

Figure 13.

Input Bias Current vs. Common Mode Voltage @ 85°C

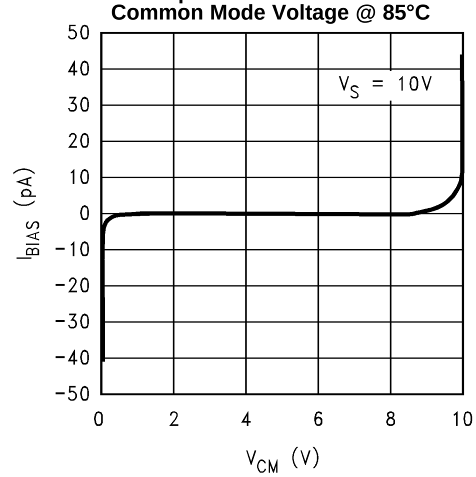

Figure 14.

Typical Performance Characteristics (continued)

V_S = 2.7V, Single Supply, V_{CM} = V^+/2, T_A = 25°C unless specified

Input Current vs. Temperature V_S = 10V

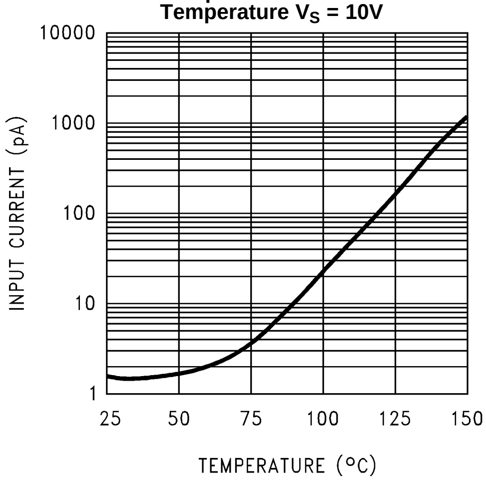

Figure 15.

V_{IN} vs. V_{OUT}

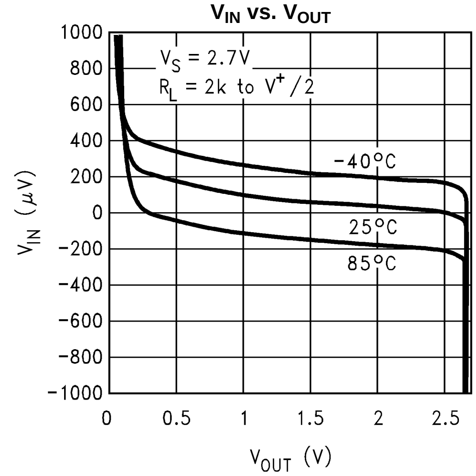

Figure 16.

V_{IN} vs. V_{OUT}

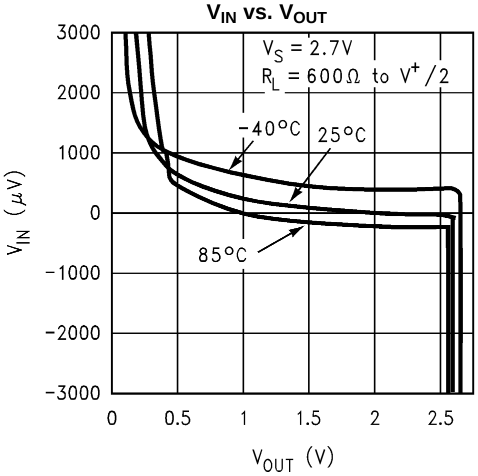

Figure 17.

V_{IN} vs. V_{OUT}

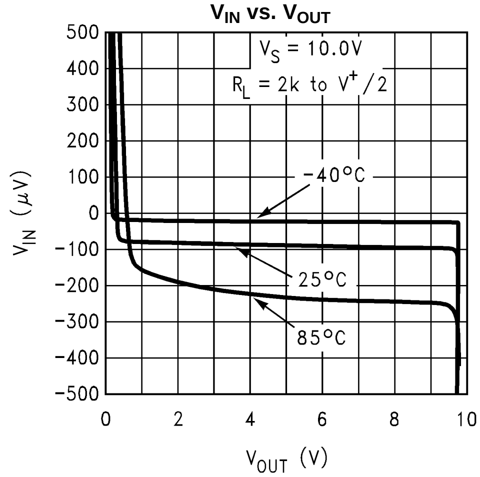

Figure 18.

V_{IN} vs. V_{OUT}

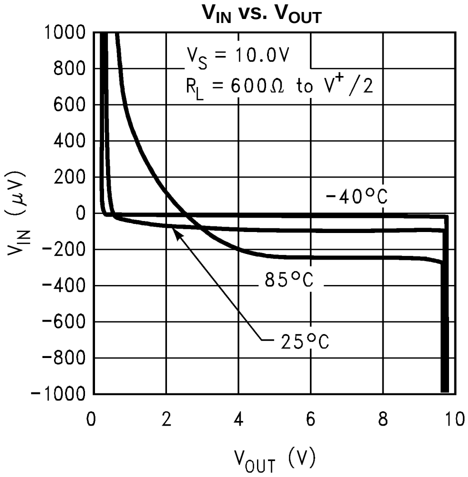

Figure 19.

Supply Current vs. Supply Voltage

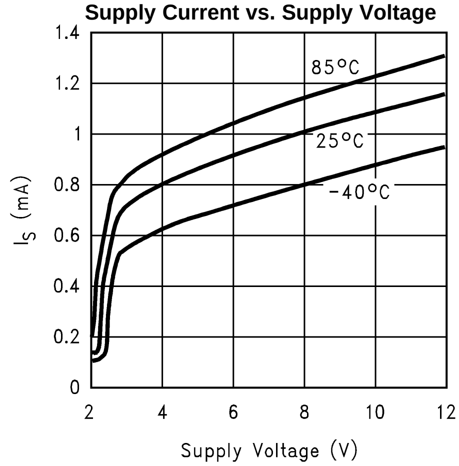

Figure 20.

Typical Performance Characteristics (continued)

V_S = 2.7V, Single Supply, V_{CM} = V^+/2, T_A = 25°C unless specified

Delta V_{OS} vs. V_{CM} (Ref V_{CM} = 1.35V)

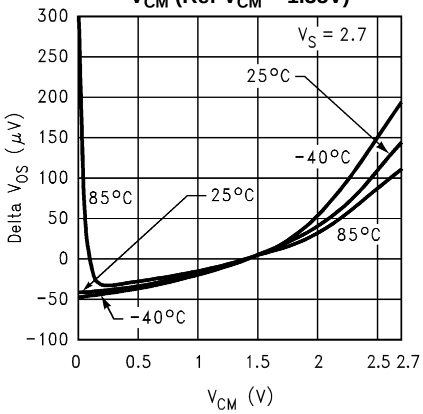

Figure 21.

Delta V_{OS} vs. V_{CM} (Ref V_{CM} = 5V)

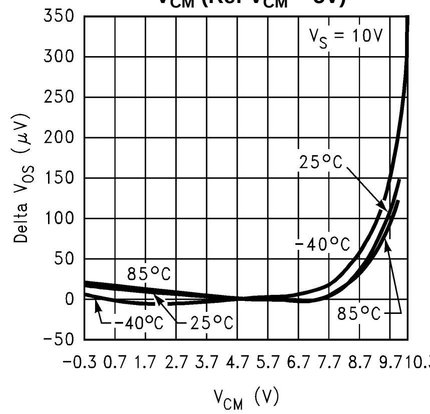

Figure 22.

Offset Voltage vs. V_{SUPPLY}

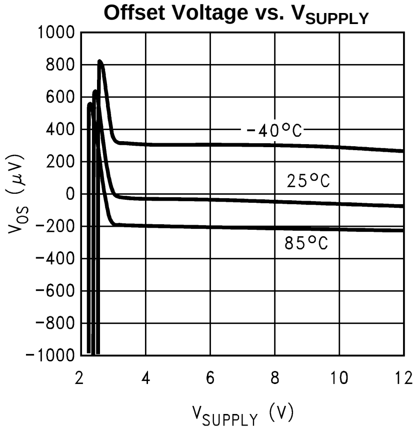

Figure 23.

Output Positive Swing vs. Supply Voltage R_L = 600Ω to V^+/2

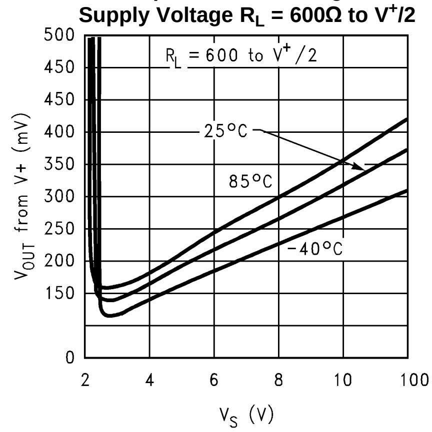

Figure 24.

Output Positive Swing vs. Supply Voltage R_L = 2k to V^+/2

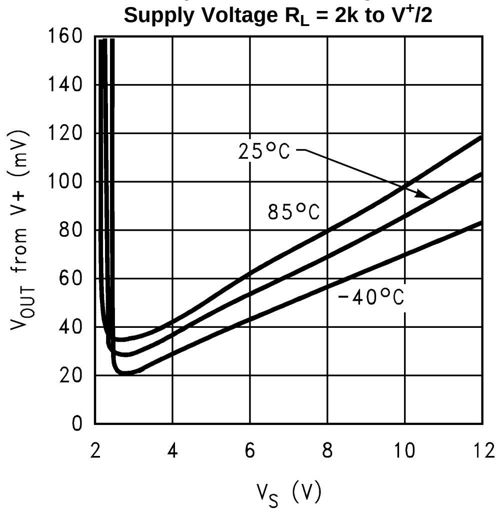

Figure 25.

Output Negative Swing vs. Supply Voltage R_L = 600Ω to V^+/2

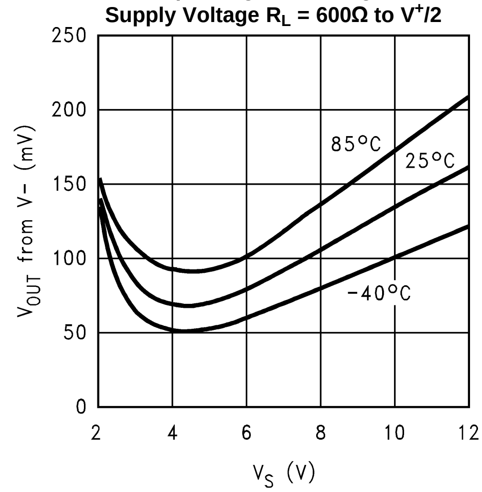

Figure 26.

Typical Performance Characteristics (continued)

V_S = 2.7V, Single Supply, V_{CM} = $V^+/2$, T_A = 25°C unless specified

Output Negative Swing vs. Supply Voltage, R_L = 2k to $V^+/2$

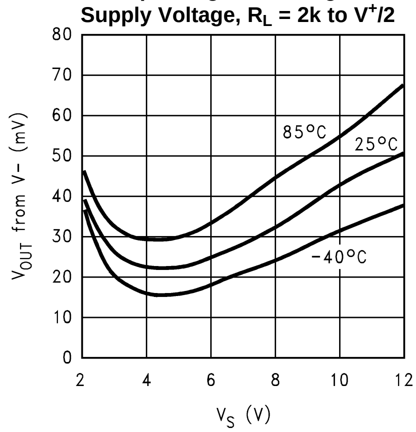

Figure 27.

Short Circuit Sinking Current vs. Supply Voltage

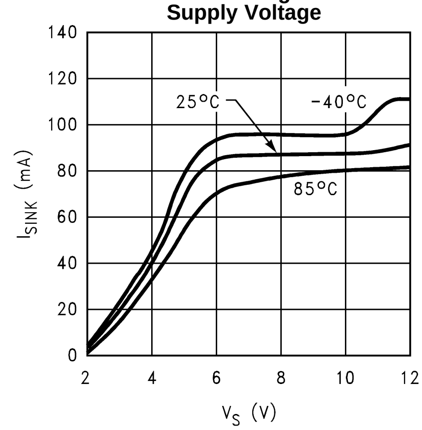

Figure 28.

Short Circuit Sourcing Current vs. Supply Voltage

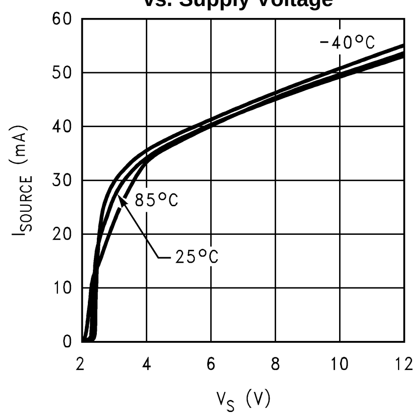

Figure 29.

Undistorted Output Voltage Swing vs. Output Load Resistance

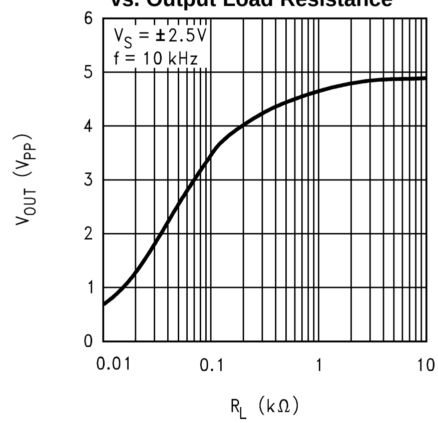

Figure 30.

Step Response 1% settling time and % overshoot vs. Cap Load

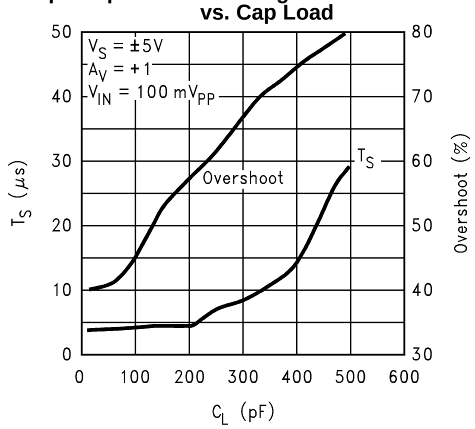

Figure 31.

Large Signal Step Response

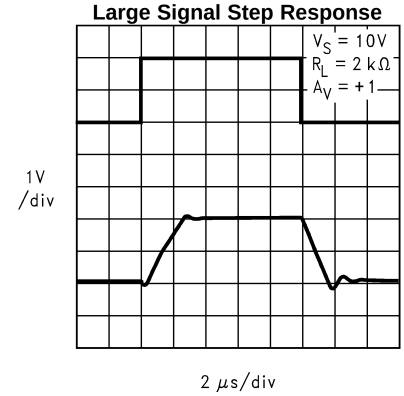

Figure 32.

Typical Performance Characteristics (continued)

V_S = 2.7V, Single Supply, V_{CM} = V^+/2, T_A = 25°C unless specified

Small Signal Step Response

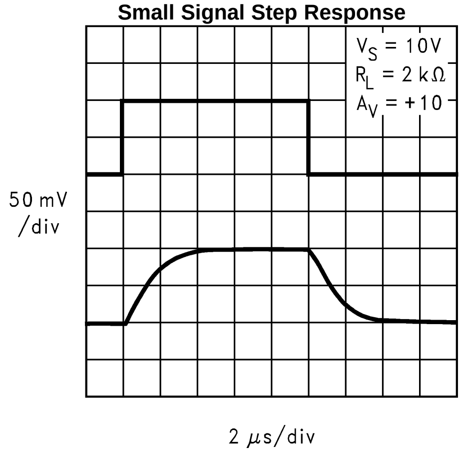

Figure 33.

Large Signal Step Response

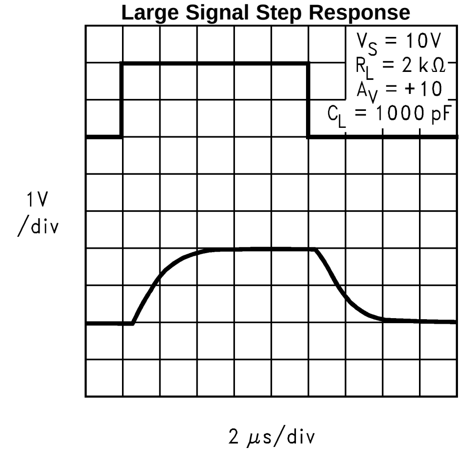

Figure 34.

Small Signal Step Response

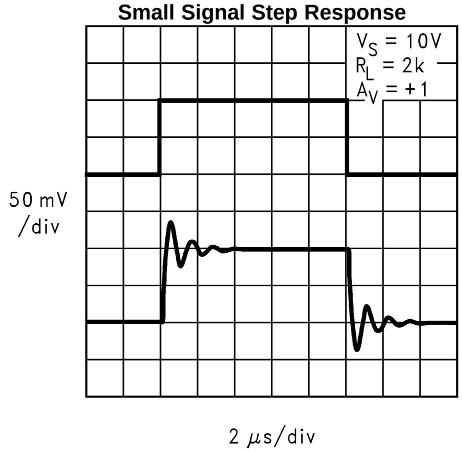

Figure 35.

Small Signal Step Response

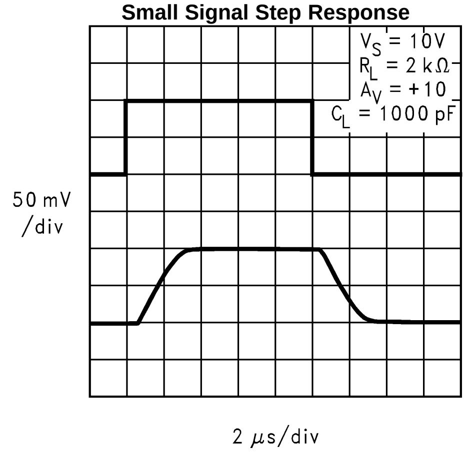

Figure 36.

Large Signal Step Response

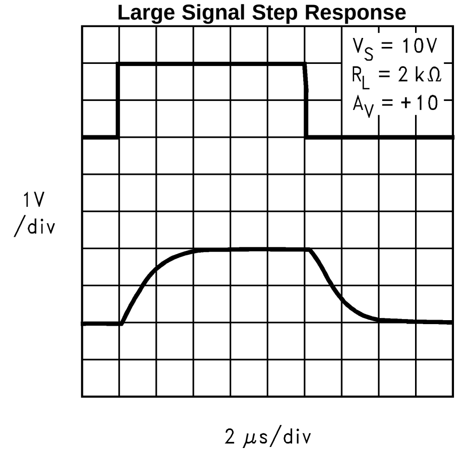

Figure 37.

Large Signal Step Response

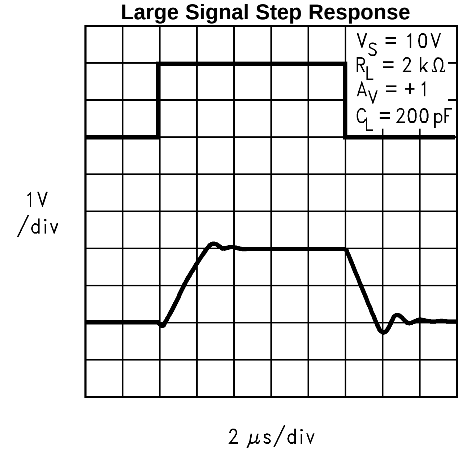

Figure 38.

Typical Performance Characteristics (continued)

V_S = 2.7V, Single Supply, V_{CM} = $V^+/2$, T_A = 25°C unless specified

Small Signal Step Response

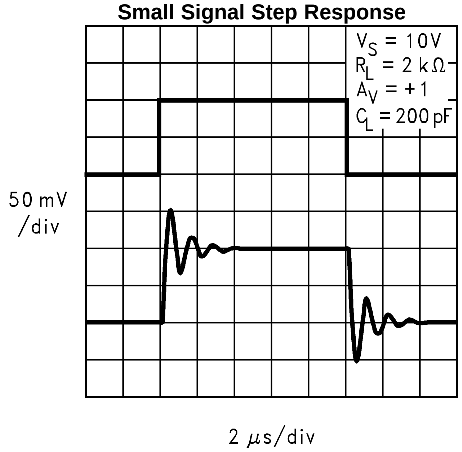

Figure 39.

Slew Rate vs. Supply Voltage

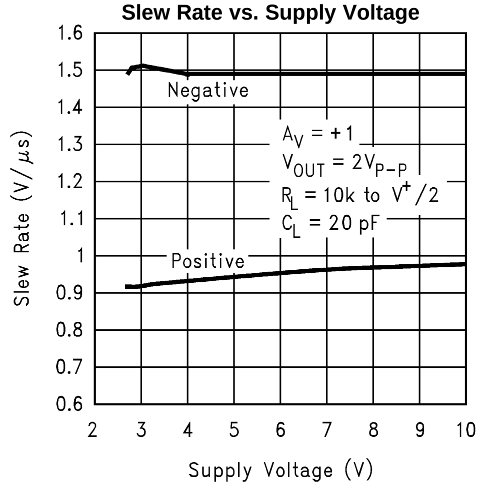

Figure 40.

Slew Rate vs. Capacitive Load

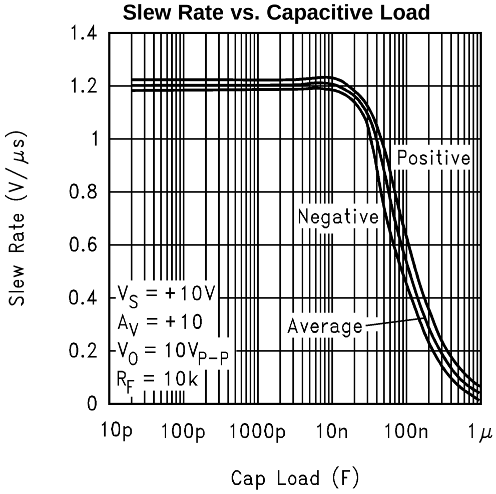

Figure 41.

Slew Rate vs. Capacitive Load

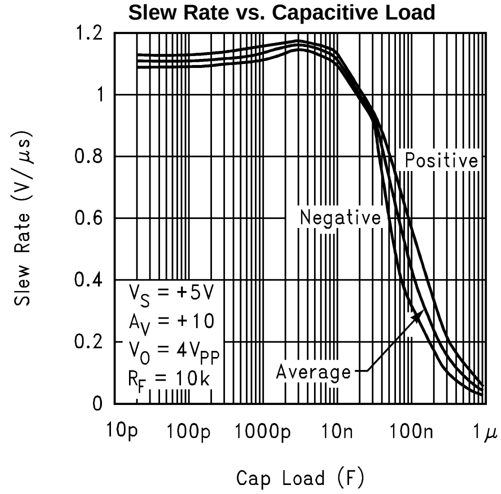

Figure 42.

Slew Rate vs. Capacitive Load

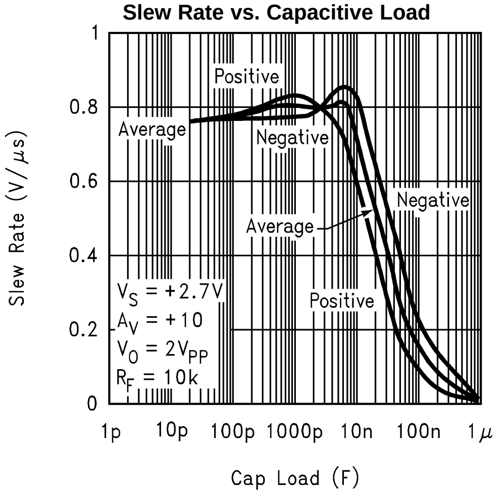

Figure 43.

Slew Rate vs. Capacitive Load

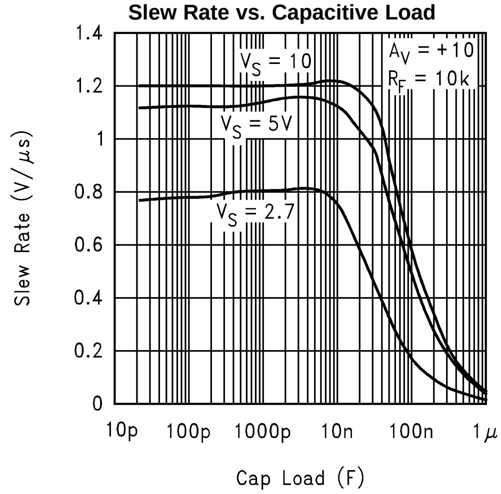

Figure 44.

Typical Performance Characteristics (continued)

V_S = 2.7V, Single Supply, V_{CM} = $V^+/2$, T_A = 25°C unless specified

Voltage Noise vs. Frequency

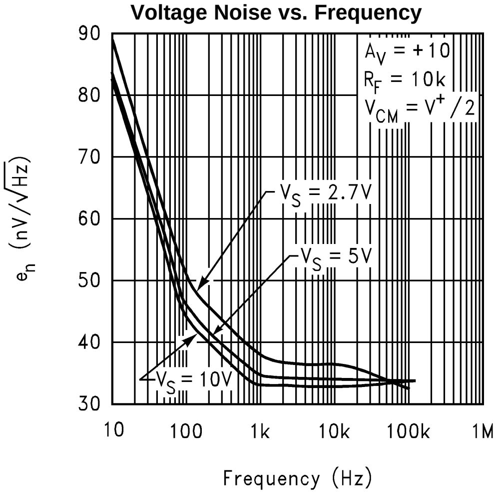

Figure 45.

Voltage Noise vs. V_{CM} @ Various Frequencies

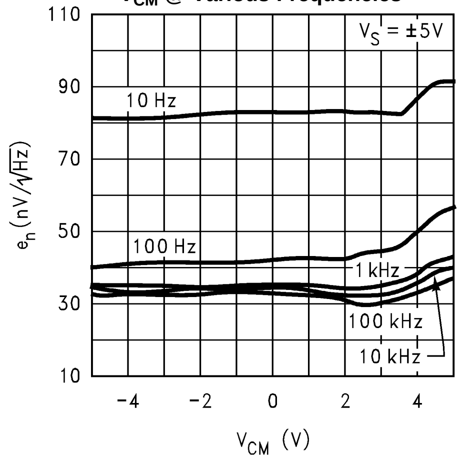

Figure 46.

THD+N vs. Amplitude

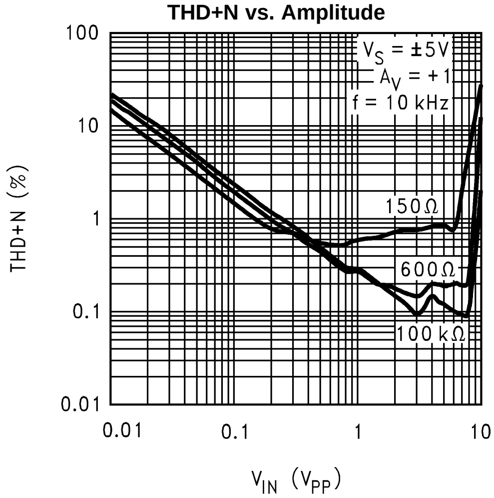

Figure 47.

THD+N vs. Frequency

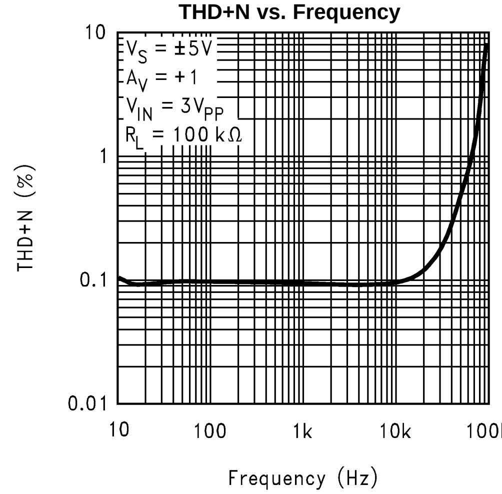

Figure 48.

Sourcing Current vs. Output Voltage (V_S = 2.7V)

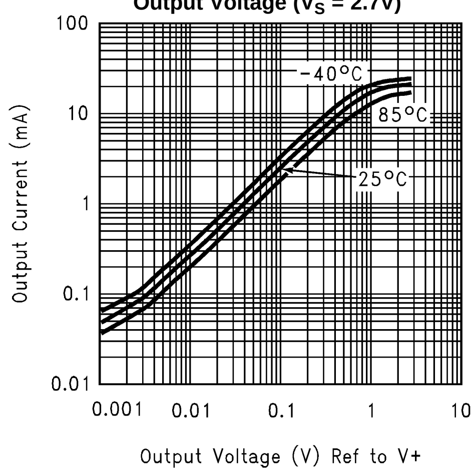

Figure 49.

Sinking Current vs. Output Voltage (V_S = 2.7V)

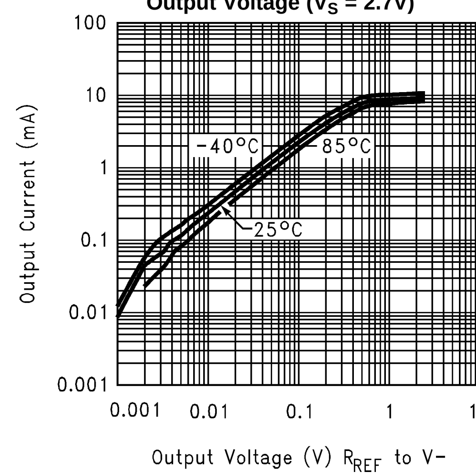

Figure 50.

Typical Performance Characteristics (continued)

V_S = 2.7V, Single Supply, V_{CM} = V^+/2, T_A = 25°C unless specified

Sourcing Current vs. Output Voltage (V_S = 10V)

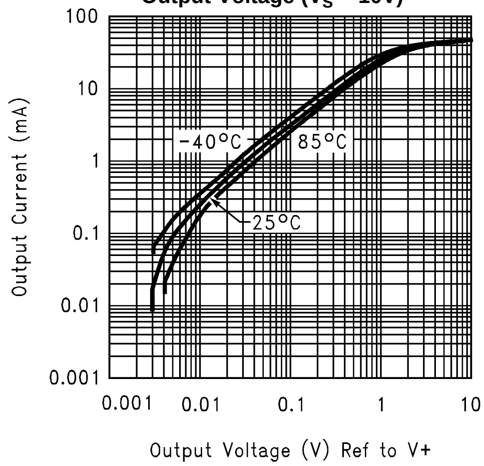

Figure 51.

Sinking Current vs. Output Voltage (V_S = 10V)

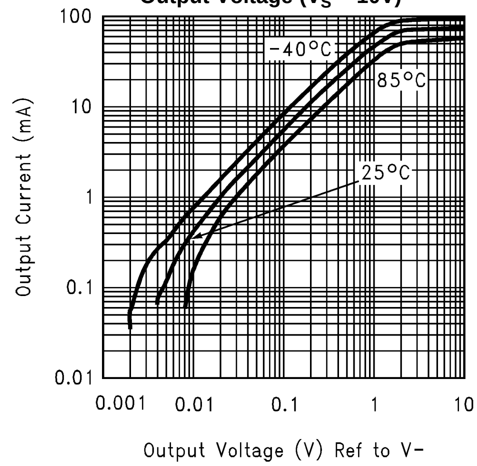

Figure 52.

Cap Load vs. I_{OUT}

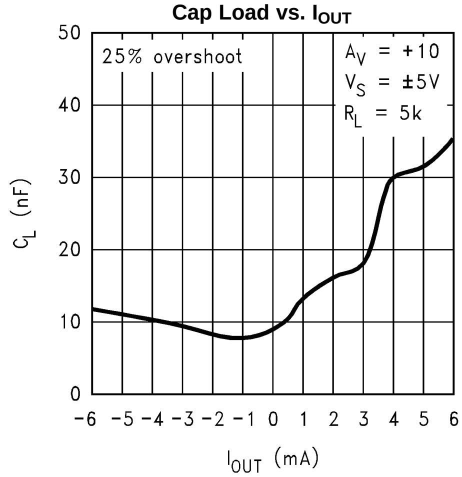

Figure 53.

Cap Load vs. Isolation Resistance

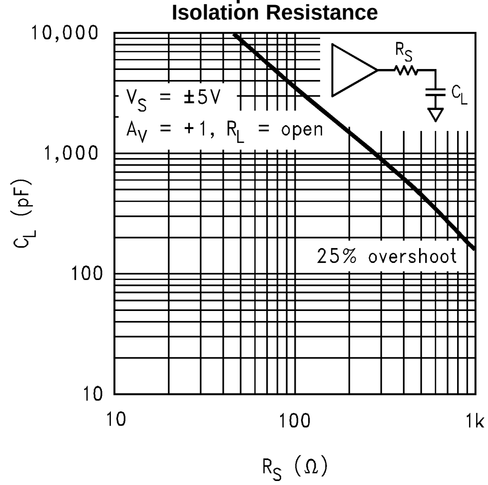

Figure 54.

APPLICATION NOTES

SHUTDOWN FEATURES

The LMC8101 is capable of being turned off in order to conserve power. Once in shutdown, the device supply current is drastically reduced (1µA maximum) and the output will be "Tri-stated".

The shutdown feature of the LMC8101 is designed for flexibility. The threshold level of the SD input can be referenced to either V^-or V^+ by setting the level on the SL input. When the SL input is connected to V^-, the SD threshold level is referenced to $V^-$and vice versa. This threshold will be about 1.5V from the supply tied to the SL pin. So, for this example, the device will be in shutdown as long as the SD pin voltage is within 1V of V^-. In order to ensure that the device would not "chatter" between active and shutdown states, hysteresis is built into the SD pin transition (see Figure 55 for an illustration of this feature). The shutdown threshold and hysteresis level are independent of the supply voltage. Figure 55 illustration applies equally well to the case when SL is tied to V^+ and the horizontal axis is referenced to V^+ instead. The SD pin should not be set within the voltage range from 1.1V to 1.9V of the selected supply voltage since this is a transition region and the device status will be undetermined.

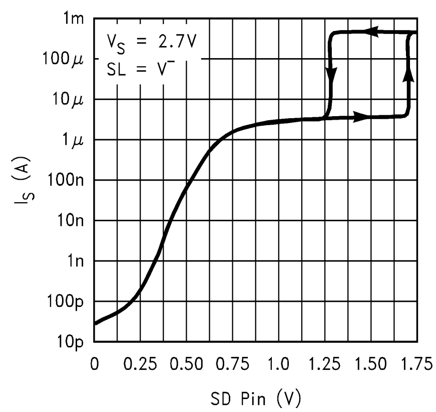

Figure 55. Supply Current vs. "SD" Voltage

Table 1 summarizes the status of the device when the SL and SD pins are connected directly to V^-or V^+:

Table 1. LMC8101 Status Summary

SL	SD	LMC8101 Status
V^-	V^-	Shutdown
V^-	V^+	Active
V^+	V^+	Shutdown
V^+	V^-	Active

In case shutdown operation is not needed, as can be seen above, the two pins SL and SD can simply be connected to opposite supply nodes to achieve "Active" operation. The SL and SD should always be tied to a node; if left unconnected, these high impedance inputs will float to an undetermined state and the device status will be undetermined as well.

With the device in shutdown, once "Active" operation is initiated, there will be a finite amount of time required before the device output is settled to its final value. This time is less than 15µs. In addition, there may be some output spike during this time while the device is transitioning into a fully operational state. Some applications may be sensitive to this output spike and proper precautions should be taken in order to ensure proper operation at all times.

TINY PACKAGE

The LMC8101 is available in the DSBGA package as well the 8 pin VSSOP package. The DSBGA package requires approximately 1/4 the board area of a SOT-23. This package is less than 1mm in height allowing it to be placed in absolute minimum height clearance areas such as cellular handsets, LCD panels, PCMCIA cards, etc. More information about the DSBGA package can be found at: http://www.ti.com/packaing.

CONVERSION BOARDS

In order to ease the evaluation of tiny packages such as the DSBGA, there is a conversion board (LMC8101CONV) available to board designers. This board converts a DSBGA device into an 8 pin DIP package (see Figure 56) for easier handling and evaluation. This board can be ordered from Texas Instruments by contacting http://www.ti.com.

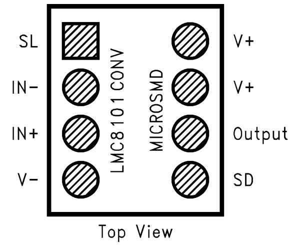

Figure 56. DSBGA Conversion Board pin-out

INCREASED OUTPUT CURRENT

Compared to the LMC7101, the LMC8101 has an improved output stage capable of up to three times larger output sourcing and sinking current. This improvement would allow a larger output voltage swing range compared to the LMC7101 when connected to relatively heavy loads. For lower supply voltages this is an added benefit since it increases the output swing range. For example, the LMC8101 can typically swing 2.5Vpp with 2mA sourcing and sinking output current (Vs = 2.7V) whereas the LMC7101 output swing would be limited to 1.9Vpp under the same conditions. Also, compared to the LMC7101 in the SOT-23 package, the LMC8101 can dissipate more power because both the VSSOP and the DSBGA packages have 40% better heat dissipation capability.

LOWER 1/f NOISE

The dominant input referred noise term for the LMC8101 is the input noise voltage. Input noise current for this device is of no practical significance unless the equivalent resistance it looks into is 5MΩ or higher.

The LMC8101's low frequency noise is significantly lower than that of the LMC7101. For example, at 10Hz, the input referred spot noise voltage density is 85 $nV\sqrt{Hz}$ as compared to about 200$nV\sqrt{Hz}$ for the LMC7101. Over a frequency range of 0.1Hz to 100Hz, the total noise of the LMC8101 will be approximately 60% less than that of the LMC7101.

LOWER THD

When connected to heavier loads, the LMC8101 has lower THD compared to the LMC7101. For example, with 5V supply at 10KHz and 2Vpp swing (Av = −2), the LMC8101 THD (0.2%) is 60% less than the LMC7101's. The LMC8101 THD can be kept below 0.1% with 3Vpp at the output for up to 10KHz (refer to the Typical Performance Characteristics plots).

IMPROVING THE CAP LOAD DRIVE CAPABILITY

This can be accomplished in several ways:

- Output resistive loading increase:

The Phase Margin increases with increasing load (refer to the Typical Performance Characteristics plots). When driving capacitive loads, stability can generally be improved by allowing some output current to flow through a load. For example, the cap load drive capability can be increased from 8200pF to 16000pF if the output load is increased from 5kΩ to 600Ω (A_V = +10, 25% overshoot limit, 10V supply).

- Isolation resistor between output and cap load:

This resistor will isolate the feedback path (where excessive phase shift due to output capacitance can cause instability) from the capacitive load. With a 10V supply, a 100Ω isolation resistor allows unlimited capacitive load without oscillation compared to only 300pF without this resistor (A_V = +1).

- Higher supply voltage:

Operating the LMC8101 at higher supply voltages allows higher cap load tolerance. At 10V, the LMC8101's low supply voltage cap load limit of 300pF improves to about 600pF (A_V = +1).

- Closed loop gain increase:

As with all Op Amps, the capacitive load tolerance of the LMC8101 increases with increasing closed loop gain. In applications where the load is mostly capacitive and the resistive loading is light, stability increases when the LMC8101 is operated at a closed loop gain larger than +1.

REVISION HISTORY

Changes from Revision E (March 2013) to Revision F	Page
• Changed layout of National Data Sheet to TI format	17

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMC8101TP/NOPB	Active	Production	DSBGA (YPB) | 8	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	A 08
LMC8101TP/NOPB.A	Active	Production	DSBGA (YPB) | 8	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	A 08
LMC8101TP/NOPB.B	Active	Production	DSBGA (YPB) | 8	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	A 08
LMC8101TPX/NOPB	Active	Production	DSBGA (YPB) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	A 08
LMC8101TPX/NOPB.A	Active	Production	DSBGA (YPB) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	A 08
LMC8101TPX/NOPB.B	Active	Production	DSBGA (YPB) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	A 08

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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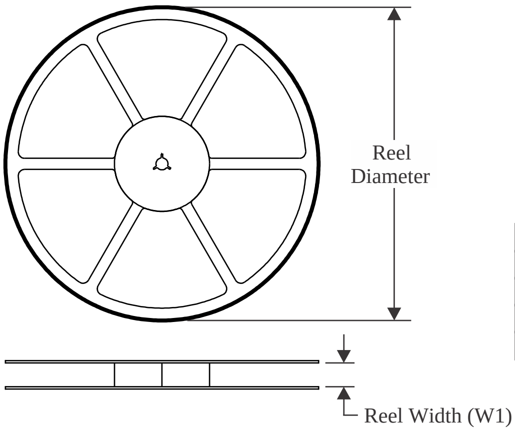
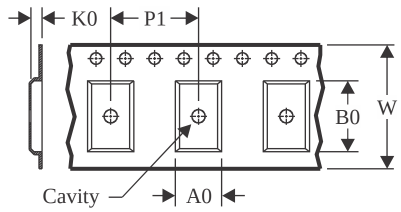
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

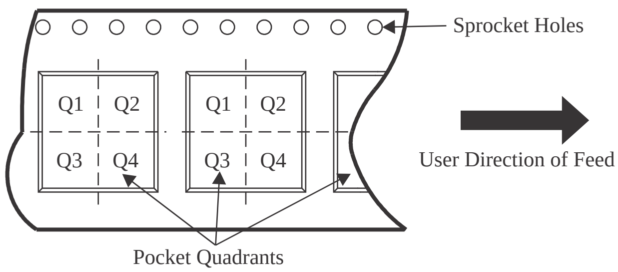


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

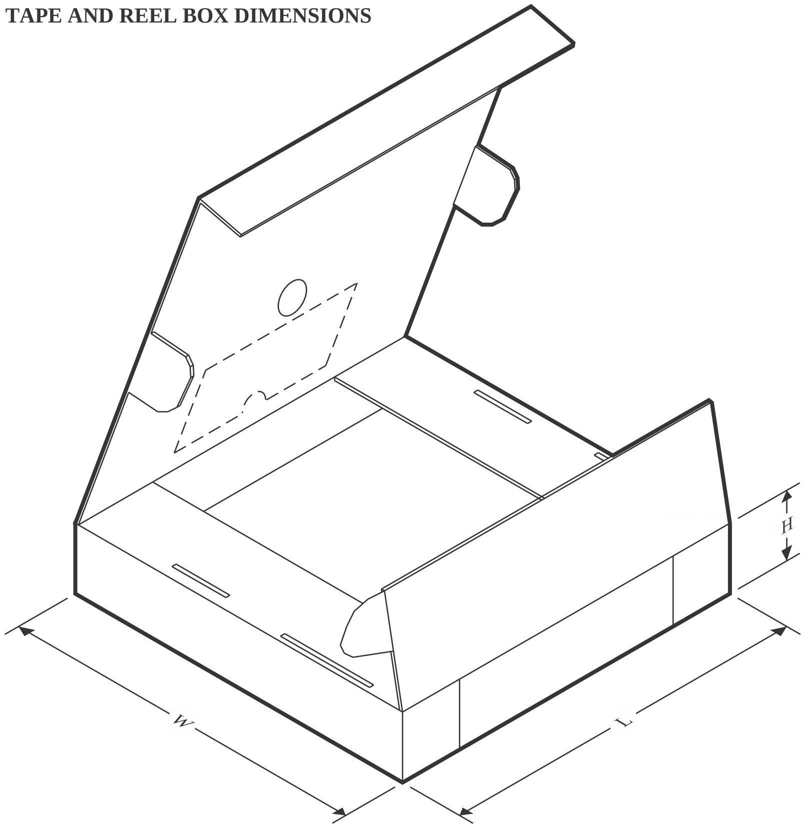
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

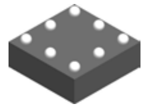
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC8101TP/NOPB	DSBGA	YPB	8	250	178.0	8.4	1.57	1.57	0.76	4.0	8.0	Q1
LMC8101TPX/NOPB	DSBGA	YPB	8	3000	178.0	8.4	1.57	1.57	0.76	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

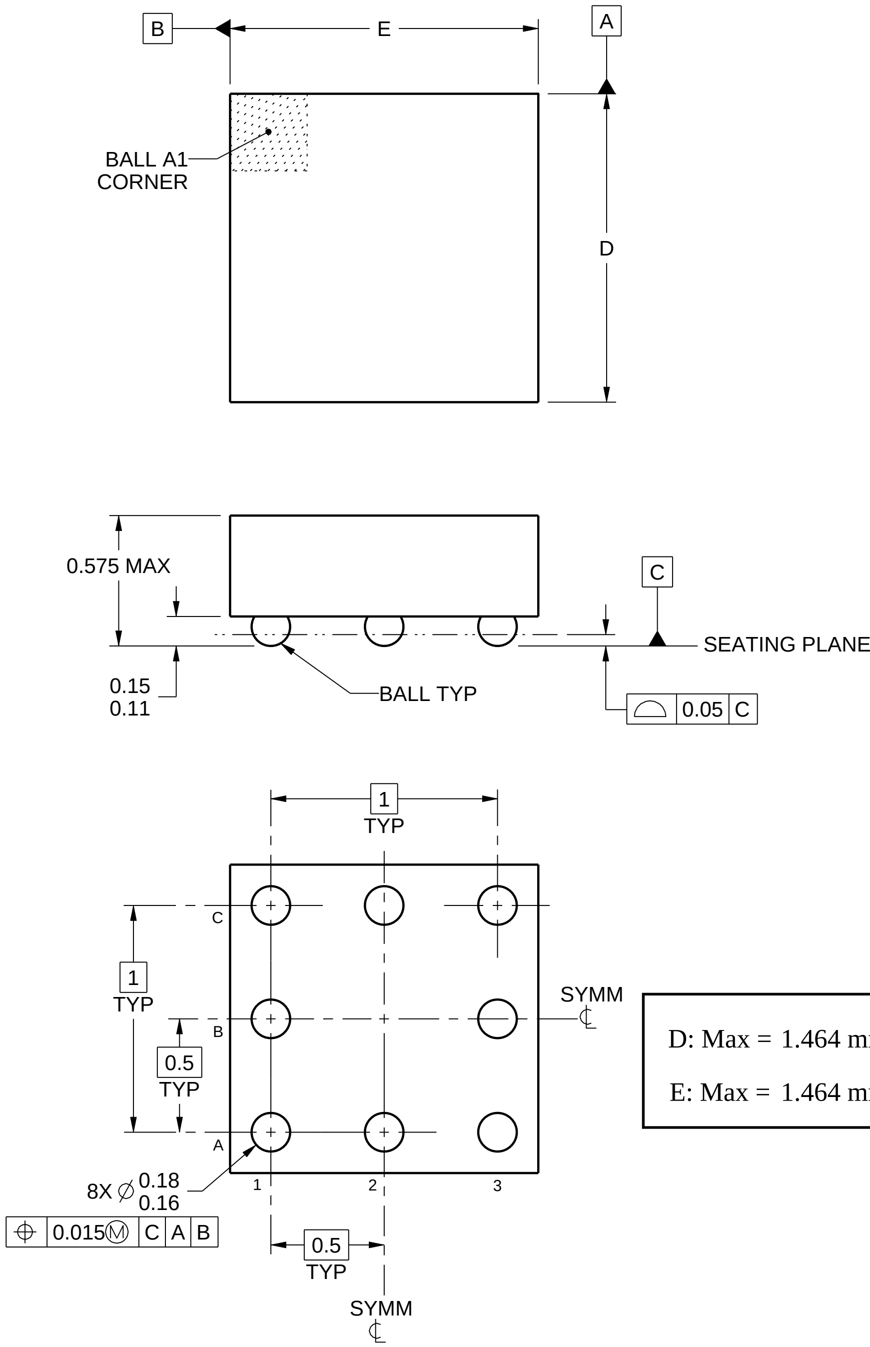
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC8101TP/NOPB	DSBGA	YPB	8	250	208.0	191.0	35.0
LMC8101TPX/NOPB	DSBGA	YPB	8	3000	208.0	191.0	35.0



PACKAGE OUTLINE

DSBGA - 0.575 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.464 mm, Min =1.403 mm

E: Max = 1.464 mm, Min =1.403 mm

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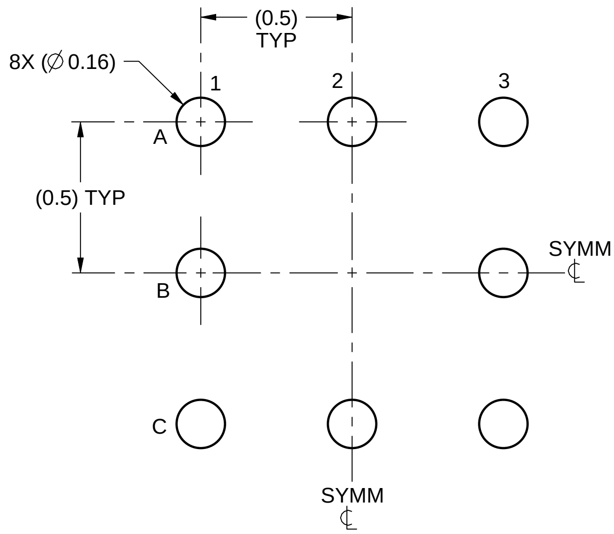
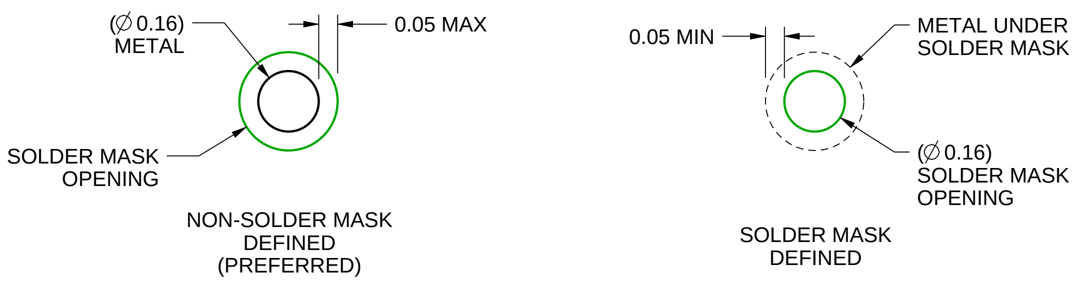
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

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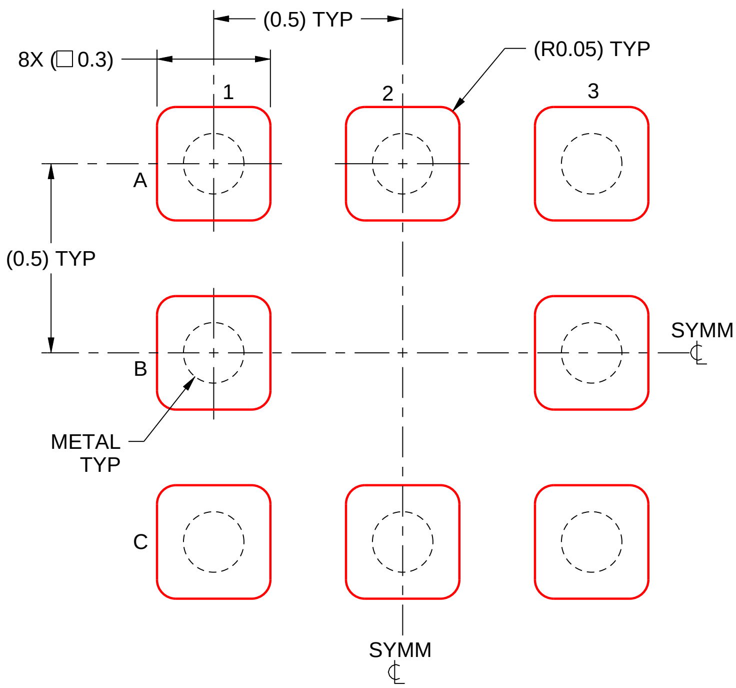
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.125mm THICK STENCIL
SCALE:50X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265