LMC648x CMOS Rail-to-Rail Input and Output Operational Amplifiers

1 Features

- Rail-to-rail input common-mode voltage range (specified over temperature)
- Rail-to-rail output swing (within 20mV of supply rail, 100kΩ load)
- Specified 3V, 5V, and 15V performance
- Excellent CMRR and PSRR: 82dB
- Ultra-low input current: 20fA
- Specified for 2kΩ and 600Ω loads
- Improved replacement for TLC272, TLC277

2 Applications

- Data acquisition (DAQ)
- Currency counter
- Oscilloscope (DSO)
- Intra-DC interconnect (METRO)
- Macro remote radio unit (RRU)
- Multiparameter patient monitor
- Merchant telecom rectifiers
- Train control and management
- Process analytics (pH, gas, concentration, force, and humidity)
- Three phase UPS

3 Description

The LMC6482 and LMC6484 (LMC648x) devices provide a common-mode range that extends to both supply rails. This rail-to-rail performance combined with excellent accuracy, due to a high CMRR, makes these devices unique among rail-to-rail input amplifiers. The devices are an excellent choice for systems that require a large input signal range, such as data acquisition. The LMC648x are also an excellent upgrade for circuits using limited common-mode range amplifiers, such as the TLC272, TLC274, TLC277 and TLC279.

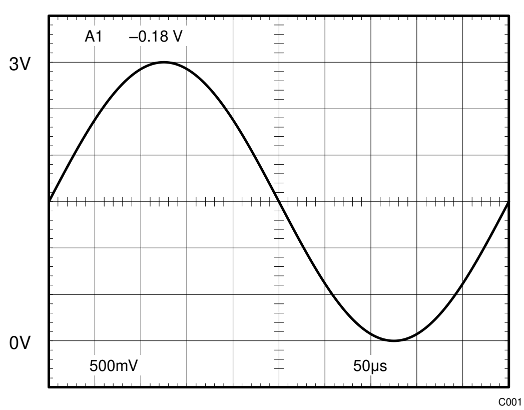
Maximum dynamic signal range is provided in low voltage and single supply systems by the rail-to-rail output swing of the LMC648x. The rail-to-rail output swing is maintained for loads down to 600Ω of the device. Specified low-voltage characteristics and low-power dissipation make the LMC648x a great choice for battery-operated systems.

The LMC648x devices are available in PDIP, SOIC, and VSSOP packages.

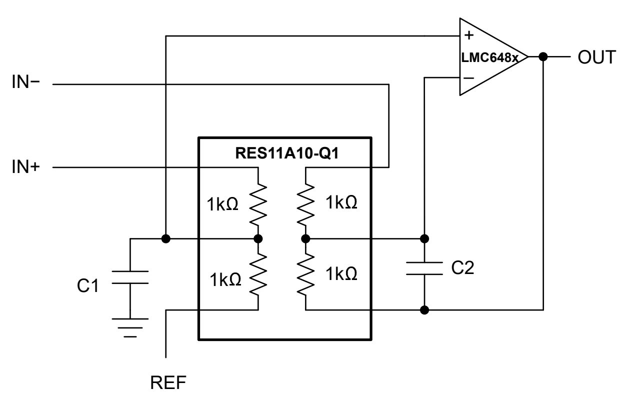
Device Information

PART NUMBER	CHANNEL COUNT	PACKAGE(1)
LMC6482	Dual	D (SOIC, 8)
		DGK (VSSOP, 8)
		P (PDIP, 8)
LMC6484	Quad	D (SOIC, 14)
		N (PDIP, 14)

(1) For more information, see Section 10.



Rail-to-Rail Input (V_S = 3V)



Unity-Gain Difference Amplifier

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4 Pin Configuration and Functions

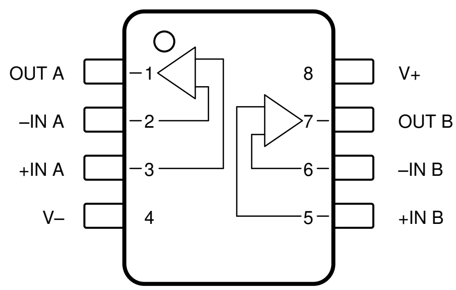


Figure 4-1. LMC6482: D Package, 8-Pin SIOIC, DGK Package, 8-Pin VSSOP, and P Package, 8-pin PDIP (Top View)

Table 4-1. Pin Functions: LMC6482

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	OUT A	Output	Output for amplifier A
2	−IN A	Input	Inverting input for amplifier A
3	+IN A	Input	Noninverting input for amplifier A
4	V–	Power	Negative supply voltage input
5	+IN B	Input	Noninverting input for amplifier B
6	−IN B	Input	Inverting input for amplifier B
7	OUT B	Output	Output for amplifier B
8	V+	Power	Positive supply voltage input

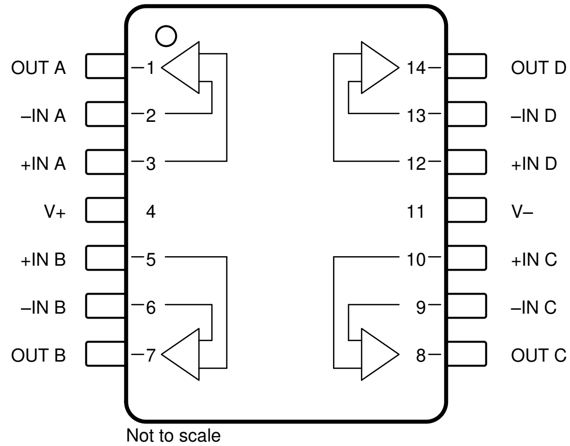


Figure 4-2. LMC6484: D Package, 14-Pin SOIC, and N Package, 14-Pin PDIP (Top View)

Table 4-2. Pin Functions: LMC6484

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	OUT A	Output	Output for amplifier A
2	−IN A	Input	Inverting input for amplifier A
3	+IN A	Input	Noninverting input for amplifier A
4	V+	Power	Positive supply voltage input
5	+IN B	Input	Noninverting input for amplifier B
6	−IN B	Input	Inverting input for amplifier B
7	OUT B	Output	Output for amplifier B
8	OUT C	Output	Output for amplifier C
9	−IN C	Input	Inverting input for amplifier C
10	+IN C	Input	Noninverting input for amplifier C
11	V–	Power	Negative supply voltage input
12	+IN C	Input	Inverting input for amplifier D
13	+IN C	Input	Noninverting input for amplifier D
14	OUT C	Output	Output for amplifier D

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)] [(2)]

		MIN	MAX	UNIT
	Differential input voltage		±Supply Voltage	
	Voltage at input/output pin	(V–) – 0.3	(V+) + 0.3	V
V_S	Supply voltage, V_S = (V+) – (V–)		16	V
	Current at input pin[(3)]	–5	5	mA
	Current at output pin[(4)] [(5)]	–30	30	mA
	Current at power supply pin		40	mA
T_J	Junction temperature[(6)]		150	°C
T_{STG}	Storage temperature	–65	150	°C
	Lead temperature (soldering, 10 sec)		260	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) If military- or aerospace-specified devices are required, contact the TI Sales Office or Distributors for availability and specifications.
(3) Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.
(4) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30mA over a long term can adversely affect reliability.
(5) Do not short circuit output to V+, when V+ is greater than 13V or reliability is adversely affected.
(6) The maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A) / \theta_{JA}$. All numbers apply for packages soldered directly into a printed circuit board (PCB).

5.2 ESD Ratings

			VALUE	UNIT
LMC6482				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±1500	V
LMC6484				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	3		15.5	V
T_J	Junction temperature	–40		85	℃

5.4 Thermal Information LMC6482

THERMAL METRIC[(1)]		LMC6482			UNIT
		D (SOIC)	DGK (VSSOP)	P (PDIP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	128.9	169.5	76.2	ºC/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	68.6	60.9	65.6	ºC/W
$R_{\theta JB}$	Junction-to-board thermal resistance	72.4	91.2	52.7	ºC/W
Ψ_{JT}	Junction-to-top characterization parameter	19.7	8.3	35.3	ºC/W
Ψ_{JB}	Junction-to-board characterization parameter	71.6	89.6	52.2	ºC/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	N/A	ºC/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Thermal Information LMC6484

THERMAL METRIC[(1)]		LMC6484		UNIT
		D (SOIC)	N (PDIP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83.0	53.6	ºC/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	42.7	32.0	ºC/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42.4	26.0	ºC/W
Ψ_{JT}	Junction-to-top characterization parameter	7.0	10.0	ºC/W
Ψ_{JB}	Junction-to-board characterization parameter	42.0	25.5	ºC/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	ºC/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.6 Electrical Characteristics: V_S = 5V

at T_J = +25°C, V+ = 5V, V– = 0V, V_{CM} = V_{OUT} = V+ / 2, and R_L > 1MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DC SPECS							
V_{OS}	Input offset voltage	LMC648xAI			±0.11	±0.75	mV
			T_A = –40°C to +85°C			±1.35	
		LMC648xI			±0.11	±3	
			T_A = –40°C to +85°C			±3.7	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +85°C			±1		μV/°C
I_B	Input bias current				±0.02		pA
		T_A = –40°C to +85°C				±4	
I_{OS}	Input offset current				±0.01		pA
		T_A = –40°C to +85°C				±2	
C_{IN}	Common-mode input capacitance				3		pF
R_{IN}	Input resistance				10		TΩ
CMRR	Common-mode rejection ratio	LMC648xAI 0V ≤ V_{CM} ≤ 15V, V+ = 15V		70	82		dB
			T_A = –40°C to +85°C	67			
		LMC648xI 0V ≤ V_{CM} ≤ 15V, V+ = 15V		65	82		
			T_A = –40°C to +85°C	62			
		LMC648xAI 0V ≤ V_{CM} ≤ 5V, V+ = 5V		70	82		
			T_A = –40°C to +85°C	67			
		LMC648xI 0V ≤ V_{CM} ≤ 5V, V+ = 5V		60	82		
			T_A = –40°C to +85°C	58			
+PSRR	Positive power-supply rejection ratio	LMC648xAI 5V ≤ V+ ≤ 15V, V– = 0V, V_O = 2.5V		70	82		dB
			T_A = –40°C to +85°C	67			
		LMC648xI 5V ≤ V+ ≤ 15V, V– = 0V, V_O = 2.5V		65	82		
			T_A = –40°C to +85°C	62			
–PSRR	Negative power-supply rejection ratio	LMC648xAI –5V ≤ V– ≤ –15V, V+ = 0V, V_O = –2.5V		70	82		dB
			T_A = –40°C to +85°C	67			
		LMC648xI –5V ≤ V– ≤ –15V, V+ = 0V, V_O = –2.5V		65	82		
			T_A = –40°C to +85°C	62			
V_{CM}	Input common-mode voltage	V+ = 5V and 15V, for CMRR ≥ 50dB	Low		(V–) – 0.3	–0.25	V
			Low, T_A = –40°C to +85°C			0	
			High	(V+) + 0.25	(V+) + 0.3		
			High, T_A = –40°C to +85°C	(V+)			

5.6 Electrical Characteristics: V_S = 5V (continued)

at T_J = +25°C, V+ = 5V, V– = 0V, V_{CM} = V_{OUT} = V+ / 2, and R_L > 1MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
A_V	Large-signal voltage gain	LMC648xAI sourcing, R_L = 2kΩ to 7.5V, V+ = 15V, 7.5V ≤ V_O ≤ 11.5V		140	666		V/mV
			T_A = –40°C to +85°C	84			
		LMC648xI sourcing, R_L = 2kΩ to 7.5V, V+ = 15V, 7.5V ≤ V_O ≤ 11.5V		120	666		
			T_A = –40°C to +85°C	72			
		LMC648xAI sinking, R_L = 2kΩ to 7.5V, V+ = 15V, 3.5V ≤ V_O ≤ 7.5V		35	75		
			T_A = –40°C to +85°C	20			
		LMC648xI sinking, R_L = 2kΩ to 7.5V, V+ = 15V, 3.5V ≤ V_O ≤ 7.5V		35	75		
			T_A = –40°C to +85°C	20			
		LMC648xAI sourcing, R_L = 600Ω to 7.5V, V+ = 15V, 7.5V ≤ V_O ≤ 11.5V		80	300		
			T_A = –40°C to +85°C	48			
		LMC648xI sourcing, R_L = 600Ω to 7.5V, V+ = 15V, 7.5V ≤ V_O ≤ 11.5V		50	300		
			T_A = –40°C to +85°C	30			
		LMC648xAI sinking, R_L = 600Ω to 7.5V, V+ = 15V, 3.5V ≤ V_O ≤ 7.5V		20	35		
			T_A = –40°C to +85°C	13			
		LMC648xI sinking, R_L = 600Ω to 7.5V, V+ = 15V, 3.5V ≤ V_O ≤ 7.5V		15	35		
			T_A = –40°C to +85°C	10			
V_O	Voltage output swing	V+ = 5V, R_L = 2kΩ to V+ / 2	Swing high	4.8	4.9		V
			Swing high, T_A = –40°C to +85°C	4.7			
			Swing low		0.1	0.18	
			Swing low, T_A = –40°C to +85°C			0.24	
		V+ = 5V, R_L = 600Ω to V+ / 2	Swing high	4.5	4.7		
			Swing high, T_A = –40°C to +85°C	4.24			
			Swing low		0.3	0.5	
			Swing low, T_A = –40°C to +85°C			0.65	
		V+ = 15V, R_L = 2kΩ to V+ / 2	Swing high	14.4	14.7		
			Swing high, T_A = –40°C to +85°C	14.2			
			Swing low		0.16	0.32	
			Swing low, T_A = –40°C to +85°C			0.45	
		V+ = 15V, R_L = 600Ω to V+ / 2	Swing high	13.4	14.1		
			Swing high, T_A = –40°C to +85°C	13			
			Swing low		0.5	1	
			Swing low, T_A = –40°C to +85°C			1.3	
I_{SC}	Output short-circuit current	V+ = 5V, sourcing, V_O = 0V		16	20		mA
			T_A = –40°C to +85°C	12			
		V+ = 5V, sinking, V_O = 5V		11	15		
			T_A = –40°C to +85°C	9.5			
		V+ = 15V, sourcing, V_O = 0V		28	30		
			T_A = –40°C to +85°C	22			
		V+ = 15V, sinking, V_O = 12V[1]		30	30		
			T_A = –40°C to +85°C	24			

5.6 Electrical Characteristics: V_S = 5V (continued)

at T_J = +25°C, V+ = 5V, V– = 0V, V_{CM} = V_{OUT} = V+ / 2, and R_L > 1MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_S	Supply current	Per amplifier, V+ = 5V, V_O = V+ / 2			0.5	0.7	mA
			T_A = –40°C to +85°C			0.9	
		Per amplifier, V+ = 15V, V_O = V+ / 2	LMC6482		0.65	0.8	
			LMC6484		0.65	0.75	
			T_A = –40°C to +85°C			0.95	
AC SPECS							
SR	Slew rate[2]	LMC648xAI V+ = 15V, 10V step		1	1.3		V/µs
			T_A = –40°C to +85°C	0.7			
		LMC648xI V+ = 15V, 10V step		0.9	1.3		
			T_A = –40°C to +85°C	0.63			
GBW	Gain bandwidth	V+ = 15V			1.5		MHz
Θ_m	Phase margin				50		Deg
G_m	Gain margin				15		dB
	Amp-to-amp isolation	V+ = 15V, R_L = 100kΩ to 7.5V, V_O = 12V_{PP}, f = 1kHz			150		dB
e_n	Input-referred voltage noise	f = 1kHz, V_{CM} = 1V			37		nV/√Hz
i_n	Input current noise density	f = 1kHz			0.03		pA/√Hz
THD	Total harmonic distortion	f = 10kHz, A_V = –2, R_L = 10kΩ	V_O = 8.5V_{PP}		0.01		%
			V+ = 10V, V_O = 4.1V_{PP}		0.01		

(1) Do not short circuit output to V+, when V+ is greater than 13V or reliability is adversely affected.
(2) Specification established from device population bench system measurements across multiple lots. Number specified is the slower of either the positive or negative slew rates.

5.7 Electrical Characteristics: V_S = 3V

at T_J = +25°C, V+ = 3V, V– = 0V, V_{CM} = V_{OUT} = V+ / 2, and R_L > 1MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DC SPECS							
V_{OS}	Input offset voltage	LMC648xAI			±0.9	±2	mV
			T_A = –40°C to +85°C			±2.7	
		LMC648xI			±0.9	±3	
			T_A = –40°C to +85°C			±3.7	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +85°C			±2		µV/°C
I_B	Input bias current				±0.02		pA
I_{OS}	Input offset current				±0.01		pA
CMRR	Common-mode rejection ratio	0V < V_{CM} < 3V	LMC648xAI	60	74		dB
			LMC648xI	55	74		
PSRR	Power-supply rejection ratio	3V < V+ < 15V, V– = 0V	LMC648xAI	68	80		dB
			LMC648xI	60	80		
V_{CM}	Input common-mode voltage	For CMRR ≥ 50dB	Low		(V–) – 0.25	0	V
			High	(V+)	(V+) + 0.25		
V_O	Voltage output swing	R_L = 2kΩ to V+ / 2	Swing high		2.8		V
			Swing low		0.2		
		R_L = 600Ω to V+ / 2	Swing high	2.5	2.7		
			Swing low		0.37	0.6	
I_S	Supply current	Per amplifier	LMC6482		0.4125	0.6	mA
			LMC6484		0.4125	0.625	
			T_A = –40°C to +85°C			0.75	
AC SPECS							
SR	Slew rate(1)	Voltage follower with 2V step input			0.9		V/µs
GBW	Gain bandwidth				1		MHz
THD	Total harmonic distortion	f = 10kHz, A_V = –2, R_L = 10kΩ, V_O = $2V_{PP}$			0.02		%

(1) Number specified is the slower of either the positive or negative slew rates.

5.8 Typical Characteristics

at V_S = 15V, single supply, and T_A = 25°C (unless otherwise specified)

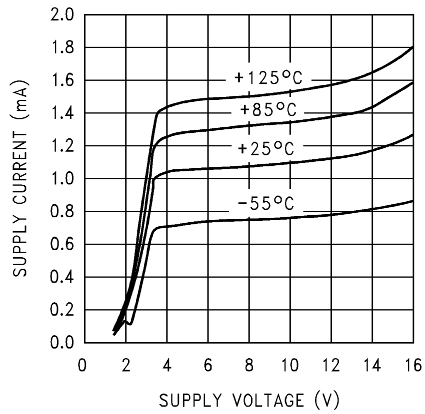


Figure 5-1. Supply Current vs Supply Voltage

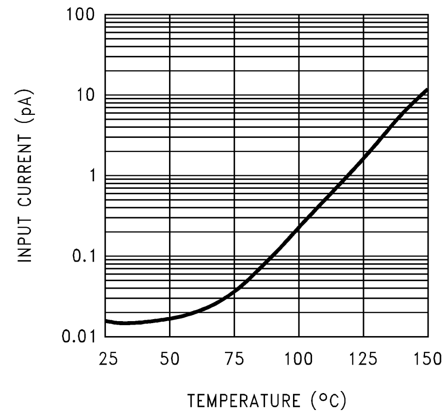


Figure 5-2. Input Current vs Temperature

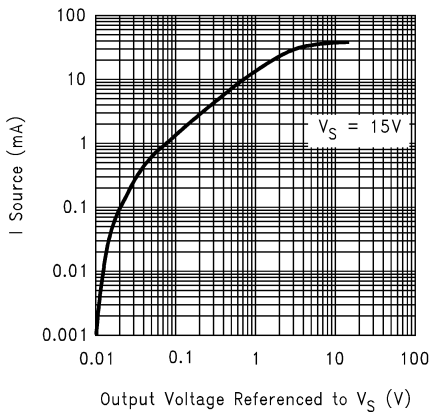


Figure 5-3. Sourcing Current vs Output Voltage

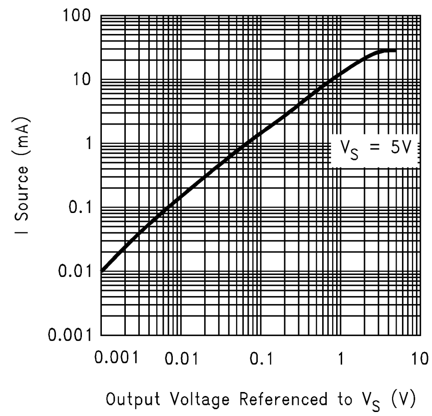


Figure 5-4. Sourcing Current vs Output Voltage

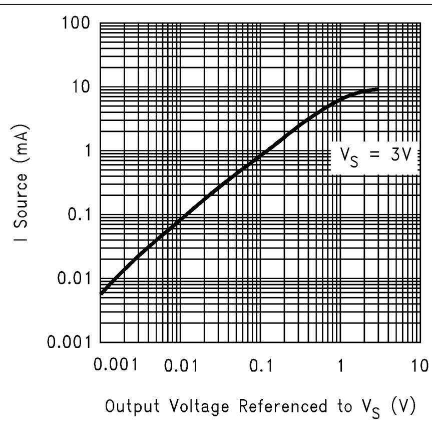


Figure 5-5. Sourcing Current vs Output Voltage

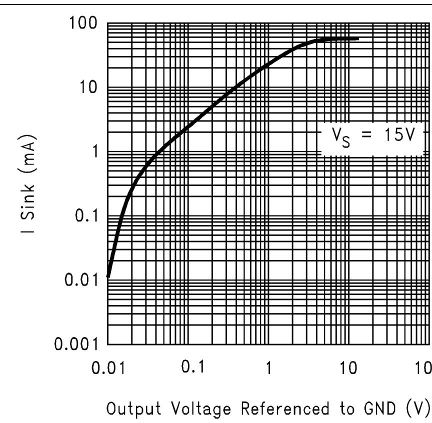


Figure 5-6. Sinking Current vs Output Voltage

5.8 Typical Characteristics (continued)

at V_S = 15V, single supply, and T_A = 25°C (unless otherwise specified)

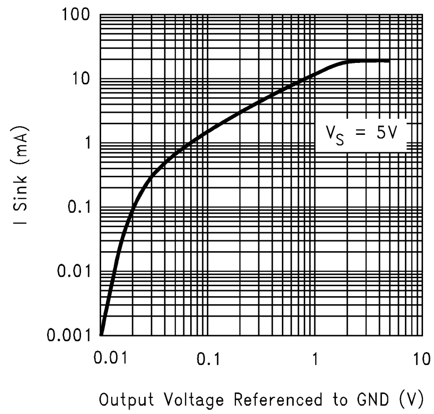


Figure 5-7. Sinking Current vs Output Voltage

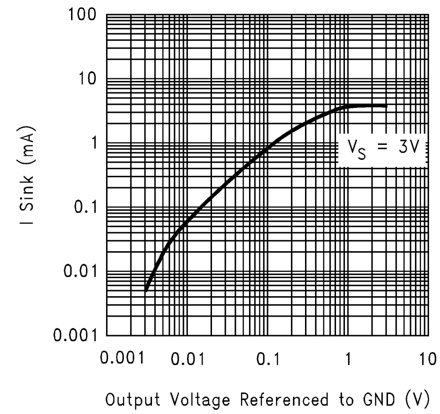


Figure 5-8. Sinking Current vs Output Voltage

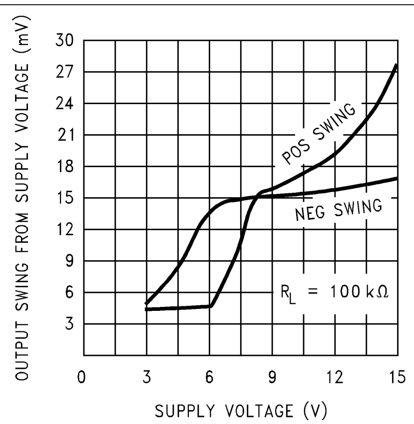


Figure 5-9. Output Voltage Swing vs Supply Voltage

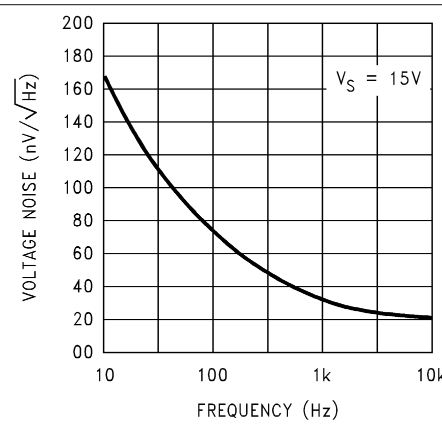


Figure 5-10. Input Voltage Noise vs Frequency

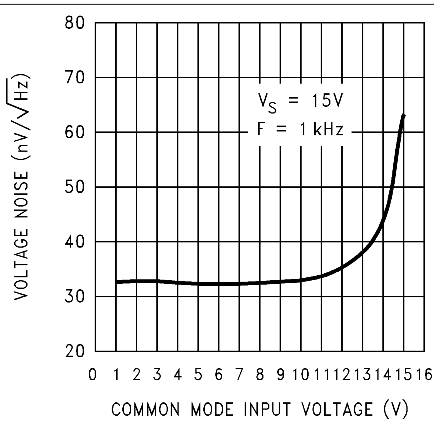


Figure 5-11. Input Voltage Noise vs Input Voltage

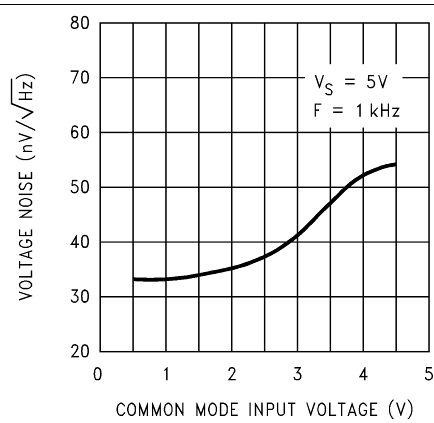


Figure 5-12. Input Voltage Noise vs Input Voltage

5.8 Typical Characteristics (continued)

at V_S = 15V, single supply, and T_A = 25°C (unless otherwise specified)

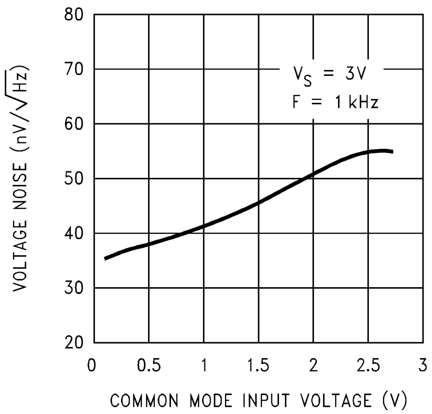


Figure 5-13. Input Voltage Noise vs Input Voltage

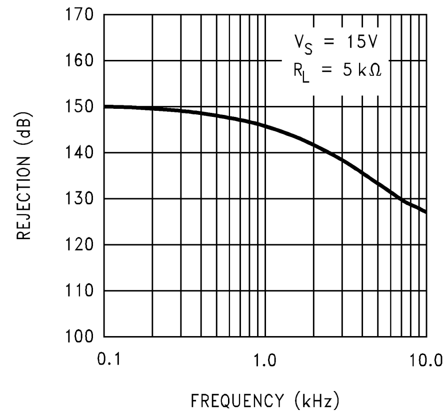


Figure 5-14. Crosstalk Rejection vs Frequency

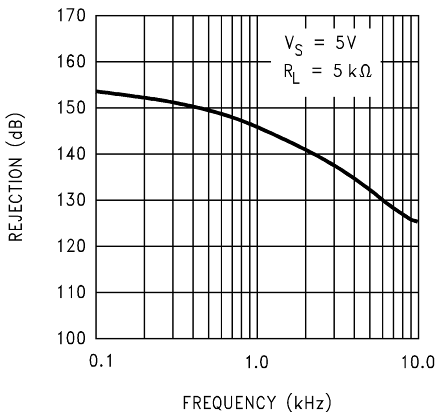


Figure 5-15. Crosstalk Rejection vs Frequency

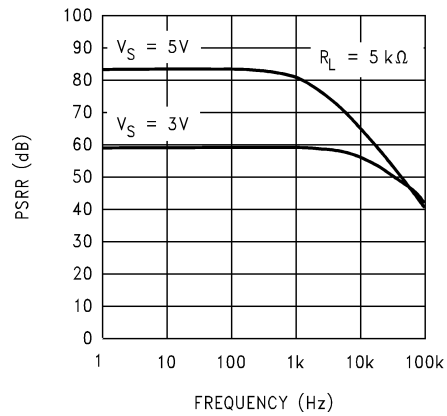


Figure 5-16. Positive PSRR vs Frequency

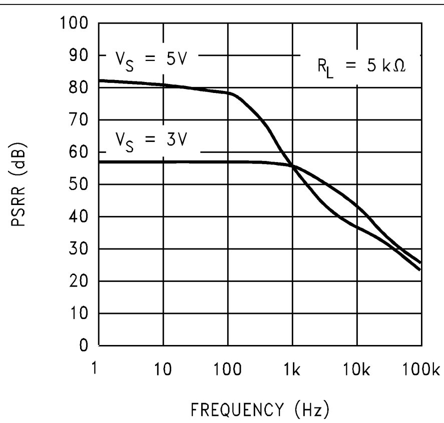


Figure 5-17. Negative PSRR vs Frequency

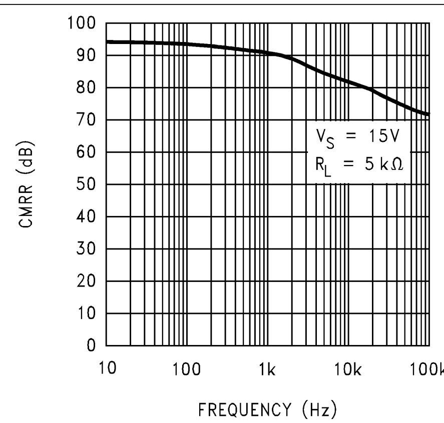


Figure 5-18. CMRR vs Frequency

5.8 Typical Characteristics (continued)

at V_S = 15V, single supply, and T_A = 25°C (unless otherwise specified)

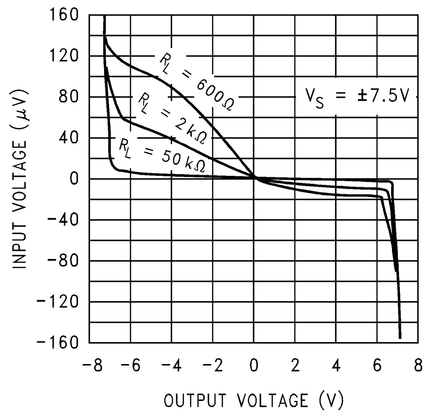


Figure 5-19. Input Voltage vs Output Voltage

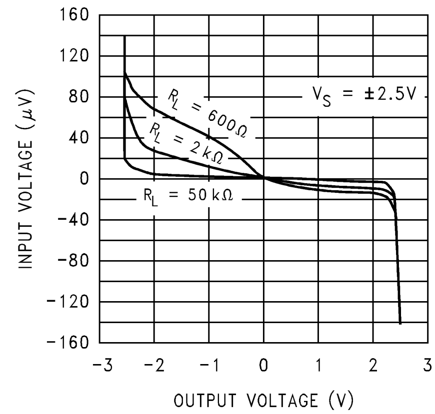


Figure 5-20. Input Voltage vs Output Voltage

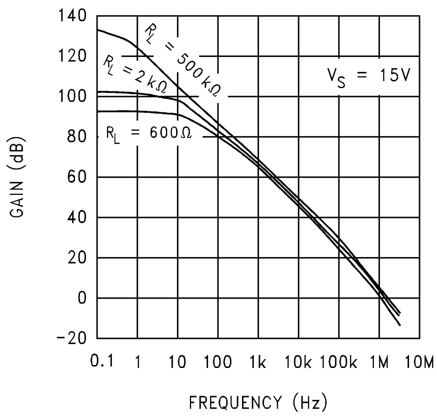


Figure 5-21. Open-Loop Frequency Response

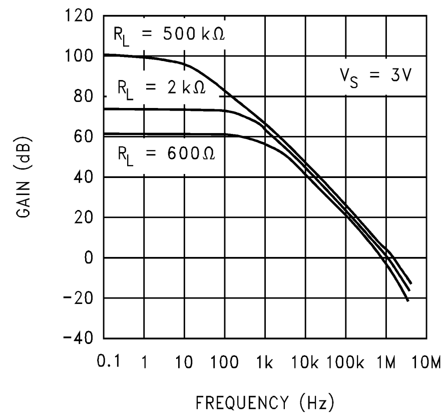


Figure 5-22. Open-Loop Frequency Response

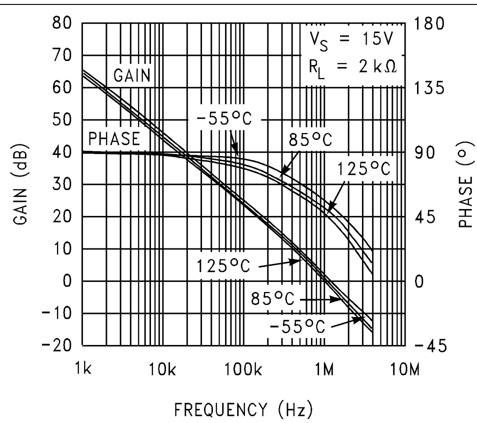


Figure 5-23. Open-Loop Frequency Response vs Temperature

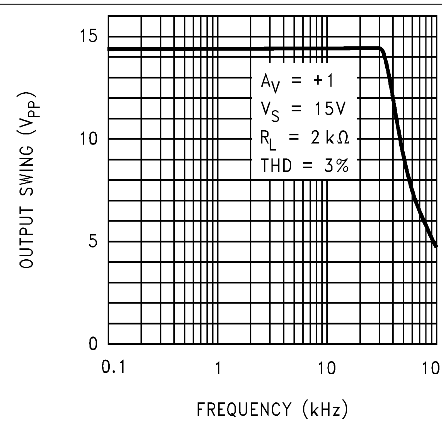


Figure 5-24. Maximum Output Swing vs Frequency

5.8 Typical Characteristics (continued)

at V_S = 15V, single supply, and T_A = 25°C (unless otherwise specified)

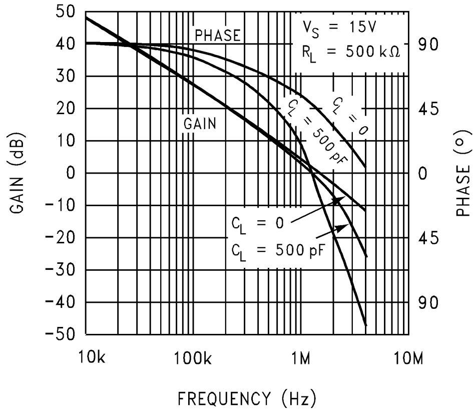


Figure 5-25. Gain and Phase vs Capacitive Load

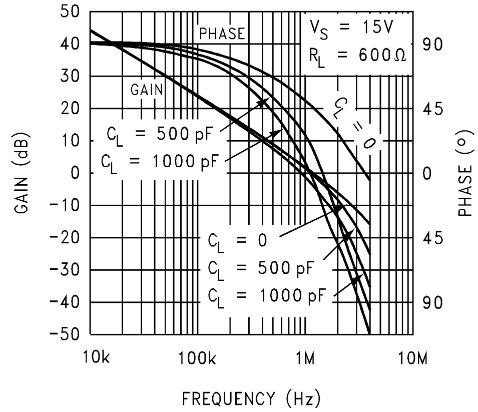


Figure 5-26. Gain and Phase vs Capacitive Load

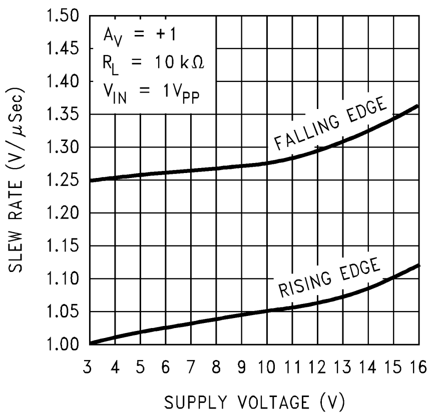


Figure 5-27. Slew Rate vs Supply Voltage

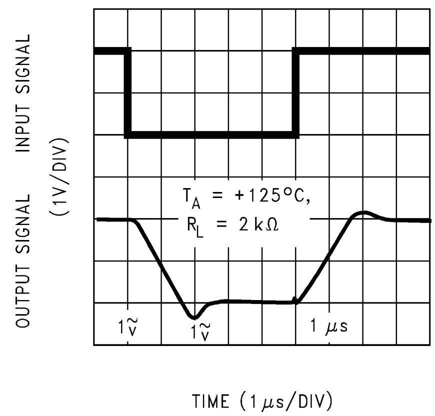


Figure 5-28. Noninverting Large Signal Pulse Response

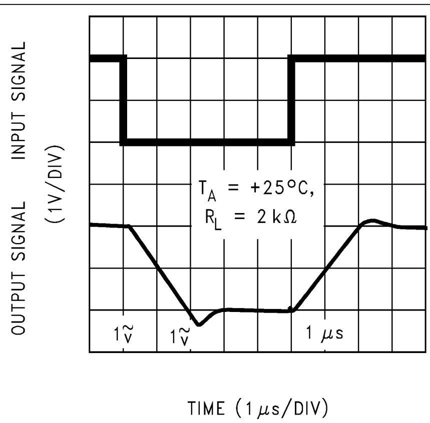


Figure 5-29. Noninverting Large Signal Pulse Response

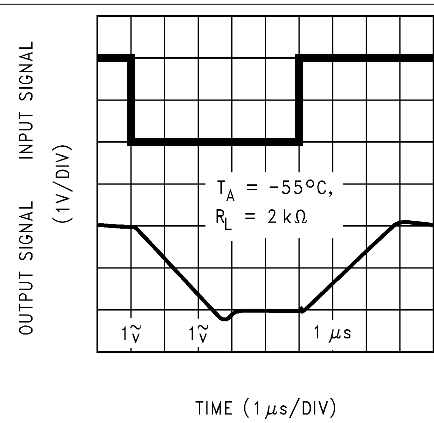


Figure 5-30. Noninverting Large Signal Pulse Response

5.8 Typical Characteristics (continued)

at V_S = 15V, single supply, and T_A = 25°C (unless otherwise specified)

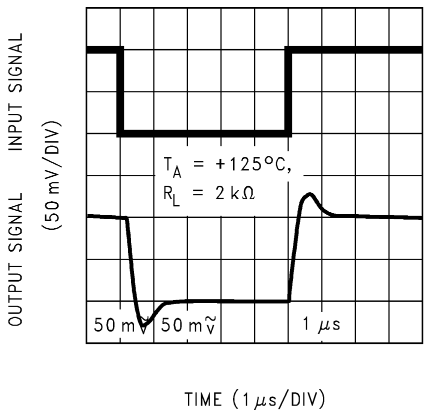


Figure 5-31. Noninverting Small Signal Pulse Response

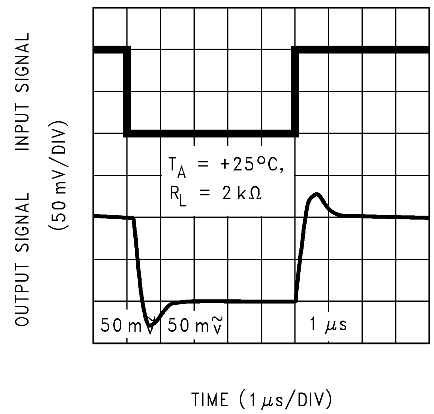


Figure 5-32. Noninverting Small Signal Pulse Response

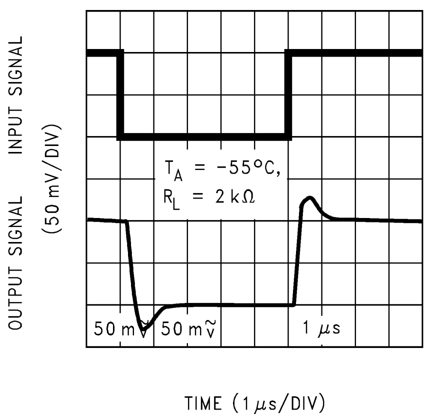


Figure 5-33. Noninverting Small Signal Pulse Response

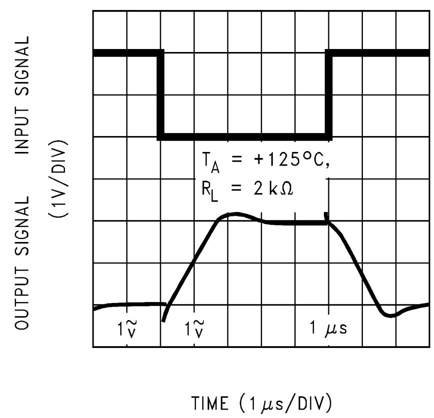


Figure 5-34. Inverting Large Signal Pulse Response

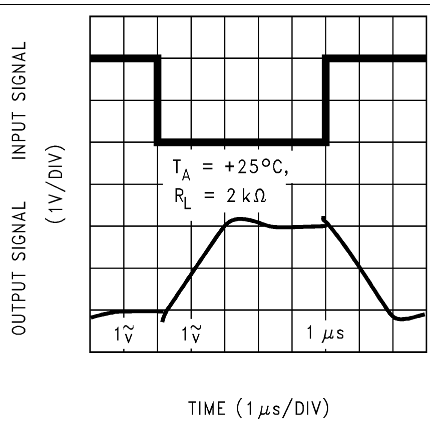


Figure 5-35. Inverting Large Signal Pulse Response

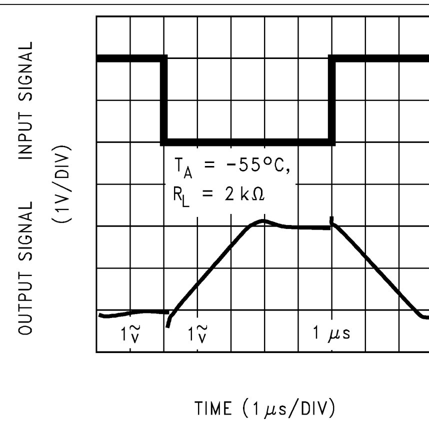


Figure 5-36. Inverting Large Signal Pulse Response

5.8 Typical Characteristics (continued)

at V_S = 15V, single supply, and T_A = 25°C (unless otherwise specified)

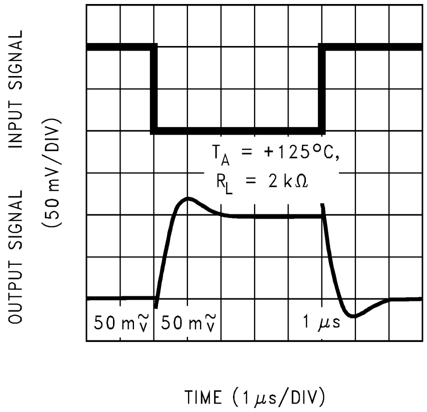


Figure 5-37. Inverting Small Signal Pulse Response

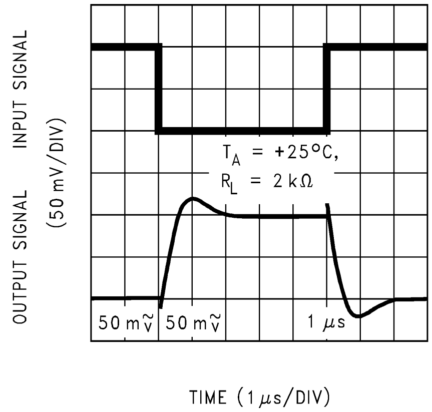


Figure 5-38. Inverting Small Signal Pulse Response

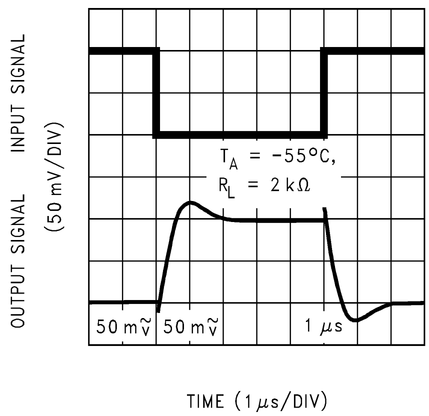


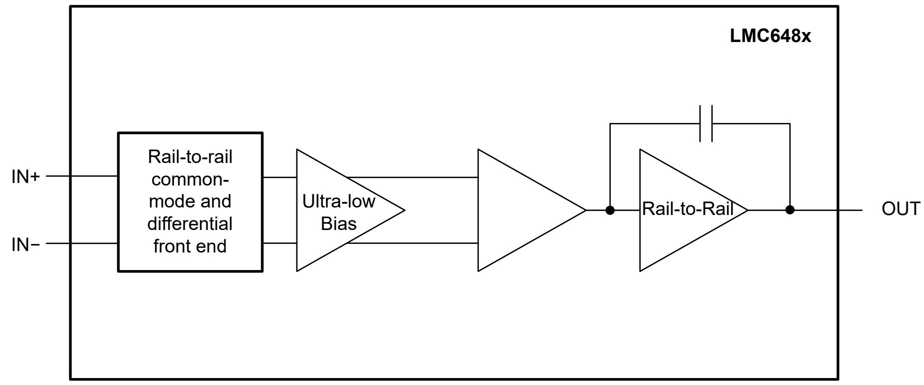
Figure 5-39. Inverting Small Signal Pulse Response

6 Detailed Description

6.1 Overview

The LMC648x are CMOS operational amplifiers that supports both rail-to-rail inputs and outputs. The device operates in both dual-supply mode and single-supply mode.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Amplifier Topology

The LMC648x are true rail-to-rail input operational amplifiers with an input common-mode range that extends 300mV beyond either supply rail. When the input common-mode voltage swings to about 3V from the positive rail, some dc specifications, namely offset voltage, can be slightly degraded. Figure 6-1 illustrates this behavior. The LMC648x incorporate a specially designed input stage to reduce the inherent accuracy problems seen in other rail-to-rail input amplifiers. The LMC648x input stage design is complemented by an output stage capable of rail-to-rail output swing even when driving a large load.

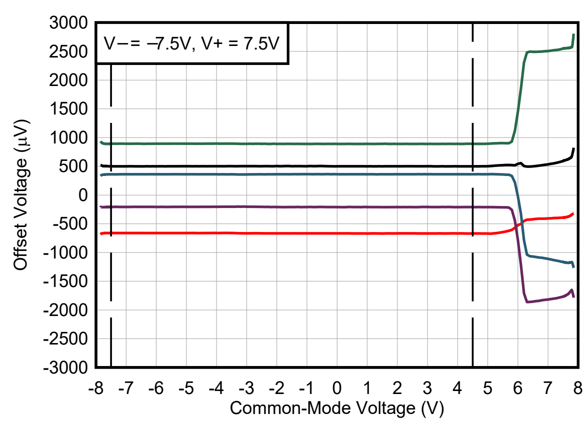
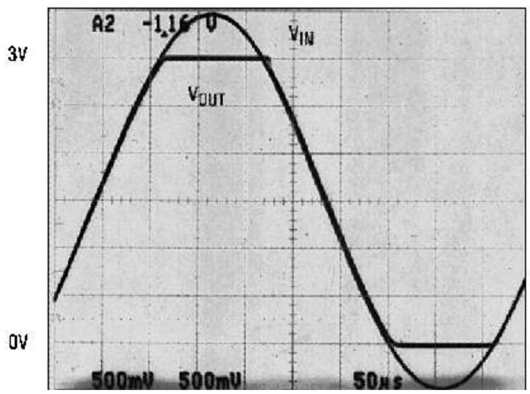


Figure 6-1. Input Offset Voltage vs Common-Mode Voltage

6.3.2 Input Common-Mode Voltage Range

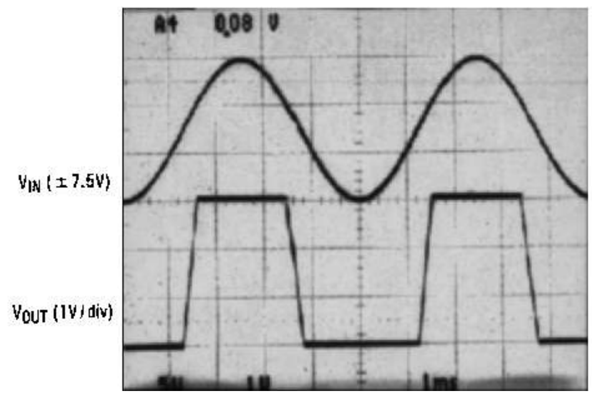
Unlike Bi-FET amplifier designs, the LMC648x do not exhibit phase inversion when an input voltage exceeds the negative supply voltage. Figure 6-2 shows an input voltage exceeding both supplies with no resulting phase inversion on the output.

The absolute maximum input voltage is 300mV beyond either supply rail at room temperature. Voltages greatly exceeding this absolute maximum rating, as in Figure 6-3, can cause excessive current to flow in or out of the input pins possibly affecting reliability.



An input voltage signal exceeds the LMC6482 power supply voltages with no output phase inversion.

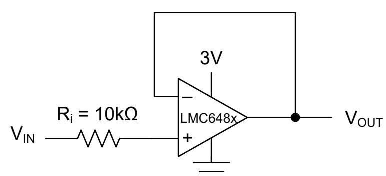
Figure 6-2. Input Voltage



A ±7.5-V input signal greatly exceeds the 3-V supply in Figure 6-4 causing no phase inversion due to R_i.

Figure 6-3. Input Signal

Applications that exceed this rating must externally limit the maximum input current to ±5mA with an input resistor (R_i) as shown in Figure 6-4.



NOTE: R_i input current protection for voltages exceeding the supply voltages.

Figure 6-4. R_i Input Current Protection for Voltages Exceeding the Supply Voltages

6.3.3 Rail-to-Rail Output

The LMC648x output can swing to within a few hundred millivolts of either supply voltage. Use the specified output swing specifications to calculate an approximate output resistance for different sourcing and sinking conditions. Use the calculated output resistance to estimate the maximum output voltage swing as a function of load.

6.4 Device Functional Modes

The LMC648x can be used in applications where each amplifier channel is used independently, or in applications in which the channels are cascaded. See Section 7.2 for more information.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

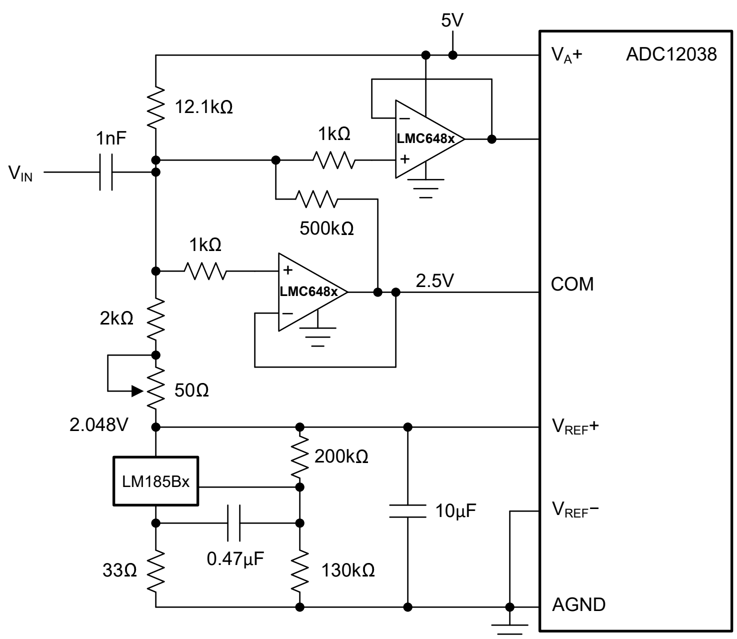
7.1.1 Upgrading Applications

The LMC648x have industry-standard pin outs to retrofit existing applications. System performance can be greatly increased by the features of the LMC648x. The key benefit of designing in the LMC648x is increased linear signal range. Most op amps have limited input common-mode ranges. Signals that exceed this range generate a nonlinear output response that persists long after the input signal returns to the common-mode range.

Linear signal range is vital in applications such as filters where signal peaking can exceed input common-mode ranges resulting in output phase inversion or severe distortion.

7.1.2 Data Acquisition Systems

Figure 7-1 shows a low-power, single-supply data-acquisition system achieved by buffering the ADC12038 with the LMC648x. Capable of using the full supply range, the LMC648x does not require input signals to be scaled down to meet limited common-mode voltage ranges. The LMC648x CMRR of 82dB maintains integral linearity of a 12-bit data acquisition system to ±0.325 LSB. Other rail-to-rail input amplifiers with only 50dB of CMRR can degrade the accuracy of the data acquisition system to only 8 bits.



NOTE: Operating from the same supply voltage, the LMC648x buffers the ADC12038 maintaining excellent accuracy.

Figure 7-1. Buffering the ADC12038 With the LMC648x

7.1.3 Instrumentation Circuits

The LMC648x have high input impedance, large common-mode range and high CMRR needed for designing instrumentation circuits. Instrumentation circuits designed with the LMC648x can reject a larger range of common-mode signals than most in-amps. This makes instrumentation circuits designed with the LMC648x an excellent choice for noisy or industrial environments. Other applications that benefit from these features include analytic medical instruments, magnetic field detectors, gas detectors, and silicon-based transducers.

A small valued potentiometer is used in series with R_G to set the differential gain of the 3-op-amp instrumentation circuit in Figure 7-2. This combination is used instead of one large valued potentiometer to increase gain trim accuracy and reduce error due to vibration. An improved design that can help increase accuracy, save cost, and reduce board space can be achieved by using the RES11A matched resistor pair series.

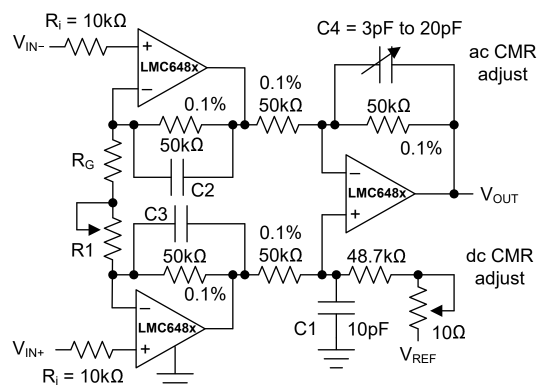


Figure 7-2. Low Power, Three Op Amp Instrumentation Amplifier

The Figure 7-3 shows how a high precision, high CMRR, and low drift in-amp can be achieved using two matched resistor pairs. Using a 1:4 ratio, a gain of 36V/V can be easily implemented. Other gain options are possible by using the various ratios available. One downside to the original implementation in Figure 7-2 is that very high performance, 0.01% resistors and a couple of potentiometers are needed to achieve very high common-mode rejection and gain accuracy. High accuracy resistors can be very expensive and add to board layout size and complexity. Another downside is that the temperature drift of the discrete resistors causes an increase in gain error that is not easily calibrated out.

The RES11A matched resistor pairs provide high common-mode rejection and gain-error performance due to excellent matching to less than 0.05%. The resistors are on the same substrate; therefore, the resistors drift in the same direction, minimizing temperature-related errors such as gain error drift. For a more detailed analysis of the benefits of the RES11A over discrete resistors, see the *Optimizing CMRR in Differential Amplifier Circuits With Precision Matched Resistor Divider Pairs* application note.

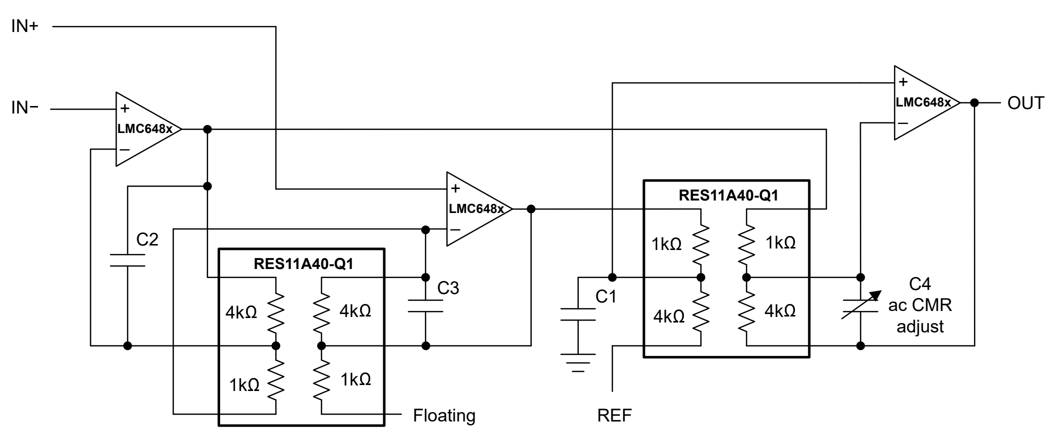


Figure 7-3. Improved Low Power, Three Op Amp Instrumentation Amplifier With RES11A

A two op amp instrumentation amplifier designed for a gain of 100V/V is shown in Figure 7-4. Low sensitivity trimming is made for offset voltage, CMRR, and gain. Low cost and low power consumption are the main advantages of this two op amp circuit. An alternative circuit with a gain of 10V/V with the RES11A is also provided for this circuit in Figure 7-5.

Higher frequency and larger common-mode range applications are best facilitated by a three op amp instrumentation amplifier.

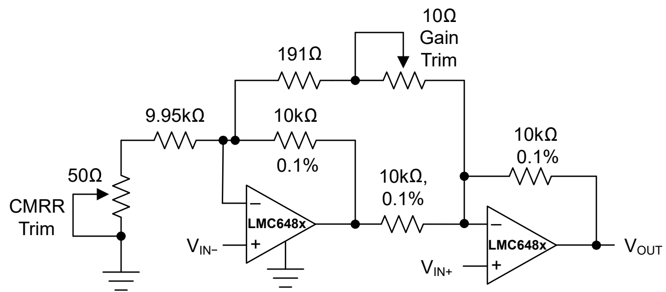


Figure 7-4. Low Power, Two Op Amp Instrumentation Amplifier

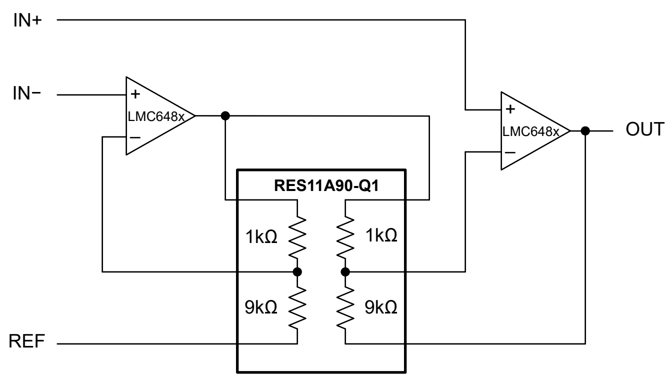


Figure 7-5. Low Power, Two Op Amp Instrumentation Amplifier with RES11A

7.2 Typical Applications

7.2.1 3V Single-Supply Buffer Circuit

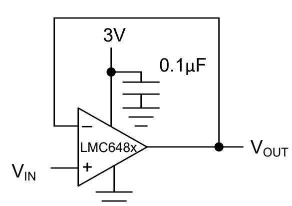


Figure 7-6. 3V Single-Supply Buffer Circuit

7.2.1.1 Design Requirements

For best performance, ensure that the input voltage swing is between V+ and V–.

Also, ensure that the input does not exceed the common-mode input voltage range.

To reduce the risk of destabilizing the output, use resistive isolation on the output when driving capacitive loads (see *Section 7.2.1.2*).

When large feedback resistors are used, compensate for parasitic capacitance on the input, if necessary. See *Section 7.2.1.2*.

7.2.1.2 Detailed Design Procedure

7.2.1.2.1 Capacitive Load Compensation

The LMC648x provides a robust output stage for directly driving capacitive loads. Capacitive loads interact with the output impedance of the amplifier to create a pole that can cause instability. When driving capacitive loads, consider the closed-loop bandwidth and output impedance of the amplifier. The LMC648x open-loop output impedance is shown in Figure 7-7.

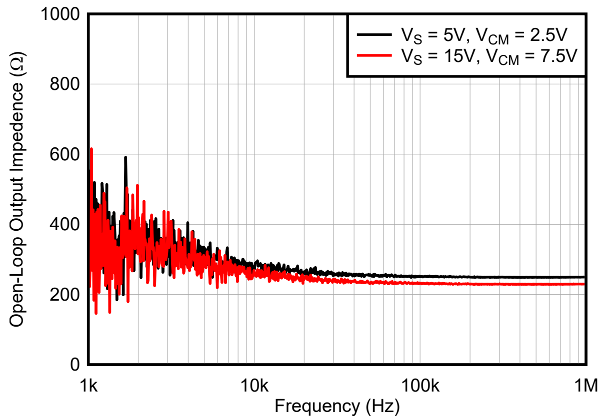


Figure 7-7. Open-Loop Output Impedance

In some applications, driving large capacitive loads is required and additional compensation is necessary. Capacitive load compensation can be accomplished using resistive isolation as shown in Figure 7-8. This simple technique is useful for isolating the capacitive inputs of multiplexers and analog-to-digital converters (ADCs).

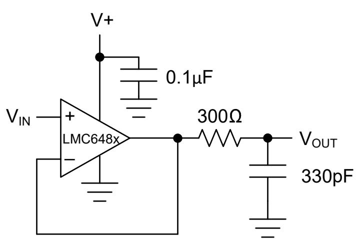


Figure 7-8. Resistive Isolation of a 330pF Capacitive Load

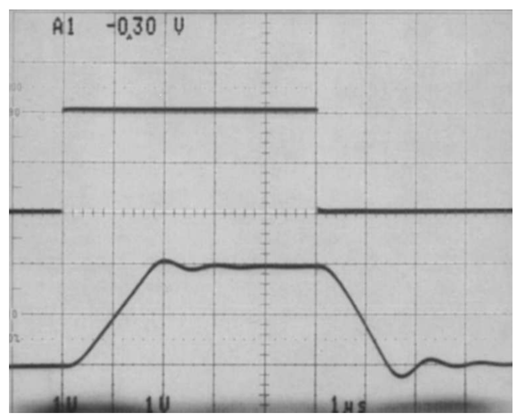
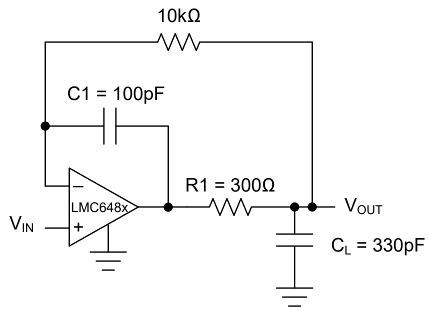


Figure 7-9. Pulse Response of the LMC6482 Circuit in Figure 7-8

7.2.1.2.2 Capacitive Load Tolerance

The LMC648x can typically directly drive a 100pF load with V_S = 15V at unity gain without oscillating. The unity gain follower is the most sensitive configuration. Direct capacitive loading reduces the phase margin of op amps. The combination of the output impedance of the op-amp and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation.

Figure 7-10 shows how improved frequency response is achieved by indirectly driving capacitive loads.



NOTE: Compensated to handle a 330pF capacitive load.

Figure 7-10. LMC648x Noninverting Amplifier

R1 and C1 serve to counteract the loss of phase margin by feeding forward the high-frequency component of the output signal back to the amplifiers inverting input, thereby preserving phase margin in the overall feedback loop. The values of R1 and C1 are experimentally determined for the desired pulse response. Figure 7-11 shows the resulting pulse response.

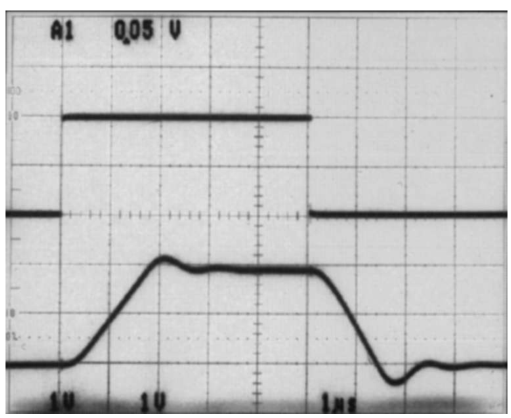


Figure 7-11. Pulse Response of LMC6482 Circuit in Figure 7-10

7.2.1.2.3 Compensating For Input Capacitance

The use of large values of feedback resistance with amplifiers that have ultra-low input current, like the LMC648x, is quite common. Large feedback resistors can react with small values of input capacitance due to transducers, photo diodes, and circuits board parasitics to reduce phase margins.

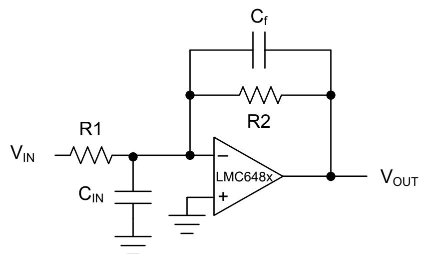


Figure 7-12. Canceling the Effect of Input Capacitance

The effect of input capacitance can be compensated for by adding a feedback capacitor. The feedback capacitor (as in Figure 7-12), C_f, is first estimated by:

$$\frac{1}{2\pi R1 C_{IN}} \geq \frac{1}{2\pi R2 C_f} \quad (1)$$

or

$$R1\ C_{IN} \leq R2\ C_f \quad (2)$$

which typically provides significant overcompensation.

Printed-circuit-board stray capacitance can be larger or smaller than that of a bread-board, so the actual optimum value for C_f can be different. Check the value of C_f on the actual circuit. (Refer to the LMC660 quad CMOS amplifier data sheet for a more detailed discussion.)

7.2.1.2.4 Offset Voltage Adjustment

Offset voltage adjustment circuits are illustrated in Figure 7-13 and Figure 7-14. Large value resistances and potentiometers are used to reduce power consumption while providing typically ±2.5mV of adjustment range, referred to the input, for both configurations with V_S = ±5V.

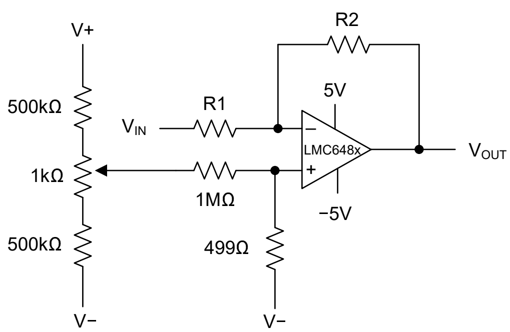


Figure 7-13. Inverting Configuration Offset Voltage Adjustment

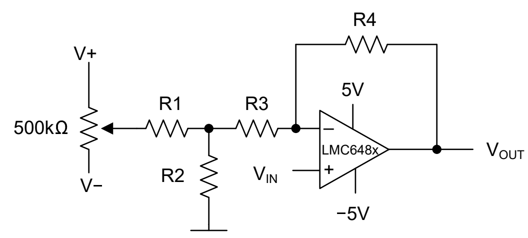


Figure 7-14. Noninverting Configuration Offset Voltage Adjustment

7.2.1.3 Application Curves

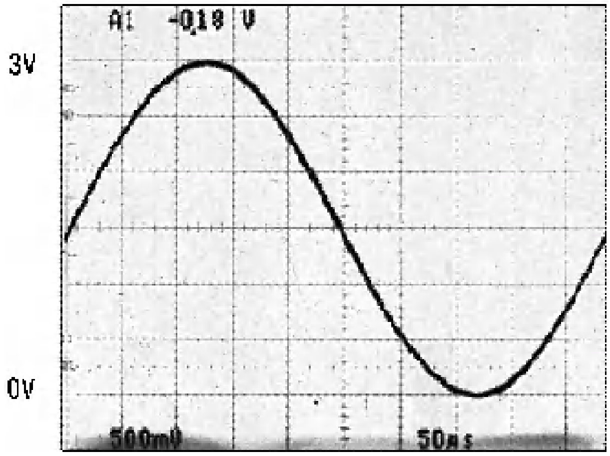


Figure 7-15. Rail-to-Rail Input

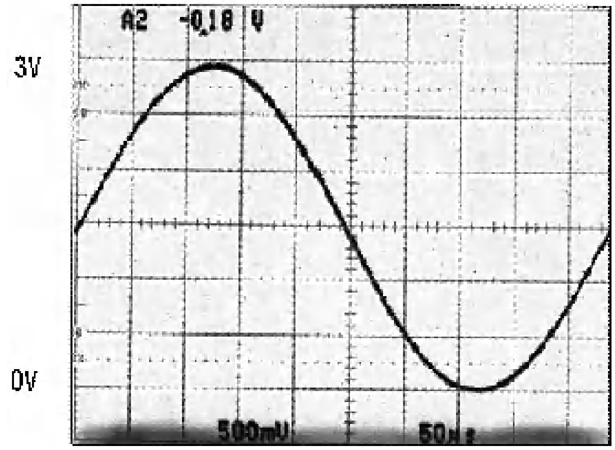


Figure 7-16. Rail-to-Rail Output

7.2.2 Typical Single-Supply Applications

The circuit in Figure 7-17 uses a single supply to half-wave rectify a sinusoid centered about ground. R_i limits current into the amplifier caused by the input voltage exceeding the supply voltage. Full-wave rectification is provided by the circuit in Figure 7-19.

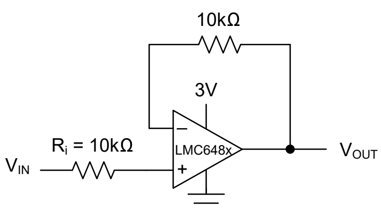


Figure 7-17. Half-Wave Rectifier With Input Current Protection (R_i)

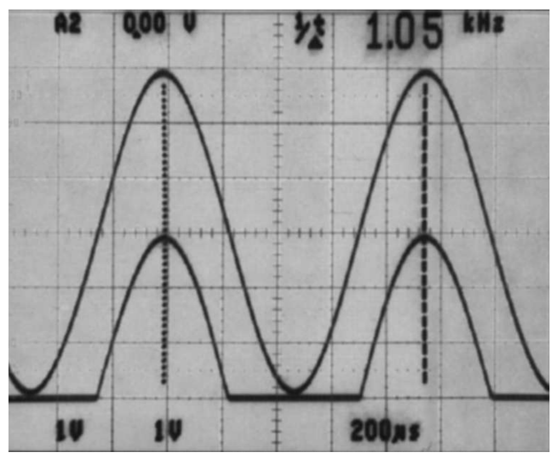


Figure 7-18. Half-Wave Rectifier Waveform

In Figure 7-23, dielectric absorption and leakage is minimized by using a polystyrene or polyethylene hold capacitor. The droop rate is primarily determined by the value of C_{HOLD} and diode leakage current. The ultra-low input current of the LMC648x has a negligible effect on droop. For applications requiring ultra-low input bias current, see the OPA928.

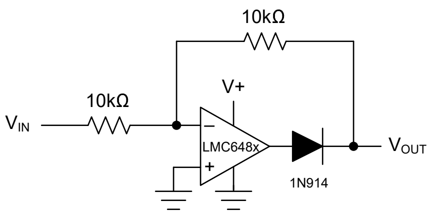


Figure 7-19. Full-Wave Rectifier With Input Current Protection (R_I)

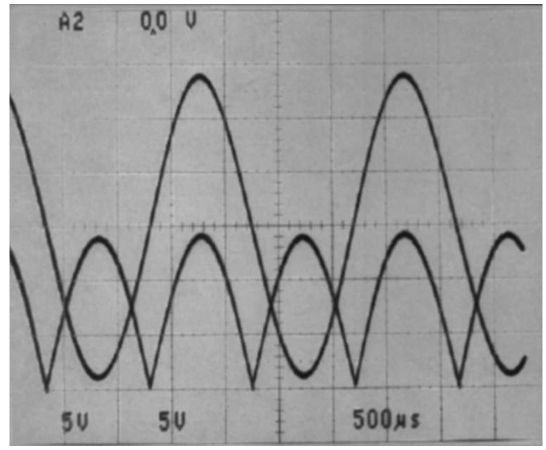


Figure 7-20. Full-Wave Rectifier Waveform

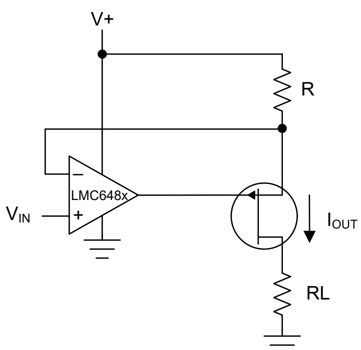


Figure 7-21. Large Compliance Range Current Source

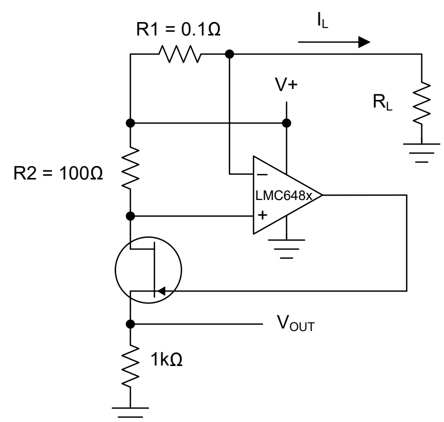


Figure 7-22. Positive Supply Current Sense

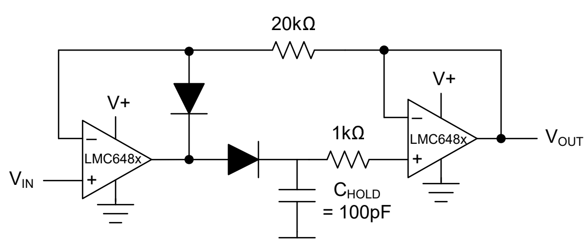


Figure 7-23. Low-Voltage Peak Detector With Rail-To-Rail Peak Capture Range

The high CMRR (82dB) of the LMC648x allows excellent accuracy throughout the rail-to-rail dynamic capture range of the circuit.

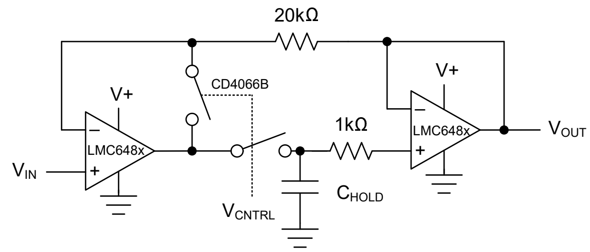


Figure 7-24. Rail-to-Rail Sample-and-Hold Circuit

The low-pass filter circuit in Figure 7-25 can be used as an anti-aliasing filter with the same voltage supply as the ADC.

Filter designs can also take advantage of the LMC648x ultra-low input current. The ultra-low input current yields negligible offset error even when large value resistors are used. This in turn allows the use of smaller valued capacitors that take less board space and cost less.

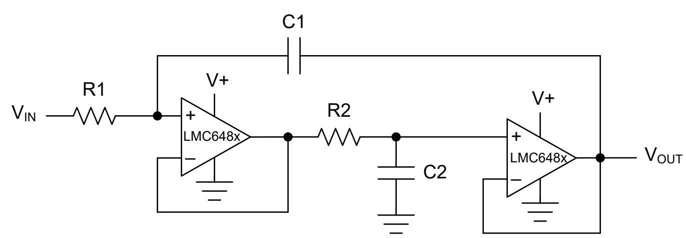


Figure 7-25. Rail-to-Rail, Single-Supply Low-Pass Filter

$$\mathrm{R1} = \mathrm{R2},\ \mathrm{C1} = \mathrm{C2},\ f = \frac{1}{2\pi \mathrm{R1C1}},\ \mathrm{DF} = \frac{1}{2}\sqrt{\frac{\mathrm{C2}}{\mathrm{C1}}}\sqrt{\frac{\mathrm{R2}}{\mathrm{R1}}} \tag{3}$$

7.3 Power Supply Recommendations

The LMC648x operate over a supply range of 3V to 15.5V. To achieve noise immunity as appropriate to the application, use good printed circuit board (PCB) layout practices for power-supply rails and planes, as well as bypass capacitors connected between the power-supply pins and ground.

7.4 Layout

7.4.1 Layout Guidelines

As a general rule, any circuit that must operate with less than 1000pA of leakage current requires special layout of the PC board. To take advantage of the ultra-low input current of the LMC648x, typically less than 20fA, an excellent layout is essential. Fortunately, the techniques of obtaining low leakages are quite simple. First, do not ignore the surface leakage of the PCB even though the leakage current can sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage can be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC648x inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, and so forth connected to the inputs of the op amp, as in Figure 7-26. To have a significant effect, place guard rings on both the top and bottom of the PCB. This PC foil must then be connected to a voltage that is at the same voltage as the amplifier inputs, because no leakage current can flow between two points at the same potential. For example, a PCB trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, can leak 5pA if the trace were a 5V bus adjacent to the pad of the input. This leakage can cause a 250 times degradation from the actual performance of the LMC648x. However, if a guard ring is held within 5mV of the inputs, then even a resistance of $10^{11}\Omega$ causes only 0.05pA of leakage current. See Figure 7-27 through Figure 7-29 for typical connections of guard rings for standard op-amp configurations.

Be aware that when laying out a PCB for the sake of just a few circuits is not practical, another technique is even better than a guard ring on a PCB: Do not insert the input pin of the amplifier into the PCB at all, but bend the pin up in the air, and use only air as an insulator. Air is an excellent insulator. In this case you forgo some of the advantages of PCB construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 7-30.

7.4.2 Layout Example

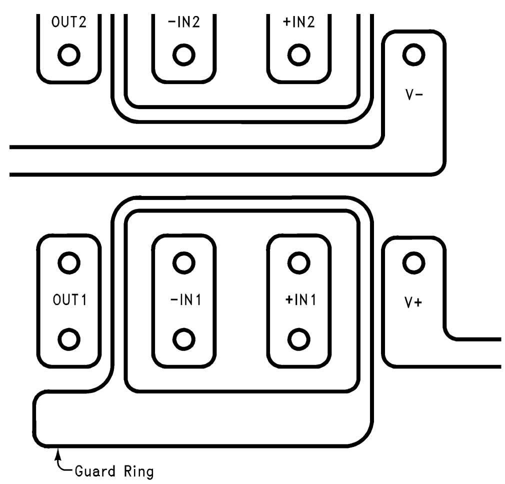


Figure 7-26. Example of Guard Ring in PCB Layout Typical Connections of Guard Rings

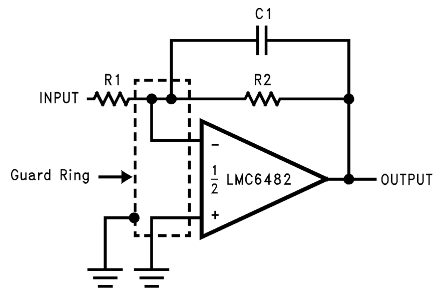


Figure 7-27. Inverting Amplifier Typical Connections of Guard Rings

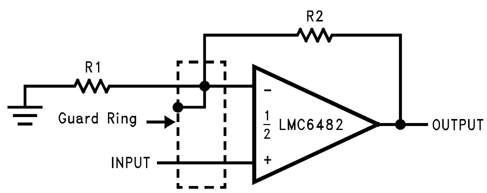


Figure 7-28. Noninverting Amplifier Typical Connections of Guard Rings

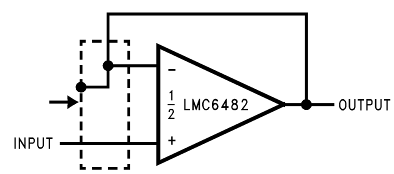
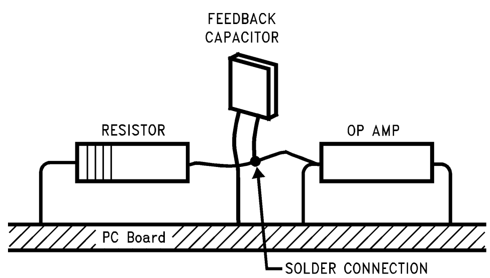


Figure 7-29. Follower Typical Connections of Guard Rings



Input pins are lifted out of PCB and soldered directly to components. All other pins connected to PCB.

Figure 7-30. Air Wiring

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 Spice Macromodel

A spice macromodel is available for the LMC648x. This model includes accurate simulation of the following:

- Input common-mode voltage range
- Frequency and transient response
- Gain bandwidth (GBW) dependence on loading conditions
- Quiescent and dynamic supply current
- Output swing dependence on loading conditions

8.1.1.2 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

8.1.1.3 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Design and simulation tools web page, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the TINA-TI™ software folder.

8.1.1.4 DIP-Adapter-EVM

Speed up your op amp prototyping and testing with the DIP-Adapter-EVM, which provides a fast, easy and inexpensive way to interface with small, surface-mount devices. Connect any supported op amp using the included Samtec terminal strips or wire them directly to existing circuits. The DIP-Adapter-EVM kit supports the following industry-standard packages: D or U (SOIC-8), PW (TSSOP-8), DGK (VSSOP-8), DBV (SOT-23-6, SOT-23-5 and SOT-23-3), DCK (SC70-6 and SC70-5), and DRL (SOT563-6).

8.1.1.5 DIYAMP-EVM

The DIYAMP-EVM is a unique evaluation module (EVM) that provides real-world amplifier circuits, enabling the user to quickly evaluate design concepts and verify simulations. This EVM is available in three industry-standard packages (SC70, SOT23, and SOIC) and 12 popular amplifier configurations, including amplifiers, filters, stability compensation, and comparator configurations for both single and dual supplies.

8.1.1.6 TI Reference Designs

TI reference designs are analog solutions created by TI's precision analog applications experts. TI reference designs offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI reference designs are available online at https://www.ti.com/reference-designs.

8.1.1.7 Analog Filter Designer

Available as a web-based tool from the Design and simulation tool web page, the Analog Filter Designer allows the user to design, optimize, and simulate complete multistage active filter solutions within minutes.

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

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PSpice® is a registered trademark of Cadence Design Systems, Inc.
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8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (February 2024) to Revision J (September 2024) — **Page**

- Updated front page figure, *Unity-Gain Difference Amplifier*, to swap IN+ and IN–..1
- Changed LMC648xI common-mode rejection ratio MIN from 65dB to 60dB for 5V supply and from 60dB to 55dB for 3V supply... 6
- Changed common-mode rejection ratio MIN for LMC648xI from 60dB to 58dB for T_A = –40°C to +85°C.........6
- Changed LMC648xAI common-mode rejection ratio MIN from 64dB to 60dB for 3V supply............................9
- Updated Figure 7-17, *Half-Wave Rectifier With Input Current Protection (R_i)* to illustrate correct circuit.........25

Changes from Revision H (November 2023) to Revision I (February 2024) — **Page**

- Added LMC6484 and associated content..1
- Updated content from previous LMC6484 data sheet (SNOS675D) as detailed in *Changes from Revision G (April 2020) to Revision H (November 2023)* of this data sheet (SNOS674I)...1
- Added values for LMC6482 and LMC6484 based on latest modeling standard to *Thermal Information* 5
- Updated *Electrical Characteristics* format for LMC6484 and as detailed in *Changes from Revision G (April 2020) to Revision H (November 2023)* of this data sheet.. 6
- Changed CMRR from 62dB to 60dB to match LMC6484 in *Electrical Characteristics: V_S = 5V* 6
- Updated footnote (2) on how slew rate minimum value is specified in *Electrical Characteristics: V_S = 5V* 6

- Changed THD from 0.01% to 0.02% in *Electrical Characteristics: V_S = 3V* 9

Changes from Revision G (April 2020) to Revision H (November 2023)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.................	1
• Deleted specifications are typical, high voltage gain, and power good output from *Features*	1
• Deleted M version device from data sheet; see the LMC6482QML for more information.................................	1
• Updated front page figures in *Description*	1
• Updated *Pin Configuration and Functions*	2
• Added ± to input offset voltage, input offset voltage drift, input bias current, and input offset current in *Electrical Characteristics*	6
• Updated parameter names throughout *Electrical Characteristics* for consistency..	6
• Deleted notes 1, 2, and 3 from *Electrical Characteristics*	6
• Changed supply current specification from total to per amplifier in *Electrical Characteristics*	6
• Deleted Figure 11 to 13, Figure 19 to 23, Figure 32 to 33, and Figure 47 to 52..	10
• Updated functional block diagram..	17
• Updated description of the input stage in *Amplifier Topology*	17
• Added Input Offset Voltage vs Common-Mode Voltage plot in *Amplifier Topology*	17
• Updated the description in *Rail-to-Rail Output*	18
• Added an improved instrumentation amplifier circuit to *Instrumentation Circuits*	20
• Added Figure 7-7, *Open-Loop Output Impedance* and related content to *Capacitive Load Compensation* ...	22
• Added OPA928 femtoampere-input bias-current op-amp recommendation to *Typical Single-Supply Applications*	25
• Deleted references to the library disk in *Spice Macromodel*	30

Changes from Revision F (April 2020) to Revision G (April 2020)	Page
• Deleted old note 4 from *Electrical Characteristics* for V+ = 5 V table..	6

Changes from Revision E (April 2015) to Revision F (April 2020)	Page
• Changed junction temperature max value from –85°C to 85°C (typo) in *Recommended Operating Conditions* table...	4

Changes from Revision D (March 2013) to Revision E (April 2015)	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

Changes from Revision C (March 2013) to Revision D (March 2013)	Page
• Changed layout of National Semiconductor Data Sheet to TI format..	25

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMC6482AIM/NOPB	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	LMC64 82AIM
LMC6482AIMX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(6482AI, LMC64) 82AIM
LMC6482AIMX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(6482AI, LMC64) 82AIM
LMC6482AIMX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(6482AI, LMC64) 82AIM
LMC6482AIN/NOPB	Active	Production	PDIP (P) | 8	40 | TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	-40 to 85	LMC64 82AIN
LMC6482AIN/NOPB.A	Active	Production	PDIP (P) | 8	40 | TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	-40 to 85	LMC64 82AIN
LMC6482AIN/NOPB.B	Active	Production	PDIP (P) | 8	40 | TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	-40 to 85	LMC64 82AIN
LMC6482IMMX/NOPB	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	A10
LMC6482IMMX/NOPB.A	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	A10
LMC6482IMMX/NOPB.B	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	A10
LMC6482IMX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LMC64 82IM
LMC6482IMX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LMC64 82IM
LMC6482IN/NOPB	Active	Production	PDIP (P) | 8	40 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	LMC6482IN
LMC6482IN/NOPB.A	Active	Production	PDIP (P) | 8	40 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	LMC6482IN
LMC6482IN/NOPBG4	Active	Production	PDIP (P) | 8	40 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	LMC6482IN
LMC6482IN/NOPBG4.A	Active	Production	PDIP (P) | 8	40 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	LMC6482IN
LMC6484AIM/NOPB	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 85	LMC6484 AIM
LMC6484AIMX/NOPB	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(LMC6484, LMC6484A IM) AIM
LMC6484AIMX/NOPB.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(LMC6484, LMC6484A IM) AIM

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMC6484AIMX/NOPB.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
LMC6484AIN/NOPB	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	-40 to 85	LMC6484AIN
LMC6484AIN/NOPB.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	-40 to 85	LMC6484AIN
LMC6484AIN/NOPB.B	Active	Production	PDIP (N) | 14	25 | TUBE	-	Call TI	Call TI	-40 to 85	
LMC6484IM/NOPB	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 85	LMC6484IM
LMC6484IMX/NOPB	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LMC6484IM
LMC6484IMX/NOPB.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LMC6484IM
LMC6484IN/NOPB	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	-40 to 85	LMC6484IN
LMC6484IN/NOPB.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	-40 to 85	LMC6484IN
LMC6484IN/NOPB.B	Active	Production	PDIP (N) | 14	25 | TUBE	-	Call TI	Call TI	-40 to 85	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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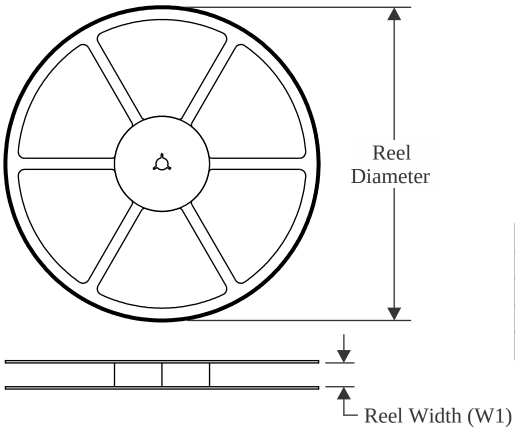
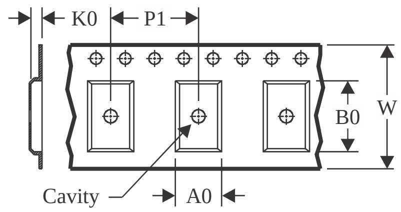
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

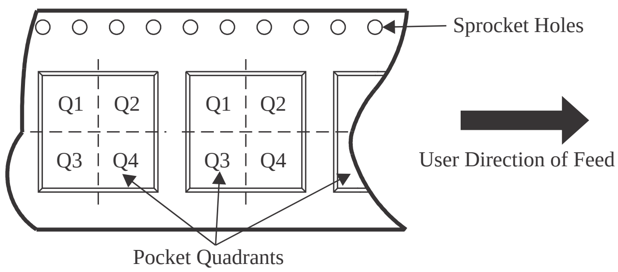


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

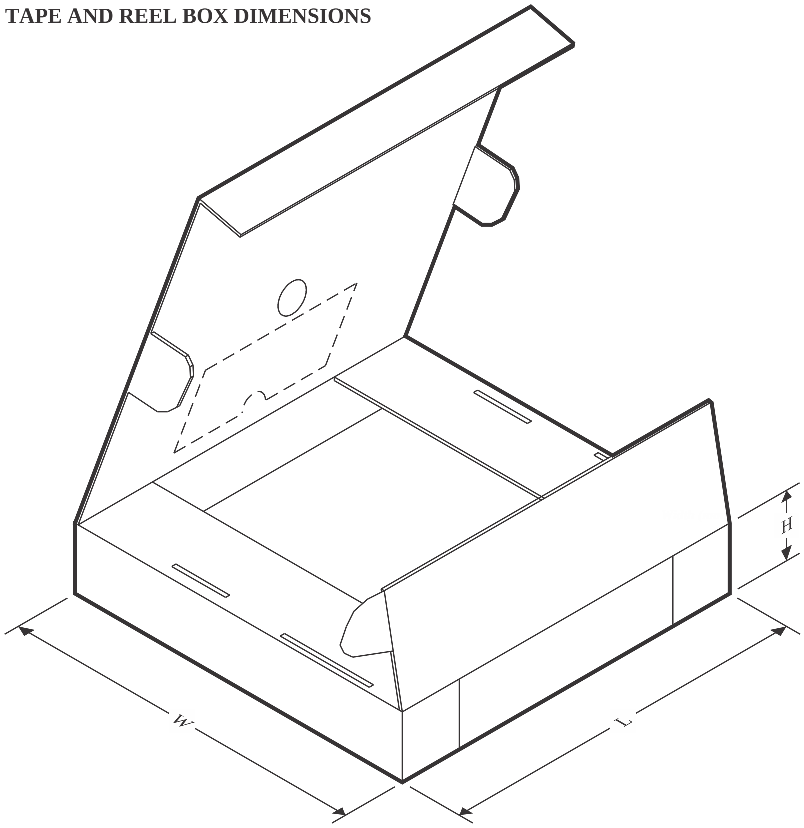
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC6482AIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC6482AIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LMC6482IMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMC6482IMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMC6482IMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LMC6484AIMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMC6484IMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

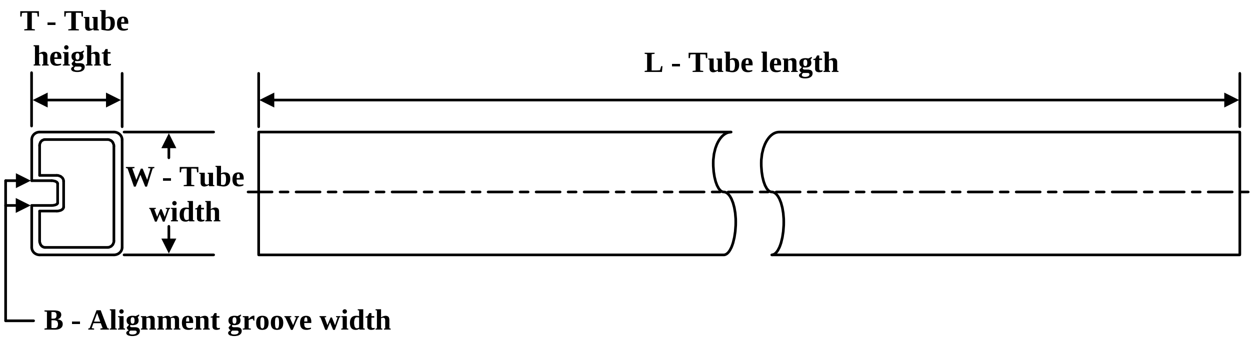
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

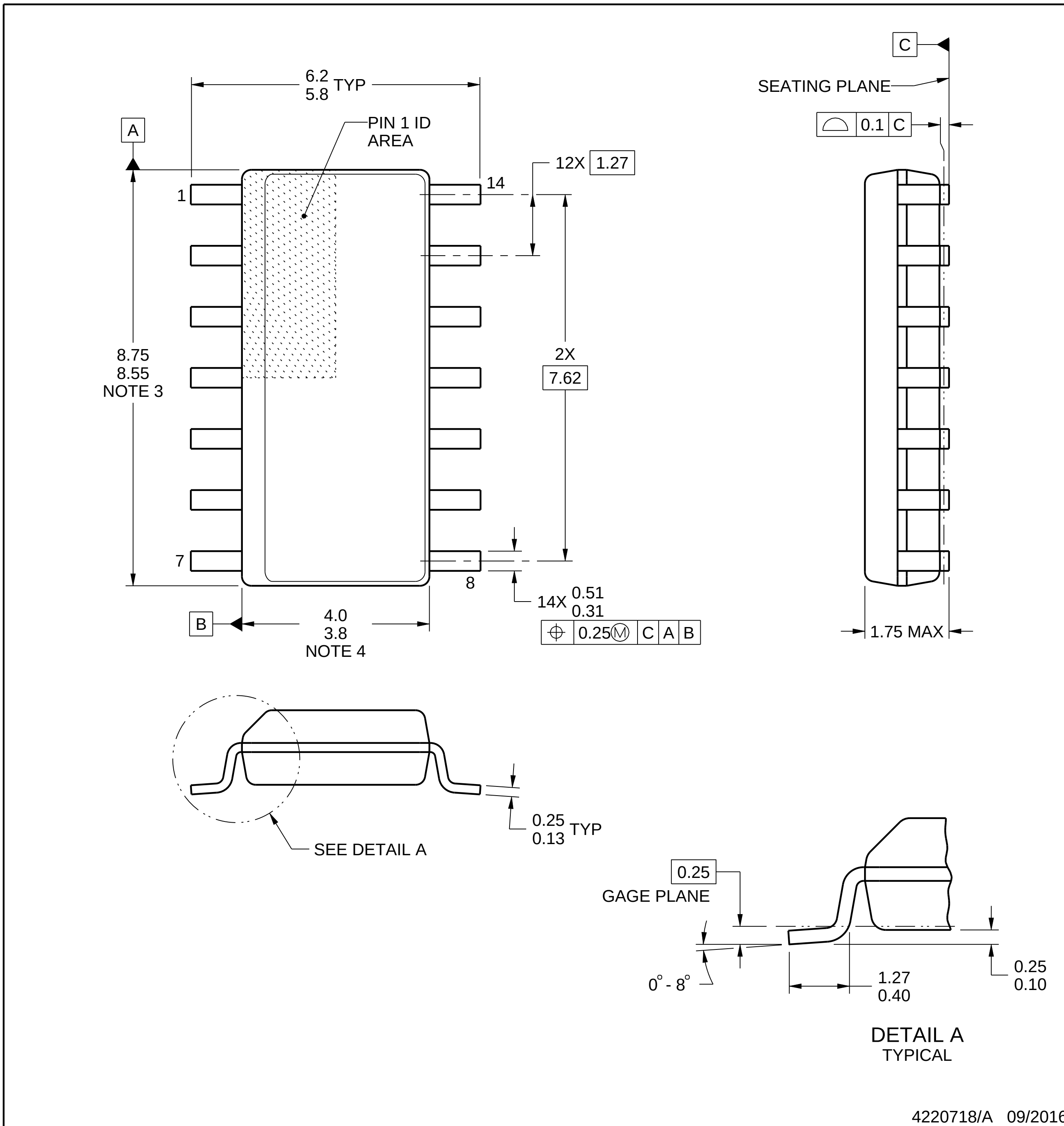
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC6482AIMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMC6482AIMX/NOPB	SOIC	D	8	2500	353.0	353.0	32.0
LMC6482IMMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMC6482IMMX/NOPB	VSSOP	DGK	8	3500	353.0	353.0	32.0
LMC6482IMX/NOPB	SOIC	D	8	2500	353.0	353.0	32.0
LMC6484AIMX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0
LMC6484IMX/NOPB	SOIC	D	14	2500	353.0	353.0	32.0

TUBE



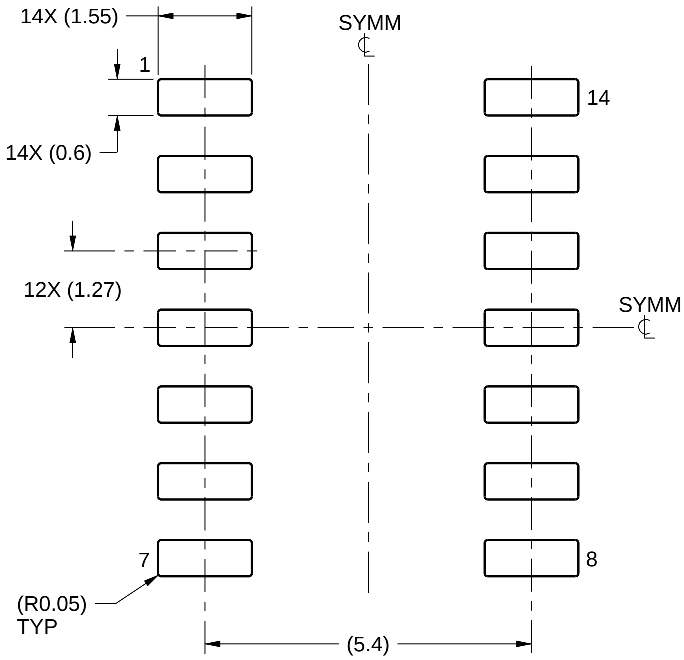
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMC6482AIN/NOPB	P	PDIP	8	40	502	14	11938	4.32
LMC6482AIN/NOPB.A	P	PDIP	8	40	502	14	11938	4.32
LMC6482AIN/NOPB.B	P	PDIP	8	40	502	14	11938	4.32
LMC6482IN/NOPB	P	PDIP	8	40	506	13.97	11230	4.32
LMC6482IN/NOPB.A	P	PDIP	8	40	506	13.97	11230	4.32
LMC6482IN/NOPBG4	P	PDIP	8	40	506	13.97	11230	4.32
LMC6482IN/NOPBG4.A	P	PDIP	8	40	506	13.97	11230	4.32
LMC6484AIN/NOPB	N	PDIP	14	25	502	14	11938	4.32
LMC6484AIN/NOPB.A	N	PDIP	14	25	502	14	11938	4.32
LMC6484IN/NOPB	N	PDIP	14	25	502	14	11938	4.32
LMC6484IN/NOPB.A	N	PDIP	14	25	502	14	11938	4.32

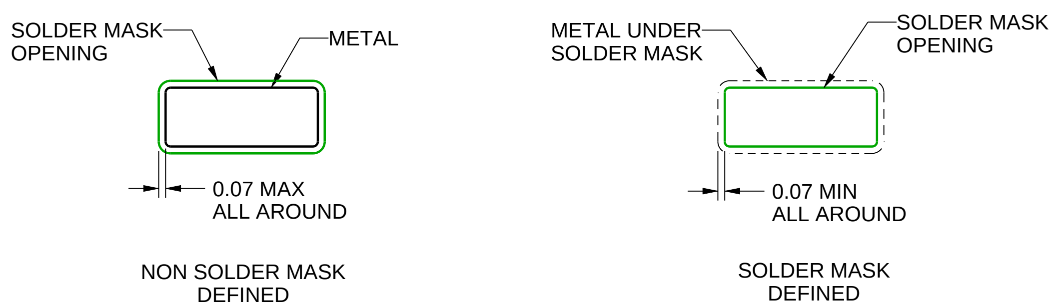


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X

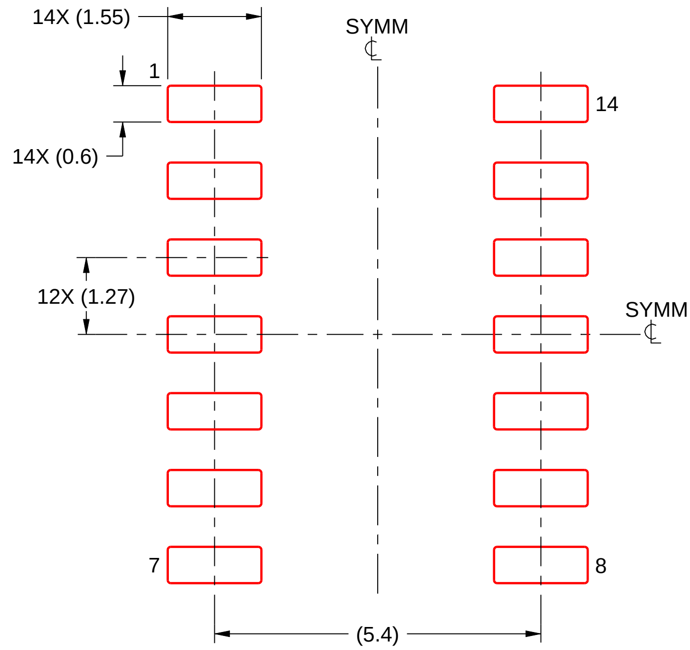


SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

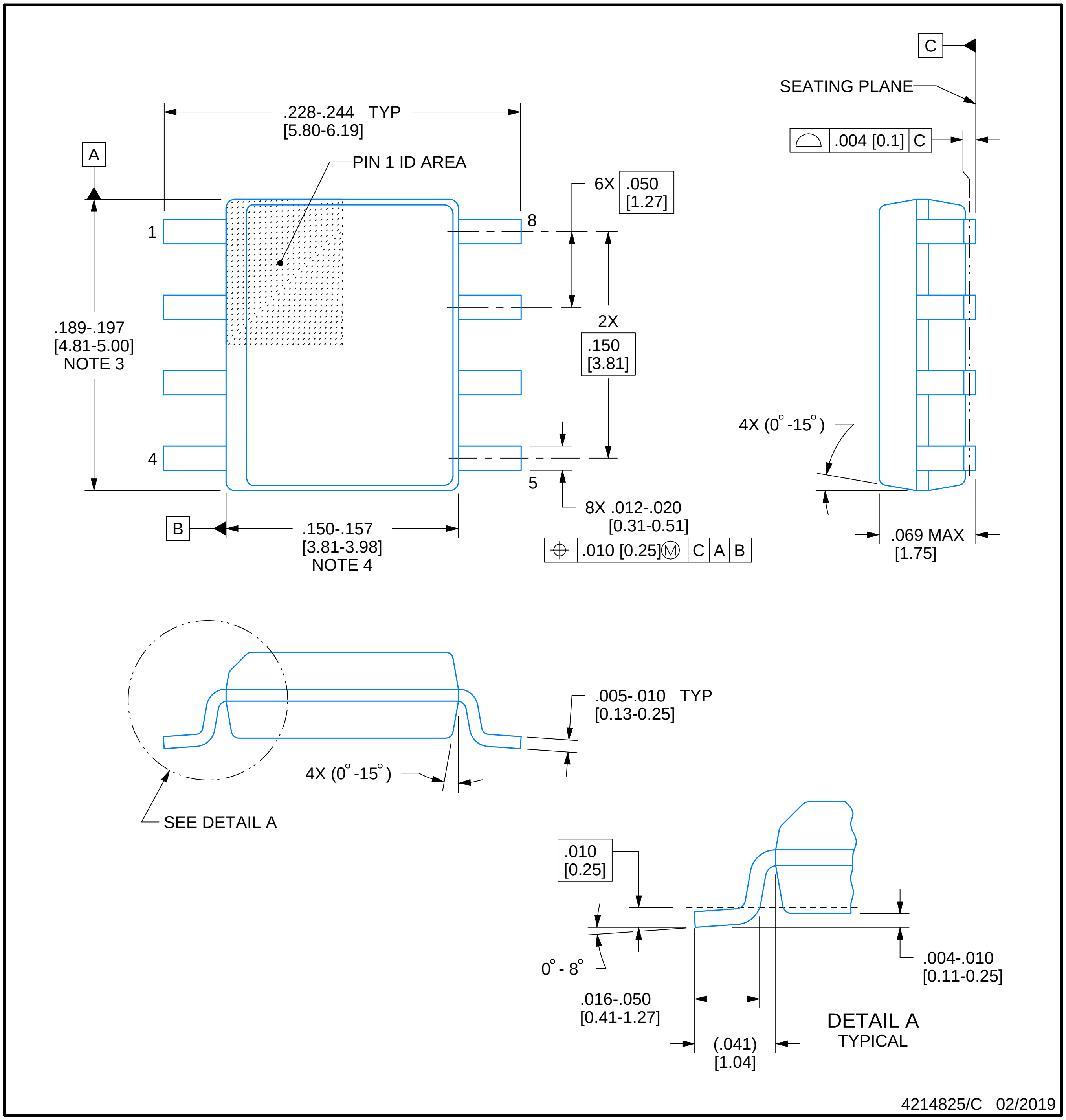


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

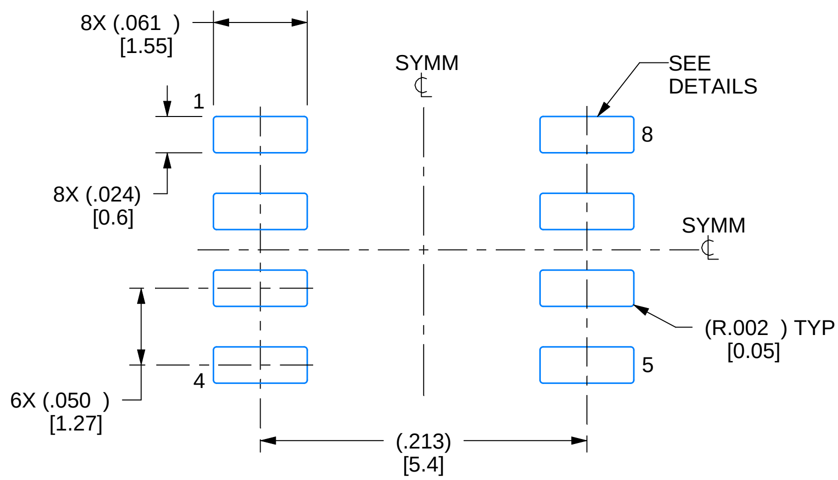
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

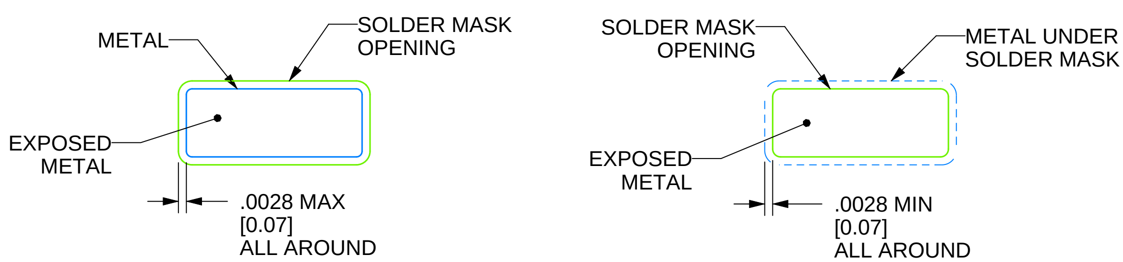


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED

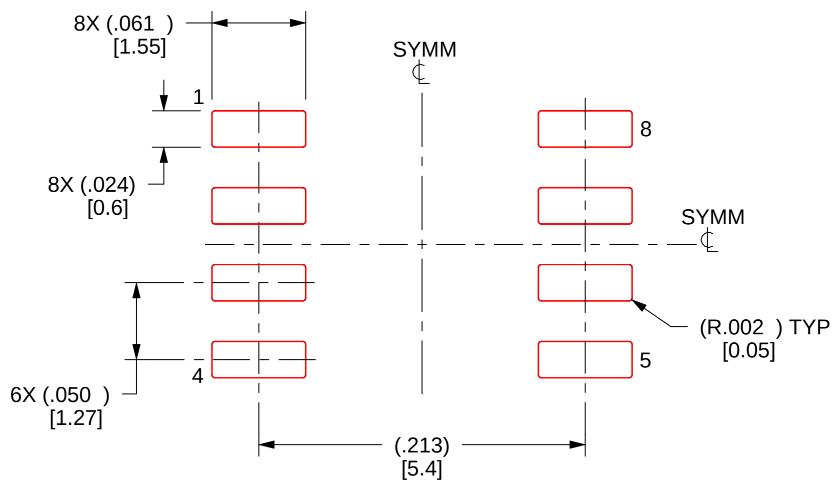
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



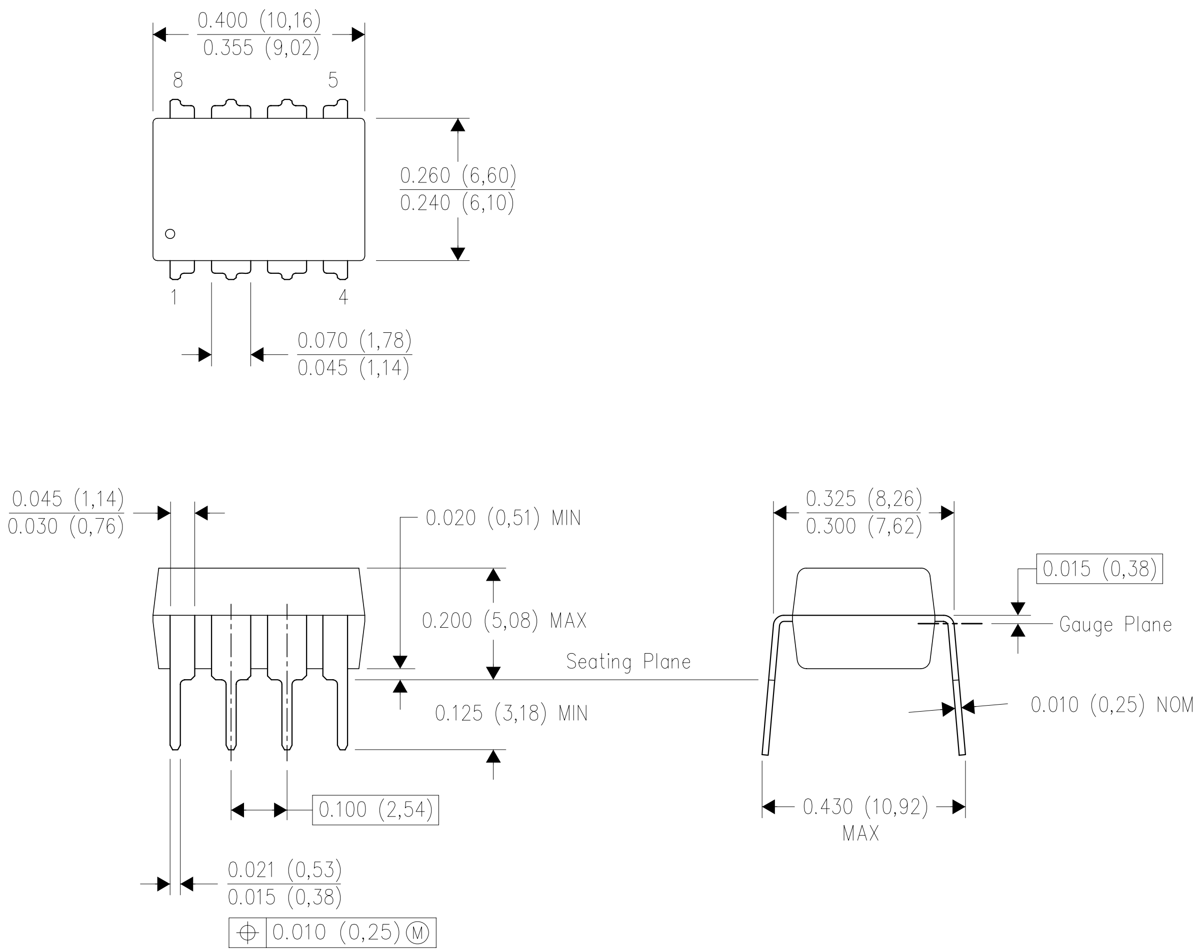
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

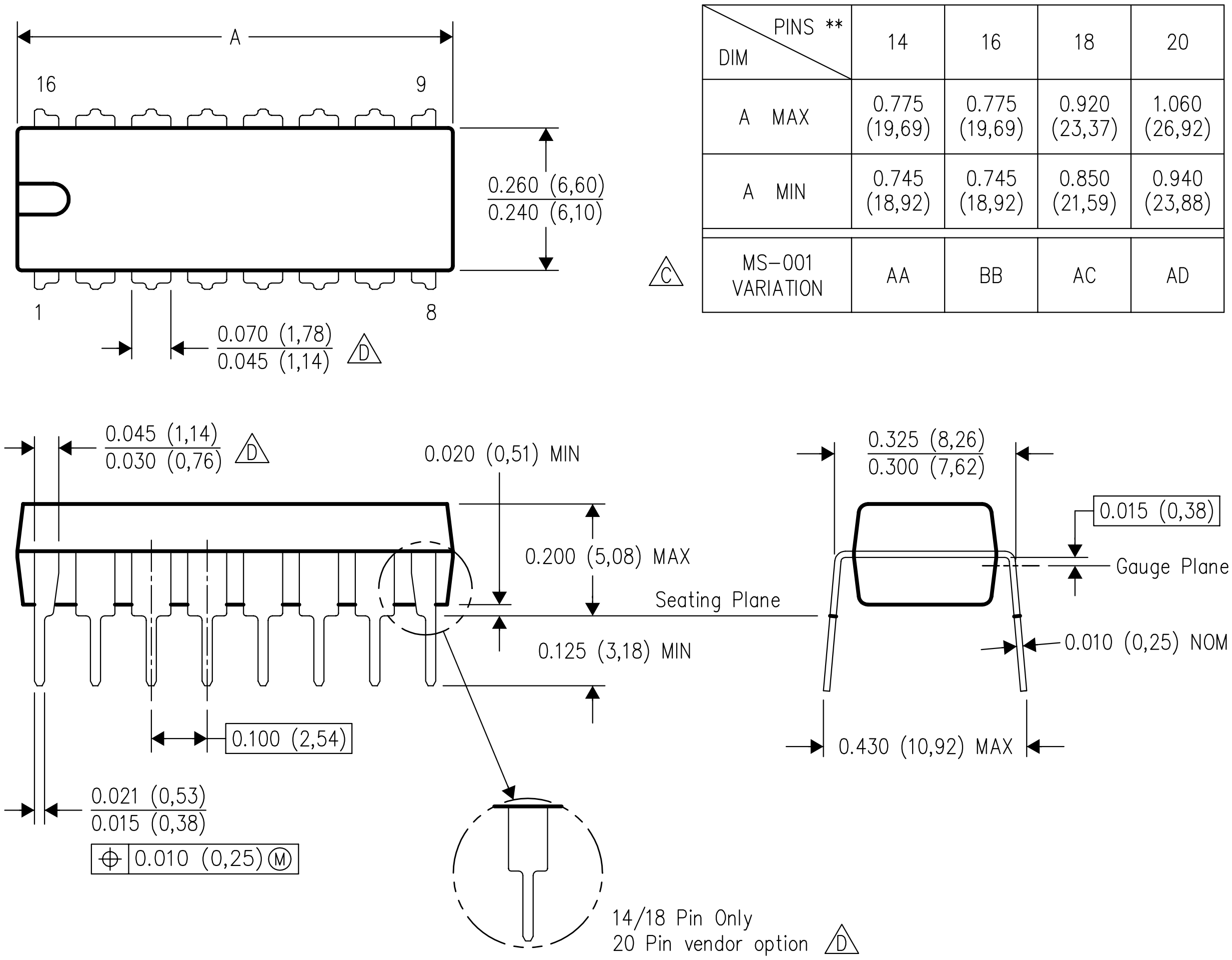


4040082/E 04/2010

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

N (R-PDIP-T**) PLASTIC DUAL-IN-LINE PACKAGE

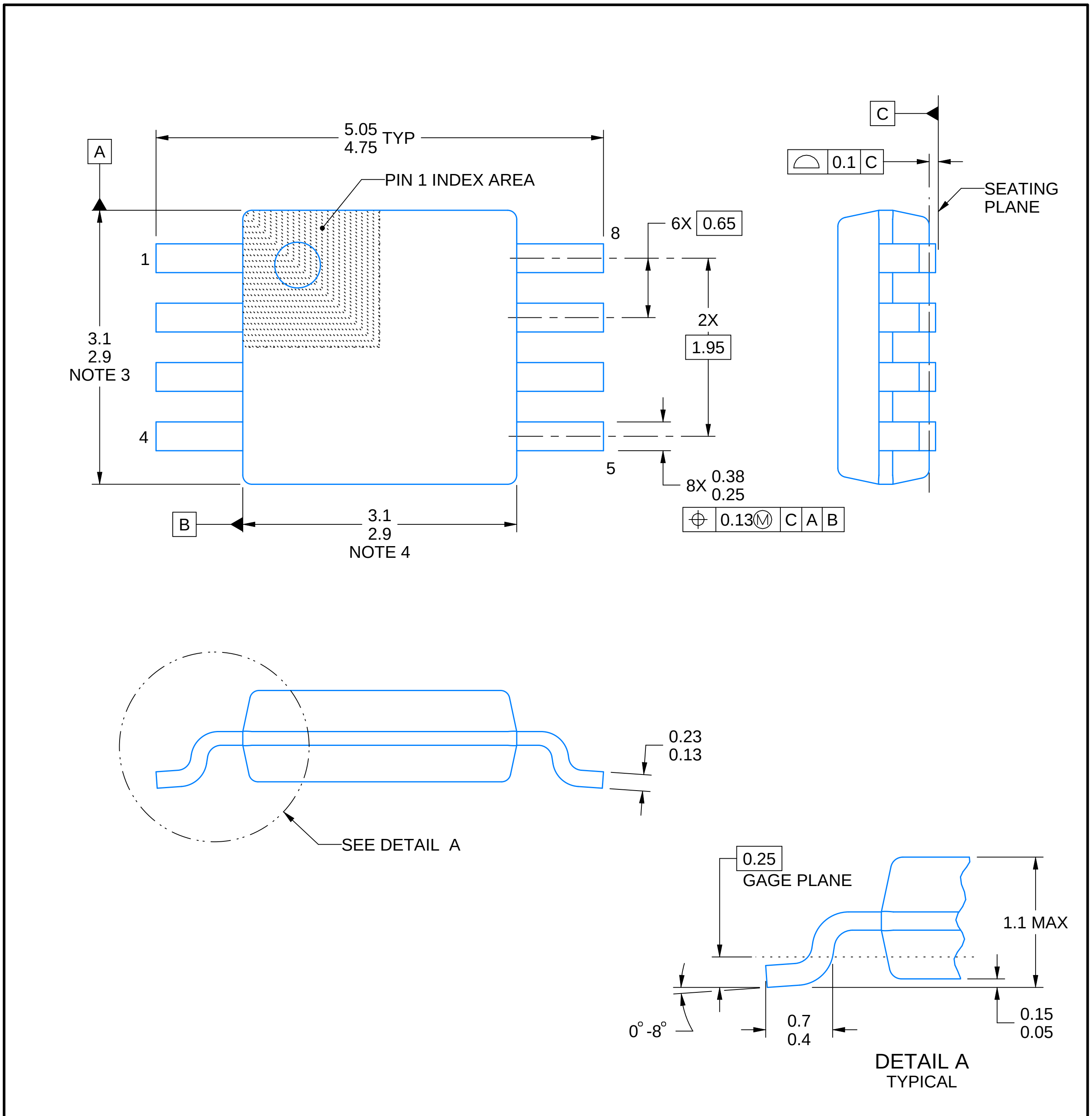
16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD

4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

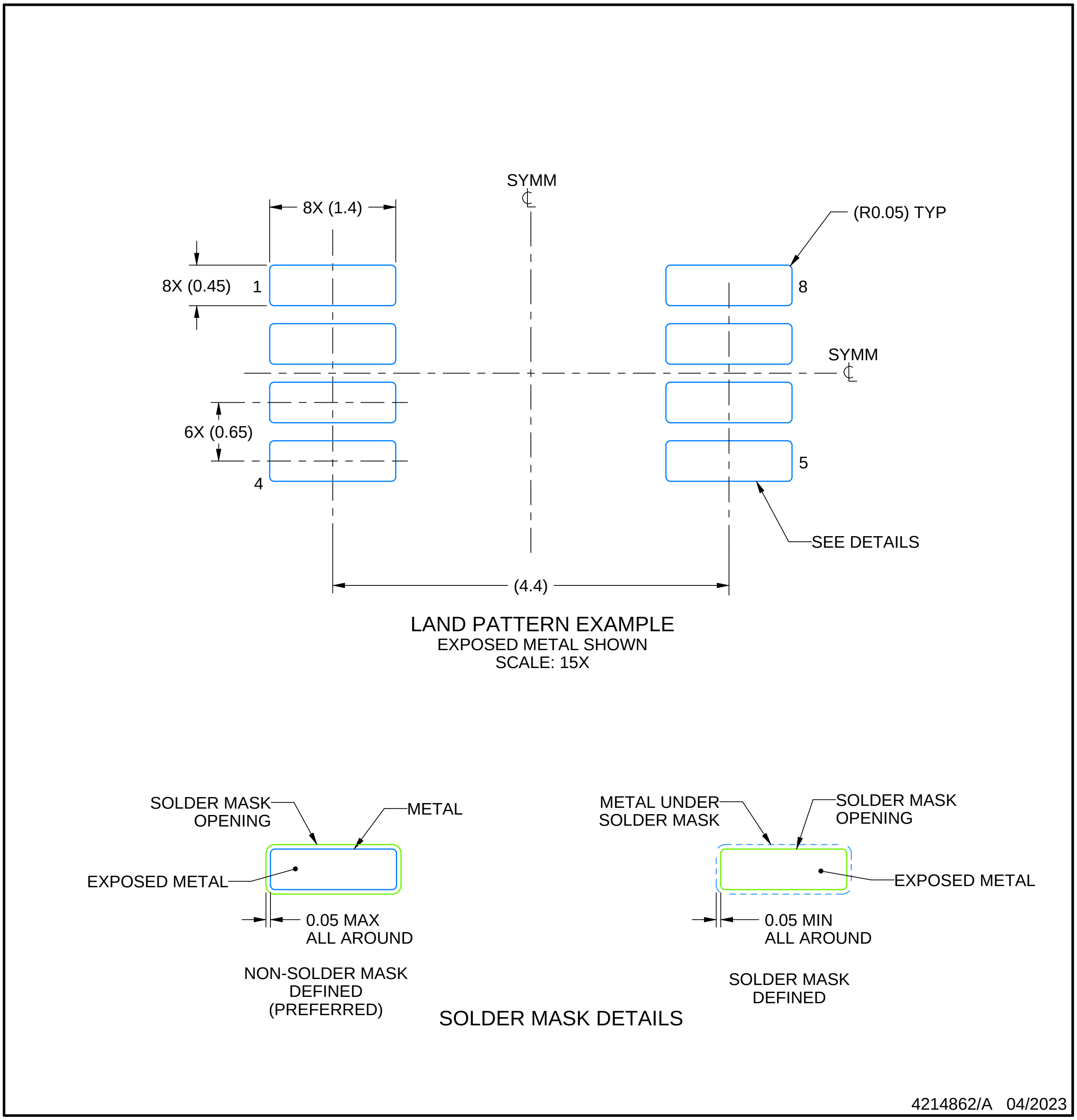


4214862/A 04/2023

PowerPAD is a trademark of Texas Instruments.

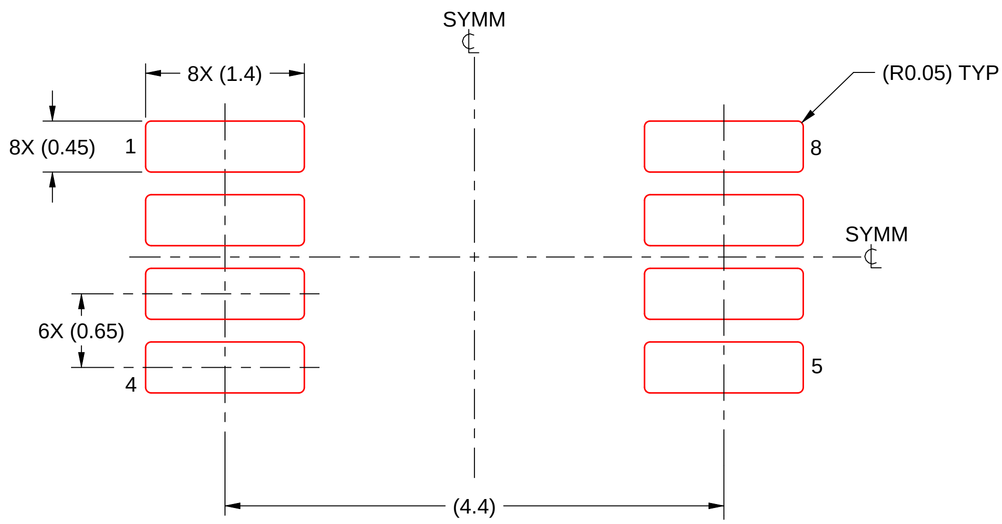
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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