

## LM74930-Q1 Automotive Ideal Diode Surge Stopper With Circuit Breaker, Overvoltage Protection, and Fault Output

## 1 Features

- AEC-Q100 qualified for automotive applications
  - Device temperature grade 1:  
–40°C to +125°C ambient operating temperature range
- 4-V to 65-V input range
- Reverse input protection down to -65 V
- Drives external back-to-back N-Channel MOSFETs in common source configuration
- Ideal diode operation with 10.5-mV A to C forward voltage drop regulation
- Low reverse detection threshold (-10.5 mV) with fast DGATE turn-off response (0.5  $\mu$ s)
- 18-mA peak gate (DGATE) turn on current
- 2.6-A peak DGATE turn-off current
- Adjustable overcurrent and short circuit protection
- Analog current monitor output with 10% accuracy (IMON)
- Adjustable overvoltage and undervoltage protection
- Low 2.5- $\mu$ A shutdown current (EN=Low)
- MODE pin to allow bi-directional current flow (MODE=Low)
- Meets automotive ISO7637 transient requirements with a suitable TVS diode
- Available in space saving 24-pin VQFN package

## 2 Applications

- 12-V / 24-V automotive reverse battery protection
- Industrial transport
- Redundant power supply ORing

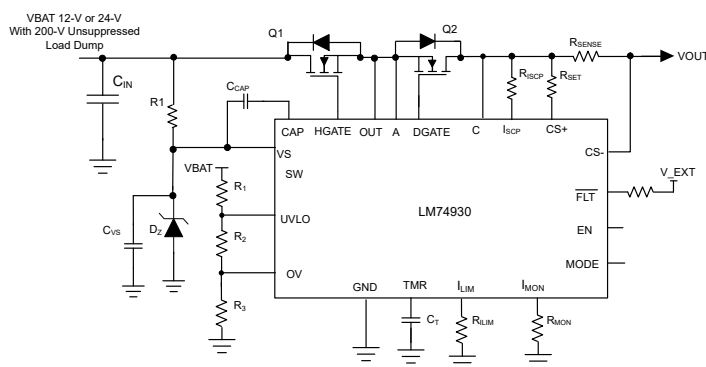
### 3 Description

The LM74930-Q1 ideal diode controller drives and controls external back to back N-Channel MOSFETs to emulate an ideal diode rectifier and power path ON and OFF control with over current and overvoltage protection. The wide input supply of 4 V to 65 V allows protection and control of 12-V and 24-V automotive battery powered ECUs. The device can withstand and protect the loads from negative supply voltages down to -65 V. An integrated high side gate control (HGATE) drives the first MOSFET in the power path. The device allows load disconnect (ON and OFF control) in case of overcurrent, overvoltage and undervoltage event using HGATE control while ideal diode controller (DGATE) drives a second MOSFET to replace a Schottky diode for input reverse polarity protection and output voltage holdup by blocking the reverse current from output to input. The device has integrated current sense amplifier which provides with an adjustable overcurrent and short circuit protection with circuit breaker functionality. The device features an adjustable overvoltage and undervoltage protection feature to protect against supply transients. LM74930-Q1 features MODE pin which can be used to selectively enable or disable reverse current blocking functionality.

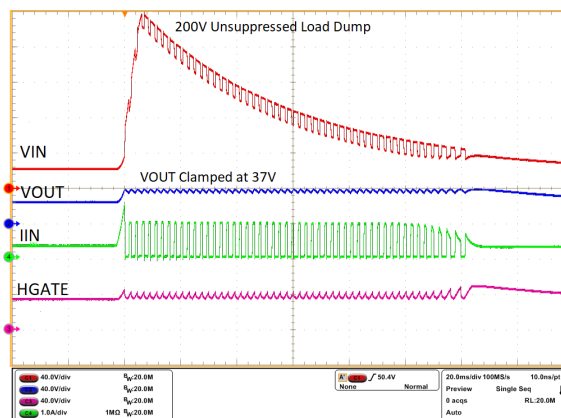
## Package Information

| PART NUMBER | PACKAGE <sup>(1)</sup> | PACKAGE SIZE <sup>(2)</sup> |
|-------------|------------------------|-----------------------------|
| LM74930-Q1  | RGE (VQFN, 24)         | 4.0 mm × 4.0 mm             |

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.



### Ideal Diode With 200-V Load Dump Protection



### Unsuppressed Load Dump 200 V - Output Clamp

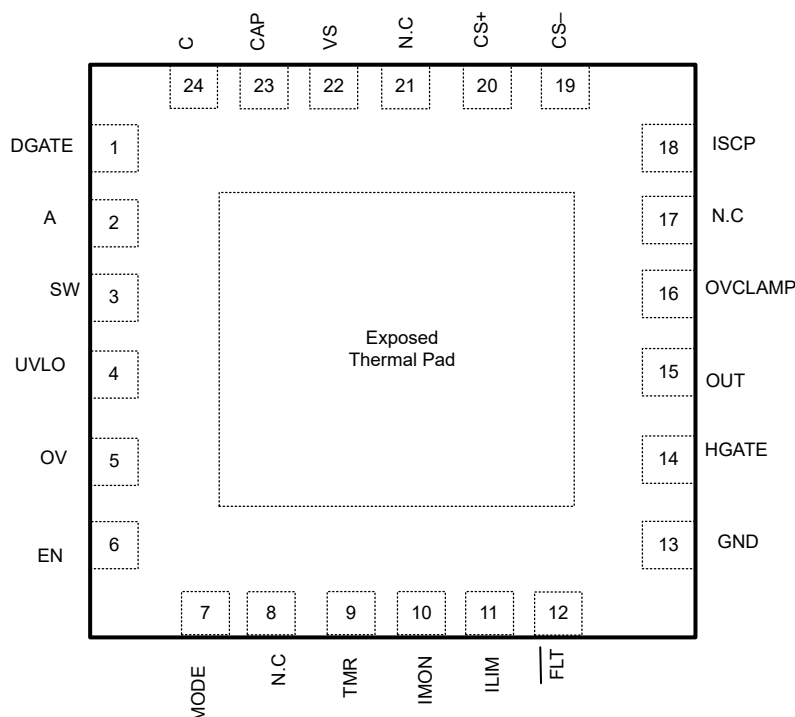
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## 4 Revision History

| DATE         | REVISION | NOTES            |
|--------------|----------|------------------|
| October 2023 | *        | Initial release. |

## 5 Pin Configuration and Functions



**Figure 5-1. VQFN 24-Pin RGE Transparent Top View**

**Table 5-1. Pin Functions**

| PIN   |                             | TYPE <sup>(1)</sup> | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                       |
|-------|-----------------------------|---------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME  | LM74930-Q1<br>RGE-24 (VQFN) |                     |                                                                                                                                                                                                                                                                                                                                                                   |
| DGATE | 1                           | O                   | Diode Controller Gate Drive Output. Connect to the GATE of the external ideal diode MOSFET.                                                                                                                                                                                                                                                                       |
| A     | 2                           | I                   | Anode of the ideal diode. Connect to the source of the external ideal diode MOSFET.                                                                                                                                                                                                                                                                               |
| SW    | 3                           | I                   | Voltage sensing disconnect switch terminal. A and SW are internally connected through a switch. Use SW as the top connection of the resistor ladder to measure voltage at the common source node. When EN is pulled low, the switch is OFF. If the internal disconnect switch between A and SW is not used then SW pin can be left floating.                      |
| UVLO  | 4                           | I                   | Adjustable undervoltage threshold input. Connect a resistor ladder across VIN to UVLO terminal to GND. When the voltage at UVLO goes below the undervoltage cut-off threshold then the HGATE is pulled low turning OFF the HSFET. HGATE turns ON when the sense voltage goes above the UVLO falling threshold. When not used UVLO should be tied to VS or EN pin. |
| OV    | 5                           | I                   | Adjustable overvoltage threshold input. Connect a resistor ladder across VIN/ VOUT to OV terminal. When the voltage at OVP exceeds the overvoltage cut-off threshold then the HGATE is pulled low turning OFF the HSFET. HGATE turns ON when the sense voltage goes below the OVP falling threshold. When not used OV should be tied to ground.                   |
| EN    | 6                           | I                   | EN Input. Connect to VS pin for always ON operation. Can be driven externally from a micro controller I/O. Pulling this pin low below V <sub>(ENF)</sub> makes the device enter into low I <sub>q</sub> shutdown mode.                                                                                                                                            |

**Table 5-1. Pin Functions (continued)**

| PIN     |               | TYPE <sup>(1)</sup> | DESCRIPTION                                                                                                                                                                                                                                            |
|---------|---------------|---------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME    | LM74930-Q1    |                     |                                                                                                                                                                                                                                                        |
|         | RGE-24 (VQFN) |                     |                                                                                                                                                                                                                                                        |
| MODE    | 7             | I                   | MODE input to disable reverse current blocking function of DGATE. MODE pin can be driven from the microcontroller. When pulled low device disables reverse current blocking feature (DGATE). When not used, MODE pin can be pulled to EN or VS.        |
| N.C     | 8             | —                   | No Connection. Keep this pin floating.                                                                                                                                                                                                                 |
| TMR     | 9             | —                   | Fault timer input. A capacitor across TMR pin to GND sets the times for fault warning, fault turn-off (FLT), and retry periods. Leave it open for fastest setting. Connect TMR to GND to disable overcurrent protection.                               |
| IMON    | 10            | O                   | Analog current monitor output. This pin sources a scaled down ratio of current through the external current sense resistor $R_{SENSE}$ . A resistor from this pin to GND converts current to proportional voltage. If unused, leave this pin floating. |
| ILIM    | 11            | —                   | Overcurrent detection setting. A resistor across ILIM to GND sets the overcurrent comparator threshold. Connect ILIM to GND if overcurrent protection feature is not desired.                                                                          |
| FLT     | 12            | O                   | Open drain fault output. FLT pin is pulled low in case of undervoltage, overvoltage, overcurrent and short circuit event.                                                                                                                              |
| GND     | 13            | G                   | Connect to the system ground plane                                                                                                                                                                                                                     |
| HGATE   | 14            | O                   | GATE driver output for the HSFET. Connect to the GATE of the external load switch MOSFET.                                                                                                                                                              |
| OUT     | 15            | I                   | Connect to the common source rail (external load switch MOSFET source)                                                                                                                                                                                 |
| OVCLAMP | 16            | I                   | Connect this pin to OV pin for overvoltage clamp with circuit breaker (timer) functionality. Connect this pin to ground when not used.                                                                                                                 |
| N.C     | 17            | —                   | No Connection. Keep this pin floating.                                                                                                                                                                                                                 |
| ISCP    | 18            | I                   | Short-circuit detection threshold setting. When ISCP is connected to C, device sets an internal fix threshold of 20 mV for output short circuit detection.                                                                                             |
| CS-     | 19            | I                   | Current sense negative input.                                                                                                                                                                                                                          |
| CS+     | 20            | I                   | Current sense positive input. Connect a 50-Ω resistor across CS+ to the external current sense resistor.                                                                                                                                               |
| N.C     | 21            | —                   | No Connection. Keep this pin floating.                                                                                                                                                                                                                 |
| VS      | 22            | P                   | Input power supply to the IC. Connect a 100-nF capacitor across VS and GND pin.                                                                                                                                                                        |
| CAP     | 23            | O                   | Internal charge pump output. Connect a 100-nF capacitor across CAP and VS pin.                                                                                                                                                                         |
| C       | 24            | I                   | Cathode of the ideal diode. Connect to the drain of the external ideal diode MOSFET.                                                                                                                                                                   |
| RTN     | Thermal pad   | —                   | Leave exposed pad floating. Do Not connect to GND plane.                                                                                                                                                                                               |

(1) I = input, O = output, I/O = input and output, P = power, G = Ground

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                                                      |                                                                                  | MIN                | MAX               | UNIT |
|------------------------------------------------------|----------------------------------------------------------------------------------|--------------------|-------------------|------|
| Input pins                                           | A to GND                                                                         | –65                | 70                | V    |
|                                                      | C, VS, CS+, CS–, ISCP to GND                                                     | –1                 | 70                |      |
|                                                      | SW, EN, MODE, UVLO, OV, OVCLAMP to GND, $V_{(A)} > 0$ V                          | –0.3               | 70                |      |
|                                                      | OUT, EN, MODE, UVLO, OV, OVCLAMP to GND, $V_{(A)} \leq 0$ V                      | $V_{(A)}$          | $(70 + V_{(A)})$  |      |
|                                                      | SW, $V_{(A)} \leq 0$ V                                                           | $V_{(A)}$          | $(0.3 + V_{(A)})$ |      |
|                                                      | RTN to GND                                                                       | –65                | 0.3               | mA   |
|                                                      | $I_{SW}$ , $I_{FLT}$                                                             | –1                 | 10                |      |
|                                                      | TMR, ILIM                                                                        | –0.3               | 5.5               | V    |
|                                                      | $I_{EN}$ , $I_{MODE}$ , $I_{OV}$ , $I_{OVCLAMP}$ , $I_{UVLO}$ $V_{(A)} > 0$ V    | –1                 |                   | mA   |
|                                                      | $I_{EN}$ , $I_{MODE}$ , $I_{OV}$ , $I_{OVCLAMP}$ , $I_{UVLO}$ $V_{(A)} \leq 0$ V | Internally limited |                   |      |
|                                                      | ISCP, CS+ to CS–                                                                 | –0.3               | 0.3               | V    |
| Output pins                                          | OUT to VS                                                                        | –65                | 16.5              | V    |
|                                                      | CAP to VS                                                                        | –0.3               | 15                | V    |
|                                                      | CAP to A, OUT                                                                    | –0.3               | 85                |      |
|                                                      | DGATE to A                                                                       | –0.3               | 15                |      |
|                                                      | FLT to GND                                                                       | –1                 | 70                |      |
|                                                      | IMON                                                                             | –0.3               | 5.5               |      |
|                                                      | HGATE to OUT                                                                     | –0.3               | 15                |      |
| Output to input pins                                 | C to A                                                                           | –5                 | 85                |      |
| Operating junction temperature, $T_j$ <sup>(2)</sup> | Operating junction temperature, $T_j$                                            | –40                | 150               | °C   |
| Storage temperature, $T_{stg}$                       |                                                                                  | –40                | 150               | °C   |

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

### 6.2 ESD Ratings

|             |                         |                                                                                        |                                                       | VALUE | UNIT |
|-------------|-------------------------|----------------------------------------------------------------------------------------|-------------------------------------------------------|-------|------|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 <sup>(1)</sup> HBM ESD classification level 2 |                                                       | ±2000 | V    |
|             |                         | Charged device model (CDM), per AEC Q100-011, CDM ESD classification level C4B         | Corner pins (DGATE, EN, MODE, FLT, GND, ISCP, CS–, C) | ±750  |      |
|             |                         |                                                                                        | Other pins                                            | ±500  |      |

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                      |                               | MIN | NOM | MAX | UNIT |
|----------------------|-------------------------------|-----|-----|-----|------|
| Input pins           | A to GND                      | –60 |     | 65  | V    |
|                      | VS, SW, CS+, CS–, ISCP to GND | 0   |     | 65  | V    |
|                      | EN, UVLO, OV, MODE to GND     | 0   |     | 65  | V    |
| External capacitance | CAP to VS, VS to GND          | 0.1 |     |     | µF   |

### 6.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                                |                                               | MIN | NOM | MAX | UNIT |
|--------------------------------|-----------------------------------------------|-----|-----|-----|------|
| External MOSFET max VGS rating | DGATE to A and HGATE to OUT                   | 15  |     |     | V    |
| T <sub>J</sub>                 | Operating Junction temperature <sup>(2)</sup> | –40 |     | 150 | °C   |

- (1) Recommended Operating Conditions are conditions under which the device is intended to be functional. For specifications and test conditions, see Electrical Characteristics.
- (2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

### 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | LM74930-Q1 | UNIT |
|-------------------------------|----------------------------------------------|------------|------|
|                               |                                              | RGE (VQFN) |      |
|                               |                                              | 24 PINS    |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 44         | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 38.3       | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 21.3       | °C/W |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 0.8        | °C/W |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 21.3       | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | 5.9        | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

### 6.5 Electrical Characteristics

T<sub>J</sub> = –40°C to +125°C; typical values at T<sub>J</sub> = 25°C, V<sub>(A)</sub> = V<sub>(OUT)</sub> = V<sub>(VS)</sub> = 12 V, V<sub>(AC)</sub> = 20 mV, C<sub>(VCAP)</sub> = 0.1 μF, V<sub>(EN/UVLO)</sub> = 2 V, over operating free-air temperature range (unless otherwise noted)

| PARAMETER                       |                                                                  | TEST CONDITIONS                 | MIN   | TYP  | MAX  | UNIT |
|---------------------------------|------------------------------------------------------------------|---------------------------------|-------|------|------|------|
| SUPPLY VOLTAGE                  |                                                                  |                                 |       |      |      |      |
| V <sub>(VS)</sub>               | Operating input voltage                                          |                                 | 4     |      | 65   | V    |
| V <sub>(VS_PORR)</sub>          | VS POR threshold, rising                                         |                                 | 2.4   | 2.6  | 2.9  | V    |
| V <sub>(VS_PORF)</sub>          | VS POR threshold, falling                                        |                                 | 2.2   | 2.1  | 2.7  | V    |
| I <sub>(SHDN)</sub>             | Shutdown current, I <sub>(GND)</sub>                             | V <sub>(EN)</sub> = 0 V         |       | 2.5  | 5    | μA   |
| I <sub>(Q)</sub>                | Total system quiescent current, I <sub>(GND)</sub>               | V <sub>(EN)</sub> = 2 V         |       | 665  | 780  | μA   |
| I <sub>(REV)</sub>              | I <sub>(A)</sub> leakage current during reverse polarity,        | 0 V ≤ V <sub>(A)</sub> ≤ − 65 V | −100  | −35  |      | μA   |
|                                 | I <sub>(OUT)</sub> leakage current during reverse polarity       |                                 | −1    | −0.3 |      | μA   |
| ENABLE                          |                                                                  |                                 |       |      |      |      |
| V <sub>(ENR)</sub>              | Enable threshold voltage for low I <sub>q</sub> shutdown, rising |                                 |       | 0.8  | 1.05 | V    |
| V <sub>(ENF)</sub>              | Enable falling threshold voltage for low I <sub>q</sub> shutdown |                                 | 0.41  | 0.7  |      | V    |
| I <sub>(EN/UVLO)</sub>          |                                                                  | 0 V ≤ V <sub>(EN)</sub> ≤ 65 V  |       | 55   | 200  | nA   |
| MODE                            |                                                                  |                                 |       |      |      |      |
| V <sub>(MODEF)</sub>            | MODE falling threshold voltage                                   |                                 | 0.41  | 0.7  |      | V    |
| V <sub>(MODER)</sub>            | MODE threshold, rising                                           |                                 |       | 0.8  | 1.05 | V    |
| I <sub>(MODE)</sub>             | MODE input leakage current                                       |                                 |       | 100  | 160  | nA   |
| UNDERVOLTAGE LOCKOUT COMPARATOR |                                                                  |                                 |       |      |      |      |
| V <sub>(UVLOR)</sub>            | UVLO threshold voltage, rising                                   |                                 | 0.585 | 0.6  | 0.63 | V    |

## 6.5 Electrical Characteristics (continued)

$T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ; typical values at  $T_J = 25^{\circ}\text{C}$ ,  $V_{(A)} = V_{(OUT)} = V_{(VS)} = 12\text{ V}$ ,  $V_{(AC)} = 20\text{ mV}$ ,  $C_{(VCAP)} = 0.1\text{ }\mu\text{F}$ ,  $V_{(EN/UVLO)} = 2\text{ V}$ , over operating free-air temperature range (unless otherwise noted)

| PARAMETER                                               |                                                             | TEST CONDITIONS                                                                                                   | MIN   | TYP   | MAX   | UNIT          |
|---------------------------------------------------------|-------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------|-------|-------|-------|---------------|
| $V_{(UVLOF)}$                                           | UVLO threshold voltage, falling                             |                                                                                                                   | 0.533 | 0.55  | 0.573 | V             |
| $I_{(UVLO)}$                                            |                                                             | $0\text{ V} \leq V_{(UVLO)} \leq 5\text{ V}$                                                                      |       | 50    | 200   | nA            |
| <b>OVERVOLTAGE PROTECTION AND BATTERY SENSING INPUT</b> |                                                             |                                                                                                                   |       |       |       |               |
| $R_{(SW)}$                                              | Battery sensing disconnect switch resistance                |                                                                                                                   | 10    | 19.5  | 46    | $\Omega$      |
| $V_{(OVR)}$                                             | Overvoltage threshold input, rising                         |                                                                                                                   | 0.585 | 0.6   | 0.63  | V             |
| $V_{(OVF)}$                                             | Overvoltage threshold input, falling                        |                                                                                                                   | 0.533 | 0.55  | 0.573 | V             |
| $I_{(OV)}$                                              | OV Input leakage current                                    | $0\text{ V} \leq V_{(OV)} \leq 5\text{ V}$                                                                        |       | 50    | 200   | nA            |
| $V_{(OVCLAMP R)}$                                       | OVCLAMP threshold input, rising                             |                                                                                                                   | 0.57  | 0.59  | 0.61  | V             |
| $V_{(OVCLAMP F)}$                                       | OVCLAMP threshold input, falling                            |                                                                                                                   | 0.435 | 0.45  | 0.475 | V             |
| $I_{(OVCLAMP)}$                                         | OVCLAMP Input leakage current                               | $0\text{ V} \leq V_{(OV)} \leq 5\text{ V}$                                                                        |       | 53    | 200   | nA            |
| <b>CURRENT SENSE AMPLIFIER</b>                          |                                                             |                                                                                                                   |       |       |       |               |
| $V_{(OFFSET)}$                                          | Input referred offset                                       | $R_{SET} = 50\Omega$ $R_{IMON} = 5\text{ k}\Omega$<br>(corresponds to $V_{SNS} = 6\text{ mV}$ to $30\text{ mV}$ ) | -2.1  |       | 2.1   | mV            |
| $V_{(GE\_SET)}$                                         | $V_{SNS}$ to $V_{IMON}$ scaling                             | $R_{SET} = 50\Omega$ $R_{IMON} = 5\text{ k}\Omega$<br>(corresponds to $V_{SNS} = 6\text{ mV}$ to $30\text{ mV}$ ) | 82    | 90    | 97    |               |
| $V_{(SNS\_TH)}$                                         | OCP comparator rising threshold                             |                                                                                                                   | 1.08  | 1.22V | 1.32  | V             |
|                                                         | OCP comparator falling threshold                            |                                                                                                                   | 1.02  | 1.15  | 1.25  | V             |
| $I_{SCP}$                                               | SCP input bias current                                      |                                                                                                                   | 9.5   | 11    | 12    | $\mu\text{A}$ |
| $V_{(HV\_SCP)}$                                         | HV SCP comparator threshold                                 | $V_{CS-} > 3\text{ V}$                                                                                            | 17.4  | 20    | 22    | mV            |
| $V_{(HV\_SCP)}$                                         | HV SCP comparator threshold                                 | $R_{ISCP} = 1\text{ k}\Omega$                                                                                     |       | 31    |       | mV            |
| IMON Accuracy                                           | Current monitor output accuracy                             | $V_{SENSE} = 20\text{ mV}$ , $R_{IMON} = 5\text{ k}\Omega$                                                        | -12.5 |       | 12.5  | %             |
| $V_{(LV\_SCP)}$                                         | LV SCP comparator threshold                                 | $V_{CS-} < 3\text{ V}$                                                                                            | 16.5  | 20    | 24    | mV            |
| <b>FAULT</b>                                            |                                                             |                                                                                                                   |       |       |       |               |
| $R_{(FLT)}$                                             | FLT pull-down resistance                                    |                                                                                                                   | 10    | 22    | 60    | $\Omega$      |
| $I_{\_FLT}$                                             | FLT input leakage current                                   |                                                                                                                   | -100  |       | 400   | nA            |
| <b>DELAY TIMER</b>                                      |                                                             |                                                                                                                   |       |       |       |               |
| $I_{(TMR\_SRC\_OCP)}$                                   | TMR source current during overcurrent                       |                                                                                                                   | 65    | 85    | 97    | $\mu\text{A}$ |
| $I_{(TMR\_SRC\_OVCLAMP)}$                               | TMR source current during overvoltage clamp                 |                                                                                                                   | 4.5   | 5.5   | 6.6   | $\mu\text{A}$ |
| $I_{(TMR\_SRC\_FLT)}$                                   | TMR source current                                          |                                                                                                                   | 1.94  | 2.97  | 3.5   | $\mu\text{A}$ |
| $I_{(TMR\_SNK)}$                                        | TMR sink current                                            |                                                                                                                   | 2     | 2.7   | 3.15  | $\mu\text{A}$ |
| $V_{(TMR\_OC)}$                                         | Voltage at TMR pin for ILIM shut off                        |                                                                                                                   | 1.1   | 1.2   | 1.4   | V             |
| $V_{(TMR\_FLT)}$                                        | Voltage at TMR pin for FLT trigger                          |                                                                                                                   | 1.04  | 1.1   | 1.2   | V             |
| $V_{(TMR\_LOW)}$                                        | Voltage at TMR pin for auto-retry counter falling threshold |                                                                                                                   | 0.1   | 0.2   | 0.3   | V             |
| $N_{(A\_R\_Count)}$                                     | Number of auto-retry cycles                                 |                                                                                                                   |       | 32    |       |               |
| <b>CHARGE PUMP</b>                                      |                                                             |                                                                                                                   |       |       |       |               |
| $I_{(CAP)}$                                             | Charge pump source current                                  | $V_{(CAP)} - V_{(A)} = 7\text{ V}$ , $6\text{ V} \leq V_{(S)} \leq 65\text{ V}$                                   | 1.3   | 2.7   |       | mA            |
| VCAP – VS                                               | Charge pump turn-on voltage                                 |                                                                                                                   | 11    | 12.2  | 13.2  | V             |
|                                                         | Charge pump turn-off voltage                                |                                                                                                                   | 11.9  | 13.2  | 14.1  | V             |

## 6.5 Electrical Characteristics (continued)

$T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ; typical values at  $T_J = 25^{\circ}\text{C}$ ,  $V_{(A)} = V_{(OUT)} = V_{(VS)} = 12\text{ V}$ ,  $V_{(AC)} = 20\text{ mV}$ ,  $C_{(VCAP)} = 0.1\text{ }\mu\text{F}$ ,  $V_{(EN/UVLO)} = 2\text{ V}$ , over operating free-air temperature range (unless otherwise noted)

| PARAMETER                   |                                                               | TEST CONDITIONS                                                             | MIN | TYP   | MAX  | UNIT          |
|-----------------------------|---------------------------------------------------------------|-----------------------------------------------------------------------------|-----|-------|------|---------------|
| $V_{(CAP\text{ UVLO})}$     | Charge pump UVLO voltage threshold, rising                    |                                                                             | 5.4 | 6.6   | 7.9  | V             |
|                             | Charge pump UVLO voltage threshold, falling                   |                                                                             | 4.4 | 5.5   | 6.6  | V             |
| <b>IDEAL DIODE</b>          |                                                               |                                                                             |     |       |      |               |
| $V_{(A\_PORR)}$             | $V_{(A)}$ POR threshold, rising                               |                                                                             | 2.2 | 2.45  | 2.7  | V             |
| $V_{(A\_PORF)}$             | $V_{(A)}$ POR threshold, falling                              |                                                                             | 2   | 2.25  | 2.45 | V             |
| $V_{(AC\_REG)}$             | Regulated forward $V_{(A)}-V_{(C)}$ threshold                 |                                                                             | 3.6 | 10.4  | 13.7 | mV            |
| $V_{(AC\_REV)}$             | $V_{(A)}-V_{(C)}$ threshold for fast reverse current blocking |                                                                             | -16 | -10.5 | -5   | mV            |
| $V_{(AC\_FWD)}$             | $V_{(A)}-V_{(C)}$ threshold for reverse to forward transition |                                                                             | 150 | 177   | 200  | mV            |
| $V_{(DGATE)} - V_{(A)}$     | Gate drive voltage                                            | $4\text{ V} < V_{(S)} < 5\text{ V}$                                         | 7   |       |      | V             |
|                             |                                                               | $5\text{ V} < V_{(S)} < 65\text{ V}$                                        | 9.2 | 11.5  | 14   | V             |
| $I_{(DGATE)}$               | Peak gate source current                                      | $V_{(A)} - V_{(C)} = 300\text{ mV}$ , $V_{(DGATE)} - V_{(A)} = 1\text{ V}$  |     | 18.5  |      | mA            |
|                             | Peak gate sink current                                        | $V_{(A)} - V_{(C)} = -12\text{ mV}$ , $V_{(DGATE)} - V_{(A)} = 11\text{ V}$ |     | 2670  |      | mA            |
|                             | Regulation sink current                                       | $V_{(A)} - V_{(C)} = 0\text{ V}$ , $V_{(DGATE)} - V_{(A)} = 11\text{ V}$    | 5   | 13.5  |      | $\mu\text{A}$ |
| $I_{(C)}$                   | Cathode leakage Current                                       | $V_{(A)} = -14\text{ V}$ , $V_{(C)} = 12\text{ V}$                          |     | 9.3   | 32   | $\mu\text{A}$ |
| <b>HIGH SIDE CONTROLLER</b> |                                                               |                                                                             |     |       |      |               |
| $V_{(HGATE)} - V_{(OUT)}$   | Gate drive voltage                                            | $4\text{ V} < V_{(S)} < 5\text{ V}$                                         | 7   |       |      | V             |
|                             |                                                               | $5\text{ V} < V_{(S)} < 65\text{ V}$                                        | 10  | 11.1  | 14.5 | V             |
| $I_{(HGATE)}$               | Source current                                                |                                                                             | 39  | 55    | 75   | $\mu\text{A}$ |
|                             | Sink current                                                  |                                                                             | 128 | 180   |      | mA            |

## 6.6 Switching Characteristics

$T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ; typical values at  $T_J = 25^{\circ}\text{C}$ ,  $V_{(A)} = V_{(C)} = V_{(OUT)} = V_{(VS)} = 12\text{ V}$ ,  $V_{(AC)} = 20\text{ mV}$ ,  $C_{(VCAP)} = 0.1\text{ }\mu\text{F}$ ,  $V_{(EN/UVLO)} = 2\text{ V}$ , over operating free-air temperature range (unless otherwise noted)

| PARAMETER                   |                                                       | TEST CONDITIONS                                                                                                          | MIN | TYP | MAX  | UNIT          |
|-----------------------------|-------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------|-----|-----|------|---------------|
| $t_{DGATE\_OFF(dly)}$       | DGATE turn-off delay during reverse voltage detection | $V_{(A)} - V_{(C)} = +30\text{ mV}$ to $-100\text{ mV}$ to $V_{(DGATE-A)} < 1\text{ V}$ , $C_{(DGATE-A)} = 10\text{ nF}$ |     | 0.5 | 0.95 | $\mu\text{s}$ |
| $t_{DGATE\_ON(dly)}$        | DGATE turn-on delay during forward voltage detection  | $V_{(A)} - V_{(C)} = -20\text{ mV}$ to $+700\text{ mV}$ to $V_{(DGATE-A)} > 5\text{ V}$ , $C_{(DGATE-A)} = 10\text{ nF}$ |     | 2   | 3.8  | $\mu\text{s}$ |
| $t_{EN(dly\_DGATE)}$        | DGATE turn-on delay during enable                     | $EN \uparrow$ to $V_{(DGATE-A)} > 5\text{ V}$ , $C_{(DGATE-A)} = 10\text{ nF}$                                           |     | 180 | 270  | $\mu\text{s}$ |
| $t_{UVLO\_OFF(deg\_HGATE)}$ | HGATE turn-off de-glitch during UVLO                  | UVLO $\downarrow$ to HGATE $\downarrow$                                                                                  |     | 5   | 7    | $\mu\text{s}$ |
| $t_{UVLO\_ON(deg\_HGATE)}$  | HGATE turn-on de-glitch during UVLO                   | UVLO $\uparrow$ to HGATE $\uparrow$                                                                                      |     | 8.5 |      | $\mu\text{s}$ |
| $t_{OVP\_OFF(deg\_HGATE)}$  | HGATE turn-off de-glitch during OV                    | OV $\uparrow$ to HGATE $\downarrow$                                                                                      |     | 4   | 7    | $\mu\text{s}$ |
| $t_{OVP\_ON(deg\_HGATE)}$   | HGATE turn-on de-glitch during OV                     | OV $\downarrow$ to HGATE $\uparrow$                                                                                      |     | 9   |      | $\mu\text{s}$ |
| $t_{SCP\_DLY}$              | Short circuit protection turn-off delay               | $(V_{ISCP} - V_{CS-}) = 0\text{ mV}$ to $100\text{ mV}$ HGATE $\downarrow$ , $C_{GS} = 4.7\text{ nF}$                    |     | 3.5 | 5.5  | $\mu\text{s}$ |

## 6.6 Switching Characteristics (continued)

$T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ; typical values at  $T_J = 25^{\circ}\text{C}$ ,  $V_{(A)} = V_{(C)} = V_{(OUT)} = V_{(VS)} = 12\text{V}$ ,  $V_{(AC)} = 20\text{ mV}$ ,  $C_{(VCAP)} = 0.1\text{ }\mu\text{F}$ ,  $V_{(EN/UVLO)} = 2\text{ V}$ , over operating free-air temperature range (unless otherwise noted)

| PARAMETER                |                                                          | TEST CONDITIONS                                                             | MIN | TYP | MAX | UNIT          |
|--------------------------|----------------------------------------------------------|-----------------------------------------------------------------------------|-----|-----|-----|---------------|
| $t_{SCP\_DLY\_START}$    | Short circuit protection turn-off delay at start-up      | $V_{(VS)} = 12\text{ V}$ , $V_{(CS-)} = 0\text{ V}$                         |     | 4   | 4.6 | $\mu\text{s}$ |
| $t_{OCP\_TMR\_DLY}$      | Overcurrent protection turn-off delay                    | $(V_{CS+} - V_{CS-})\uparrow$ HGATE $\downarrow$ , $C_{TMR} = 50\text{ pF}$ |     | 35  |     | $\mu\text{s}$ |
| $t_{OCP\_TMR\_DLY}$      | Overcurrent protection turn-off delay                    | $(V_{CS+} - V_{CS-})\uparrow$ HGATE $\downarrow$ , $C_{TMR} = 10\text{ nF}$ |     | 190 |     | $\mu\text{s}$ |
| $t_{AUTO\_RETRY\_DLY}$   | Over current / Short circuit protection auto retry delay | $(V_{CS+} - V_{CS-})\uparrow$ HGATE $\uparrow$ , $C_{TMR} = 50\text{ pF}$   |     | 1.5 |     | ms            |
| $t_{AUTO\_RETRY\_DLY}$   | Overvoltage clamp timer delay                            | $(V_{CS+} - V_{CS-})\uparrow$ HGATE $\uparrow$ , $C_{TMR} = 10\text{ nF}$   |     | 230 |     | ms            |
| $t_{FLT\_ASSERT}$        | Fault assert delay                                       | $(V_{CS+} - V_{CS-})\uparrow$ FLT $\downarrow$ , $C_{TMR} = 50\text{ pF}$   |     | 35  |     | $\mu\text{s}$ |
| $t_{FLT\_ASSERT\_UV/OV}$ | Fault assert delay during UVLO or OV                     |                                                                             |     | 3   |     | $\mu\text{s}$ |
| $t_{FLT\_DE-ASSERT}$     | Fault de-assert delay                                    |                                                                             |     | 4   |     | $\mu\text{s}$ |
| $t_{MODE\_ENTRY}$        | No RCB mode entry delay                                  |                                                                             |     | 5   |     | $\mu\text{s}$ |
| $t_{MODE\_ENTRY}$        | No RCB to RCB mode entry delay                           |                                                                             |     | 6   |     | $\mu\text{s}$ |

## 6.7 Typical Characteristics

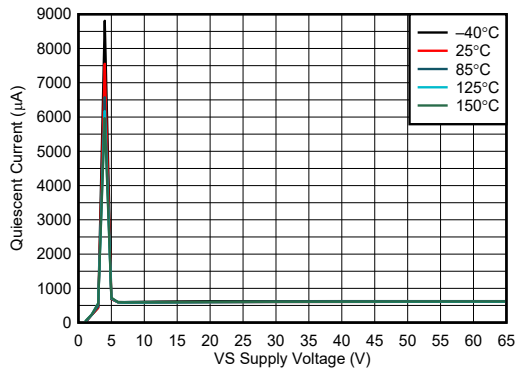


Figure 6-1. Operating Quiescent Current vs Supply Voltage

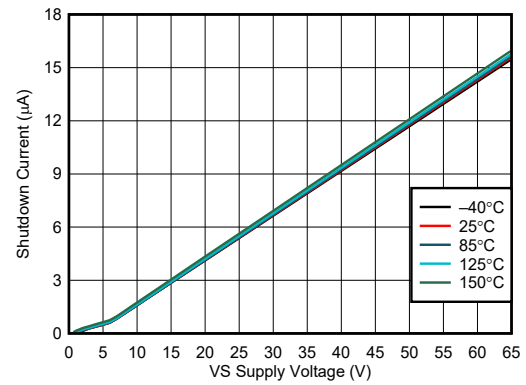


Figure 6-2. Shutdown Current vs Supply Voltage

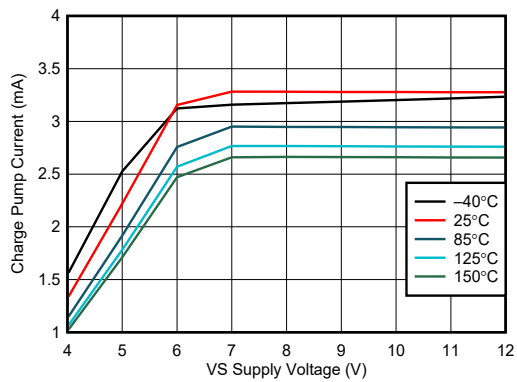


Figure 6-3. Charge Pump Current vs Supply Voltage at CAP – VS ≥ 6 V

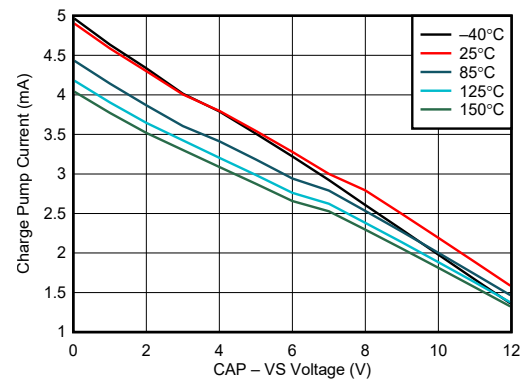


Figure 6-4. Charge Pump V-I Characteristics at VS ≥ 12 V

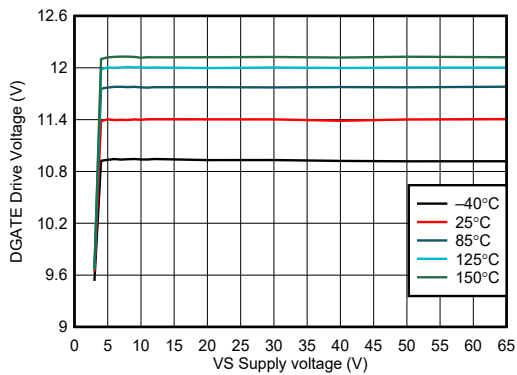


Figure 6-5. DGATE Drive Voltage vs Supply Voltage

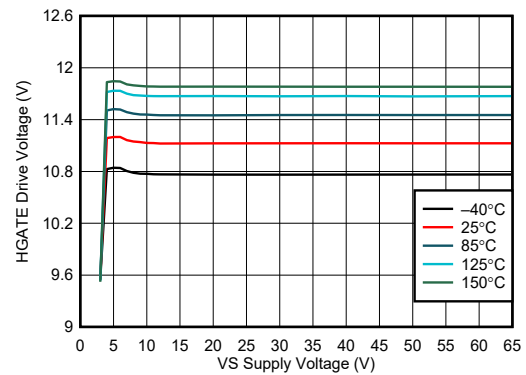
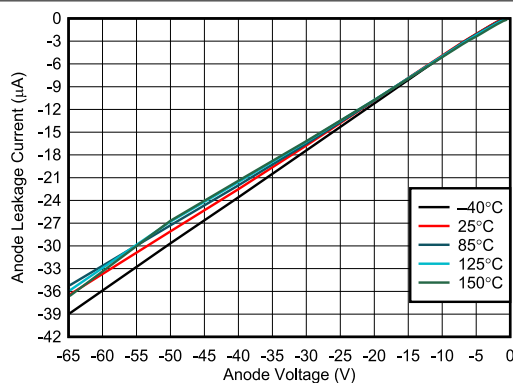
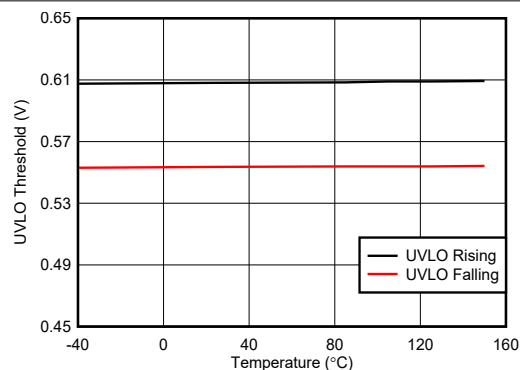


Figure 6-6. HGATE Drive Voltage vs Supply Voltage

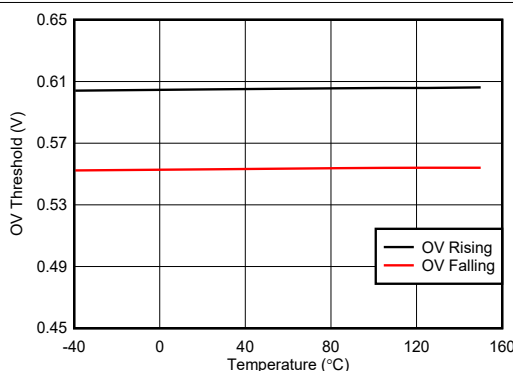
## 6.7 Typical Characteristics (continued)



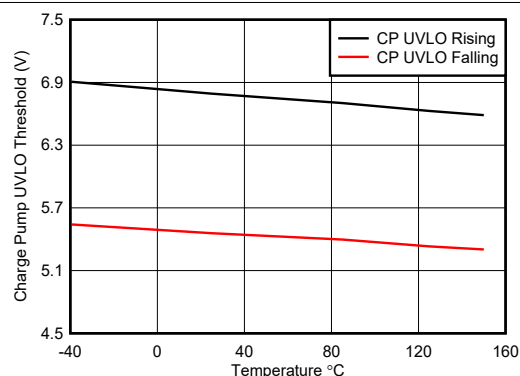
**Figure 6-7. ANODE Leakage Current vs Reverse ANODE Voltage**



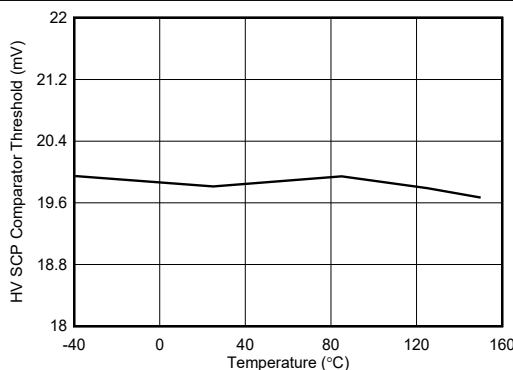
**Figure 6-8. UVLO Threshold vs Temperature**



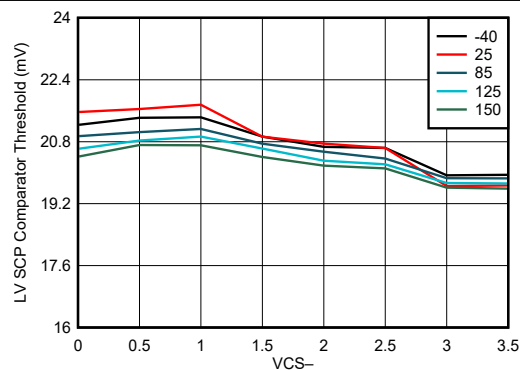
**Figure 6-9. OV Threshold vs Temperature**



**Figure 6-10. Charge Pump UVLO Threshold vs Temperature**



**Figure 6-11. ISCP to CS- Threshold vs Temperature (HV SCP Comparator)**



**Figure 6-12. ISCP to CS- Threshold vs Temperature (LV SCP Comparator)**

## 6.7 Typical Characteristics (continued)

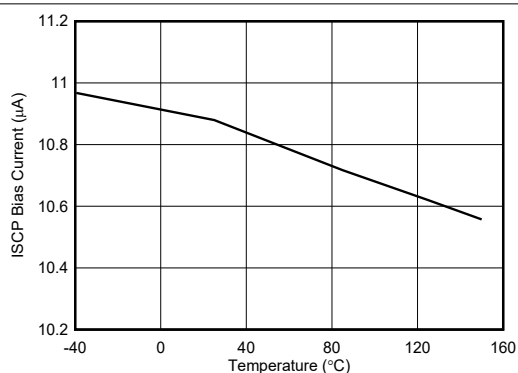


Figure 6-13. ISCP Bias Current vs Temperature

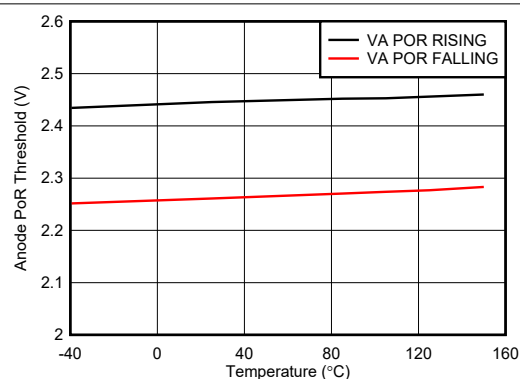


Figure 6-14. VA POR Threshold vs Temperature

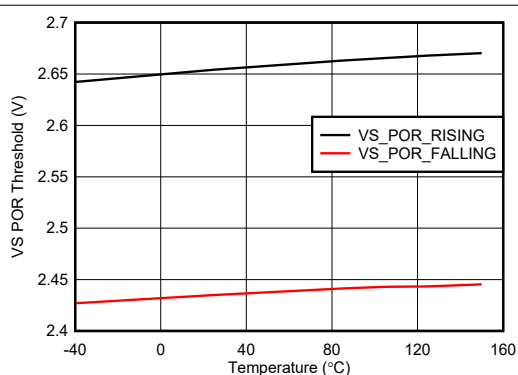


Figure 6-15. VS POR Threshold vs Temperature

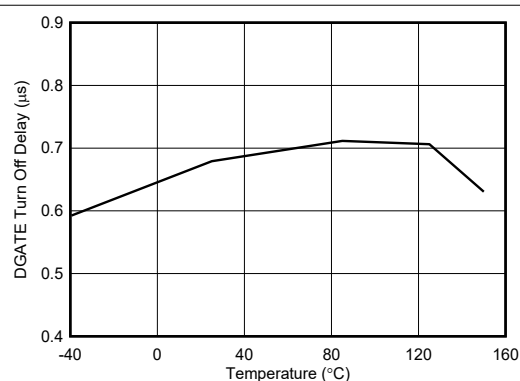


Figure 6-16. DGATE Turn OFF Delay

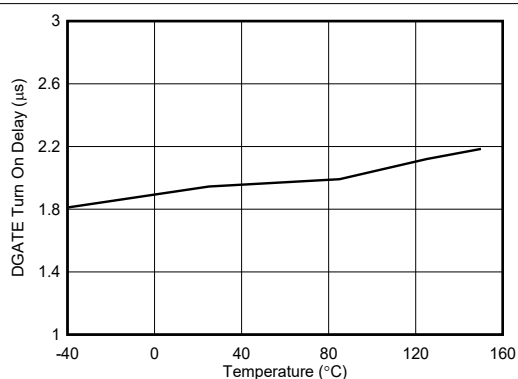


Figure 6-17. DGATE Turn-On Delay During Forward Conduction

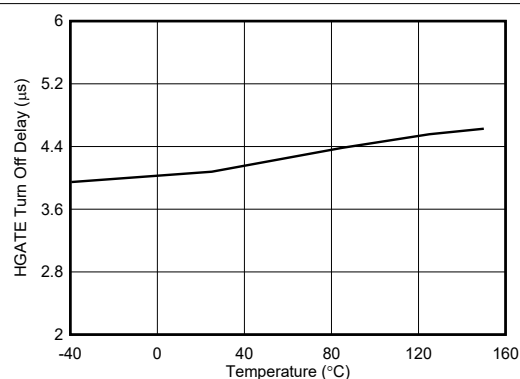
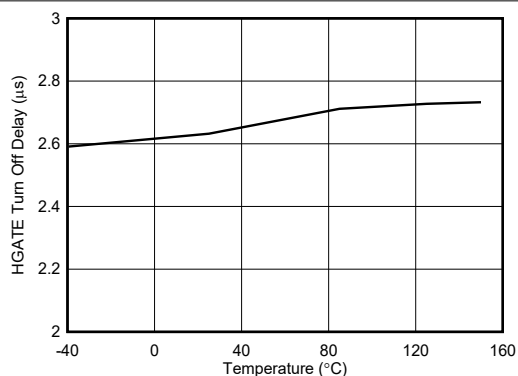
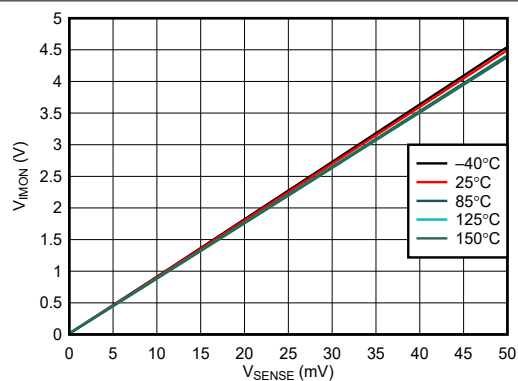


Figure 6-18. HGATE Turn-OFF Delay During Input Overvoltage Condition

## 6.7 Typical Characteristics (continued)



**Figure 6-19. HGATE Turn-OFF Delay During Output Short Circuit Condition**



**Figure 6-20. Current Monitor Output vs Sense Voltage ( $R_{MON} = 5\text{ k}\Omega$ ,  $R_{SET} = 50\text{ }\Omega$ )**

## 7 Detailed Description

## 7.1 Overview

The LM74930-Q1 is an ideal diode controller with surge stopper functionality. The device can drive back-to-back external N-Channel MOSFETs connected in common source topology to realize low loss power path protection with short circuit, overcurrent with circuit breaker, overvoltage and undervoltage protection.

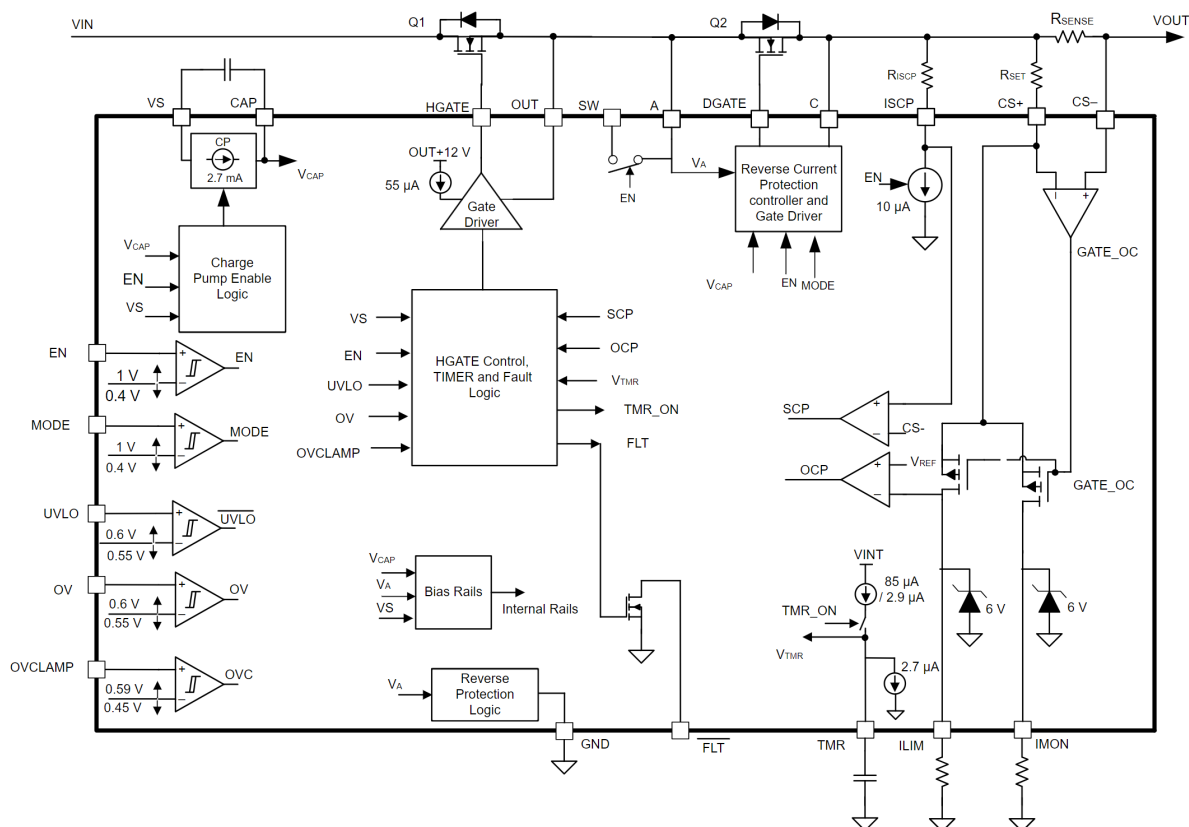
The wide input supply of 4 V to 65 V allows protection and control of 12-V and 24-V automotive battery powered ECUs. The device can withstand and protect the loads from negative supply voltages down to -65 V. With the first MOSFET in the power path the device allows load disconnect (ON and OFF control) using HGATE control. An integrated ideal diode controller (DGATE) drives a second MOSFET to replace a Schottky diode for reverse input protection and output voltage holdup. The device features an adjustable overvoltage protection feature. The LM74930-Q1 has a maximum input voltage rating of 65 V.

The device has integrated short-circuit and overcurrent protection with complete adjustability of thresholds and response time. The device offers adjustable overvoltage and undervoltage protection, providing robust load disconnect in case of voltage transient events. The fault pin  $\overline{\text{FLT}}$  is pulled low in case overcurrent, short circuit, overvoltage or undervoltage fault condition is triggered.

LM74930-Q1 incorporates MODE pin to selectively enable or disable reverse current blocking functionality of ideal diode FET (Q2).

LM74930-Q1 features enable functionality. With the enable (EN) pin pulled low, the device enters into ultra low power mode by completely cutting off loads with typical current consumption of 2.5  $\mu$ A.

## 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Charge Pump

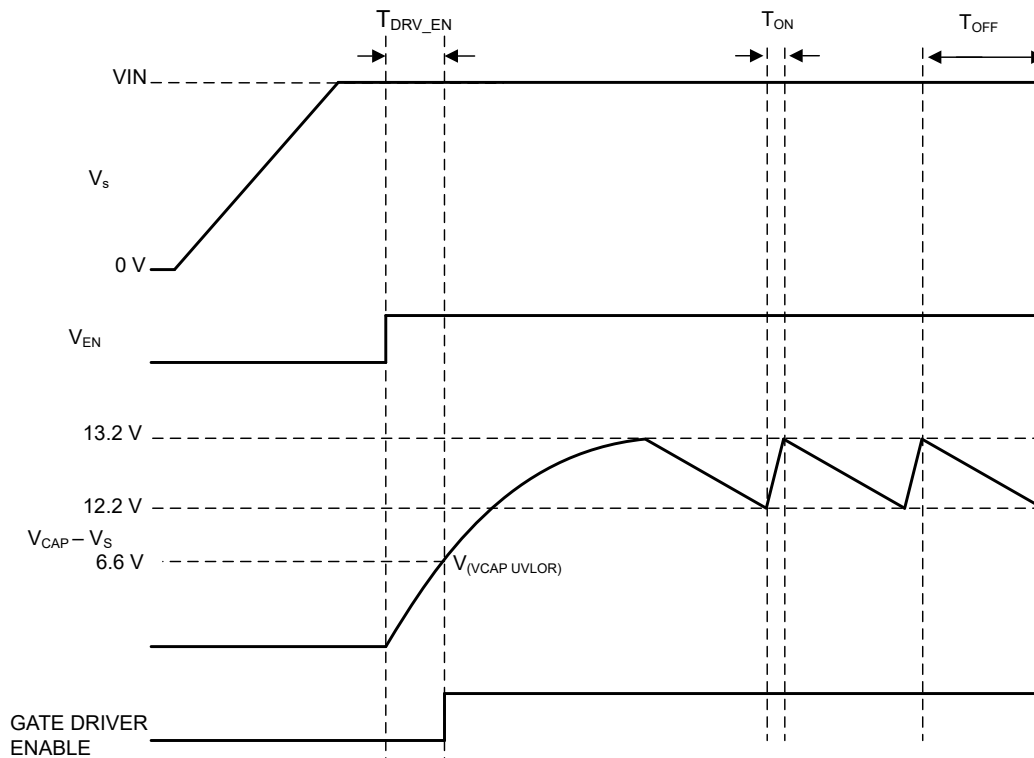
The charge pump supplies the voltage necessary to drive the external N-channel MOSFET. An external charge pump capacitor is placed between CAP and VS pins to provide energy to turn on the external MOSFET. In order for the charge pump to supply current to the external capacitor, the EN pin voltage must be above the specified input high threshold. When enabled the charge pump sources a charging current of 2.7-mA typical. If EN pin is pulled low, then the charge pump remains disabled. To ensure that the external MOSFET can be driven above its specified threshold voltage, the CAP to VS voltage must be above the undervoltage lockout threshold, typically 6.6 V, before the internal gate driver is enabled. Use [Equation 1](#) to calculate the initial gate driver enable delay.

$$T_{DRV\_EN} = 175\mu s + C_{VCAP} \times \frac{V_{VCAP\_UVLOR}}{2.7\text{ mA}} \quad (1)$$

where

- $C_{(CAP)}$  is the charge pump capacitance connected across VS and CAP pins
- $V_{(CAP\_UVLOR)} = 6.6\text{ V}$  (typical)

To remove any chatter on the gate drive approximately 1 V of hysteresis is added to the VCAP undervoltage lockout. The charge pump remains enabled until the CAP to VS voltage reaches 13.2 V, typically, at which point the charge pump is disabled decreasing the current draw on the VS pin. The charge pump remains disabled until the CAP to VS voltage is below to 12.2 V typically at which point the charge pump is enabled. The voltage between CAP and VS continue to charge and discharge between 12.2 V and 13.2 V as shown in [Figure 7-1](#). By enabling and disabling the charge pump, the operating quiescent current of the LM74930-Q1 is reduced. When the charge pump is disabled it sinks 15  $\mu$ A.



**Figure 7-1. Charge Pump Operation**

### 7.3.2 Dual Gate Control (DGATE, HGATE)

The LM74930-Q1 feature two separate gate control and driver outputs i.e DGATE and HGATE to drive back to back N-channel MOSFETs in common source configuration.

#### 7.3.2.1 Load Disconnect Switch Control (HGATE, OUT)

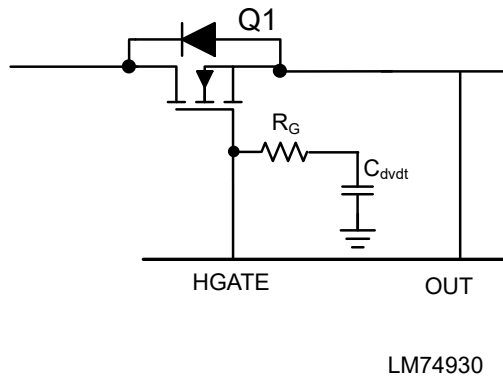
HGATE and OUT comprises of Load disconnect switch control stage. Connect the Source of the external MOSFET to OUT and Gate to HGATE.

Before the HGATE driver is enabled, following conditions must be achieved:

- The EN pin voltage must be greater than the specified input high voltage.
- The CAP to VS voltage must be greater than the undervoltage lockout voltage.
- Voltage at VS pin must be greater than VS POR Rising threshold.
- OV pin voltage must be lower than  $V_{OVR}$  threshold and UVLO pin voltage must be higher than  $V_{UVLOR}$  threshold.

If the above conditions are not achieved, then the HGATE pin is internally connected to the OUT pin, assuring that the external MOSFET is disabled.

For Inrush Current limiting, connect  $C_{dVdT}$  capacitor and  $R_G$  as shown in Figure 7-2.



**Figure 7-2. Inrush Current Limiting**

The  $C_{dVdT}$  capacitor is required for slowing down the HGATE voltage ramp during power up for inrush current limiting. Use Equation 2 to calculate  $C_{dVdT}$  capacitance value .

$$C_{dVdT} = C_{OUT} \times \frac{I_{HGATE\_DRV}}{I_{INRUSH}} \quad (2)$$

where  $I_{HATE\_DRV}$  is 55  $\mu A$  (typ),  $I_{INRUSH}$  is the inrush current and  $C_{OUT}$  is the output load capacitance. An extra resistor  $R_G$  in series with the  $C_{dVdT}$  capacitor improves the turn off time.

#### 7.3.2.2 Reverse Battery Protection (A, C, DGATE)

A, C, DGATE comprises of Ideal Diode stage. Connect the Source of the external MOSFET to A, Drain to C and Gate to DGATE. The LM74930-Q1 has integrated input reverse polarity protection down to -65 V.

Before the DGATE driver is enabled, following conditions must be achieved:

- The EN pin voltage must be greater than the specified input high voltage.
- The CAP to VS voltage must be greater than the undervoltage lockout voltage.
- Voltage at A pin must be greater than VA POR Rising threshold.
- Voltage at VS pin must be greater than VS POR Rising threshold.

If the above conditions are not achieved, then the DGATE pin is internally connected to the A pin, assuring that the external MOSFET is disabled.

In LM74930-Q1 the voltage drop across the MOSFET is continuously monitored between the A and C pins, and the DGATE to A voltage is adjusted as needed to regulate the forward voltage drop at 10.5 mV (typ). This closed loop regulation scheme enables graceful turn off of the MOSFET during a reverse current event and ensures zero DC reverse current flow. This scheme ensures robust performance during slow input voltage ramp down tests. Along with the linear regulation amplifier scheme, the LM74930-Q1 also integrates a fast reverse voltage comparator. When the voltage drop across A and C reaches  $V_{(AC\_REV)}$  threshold then the DGATE goes low within 0.5- $\mu$ s (typ). This fast reverse voltage comparator scheme ensures robust performance during fast input voltage ramp down tests such as input micro-shorts. The external MOSFET is turned ON back when the voltage across A and C hits  $V_{(AC\_FWD)}$  threshold within 2.8  $\mu$ s (typ).

### 7.3.3 Overcurrent Protection (CS+, CS-, ILIM, IMON, TMR)

LM74930-Q1 has two level overcurrent protection. The device senses the voltage across the external current sense resistor through CS+ and CS-.

### 7.3.4 Overcurrent Protection with Circuit Breaker (ILIM, TMR)

LM74930-Q1 provides programmable overcurrent threshold setting by means of resistor ( $R_{LIM}$ ) connected from  $I_{LIM}$  pin to GND.

$$R_{LIM} = \frac{12 \times R_{SET}}{I_{LIM} \times R_{SENSE}} \quad (3)$$

where

- $R_{SET}$  is the resistor connected across CS+ and VS
- $R_{SNS}$  is the current sense resistor
- $I_{LIM}$  is the overcurrent level

The  $C_{TMR}$  programs the circuit breaker and auto-retry time. After the voltage across CS+ and CS- exceeds the set point, the  $C_{TMR}$  starts charging with 85- $\mu$ A pull up current. After the  $C_{TMR}$  charges to  $V_{TMR\_FLT}$ ,  $\overline{FLT}$  asserts low providing warning on impending FET turn OFF. After  $C_{TMR}$  charges to  $V_{TMR\_OC}$ , HGATE is pulled to OUT turning off the load disconnect FET. After this event, the auto-retry behavior starts. The  $C_{TMR}$  capacitor starts discharging with 2.7- $\mu$ A pull down current. After the voltage reaches  $V_{TMR\_Low}$  level, the capacitor starts charging with 2.7- $\mu$ A pull up. After 32 charging/discharging cycles of  $C_{TMR}$ , the FET turns ON and  $\overline{FLT}$  de-asserts after de-assertion delay.

$$T_{OC} = 1.2 \times \frac{C_{TMR}}{82.3 \mu A} \quad (4)$$

where

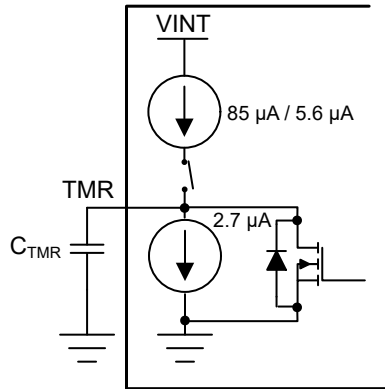
- $T_{OC}$  is the delay to turn OFF the FET
- $C_{TMR}$  is the capacitance across TMR to GND

The auto-retry time can be computed as

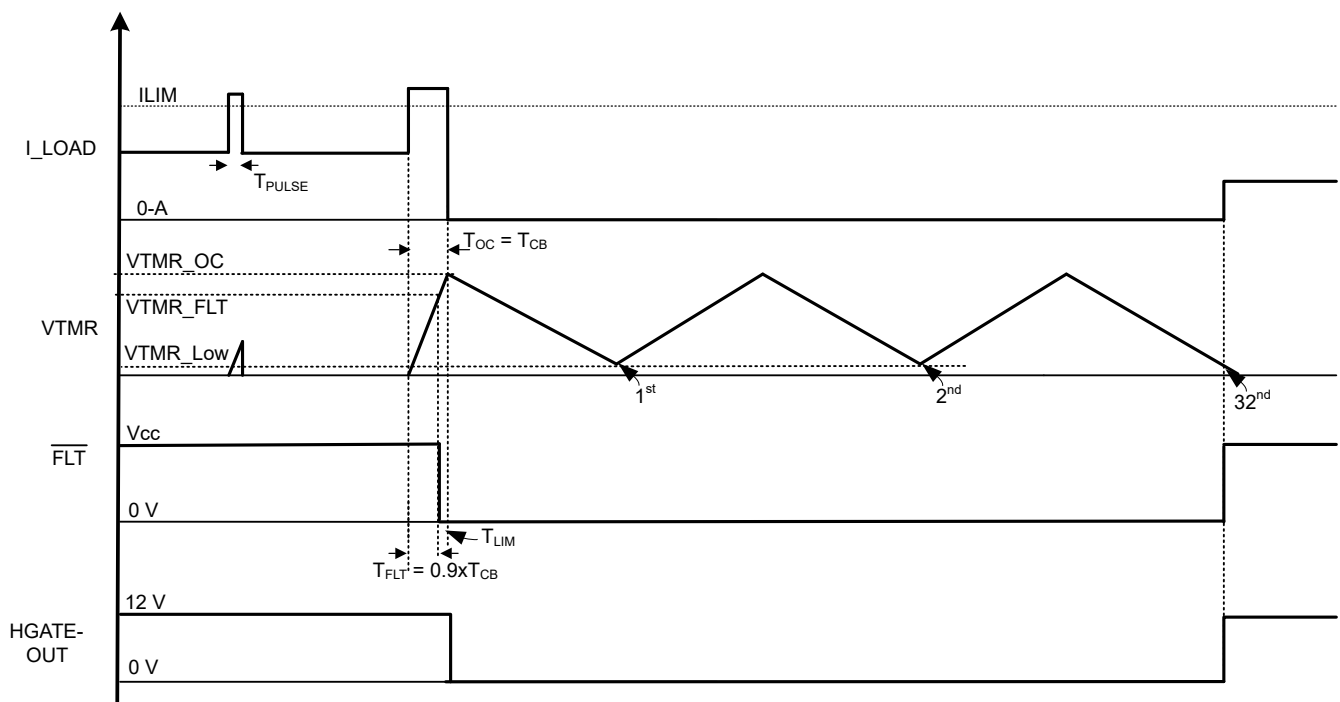
$$T_{RETRY} = 22.7 \times 10^6 \times C_{TMR} \quad (5)$$

If the overcurrent pulse duration is below  $T_{OC}$  then the FET remains ON and  $C_{TMR}$  gets discharged using internal pull down switch.

When not used, ILIM is connected to ground while TMR can be left floating.



### Figure 7-3. LM74930-Q1 Auto Retry TIMER Functionality

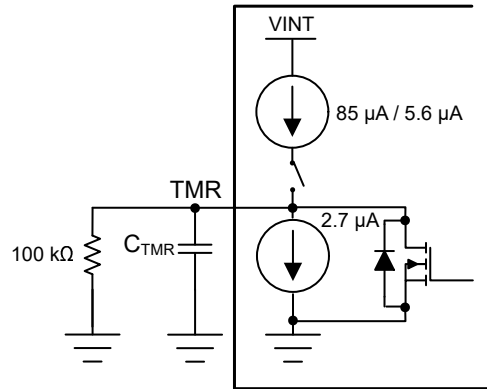


### Figure 7-4. Overcurrent Protection With Auto Retry Timing Diagram

If the overcurrent pulse duration is below  $T_{OC}$  then the FET remains ON and  $C_{TMR}$  gets discharged using internal pull down switch.

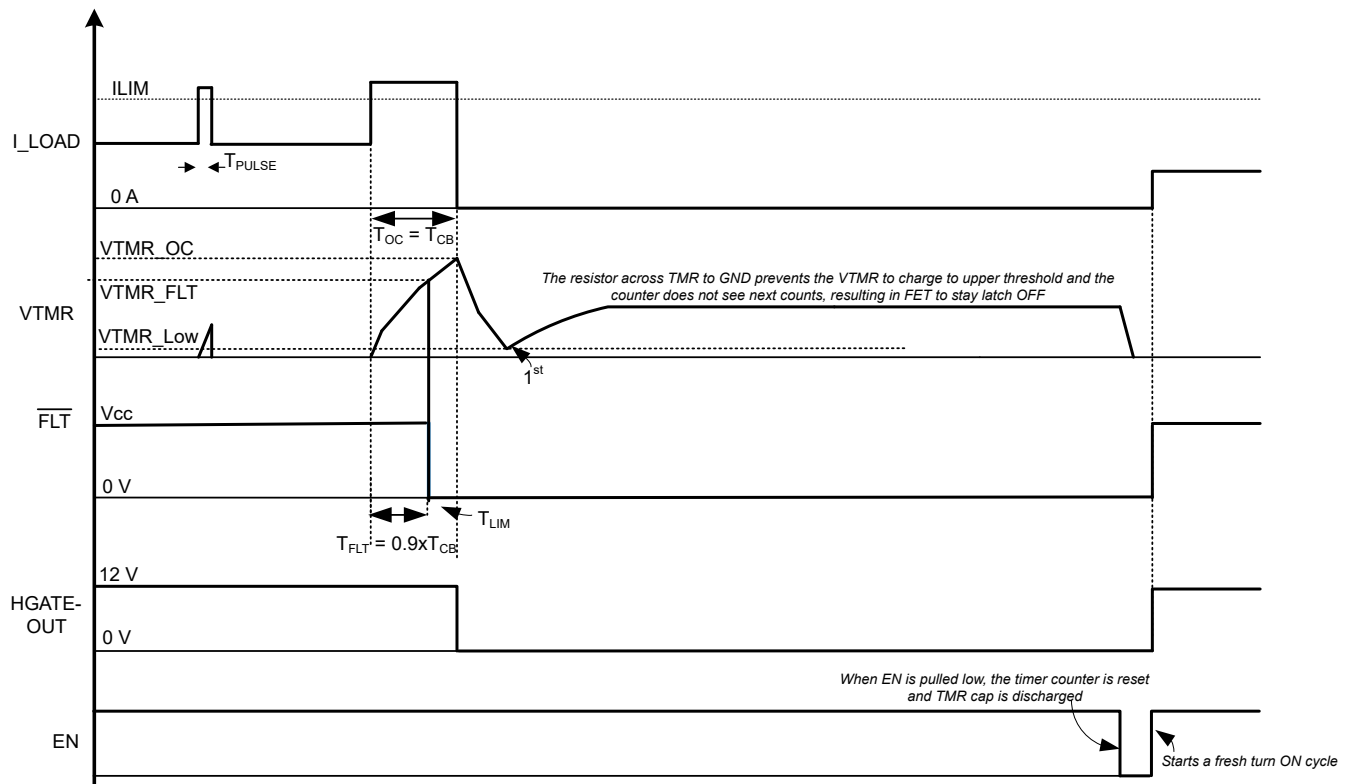
### 7.3.5 Overcurrent Protection With Latch-Off

With about a 100-k $\Omega$  resistor across C<sub>TMR</sub> as shown in figure, overcurrent latch-off functionality can be achieved. With this resistor, during the charging cycle the voltage across C<sub>TMR</sub> gets clamped to a level below V<sub>TMR\_OC</sub> resulting in a latch-off behavior.



**Figure 7-5. LM74930-Q1 Overcurrent Protection With Latch Off**

Toggle EN (below  $V_{ENF}$ ) or power cycle VS below  $V_{SPORF}$  to reset the latch. At low edge, the timer counter is reset and  $C_{TMR}$  is discharged.



**Figure 7-6. Overcurrent Protection With Latch Timing Diagram**

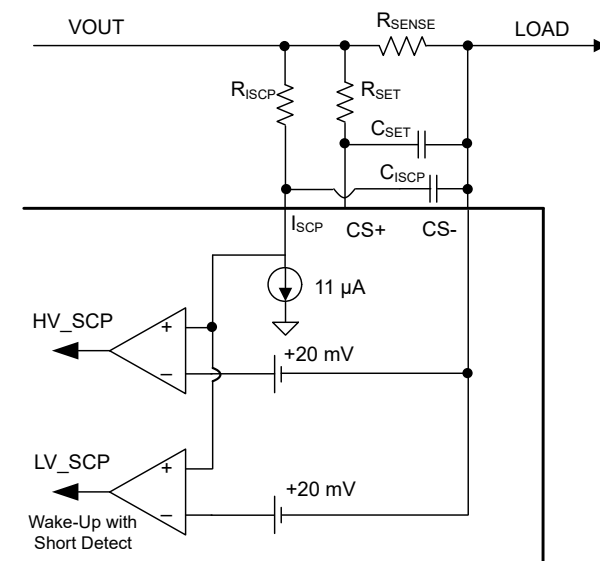
### 7.3.6 Short-Circuit Protection (ISCP)

LM74930-Q1 offers fast response to output short circuit events with the short-circuit protection feature. After the voltage across ISCP and CS– exceeds the default threshold of 20-mV typical, HGATE is pulled to OUT within 3-μs protecting the load disconnect FET. FLT asserts low at the same time. Subsequent to this event, the charge/discharge cycles of  $C_{TMR}$  starts similar to the behavior post FET OFF event in circuit breaker operation.

Short circuit protection threshold can be increased using an external series resistor ( $R_{ISCP}$ ) from ISCP pin to current sense resistor. The shift in the short circuit protection threshold can be calculated using [Equation 6](#).

$$V_{SNS\_SCP} = 20\text{mV} + (R_{ISCP} \times 11 \mu\text{A}) \quad (6)$$

An additional deglitch filter consisting of  $R_{ISCP}$  and  $C_{ISCP}$  can be added from ISCP pin to CS- pin as shown in Figure 7-7 to avoid any false short circuit trigger in case of fast automotive transients such as Input short interruptions (LV124, E-10), AC superimpose (LV124 E-06, ISO16750-2), ISO7637-2 Pulse 2A.



**Figure 7-7. Short-Circuit Protection With Deglitch Filter**

Short-circuit protection with latch off can also be achieved in the similar way as explained in the circuit breaker section.

#### 7.3.6.1 Device Wake-Up With Output Short-Circuit Condition

LM74930-Q1 uses a low voltage short-circuit comparator (LV\_SCP) to protect the system from output short-circuit condition during device power-up. When device is powering up with output short condition, low voltage comparator (LV\_SCP) compares the voltage drop across external current sense resistor (ISCP and CS- pins) against internal fixed internal threshold of 20 mV. If this voltage drop is more than LV\_SCP comparator short-circuit protection threshold then HGATE drive is disabled.

After the device is powered on, then device uses high voltage short-circuit protection comparator (HV\_SCP) as described in [Section 7.3.6](#).

LM74930-Q1 features analog load current monitor output (IMON) with adjustable gain. LM74930-Q1 starts providing overcurrent protection with circuit breaker functionality and current monitoring information when device is powered up ( $V_S > V_{S_{PORR}}$  and  $V_{CS-} > 3\text{ V}$ ). The resistor connected from IMON pin to ground sets the current monitor output voltage given by [Equation 7](#).

[illegible]

### 7.3.8 Overvoltage and Undervoltage Protection (OV, UVLO, OVCLAMP)

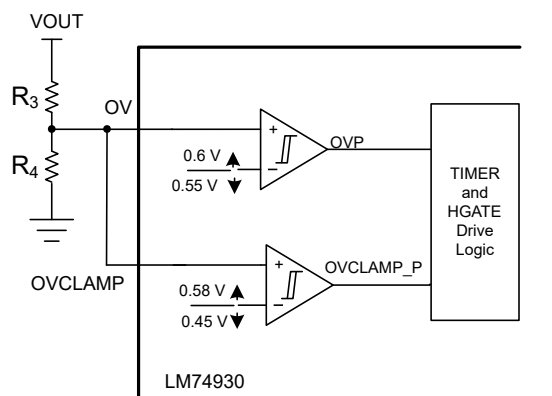
The diagram illustrates the UVLO and OVP protection circuit for the LM74930. The circuit includes a voltage divider (R1, R2) for UVLO, a switch (OV Cut-Off, OV Clamp) for VOUT, and another voltage divider (R3, R4) for OVP. The LM74930 chip is shown with its UVLO and OVP pins connected to the respective nodes. The chip is labeled LM74930.

A disconnect switch is integrated between A and SW pin to monitor common source node voltage as well. This switch is turned OFF when EN pin is pulled low.

LM74930-Q1 also supports overvoltage clamp operation with circuit breaker (Timer) functionality. To enable device operation in overvoltage clamp with circuit breaker functionality, connect OVCLAMP pin to OV pin as shown in [#none#](#). In case of overvoltage event, device clamps output voltage to threshold set by the external resistor divider  $R_3$ ,  $R_4$ . The TMR pin source current during overvoltage clamp with circuit breaker functionality is 5.5- $\mu$ A typical. The circuit breaker time after which load disconnect switch is turned off can be calculated using [Equation 8](#).

$$T_{OVC} = 1.2 \times \frac{C_{TMR}}{2.8 \mu A} \quad (8)$$

The rest of the device functionality in terms of auto-retry and latch off behavior of HGATE drive is same as described in [overcurrent with circuit breaker section](#).



**Figure 7-10. LM74930-Q1 Overvoltage Clamp With Circuit Breaker Functionality**

The falling threshold of OVCLAMP comparator is kept lower than OV comparator to ensure no false timer reset when system is recovering from overvoltage event. As device does hysteretic output on/off control during overvoltage clamp operation it is recommended to keep the minimum output voltage level during overvoltage clamp operation above OVCLAMP falling threshold. [Equation 9](#) shows the minimum output capacitor required to ensure no false timer resets during overvoltage clamp operation for given load current.

$$C_{OUT} > \frac{V_T \times C_{GATE\_EFF} \times I_{LOAD} \times R_4}{I_{HGATE\_DRV} \times (R_3 + R_4) \times (V_{OVF} - V_{OVCLAMPF})} \quad (9)$$

where

- $V_T$  is the MOSFET VGS threshold voltage
- $I_{HGATE\_DRV}$  is HGATE drive strength = 55  $\mu$ A (typical)
- $C_{GATE\_EFF}$  is effective gate capacitance as seen by HGATE pin ( $C_{GS} + C_{dVdT}$ )
- $V_{OVF}$  and  $V_{OVCLAMPF}$  is a falling threshold of OV and OVCLAMP comparators respectively

### 7.3.9 Disabling Reverse Current Blocking Functionality (MODE)

LM74930-Q1 incorporates MODE pin to selectively enable or disable reverse current blocking functionality of ideal diode FET. For applications which requires back-to-back MOSFET driver with input reverse polarity protection however reverse current blocking is not a must have function, reverse current blocking functionality can be disabled by pulling MODE pin to ground. All other protection features related to load disconnect functionality such as undervoltage, overvoltage and overcurrent protection remain unaffected.

When not used MODE pin can be pulled to VS or EN pin of the device.

### 7.3.10 Device Functional Modes

#### 7.3.10.1 Low Quiescent Current Shutdown Mode (EN)

The enable pin allows for the LM74930-Q1 to be either enabled or disabled by an external signal. If the EN pin voltage is greater than the rising threshold, the gate driver and charge pump operates as described in Charge

Pump section. If EN pin voltage is less than the input low threshold,  $V_{(ENF)}$ , the charge pump and both the gate drivers (DGATE and HGATE) are disabled placing the LM74930-Q1 in shutdown mode with ultra-low-current consumption of 2.5- $\mu$ A. The EN pin can withstand a maximum voltage of 65 V. For always ON operation, connect EN pin to VS.

## 8 Applications and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

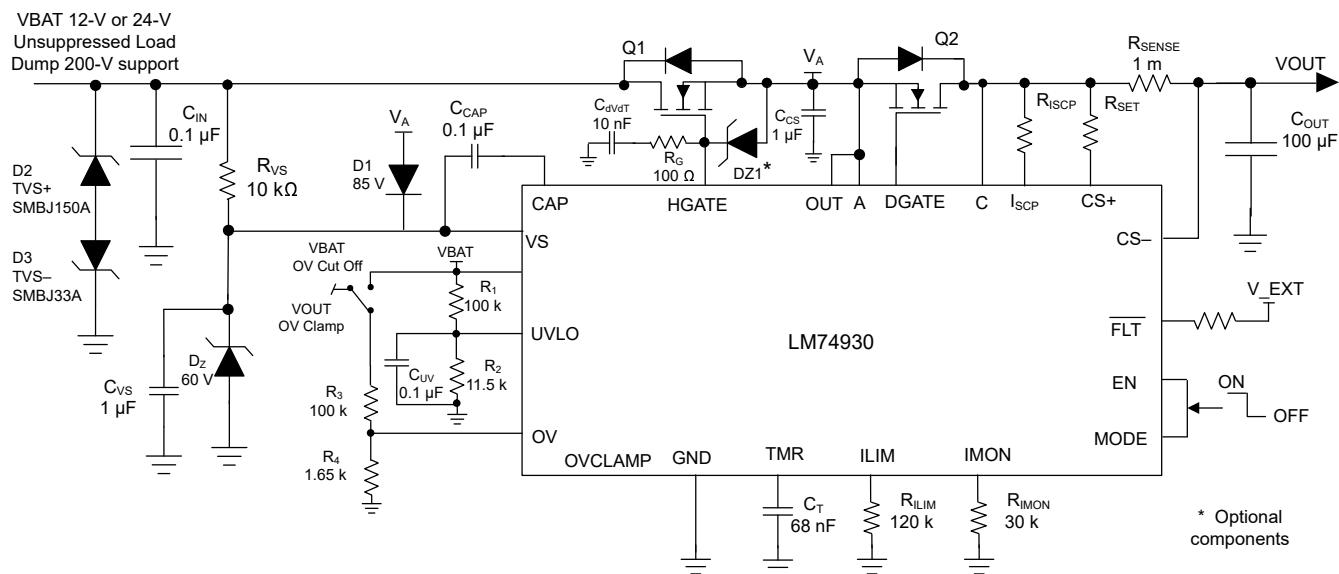
### 8.1 Application Information

LM74930-Q1 controls two N-channel power MOSFETs with DGATE used to control ideal diode MOSFET to emulate an ideal diode and HGATE controlling second MOSFET for power path cut-off when disabled or during system fault conditions such as overcurrent, overvoltage or undervoltage event. HGATE controlled MOSFET can be used to clamp the output during overvoltage or load dump conditions. LM74930-Q1 can be placed into low quiescent current mode using EN, where both DGATE and HGATE are turned OFF.

The device has a separate supply input pin (VS). The charge pump is derived from this supply input. With the separate supply input provision and separate GATE control architecture, the LM74930-Q1 device offers flexibility in system design architectures and enables circuit design with various power path control topologies like common source, ORing and Power MUXing. With these various topologies, the system designers can design the front-end power system to meet various system design requirements.

### 8.2 Typical Application: 200-V Unsuppressed Load Dump Protection Application

Independent gate drive topology of LM74930-Q1 enables to configure the device into unsuppressed load dump or surge protection along with input reverse battery protection. LM74930-Q1 configured in **common-source topology** to provide 200-V unsuppressed load dump protection with reverse battery protection is [Figure 8-1](#).



**Figure 8-1. Typical Application Circuit: 200-V Unsuppressed Load Dump Protection with Reverse Battery Protection**

## 8.2.1 Design Requirements for 200-V Unsuppressed Load Dump Protection

**Table 8-1. Design Parameters - 24-V Unsuppressed Load Dump Protection**

| DESIGN PARAMETER                         | EXAMPLE VALUE                                                               |
|------------------------------------------|-----------------------------------------------------------------------------|
| Operating input voltage range            | 12-V/24-V battery, 200-V unsuppressed load lump                             |
| Output power                             | 45 W                                                                        |
| Output current range                     | 3-A nominal, 5-A peak                                                       |
| Input capacitance                        | 0.1-μF minimum                                                              |
| Output capacitance                       | 0.1-μF minimum, 100-μF typical hold-up capacitance                          |
| Overvoltage cut-off / clamp threshold    | 37.0 V                                                                      |
| Overcurrent limit                        | 5 A                                                                         |
| Short-circuit limit                      | 20 A                                                                        |
| Automotive transient immunity compliance | ISO 7637-2 and ISO 16750-2 including 200-V unsuppressed load dump Pulse 5 A |

## 8.2.2 Detailed Design Procedure

Load dump transients occurs on loads connected to the alternator when a discharged battery is disconnected from alternator while it is still generating charging current. Load dump amplitude and duration depends on alternator speed and field current into the rotor. The pulse shape and parameter are specified in ISO 7637-2 5A where a 200-V pulse lasts maximum 350 ms on 24-V battery system. Circuit topology and MOSFET ratings are important when designing a 200-V unsuppressed load dump protection circuit using LM74930-Q1. Dual gate drive enables LM74930-Q1 to be configured in common source topology in [Figure 8-1](#) where MOSFET Q1 is used to turn off or clamp output voltage to acceptable safe level and protect the MOSFET Q2 and LM74930-Q1 from 200 V. Note that only the VS pin is exposed to 200 V through a 10-kΩ resistor. A 60-V rated Zener diode is used to clamp and protect the VS pin. Rest of the circuit is not exposed to higher voltage as the MOSFET Q1 can either be turned off completely or output voltage clamped to safe level. MOSFET Q1 selection, input TVS selection and MOSFET Q2 selection for ISO 7637-2 and ISO 16750-2 compliance are discussed in this section.

### 8.2.2.1 VS Capacitance, Resistor R<sub>1</sub> and Zener Clamp (D<sub>Z</sub>)

A minimum of 1-μF C<sub>VS</sub> capacitance is required. During input overvoltage transient, resistor R<sub>VS</sub> and Zener diode, D<sub>Z</sub>, are used to protect VS pin from exceeding the maximum ratings by clamping V<sub>VS</sub> to 60 V. Choosing R<sub>VS</sub> = 10 kΩ, the peak power dissipated in Zener diode D<sub>Z</sub> can be calculated using [Equation 10](#).

$$P_{DZ} = V_{DZ} \times \frac{V_{INMAX} - V_{DZ}}{R_{VS}} \quad (10)$$

Where V<sub>DZ</sub> is the breakdown voltage of Zener diode. Select the Zener diode that can handle peak power requirement.

Peak power dissipated in resistor R<sub>1</sub> can be calculated using [Equation 11](#).

$$P_{RVS} = \frac{(V_{INMAX} - V_{DZ})^2}{R_{VS}} \quad (11)$$

Select a resistor package which can handle peak power and maximum DC voltage.

### 8.2.2.2 Charge Pump Capacitance VCAP

Minimum required capacitance for charge pump VCAP is based on input capacitance of the MOSFET Q1, C<sub>ISS(MOSFET\_Q1)</sub> and input capacitance of Q2 C<sub>ISS(MOSFET\_Q2)</sub>.

Charge Pump VCAP: Minimum 0.1 μF is required; recommended value of VCAP (μF) ≥ 10 x ( C<sub>ISS(MOSFET\_Q1)</sub> + C<sub>ISS(MOSFET\_Q2)</sub> ) (μF)

### 8.2.2.3 Input and Output Capacitance

TI recommends a minimum input capacitance  $C_{IN}$  of 0.1  $\mu\text{F}$  and output capacitance  $C_{OUT}$  of 0.1  $\mu\text{F}$ .

### 8.2.2.4 Overvoltage and Undervoltage Protection Component Selection

Resistors  $R_1$ ,  $R_2$  and  $R_3$ ,  $R_4$  connected from SW pin to ground is used to program the undervoltage and overvoltage threshold. The resistor values required for setting the undervoltage threshold ( $V_{UVLO}$  to 5.5 V) and overvoltage threshold ( $V_{OVR}$  to 37.0 V) are calculated by solving

$$V_{UVLOF} = V_{UVSET} \times \frac{R_2}{R_1 + R_2} \quad (12)$$

$$V_{OVR} = V_{OVSET} \times \frac{R_4}{R_3 + R_4} \quad (13)$$

For minimizing the input current drawn from the battery through resistors  $R_1$ ,  $R_2$ , and  $R_3$ ,  $R_4$ , TI recommends to use higher value of resistance. Using high value resistors adds error in the calculations because the current through the resistors at higher value becomes comparable to the leakage current into the OV pin. Maximum leakage current into the UVLO and OV pin is 0.2  $\mu\text{A}$  and choosing total ladder resistor in 100k $\Omega$  range ensures current through resistors is much higher than leakage through the OV pin.

Based on the device electrical characteristics,  $V_{UVLOF}$  is 0.55 V. Select  $R_1 = 100 \text{ k}\Omega$ . Solving Equation 12 gives  $R_2 = 11.5 \text{ k}\Omega$ . Solving Equation 13 with  $R_3$  selected as 100 k $\Omega$  and  $V_{OVR} = 0.6 \text{ V}$  gives  $R_4 = 1.65 \text{ k}\Omega$  as standard 1% resistor values closest to the calculated resistor values.

An optional capacitor  $C_{UV}$  can be placed in parallel with  $R_2$  on UVLO resistor ladder to filter out any fast undervoltage transients on battery lines to avoid false UVLO trigger.

### 8.2.2.5 Selection of Scaling Resistor ( $R_{SET}$ ) and Short-Circuit Protection Setting Resistor ( $R_{SCP}$ )

$R_{SET}$  is the resistor connected between C and CS+ pin. This resistor scales the overcurrent protection threshold voltage and coordinates with  $R_{ILIM}$  and  $R_{IMON}$  to determine the overcurrent protection threshold and current monitoring output. The recommended range of  $R_{SET}$  is 50  $\Omega$  to 100  $\Omega$ .  $R_{SET}$  is selected as 50  $\Omega$ , 1% for this design example.

LM74930-Q1 default short circuit threshold of 20 mV can be shifted to higher value as given by Equation 14.

$$V_{SNS\_SCP} = 20\text{mV} + (R_{ISCP} \times 11 \mu\text{A}) \quad (14)$$

For this application, ISCP pin is shorted directly to C pin (Drain of Q2). User has a flexibility to populate suitable value of  $R_{ISCP}$  resistor to adjust short circuit protection current limit and also gives flexibility in terms of selecting different current sense resistor value.

An additional de-glitch filter (optional) consisting of  $R_{ISCP}$  and  $C_{SCP}$  can be added from ISCP pin to CS– pin as shown in Figure 8-1 to avoid any false short circuit trigger in case of fast automotive transients such as Input Micro cuts (LV124, E-10), AC superimpose (LV124, E-06), ISO7637-2 Pulse 2 A.

### 8.2.2.6 Overcurrent Limit ( $I_{LIM}$ ), Circuit Breaker Timer ( $TMR$ ), and Current Monitoring Output ( $IMON$ ) Selection

#### Programming the Overcurrent Protection Threshold – $R_{ILIM}$ Selection

The  $R_{ILIM}$  sets the overcurrent protection (circuit breaker detection) threshold, whose value can be calculated using Equation 15.

$$R_{ILIM} = \frac{12 \times R_{SET}}{I_{LIM} \times R_{SENSE}} \quad (15)$$

To set 5 A as overcurrent protection threshold,  $R_{ILIM}$  value is calculated to be 120 k $\Omega$ . Choose available standard value: 120 k $\Omega$ , 1%.

### Programming the Circuit Breaker Time – C<sub>TMR</sub> Selection

For the design example under discussion, overcurrent transients are allowed for 1-ms duration. This blanking interval, T<sub>OC</sub> (or circuit breaker interval, T<sub>CB</sub>) can be set by selecting appropriate capacitor C<sub>TMR</sub> from TMR pin to ground. The value of C<sub>TMR</sub> can be calculated using [Equation 16](#).

$$T_{OC} = 1.2 \times \frac{C_{TMR}}{82.3 \mu A} \quad (16)$$

C<sub>TMR</sub> value of 68 nF, 10% is selected to allow circuit breaker duration of close to 1-ms.

### Programming Current Monitoring Output – R<sub>IMON</sub> Selection

Voltage at IMON pin V<sub>IMON</sub> is proportional to the output load current. This can be connected to an ADC of the downstream system for monitoring the operating condition and health of the system. The R<sub>IMON</sub> must be selected based on the maximum load current and the input voltage range of the ADC used. R<sub>IMON</sub> is set using [Equation 17](#).

$$V_{IMON} = \frac{0.9 \times V_{SENSE} \times R_{IMON}}{R_{SET}} \quad (17)$$

For this application example, V<sub>IMON</sub> is selected to be 2.7 V at full load current of 5 A. R<sub>IMON</sub> value of 30.1 kΩ, 1% is selected.

#### 8.2.2.7 Selection of Current Sense Resistor, R<sub>SNS</sub>

LM74930-Q1 has integrated short-circuit detection comparator with default sense threshold of 20 mV. For this application, short-circuit limit is set to 20 A. The sense resistor value based on short circuit comparator can be calculated by [Equation 18](#).

$$R_{SENSE} = \frac{V_{SENSE}}{I_{SCP}} \quad (18)$$

Select a 1-mΩ resistor with 1% tolerance to set short-circuit protection limit of 20 A.

Selecting the lower current sense resistor value helps with lower power dissipation, however it has comparatively smaller drop across current sense resistor at full load. If higher drop across current sense resistor is desired for better current monitoring accuracy, device short-circuit limit can be increased using R<sub>ISCP</sub> resistor. Please refer to device design calculator on LM74930-Q1 product page.

#### 8.2.2.8 Hold-Up Capacitance

Usually bulk capacitors are placed on the output due to various reasons such as uninterrupted operation during power interruption or micro-short at the input, hold-up requirements for doing a memory dump before turning of the module and filtering requirements as well. This design considers minimum bulk capacitors requirements for meeting functional status "A" during LV124 E10 test case 2 100-μs input interruption. To achieve functional pass status A, acceptable voltage droop in the output of LM74930-Q1 is based on the UVLO settings of downstream DC-DC converters. For this design, drop from 12 V to 6.5 V in output voltage for 100 μs is considered (assuming downstream converter with 5-V output) and the minimum hold-up capacitance required is calculated by

$$C_{HOLD\_UP\_MIN} = \frac{I_{LOAD} \times 100 \mu s}{\Delta V_{OUT}} \quad (19)$$

Minimum hold-up capacitance required for 5.5-V drop in 100 μs is 100 μF. Note that the typical application circuit shows the hold-up capacitor as optional because not all designs require hold-up capacitance.

#### 8.2.2.9 MOSFET Q1 Selection

The V<sub>DS</sub> rating of the MOSFET Q1 must be minimum 200 V for a output cut-off design where output can reach 0 V while the load dump transient is present and must be a minimum of 164.5 V when output is clamped to 37 V

( $\pm 1.5$  V). The  $V_{GS}$  rating is based on HGATE-OUT maximum voltage of 15 V. TI recommends a 20-V  $V_{GS}$  rated MOSFET.

Power dissipation on MOSFET Q1 on a design where output is clamped is critical and SOA characteristics of the MOSFET must be considered with sufficient design margin for reliable operation.

#### 8.2.2.10 MOSFET Q2 Selection

For selecting the blocking MOSFET Q1, important electrical parameters are the maximum continuous drain current  $I_D$ , the maximum drain-to-source voltage  $V_{DS(MAX)}$ , the maximum drain-to-source voltage  $V_{GS(MAX)}$ , the maximum source current through body diode and the drain-to-source ON resistance  $R_{DS(ON)}$ .

The maximum continuous drain current,  $I_D$  rating must exceed the maximum continuous load current. The maximum drain-to-source voltage,  $V_{DS(MAX)}$ , must be high enough to withstand the highest differential voltage seen in the application. This can include all the automotive transient events and any anticipated fault conditions. TI recommends to use MOSFETs with VDS voltage rating of 60 V along with a single bidirectional TVS or a VDS rating 40-V maximum rating along with two unidirectional TVS connected back-back at the input.

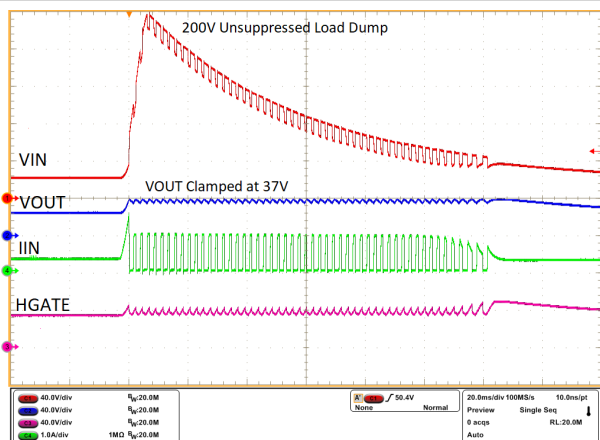
The maximum VGS LM74930-Q1 can drive is 14 V, so a MOSFET with 15-V minimum VGS rating must be selected. If a MOSFET with < 15-V  $V_{GS}$  rating is selected, a Zener diode can be used to clamp VGS to safe level, but this action can result in increased IQ current.

To reduce the MOSFET conduction losses, lowest possible  $R_{DS(ON)}$  is preferred, but selecting a MOSFET based on low  $R_{DS(ON)}$  can not be beneficial always. Higher  $R_{DS(ON)}$  provides increased voltage information to LM74930-Q1 reverse comparator at a lower reverse current. Reverse current detection is better with increased  $R_{DS(ON)}$ . Choosing a MOSFET with < 50-mV forward voltage drop at maximum current is a good starting point.

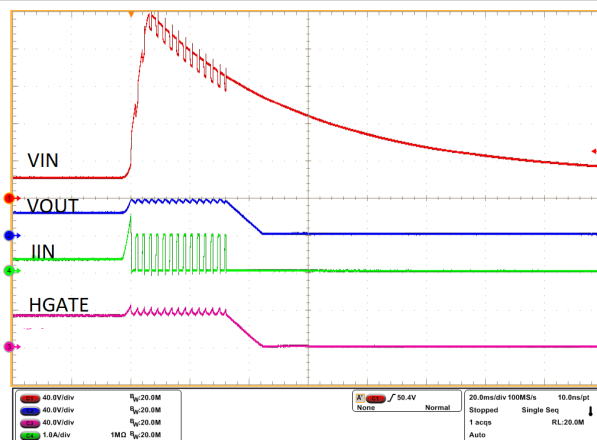
#### 8.2.2.11 Input TVS Selection

Two series connected diodes D2 and D3 are required at the input. For the negative voltage transient clamping, TVS diode D3 is used to clamp ISO 7637-2 pulse 1 and its selection is similar to procedure in [TVS selection for 24-V Battery Systems](#). The diode on the positive side is required to block the current flowing through D3 in case of input reverse polarity. The breakdown voltage of D3 must be higher than the maximum system voltage of 200 V. This diode can be a schottky, standard rectifier diode or TVS diode with breakdown voltage of 200-V..

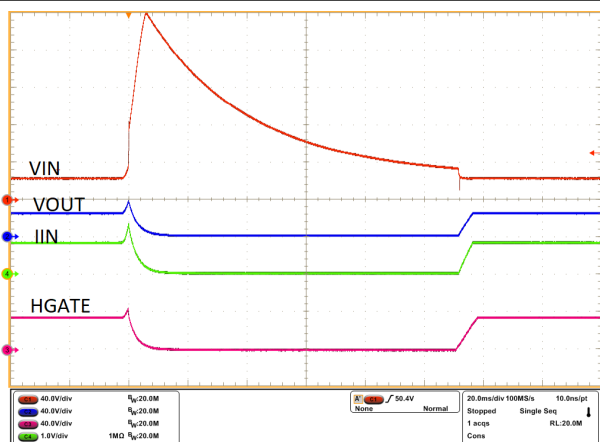
## 8.2.3 Application Curves



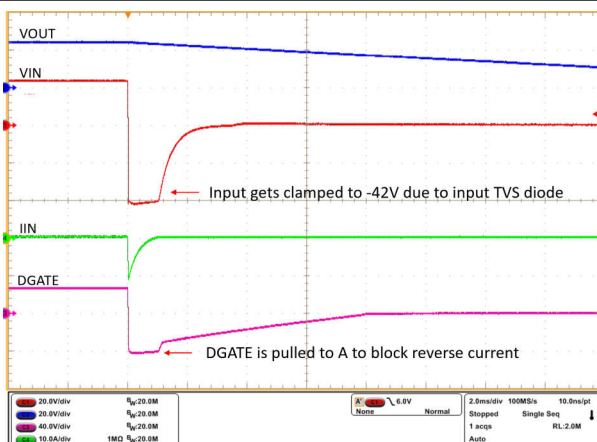
**Figure 8-2. Unsuppressed Load Dump 200 V - Output Clamp (OVCLAMP = GND)**



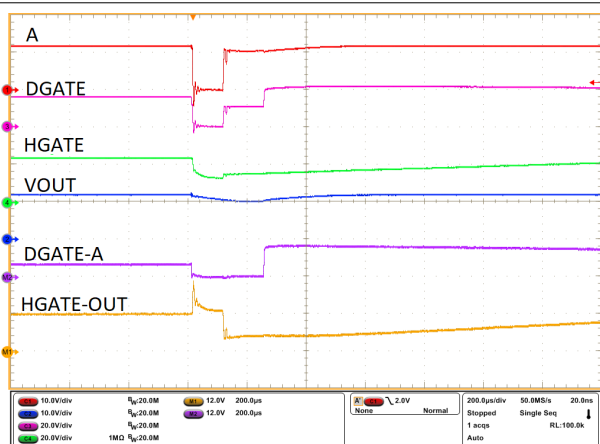
**Figure 8-3. Unsuppressed Load Dump 200 V - Output Clamp (OVCLAMP = OV, TMR = 68 nF)**



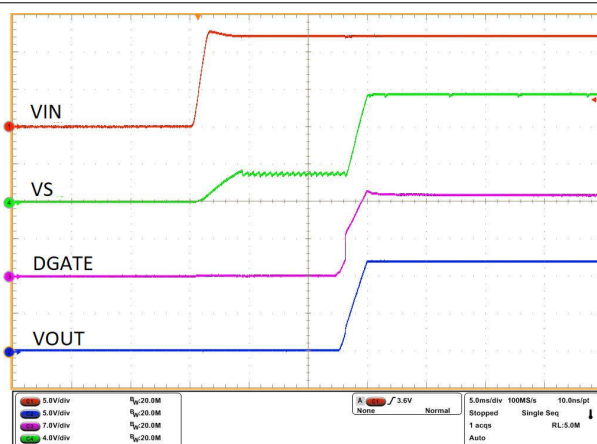
**Figure 8-4. Unsuppressed Load Dump 200 V - Output Cut-off**



**Figure 8-5. ISO 7637-2 Pulse 1 -600 V 50 Ω**



**Figure 8-6. Input Supply Short Interruption (100 μs)**



**Figure 8-7. Power up 12 V - DGATE and Output**

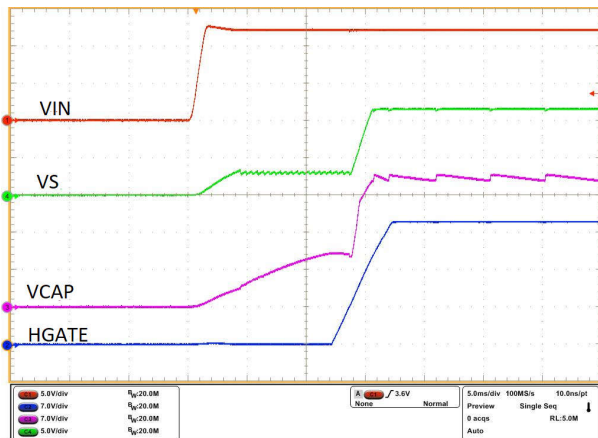


Figure 8-8. Power up 12 V - Charge Pump VCAP

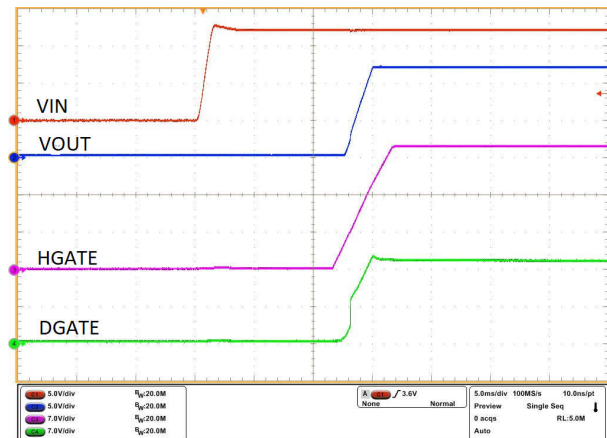


Figure 8-9. Power up 12 V - DGATE and HGATE

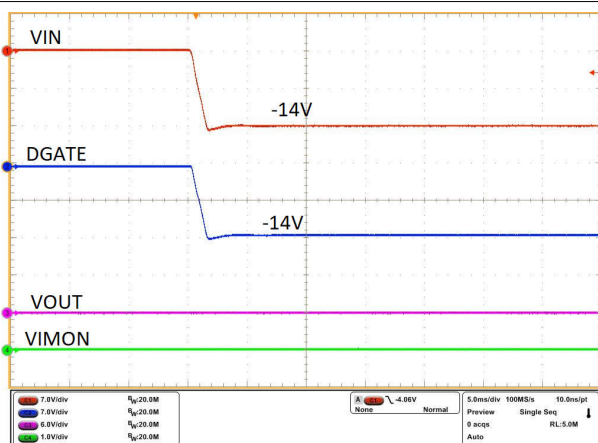


Figure 8-10. Input Reverse Polarity (-14 V)

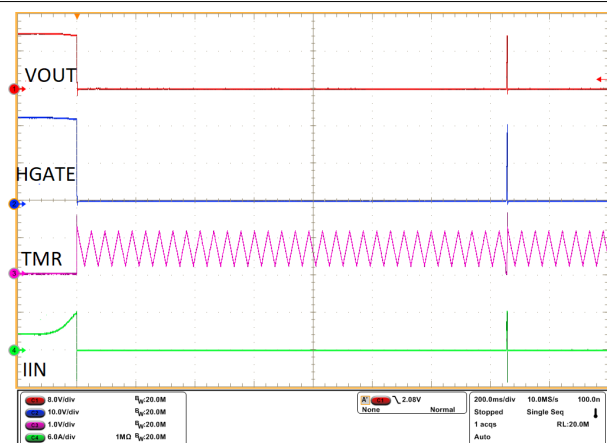


Figure 8-11. Overcurrent Protection with Circuit Breaker (5-A)

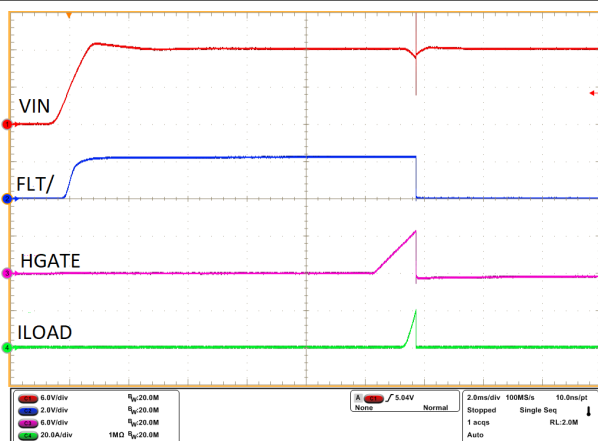


Figure 8-12. Device Wake-Up with Output Short to Ground

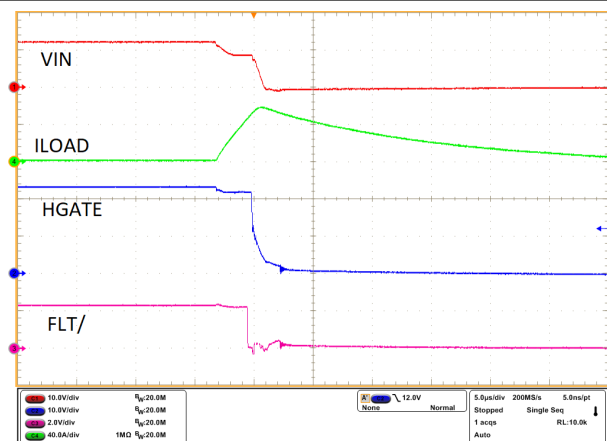


Figure 8-13. Output Short-Circuit Protection On-the-Fly

### 8.3 Best Design Practices

Leave the exposed pad (RTN) of the IC floating. Do not connect it to the GND plane. Connecting RTN to GND disables the Reverse Polarity protection feature.

## 8.4 Power Supply Recommendations

### 8.4.1 Transient Protection

When the external MOSFETs turn OFF during the conditions such as overvoltage cut-off, reverse current blocking, EN/UVLO causing an interruption of the current flow, the input line inductance generates a positive voltage spike on the input and output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) depends on the value of inductance in series to the input or output of the device. These transients can exceed the *Absolute Maximum Ratings* of the device if steps are not taken to address the issue.

Typical methods for addressing transients include:

- Minimizing lead length and inductance into and out of the device.
- Using large PCB GND plane.
- Use of a Schottky diode across the output and GND to absorb negative spikes.
- A low value ceramic capacitor ( $C_{IN}$ ) to approximately 0.1  $\mu\text{F}$  to absorb the energy and dampen the transients.

The approximate value of input capacitance can be estimated with [Equation 20](#).

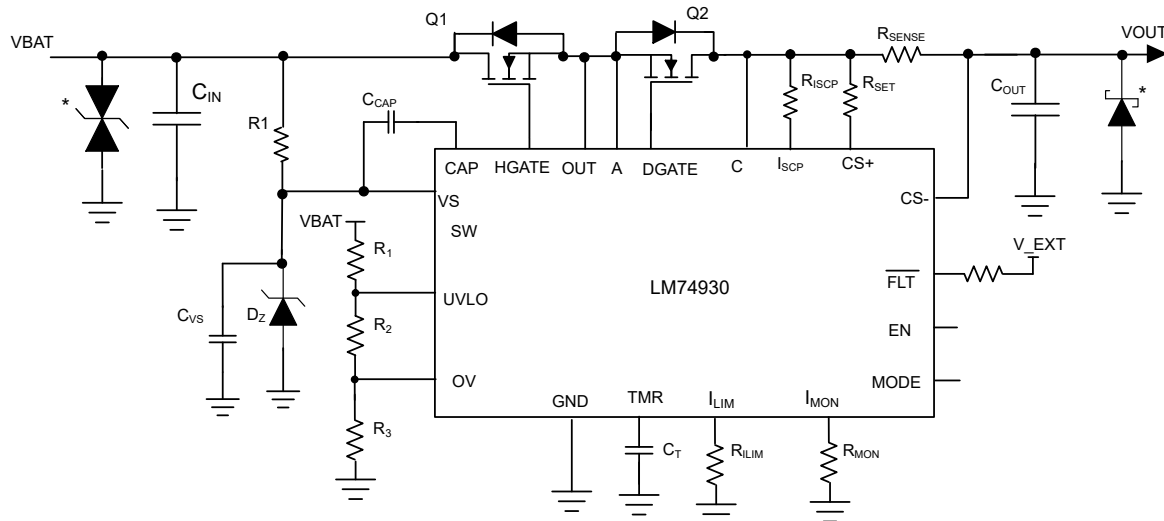
$$V_{\text{SPIKE\_MAX}} = V_{IN} + I_{\text{LOAD}} \times \sqrt{\frac{L_{IN}}{C_{IN}}} \quad (20)$$

where

- $V_{(IN)}$  is the nominal supply voltage
- $I_{(LOAD)}$  is the load current
- $L_{(IN)}$  equals the effective inductance seen looking into the source
- $C_{(IN)}$  is the capacitance present at the input

Some applications can require additional Transient Voltage Suppressor (TVS) to prevent transients from exceeding the *Absolute Maximum Ratings* of the device. These transients can occur during EMC testing such as automotive ISO7637 pulses.

The circuit implementation with optional protection components (a ceramic capacitor, TVS and Schottky diode) is shown in [Figure 8-14](#)



\* Optional components needed for suppression of transients

**Figure 8-14. Circuit Implementation with Optional Protection Components for LM74930-Q1**

## 8.4.2 TVS Selection for 12-V Battery Systems

In selecting the TVS, important specifications are breakdown voltage and clamping voltage. The breakdown voltage of the TVS+ must be higher than 24-V jump start voltage and 35-V suppressed load dump voltage and less than the maximum ratings of LM74930-Q1 (65 V). The breakdown voltage of TVS- must be beyond than maximum reverse battery voltage –16 V, so that the TVS- is not damaged due to long time exposure to reverse connected battery.

Clamping voltage is the voltage the TVS diode clamps in high current pulse situations and this voltage is much higher than the breakdown voltage. In the case of an ISO 7637-2 pulse 1, the input voltage goes up to –150 V with a generator impedance of 10  $\Omega$ . This translates to 15 A flowing through the TVS-, and the voltage across the TVS can be close to the clamping voltage.

The next criterion is that the absolute maximum rating of cathode to anode voltage of the LM74930-Q1 (85 V) and the maximum  $V_{DS}$  rating MOSFET are not exceeded. In the design example, 60-V rated MOSFET is chosen and maximum limit on the cathode to anode voltage is 60 V.

During ISO 7637-2 pulse 1, the anode of LM74930-Q1 is pulled down by the ISO pulse, clamped by TVS- and the MOSFET Q1 is turned off quickly to prevent reverse current from discharging the bulk output capacitors. When the MOSFET turns off, the cathode to anode voltage seen is equal to (TVS Clamping voltage + Output capacitor voltage). If the maximum voltage on output capacitor is 16 V (maximum battery voltage), then the clamping voltage of the TVS- must not exceed,  $(60\text{ V} - 16\text{ V}) = -44\text{ V}$ .

The SMBJ33CA TVS diode can be used for 12-V battery protection application. The breakdown voltage of 36.7 V meets the jump start, load dump requirements on the positive side and 16-V reverse battery connection on the negative side. During ISO 7637-2 pulse 1 test, the SMBJ33CA clamps at –44 V with 12 A of peak surge current as shown in and it meets the clamping voltage  $\leq 44\text{ V}$ .

SMBJ series of TVS are rated up to 600-W peak pulse power levels and are sufficient for ISO 7637-2 pulses.

## 8.4.3 TVS Selection for 24-V Battery Systems

For 24-V battery protection application, the TVS and MOSFET in [Figure 8-1](#) must be changed to meet 24-V battery requirements.

The breakdown voltage of the TVS+ must be higher than 48-V jump start voltage, less than the absolute maximum ratings of anode and enable pin of LM74930-Q1 (70 V) and must withstand 65-V suppressed load dump. The breakdown voltage of TVS- must be lower than maximum reverse battery voltage –32 V, so that the TVS- is not damaged due to long time exposure to reverse connected battery.

During ISO 7637-2 pulse 1, the input voltage goes up to –600 V with a generator impedance of 50  $\Omega$ . This translates to 12-A flowing through the TVS-. The clamping voltage of the TVS- cannot be same as that of 12-V battery protection circuit. Because during the ISO 7637-2 pulse, the Anode to Cathode voltage seen is equal to (-TVS Clamping voltage + Output capacitor voltage). For 24-V battery application, the maximum battery voltage is 32 V, then the clamping voltage of the TVS- must not exceed,  $85\text{ V} - 32\text{ V} = 53\text{ V}$ .

Single bi-directional TVS cannot be used for 24-V battery protection because breakdown voltage for TVS+  $\geq 65\text{V}$ , maximum clamping voltage is  $\leq 53\text{ V}$  and the clamping voltage cannot be less than the breakdown voltage. Two un-directional TVS connected back-back needs to be used at the input. For positive side TVS+, SMBJ58A with the breakdown voltage of 64.4 V (minimum), TI recommends 67.8 (typical). For the negative side TVS-, TI recommends SMBJ28A with breakdown voltage close to 32 V (to withstand maximum reverse battery voltage –32 V) and maximum clamping voltage of 42.1 V.

For 24-V battery protection, TI recommends a 75-V rated MOSFET to be used along with SMBJ28A and SMBJ58A connected back-back at the input.

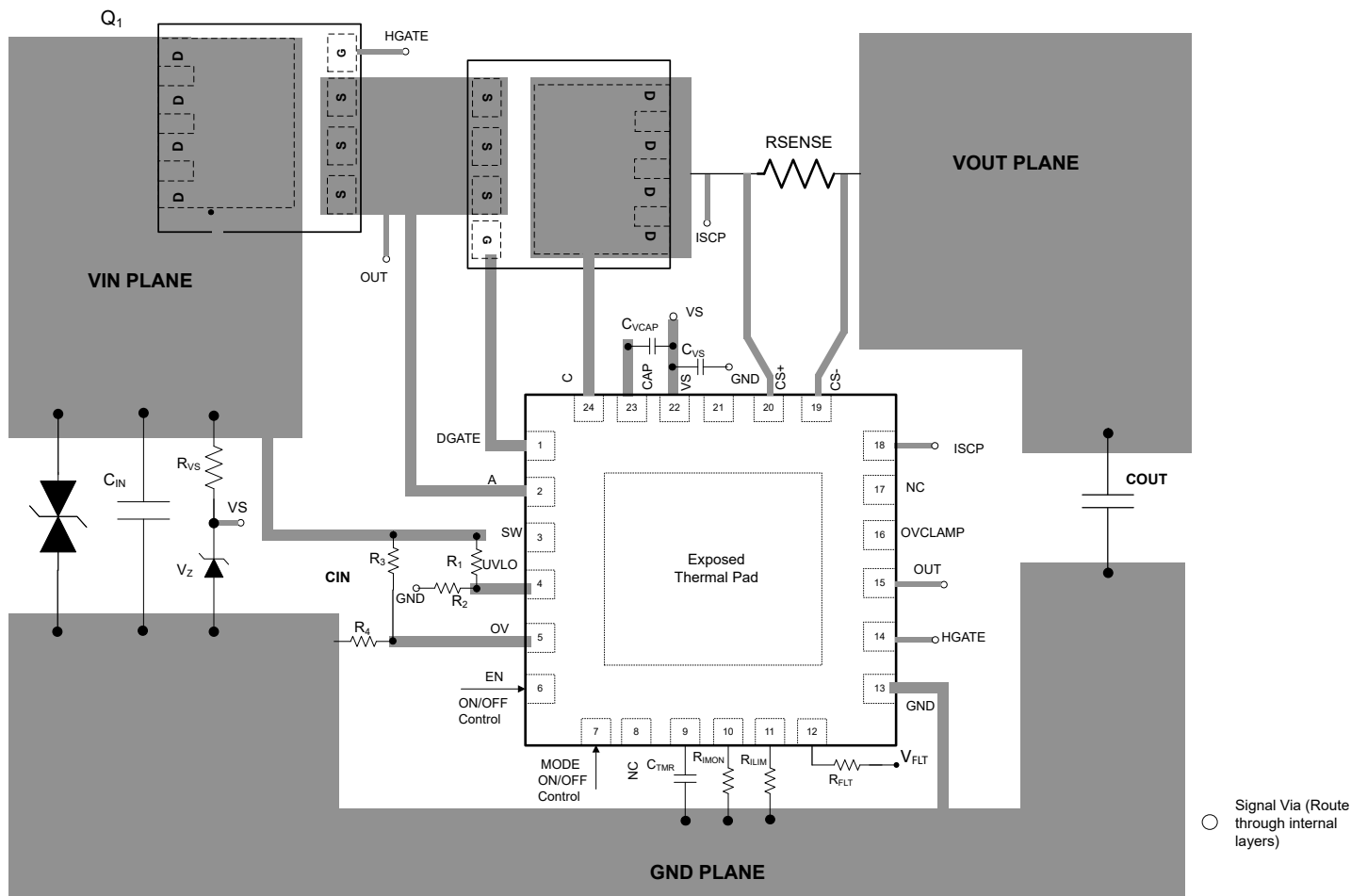
## 8.5 Layout

### 8.5.1 Layout Guidelines

- Connect A, DGATE and C pins of LM74930-Q1 close to the MOSFET SOURCE, GATE and DRAIN pins for the ideal diode stage.

- Connect HGATE and OUT pins of LM74930-Q1 close to the MOSFET GATE and SOURCE pins for the load disconnect stage.
- Use thick and short traces for source and drain of the MOSFET to minimize resistive losses. The high current path for this design is through the MOSFET.
- Connect the DGATE pin of the LM74930-Q1 to the MOSFET GATE with short trace.
- Follow kelvin connection for connecting CS+ and CS- pin to external current sense resistor.
- Place transient suppression components close to LM74930-Q1.
- Place the decoupling capacitor,  $C_{VS}$ , close to VS pin and chip GND.
- Keep the charge pump capacitor across CAP and VS pins away from the MOSFET to lower the thermal effects on the capacitance value.
- Obtaining acceptable performance with alternate layout schemes is possible, however the layout shown in the [Layout Example](#) is intended as a guideline and to produce good results.

### 8.5.2 Layout Example



**Figure 8-15. PCB Layout Example**

## 9 Device and Documentation Support

### 9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 9.3 Trademarks

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All trademarks are the property of their respective owners.

### 9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable part number | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-----------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| LM74930QRGERQ1        | Active        | Production           | VQFN (RGE)   24 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | LM<br>74930Q        |
| LM74930QRGERQ1.A      | Active        | Production           | VQFN (RGE)   24 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | LM<br>74930Q        |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LM74930QRGERQ1 | VQFN         | RGE             | 24   | 3000 | 330.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

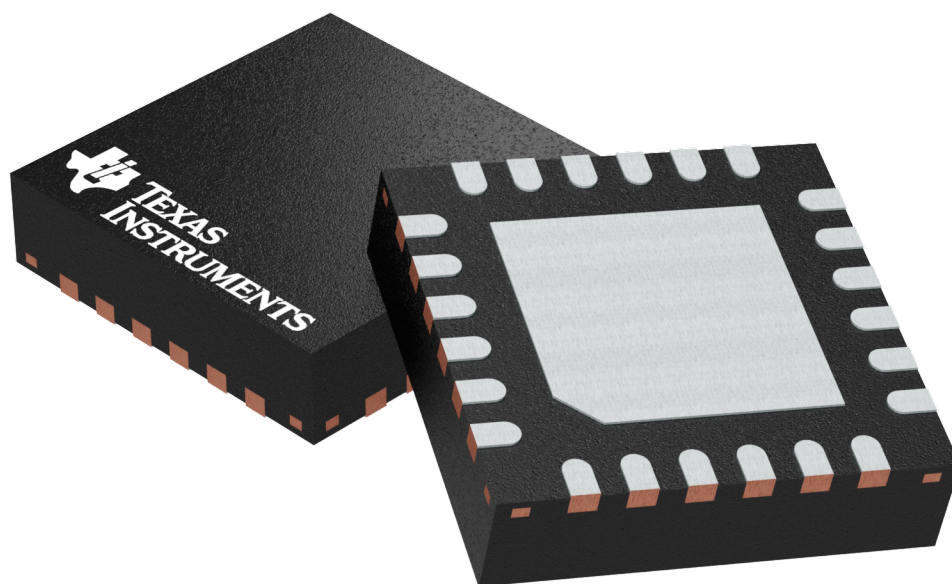
| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LM74930QRGERQ1 | VQFN         | RGE             | 24   | 3000 | 367.0       | 367.0      | 35.0        |

**RGE 24**

**GENERIC PACKAGE VIEW**

**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



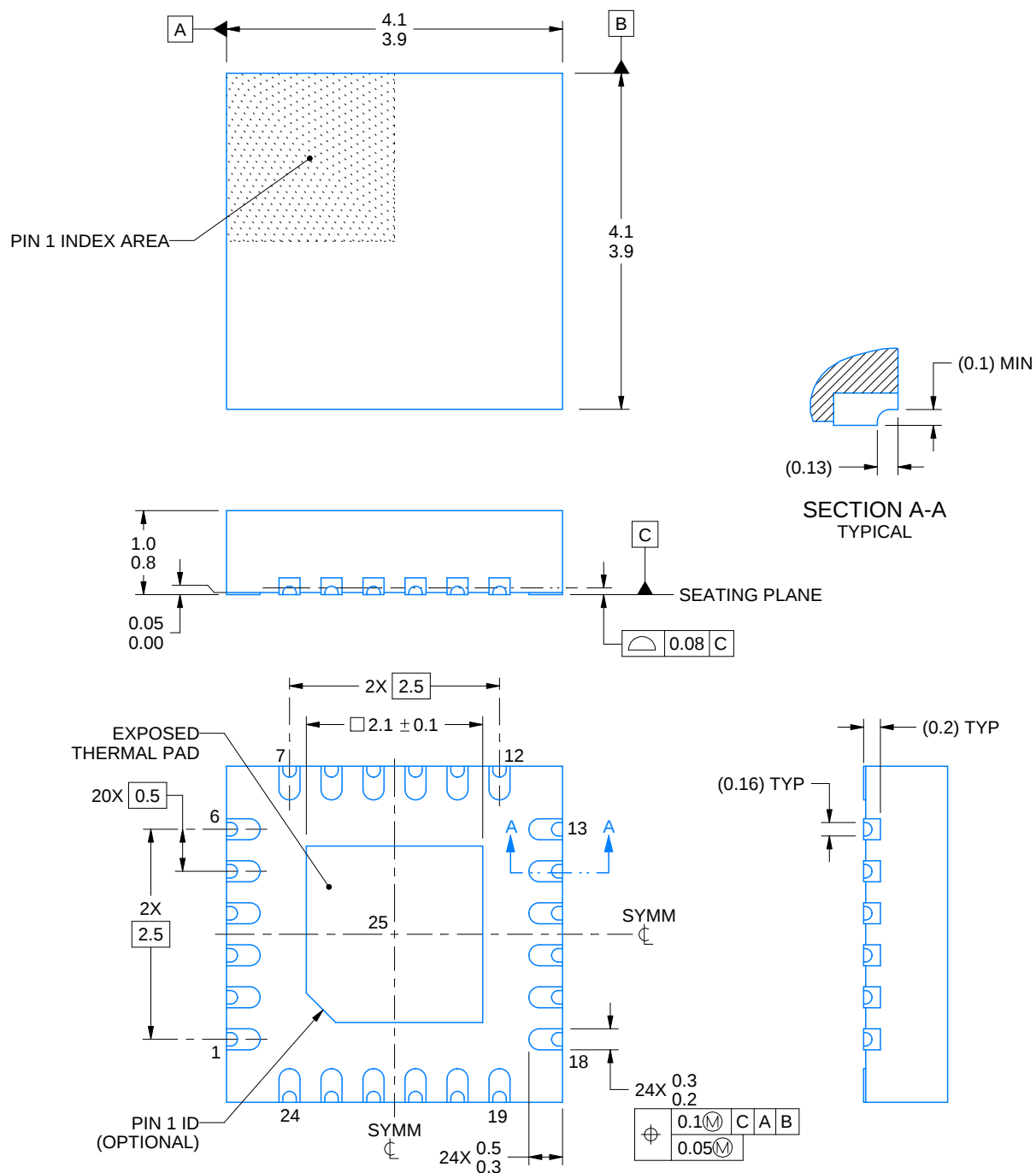
Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4204104/H



## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4228214/A 11/2021

NOTES:

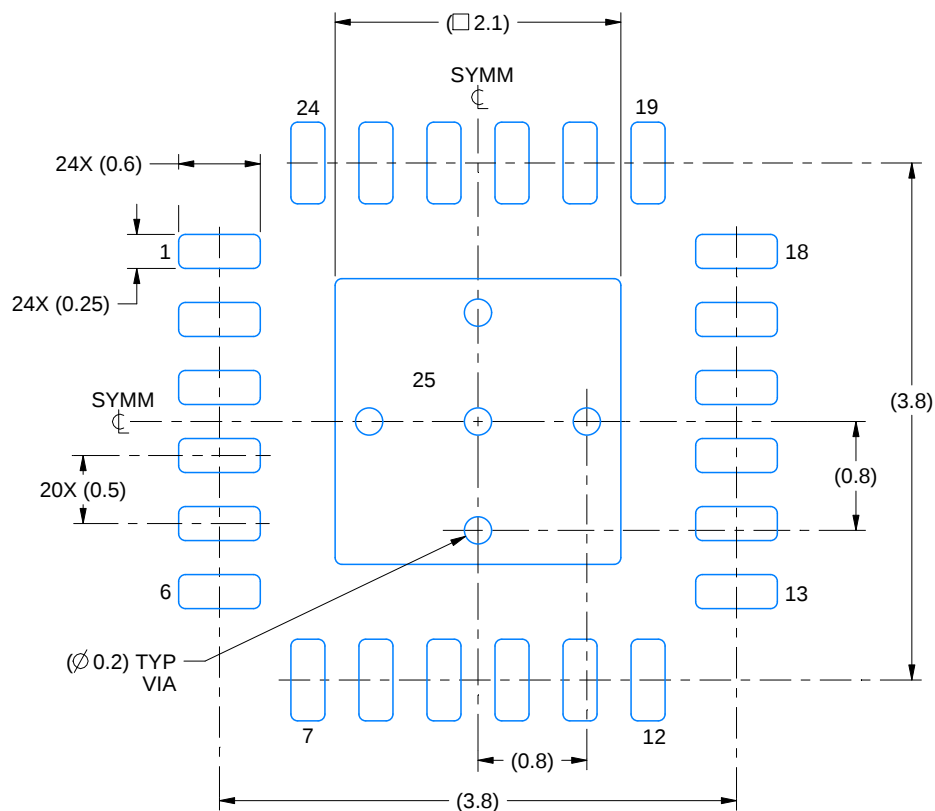
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

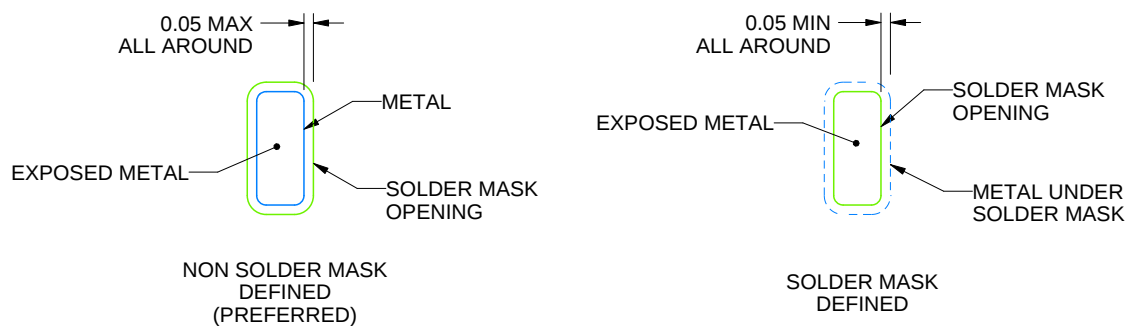
RGE0024T

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**LAND PATTERN EXAMPLE**  
EXPOSED METAL SHOWN  
SCALE:18X



**SOLDER MASK DETAILS**

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NOTES: (continued)

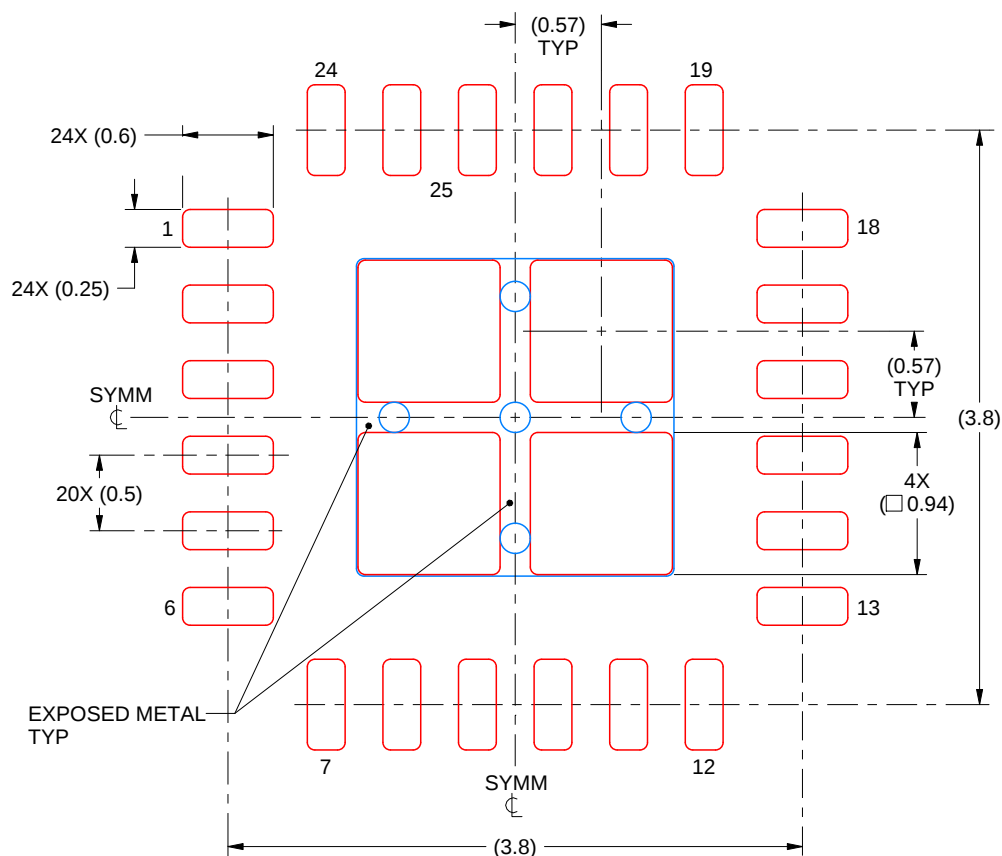
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RGE0024T

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



## SOLDER PASTE EXAMPLE BASED ON 0.1 mm THICK STENCIL

THERMAL PAD 25:  
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:20X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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