LM7121 235-MHz Tiny Low Power Voltage Feedback Amplifier

1 Features

- (Typical Unless Otherwise Noted). V_S = ±15 V
- Easy to use Voltage Feedback Topology
- Stable with Unlimited Capacitive Loads
- Tiny SOT23-5 Package — Typical Circuit Layout Takes Half the Space Of SO-8 Designs
- Unity Gain Frequency: 175 MHz
- Bandwidth (−3 dB, A_V = +1, R_L = 100Ω): 235 MHz
- Slew Rate: 1300V/µs
- Supply Voltages:
  - SO-8: 5 V to ±15 V
  - SOT23-5: 5 V to ±5 V
- Characterized for: +5 V, ±5 V, ±15 V
- Low Supply Current: 5.3 mA

2 Applications

- Scanners, Color Fax, Digital Copiers
- PC Video Cards
- Cable Drivers
- Digital Cameras
- ADC/DAC Buffers
- Set-top Boxes

3 Description

The LM7121 is a high performance operational amplifier which addresses the increasing AC performance needs of video and imaging applications, and the size and power constraints of portable applications.

The LM7121 can operate over a wide dynamic range of supply voltages, from 5 V (single supply) up to ±15V (see *Application and Implementation* for more details). It offers an excellent speed-power product delivering 1300 V/µs and 235 MHz Bandwidth (−3 dB, A_V = +1). Another key feature of this operational amplifier is stability while driving unlimited capacitive loads.

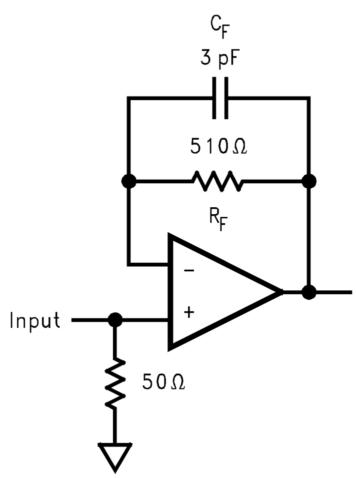
Due to its tiny SOT23-5 package, the LM7121 is ideal for designs where space and weight are the critical parameters. The benefits of the tiny package are evident in small portable electronic devices, such as cameras, and PC video cards. Tiny amplifiers are so small that they can be placed anywhere on a board close to the signal source or near the input to an A/D converter.

Device Information(1)

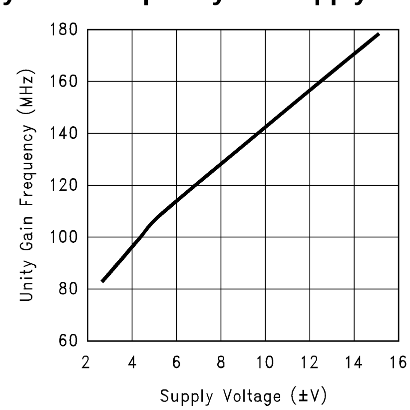
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM7121	SOT-23 (5)	2.921 mm × 1.651 mm
	SOIC (8)	4.902 mm × 3.912 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Circuit for A_V = +1 Operation (V_S= 6 V)



Unity Gain Frequency vs. Supply Voltage



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4 Revision History

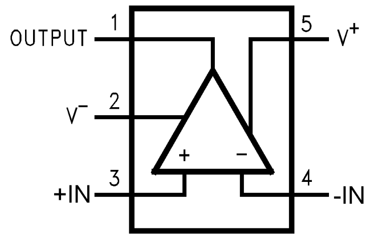
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (August 1999) to Revision A — **Page**

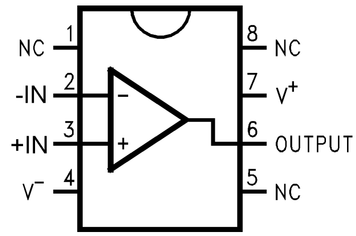
- Added, updated, or renamed the following sections: Device Information Table, *Pin Configuration and Functions*, *Application and Implementation*; *Power Supply Recommendations* ; *Layout*; *Device and Documentation Support*; *Mechanical, Packaging, and Ordering Information* 1
- Deleted T_J = 25°C from Electrical Characteristics tables 5

5 Pin Configuration and Functions

Package DBV
5-Pin
Top View



Package D0008A
8-Pin
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	NUMBER			
	DBV	D0008A		
-IN	4	2	I	Inverting input
+IN	3	3	I	Non-inverting input
N/C	—	5, 8	—	No connection
OUTPUT	1	6	O	Output
V^-	2	4	I	Negative supply
V^+	5	7	I	Positive supply

6 Specifications

6.1 Absolute Maximum Ratings[(1)]

over operating free-air temperature range (unless otherwise noted) [(1)]

	MIN	MAX	UNIT
Differential Input Voltage [(2)]		±2	V
Voltage at Input/Output Pins		(V+)−1.4, (V−)+1.4	V
Supply Voltage (V+–V−)		36	V
Output Short Circuit to Ground [(3)]		Continuous	
Lead Temperature (soldering, 10 sec)		260	°C
Junction Temperature[(4)]		150	˚C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(3) The maximum power dissipation is a function of $T_{J(max)}$, $R_{θJA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)}–T_A)/R_{θJA}$. All numbers apply for packages soldered directly into a PC board.
(4) Typical Values represent the most likely parametric norm.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		−65	+150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)]		2000	V

(1) JEDEC document JEP155 states that 2000-V HBM allows safe manufacturing with a standard ESD control process. Human body model, 1.5 k in series with 100 pF.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Operating Temperature Range	-40		85	°C

6.4 Thermal Information

THERMAL METRIC[(1)]		D0008A (8)	DBV (5)	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance	165	325	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 ±15V DC Electrical Characteristics

Unless otherwise specified, all limits ensured for $V^+ = +15V$, $V^- = -15V$, $V_{CM} = V_O = 0$ V and $R_L > 1$ MΩ. **Boldface** limits apply at the temperature extremes.

PARAMETER		TEST CONDITIONS	TYP(1)	LM7121I LIMIT(2)	UNIT
V_{OS}	Input Offset Voltage		0.9	8 **15**	mV max
I_B	Input Bias Current		5.2	9.5 **12**	µA max
I_{OS}	Input Offset Current		0.04	4.3 **7**	µA max
R_{IN}	Input Resistance	Common Mode	10		MΩ
		Differential Mode	3.4		MΩ
C_{IN}	Input Capacitance	Common Mode	2.3		pF
CMRR	Common Mode Rejection Ratio	$-10V \le V_{CM} \le 10V$	93	73 **70**	dB min
+PSRR	Positive Power Supply Rejection Ratio	$10V \le V^+ \le 15$ V	86	70 **68**	dB min
−PSRR	Negative Power Supply Rejection Ratio	$-15V \le V^- \le -10V$	81	68 **65**	dB min
V_{CM}	Input Common-Mode Voltage Range	CMRR ≥ 70 dB	13	11	V min
			−13	−11	V max
A_V	Large Signal Voltage Gain	$R_L = 2$ kΩ , $V_O = 20$ V_{PP}	72	65 **57**	dB min
V_O	Output Swing	$R_L = 2$ kΩ	13.4	11.1 **10.8**	V min
			−13.4	−11.2 **−11.0**	V max
		$R_L = 150$ Ω	10.2	7.75 **7.0**	V min
			−7.0	−5.0 **−4.8**	V max
I_{SC}	Output Short Circuit Current	Sourcing	71	54 **44**	mA min
		Sinking	52	39 **34**	mA min
I_S	Supply Current		5.3	6.6 **7.5**	mA max

(1) Typical Values represent the most likely parametric norm.
(2) All limits are ensured by testing or statistical analysis.

6.6 ±15V AC Electrical Characteristics

Unless otherwise specified, all limits ensured for V+ = 15V, V^- = −15V, V_{CM} = V_O = 0 V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

PARAMETER		TEST CONDITIONS	TYP (1)	LM7121I LIMIT (2)	UNIT
SR	Slew Rate (3)	A_V = +2, R_L = 1 kΩ, V_O = 20 V_{PP}	1300		V/µs
GBW	Unity Gain-Bandwidth	R_L = 1 kΩ	175		MHz
$Ø_m$	Phase Margin		63		Deg
f (−3 dB)	Bandwidth (4) (5)	R_L = 100 Ω, A_V = +1	235		MHz
		R_L = 100 Ω, A_V = +2	50		
t_s	Settling Time	10 V_{PP} Step, to 0.1%, R_L = 500 Ω	74		ns
t_r, t_f	Rise and Fall Time (5)	A_V = +2, R_L = 100 Ω, V_O = 0.4 V_{PP}	5.3		ns
A_D	Differential Gain	A_V = +2, R_L = 150 Ω	0.3%		
$Ø_D$	Differential Phase	A_V = +2, R_L = 150 Ω	0.65		Deg
e_n	Input-Referred Voltage Noise	f = 10 kHz	17		nV / √HZ
i_n	Input-Referred Current Noise	f = 10 kHz	1.9		pA / √HZ
T.H.D.	Total Harmonic Distortion	2 V_{PP} Output, R_L = 150 Ω, A_V = +2, f = 1 MHz	0.065%		
		2 V_{PP} Output, R_L = 150 Ω, A_V = +2, f = 5 MHz	0.52%		

(1) Typical Values represent the most likely parametric norm.
(2) All limits are ensured by testing or statistical analysis.
(3) Slew rate is the average of the rising and falling slew rates.
(4) Unity gain operation for ±5 V and ±15 V supplies is with a feedback network of 510 Ω and 3 pF in parallel (see *Application and Implementation*). For +5V single supply operation, feedback is a direct short from the output to the inverting input.
(5) A_V = +2 operation with 2 kΩ resistors and 2 pF capacitor from summing node to ground.

6.7 ±5V DC Electrical Characteristics

Unless otherwise specified, all limits ensured for V+ = 5V, V^- = −5V, V_{CM} = V_O = 0 V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

PARAMETER		TEST CONDITIONS	TYP (1)	LM7121I LIMIT (2)	UNIT
V_{OS}	Input Offset Voltage		1.6	8 **15**	mV max
I_B	Input Bias Current		5.5	9.5 **12**	µA max
I_{OS}	Input Offset Current		0.07	4.3 **7.0**	µA max
R_{IN}	Input Resistance	Common Mode	6.8		MΩ
		Differential Mode	3.4		MΩ
C_{IN}	Input Capacitance	Common Mode	2.3		pF
CMRR	Common Mode Rejection Ratio	−2V ≤ V_{CM} ≤ 2V	75	65 **60**	dB min
+PSRR	Positive Power Supply Rejection Ratio	3V ≤ V^+ ≤ 5V	89	65 **60**	dB min
−PSRR	Negative Power Supply Rejection Ratio	−5V ≤ V^- ≤ −3V	78	65 **60**	dB min

(1) Typical Values represent the most likely parametric norm.
(2) All limits are ensured by testing or statistical analysis.

±5V DC Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for V+ = 5V, V^- = −5V, V_{CM} = V_O = 0 V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

PARAMETER		TEST CONDITIONS	TYP[1]	LM7121I LIMIT[2]	UNIT
V_{CM}	Input Common Mode Voltage Range	CMRR ≥ 60 dB	3	2.5	V min
			−3	−2.5	V max
A_V	Large Signal Voltage Gain	R_L = 2 kΩ, V_O = 3 V_{PP}	66	60 **58**	dB min
V_O	Output Swing	R_L = 2 kΩ	3.62	3.0 **2.75**	V min
			−3.62	−3.0 **−2.70**	V max
		R_L = 150 Ω	3.1	2.5 **2.3**	V min
			−2.8	−2.15 **−2.00**	V max
I_{SC}	Output Short Circuit Current	Sourcing	53	38 **33**	mA min
		Sinking	29	21 **19**	mA min
I_S	Supply Current		5.1	6.4 **7.2**	mA max

6.8 ±5V AC Electrical Characteristics

Unless otherwise specified, all limits ensured for V^+ = 5V, V^- = −5V, V_{CM} = V_O = 0 V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

PARAMETER		TEST CONDITIONS	TYP[1]	LM7121I LIMIT[2]	UNIT
SR	Slew Rate[3]	A_V = +2, R_L = 1 kΩ, V_O = 6 V_{PP}	520		V/µs
GBW	Unity Gain-Bandwidth	R_L = 1 kΩ	105		MHz
$Ø_m$	Phase Margin	R_L = 1 kΩ	74		Deg
f (−3 dB)	Bandwidth[4][5]	R_L = 100 Ω, A_V = +1	160		MHz
		R_L = 100 Ω, A_V = +2	50		MHz
t_s	Settling Time	5 V_{PP} Step, to 0.1%, R_L = 500 Ω	65		ns
t_r, t_f	Rise and Fall Time[5]	A_V = +2, R_L = 100 Ω, V_O = 0.4 V_{PP}	5.8		ns
A_D	Differential Gain	A_V = +2, R_L = 150 Ω	0.3%		
$Ø_D$	Differential Phase	A_V = +2, R_L = 150 Ω	0.65		Deg
e_n	Input-Referred Voltage Noise	f = 10 kHz	17		nV / √Hz
i_n	Input-Referred Current Noise	f = 10 kHz	2		pA / √Hz
T.H.D.	Total Harmonic Distortion	2 V_{PP} Output, R_L = 150 Ω, A_V = +2, f = 1 MHz	0.1%		
		2 V_{PP} Output, R_L = 150 Ω, A_V = +2, f = 5 MHz	0.6		

(1) Typical Values represent the most likely parametric norm.
(2) All limits are ensured by testing or statistical analysis.
(3) Slew rate is the average of the rising and falling slew rates.
(4) Unity gain operation for ±5 V and ±15 V supplies is with a feedback network of 510 Ω and 3 pF in parallel (see *Application and Implementation*). For +5V single supply operation, feedback is a direct short from the output to the inverting input.
(5) A_V = +2 operation with 2 kΩ resistors and 2 pF capacitor from summing node to ground.

6.9 +5V DC Electrical Characteristics

Unless otherwise specified, all limits ensured for $V^+ = +5V$, $V^- = 0$ V, $V_{CM} = V_O = V^+/2$ and $R_L > 1$ MΩ. **Boldface** limits apply at the temperature extremes.

PARAMETER		TEST CONDITIONS	TYP (1)	LM7121I LIMIT (2)	UNIT
V_{OS}	Input Offset Voltage		2.4		mV
I_B	Input Bias Current		4		µA
I_{OS}	Input Offset Current		0.04		µA
R_{IN}	Input Resistance	Common Mode	2.6		M
		Differential Mode	3.4		M
C_{IN}	Input Capacitance	Common Mode	2.3		pF
CMRR	Common Mode Rejection Ratio	$2V \le V_{CM} \le 3V$	65		dB
+PSRR	Positive Power Supply Rejection Ratio	$4.6V \le V^+ \le 5V$	85		dB
−PSRR	Negative Power Supply Rejection Ratio	$0V \le V^- \le 0.4V$	61		dB
V_{CM}	Input Common-Mode Voltage Range	CMRR 45 dB	3.5		V min
			1.5		V max
A_V	Large Signal Voltage Gain	$R_L = 2$ kΩ to $V^+/2$	64		dB
V_O	Output Swing	$R_L = 2$ kΩ to $V^+/2$, High	3.7		V
		$R_L = 2$ kΩ to $V^+/2$, Low	1.3		
		$R_L = 150$ Ω to $V^+/2$, High	3.48		
		$R_L = 150$ Ω to $V^+/2$, Low	1.59		
I_{SC}	Output Short Circuit Current	Sourcing	33		mA
		Sinking	20		mA
I_S	Supply Current		4.8		mA

(1) Typical Values represent the most likely parametric norm.
(2) All limits are ensured by testing or statistical analysis.

6.10 +5V AC Electrical Characteristics

Unless otherwise specified, all limits ensured for $V^+ = +5V$, $V^- = 0$ V, $V_{CM} = V_O = V^+/2$ and $R_L > 1$ MΩ. **Boldface** limits apply at the temperature extremes.

PARAMETER		TEST CONDITIONS	TYP (1)	LM7121I LIMIT (2)	UNIT
SR	Slew Rate (3)	$A_V = +2$, $R_L = 1$ kΩ to $V^+/2$, $V_O = 1.8$ V_{PP}	145		V/µs
GBW	Unity Gain-Bandwidth	$R_L = 1k$ to $V^+/2$	80		MHz
$Ø_m$	Phase Margin	$R_L = 1k$ to $V^+/2$	70		Deg
f (−3 dB)	Bandwidth (4) (5)	$R_L = 100$ Ω to $V^+/2$, $A_V = +1$	200		MHz
		$R_L = 100$ Ω to $V^+/2$, $A_V = +2$	45		
t_r, t_f	Rise and Fall Time (5)	$A_V = +2$, $R_L = 100$ Ω , $V_O = 0.2$ V_{PP}	8		ns
T.H.D.	Total Harmonic Distortion	0.6 V_{PP} Output, $R_L = 150$ Ω, $A_V = +2$, f = 1 MHz	0.067%		
		0.6 V_{PP} Output, $R_L = 150$ Ω, $A_V = +2$, f = 5 MHz	0.33%		

(1) Typical Values represent the most likely parametric norm.
(2) All limits are ensured by testing or statistical analysis.
(3) Slew rate is the average of the rising and falling slew rates.
(4) Unity gain operation for ±5 V and ±15 V supplies is with a feedback network of 510 Ω and 3 pF in parallel (see *Application and Implementation*). For +5V single supply operation, feedback is a direct short from the output to the inverting input.
(5) $A_V = +2$ operation with 2 kΩ resistors and 2 pF capacitor from summing node to ground.

6.11 Typical Characteristics

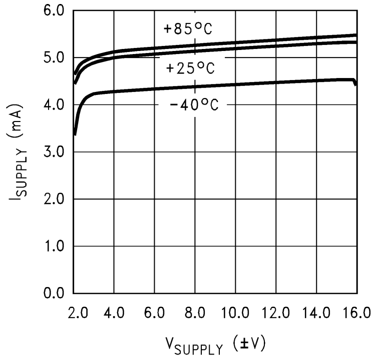


Figure 1. Supply Current vs. Supply Voltage

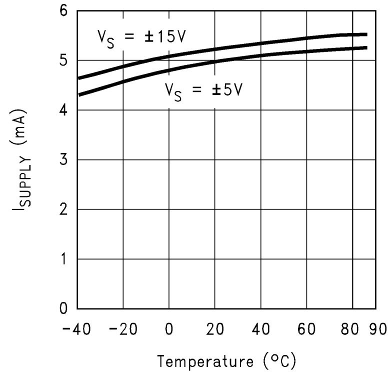


Figure 2. Supply Current vs. Temperature

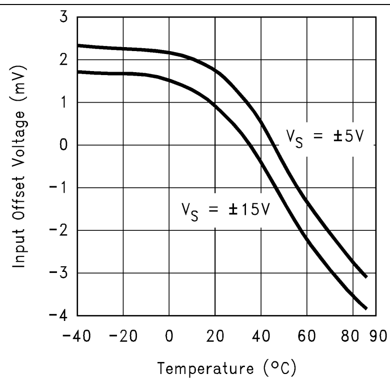


Figure 3. Input Offset Voltage vs. Temperature

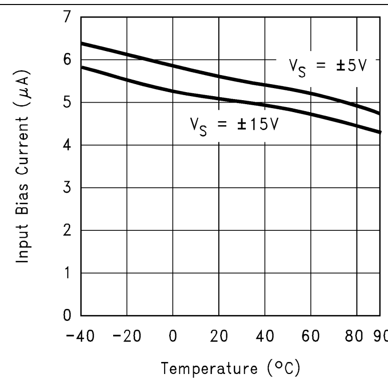


Figure 4. Input Bias Current vs Temperature

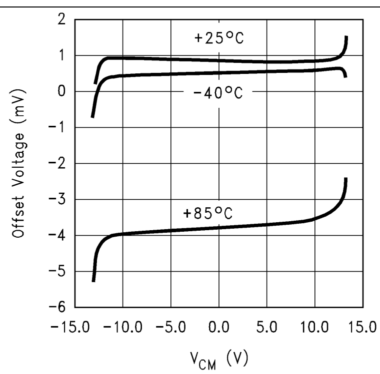


Figure 5. Input Offset Voltage vs. Common Mode Voltage at V_S = ±15 V

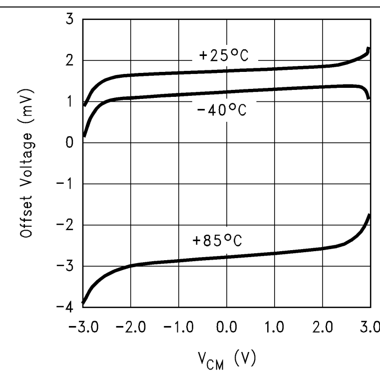


Figure 6. Input Offset Voltage vs. Common Mode Voltage at V_S = ±5 V

Typical Characteristics (continued)

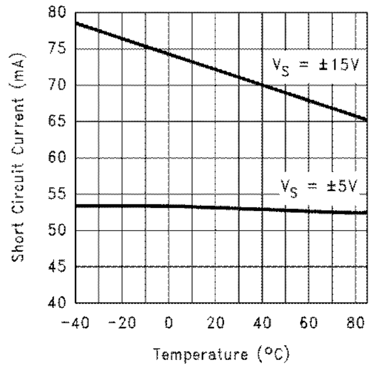


Figure 7. Short Circuit Current vs. Temperature (Sourcing)

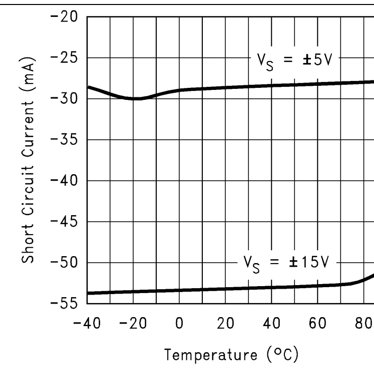


Figure 8. Short Circuit Current vs Temperature (Sinking)

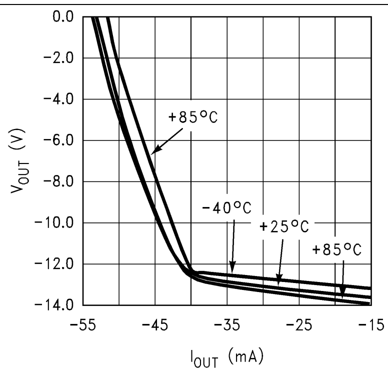


Figure 9. Output Voltage vs Output Current (I_{SINK}, V_S = ±15 V)

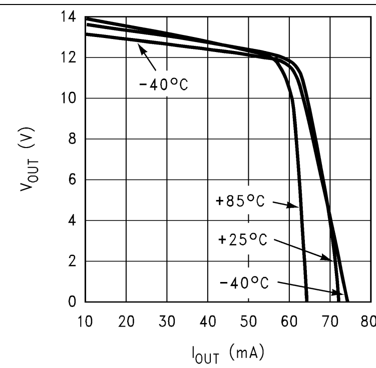


Figure 10. Output Voltage vs Output Current (I_{SOURCE}, V_S = ±15 V)

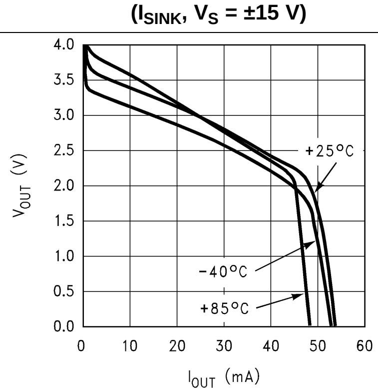


Figure 11. Output Voltage vs Output Current (I_{SOURCE}, V_S = ±5 V)

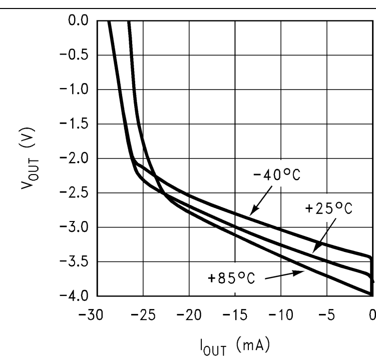


Figure 12. Output Voltage vs Output Current (I_{SINK}, V_S = ±5 V)

Typical Characteristics (continued)

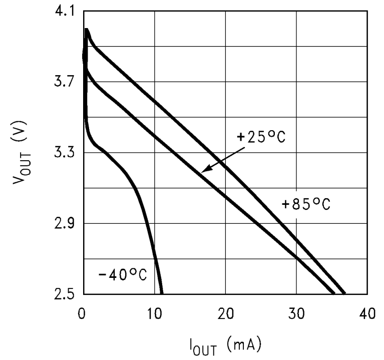


Figure 13. Output Voltage vs. Output Current (I_{SOURCE}, V_S = +5 V)

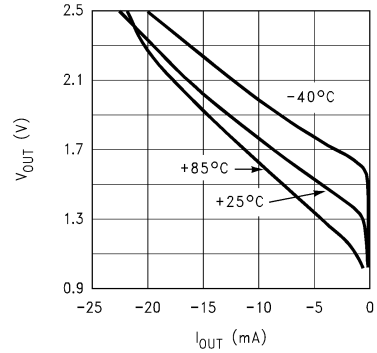


Figure 14. Output Voltage vs Output Current (I_{SINK}, V_S = +5 V)

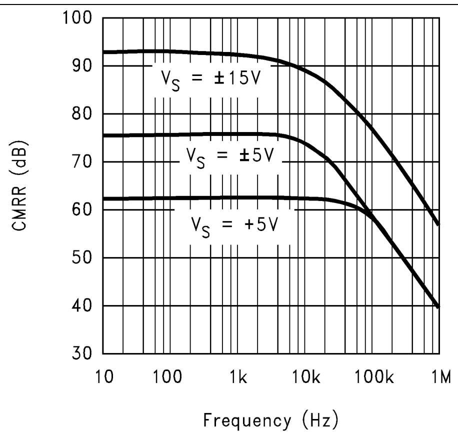


Figure 15. CMRR vs. Frequency

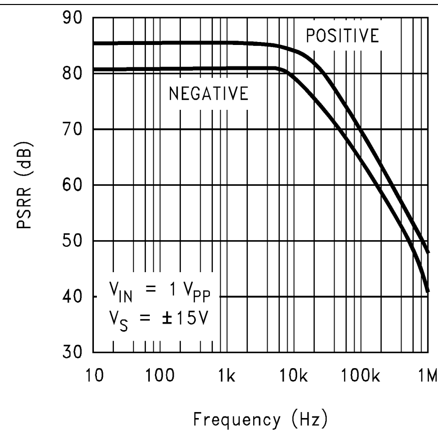


Figure 16. PSRR vs. Frequency

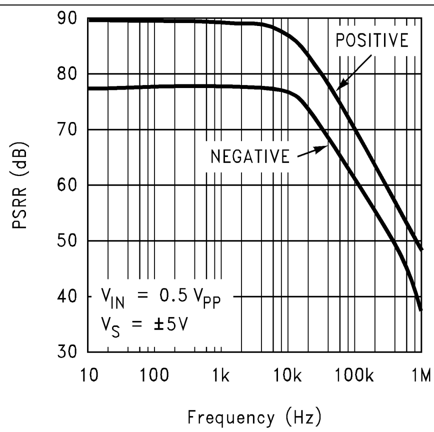


Figure 17. PSRR vs. Frequency

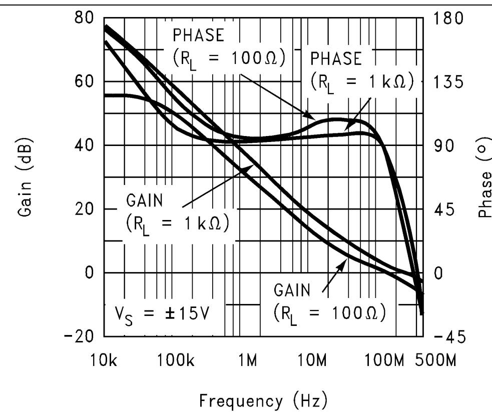


Figure 18. Open Loop Frequency Response

Typical Characteristics (continued)

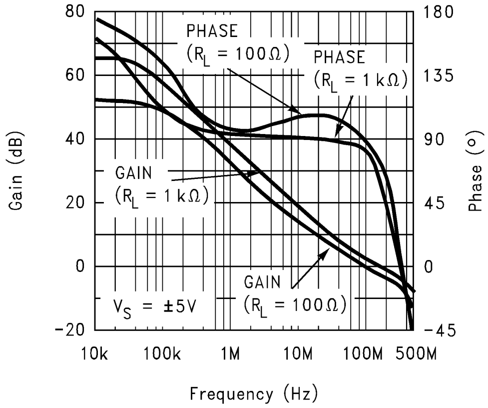


Figure 19. Open Loop Frequency Response

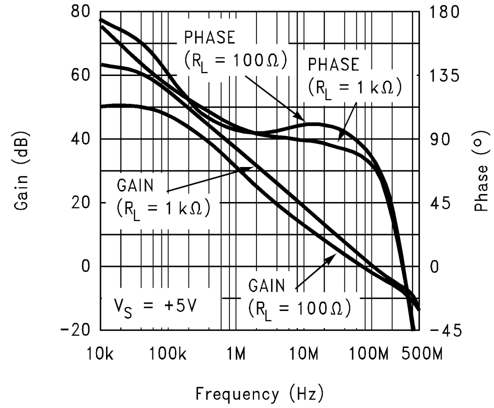


Figure 20. Open Loop Frequency Response

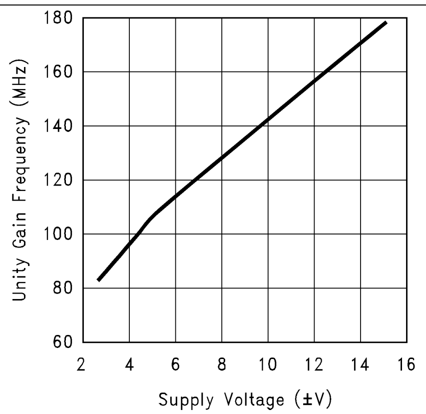


Figure 21. Unity Gain Frequency vs. Supply Voltage

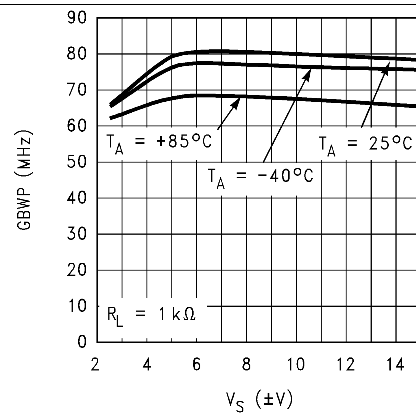


Figure 22. GBWP at 10 MHz vs. Supply Voltage

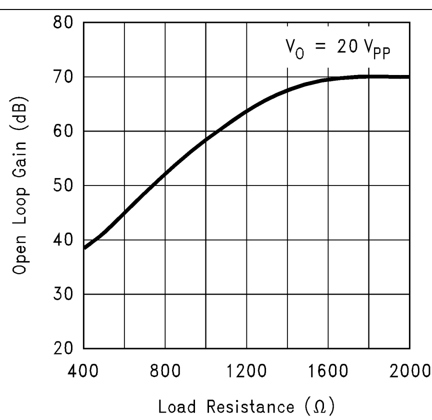


Figure 23. Large Signal Voltage Gain vs. Load, V_S = ±15 V

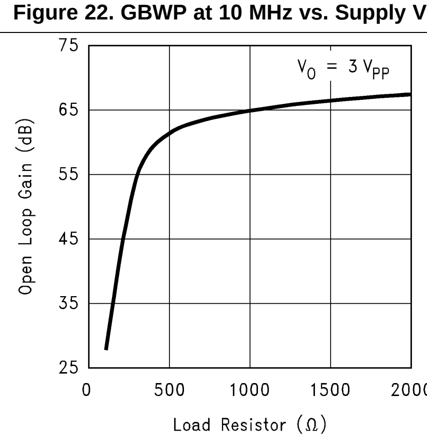


Figure 24. Large Signal Voltage Gain vs. Load, V_S = ±5 V

Typical Characteristics (continued)

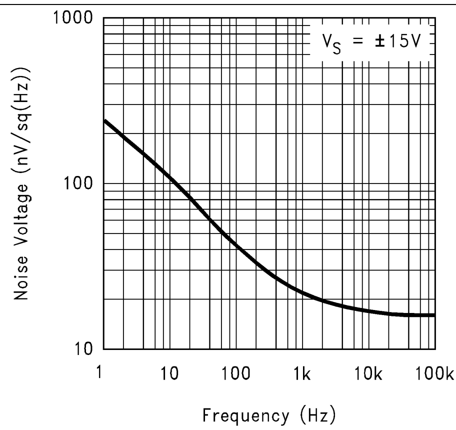


Figure 25. Input Voltage Noise vs. Frequency

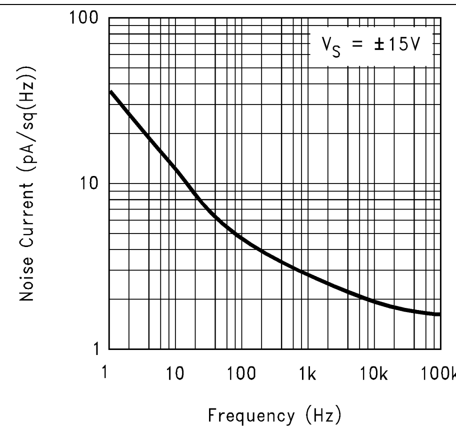


Figure 26. Input Current Noise vs. Frequency

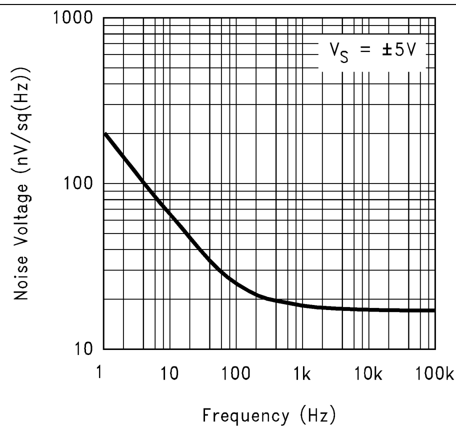


Figure 27. Input Voltage Noise vs. Frequency

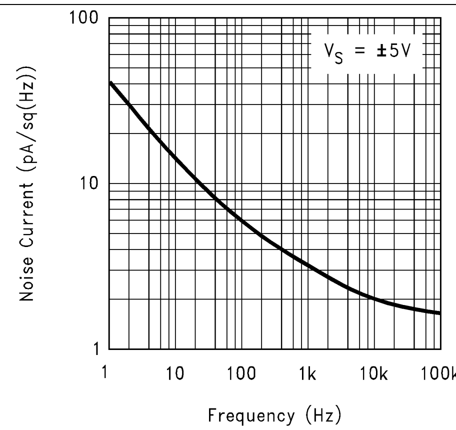


Figure 28. Input Current Noise vs. Frequency

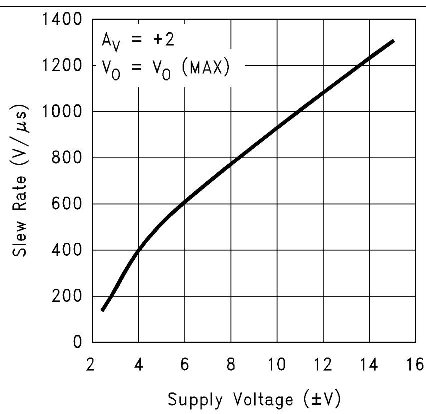


Figure 29. Slew Rate vs. Supply Voltage

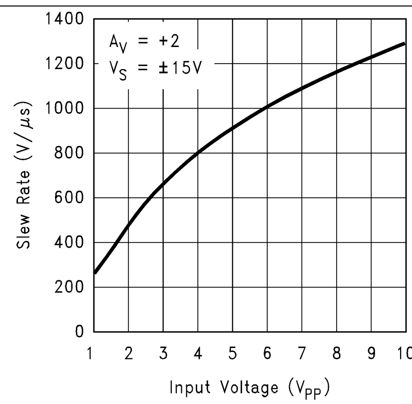


Figure 30. Slew Rate vs. Input Voltage

Typical Characteristics (continued)

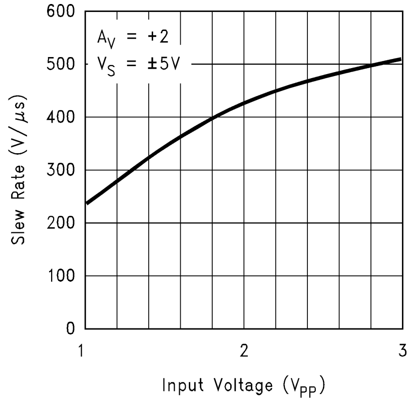


Figure 31. Slew Rate vs. Input Voltage

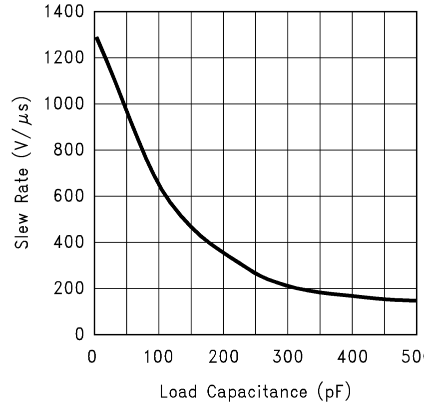


Figure 32. Slew Rate vs. Load Capacitance

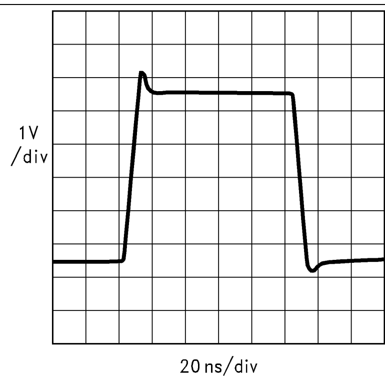


Figure 33. Large Signal Pulse Response, A_V = -1 V_S = ±15 V

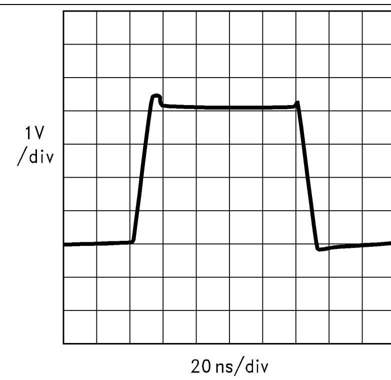


Figure 34. Large Signal Pulse Response, A_V = -1, V_S = ±5V

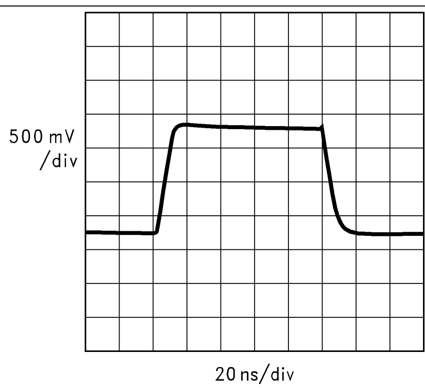


Figure 35. Large Signal Pulse Response, A_V = -1, V_S = +5 V

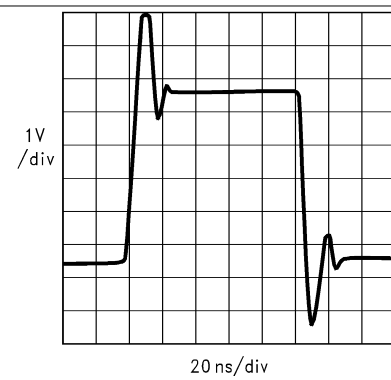


Figure 36. Large Signal Pulse Response, A_V = +1, V_S = ±15 V

Typical Characteristics (continued)

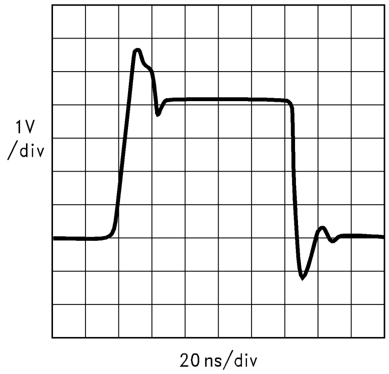


Figure 37. Large Signal Pulse Response, A_V = +1, V_S = ±5 V

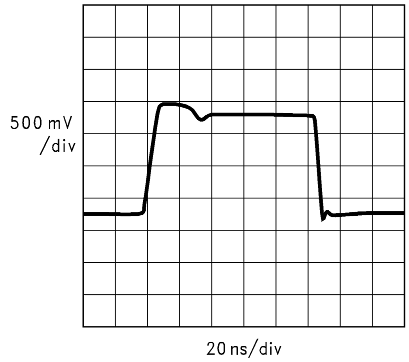


Figure 38. Large Signal Pulse Response, A_V = +1, V_S = +5 V

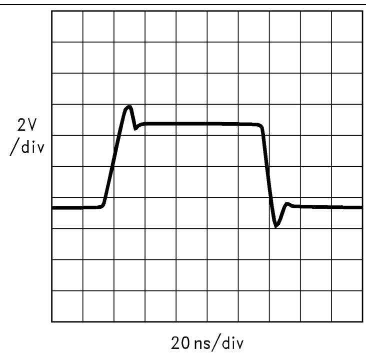


Figure 39. Large Signal Pulse Response, A_V = +2, V_S = ±15 V

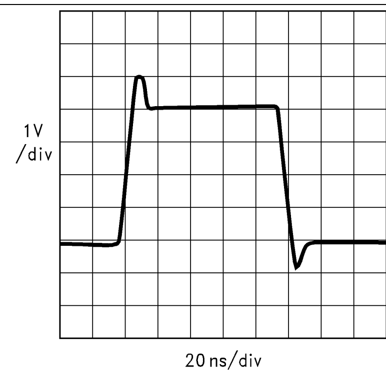


Figure 40. Large Signal Pulse Response, A_V= +2, V_S = ±5 V

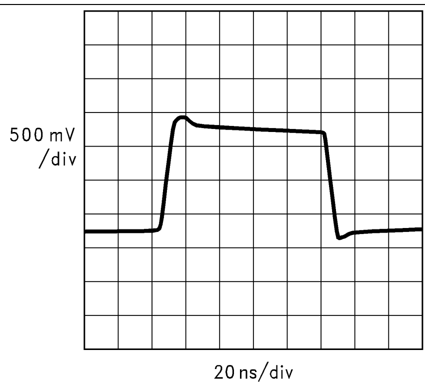


Figure 41. Large Signal Pulse Response, A_V = +2, V_S = +5 V

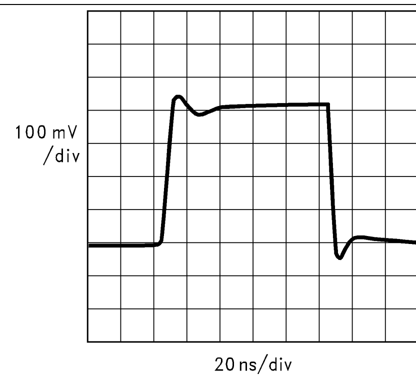


Figure 42. Small Signal Pulse Response, A_V = -1, V_S = ±15 V, R_L = 100 Ω

Typical Characteristics (continued)

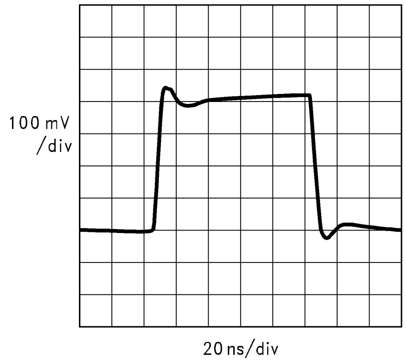


Figure 43. Small Signal Pulse Response, A_V = - 1, V_S = ±5 V, R_L= 100 Ω

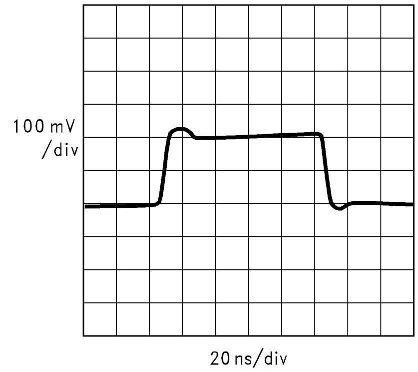


Figure 44. Small Signal Pulse Response, A_V = -1, V_S = +5 V, R_L = 100 Ω

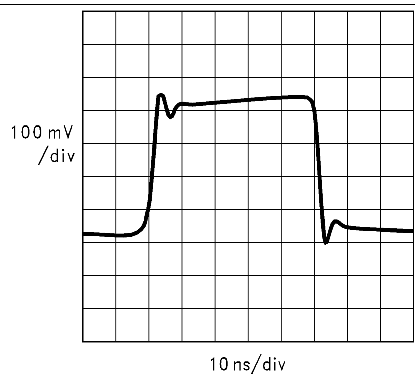


Figure 45. Small Signal Pulse Response, A_V = +1, V_S = ±15 V, R_L = 100 Ω

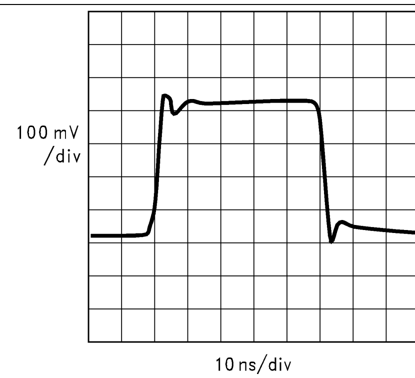


Figure 46. Small Signal Pulse Response, A_V = +1, V_S = ±5 V, R_L = 100 Ω

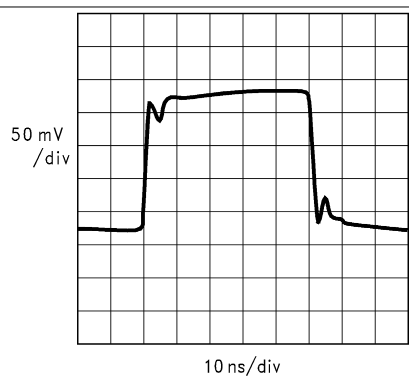


Figure 47. Small Signal Pulse Response, A_V = +1, V_S = +5 V, R_L = 100 Ω

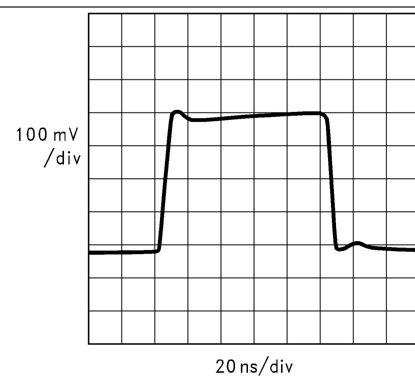


Figure 48. Small Signal Pulse Response, A_V = +2, V_S = ±15 V, R_L = 100 Ω

Typical Characteristics (continued)

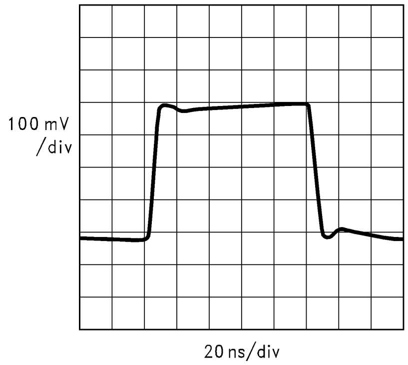


Figure 49. Small Signal Pulse Response, A_V = +2, V_S = ±5 V, R_L = 100 Ω

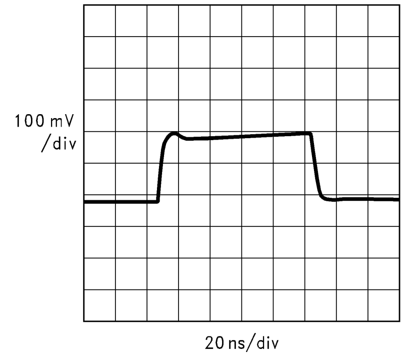


Figure 50. Small Signal Pulse Response, A_V = +2, V_S = +5 V, R_L = 100 Ω

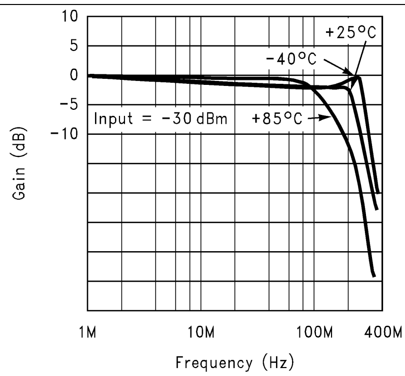


Figure 51. Closed Loop Frequency Response vs. Temperature, V_S = ±15 V, A_V = +1, R_L = 100 Ω

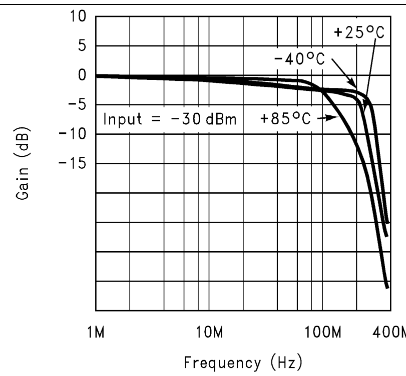


Figure 52. Closed Loop Frequency Response vs. Temperature V_S = ±5 V, A_V = +1, R_L = 100 Ω

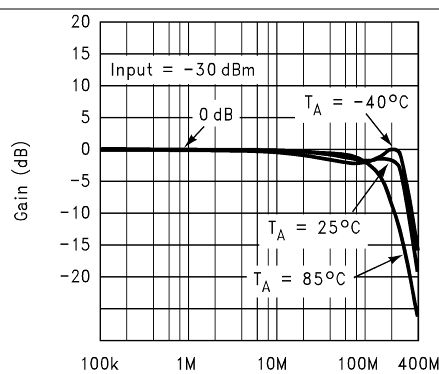


Figure 53. Closed Loop Frequency Response vs. Temperature, V_S = +5 V, A_V = +1, R_L= 100 Ω

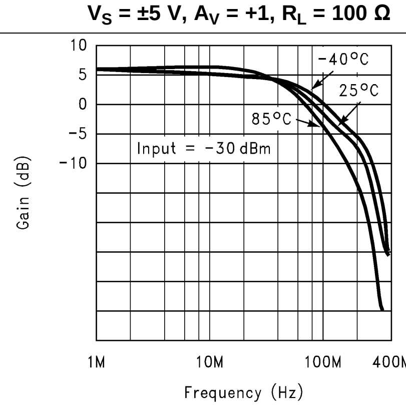


Figure 54. Closed Loop Frequency Response vs. Temperature, V_S = ±15 V, A_V = +2, R_L= 100 Ω

Typical Characteristics (continued)

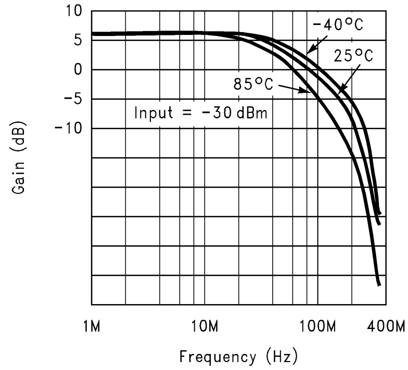


Figure 55. Closed Loop Frequncy Response vs. Temperature, V_S = ±5 V, A_V = +2 , R_L = 100 Ω

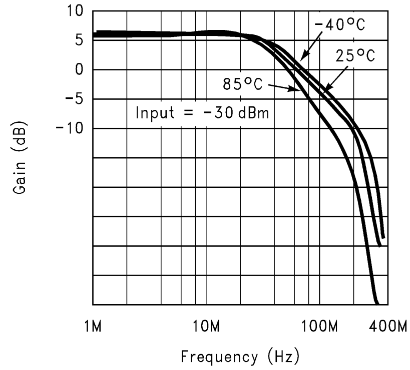


Figure 56. Closed Loop Frequency Response vs. Temperature, V_S = +5 V, A_V = +2, R_L = 100 Ω

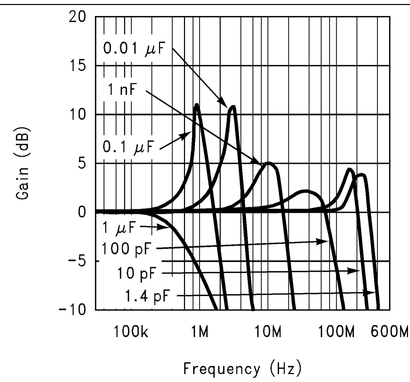


Figure 57. Closed Loop Frequency Response vs. Capacitance Load (A_V = +1, V_S = ±15 V)

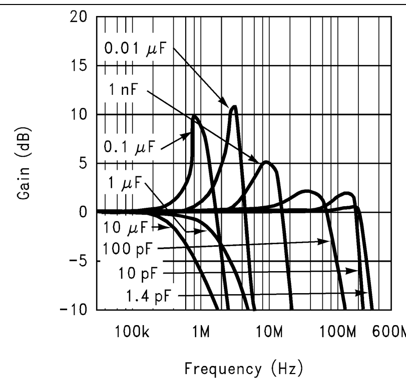


Figure 58. Closed Loop Frequency Response vs. Capacitive Load (A_V = +1, V_S = ±5 V)

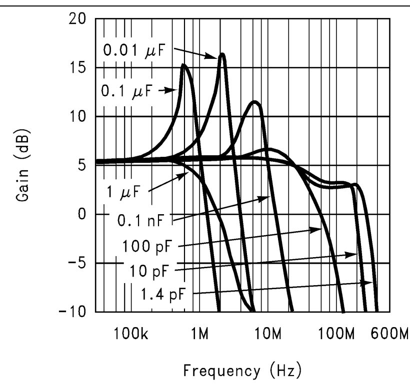


Figure 59. Closed Loop Frequency Response vs. Capacitive Load (A_V = +2, V_S = ±15 V)

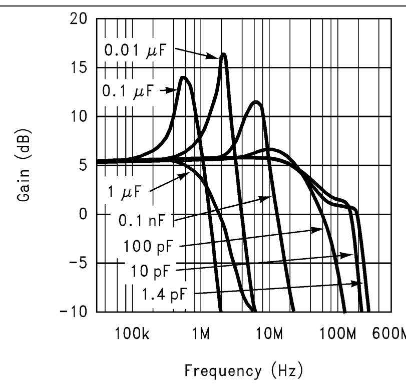


Figure 60. Closed Loop Frequency Response vs. Capacitive Load (A_V = +2, V_S = ±5 V)

Typical Characteristics (continued)

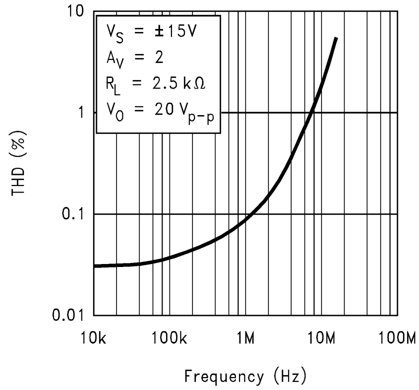


Figure 61. Total Harmonic Distortion vs. Frequency

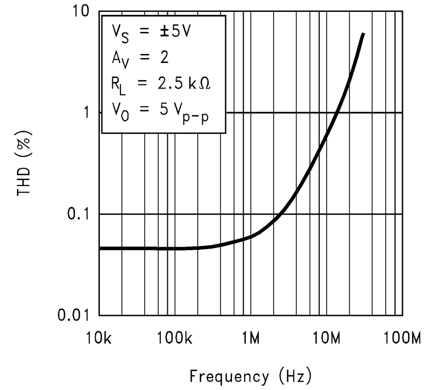


Figure 62. Total Harmonic Distortion vs. Frequency

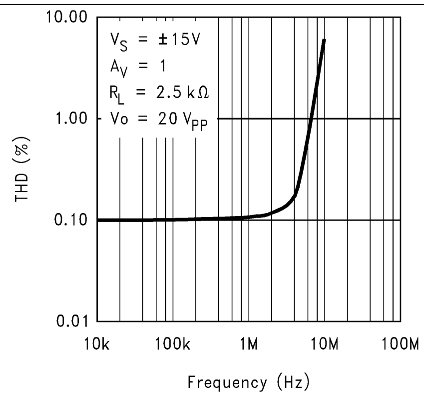


Figure 63. Total Harmonic Distortion vs. Frequency

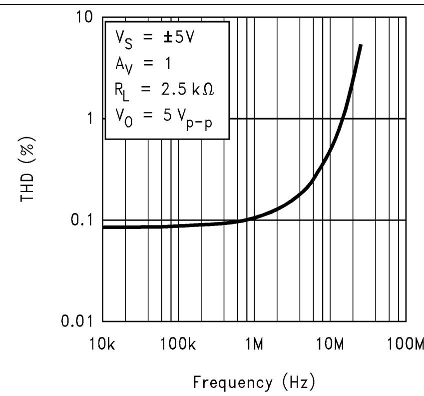


Figure 64. Total Harmonic Distortion vs. Frequency

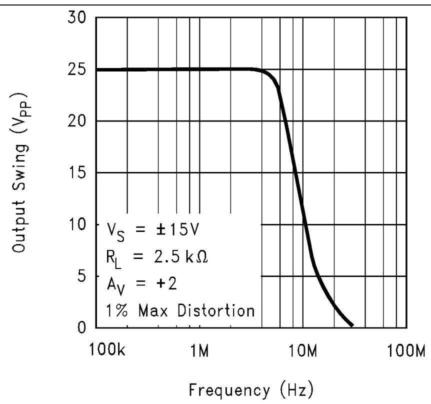


Figure 65. Undistorted Output Swing vs. Frequency

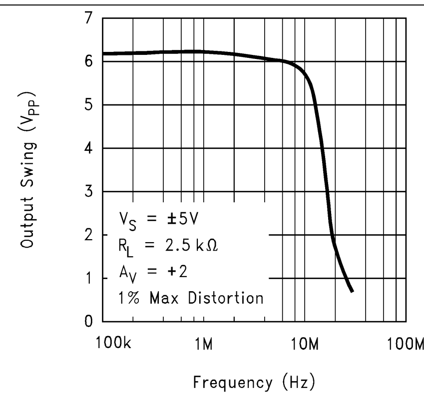


Figure 66. Undistorted Output Swing vs. Frequency

Typical Characteristics (continued)

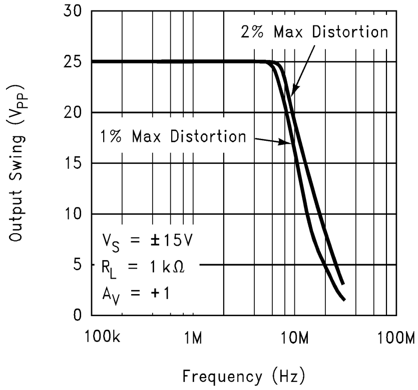


Figure 67. Undistorted Output Swing vs. Frequency

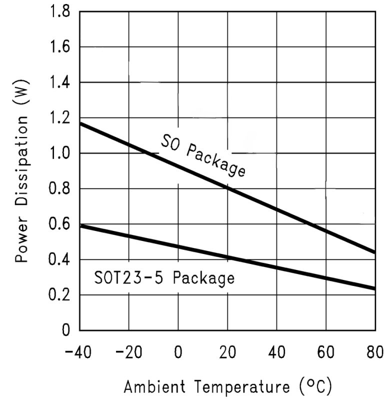


Figure 68. Total Power Dissipation vs. Ambient Temperature

7 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

Table 1 depicts the maximum operating supply voltage for each package type

Table 1. Maximum Supply Voltage Values

	SOT-23	SO-8
Single Supply	10 V	30 V
Dual Supplies	±5 V	±15 V

Stable unity gain operation is possible with supply voltage of 5 V for all capacitive loads. This allows the possibility of using the device in portable applications with low supply voltages with minimum components around it.

Above a supply voltage of 6 V (±3 V Dual supplies), an additional resistor and capacitor (shown in Figure 69) should be placed in the feedback path to achieve stability at unity gain over the full temperature range.

The package power dissipation should be taken into account when operating at high ambient temperatures and/or high power dissipative conditions. Refer to the power derating curves in the data sheet for each type of package.

In determining maximum operable temperature of the device, make sure the total power dissipation of the device is considered; this includes the power dissipated in the device with a load connected to the output as well as the nominal dissipation of the op amp.

The device is capable of tolerating momentary short circuits from its output to ground but prolonged operation in this mode will damage the device, if the maximum allowed junction temperation is exceeded.

7.2 Typical Applications

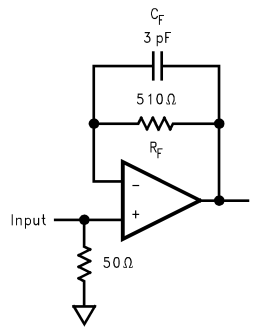


Figure 69. Typical Circuit for A_V = +1 Operation (V_S = 6 V)

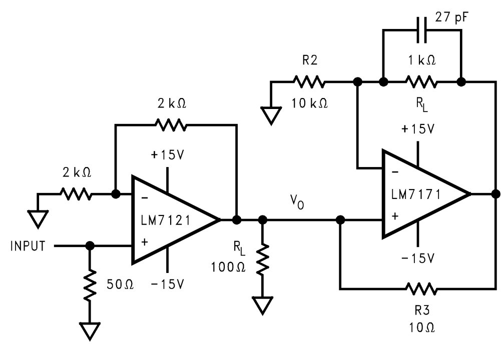


Figure 70. Simple Circuit to Improve Linearity and Output Drive Current

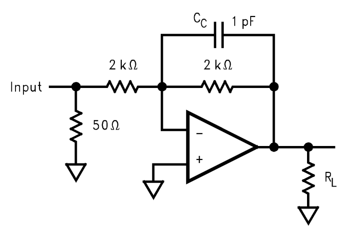
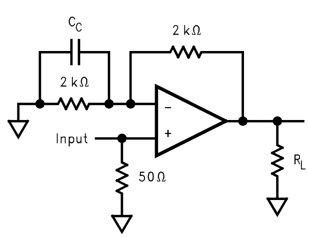


Figure 71. A_V = -1



C_C = 2 pF for R_L = 100 Ω
C_C = Open for R_L = Open

Figure 72. A_V = +2

Typical Applications (continued)

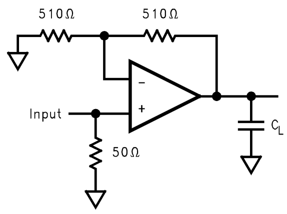
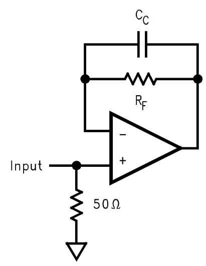


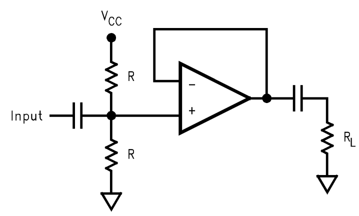
Figure 73. A_V = +2, Capacitive Load



R_F = 0 Ω, C_C = Open for V_S < 6 V

R_F = 510 Ω, C_C = 3 pF for $V_S \geq$ 6 V

Figure 74. A_V = +1



R_F = 0 Ω, C_C = Open for V_S < 6 V

R_F = 510 Ω, C_C = 3 pF for $V_S \geq$ 6 V

Figure 75. A_V = +1. V_S = +5 V, Single Supply Operation

7.2.1 Design Requirements

7.2.1.1 Current Boost Circuit

The circuit in Figure 70 can be used to achieve good linearity along with high output current capability.

By proper choice of R_3, the LM7121 output can be set to supply a minimal amount of current, thereby improving its output linearity.

R_3 can be adjusted to allow for different loads:

$$R_3 = 0.1\ R_L \quad (1)$$

Figure 70 has been set for a load of 100 Ω. Reasonable speeds (< 30 ns rise and fall times) can be expected up to 120 mApp of load current (see Figure 77 for step response across the load).

Typical Applications (continued)

7.2.2 Detailed Design Procedure

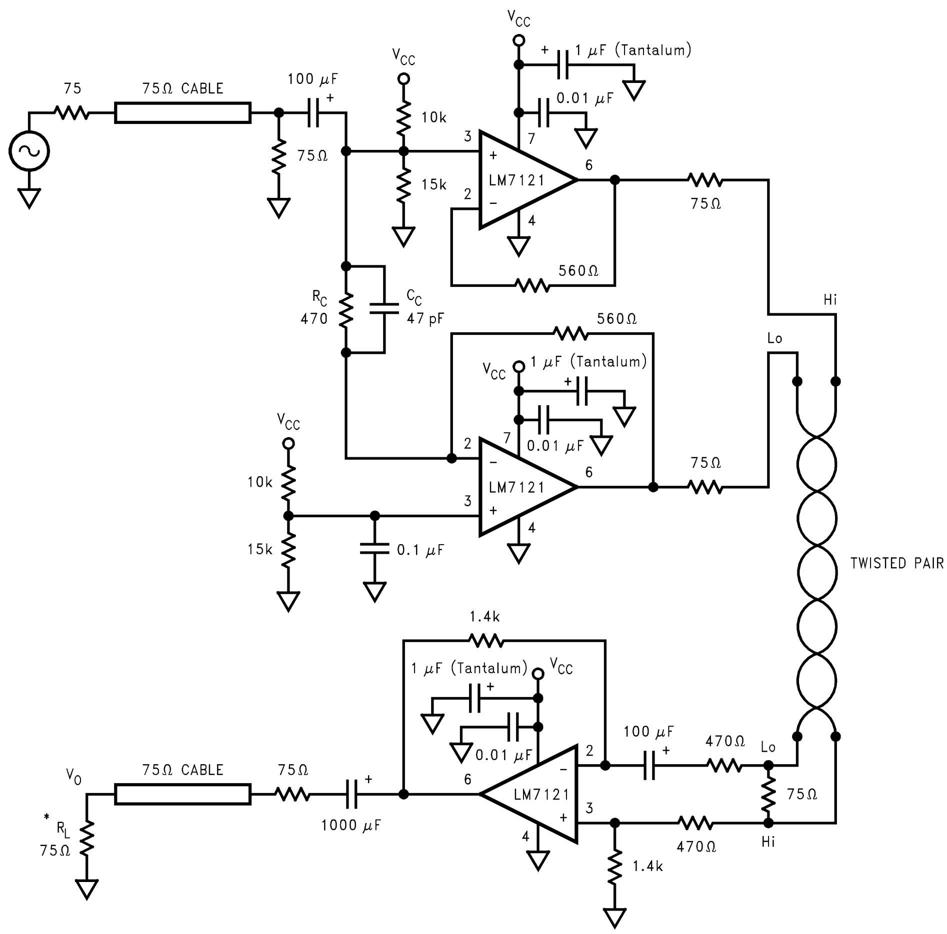
It is very important to keep the lead lengths to a minimum and to provide a low impedance current path by using a ground-plane on the board.

CAUTION

If R_L is removed, the current balance at the output of LM7121 would be disturbed and it would have to supply the full amount of load current. This might damage the part if power dissipation limit is exceeded.

7.2.2.1 Color Video on Twisted Pairs Using Single Supply

The circuit shown in Figure 76 can be used to drive in excess of 25 meters length of twisted pair cable with no loss of resolution or picture definition when driving a NTSC monitor at the load end.



Pin numbers shown are for SO-8 package.

* Input termination of NTSC monitor.

Figure 76. Single Supply Differential Twister Pair Cable Transmitter/Receiver, 8.5 V ≤ V_{CC} ≤ 30 V

Typical Applications (continued)

Differential Gain and Differential Phase errors measured at the load are less than 1% and 1˚ respectively

R_G and C_C can be adjusted for various cable lengths to compensate for the line losses and for proper response at the output. Values shown correspond to a twisted pair cable length of 25 meters with about 3 turns/inch (see Figure 78 for step response).

The supply voltage can vary from 8.5 V up to 30 V with the output rise and fall times under 12 ns. With the component values shown, the overall gain from the input to the output is about 1.

Even though the transmission line is not terminated in its nominal characteristic impedance of about 600 Ω, the resulting reflection at the load is only about 5% of the total signal and in most cases can be neglected. Using 75 termination instead, has the advantage of operating at a low impedance and results in a higher realizable bandwidth and signal fidelity.

7.2.3 Application Performance Plots

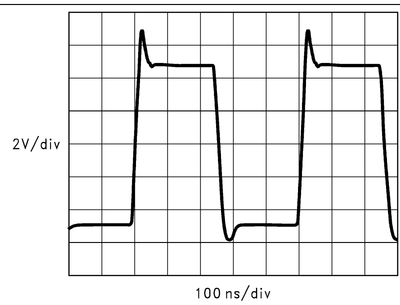


Figure 77. Waveform across a 100-Ω Load

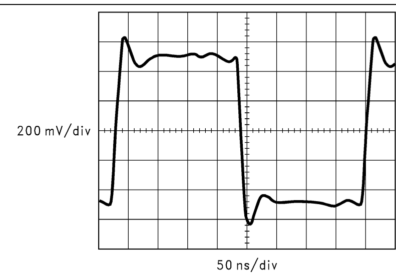


Figure 78. Step Response to a 1 V_{PP} Input Signal Measured across the 75-Ω Load

8 Device and Documentation Support

8.1 Trademarks

All trademarks are the property of their respective owners.

8.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

8.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM7121IM/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM71 21IM
LM7121IM/NOPB.B	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM71 21IM
LM7121IM5/NOPB	Active	Production	SOT-23 (DBV) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A03A
LM7121IM5/NOPB.B	Active	Production	SOT-23 (DBV) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A03A
LM7121IM5X/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A03A
LM7121IM5X/NOPB.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A03A
LM7121IMX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM71 21IM
LM7121IMX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM71 21IM

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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