



# LM6152/LM6154 Dual and Quad 75 MHz GBW Rail-to-Rail I/O Operational Amplifiers

## 1 Features

- At  $V_S = 5V$ , typical unless noted.
- Greater than Rail-to-rail Input CMVR  $-0.25V$  to  $5.25V$
- Rail-to-rail Output Swing  $0.01V$  to  $4.99V$
- Wide Gain-bandwidth  $75MHz @ 100kHz$
- Slew Rate
  - Small Signal  $5V/\mu s$
  - Large Signal  $45V/\mu s$
- Low Supply Current  $1.4mA/amplifier$
- Wide Supply Range  $2.7V$  to  $24V$
- Fast Settling Time of  $1.1\mu s$  for  $2V$  Step (to  $0.01\%$ )
- PSRR  $91dB$
- CMRR  $84dB$

## 2 Applications

- Portable High Speed Instrumentation
- Signal Conditioning Amplifier/ADC Buffers
- Barcode Scanners

## 3 Description

Using patented circuit topologies, the LM6152/LM6154 provides new levels of speed vs. power performance in applications where low voltage supplies or power limitations previously made compromise necessary. With only  $1.4mA/amplifier$  supply current, the  $75MHz$  gain bandwidth of this device supports new portable applications where higher power devices unacceptably drain battery life. The slew rate of the devices increases with increasing input differential voltage, thus allowing the device to handle capacitive loads while maintaining large signal amplitude.

The LM6152/LM6154 can be driven by voltages that exceed both power supply rails, thus eliminating concerns about exceeding the common-mode voltage range. The rail-to-rail output swing capability provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

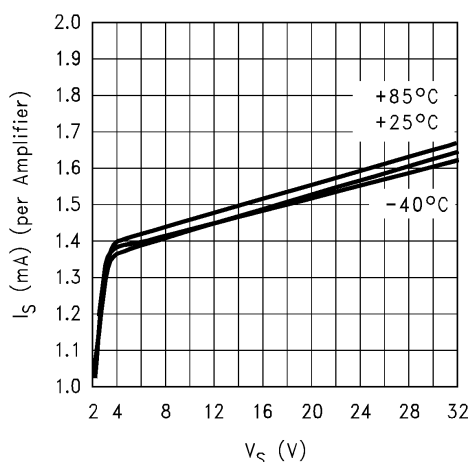
Operating on supplies from  $2.7V$  to over  $24V$ , the LM6152/LM6154 is excellent for a very wide range of applications, from battery operated systems with large bandwidth requirements to high speed instrumentation.

### Device Information<sup>(1)</sup>

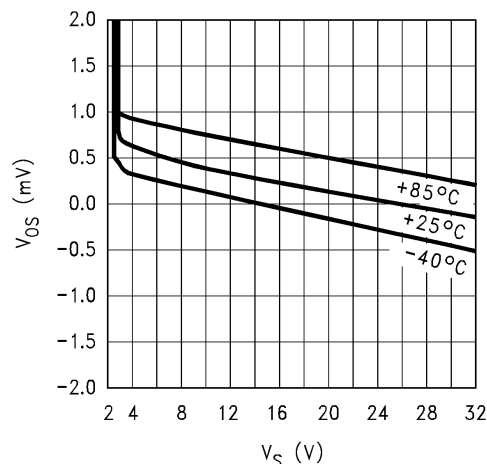
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM6152	SOIC (8)	4.902 mm × 3.912 mm
LM6154	SOIC (14)	8.636 mm × 3.912 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

**Supply Current vs. Supply Voltage**



**Offset Voltage vs. Supply voltage**



## Table of Contents

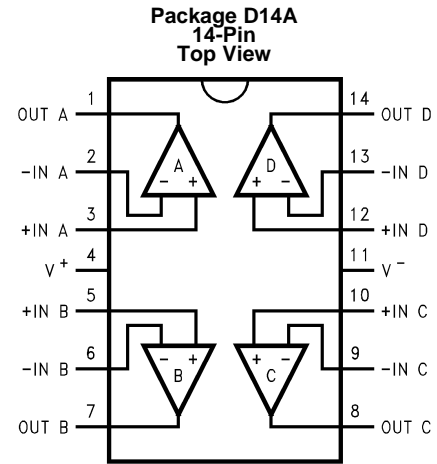
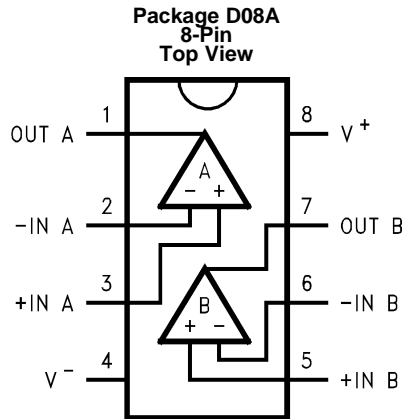
<b>1 Features</b> .....	<b>1</b>	6.7 2.7 V DC Electrical Characteristics .....	<b>7</b>
<b>2 Applications</b> .....	<b>1</b>	6.8 2.7 V AC Electrical Characteristics .....	<b>7</b>
<b>3 Description</b> .....	<b>1</b>	6.9 24 V DC Electrical Characteristics .....	<b>8</b>
<b>4 Revision History</b> .....	<b>2</b>	6.10 24 V AC Electrical Characteristics .....	<b>8</b>
<b>5 Pin Configuration and Functions</b> .....	<b>3</b>	6.11 Typical Performance Characteristics .....	<b>9</b>
<b>6 Specifications</b> .....	<b>4</b>	<b>7 Application and Implementation</b> .....	<b>14</b>
6.1 Absolute Maximum Ratings .....	4	<b>8 Device and Documentation Support</b> .....	<b>16</b>
6.2 Handling Ratings .....	4	8.1 Related Links .....	16
6.3 Recommended Operating Conditions <sup>(1)</sup> .....	4	8.2 Trademarks .....	16
6.4 Thermal Information .....	4	8.3 Electrostatic Discharge Caution .....	16
6.5 5.0 V DC Electrical Characteristics .....	5	8.4 Glossary .....	16
6.6 5.0 V AC Electrical Characteristics .....	6	<b>9 Mechanical, Packaging, and Orderable Information</b> .....	<b>16</b>

## 4 Revision History

Changes from Revision D (March 2013) to Revision E	Page
<ul style="list-style-type: none"> <li>Changed "Junction Temperature Range" to "Operating Temperature Range" and deleted "T<sub>J</sub>" in Recommended Operating Conditions .....</li> </ul>	<b>4</b>
<ul style="list-style-type: none"> <li>Deleted T<sub>J</sub> = 25°C for Electrical Characteristics Tables .....</li> </ul>	<b>5</b>

Changes from Revision C (March 2013) to Revision D	Page
<ul style="list-style-type: none"> <li>Changed layout of National Data Sheet to TI format .....</li> </ul>	<b>15</b>

## 5 Pin Configuration and Functions



### Pin Functions

NAME	PIN		I/O	DESCRIPTION
	LM6152 D08A	LM6154 D14A		
-IN A	2	2	I	ChA Inverting Input
+IN A	3	3	I	ChA Non-inverting Input
-IN B	6	6	I	ChB Inverting Input
+IN B	5	5	I	ChB Non-inverting Input
-IN C		9	I	ChC Inverting Input
+IN C		10	I	ChC Non-inverting Input
-IN D		13	I	ChD Inverting Input
+IN D		12	I	ChD Non-inverting Input
OUT A	1	1	O	ChA Output
OUT B	7	7	O	ChB Output
OUT C		8	O	ChC Output
OUT D		14	O	ChD Output
V-	4	11	I	Negative Supply
V+	8	4	I	Positive Supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings<sup>(1)(2)</sup>

	MIN	MAX	UNIT
Differential Input Voltage		±15	V
Voltage at Input/Output Pin		(V <sup>+</sup> ) + 0.3 (V <sup>-</sup> ) - 0.3	V
Supply Voltage (V <sup>+</sup> - V <sup>-</sup> )		35	V
Current at Input Pin		±10	mA
Current at Output Pin <sup>(3)</sup>		±25	mA
Current at Power Supply Pin		50	mA
Lead Temperature (soldering, 10 sec)		260	°C
Junction Temperature <sup>(4)</sup>		150	°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
- (4) The maximum power dissipation is a function of T<sub>J(MAX)</sub>, R<sub>θJA</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any ambient temperature is P<sub>D</sub> = (T<sub>J(MAX)</sub> - T<sub>A</sub>) / R<sub>θJA</sub>. All numbers apply for packages soldered directly into a PC board.

### 6.2 Handling Ratings

	MIN	MAX	UNIT
T <sub>stg</sub> Storage temperature range	-65	+150	°C
V <sub>(ESD)</sub> Electrostatic discharge Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>		2500	V

- (1) JEDEC document JEP155 states that 2500-V HBM allows safe manufacturing with a standard ESD control process. Human body model is 1.5 kΩ in series with 100 pF

### 6.3 Recommended Operating Conditions<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply Voltage		2.7 ≤ V <sup>+</sup> ≤ 24	V
Operating Temperature Range, LM6152, LM6154	0	+70	°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	D08A	D14A	UNIT
	8 PINS	14 PINS	
R <sub>θJA</sub> Junction-to-ambient thermal resistance	193°C/W	126°C/W	°C/W

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 5.0 V DC Electrical Characteristics

Unless otherwise specified, all limits are ensured for  $V^+ = 5.0V$ ,  $V^- = 0V$ ,  $V_{CM} = V_O = V^+/2$  and  $R_L > 1\text{ M}\Omega$  to  $V^+/2$ . **Boldface** limits apply at the temperature extremes.

PARAMETER	TEST CONDITIONS	TYP <sup>(1)</sup>	LM6152AC LIMIT <sup>(2)</sup>	LM6154BC LM6152BC LIMIT <sup>(2)</sup>	UNIT
$V_{OS}$ Input Offset Voltage		0.54	2 4	5 7	mV max
$TCV_{OS}$ Input Offset Voltage Average Drift		10			$\mu V/^{\circ}C$
$I_B$ Input Bias Current	$0V \leq V_{CM} \leq 5V$	500 750	980 1500	980 1500	nA max
$I_{OS}$ Input Offset Current		32 40	100 160	100 160	nA max
$R_{IN}$ Input Resistance, CM	$0V \leq V_{CM} \leq 4V$	30			M $\Omega$
$CMRR$ Common Mode Rejection Ratio	$0V \leq V_{CM} \leq 4V$	94	70	70	dB min
	$0V \leq V_{CM} \leq 5V$	84	60	60	
$PSRR$ Power Supply Rejection Ratio	$5V \leq V^+ \leq 24V$	91	80	80	dB min
$V_{CM}$ Input Common-Mode Voltage Range	Low	-0.25	0	0	V
	High	5.25	5.0	5.0	V
$A_V$ Large Signal Voltage Gain	$R_L = 10\text{ k}\Omega$	214	50	50	V/mV min
$V_O$ Output Swing	$R_L = 100\text{ k}\Omega$	0.006	0.02 0.03	0.02 0.03	V max
		4.992	4.97 4.96	4.97 4.96	V min
	$R_L = 2\text{ k}\Omega$	0.04	0.10 0.12	0.10 0.12	V max
		4.89	4.80 4.70	4.80 4.70	V min
$I_{SC}$ Output Short Circuit Current	Sourcing	6.2	3 2.5	3 2.5	mA min
			27 17	27 17	mA max
	Sinking	16.9	7 5	7 5	mA min
			40	40	mA max
$I_S$ Supply Current	Per Amplifier	1.4	2 2.25	2 2.25	mA max

(1) Typical Values represent the most likely parametric norm.

(2) All limits are specified by testing or statistical analysis.

**LM6152, LM6154**

SNOS752E –MAY 1999–REVISED SEPTEMBER 2014

[www.ti.com](http://www.ti.com)
**6.6 5.0 V AC Electrical Characteristics**

Unless otherwise specified, all limits ensured for  $V^+ = 5.0V$ ,  $V^- = 0V$ ,  $V_{CM} = V_O = V^+/2$  and  $R_L > 1\text{ M}\Omega$  to  $V^+/2$ . **Boldface** limits apply at the temperature extremes.

PARAMETER		TEST CONDITIONS	TYP <sup>(1)</sup>	LM6152AC LIMIT <sup>(2)</sup>	LM6154BC LM6152BC LIMIT <sup>(2)</sup>	UNIT
SR	Slew Rate	$\pm 4V$ Step @ $V_S = \pm 6V$ , $R_S < 1\text{ k}\Omega$	30	24 <b>15</b>	24 <b>15</b>	V/ $\mu$ s min
GBW	Gain-Bandwidth Product	$f = 100\text{ kHz}$	75			MHz
	Amp-to-Amp Isolation	$R_L = 10\text{ k}\Omega$	125			dB
$e_n$	Input-Referred Voltage Noise	$f = 1\text{ kHz}$	9			nV/ $\sqrt{\text{Hz}}$
$i_n$	Input-Referred Current Noise	$f = 1\text{ kHz}$	0.34			pA/ $\sqrt{\text{Hz}}$
T.H.D	Total Harmonic Distortion	$f = 100\text{ kHz}$ , $R_L = 10\text{ k}\Omega$ $A_V = -1$ , $V_O = 2.5\text{ V}_{PP}$	-65			dBc
ts	Settling Time	2V Step to 0.01%	1.1			$\mu$ s

(1) Typical Values represent the most likely parametric norm.

(2) All limits are specified by testing or statistical analysis.

## 6.7 2.7 V DC Electrical Characteristics

Unless otherwise specified, all limits are ensured for  $V^+ = 2.7V$ ,  $V^- = 0V$ ,  $V_{CM} = V_O = V^+/2$  and  $R_L > 1\text{ M}\Omega$  to  $V^+/2$ . **Boldface** limits apply at the temperature extremes.

PARAMETER	TEST CONDITIONS	TYP <sup>(1)</sup>	LM6152AC LIMIT <sup>(2)</sup>	LM6154BC LM6152BC LIMIT <sup>(2)</sup>	UNIT
$V_{OS}$ Input Offset Voltage		0.8	2 5	5 8	mV max
$TCV_{OS}$ Input Offset Voltage Average Drift		10			$\mu V/^{\circ}C$
$I_B$ Input Bias Current		500			nA
$I_{OS}$ Input Offset Current		50			nA
$R_{IN}$ Input Resistance, CM	$0V \leq V_{CM} \leq 1.8V$	30			M $\Omega$
$CMRR$ Common Mode Rejection Ratio	$0V \leq V_{CM} \leq 1.8V$	88			dB
	$0V \leq V_{CM} \leq 2.7V$	78			
$PSRR$ Power Supply Rejection Ratio	$3V \leq V^+ \leq 5V$	69			dB
$V_{CM}$ Input Common-Mode Voltage Range	Low	-0.25	0	0	V
	High	2.95	2.7	2.7	V
$A_V$ Large Signal Voltage Gain	$R_L = 10\text{ k}\Omega$	5.5			V/mV
$V_O$ Output Swing	$R_L = 10\text{ k}\Omega$	0.032	0.07 0.11	0.07 0.11	V max
		2.68	2.64 2.62	2.64 2.62	V min
$I_S$ Supply Current	Per Amplifier	1.35			mA

(1) Typical Values represent the most likely parametric norm.

(2) All limits are specified by testing or statistical analysis.

## 6.8 2.7 V AC Electrical Characteristics

Unless otherwise specified, all limits are ensured for  $V^+ = 2.7V$ ,  $V^- = 0V$ ,  $V_{CM} = V_O = V^+/2$  and  $R_L > 1\text{ M}\Omega$  to  $V^+/2$ . **Boldface** limits apply at the temperature extremes.

PARAMETER	TEST CONDITIONS	TYP <sup>(1)</sup>	LM6152AC LIMIT <sup>(2)</sup>	LM6154BC LM6152BC LIMIT <sup>(2)</sup>	UNIT
GBW Gain-Bandwidth Product	$f = 100\text{ kHz}$	80			MHz

(1) Typical Values represent the most likely parametric norm.

(2) All limits are specified by testing or statistical analysis.

## LM6152, LM6154

SNOS752E –MAY 1999–REVISED SEPTEMBER 2014

www.ti.com

### 6.9 24 V DC Electrical Characteristics

Unless otherwise specified, all limits are ensured for  $V^+ = 24V$ ,  $V^- = 0V$ ,  $V_{CM} = V_O = V^+/2$  and  $R_L > 1\text{ M}\Omega$  to  $V^+/2$ . **Boldface** limits apply at the temperature extremes.

PARAMETER	TEST CONDITIONS	TYP <sup>(1)</sup>	LM6152AC LIMIT <sup>(2)</sup>	LM6154BC LM6152BC LIMIT <sup>(2)</sup>	UNIT
$V_{OS}$ Input Offset Voltage		0.3	2 4	7 9	mV max
$TCV_{OS}$ Input Offset Voltage Average Drift		10			$\mu V/^{\circ}C$
$I_B$ Input Bias Current		500			nA
$I_{OS}$ Input Offset Current		32			nA
$R_{IN}$ Input Resistance, CM	$0V \leq V_{CM} \leq 23V$	60			Meg $\Omega$
$CMRR$ Common Mode Rejection Ratio	$0V \leq V_{CM} \leq 23V$	94			dB
	$0V \leq V_{CM} \leq 24V$	84			
$PSRR$ Power Supply Rejection Ratio	$0V \leq V_{CM} \leq 24V$	95			dB
$V_{CM}$ Input Common-Mode Voltage Range	Low	-0.25	0	0	V
	High	24.25	24	24	V
$A_V$ Large Signal Voltage Gain	$R_L = 10\text{ k}\Omega$	55			V/mV
$V_O$ Output Swing	$R_L = 10\text{ k}\Omega$	0.044	0.075 0.090	0.075 0.090	V max
		23.91	23.8 23.7	23.8 23.7	V min
$I_S$ Supply Current	Per Amplifier	1.6	2.25 2.50	2.25 2.50	mA max

(1) Typical Values represent the most likely parametric norm.

(2) All limits are specified by testing or statistical analysis.

### 6.10 24 V AC Electrical Characteristics

Unless otherwise specified, all limits are ensured for  $V^+ = 24V$ ,  $V^- = 0V$ ,  $V_{CM} = V_O = V^+/2$  and  $R_L > 1\text{ M}\Omega$  to  $V^+/2$ . **Boldface** limits apply at the temperature extremes.

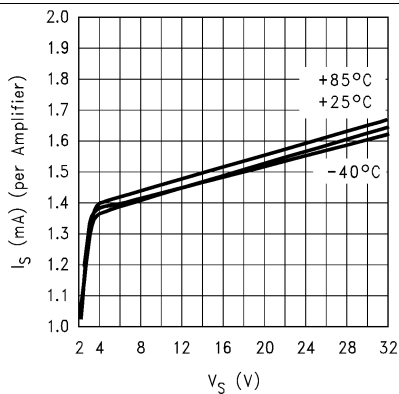
PARAMETER	TEST CONDITIONS	TYP <sup>(1)</sup>	LM6152AC LIMIT <sup>(2)</sup>	LM6154BC LM6152BC LIMIT <sup>(2)</sup>	UNIT
GBW Gain-Bandwidth Product	$f = 100\text{ kHz}$	80			MHz

(1) Typical Values represent the most likely parametric norm.

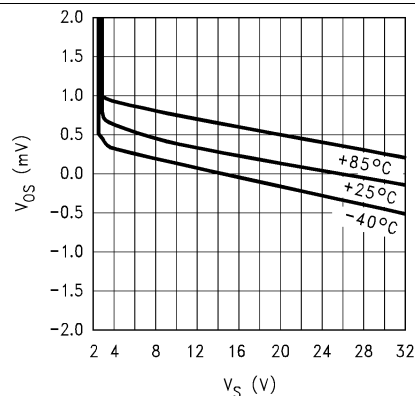
(2) All limits are specified by testing or statistical analysis.



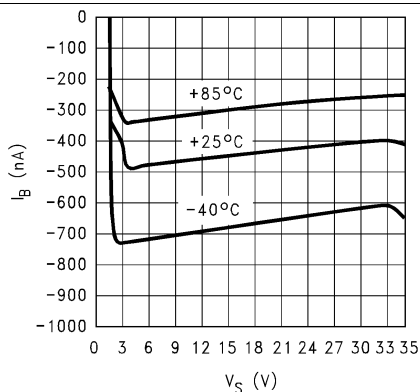
## 6.11 Typical Performance Characteristics



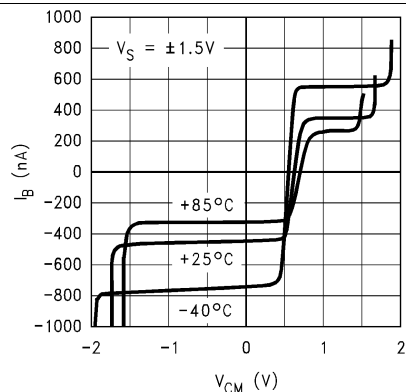
**Figure 1. Supply Current vs. Supply Voltage**



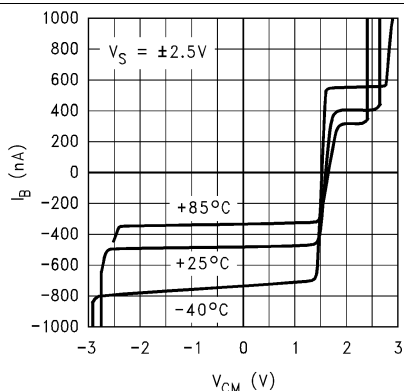
**Figure 2. Offset Voltage vs. Supply Voltage**



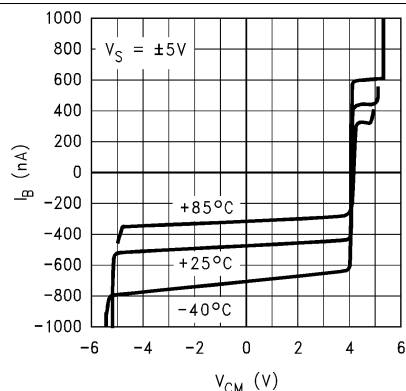
**Figure 3. Bias Current vs. Supply Voltage**



**Figure 4. Bias Current vs.  $V_{CM}$**



**Figure 5. Bias Current vs.  $V_{CM}$**



**Figure 6. Bias Current vs.  $V_{CM}$**

## Typical Performance Characteristics (continued)

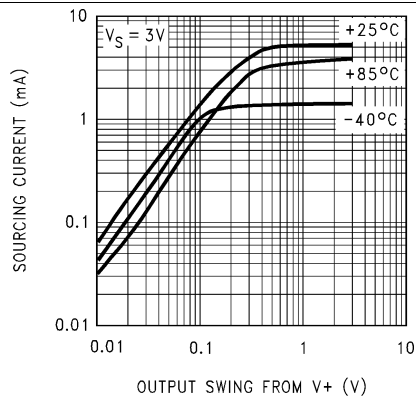


Figure 7. Output Voltage vs. Source Current

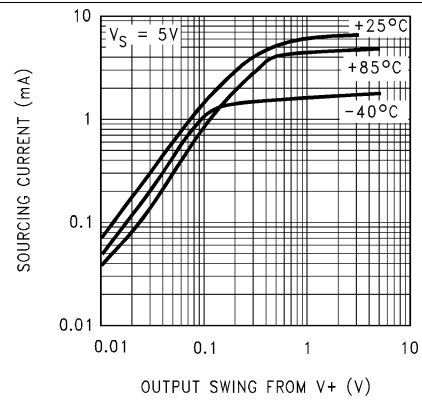


Figure 8. Output Voltage vs. Source Current

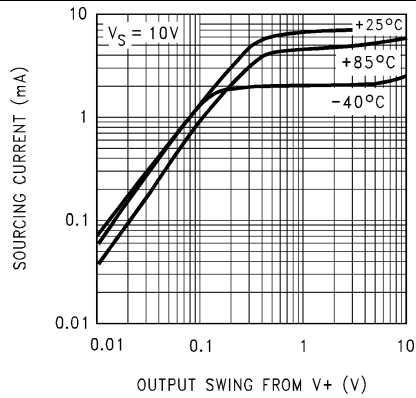


Figure 9. Output Voltage vs. Source Current

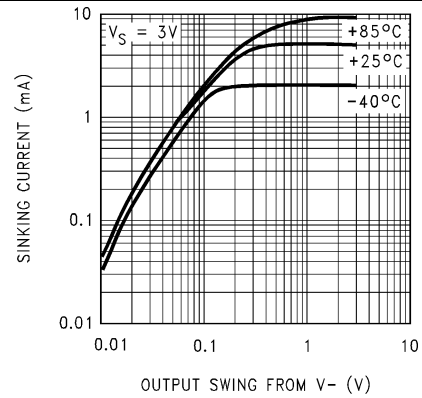


Figure 10. Output Voltage vs. Sink Current

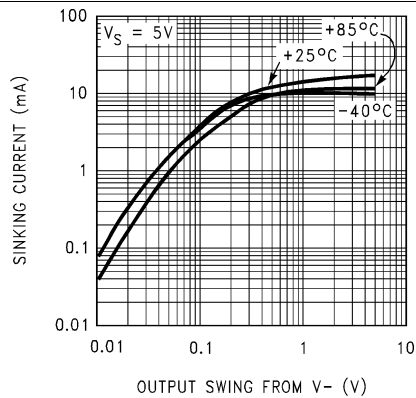


Figure 11. Output Voltage vs. Sink Current

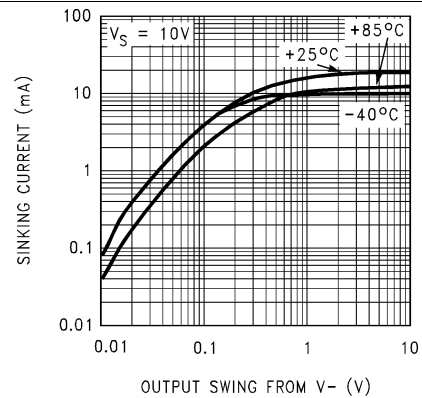
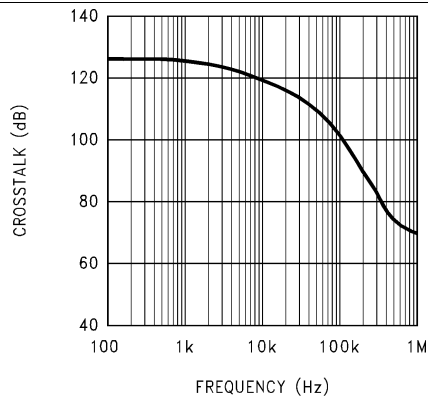
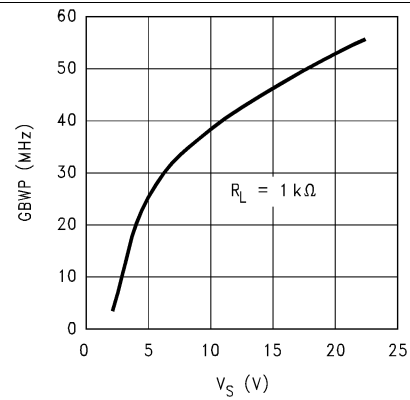


Figure 12. Output Voltage vs. Sink Current

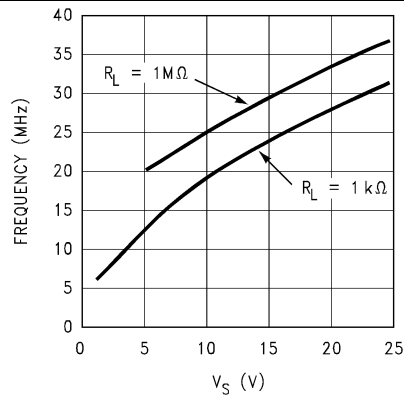
## Typical Performance Characteristics (continued)



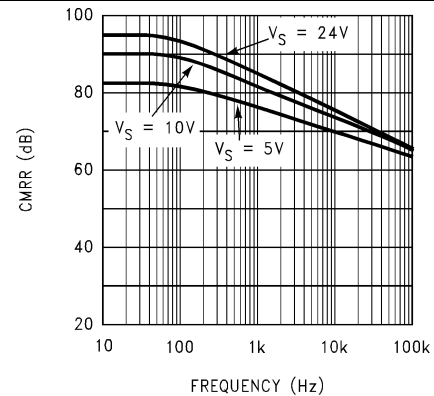
**Figure 13. Crosstalk (dB) vs. Frequency**



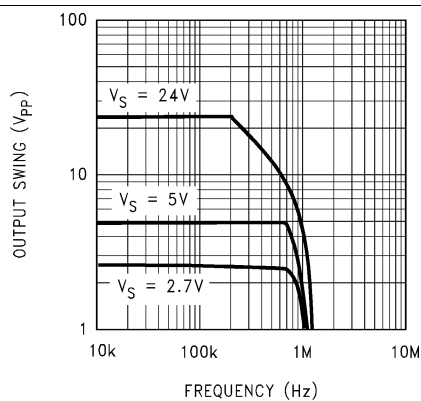
**Figure 14. GBWP (@ 100 kHz) vs. Supply Voltage**



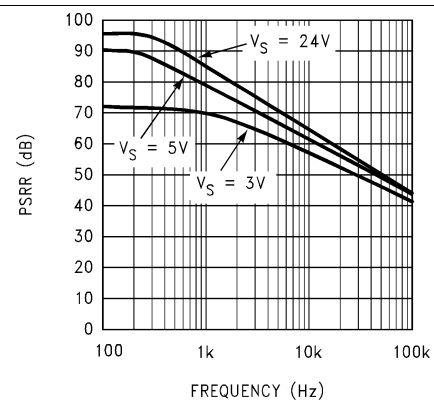
**Figure 15. Unity Gain Frequency vs. Supply Voltage for Various Loads**



**Figure 16. CMRR**

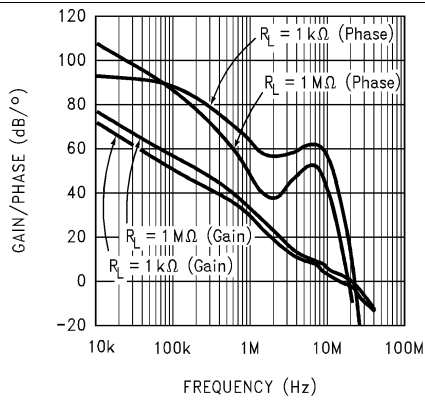


**Figure 17. Voltage Swing vs. Frequency (C<sub>L</sub> = 100 pF)**

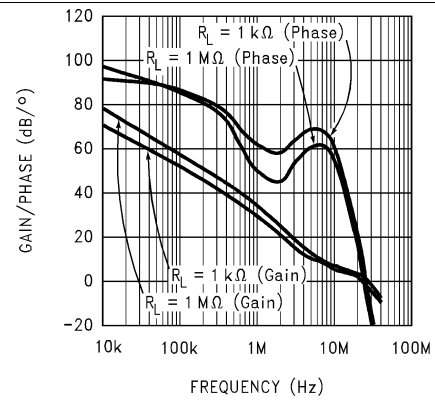


**Figure 18. PSRR vs. Frequency**

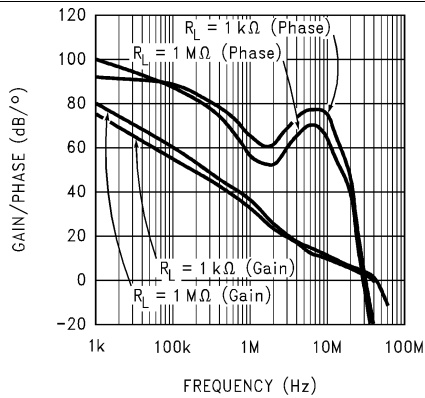
## Typical Performance Characteristics (continued)



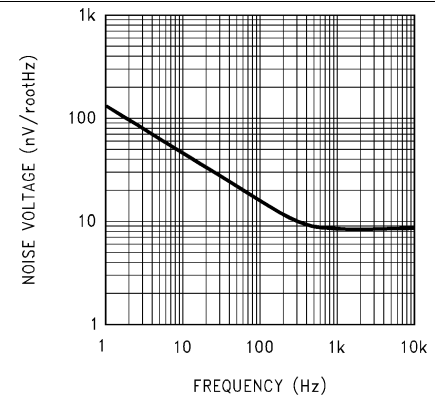
**Figure 19. Open Loop Gain/Phase**  
( $V_S = 5V$ )



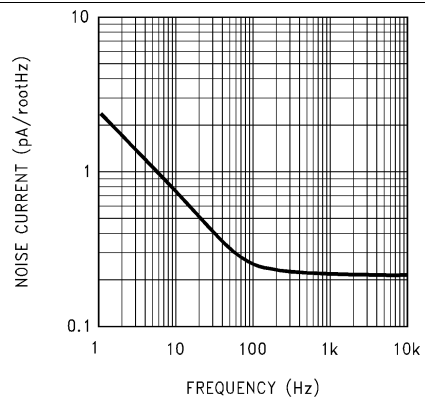
**Figure 20. Open Loop Gain/Phase**  
( $V_S = 10V$ )



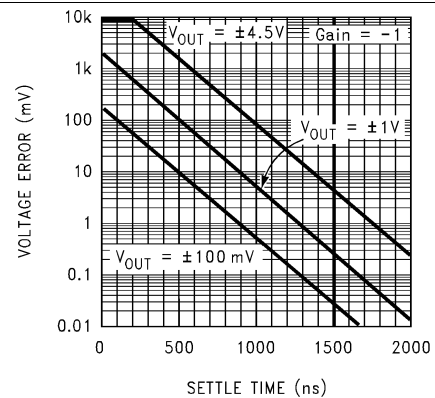
**Figure 21. Open Loop Gain/Phase**  
( $V_S = 24V$ )



**Figure 22. Noise Voltage vs. Frequency**

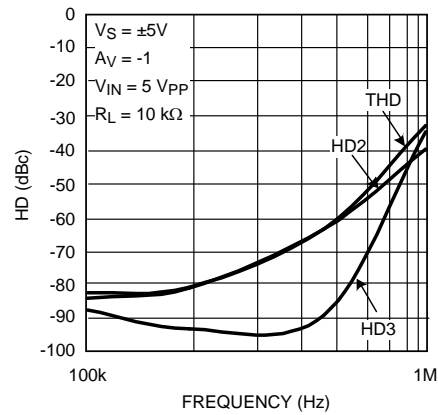


**Figure 23. Noise Current vs. Frequency**



**Figure 24. Voltage Error vs. Settle Time**

## Typical Performance Characteristics (continued)



**Figure 25. Distortion vs. Frequency**

## 7 Application and Implementation

The LM6152/LM6154 is ideally suited for operation with about 10 k $\Omega$  (Feedback Resistor,  $R_F$ ) between the output and the negative input terminal.

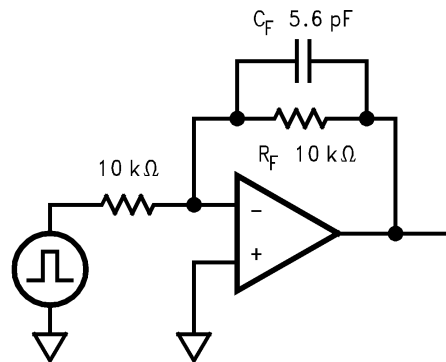
With  $R_F$  set to this value, for most applications requiring a close loop gain of 10 or less, an additional small compensation capacitor ( $C_F$ ) (see Figure 26) is recommended across  $R_F$  in order to achieve a reasonable overshoot (10%) at the output by compensating for stray capacitance across the inputs.

The optimum value for  $C_F$  can best be established experimentally with a trimmer cap in place since its value is dependant on the supply voltage, output driving load, and the operating gain. Below, some typical values used in an inverting configuration and driving a 10 k $\Omega$  load have been tabulated for reference:

**Table 1. Typical BW (–3 dB) at Various Supply Voltage and Gains**

$V_S$ Volts	GAIN	$C_F$ pF	BW (–3 dB) MHz
3	–1	5.6	4
	–10	6.8	1.97
	–100	None	0.797
24	–1	2.2	6.6
	–10	4.7	2.2
	–100	None	0.962

In the non-inverting configuration, the LM6152/LM6154 can be used for closed loop gains of +2 and above. In this case, also, the compensation capacitor ( $C_F$ ) is recommended across  $R_F$  (= 10 k $\Omega$ ) for gains of 10 or less.



**Figure 26. Typical Inverting Gain Circuit  $A_V = -1$**

Because of the unique structure of this amplifier, when used at low closed loop gains, the realizable BW will be much less than the GBW product would suggest.

The LM6152/LM6154 brings a new level of ease of use to op amp system design.

The greater than rail-to-rail input voltage range eliminates concern over exceeding the common-mode voltage range. The rail-to-rail output swing provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

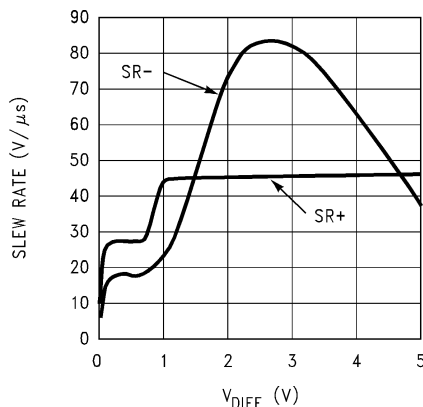
The high gain-bandwidth with low supply current opens new battery powered applications where higher power consumption previously reduced battery life to unacceptable levels.

The ability to drive large capacitive loads without oscillating functional removes this common problem.

To take advantage of these features, some ideas should be kept in mind.

The LM6152/LM6154, capacitive loads do not lead to oscillations, in all but the most extreme conditions, but they will result in reduced bandwidth. They also cause increased settling time.

Unlike most bipolar op amps, the unique phase reversal prevention/speed-up circuit in the input stage, causes the slew rate to be very much a function of the input pulse amplitude. This results in a 10 to 1 increase in slew rate when the differential input signal increases. Large fast pulses will raise the slew-rate to more than 30 V/ $\mu$ s.



**Figure 27. Slew Rate vs.  $V_{DIFF}$**

The speed-up action adds stability to the system when driving large capacitive loads.

A conventional op amp exhibits a fixed maximum slew-rate even though the differential input voltage rises due to the lagging output voltage. In the LM6152/LM6154, increasing lag causes the differential input voltage to increase but as it does, the increased slew-rate keeps the output following the input much better. This effectively reduces phase lag. As a result, the LM6152/LM6154 can drive capacitive loads as large as 470 pF at gain of 2 and above, and not oscillate.

Capacitive loads decrease the phase margin of all op amps. This can lead to overshoot, ringing and oscillation. This is caused by the output resistance of the amplifier and the load capacitance forming an R-C phase shift network. The LM6152/6154 senses this phase shift and partly compensates for this effect.

## 8 Device and Documentation Support

### 8.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 2. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM6152	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
LM6154	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 8.2 Trademarks

All trademarks are the property of their respective owners.

### 8.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 8.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">LM6152ACM/NOPB</a>	Active	Production	SOIC (D)   8	95   TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 70	LM61 52ACM
LM6152ACM/NOPB.A	Active	Production	SOIC (D)   8	95   TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 70	LM61 52ACM
LM6152ACM/NOPB.B	Active	Production	SOIC (D)   8	95   TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 70	LM61 52ACM
<a href="#">LM6152ACMX/NOPB</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	LM61 52ACM
LM6152ACMX/NOPB.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	LM61 52ACM
LM6152ACMX/NOPB.B	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	LM61 52ACM
<a href="#">LM6152BCM/NOPB</a>	Active	Production	SOIC (D)   8	95   TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 70	LM61 52BCM
LM6152BCM/NOPB.A	Active	Production	SOIC (D)   8	95   TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 70	LM61 52BCM
LM6152BCM/NOPB.B	Active	Production	SOIC (D)   8	95   TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 70	LM61 52BCM
<a href="#">LM6152BCMX/NOPB</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	LM61 52BCM
LM6152BCMX/NOPB.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	LM61 52BCM
LM6152BCMX/NOPB.B	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	LM61 52BCM
<a href="#">LM6154BCM/NOPB</a>	Active	Production	SOIC (D)   14	55   TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 70	LM6154BCM
LM6154BCM/NOPB.A	Active	Production	SOIC (D)   14	55   TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 70	LM6154BCM
LM6154BCM/NOPB.B	Active	Production	SOIC (D)   14	55   TUBE	-	Call TI	Call TI	0 to 70	
<a href="#">LM6154BCMX/NOPB</a>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	LM6154BCM
LM6154BCMX/NOPB.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	LM6154BCM
LM6154BCMX/NOPB.B	Active	Production	SOIC (D)   14	2500   LARGE T&R	-	Call TI	Call TI	0 to 70	

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM6152ACMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM6152BCMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM6154BCMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM6152ACMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM6152BCM/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM6154BCM/NOPB	SOIC	D	14	2500	367.0	367.0	35.0

## TUBE

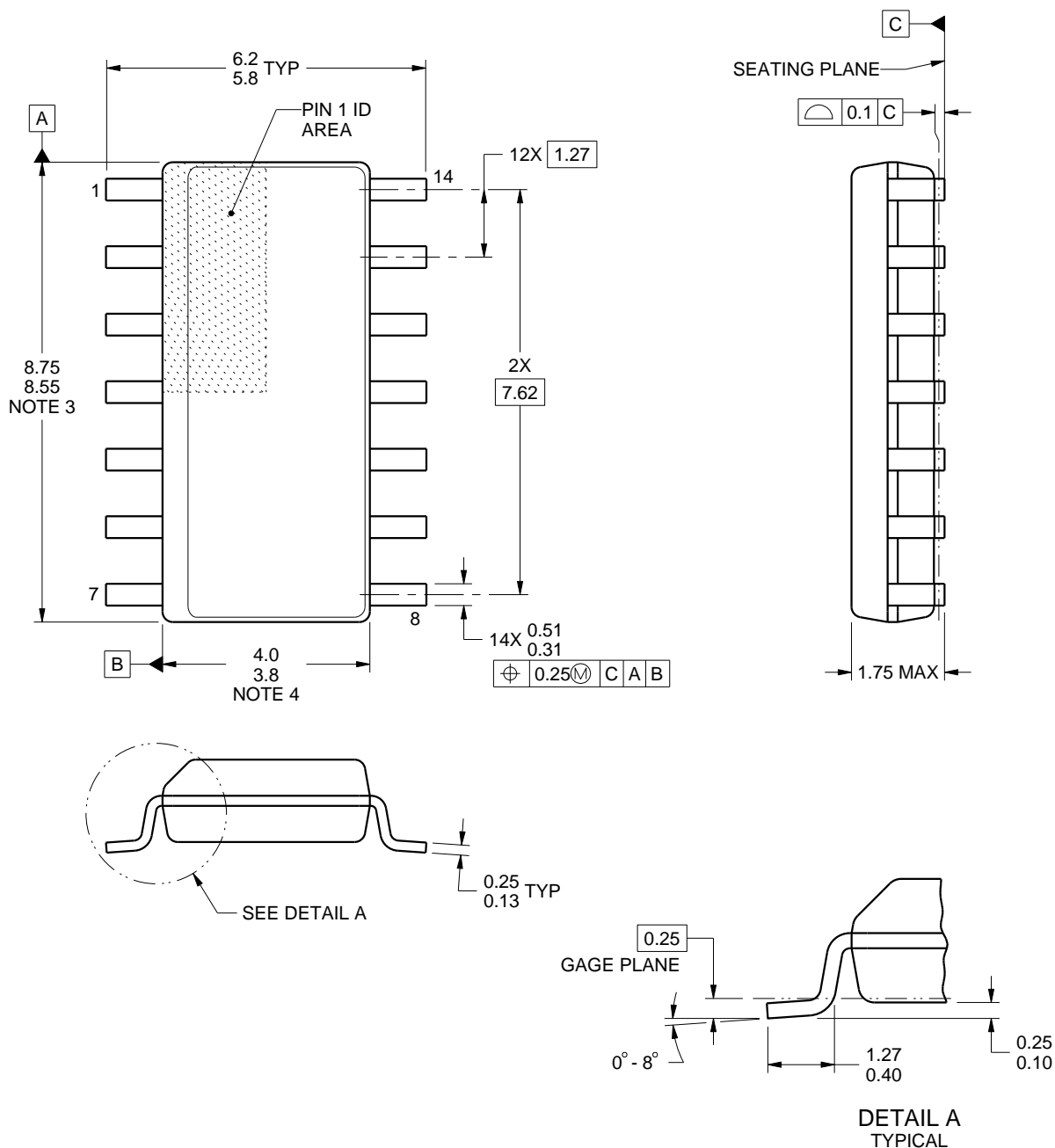


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
LM6152ACM/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM6152ACM/NOPB.A	D	SOIC	8	95	495	8	4064	3.05
LM6152ACM/NOPB.B	D	SOIC	8	95	495	8	4064	3.05
LM6152BCM/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM6152BCM/NOPB.A	D	SOIC	8	95	495	8	4064	3.05
LM6152BCM/NOPB.B	D	SOIC	8	95	495	8	4064	3.05
LM6154BCM/NOPB	D	SOIC	14	55	495	8	4064	3.05
LM6154BCM/NOPB.A	D	SOIC	14	55	495	8	4064	3.05

**D0014A****PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

**NOTES:**

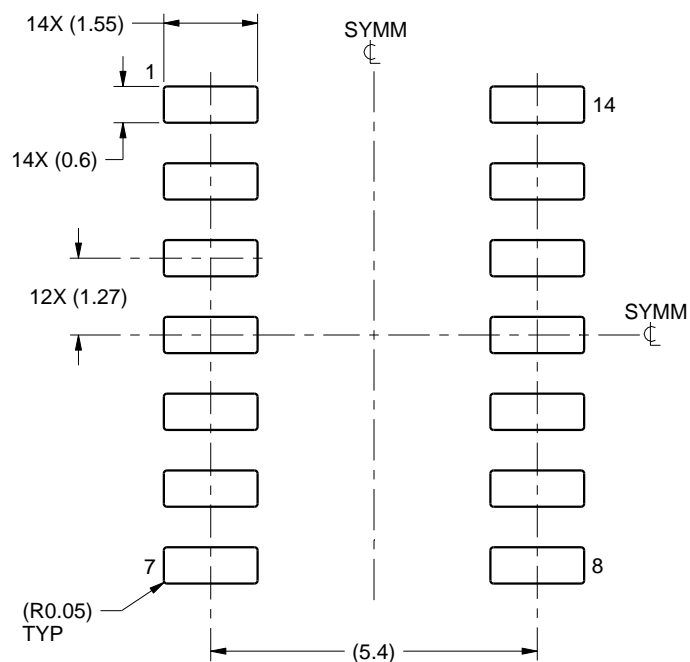
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

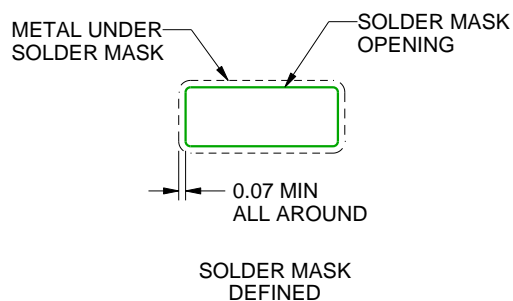
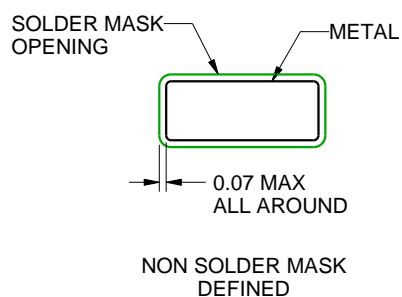
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



**D0008A****PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

**NOTES:**

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

**D0008A**

## SOIC - 1.75 mm max height

## SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



## SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2025, Texas Instruments Incorporated