LM5001x High-Voltage Switch-Mode Regulator

1 Features

- AEC-Q100 Qualified (T_J = –40°C to 125°C)
- Integrated 75-V N-Channel MOSFET
- Ultra-Wide Input Voltage Range from 3.1 V to 75 V
- Integrated High Voltage Bias Regulator
- Adjustable Output Voltage
- 1.5% Output Voltage Accuracy
- Current Mode Control with Selectable Compensation
- Wide Bandwidth Error Amplifier
- Integrated Current Sensing and Limiting
- Integrated Slope Compensation
- 85% Maximum Duty Cycle Limit
- Single Resistor Oscillator Programming
- Oscillator Synchronization Capability
- Enable / Undervoltage Lockout (UVLO) Pin
- Thermal Shutdown

2 Applications

- DC-DC Power Supplies for Industrial, Communications, and Automotive Applications
- Boost, Flyback, SEPIC and Forward Converter Topologies

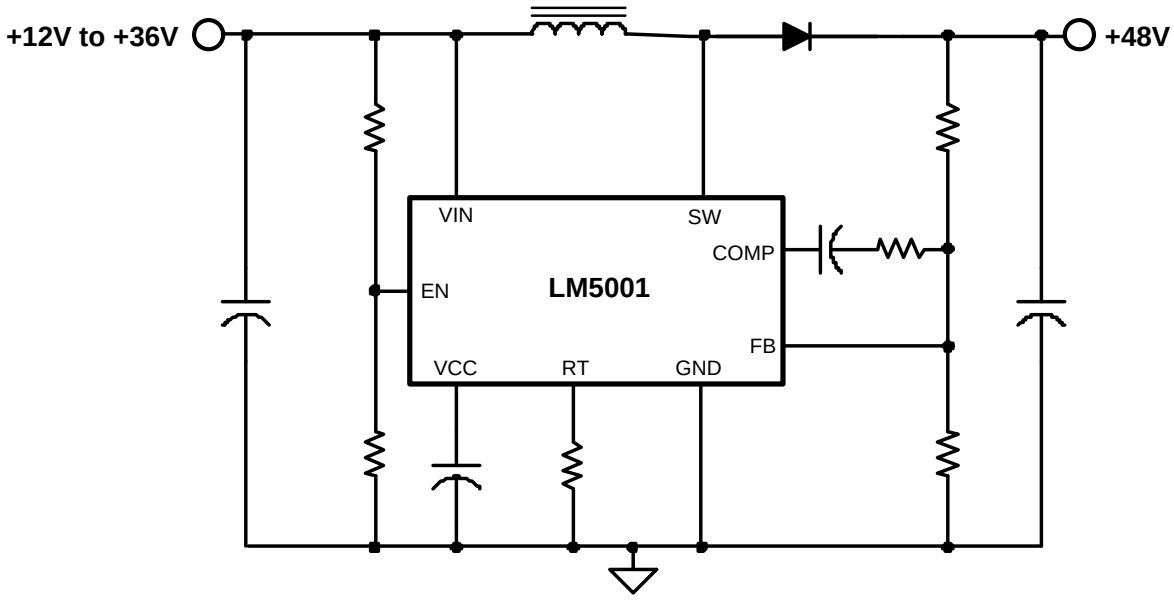
3 Description

The LM5001 high-voltage switch-mode regulator features all of the functions necessary to implement efficient high-voltage Boost, Flyback, SEPIC and Forward converters, using few external components. This easy-to-use regulator integrates a 75-V N-Channel MOSFET with a 1-A peak current limit. Current mode control provides inherently simple loop compensation and line-voltage feed-forward for superior rejection of input transients. The switching frequency is set with a single resistor and is programmable up to 1.5 MHz. The oscillator can also be synchronized to an external clock. Additional protection features include: current limit, thermal shutdown, undervoltage lockout and remote shutdown capability.

Device Information(1)

DEVICE NAME	PACKAGE	BODY SIZE
LM5001	SOIC (8)	4.9 mm x 3.91 mm
	WSON (8)	4 mm x 4 mm
LM5001Q1	SOIC (8)	4.9 mm x 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



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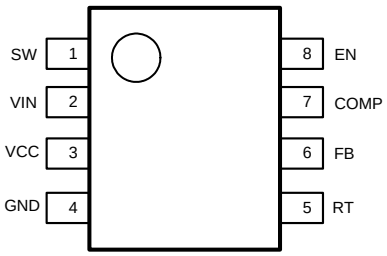
- Added LM5001-Q1 option to Electrical Characteristics table ... 5

Changes from Revision E (March 2013) to Revision F **Page**

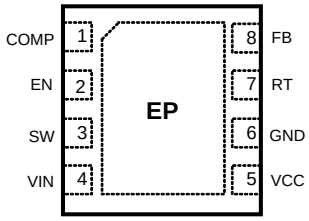
- Added availability of LM5001-Q1 option ... 1
- Changed to new TI standard: Added Handling Ratings table and the Device and Documentation Support section. ... 1

5 Pin Configuration and Functions

SOIC (D) 8 Pins
Top View



WSON (NGT) 8 Pins
Top View



Pin Functions

PIN		NAME	TYPE	DESCRIPTION
SOIC	WSON			
1	3	SW	Switch pin	The drain terminal of the internal power MOSFET.
2	4	VIN	Input supply pin	Nominal operating range: 3.1 V to 75 V.
3	5	VCC	Bias regulator output, or input for external bias supply	VCC tracks VIN up to 6.9 V. Above VIN = 6.9 V, VCC is regulated to 6.9 V. A 0.47-µF or greater ceramic decoupling capacitor is required. An external voltage (7 V – 12 V) can be applied to this pin which disables the internal VCC regulator to reduce internal power dissipation and improve converter efficiency.
4	6	GND	Ground	Internal reference for the regulator control functions and the power MOSFET current sense resistor connection.
5	7	RT	Oscillator frequency programming and optional synchronization pulse input	The internal oscillator is set with a resistor, between this pin and the GND pin. The recommended frequency range is 50 KHz to 1.5 MHz. The RT pin can accept synchronization pulses from an external clock. A 100-pF capacitor is recommended for coupling the synchronizing clock to the RT pin.
6	8	FB	Feedback input from the regulated output voltage	This pin is connected to the inverting input of the internal error amplifier. The 1.26-V reference is internally connected to the non-inverting input of the error amplifier.
7	1	COMP	Open drain output of the internal error amplifier	The loop compensation network should be connected between the COMP pin and the FB pin. COMP pull-up is provided by an internal 5-kΩ resistor which may be used to bias an opto-coupler transistor (while FB is grounded) for isolated ground applications.
8	2	EN	Enable / Undervoltage Lock-Out / Shutdown input	An external voltage divider can be used to set the line undervoltage lockout threshold. If the EN pin is left unconnected, a 6-µA pull-up current source pulls the EN pin high to enable the regulator.
NA	EP	EP	Exposed Pad, WSON only	Exposed metal pad on the underside of the package with a resistive connection to pin 6. It is recommended to connect this pad to the PC board ground plane in order to improve heat dissipation.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
VIN to GND		76	V
SW to GND (Steady State)	–0.3	76	V
VCC, EN to GND		14	V
COMP, FB, RT to GND	–0.3	7	V
Maximum Junction Temperature		150	°C
Storage Temperature Range, T_{stg}	-65	150	°C

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
VIN	3.1		75	V
Operating Junction Temperature	−40		125	°C

6.4 Thermal Information

THERMAL METRIC		LM5001-Q1	LM5001		UNIT
		SOIC	SOIC	WSON	
		(8 PINS)			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	140	140	40	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	32	32	4.5	

6.5 Electrical Characteristics

Minimum and Maximum limits are ensured through test, design, or statistical correlation, over the junction temperature (T_J) range of –40°C to +125°C. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. V_{VIN} = 10 V, R_{RT} = 48.7 kΩ unless otherwise stated(1).

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Startup Regulator						
$V_{VCC-REG}$	VCC Regulator Output		6.55	6.85	7.15	V
	VCC Current Limit	V_{VCC} = 6 V	15	20		mA
	VCC UVLO Threshold	V_{VCC} increasing	2.6	2.8	3	V
	VCC Undervoltage Hysteresis			0.1		
	Bias Current (I_{IN})	V_{FB} = 1.5 V		3.1	4.5	mA
I_Q	Shutdown Current (I_{IN})	V_{EN} = 0V		95	130	µA

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate TI's Average Outgoing Quality Level (AOQL).

Electrical Characteristics (continued)

Minimum and Maximum limits are ensured through test, design, or statistical correlation, over the junction temperature (T_J) range of –40°C to +125°C. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. V_{VIN} = 10 V, R_{RT} = 48.7 kΩ unless otherwise stated(1).

SYMBOL	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EN Thresholds							
	EN Shutdown Threshold		V_{EN} increasing	0.25	0.45	0.65	V
	EN Shutdown Hysteresis				0.1		
	EN Standby Threshold		V_{EN} increasing	1.2	1.26	1.32	
	EN Standby Hysteresis				0.1		
	EN Current Source				6		µA
MOSFET Characteristics							
	MOSFET $R_{DS(ON)}$ plus Current Sense Resistance	LM5001	I_D = 0.5 A		490	800	mΩ
		LM5001-Q1			490	880	
	MOSFET Leakage Current		V_{SW} = 75 V		0.05	5	µA
	MOSFET Gate Charge		V_{VCC} = 6.9 V		4.5		nC
Current Limit							
I_{LIM}	Cycle by Cycle Current Limit			0.8	1.0	1.2	A
	Cycle by Cycle Current Limit Delay				100	200	ns
Oscillator							
F_{SW1}	Frequency1		R_{RT} = 48.7 kΩ	225	260	295	KHz
F_{SW2}	Frequency2		R_{RT} = 15.8 kΩ	660	780	900	
$V_{RT-SYNC}$	SYNC Threshold			2.2	2.6	3.2	V
	SYNC Pulse Width Minimum		$V_{RT} > V_{RT-SYNC}$ + 0.5 V		15		ns
PWM Comparator							
	Maximum Duty Cycle			80%	85%	90%	
	Min On-time		$V_{COMP} > V_{COMP-OS}$		35		ns
	Min On-time		$V_{COMP} < V_{COMP-OS}$		0		
$V_{COMP-OS}$	COMP to PWM Comparator Offset			0.9	1.30	1.55	V
Error Amplifier							
V_{FB-REF}	Feedback Reference Voltage		Internal reference $V_{FB} = V_{COMP}$	1.241	1.260	1.279	V
	FB Bias Current				10		nA
	DC Gain				72		dB
	COMP Sink Current		V_{COMP} = 250 mV	2.5			mA
	COMP Short Circuit Current		V_{FB} = 0, V_{COMP} = 0	0.9	1.2	1.5	
	COMP Open Circuit Voltage		V_{FB} = 0	4.8	5.5	6.2	V
	COMP to SW Delay				50		ns
	Unity Gain Bandwidth				3		MHz
Thermal Shutdown							
T_{SD}	Thermal Shutdown Threshold				165		°C
	Thermal Shutdown Hysteresis				20		

6.6 Typical Characteristics

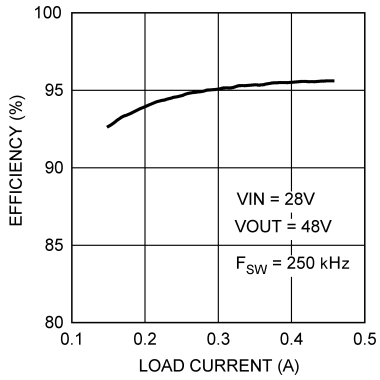


Figure 1. Efficiency, Boost Converter

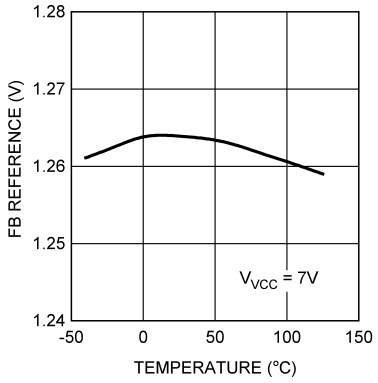


Figure 2. V_{FB} vs Temperature

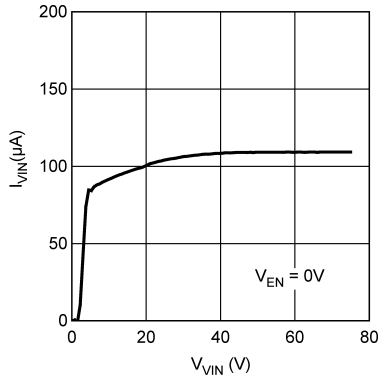


Figure 3. I_Q (Non-Switching) vs VIN

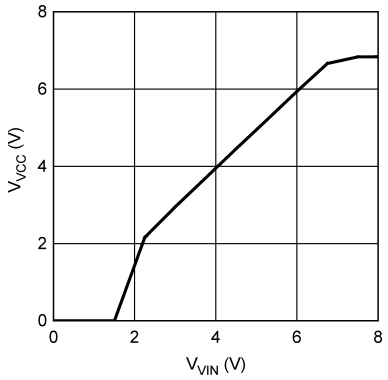


Figure 4. VCC vs VIN

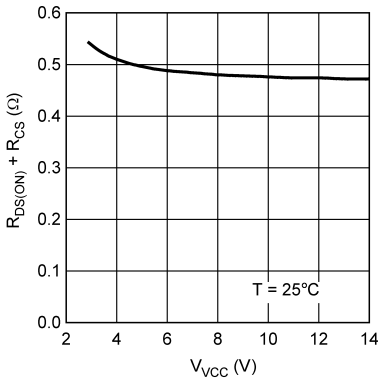


Figure 5. $R_{DS(ON)}$ vs VCC

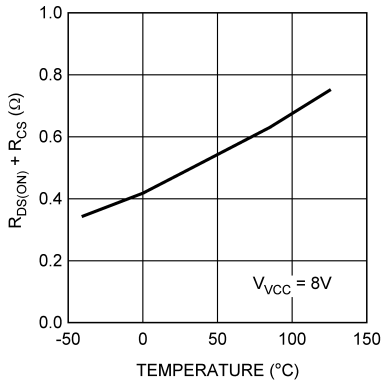


Figure 6. $R_{DS(ON)}$ vs Temperature

Typical Characteristics (continued)

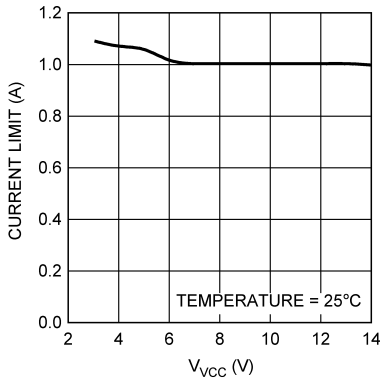


Figure 7. I_{LIM} vs VCC

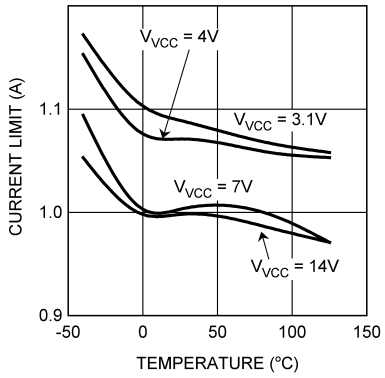


Figure 8. I_{LIM} vs VCC vs Temperature

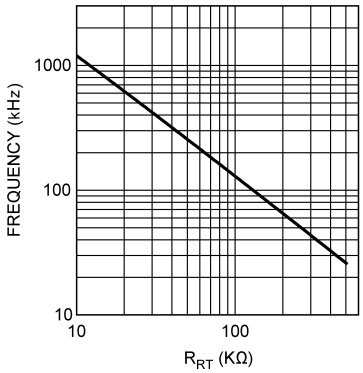


Figure 9. F_{SW} vs R_{RT}

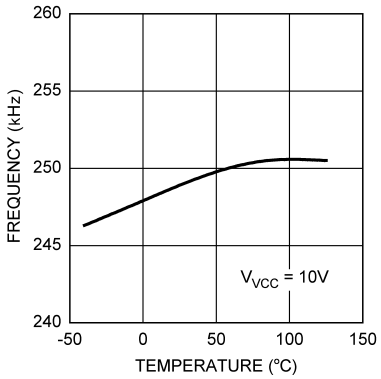


Figure 10. F_{SW} vs Temperature

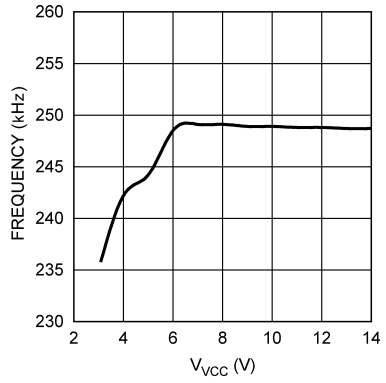


Figure 11. F_{SW} vs VCC

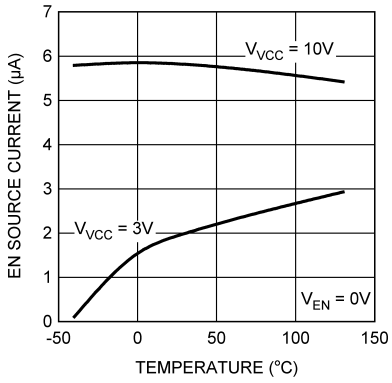


Figure 12. I_{EN} vs V_{VIN} vs Temperature

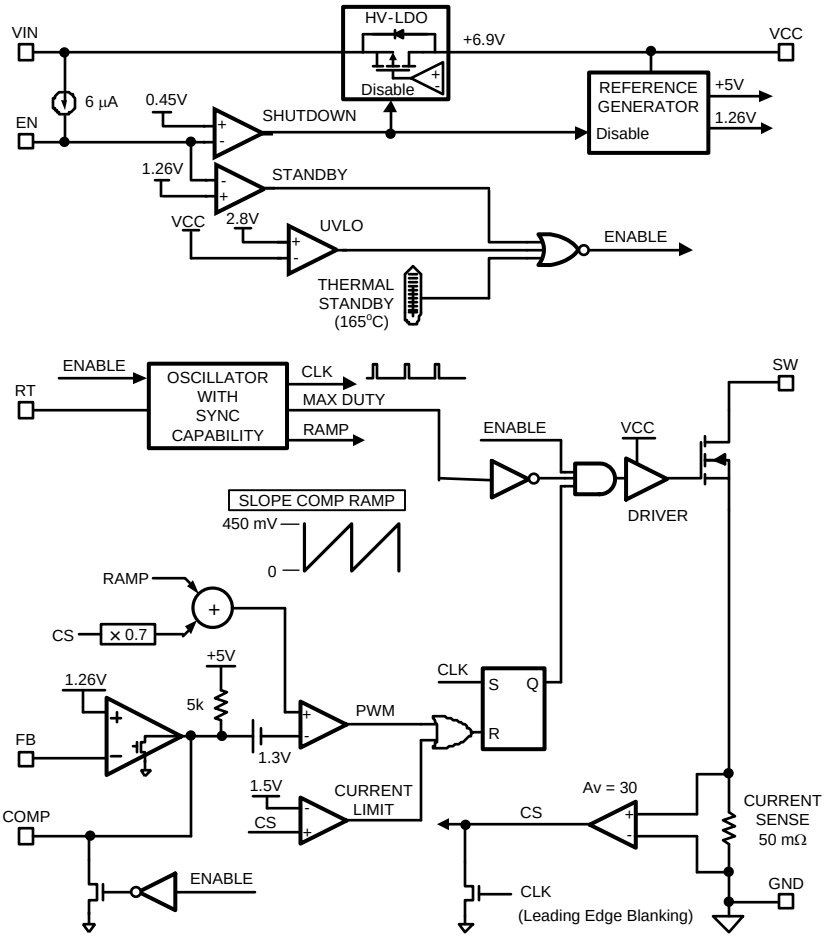
7 Detailed Description

7.1 Overview

The LM5001 high voltage switching regulator features all the functions necessary to implement an efficient boost, flyback, SEPIC or forward current mode power converter. The operation can be best understood by referring to the block diagram. At the start of each cycle, the oscillator sets the driver logic and turns on the power MOSFET to conduct current through the inductor or transformer. The peak current in the MOSFET is controlled by the voltage at the COMP pin. The COMP voltage increases with larger loads and decrease with smaller loads. This voltage is compared with the sum of a voltage proportional to the power MOSFET current and an internally generated Slope Compensation ramp. Slope Compensation is used in current mode PWM architectures to eliminate sub-harmonic current oscillation that occurs with static duty cycles greater than 50%. When the summed signal exceeds the COMP voltage, the PWM comparator resets the driver logic, turning off the power MOSFET. The driver logic is then set by the oscillator at the end of the switching cycle to initiate the next power period.

The LM5001 has dedicated protection circuitry to protect the IC from abnormal operating conditions. Cycle-by-cycle current limiting prevents the power MOSFET current from exceeding 1 A. This feature can also be used to soft-start the regulator. Thermal Shutdown circuitry holds the driver logic in reset when the die temperature reaches 165°C, and returns to normal operation when the die temperature drops by approximately 20°C. The EN pin can be used as an input voltage undervoltage lockout (UVLO) during start-up to prevent operation with less than the minimum desired input voltage.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 High-Voltage VCC Regulator

The LM5001 VCC Low Drop Out (LDO) regulator allows the LM5001 to operate at the lowest possible input voltage. The VCC pin voltage is very nearly equal to the input voltage from 2.8 V up to approximately 6.9 V. As the input voltage continues to increase, the VCC pin voltage is regulated at the 6.9 V set-point. The total input operating range of the VCC LDO regulator is 3.1 V to 75 V.

The output of the VCC regulator is current limited to 20 mA. During power up, the VCC regulator supplies current into the required decoupling capacitor (0.47 µF or greater ceramic capacitor) at the VCC pin. When the voltage at the VCC pin exceeds the VCC UVLO threshold of 2.8 V and the EN pin is greater than 1.26 V the PWM controller is enabled and switching begins. The controller remains enabled until VCC falls below 2.7 V or the EN pin falls below 1.16 V.

An auxiliary supply voltage can be applied to the VCC pin to reduce the IC power dissipation. If the auxiliary voltage is greater than 6.9 V, the internal regulator essentially shuts off, and internal power dissipation decreases by the VIN voltage times the operating current. The overall converter efficiency improves if the VIN voltage is much higher than the auxiliary voltage. The externally applied VCC voltage should not exceed 14 V. The VCC regulator series pass MOSFET includes a body diode (Functional Block Diagram) between VCC and VIN that should not be forward biased in normal operation. Therefore, the auxiliary VCC voltage should never exceed the VIN voltage.

In high voltage applications extra care should be taken to ensure the VIN pin does not exceed the absolute maximum voltage rating of 76 V. Voltage ringing on the VIN line during line transients that exceeds the Absolute Maximum Ratings damages the IC. Both careful PC board layout and the use of quality bypass capacitors located close to the VIN and GND pins are essential.

7.3.2 Oscillator

A single external resistor connected between RT and GND pins sets the LM5001 oscillator frequency. To set a desired oscillator frequency (F_{SW}), the necessary value for the RT resistor can be calculated from:

$$RT = 13.1 \times 10^9 \times \left(\frac{1}{F_{SW}} - 83\ ns\right) \quad (1)$$

The tolerance of the external resistor and the frequency tolerance indicated in the Electrical Characteristics must be taken into account when determining the worst case frequency range.

7.3.3 External Synchronization

The LM5001 can be synchronized to the rising edge of an external clock. The external clock must have a higher frequency than the free running oscillator frequency set by the RT resistor. The clock signal should be coupled through a 100 pF capacitor into the RT pin. A peak voltage level greater than 2.6 V at the RT pin is required for detection of the sync pulse. The DC voltage across the RT resistor is internally regulated at 1.5 V. The negative portion of the AC voltage of the synchronizing clock is clamped to this 1.5 V by an amplifier inside the LM5001 with ~100 Ω output impedance. Therefore, the AC pulse superimposed on the RT resistor must have positive pulse amplitude of 1.1 V or greater to successfully synchronize the oscillator. The sync pulse width measured at the RT pin should have a duration greater than 15 ns and less than 5% of the switching period. The sync pulse rising edge initiates the internal CLK signal rising edge, which turns off the power MOSFET. The RT resistor is always required, whether the oscillator is free running or externally synchronized. The RT resistor should be located very close to the device and connected directly to the RT and GND pins of the LM5001.

7.3.4 Enable / Standby

The LM5001 contains a dual level Enable circuit. When the EN pin voltage is below 450 mV, the IC is in a low current shutdown mode with the VCC LDO disabled. When the EN pin voltage is raised above the shutdown threshold but below the 1.26 V standby threshold, the VCC LDO regulator is enabled, while the remainder of the IC is disabled. When the EN pin voltage is raised above the 1.26 V standby threshold, all functions are enabled and normal operation begins. An internal 6 µA current source pulls up the EN pin to activate the IC when the EN pin is left disconnected.

Feature Description (continued)

An external set-point resistor divider from VIN to GND can be used to determine the minimum operating input range of the regulator. The divider must be designed such that the EN pin exceeds the 1.26 V standby threshold when VIN is in the desired operating range. The internal 6 µA current source should be included when determining the resistor values. The shutdown and standby thresholds have 100 mV hysteresis to prevent noise from toggling between modes. When the VIN voltage is below 3.5 VDC during start-up and the operating temperature is below –20°C, the EN pin should have a pull-up resistor provides 2 µA or greater current. The EN pin is internally protected by a 6 V Zener diode through a 1 kΩ resistor. The enabling voltage may exceed the Zener voltage, however the Zener current should be limited to less than 4 mA.

7.3.5 Error Amplifier and PWM Comparator

An internal high gain error amplifier generates an error signal proportional to the difference between the regulated output voltage and an internal precision reference. The output of the error amplifier is connected to the COMP pin allowing the user to add loop compensation, typically a Type II network, as illustrated in Figure 13. This network creates a low frequency pole that rolls off the high DC gain of the amplifier, which is necessary to accurately regulate the output voltage. F_{DC_POLE} is the closed loop unity gain (0 dB) frequency of this pole. A zero provides phase boost near the closed loop unity gain frequency, and a high frequency pole attenuates switching noise. The PWM comparator compares the current sense signal from the current sense amplifier to the error amplifier output voltage at the COMP pin.

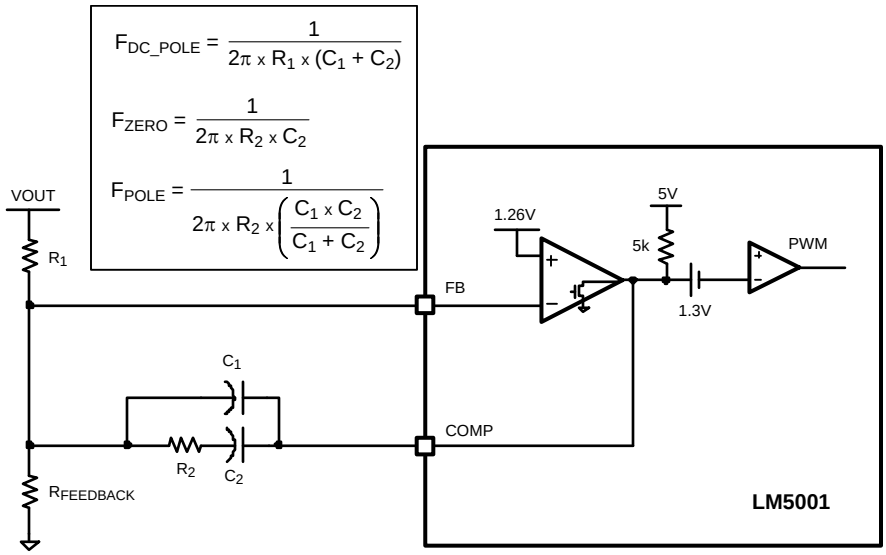


Figure 13. Type II Compensator

When isolation between primary and secondary circuits is required, the Error Amplifier is usually disabled by connecting the FB pin to GND. This allows the COMP pin to be driven directly by the collector of an opto-coupler. In isolated designs the external error amplifier is located on the secondary circuit and drives the opto-coupler LED. The compensation network is connected to the secondary side error amplifier. An example of an isolated regulator with an opto-coupler is shown in Figure 19.

7.3.6 Current Amplifier and Slope Compensation

The LM5001 employs peak current mode control which also provides a cycle-by-cycle over current protection feature. An internal 50 mΩ current sense resistor measures the current in the power MOSFET source. The sense resistor voltage is amplified 30 times to provide a 1.5 V/A signal into the current limit comparator. Current limiting is initiated if the internal current limit comparator input exceeds the 1.5 V threshold, corresponding to 1 A. When the current limit comparator is triggered, the SW output pin immediately switches to a high impedance state.

Feature Description (continued)

The current sense signal is reduced to a scale factor of 1.05 V/A for the PWM comparator signal. The signal is then summed with a 450 mV peak slope compensation ramp. The combined signal provides the PWM comparator with a control signal that reaches 1.5 V when the MOSFET current is 1 A. For duty cycles greater than 50%, current mode control circuits are subject to sub-harmonic oscillation (alternating between short and long PWM pulses every other cycle). Adding a fixed slope voltage ramp signal (slope compensation) to the current sense signal prevents this oscillation. The 450 mV ramp (zero volts when the power MOSFET turns on, and 450 mV at the end of the PWM clock cycle) adds a fixed slope to the current sense ramp to prevent oscillation.

To prevent erratic operation at low duty cycle, a leading edge blanking circuit attenuates the current sense signal when the power MOSFET is turned on. When the MOSFET is initially turned on, current spikes from the power MOSFET drain-source and gate-source capacitances flow through the current sense resistor. These transient currents normally cease within 50 ns with proper selection of rectifier diodes and proper PC board layout.

7.3.7 Thermal Protection

Internal Thermal Shutdown circuitry is provided to protect the IC in the event the maximum junction temperature is exceeded. When the 165°C junction temperature threshold is reached, the regulator is forced into a low power standby state, disabling all functions except the VCC regulator. Thermal hysteresis allows the IC to cool down before it is re-enabled. Note that since the VCC regulator remains functional during this period, the soft-start circuit shown in Figure 17 should be augmented if soft-start from Thermal Shutdown state is required.

7.3.8 Power MOSFET

The LM5001 switching regulator includes an N-Channel MOSFET with 440-mΩ on-resistance. The on-resistance of the LM5001 MOSFET varies with temperature as shown in the Typical Characteristics graph. The typical total gate charge for the MOSFET is 4.5 nC which is supplied from the VCC pin when the MOSFET is turned on.

8 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

This information is intended to provide guidelines for the power supply designer using the LM5001.

8.1.1 VIN

The voltage applied to the VIN pin can vary within the range of 3.1 V to 75 V. The current into the VIN pin depends primarily on the gate charge of the power MOSFET, the switching frequency, and any external load on the VCC pin. It is recommended the filter shown in Figure 14 be used to suppress transients which may occur at the input supply. This is particularly important when VIN is operated close to the maximum operating rating of the LM5001.

When power is applied and the VIN voltage exceeds 2.8 V with the EN pin voltage greater than 0.45 V, the VCC regulator is enabled, supplying current into the external capacitor connected to the VCC pin. When the VIN voltage is between 2.8 V and 6.9 V, the VCC voltage is approximately equal to the VIN voltage. When the voltage on the VCC pin exceeds 6.9 V, the VCC pin voltage is regulated at 6.9 V. In typical flyback applications, an auxiliary transformer winding is connected through a diode to the VCC pin. This winding must raise the VCC voltage above 6.9 V to shut off the internal start-up regulator. The current requirements from this winding are relatively small, typically less than 20 mA. If the VIN voltage is much higher than the auxiliary voltage, the auxiliary winding significantly improves conversion efficiency. It also reduces the power dissipation within the LM5001. The externally applied VCC voltage should never exceed 14 V. Also the applied VCC should never exceed the VIN voltage to avoid reverse current through the internal VCC to VIN diode shown in the LM5001 block diagram.

Application Information (continued)

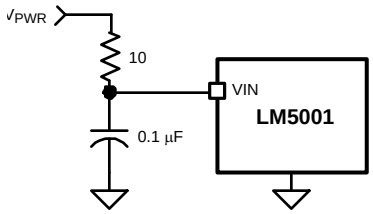


Figure 14. Input Transient Protection

8.1.2 SW Pin

Attention must be given to the PC board layout for the SW pin which connects to the power MOSFET drain. Energy can be stored in parasitic inductance and capacitance which cause switching spikes that negatively effect efficiency, and conducted and radiated emissions. These connections should be as short as possible to reduce inductance and as wide as possible to reduce resistance. The loop area, defined by the SW and GND pin connections, the transformer or inductor terminals, and their respective return paths, should be minimized.

8.1.3 EN / UVLO Voltage Divider Selection

Two dedicated comparators connected to the EN pin are used to detect under-voltage and shutdown conditions. When the EN pin voltage is below 0.45 V, the controller is in a low current shutdown mode where the VIN current is reduced to 95 µA. For an EN pin voltage greater than 0.45 V but less than 1.26 V the controller is in standby mode, with all internal circuits operational, but the PWM gate driver signal is blocked. Once the EN pin voltage is greater than 1.26 V, the controller is fully enabled. Two external resistors can be used to program the minimum operational voltage for the power converter as shown in Figure 15. When the EN pin voltage falls below the 1.26 V threshold, an internal 100 mV threshold hysteresis prevents noise from toggling the state, so the voltage must be reduced to 1.16 V to transition to standby. Resistance values for R1 and R2 can be determined from Equation 2 and Equation 3:

$$R1 = \frac{V_{PWR} - 1.26V}{I_{DIVIDER}} \quad (2)$$

$$R2 = \frac{1.26V}{I_{DIVIDER} + 6\ \mu A} \quad (3)$$

where V_{PWR} is the desired turn-on voltage and $I_{DIVIDER}$ is an arbitrary current through R1 and R2.

For example, if the LM5001 is to be enabled when V_{PWR} reaches 16 V, $I_{DIVIDER}$ could be chosen as 501 µA which would set R1 to 29.4 kΩ and R2 to 2.49 kΩ. The voltage at the EN pin should not exceed 10 V unless the current into the 6 V protection Zener diode is limited below 4 mA. The EN pin voltage should not exceed 14 V at any time. Be sure to check both the power and voltage rating (some 0603 resistors are rated as low as 50 V) for the selected R1 resistor.

Application Information (continued)

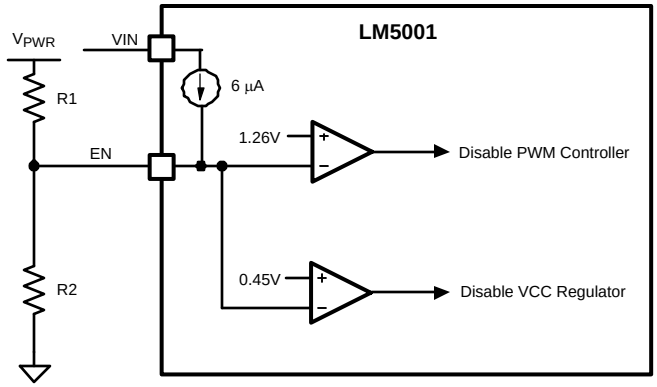


Figure 15. Basic EN (UVLO) Configuration

Remote configuration of the controller's operational modes can be accomplished with open drain device(s) connected to the EN pin as shown in Figure 16. A MOSFET or an NPN transistor connected to the EN pin can force the regulator into the low power 'off' state. Adding a PN diode in the drain (or collector) provides the offset to achieve the standby state. The advantage of standby is that the VCC LDO is not disabled and external circuitry powered by VCC remains functional.

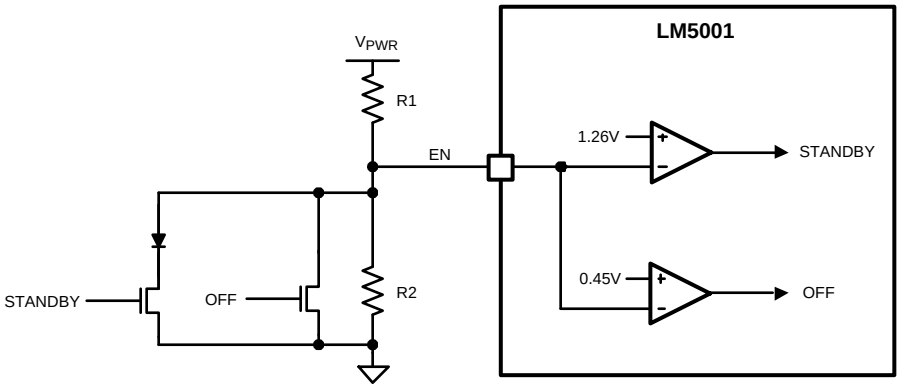


Figure 16. Remote Standby and Disable Control

8.1.4 Soft-Start

Soft-start (SS) can be implemented with an external capacitor connected to COMP through a diode as shown in Figure 17. The COMP discharge MOSFET conducts during Shutdown and Standby modes to keep the COMP voltage below the PWM offset (1.3 V), which inhibits PWM pulses. The error amplifier attempts to raise the COMP voltage after the EN pin exceeds the 1.26-V standby threshold. Because the error amplifier output can only sink current, the internal COMP pull-up resistor (~5 kΩ) supplies the charging current to the SS capacitor. The SS capacitor causes the COMP voltage to gradually increase, until the output voltage achieves regulation and FB assumes control of the COMP and the PWM duty cycle. The SS capacitor continues charging through a large resistance, R_{SS}, preventing the SS circuit from interfering with the normal error amplifier function. During shutdown, the VCC diode discharges the SS capacitor.

Application Information (continued)

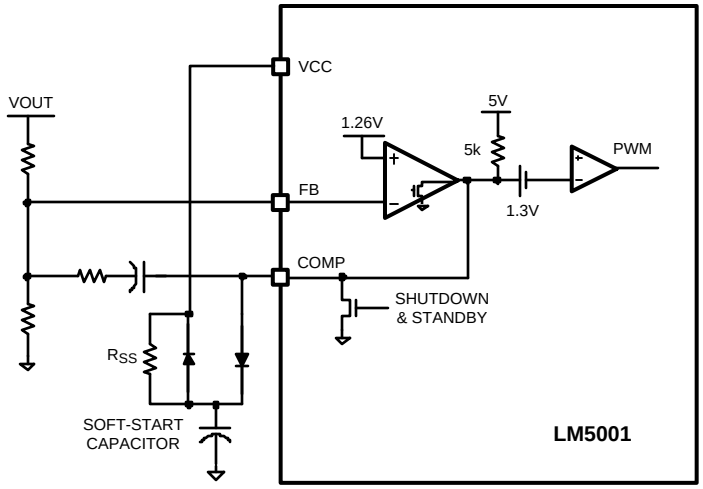


Figure 17. Soft-Start

8.2 Typical Applications

Figure 18, Figure 19, Figure 20, Figure 21, and Figure 22 present examples of a Non-Isolated Flyback, Isolated Flyback, Boost, 24-V SEPIC and a 12-V Automotive range SEPIC converters utilizing the LM5001 switching regulator.

8.2.1 Non-Isolated Flyback

The Non-Isolated Flyback converter (Figure 18) utilizes the internal voltage reference for the regulation setpoint. The output is 5 V at 1 A while the input voltage can vary from 16 V to 42 V. The switching frequency is set to 250 kHz. An auxiliary winding on transformer (T1) provides 7.5 V to power the LM5001 when the output is in regulation. This disables the internal high voltage VCC LDO regulator and improves efficiency. The input under-voltage threshold is 13.9 V. The converter can be shut down by driving the EN input below 1.26 V with an open-collector or open-drain transistor. An external synchronizing frequency can be applied to the SYNC input. An optional soft-start circuit is connected to the COMP pin input. When power is applied, the soft-start capacitor (C7) is discharged and limits the voltage applied to the PWM comparator by the internal error amplifier. The internal ~5 kΩ COMP pull-up resistor charges the soft-start capacitor until regulation is achieved. The VCC pull-up resistor (R7) continues to charge C7 so that the soft-start circuit will not affect the compensation network in normal operation. If the output capacitance is small, the soft-start circuit can be adjusted to limit the power-on output voltage overshoot. If the output capacitance is sufficiently large, no soft-start circuit is needed because the LM5001 gradually charges the output capacitor by current limiting at approximately 1 A (I_{LIM}) until regulation is achieved.

Typical Applications (continued)

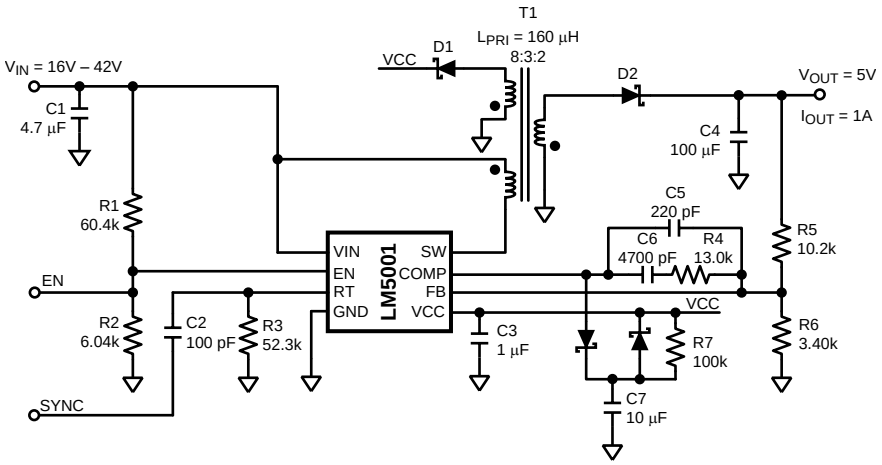


Figure 18. Non-Isolated Flyback

8.2.2 Isolated Flyback

The Isolated Flyback converter (Figure 19) utilizes a 2.5 V voltage reference (LM431) located on the isolated secondary side for the regulation setpoint. The LM5001 internal error amplifier is disabled by grounding the FB pin. The LM431 controls the current through the opto-coupler LED, which sets the COMP pin voltage. The R4 and C3 network boosts the phase response of the opto-coupler to increase the loop bandwidth. The output is 5 V at 1 A and the input voltage ranges from 16 V to 42 V. The switching frequency is set to 250 kHz.

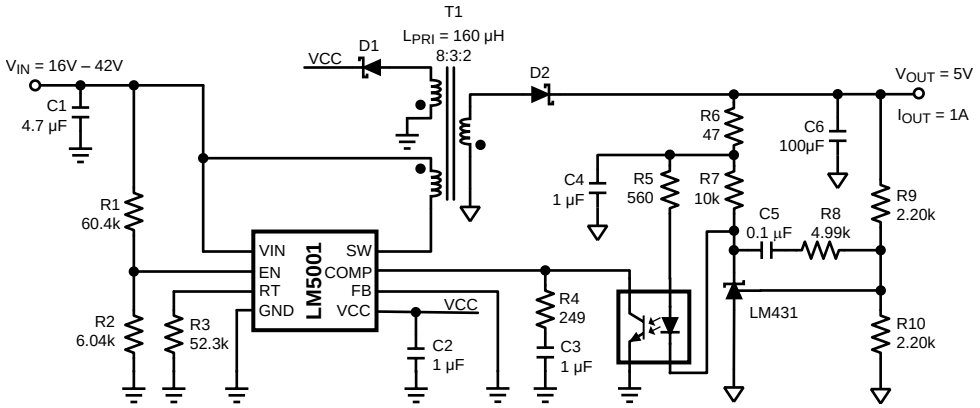


Figure 19. Isolated Flyback

8.2.3 Boost

The Boost converter (Figure 20) utilizes the internal voltage reference for the regulation setpoint. The output is 48 V at 150 mA, while the input voltage can vary from 16 V to 36 V. The switching frequency is set to 250 kHz. The internal VCC regulator provides 6.9 V bias power, since there isn't a simple method for creating an auxiliary voltage with the boost topology. Note that the boost topology does not provide output short-circuit protection because the power MOSFET cannot interrupt the path between the input and the output.

Typical Applications (continued)

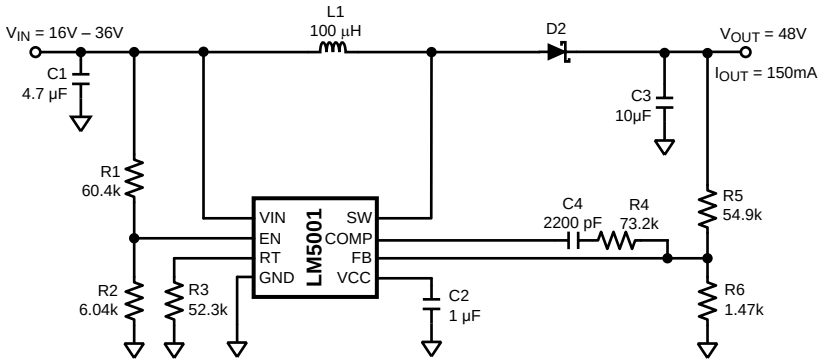


Figure 20. Boost

8.2.4 24-V SEPIC

The 24-V SEPIC converter (Figure 21) utilizes the internal voltage reference for the regulation setpoint. The output is 24 V at 250 mA while the input voltage can vary from 16 V to 48 V. The switching frequency is set to 250 kHz. The internal VCC regulator provides 6.9 V bias power for the LM5001. An auxiliary voltage can be created by adding a winding on L2 and a diode into the VCC pin.

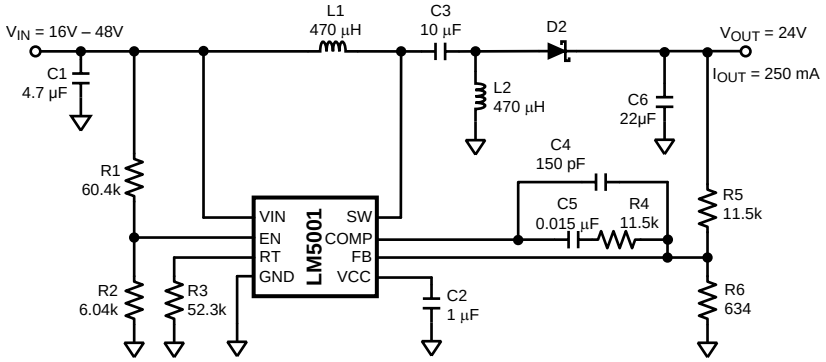


Figure 21. 24-V SEPIC

8.2.5 12-V Automotive SEPIC

The 12-V Automotive SEPIC converter (Figure 22) utilizes the internal bandgap voltage reference for the regulation setpoint. The output is 12 V at 50 mA while the input voltage can vary from 3.1 V to 60 V. The output current rating can be increased if the minimum VIN voltage requirement is increased. The switching frequency is set to 750 kHz. The internal VCC regulator provides 6.9 V bias power for the LM5001. The output voltage can be used as an auxiliary voltage if the nominal VIN voltage is greater than 12 V by adding a diode from the output into the VCC pin. In this configuration, the minimum input voltage must be greater than 12 V to prevent the internal VCC to VIN diode from conducting. If the applied VCC voltage exceeds the minimum VIN voltage, then an external blocking diode is required between the VIN pin and the power source to block current flow from VCC to the input supply.

Typical Applications (continued)

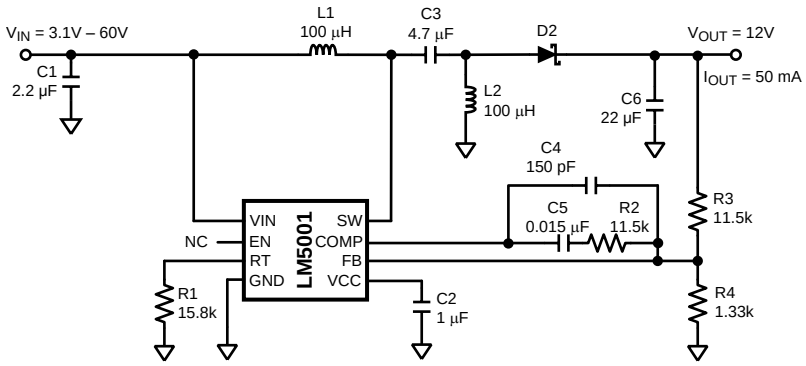


Figure 22. 12-V SEPIC

9 Layout

9.1 Layout Guidelines

The LM5001 Current Sense and PWM comparators are very fast and may respond to short duration noise pulses. The components at the SW, COMP, EN and the RT pins should be as physically close as possible to the IC, thereby minimizing noise pickup on the PC board tracks.

The SW output pin of the LM5001 should have a short, wide conductor to the power path inductors, transformers and capacitors in order to minimize parasitic inductance that reduces efficiency and increases conducted and radiated noise. Ceramic decoupling capacitors are recommended between the VIN pin to the GND pin and between the VCC pin to the GND pin. Use short, direct connections to avoid clock jitter due to ground voltage differentials. Small package surface mount X7R or X5R capacitors are preferred for high frequency performance and limited variation over temperature and applied voltage.

If an application using the LM5001 produces high junction temperatures during normal operation, multiple vias from the GND pin to a PC board ground plane helps conduct heat away from the IC. Judicious positioning of the PC board within the end product, along with use of any available air flow helps reduce the junction temperatures. If using forced air cooling, avoid placing the LM5001 in the airflow shadow of large components, such as input capacitors, inductors or transformers.

10 Device and Documentation Support

10.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM5001	Click here	Click here	Click here	Click here	Click here
LM5001-Q1	Click here	Click here	Click here	Click here	Click here

10.2 Trademarks

All trademarks are the property of their respective owners.

10.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

10.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM5001IDQ1	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L5001 IDQ1
LM5001IDQ1.Z	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L5001 IDQ1
LM5001IDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L5001 IDQ1
LM5001IDRQ1.Z	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L5001 IDQ1
LM5001MA/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L5001 MA
LM5001MA/NOPB.Z	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L5001 MA
LM5001MAX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L5001 MA
LM5001MAX/NOPB.Z	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L5001 MA
LM5001SD/NOPB	Active	Production	WSON (NGT) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5001
LM5001SD/NOPB.Z	Active	Production	WSON (NGT) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5001
LM5001SDE/NOPB	Active	Production	WSON (NGT) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5001
LM5001SDE/NOPB.Z	Active	Production	WSON (NGT) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5001
LM5001SDX/NOPB	Active	Production	WSON (NGT) | 8	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5001
LM5001SDX/NOPB.Z	Active	Production	WSON (NGT) | 8	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5001

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF LM5001, LM5001-Q1 :

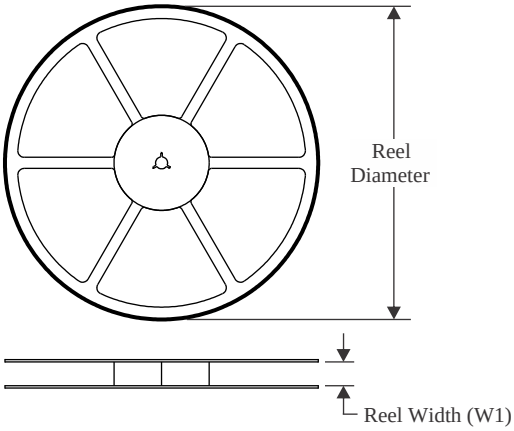
- Catalog : LM5001
- Automotive : LM5001-Q1

NOTE: Qualified Version Definitions:

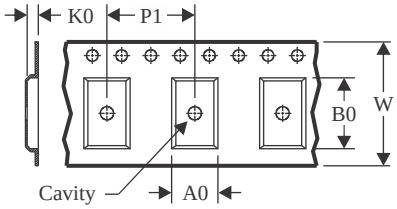
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

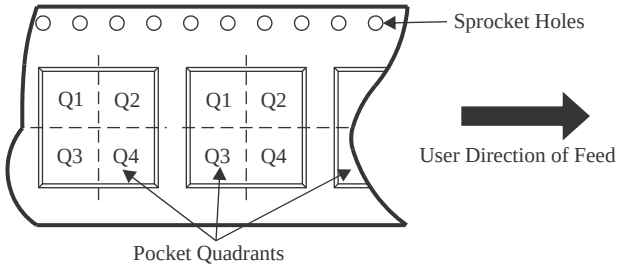


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

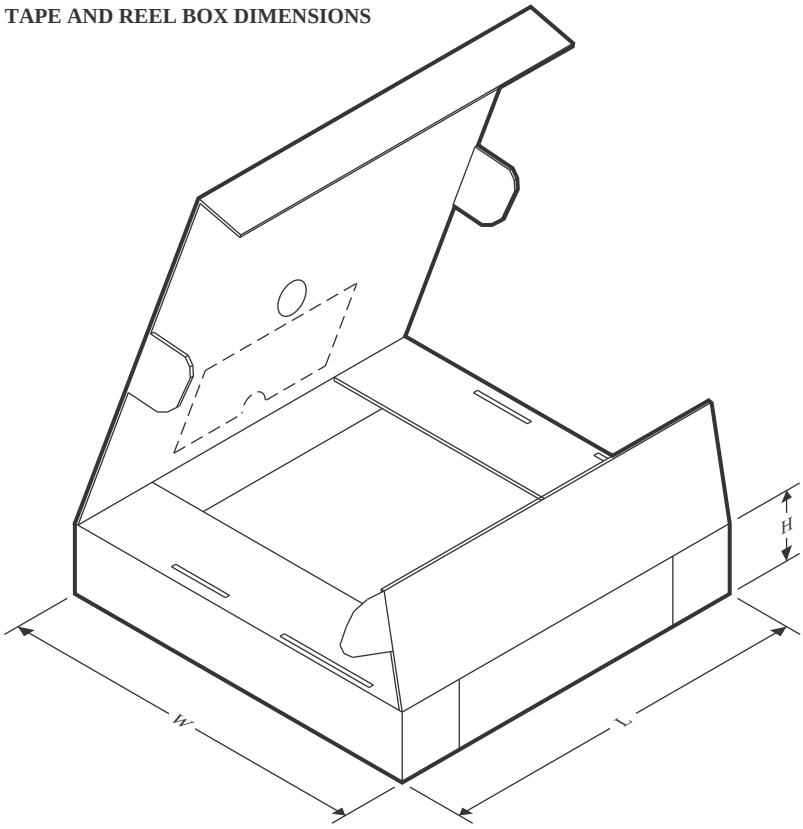
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5001IDRQ1	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5001MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5001SD/NOPB	WSON	NGT	8	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5001SDE/NOPB	WSON	NGT	8	250	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5001SDX/NOPB	WSON	NGT	8	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

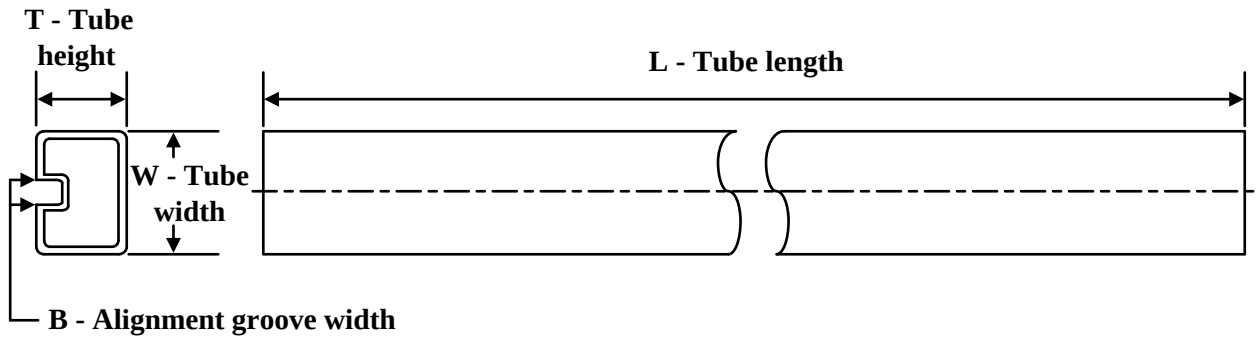
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5001IDRQ1	SOIC	D	8	2500	367.0	367.0	35.0
LM5001MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM5001SD/NOPB	WSON	NGT	8	1000	208.0	191.0	35.0
LM5001SDE/NOPB	WSON	NGT	8	250	208.0	191.0	35.0
LM5001SDX/NOPB	WSON	NGT	8	4500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

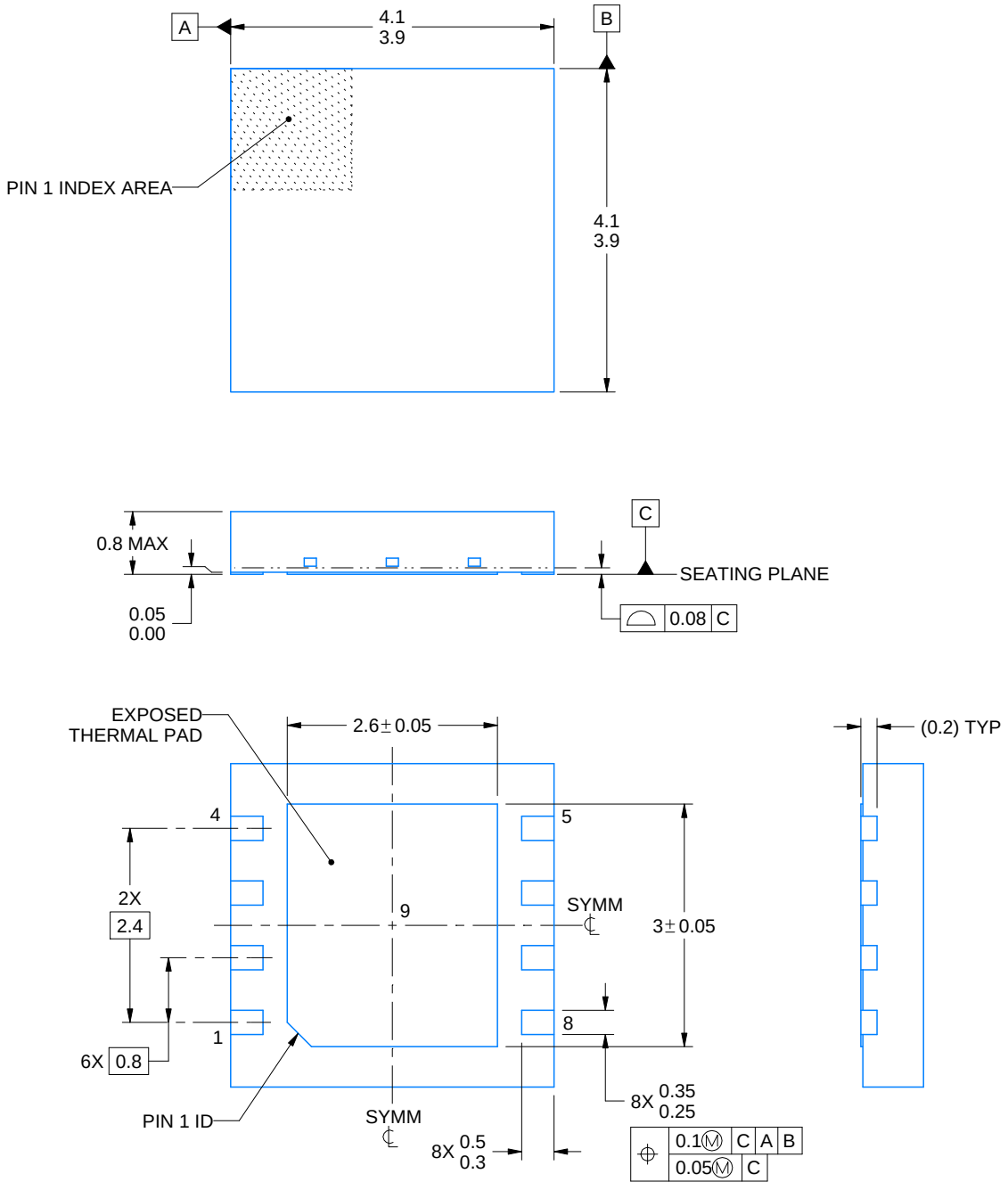
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM5001IDQ1	D	SOIC	8	95	495	8	4064	3.05
LM5001IDQ1.Z	D	SOIC	8	95	495	8	4064	3.05
LM5001MA/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM5001MA/NOPB.Z	D	SOIC	8	95	495	8	4064	3.05

PACKAGE OUTLINE

NGT0008A

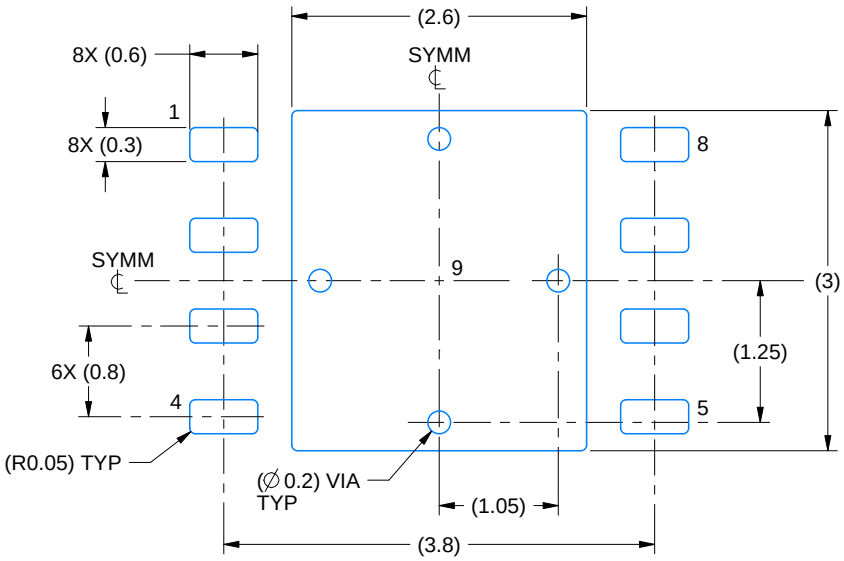
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

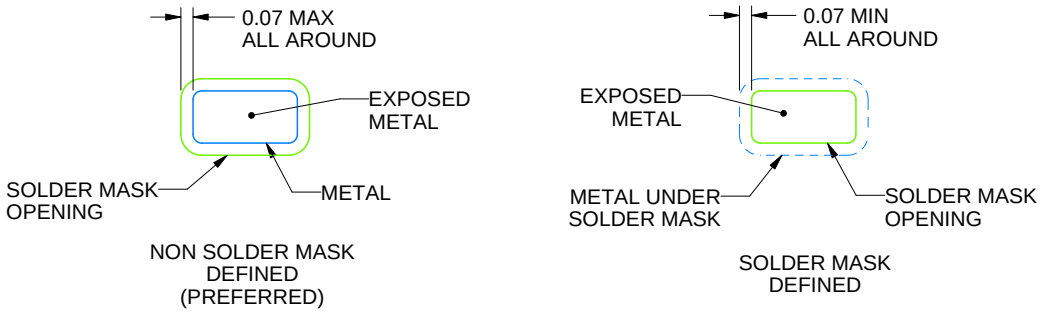


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

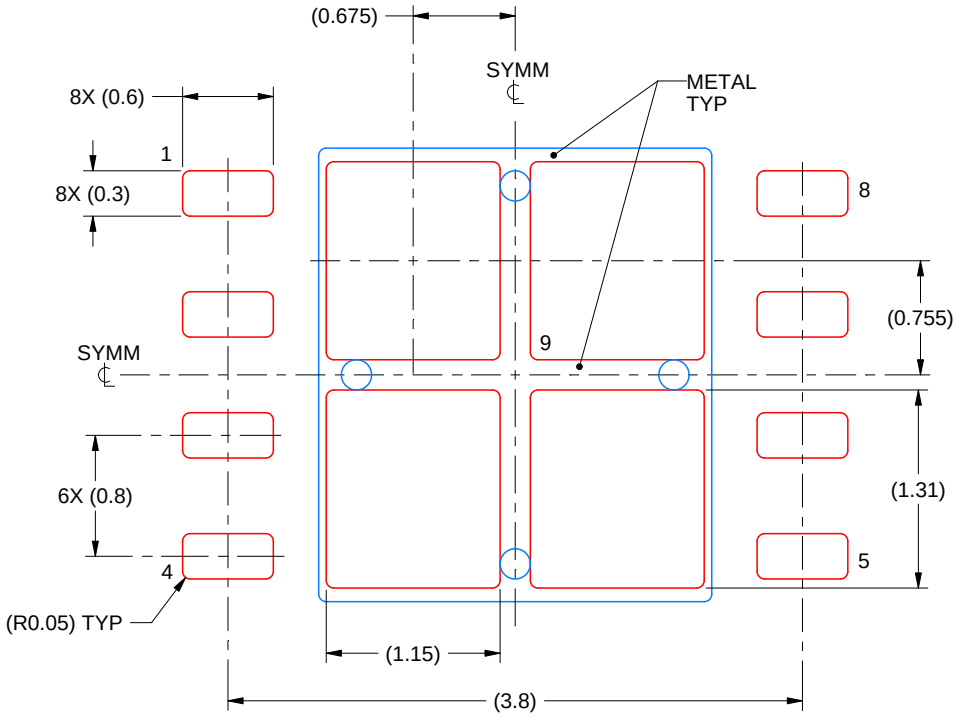


SOLDER MASK DETAILS

4214935/A 08/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



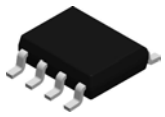
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4214935/A 08/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

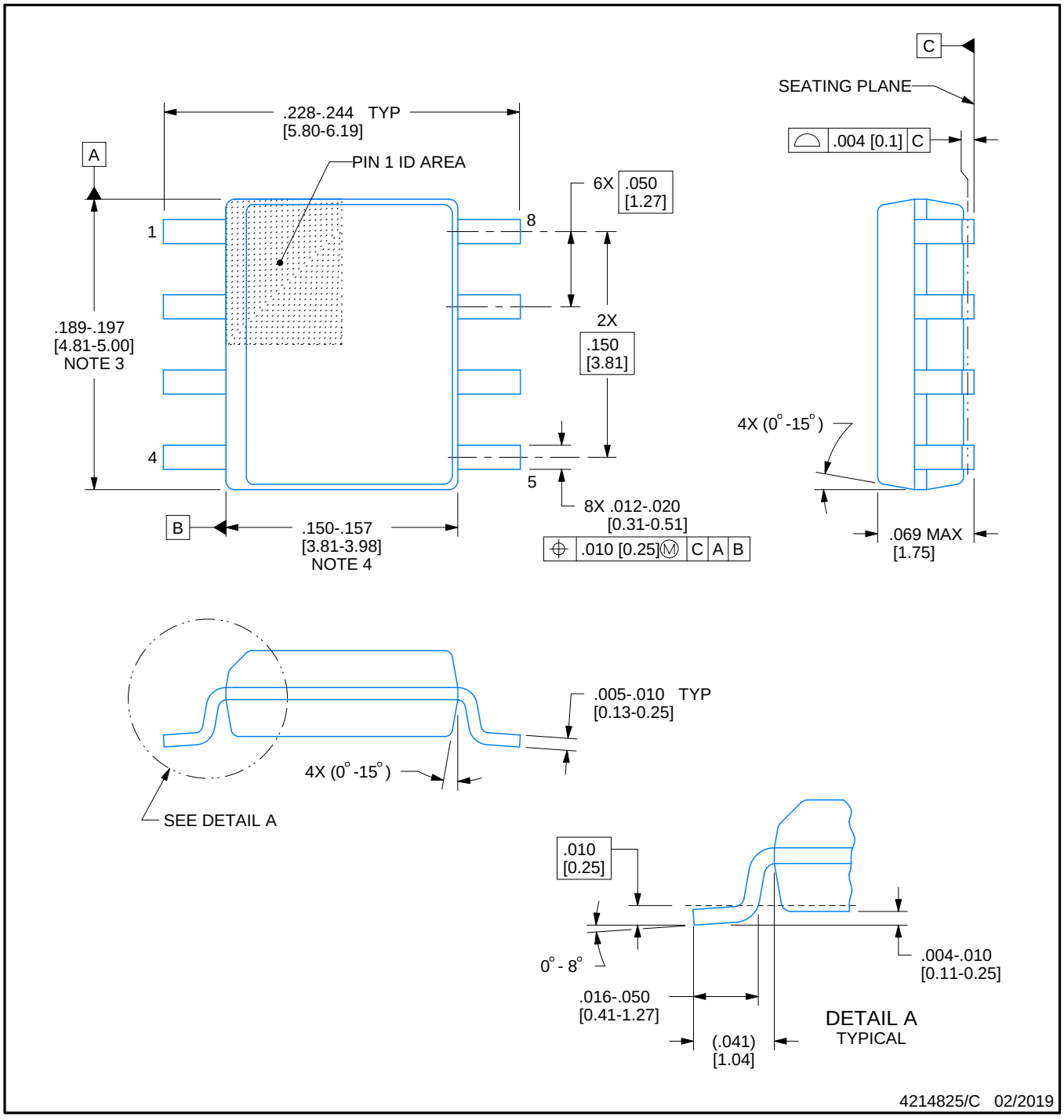


PACKAGE OUTLINE

D0008A

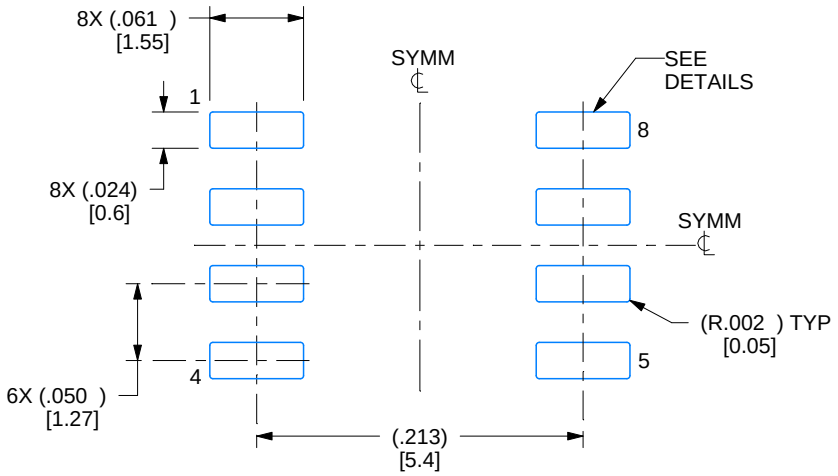
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

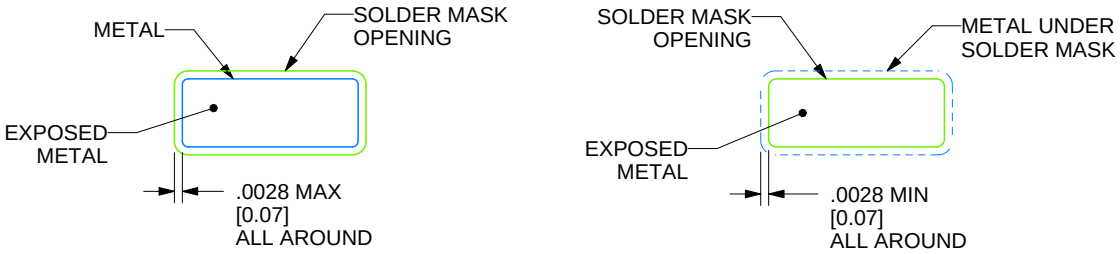


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

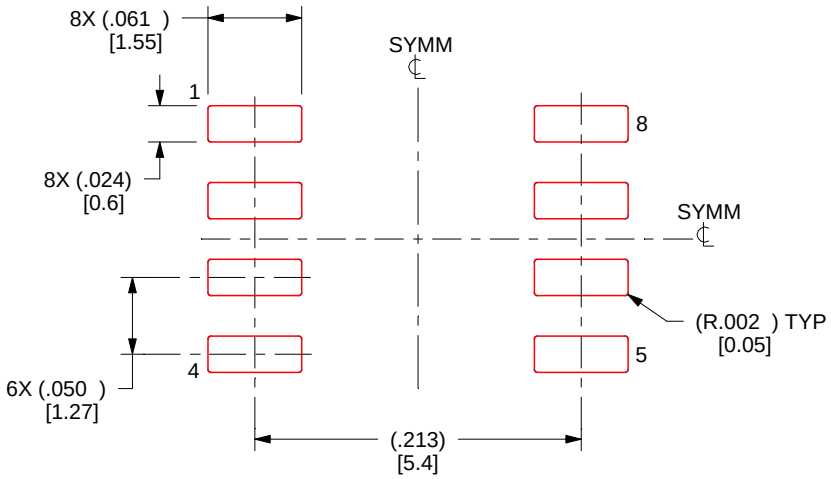
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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