LM4819 Boomer® Audio Power Amplifier Series
350mW Audio Power Amplifier with Shutdown Mode

Check for Samples: LM4819, LM4819MBD

FEATURES

- **WSON, SOIC, and VSSOP Surface Mount Packaging**
- **Switch On/Off Click Suppression**
- **Unity-Gain Stable**
- **Minimum External Components**

KEY SPECIFICATIONS

- **THD+N at 1kHz, 350mW Continuous Average Output Power into 16Ω: 10% (max)**
- **THD+N at 1kHz, 300mW Continuous Average Output Power into 8Ω: 10% (max)**
- **Shutdown Current: 0.7µA (typ)**

APPLICATIONS

- **General Purpose Audio**
- **Portable Electronic Devices**
- **Information Appliances (IA)**

DESCRIPTION

The LM4819 is a mono bridged power amplifier that is capable of delivering 350mW$_{RMS}$ output power into a 16Ω load or 300mW$_{RMS}$ output power into an 8Ω load with 10% THD+N from a 5V power supply.

The LM4819 Boomer audio power amplifier is designed specifically to provide high quality output power and minimize PCB area with surface mount packaging and a minimal amount of external components. Since the LM4819 does not require output coupling capacitors, bootstrap capacitors or snubber networks, it is optimally suited for low-power portable applications.

The closed loop response of the unity-gain stable LM4819 can be configured using external gain-setting resistors. The device is available in WSON, VSSOP, and SOIC package types to suit various applications.

Typical Application

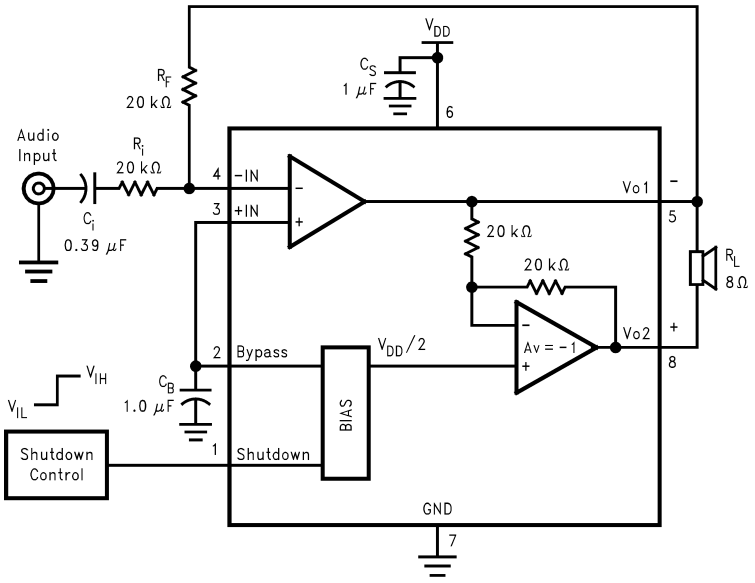


Figure 1. Typical Audio Amplifier Application Circuit

Connection Diagrams

Top View

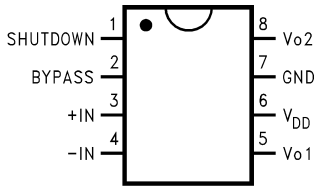


Figure 2. Small Outline (SOIC) Package
See Package Number D0008A

Top View

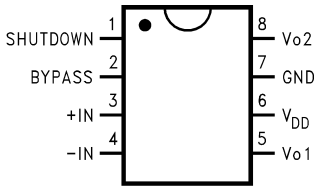


Figure 3. Mini Small Outline (VSSOP) Package
See Package Number DGK0008A

Top View

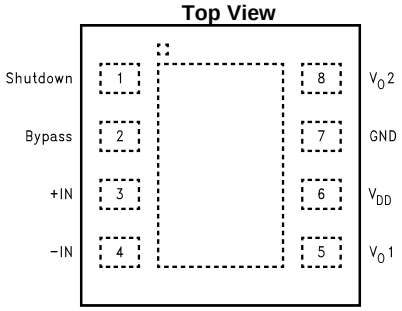


Figure 4. WSON Package
See Package Number NGL0008B

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)(3)

Supply Voltage			6.0V
Storage Temperature			−65°C to +150°C
Input Voltage			−0.3V to V_{DD} +0.3V
Power Dissipation (P_D)(4)			Internally Limited
ESD Susceptibility(5)			3.5kV
ESD Susceptibility(6)			250V
Junction Temperature (T_J)			150°C
Soldering Information	Small Outline Package	Vapor Phase (60 seconds)	215°C
		Infrared (15 seconds)	220°C
Thermal Resistance		θ_{JC} (VSSOP)	56°C/W
		θ_{JA} (VSSOP)	210°C/W
		θ_{JC} (SOIC)	35°C/W
		θ_{JA} (SOIC)	170°C/W
		θ_{JA} (WSON)	117°C/W(7)
		θ_{JA} (WSON)	150°C/W(8)

(1) All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given. However, the typical value is a good indication of device's performance.
(3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(4) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX}–T_A)/\theta_{JA}$. For the LM4819, T_{JMAX} = 150°C and the typical junction-to-ambient thermal resistance (θ_{JA}) when board mounted is 210°C/W for the VSSOP package and 170°C/W for the SOIC package.
(5) Human body model, 100pF discharged through a 1.5 kΩ resistor.
(6) Machine Model, 220pF–240pF capacitor is discharged through all pins.
(7) The given θ_{JA} is for an LM4819 package in an NGL0008B with the Exposed-DAP soldered to a printed circuit board copper pad with an area equivalent to that of the Exposed-DAP itself. The Exposed-DAP of the NGL0008B package should be electrically connected to GND or an electrically isolated copper area.
(8) The given θ_{JA} is for an LM4819 package in an NGL0008B with the Exposed-DAP not soldered to any printed circuit board copper.

Operating Ratings(1)(2)

Temperature Range $T_{MIN} \le T_A \le T_{MAX}$	−40°C ≤ T_A ≤ 85°C
Supply Voltage	2.0V ≤ V_{CC} ≤ 5.5V

(1) All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given. However, the typical value is a good indication of device's performance.

Electrical Characteristics V_{DD} = 5V(1)(2)

The following specifications apply for V_{DD} = 5V, R_L = 16Ω unless otherwise stated. Limits apply for T_A = 25°C.

Parameter		Test Conditions	LM4819		Units (Limits)
			Typical(3)	Limit(4)(5)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_o = 0A	1.5	3.0	mA (max)
I_{SD}	Shutdown Current	V_{PIN1} = V_{DD}(6)	1.0	5.0	µA (max)
V_{SDIH}	Shutdown Voltage Input High			4.0	V (min)
V_{SDIL}	Shutdown Voltage Input Low			1.0	V (max)
V_{OS}	Output Offset Voltage	V_{IN} = 0V	5	50	mV (max)
P_O	Output Power	THD = 10%, f_{IN} = 1kHz	350		mW
		THD = 10%, f_{IN} = 1kHz, R_L = 8Ω	300		mW
THD+N	Total Harmonic Distortion + Noise	P_O = 270mW_{RMS}, A_{VD} = 2, f_{IN} = 1kHz	1		%

(1) All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given. However, the typical value is a good indication of device's performance.
(3) Typical specifications are specified at 25°C and represent the parametric norm.
(4) Tested limits are specified to TI's AOQL (Average Outgoing Quality Level).
(5) Datasheet min/max specification limits are specified by designs, test, or statistical analysis.
(6) The shutdown pin (pin1) should be driven as close as possible to V_{DD} for minimum current in Shutdown Mode.

Electrical Characteristics V_{DD} = 3V(1)(2)

The following specifications apply for V_{DD} = 3V and R_L = 16Ω load unless otherwise stated. Limits apply to T_A = 25°C.

Parameter		Test Conditions	LM4819		Units (Limits)
			Typical(3)	Limit(4)(5)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_o = 0A	1.0	3.0	mA (max)
I_{SD}	Shutdown Current	V_{PIN1} = V_{DD}(6)	0.7	5.0	µA (max)
V_{SDIH}	Shutdown Voltage Input High			2.4	V (min)
V_{SDIL}	Shutdown Voltage Input Low			0.6	V (max)
V_{OS}	Output Offset Voltage	V_{IN} = 0V	5	50	mV
P_O	Output Power	THD = 10%, f_{IN} = 1kHz	110		mW
		THD = 10%, f_{IN} = 1kHz, R_L = 8Ω	90		mW
THD+N	Total Harmonic Distortion + Noise	P_O = 80mW_{RMS}, A_{VD} = 2, f_{IN} = 1kHz	1		%

(1) All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given. However, the typical value is a good indication of device's performance.
(3) Typical specifications are specified at 25°C and represent the parametric norm.
(4) Tested limits are specified to TI's AOQL (Average Outgoing Quality Level).
(5) Datasheet min/max specification limits are specified by designs, test, or statistical analysis.
(6) The shutdown pin (pin1) should be driven as close as possible to V_{DD} for minimum current in Shutdown Mode.

External Components Description

(See Figure 1)

Components		Functional Description
1.	R_i	Combined with R_f, this inverting input resistor sets the closed-loop gain. R_i also forms a high pass filter with C_i at $f_c = 1/(2\pi R_i C_i)$.
2.	C_i	This input coupling capacitor blocks DC voltage at the amplifier's terminals. Combined with R_i, it creates a high pass filter with R_i at $f_c = 1/(2\pi R_i C_i)$. Refer to the section, Proper Selection of External Components for an explanation of how to determine the value of C_i.
3.	R_f	Combined with R_i, this is the feedback resistor that sets the closed-loop gain: $A_v = 2(R_F/R_i)$.
4.	C_S	This is the power supply bypass capacitor that filters the voltage applied to the power supply pin. Refer to the Application Information section for proper placement and selection of C_s.
5.	C_B	This is the bypass pin capacitor that filters the voltage at the BYPASS pin. Refer to the section, Proper Selection of External Components, for information concerning proper placement and selection of C_B.

Typical Performance Characteristics

THD+N vs Frequency

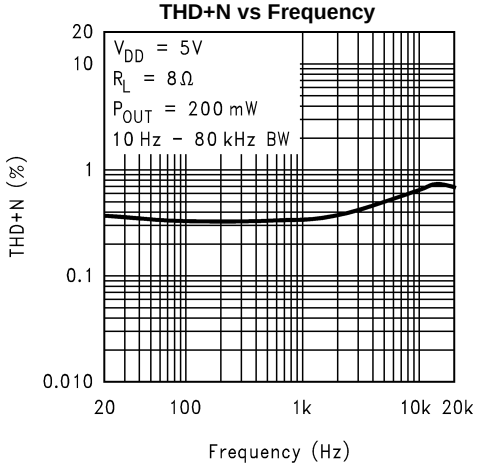


Figure 5.

THD+N vs Frequency

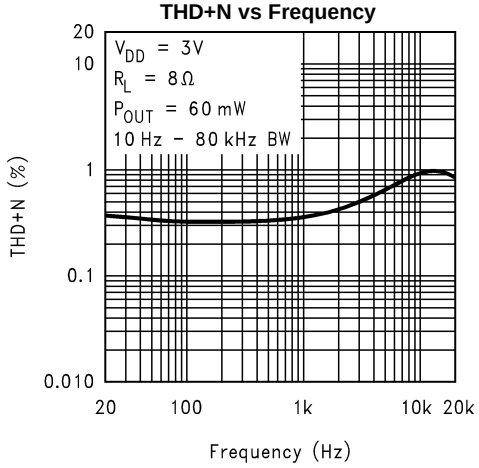


Figure 6.

THD+N vs Frequency

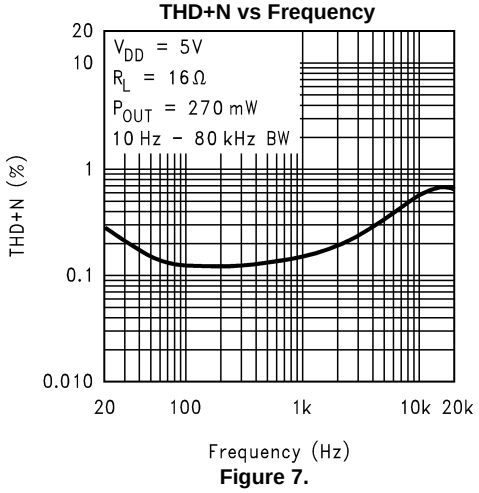


Figure 7.

THD+N vs Frequency

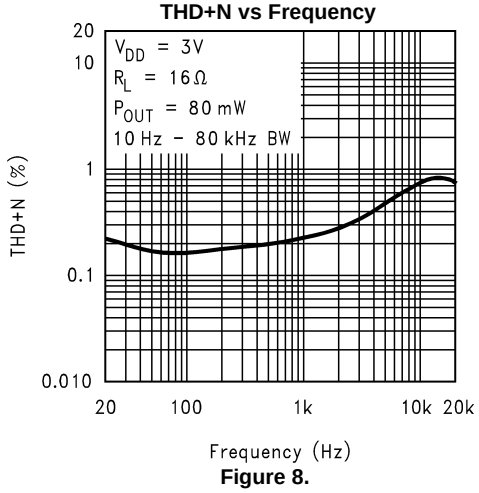


Figure 8.

THD+N vs Frequency

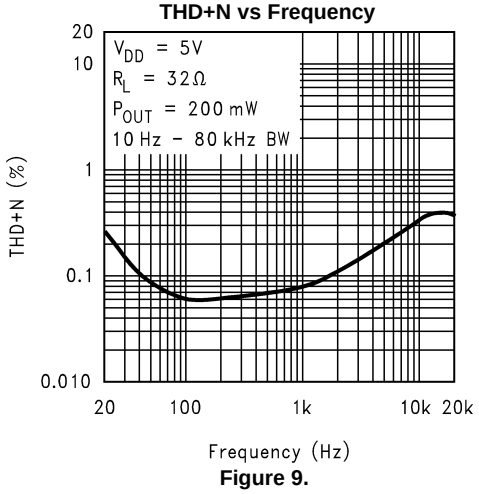


Figure 9.

THD+N vs Frequency

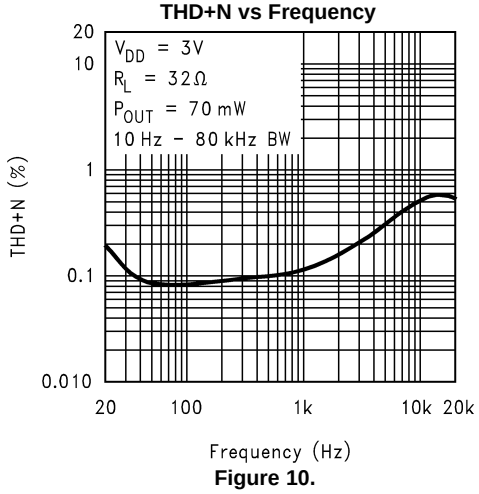


Figure 10.

Typical Performance Characteristics (continued)

THD+N vs Output Power

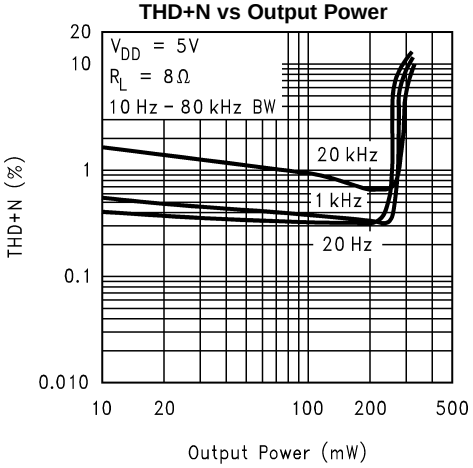


Figure 11.

THD+N vs Output Power

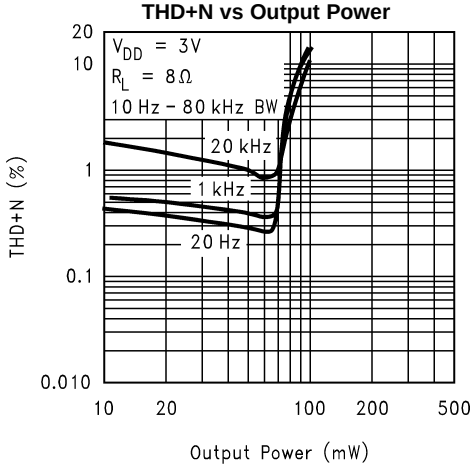


Figure 12.

THD+N vs Output Power

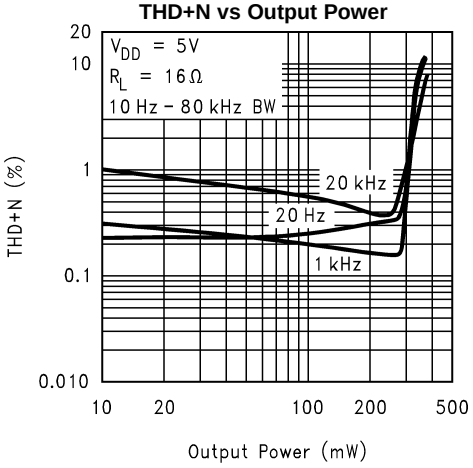


Figure 13.

THD+N vs Output Power

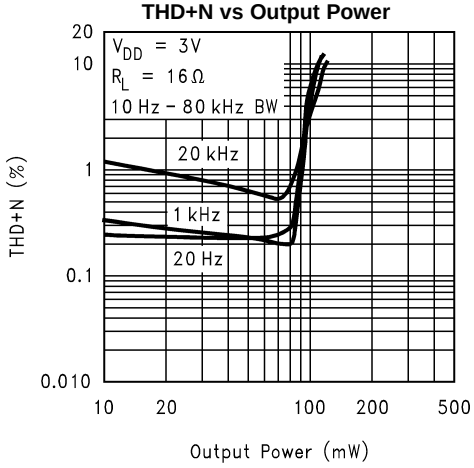


Figure 14.

THD+N vs Output Power

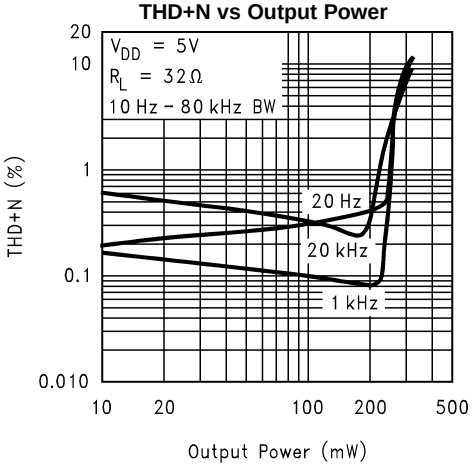


Figure 15.

THD+N vs Output Power

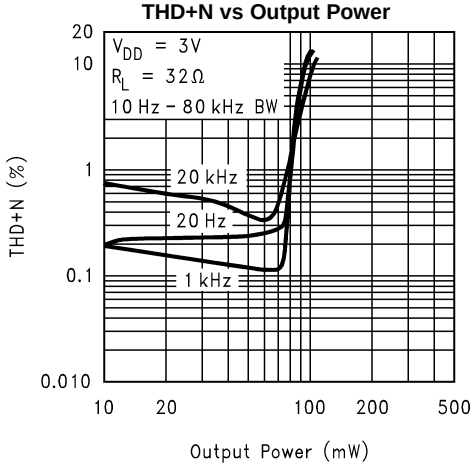


Figure 16.

Typical Performance Characteristics (continued)

Output Power vs Supply Voltage
R_L = 8Ω

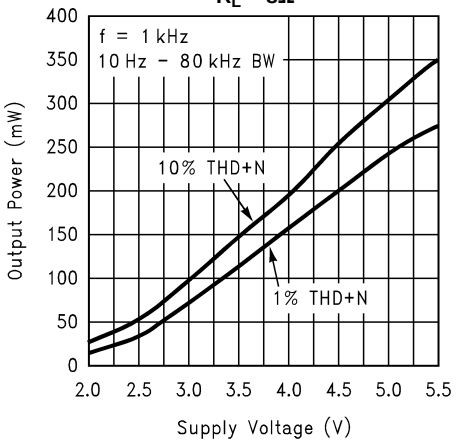


Figure 17.

Output Power vs Supply Voltage
R_L = 16Ω

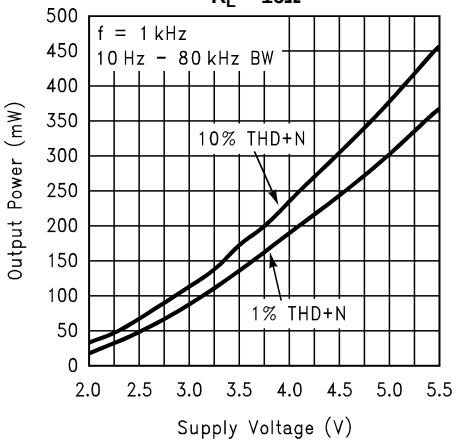


Figure 18.

Output Power vs Supply Voltage
R_L = 32Ω

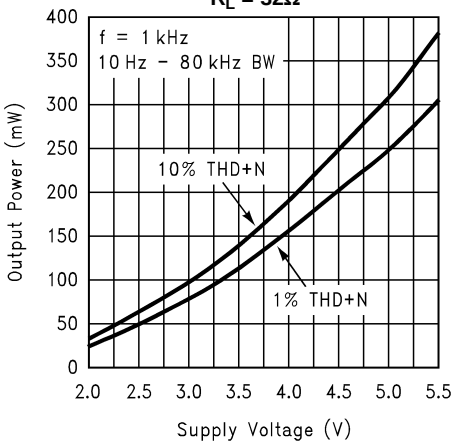


Figure 19.

Output Power vs Load Resistance

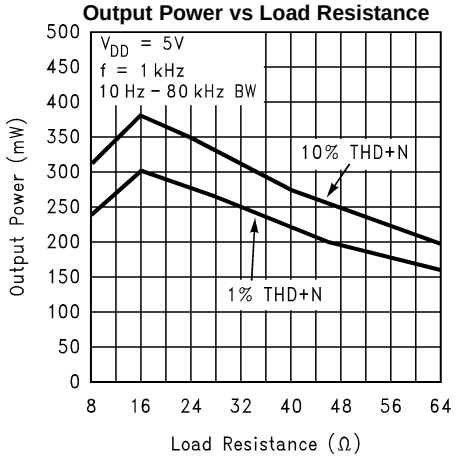


Figure 20.

Power Dissipation vs Output Power
V_{DD} = 5V

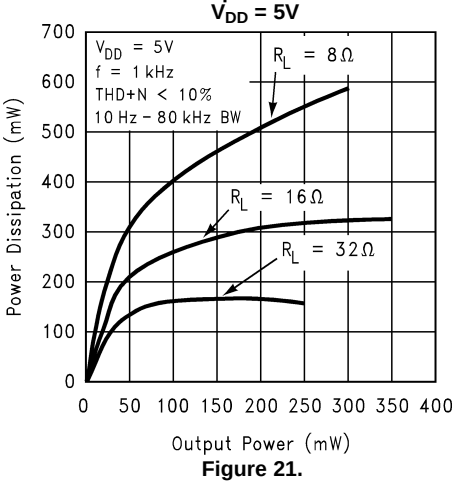


Figure 21.

Power Dissipation vs Output Power
V_{DD} = 3V

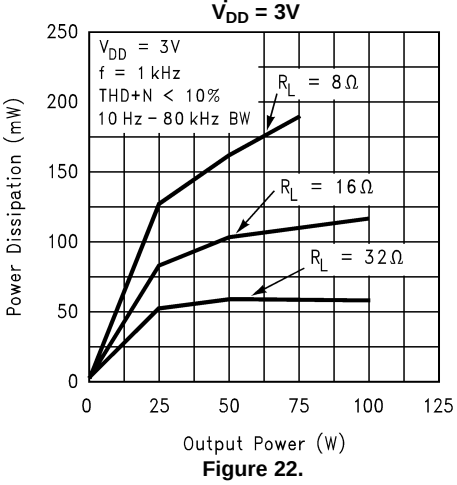


Figure 22.

Typical Performance Characteristics (continued)

Power Derating Curves

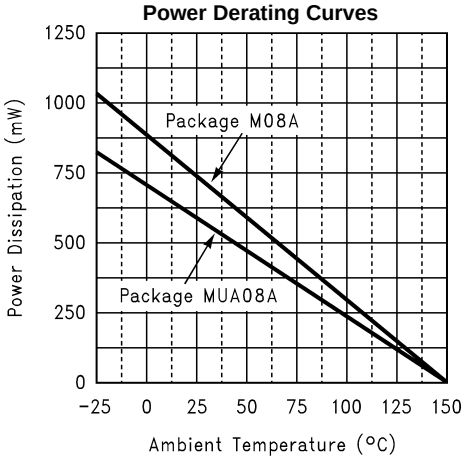


Figure 23.

Frequency Response vs Input Capacitor Size

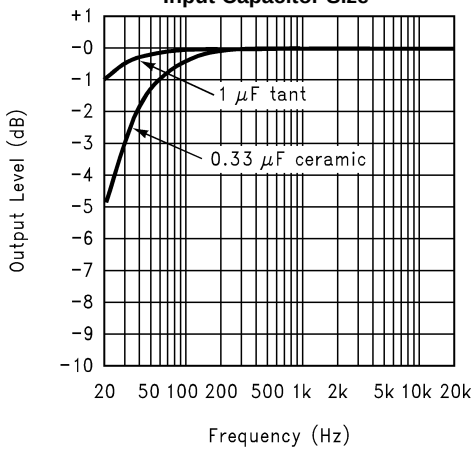


Figure 24.

Supply Current vs Supply Voltage

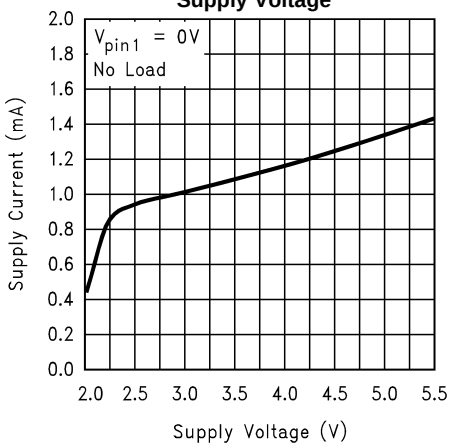


Figure 25.

APPLICATION INFORMATION

BRIDGE CONFIGURATION EXPLANATION

As shown in Figure 1, the LM4819 consists of two operational amplifiers. External resistors, R_i and R_F set the closed-loop gain of the first amplifier (and the amplifier overall), whereas two internal 20kΩ resistors set the second amplifier's gain at -1. The LM4819 is typically used to drive a speaker connected between the two amplifier outputs.

Figure 1 shows that the output of Amp1 servers as the input to Amp2, which results in both amplifiers producing signals identical in magnitude but 180° out of phase. Taking advantage of this phase difference, a load is placed between V_{01} and V_{02} and driven differentially (commonly referred to as "bridge mode"). This results in a differential gain of

$$A_{VD} = 2 * (R_f / R_i) \quad (1)$$

Bridge mode is different from single-ended amplifiers that drive loads connected between a single amplifier's output and ground. For a given supply voltage, bridge mode has a distinct advantage over the single-ended configuration: its differential output doubles the voltage swing across the load. This results in four times the output power when compared to a single-ended amplifier under the same conditions. This increase in attainable output assumes that the amplifier is not current limited or the output signal is not clipped. To ensure minimum output signal clipping when choosing an amplifier's closed-loop gain, refer to the Audio Power Amplifier Design Example section.

Another advantage of the differential bridge output is no net DC voltage across the load. This results from biasing V_{01} and V_{02} at half-supply. This eliminates the coupling capacitor that single supply, single-ended amplifiers require. Eliminating an output coupling capacitor in a single-ended configuration forces a single supply amplifier's half-supply bias voltage across the load. The current flow created by the half-supply bias voltage increases internal IC power dissipation and may permanently damage loads such as speakers.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful bridged or single-ended amplifier. Equation 2 states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified load.

$$P_{DMAX} = (V_{DD})^2 / (2\pi^2 R_L) \text{ (W) Single-ended} \quad (2)$$

However, a direct consequence of the increased power delivered to the load by a bridged amplifier is an increase in the internal power dissipation point for a bridge amplifier operating at the same given conditions. Equation 3 states the maximum power dissipation point for a bridged amplifier operating at a given supply voltage and driving a specified load.

$$P_{DMAX} = 4(V_{DD})^2 / (2\pi^2 R_L) \text{ (W) Bridge Mode} \quad (3)$$

The LM4819 has two operational amplifiers in one package and the maximum internal power dissipation is four times that of a single-ended amplifier. However, even with this substantial increase in power dissipation, the Lm4819 does not require heatsinking. From Equation 3, assuming a 5V power supply and an 8Ω load, the maximum power dissipation point is 633mW. The maximum power dissipation point obtained from Equation 3 must not exceed the power dissipation predicted by Equation 4:

$$P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA} \text{ (W)} \quad (4)$$

For the micro DGK0008A package, θ_{JA} = 210°C/W, for the D0008A package, θ_{JA} = 170°C/W , and T_{JMAX} = 150°C for the LM4819. For a given ambient temperature, T_A, Equation 4 can be used to find the maximum internal power dissipation supported by the IC packaging. If the result of Equation 3 is greater than the result of Equation 4, then decrease the supply voltage, increase the load impedance, or reduce the ambient temperature. For a typical application using the D0008A packaged LM4819 with a 5V power supply and an 8Ω load, the maximum ambient temperature that does not violate the maximum junction temperature is approximately 42°C. If a DGK0008A packaged part is used instead with the same supply voltage and load, the maximum ambient temperature is 17°C. In both cases, it is assumed that a device is a surface mount part operating around the maximum power dissipation point. The assumption that the device is operating around the maximum power dissipation point is incorrect for an 8Ω load. The maximum power dissipation point occurs when the output power is equal to the maximum power dissipation or 50% efficiency. The LM4819 is not capable of the output power level (633mW) required to operate at the maximum power dissipation point for an 8Ω load. To find the maximum power dissipation, the graph Figure 22 must be used. From the graph, the maximum power dissipation for an 8Ω

load and a 5V supply is approximately 575mW. Substituting this value back into Equation 4 for P_{DMAX} and using θ_{JA} = 210°C/W for the DGK0008A package, the maximum ambient temperature is calculated to be 29°C. Using θ_{JA} = 170°C/W for the D0008A package, the maximum ambient temperature is 52°C. Refer to the Typical Performance Characteristics curves for power dissipation information for lower output powers and maximum power dissipation for each package at a given ambient temperature.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitors connected to the bypass and power supply pins should be placed as close to the LM4819 as possible. The capacitor connected between the bypass pin and ground improves the internal bias voltage's stability, producing improved PSRR. The improvements to PSRR increase as the bypass pin capacitor value increases. Typical applications employ a 5V regulator with 10µF and 0.1µF filter capacitors that aid in supply stability. Their presence, however, does not eliminate the need for bypassing the supply nodes of the LM4819. The selection of bypass capacitor values, especially C_B , depends on desired PSRR requirements, click and pop performance as explained in the section, Proper Selection of External Components, as well as system cost and size constraints.

SHUTDOWN FUNCTION

The voltage applied to the LM4819's SHUTDOWN pin controls the shutdown function. Activate micro-power shutdown by applying V_{DD} to the SHUTDOWN pin. When active, the LM4819's micro-power shutdown feature turns off the amplifier's bias circuitry, reducing the supply current. The logic threshold is typically $1/2V_{DD}$. The low 0.7µA typical shutdown current is achieved by applying a voltage that is as near as V_{DD} as possible to the SHUTDOWN pin. A voltage that is less than V_{DD} may increase the shutdown current. Avoid intermittent or unexpected micro-power shutdown by ensuring that the SHUTDOWN pin is not left floating but connected to either V_{DD} or GND.

There are a few ways to activate micro-power shutdown. These included using a single-pole, single-throw switch, a microcontroller, or a microprocessor. When using a switch, connect an external 10kΩ to 100kΩ pull-up resistor between the SHUTDOWN pin and V_{DD}. Connect the switch between the SHUTDOWN pin and ground. Select normal amplifier operation by closing the switch. Opening the switch connects the shutdown pin to V_{DD} through the pull-up resistor, activating micro-power shutdown. The switch and resistor ensure that the SHUTDOWN pin will not float. This prevents unwanted state changes. In a system with a microprocessor or a microcontroller, use a digital output to apply the control voltage to the SHUTDOWN pin. Driving the SHUTDOWN pin with active circuitry eliminates the pull-up resistor

PROPER SELECTION OF EXTERNAL COMPONENTS

Optimizing the LM4819's performance requires properly selecting external components. Though the LM4819 operates well when using external components with wide tolerances, best performance is achieved by optimizing component values.

The LM4819 is unity gain stable, giving the designer maximum design flexibility. The gain should be set to no more than a given application requires. This allows the amplifier to achieve minimum THD+N and maximum signal-to-noise ratio. These parameters are compromised as the closed-loop gain increases. However, low gain demands input signals with greater voltage swings to achieve maximum output power. Fortunately, many signal sources such as audio CODECs have outputs of $1V_{RMS}$ ($2.83V_{P-P}$). Please refer to the Audio Power Amplifier Design section for more information on selecting the proper gain.

Another important consideration is the amplifier's close-loop bandwidth. To a large extent, the bandwidth is dictated by the choice of external components shown in Figure 1. The input coupling capacitor, C_i, forms a first order high pass filter that limits low frequency response. This value should be chosen based on needed frequency response for a few distinct reasons discussed below

Input Capacitor Value Selection

Amplifying the lowest audio frequencies requires a high value input coupling capacitor (C_i in Figure 1). A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150Hz. Applications using speakers with limited frequency response reap little improvement by using a large input capacitor.

Besides affecting system cost and size, C_i has an effect on the LM4819's click and pop performance. When the supply voltage is first applied, a transient (pop) is created as the charge on the input capacitor changes from zero to a quiescent state. The magnitude of the pop is directly proportional to the input capacitor's value. Higher value capacitors need more time to reach a quiescent DC voltage (usually 1/2 V_{DD}) when charged with a fixed current. The amplifier's output charges the input capacitor through the feedback resistor, R_F. Thus, selecting an input capacitor value that is no higher than necessary to meet the desired -3dB frequency can minimize pops.

As shown in Figure 1, the input resistor (R_i) and the input capacitor, C_i produce a -3dB high pass filter cutoff frequency that is found using Equation 5.

$$f_{-3dB} = 1/(2\ \pi R_i C_i)\ (Hz) \quad (5)$$

As an example when using a speaker with a low frequency limit of 150Hz, C_i, using Equation 5 is 0.063µF. The 0.39µF C_i shown in Figure 1 allows the LM4819 to drive a high efficiency, full range speaker whose response extends down to 20Hz.

Besides optimizing the input capacitor value, the bypass capacitor value, C_B requires careful consideration. The bypass capacitor's value is the most critical to minimizing turn-on pops because it determines how fast the LM4819 turns on. The slower the LM4819's outputs ramp to their quiescent DC voltage (nominally 1/2V_{DD}), the smaller the turn-on pop. While the device will function properly (no oscillations or motorboating), with C_B less than 1.0µF, the device will be much more susceptible to turn-on clicks and pops. Thus, a value of C_B equal to or greater than 1.0µF is recommended in all but the most cost sensitive designs.

Bypass Capacitor Value Selection

Besides minimizing the input capacitor size, careful consideration should be paid to the value of C_B, the capacitor connected to the BYPASS pin. Since C_B determines how fast the LM4819 settles to quiescent operation, its value is critical when minimizing turn-on pops. The slower the LM4819's outputs ramp to their quiescent DC voltage (nominally 1/2V_{DD}), the smaller the turn-on pop. Choosing C_B equal to 1.0µF along with a small value of C_i (in the range of 0.1µF to 0.39µF) produces a click-less and pop-less shutdown function. As discussed above, choosing C_i no larger than necessary for the desired bandwidth helps minimize clicks and pops.

Optimizing Click and Pop Reduction Performance

The LM4819 contains circuitry that minimizes turn-on and shutdown transients or "clicks and pops". For this discussion, turn on refers to either applying the power or supply voltage or when the shutdown mode is deactivated. While the power supply is ramping to it's final value, the LM4819's internal amplifiers are configured as unity gain buffers. An internal current source charges the voltage of the bypass capacitor, C_B, connected to the BYPASS pin in a controlled, linear manner. Ideally, the input and outputs track the voltage charging on the bypass capacitor. The gain of the internal amplifiers remains unity until the bypass capacitor is fully charged to 1/2V_{DD}. As soon as the voltage on the bypass capacitor is stable, the device becomes fully operational. Although the BYPASS pin current cannot be modified, changing the size of the bypass capacitor, C_B, alters the device's turn-on time and magnitude of "clicks and pops". Increasing the value of C_B reduces the magnitude of turn-on pops. However, this presents a tradeoff: as the size of C_B increases, the turn-on time (Ton) increases. There is a linear relationship between the size of C_B and the turn on time. Below are some typical turn-on times for various values of C_B:

C_B	T_{ON}
0.01µF	20ms
0.1µF	200ms
0.22µF	440ms
0.47µF	940ms
1.0µF	2S

In order to eliminate "clicks and pops", all capacitors must be discharged before turn-on. Rapidly switching V_{DD} may not allow the capacitors to fully discharge, which may cause "clicks and pops".

AUDIO POWER AMPLIFIER DESIGN EXAMPLE

The following are the desired operational parameters:

Given:

Power Output	100mW
Load Impedance	16Ω
Input Level	1Vrms (max)
Input Impedance	20kΩ
Bandwidth	100Hz–20kHz ± 0.25dB

The design begins by specifying the minimum supply voltage necessary to obtain the specified output power. To find this minimum supply voltage, use the Output Power vs. Supply Voltage graph in the Typical Performance Characteristics section. From the graph for a 16Ω load, (graphs are for 8Ω, 16Ω, and 32Ω loads) the supply voltage for 100mW of output power with 1% THD+N is approximately 3.15 volts.

Additional supply voltage creates the benefit of increased headroom that allows the LM4819 to reproduce peaks in excess of 100mW without output signal clipping or audible distortion. The choice of supply voltage must also not create a situation that violates maximum dissipation as explained above in the Power Dissipation section. For example, if a 3.3V supply is chosen for extra headroom then according to Equation 3 the maximum power dissipation point with a 16Ω load is 138mW. Using Equation 4 the maximum ambient temperature is 121°C for the DGK0008A package and 126°C for the D0008A package.

After satisfying the LM4819's power dissipation requirements, the minimum differential gain is found using Equation 6.

$$A_{VD} \geq \sqrt{(P_O R_L)}/(V_{IN}) = V_{orms}/V_{inrms} \quad (6)$$

Thus a minimum gain of 1.27 V/V allows the LM4819 to reach full output swing and maintain low noise and THD+N performance. For this example, let A_{VD} = 1.27. The amplifier's overall gain is set using the input (R_i) and feedback (R_F) resistors. With the desired input impedance set to 20kΩ, the feedback resistor is found using Equation 7.

$$R_F/R_i = A_{VD}/2 \text{ (V/V)} \quad (7)$$

The value of R_F is 13kΩ.

The last step in this design example is setting the amplifier's -3dB frequency bandwidth. To achieve the desired ±0.25dB pass band magnitude variation limit, the low frequency response must extend to at least one-fifth the lower bandwidth limit and the high frequency response must extend to at least five times the upper bandwidth limit. The gain variation for both response limits is 0.17dB, well with in the ±0.25dB desired limit.

The results are:

f_L = 100Hz/5 = 20Hz

f_H = 20 kHz*5 = 100kHz

As mentioned in the External Components section, R_i and C_i create a high pass filter that sets the amplifier's lower band pass frequency limit. Find the coupling capacitor's value using Equation 8.

$$C_i \geq 1/(2\pi R_i f_c) \text{ (F)} \quad (8)$$

$C_i \geq 0.398\mu F$, a standard value of 0.39µF will be used. The product of the desired high frequency cutoff (100kHz in this example) and the differential gain, A_{VD}, determines the upper pass band response limit. With A_{VD} = 1.27 and f_H = 100kHz, the closed-loop gain bandwidth product (GBWP) is 127kHz. This is less than the LM4819's 900kHz GBWP. With this margin the amplifier can be used in designs that require more differential gain while avoiding performance restricting bandwidth limitations.

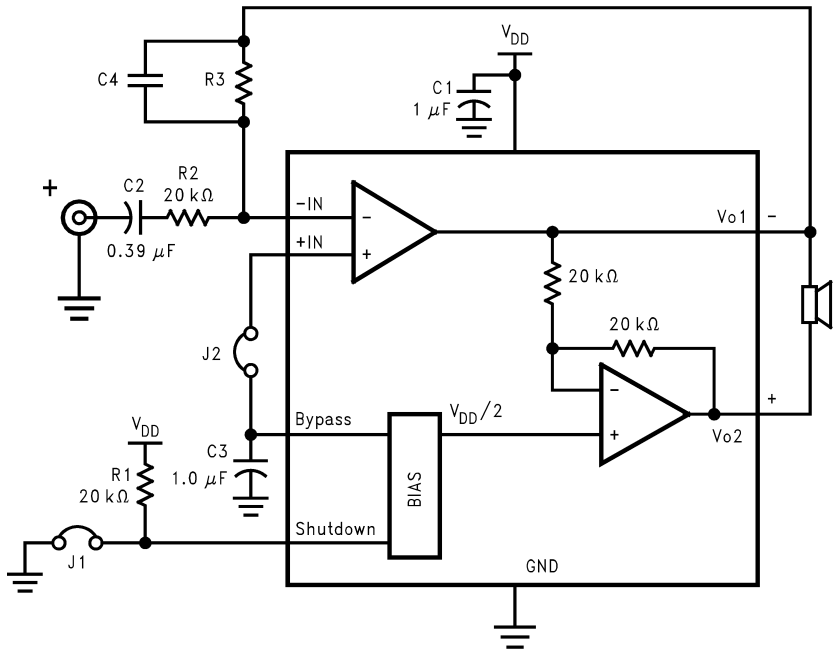


Figure 26. Higher Gain Audio Amplifier

The LM4819 is unity-gain stable and requires no external components besides gain-setting resistors, an input coupling capacitor, and proper supply bypassing in the typical application. However, if a closed-loop differential gain of greater than 10 is required, a feedback capacitor (C_4) may be needed as shown in Figure 26 to bandwidth limit the amplifier. This feedback capacitor creates a low pass filter that eliminates possible high frequency oscillations. Care should be taken when calculating the -3dB frequency in that an incorrect combination of R_3 and C_4 will cause rolloff before 20kHz. A typical combination of feedback resistor and capacitor that will not produce audio band high frequency rolloff is R_3 = 20kΩ and C_4 = 25pF. These components result in a -3dB point of approximately 320 kHz. It is not recommended that the feedback resistor and capacitor be used to implement a band limiting filter below 100kHz.

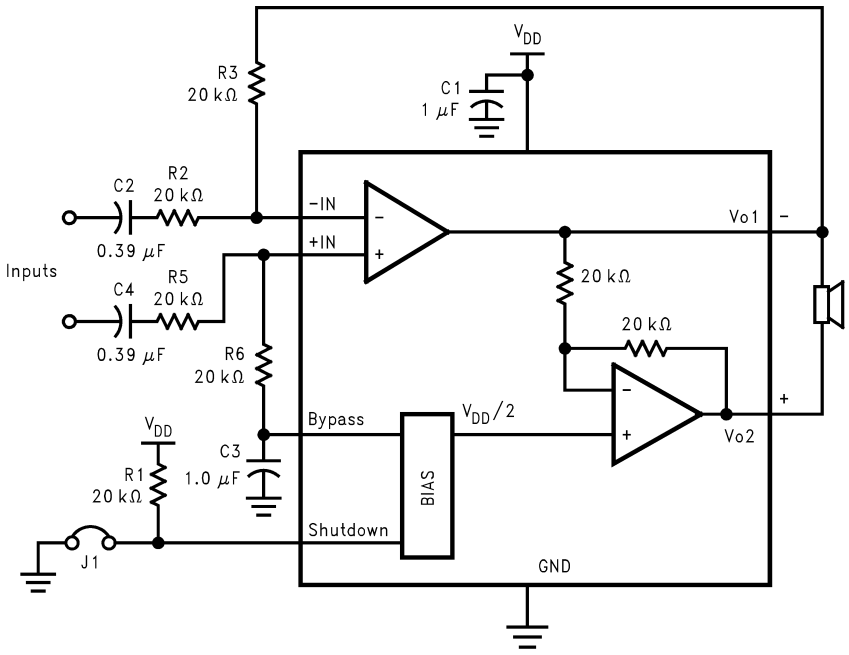


Figure 27. Differential Amplifier Configuration for LM4819

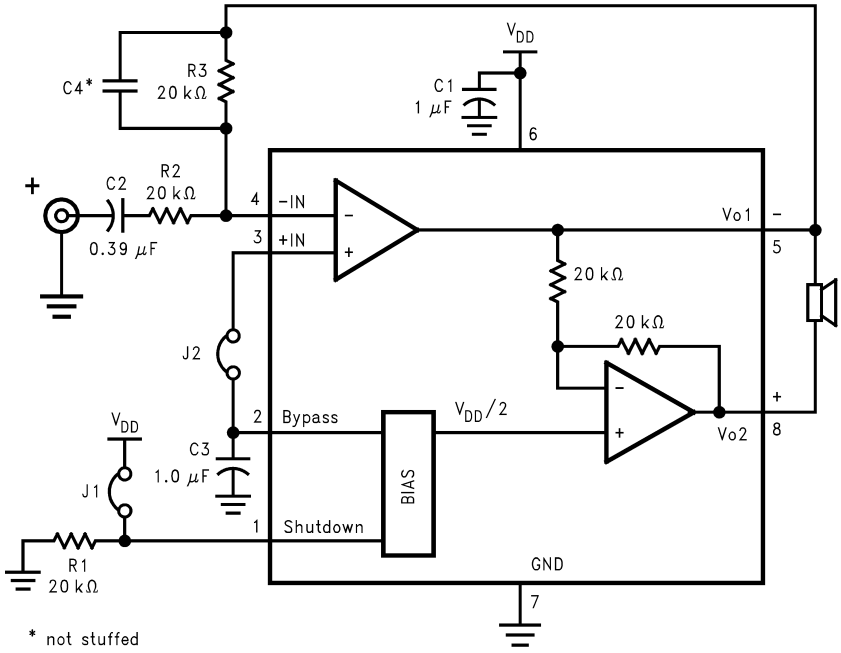


Figure 28. Reference Design Board and PCB Layout Guidelines

LM4819 SOIC DEMO BOARD ARTWORK

Figure 29. Silk Screen

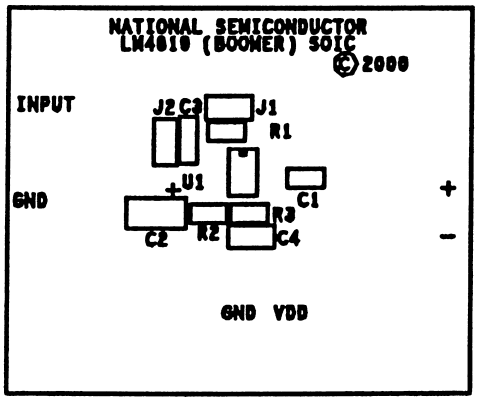


Figure 30. Top Layer

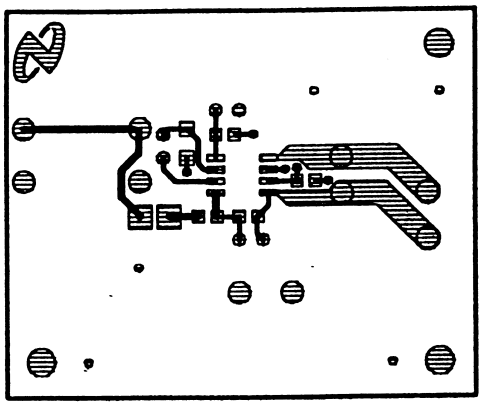
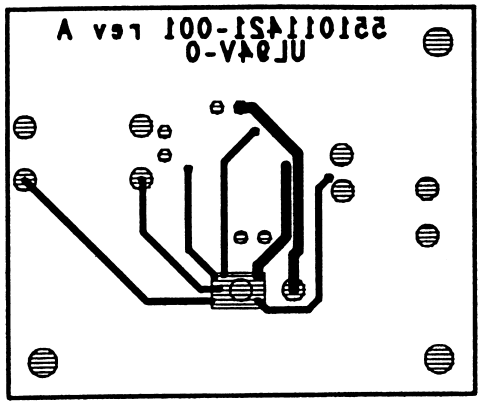


Figure 31. Bottom Layer



LM4819 VSSOP DEMO BOARD ARTWORK

Figure 32. Silk Screen

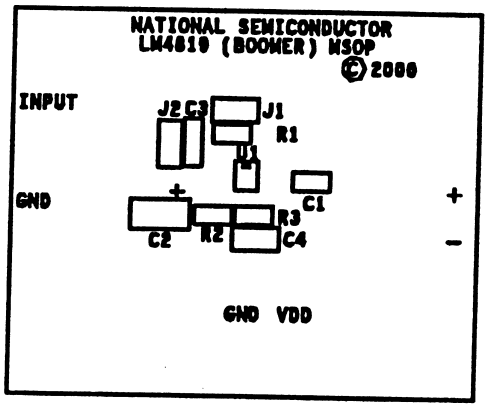


Figure 33. Top Layer

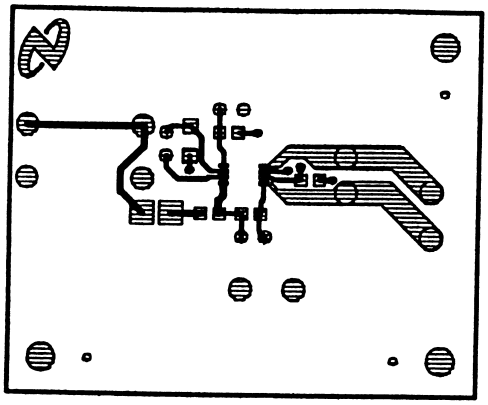
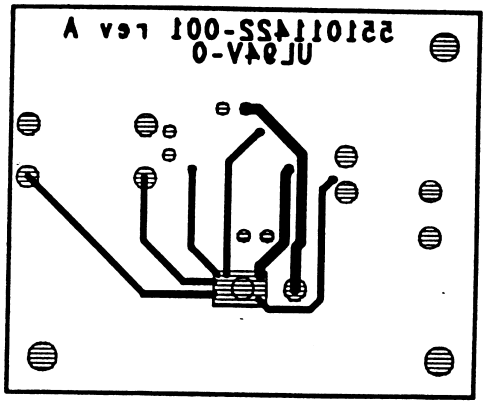
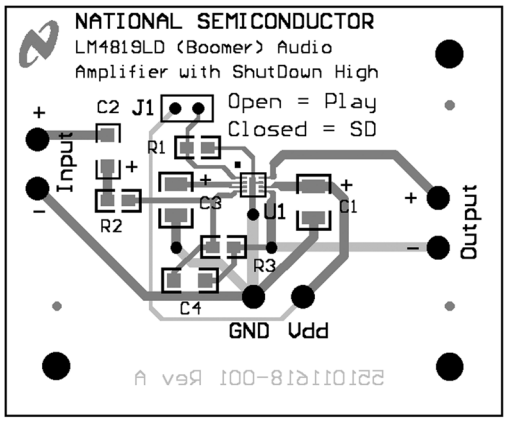


Figure 34. Bottom Layer

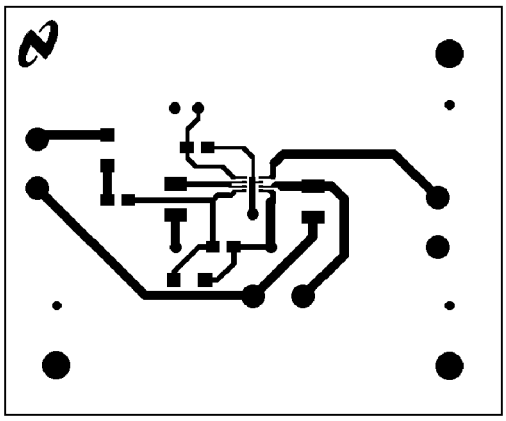


LM4819 WSON DEMO BOARD ARTWORK

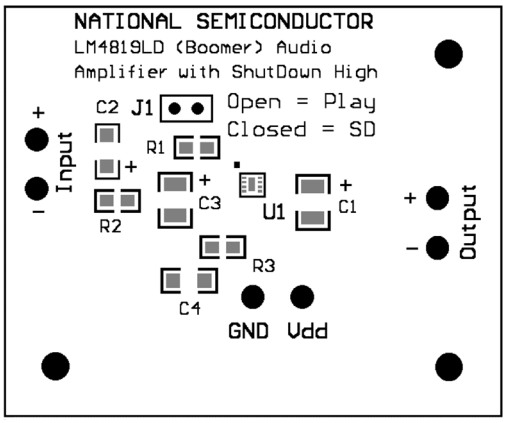
Composite View



Top Layer



Silk Screen



Bottom Layer

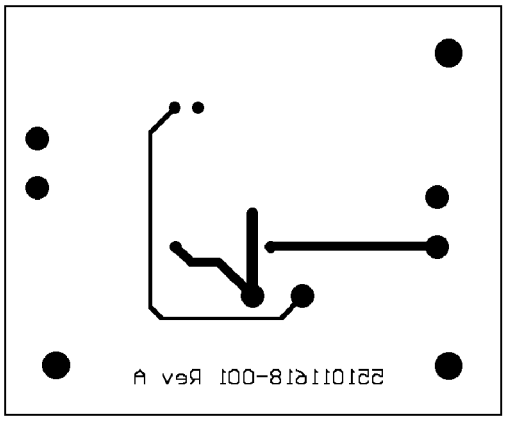


Table 1. Mono LM4819 Reference Design Boards
Bill of Material for all Demo Boards

Item	Part Number	Part Description	Qty	Ref Designator
1	551011208-001	LM4819 Mono Reference Design Board	1	
10	482911183-001	LM4819 Audio AMP	1	U1
20	151911207-001	Tant Cap 1uF 16V 10	1	C1

Table 1. Mono LM4819 Reference Design Boards
Bill of Material for all Demo Boards (continued)

Item	Part Number	Part Description	Qty	Ref Designator
21	151911207-002	Cer Cap 0.39uF 50V Z5U 20% 1210	1	C2
25	152911207-001	Tant Cap 1uF 16V 10	1	C3
30	472911207-001	Res 20K Ohm 1/10W 5	3	R1, R2, R3
35	210007039-002	Jumper Header Vertical Mount 2X1 0.100	2	J1, J2

PCB LAYOUT GUIDELINES

This section provides practical guidelines for mixed signal PCB layout that involves various digital/analog power and ground traces. Designers should note that these are only "rule-of-thumb" recommendations and the actual results will depend heavily on the final layout.

General Mixed Signal Layout Recommendation

Power and Ground Circuits

For two layer mixed signal design, it is important to isolate the digital power and ground trace paths from the analog power and ground trace paths. Star trace routing techniques (bringing individual traces back to a central point rather than daisy chaining traces together in a serial manner) can have a major impact on low level signal performance. Star trace routing refers to using individual traces to feed power and ground to each circuit or even device. This technique will take require a greater amount of design time but will not increase the final price of the board. The only extra parts required will be some jumpers.

Single-Point Power / Ground Connections

The analog power traces should be connected to the digital traces through a single point (link). A "Pi-filter" can be helpful in minimizing high frequency noise coupling between the analog and digital sections. It is further recommended to put digital and analog power traces over the corresponding digital and analog ground traces to minimize noise coupling.

Placement of Digital and Analog Components

All digital components and high-speed digital signals traces should be located as far away as possible from analog components and circuit traces.

Avoiding Typical Design / Layout Problems

Avoid ground loops or running digital and analog traces parallel to each other (side-by-side) on the same PCB layer. When traces must cross over each other do it at 90 degrees. Running digital and analog traces at 90 degrees to each other from the top to the bottom side as much as possible will minimize capacitive noise coupling and cross talk.

REVISION HISTORY

Changes from Revision C (March 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	18

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM4819LD/NOPB	Active	Production	WSON (NGL) | 8	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	G19
LM4819LD/NOPB.A	Active	Production	WSON (NGL) | 8	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	G19
LM4819MM/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	G19
LM4819MM/NOPB.A	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	G19
LM4819MMX/NOPB	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	G19
LM4819MMX/NOPB.A	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	G19
LM4819MX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM48 19M
LM4819MX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM48 19M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

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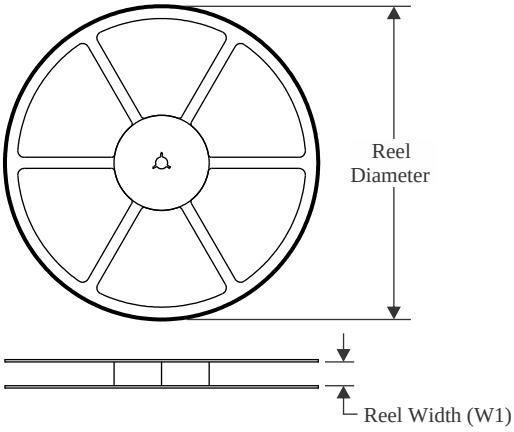
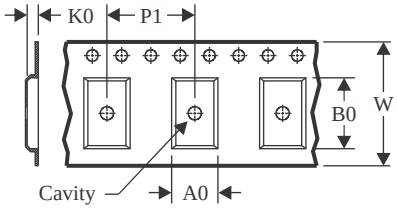
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

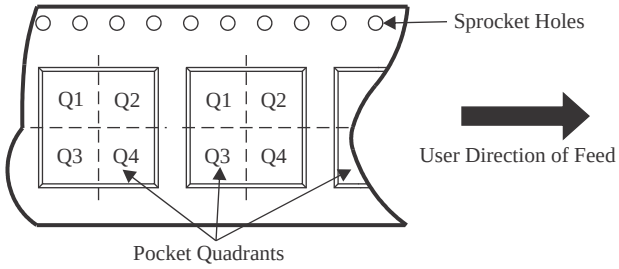


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

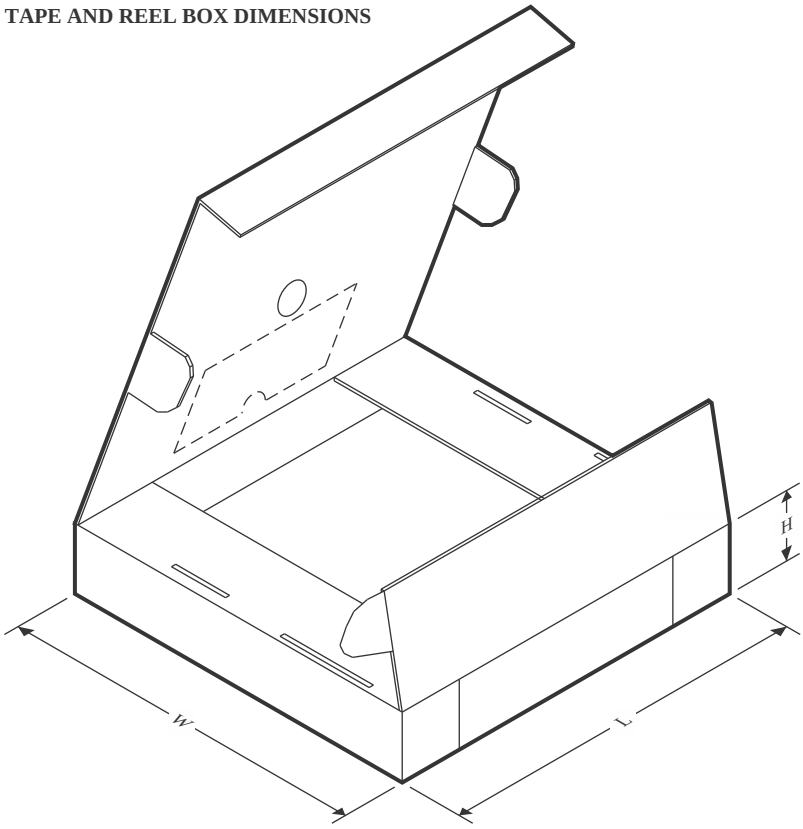
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4819LD/NOPB	WSON	NGL	8	1000	178.0	12.4	2.8	2.8	1.0	8.0	12.0	Q1
LM4819MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM4819MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM4819MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

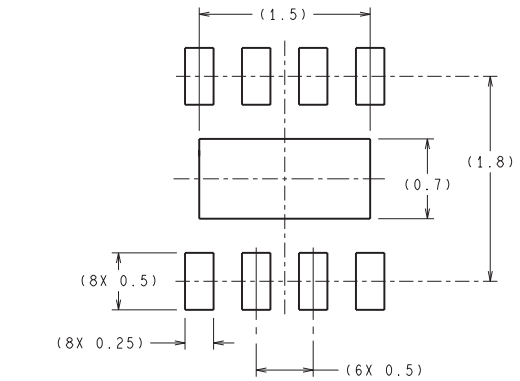
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

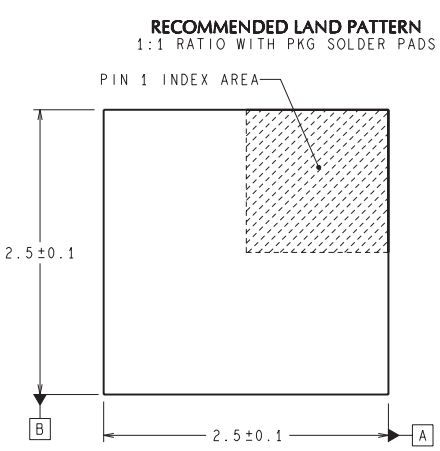
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4819LD/NOPB	WSON	NGL	8	1000	208.0	191.0	35.0
LM4819MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LM4819MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM4819MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

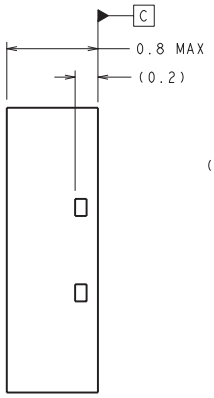
NGL0008B

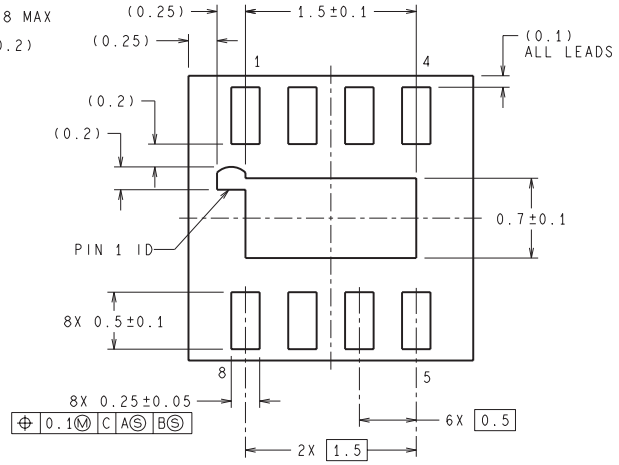


RECOMMENDED LAND PATTERN
1:1 RATIO WITH PKG SOLDER PADS

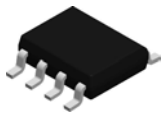
DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY







LDA08B (Rev B)

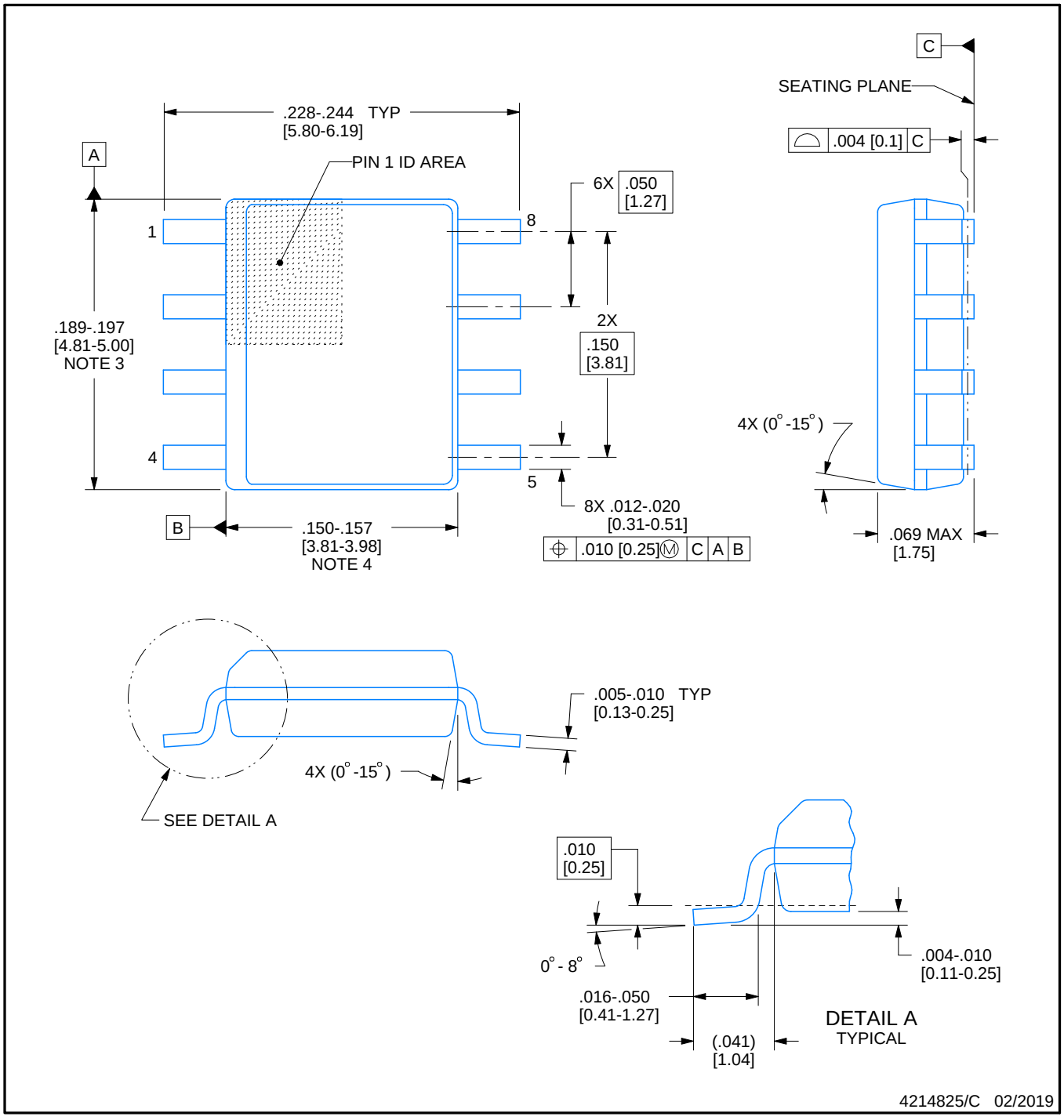


PACKAGE OUTLINE

D0008A

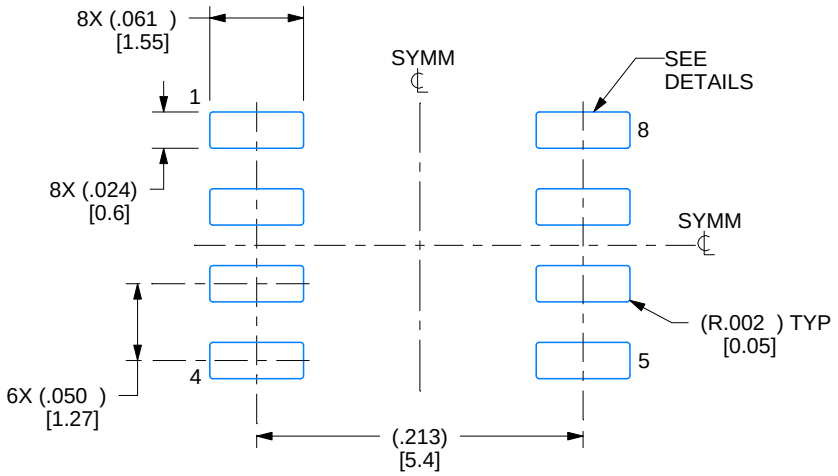
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

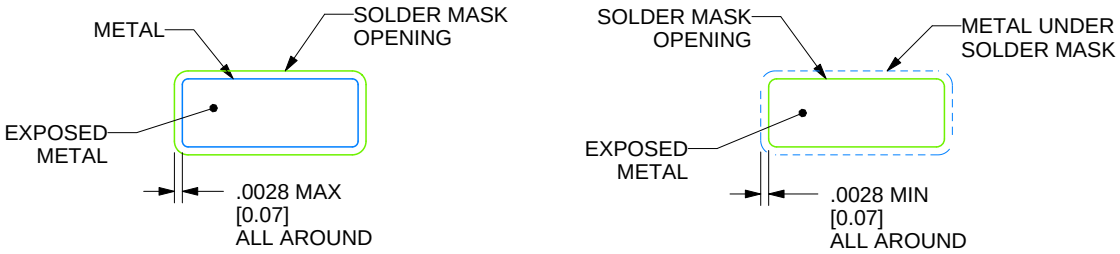


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

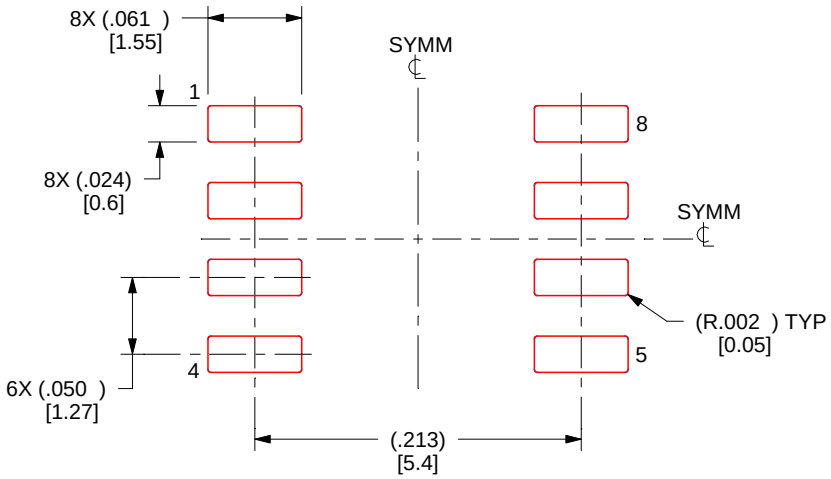
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

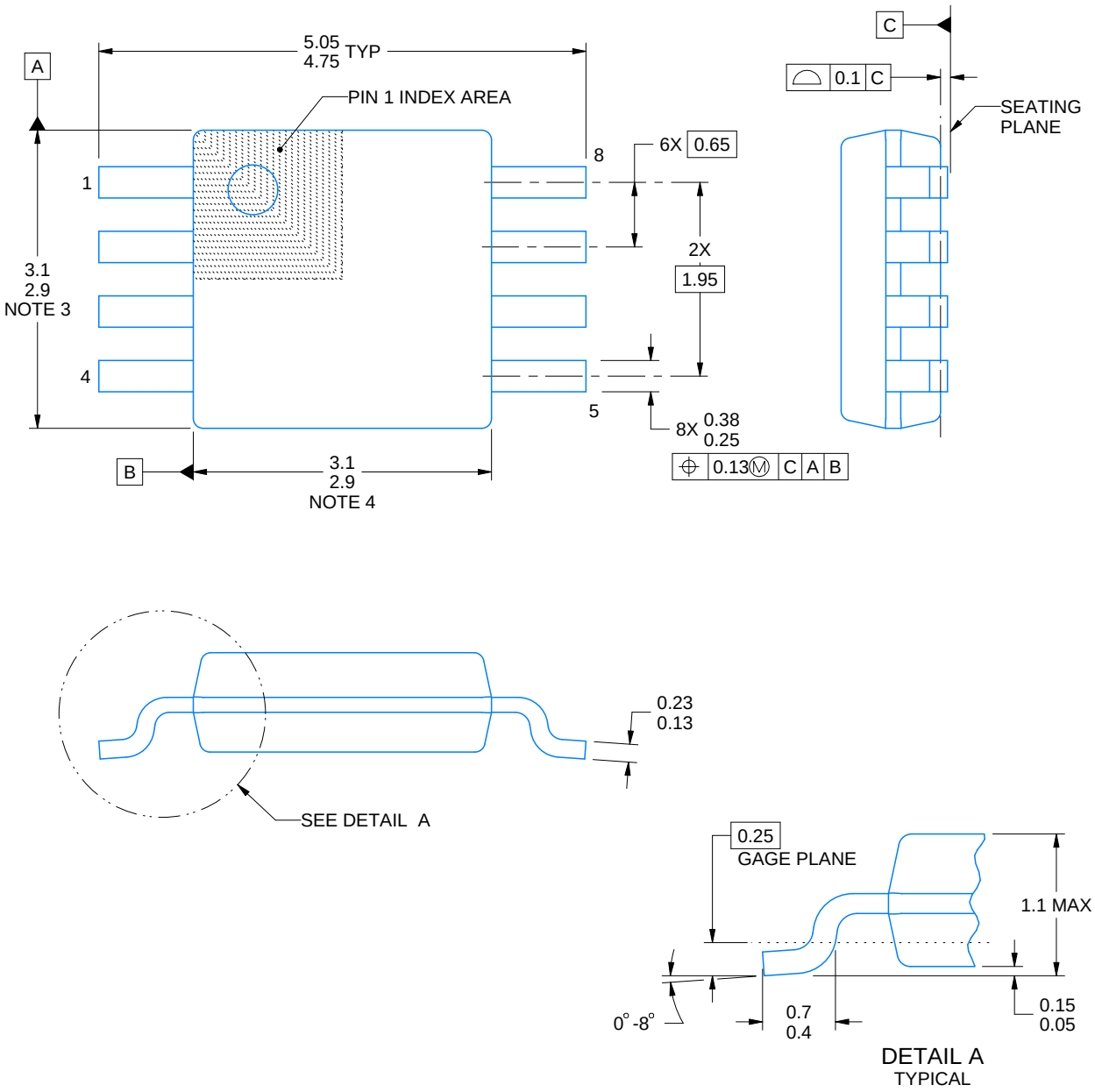
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

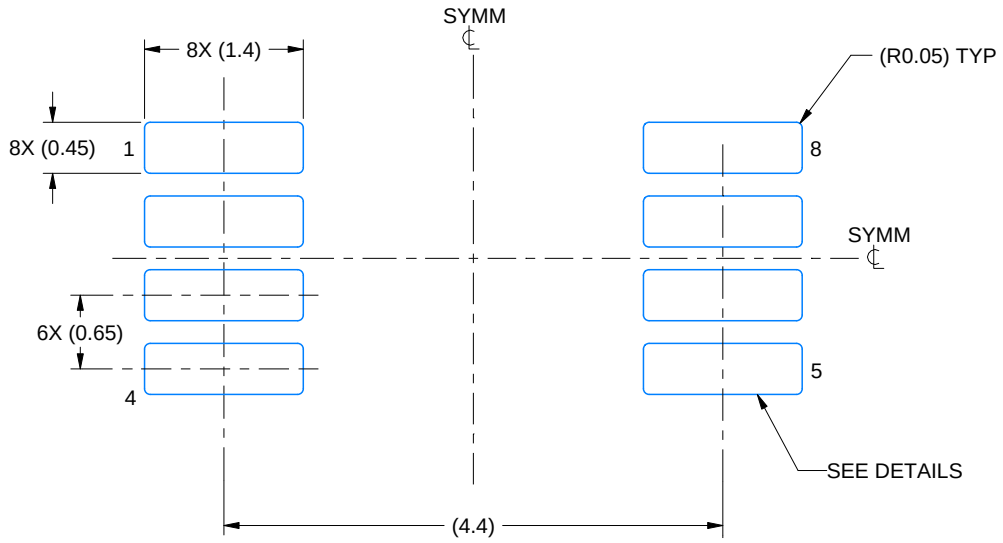
SMALL OUTLINE PACKAGE



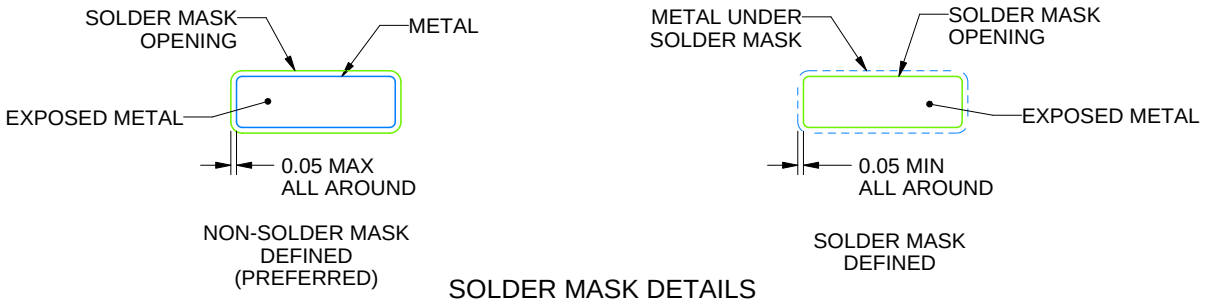
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

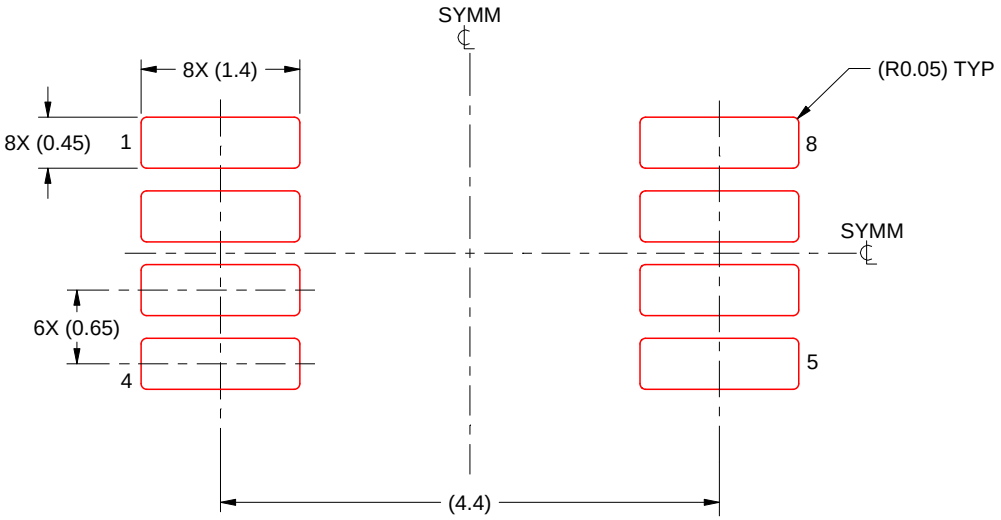


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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