

LM161/LM361 High Speed Differential Comparators

Check for Samples: LM161, LM361

FEATURES

- Independent strobes
- Ensured high speed: 20 ns max
- · Tight delay matching on both outputs
- Complementary TTL outputs
- Operates from op amp supplies: ±15V
- Low speed variation with overdrive variation
- Low input offset voltage
- Versatile supply voltage range

DESCRIPTION

The LM161/LM361 is a very high speed differential input, complementary TTL output voltage comparator with improved characteristics over the SE529/NE529 for which it is a pin-for-pin replacement. The device has been optimized for greater speed performance and lower input offset voltage. Typically delay varies only 3 ns for over-drive variations of 5 mV to 500 mV. It may be operated from op amp supplies (±15V).

Complementary outputs having maximum skew are provided. Applications involve high speed analog to digital converters and zero-crossing detectors in disk file systems.

CONNECTION DIAGRAMS

SOIC or PDIP Package

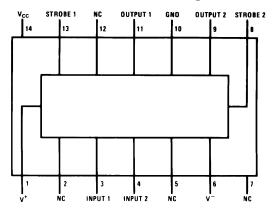


Figure 1. Top View Package Numbers D0014A, NFF0014A

TO-100 Package

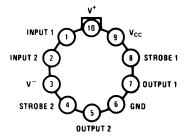


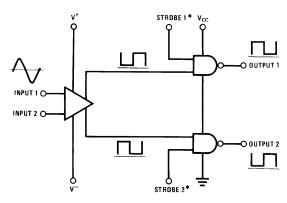
Figure 2. Package Number LME0010C

ATA.

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LOGIC DIAGRAM



*Output is low when current is drawn from strobe pin.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

+16V
-16V
+7V
+7V
±5V
±6V
600 mW
−65°C to +150°C
T _{MIN} T _{MAX}
−55°C to +125°C
−25°C to +85°C
0°C to +70°C
260°C
0.3V

⁽¹⁾ The device may be damaged by use beyond the maximum ratings.

Operating Conditions

			Min	Тур	Max
Complex Valtage V/t	LM161		5V		15V
Supply Voltage V ⁺	LM361		5V		15V
Cupply Valtage V	LM161		-6V		-15V
Supply Voltage V ⁻	LM361		-6V		-15V
Complex Valtage V	LM161		4.5V	5V	5.5V
Supply Voltage V _{CC}	LM361		4.75V	5V	5.25V
ESD Tolerance (1)	·				1600V
	PDIP Package	Soldering (10 seconds) ⁽²⁾			260°C
Soldering Information (2)	SOIC Package	Vapor Phase (60 seconds)			215°C
		Infrared (15 seconds)			220°C

⁽¹⁾ Human body model, $1.5 \text{ k}\Omega$ in series with 100 pF.

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⁽²⁾ See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.



Electrical Characteristics (1)(2)(1)

 $(V^{+} = +10V, V_{CC} = +5V, V^{-} = -10V, T_{MIN} \le T_{A} \le T_{MAX}, \text{ unless noted})$

Parameter	Conditions	Limits							
			LM161		LM361				
		Min	Тур	Max	Min	Тур	Max		
Input Offset Voltage			1	3		1	5	mV	
Input Bias Current	T _25°C		5			10		μΑ	
input bias Current	T _A =25°C			20			30	μA	
Input Offset Current	T _A =25°C		2			2		μΑ	
input Onset Current	1 _A =25 C			3			5	μΑ	
Voltage Gain	T _A =25°C		3			3		V/mV	
Input Resistance	T _A =25°C, f=1 kHz		20			20		kΩ	
Logical "1" Output Voltage	V_{CC} =4.75V, I_{SOURCE} =-0.5 mA	2.4	3.3		2.4	3.3		V	
Logical "0" Output Voltage	V_{CC} =4.75V, I_{SINK} =6.4 mA			0.4			0.4	V	
Strobe Input "1" Current (Output Enabled)	V _{CC} =5.25V, V _{STROBE} =2.4V			200			200	μA	
Strobe Input "0" Current (Output Disabled)	V _{CC} =5.25V, V _{STROBE} =0.4V			-1.6			-1.6	mA	
Strobe Input "0" Voltage	V _{CC} =4.75V			8.0			0.8	V	
Strobe Input "1" Voltage	V _{CC} =4.75V	2			2			V	
Output Short Circuit Current	V _{CC} =5.25V, V _{OUT} =0V	-18		-55	-18		-55	mA	
Supply Current I ⁺	V ⁺ =10V, V ⁻ =−10V, V _{CC} =5.25V, -55°C≤T _A ≤125°C			4.5				mA	
Supply Current I ⁺	V ⁺ =10V, V ⁻ =−10V, V _{CC} =5.25V, 0°C≤T _A ≤70°C						5	mA	
Supply Current I ⁻	V ⁺ =10V, V ⁻ =−10V, V _{CC} =5.25V, -55°C≤T _A ≤125°C			10				mA	
Supply Current I ⁻	V ⁺ =10V, V ⁻ =−10V,V _{CC} =5.25V, 0°C≤T _A ≤70°C						10	mA	
Supply Current I _{CC}	$V^{+}=10V, V^{-}=-10V, V_{CC}=5.25V, -55^{\circ}C \le T_{A} \le 125^{\circ}C$			18				mA	
Supply Current I _{CC} $V^{+}=10V, \ V^{-}=-10V, \\ V_{CC}=5.25V, \\ 0^{\circ}C \leq T_{A} \leq 70^{\circ}C$							20	mA	
Transient Response	V _{IN} = 50 mV overdrive ⁽³⁾								
Propagation Delay Time $(t_{pd(0)})$	T _A =25°C		14	20		14	20	ns	
Propagation Delay Time (t _{pd(1)})	T _A =25°C		14	20		14	20	ns	
Delay Between Output A and B	T _A =25°C		2	5		2	5	ns	
Strobe Delay Time (t _{pd(0)})	T _A =25°C		8			8		ns	
Strobe Delay Time (t _{pd(1)})	T _A =25°C		8			8		ns	

(1) Typical thermal impedances are as follows:

H Package J Package N Package 165°C/W (Still Air) 112°C/W 105°C/W 67°C/W (400 LF/Min Air Flow) $\theta_{\rm jC}$

Refer to RETS161X for LM161H and LM161J military specifications.

Measurements using AC Test circuit, Fanout = 1. The devices are faster at low supply voltages.

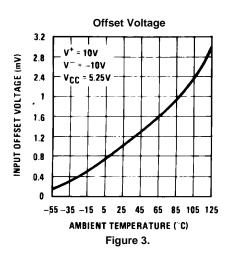
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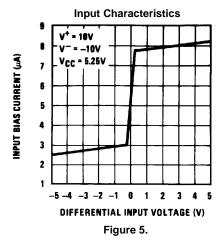
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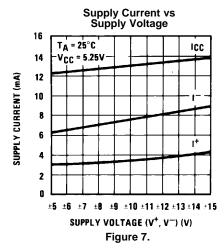


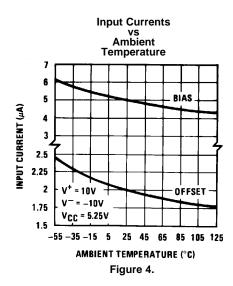
Typical Performance Characteristics

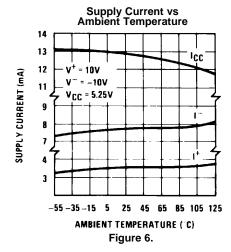
Product Folder Links: LM161 LM361

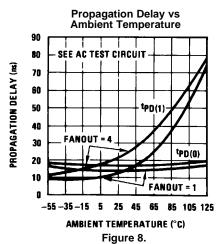






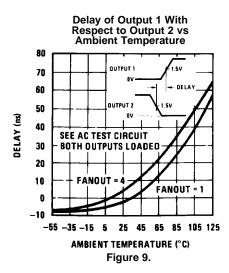


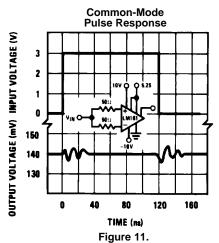


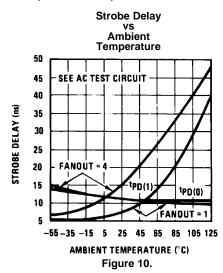


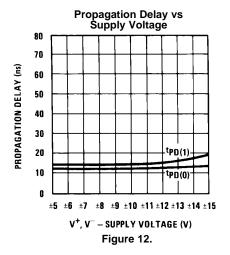


Typical Performance Characteristics (continued)



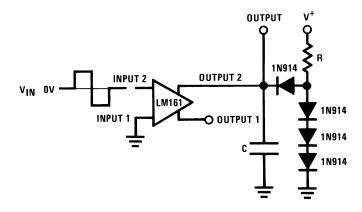








AC TEST CIRCUIT

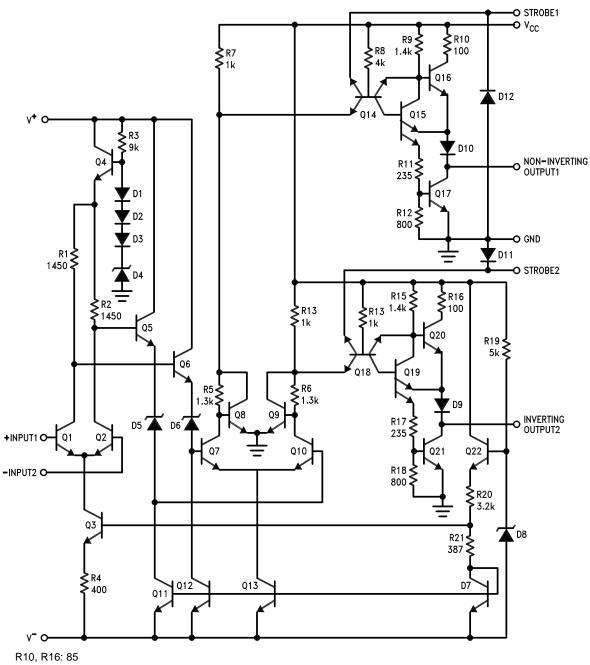


$V_{IN} = \pm 50 \text{ mV}$	FANOUT = 1	FANOUT = 4	V ⁻ = −10V	C=15 pF	C = 30 pF
$V^{+} = +10V$	R = 2.4k	$R = 680\Omega$	$V_{CC} = 5.25V$		



SCHEMATIC DIAGRAM

LM161



R11, R17: 205

SNOSBJ5C-MAY 1999-REVISED MARCH 2013



REVISION HISTORY

Cł	hanges from Revision B (March 2013) to Revision C	Page
•	Changed layout of National Data Sheet to TI format	7

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
LM361H/NOPB	Active	Production	TO-100 (LME) 10	500 TUBE	Yes	Call TI	Level-1-NA-UNLIM	0 to 70	(LM361H, LM361H)
LM361H/NOPB.B	Active	Production	TO-100 (LME) 10	500 TUBE	Yes	Call TI	Level-1-NA-UNLIM	0 to 70	(LM361H, LM361H)
LM361M	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	0 to 70	LM361M
LM361M/NOPB	Active	Production	SOIC (D) 14	55 TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 70	LM361M
LM361M/NOPB.B	Active	Production	SOIC (D) 14	55 TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 70	LM361M
LM361MX/NOPB	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	LM361M
LM361MX/NOPB.B	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	LM361M
LM361N/NOPB	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	0 to 70	LM361N
LM361N/NOPB.B	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	0 to 70	LM361N

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No. RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

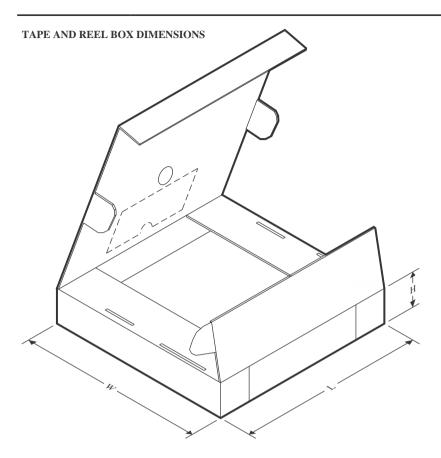


*All dimensions are nominal

Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM361MX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

Ì	Device	Device Package Type		Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
ı	LM361MX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0	

PACKAGE MATERIALS INFORMATION

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TUBE

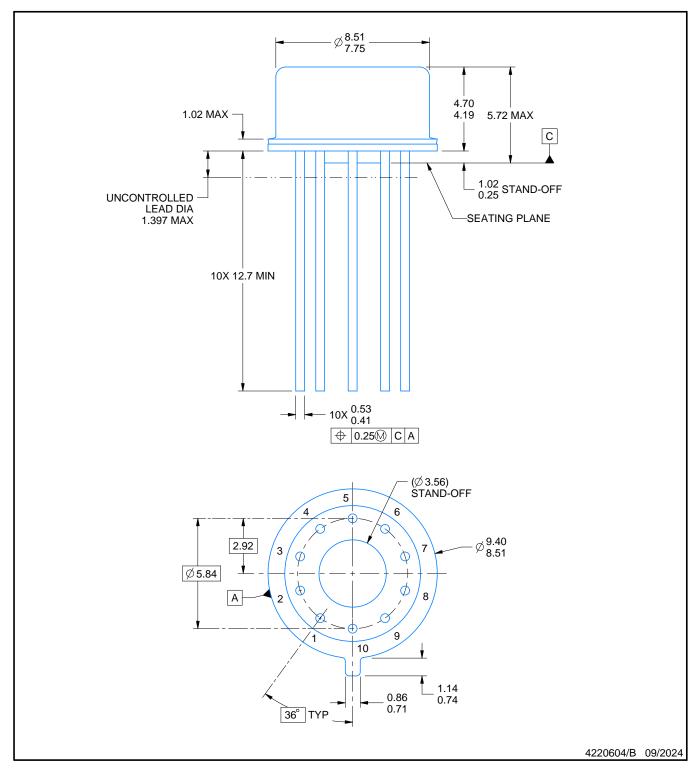


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM361M/NOPB	D	SOIC	14	55	495	8	4064	3.05
LM361M/NOPB.B	D	SOIC	14	55	495	8	4064	3.05
LM361N/NOPB	N	PDIP	14	25	502	14	11938	4.32
LM361N/NOPB.B	N	PDIP	14	25	502	14	11938	4.32



TRANSISTOR OUTLINE

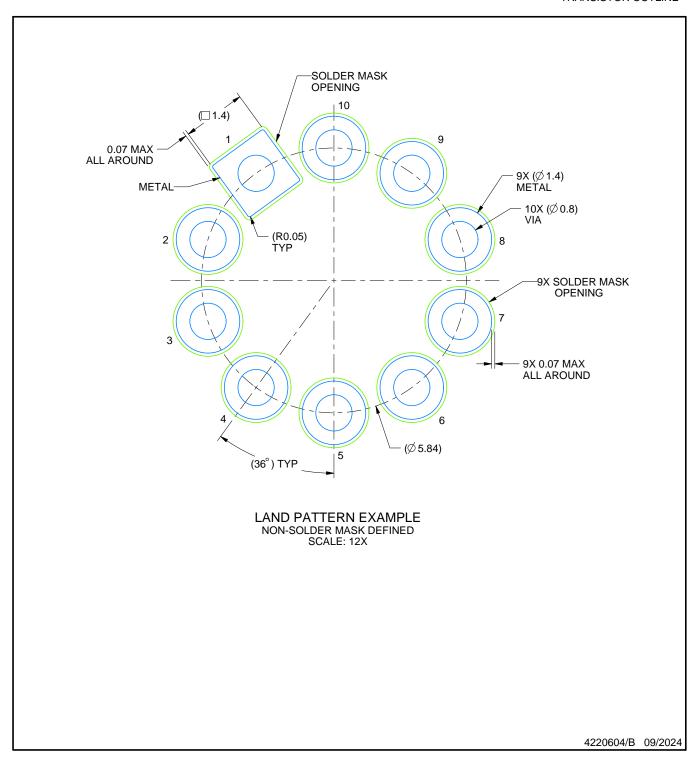


NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
 3. Reference JEDEC registration MO-006/TO-100.



TRANSISTOR OUTLINE





SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



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