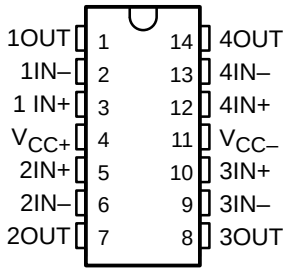
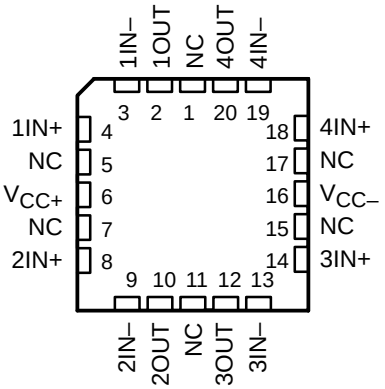
- **μA741 Operating Characteristics**
- **Low Supply-Current Drain . . . 0.6 mA Typ (per amplifier)**
- **Low Input Offset Voltage**
- **Low Input Offset Current**
- **Class AB Output Stage**
- **Input/Output Overload Protection**
- **Designed to Be Interchangeable With Industry Standard LM148, LM248, and LM348**

LM148 . . . J PACKAGE
LM248 . . . D OR N PACKAGE
LM348 . . . D, N, OR NS PACKAGE
(TOP VIEW)



LM148 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

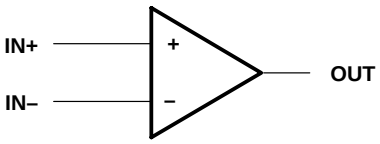
The LM148, LM248, and LM348 are quadruple, independent, high-gain, internally compensated operational amplifiers designed to have operating characteristics similar to the μA741. These amplifiers exhibit low supply-current drain and input bias and offset currents that are much less than those of the μA741.

ORDERING INFORMATION

T_A	V_{IO}max AT 25°C	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	6 mV	PDIP (N)	Tube of 25	LM348N	LM348N
		SOIC (D)	Tube of 50	LM348D	LM348
			Reel of 2500	LM348DR	
		SOP (NS)	Reel of 2000	LM348NSR	LM348
–25°C to 85°C	6 mV	PDIP (N)	Tube of 25	LM248N	LM248N
		SOIC (D)	Tube of 50	LM248D	LM248
			Reel of 2500	LM248DR	
–55°C to 125°C	5 mV	CDIP (J)	Tube of 25	LM148J	LM148J
		LCCC (FK)	Tube of 50	LM148FK	LM148FK

† Package drawings, standard packing quantities, thermal data, symboliztion, and PCB design guidelines are available at www.ti.com/sc/package.

symbol (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1): LM148 . . . . . 22 V
LM248, LM348 . . . . . 18 V
Supply voltage, $V_{CC–}$ (see Note 1): LM148 . . . . . –22 V
LM248, LM348 . . . . . –18 V
Differential input voltage, V_{ID} (see Note 2): LM148 . . . . . 44 V
LM248, LM348 . . . . . 36 V
Input voltage, V_I (either input, see Notes 1 and 3): LM148 . . . . . –22 V
LM248, LM348 . . . . . –18 V
Duration of output short circuit (see Note 4) . . . . . Unlimited
Operating virtual junction temperature, T_J . . . . . 150°C
Package thermal impedance, θ_{JA} (see Notes 5 and 6): D package . . . . . 86°C/W
N package . . . . . 80°C/W
NS package . . . . . 76°C/W
Package thermal impedance, θ_{JC} (see Notes 7 and 8): FK package . . . . . 5.61°C/W
J package . . . . . 15.05°C/W
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: D, N, or NS package . . . . . 260°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and $V_{CC–}$.
2. Differential voltages are at IN+ with respect to IN–.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or the value specified in the table, whichever is less.
4. The output may be shorted to ground or either power supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
5. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperautre is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
6. The package thermal impedance is calculated in accordance with JESD 51-7.
7. Maximum power dissipation is a function of $T_J(max)$, θ_{JC}, and T_C. The maximum allowable power dissipation at any allowable ambient temperautre is $P_D = (T_J(max) – T_C)/\theta_{JC}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
8. The package thermal impedance is calculated in accordance with MIL-STD-883.

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC+}	4	18	V
Supply voltage, $V_{CC–}$	–4	–18	V

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			LM148			LM248			LM348			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0		25°C		1	5		1	6		1	6	mV
				Full range			6			7.5			7.5	
I_{IO}	Input offset current	V_O = 0		25°C		4	25		4	50		4	50	nA
				Full range			75			125			100	
I_{IB}	Input bias current	V_O = 0		25°C		30	100		30	200		30	200	nA
				Full range			325			500			400	
V_{ICR}	Common-mode input voltage range			Full range	±12			±12			±12			V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ		25°C	±12	±13		±12	±13		±12	±13		V
		R_L ≥ 10 kΩ		Full range	±12			±12			±12			
		R_L = 2 kΩ		25°C	±10	±12		±10	±12		±10	±12		
		R_L ≥ 2 kΩ		Full range	±10			±10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L = ≥ 2 kΩ		25°C	50	160		25	160		25	160		V/mV
				Full range	25			15			15			
r_i	Input resistance‡			25°C	0.8	2.5		0.8	2.5		0.8	2.5		MΩ
B_1	Unity-gain bandwidth	A_{VD} = 1		25°C		1			1			1		MHz
ϕ_m	Phase margin	A_{VD} = 1		25°C		60°			60°			60°		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0		25°C	70	90		70	90		70	90		dB
				Full range	70			70			70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±9 V to ±15 V, V_O = 0		25°C	77	96		77	96		77	96		dB
				Full range	77			77			77			
I_{OS}	Short-circuit output current			25°C		±25			±25			±25		mA
I_{CC}	Supply current (four amplifiers)	No load	V_O = 0	25°C					2.4	4.5		2.4	4.5	mA
			V_O = V_{OM}			2.4	3.6							
V_{O1}/V_{O2}	Crosstalk attenuation	f = 1 Hz to 20 kHz		25°C		120			120			120		dB

† All characteristics are measured under open-loop conditions with zero common-mode input voltage, unless otherwise specified. Full range for T_A is –55°C to 125°C for LM148, –25°C to 85°C for LM248, and 0°C to 70°C for LM348.

‡ This parameter is not production tested.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 2 kΩ, C_L = 100 pF, See Figure 1		0.5		V/μs

PARAMETER MEASUREMENT INFORMATION

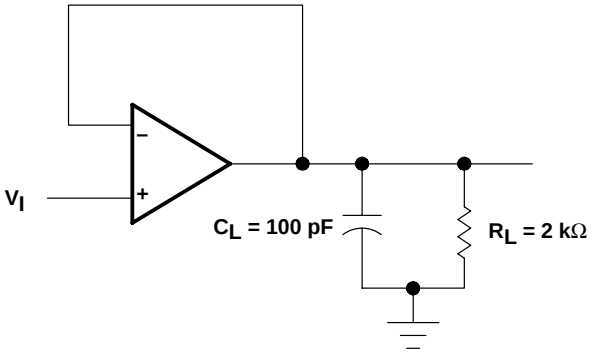


Figure 1. Unity-Gain Amplifier

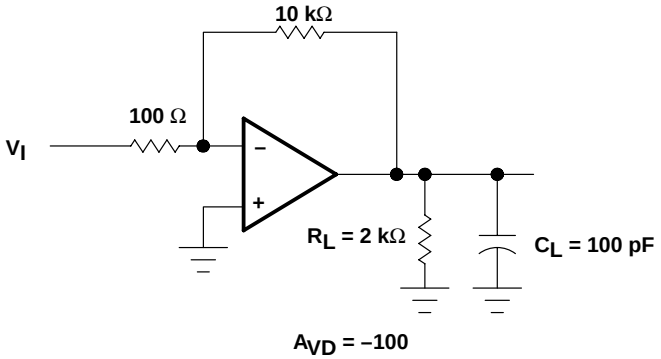


Figure 2. Inverting Amplifier

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM148 MW8	Active	Production	WAFERSALE (YS) | 0	1 | NOT REQUIRED	-	Call TI	Level-1-NA-UNLIM	-55 to 125	
LM148FKB	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	LM148FKB
LM148FKB.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	LM148FKB
LM148J	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	LM148J
LM148J.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	LM148J
LM148JB	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	LM148JB
LM148JB.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	LM148JB
LM248D	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-25 to 85	LM248
LM248DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM248
LM248DR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM248
LM248N	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-25 to 85	LM248N
LM248N.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-25 to 85	LM248N
LM348D	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	0 to 70	LM348
LM348DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM348
LM348DR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM348
LM348DRE4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM348
LM348DRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM348
LM348N	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	LM348N
LM348N.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	LM348N
LM348NSR	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM348
LM348NSR.A	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM348

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

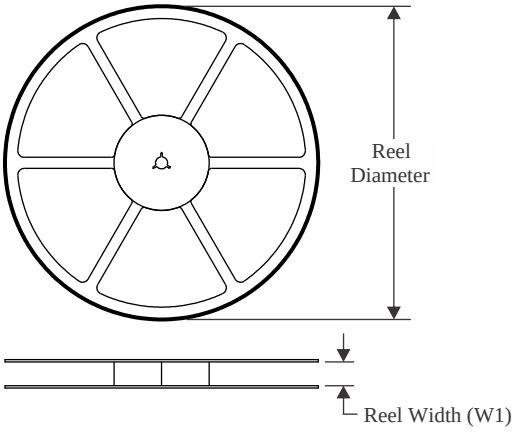
(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

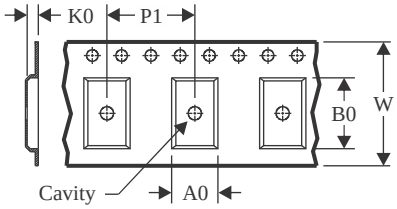
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

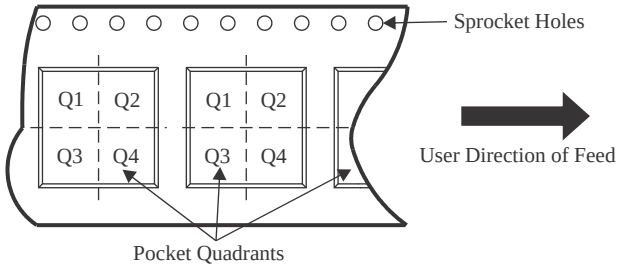


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

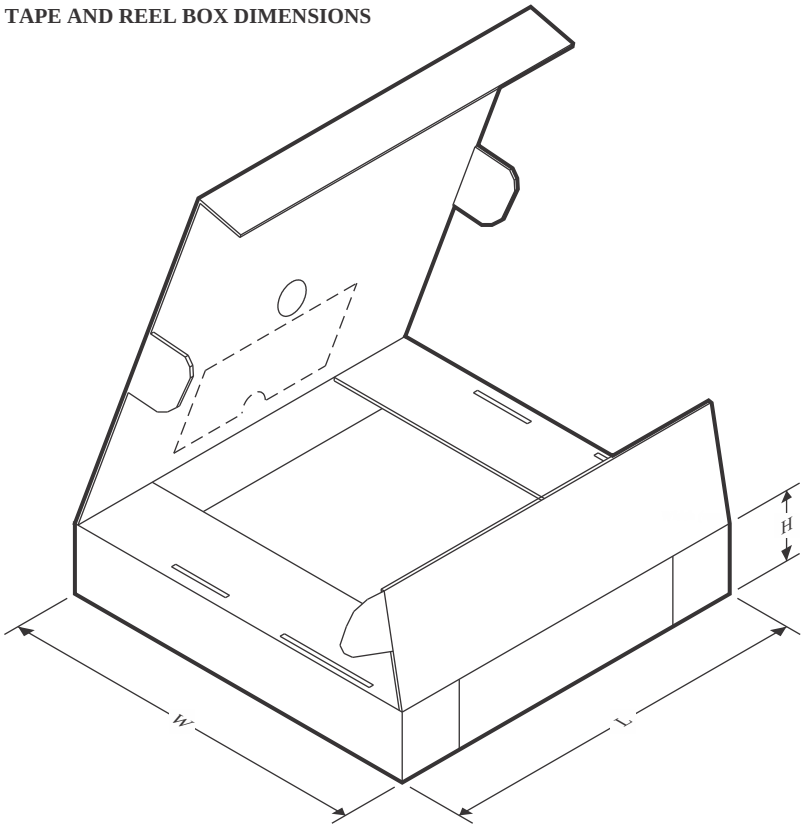
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM248DR	SOIC	D	14	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM348DR	SOIC	D	14	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM348DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM348NSR	SOP	NS	14	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1

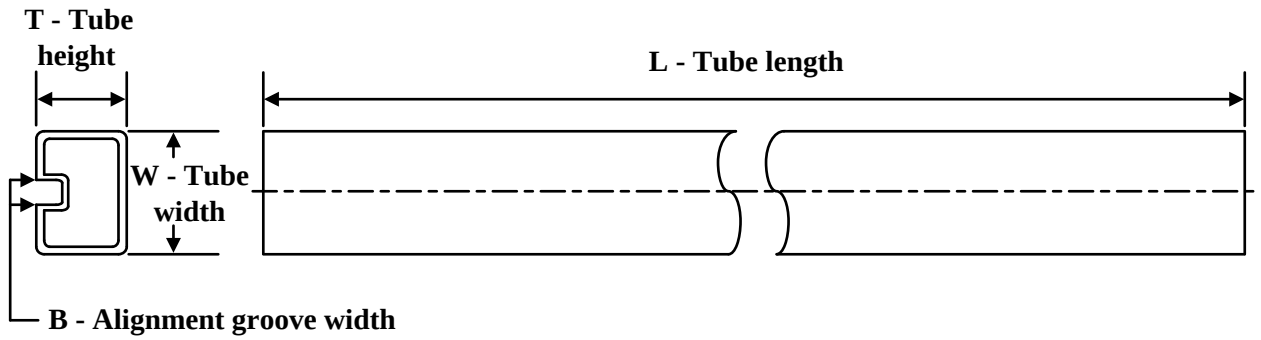
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

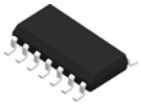
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM248DR	SOIC	D	14	2500	340.5	336.1	25.0
LM348DR	SOIC	D	14	2500	340.5	336.1	25.0
LM348DR	SOIC	D	14	2500	353.0	353.0	32.0
LM348NSR	SOP	NS	14	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM148FKB	FK	LCCC	20	55	506.98	12.06	2030	NA
LM148FKB.A	FK	LCCC	20	55	506.98	12.06	2030	NA
LM248N	N	PDIP	14	25	506	13.97	11230	4.32
LM248N	N	PDIP	14	25	506	13.97	11230	4.32
LM248N.A	N	PDIP	14	25	506	13.97	11230	4.32
LM248N.A	N	PDIP	14	25	506	13.97	11230	4.32
LM348N	N	PDIP	14	25	506	13.97	11230	4.32
LM348N	N	PDIP	14	25	506	13.97	11230	4.32
LM348N.A	N	PDIP	14	25	506	13.97	11230	4.32
LM348N.A	N	PDIP	14	25	506	13.97	11230	4.32

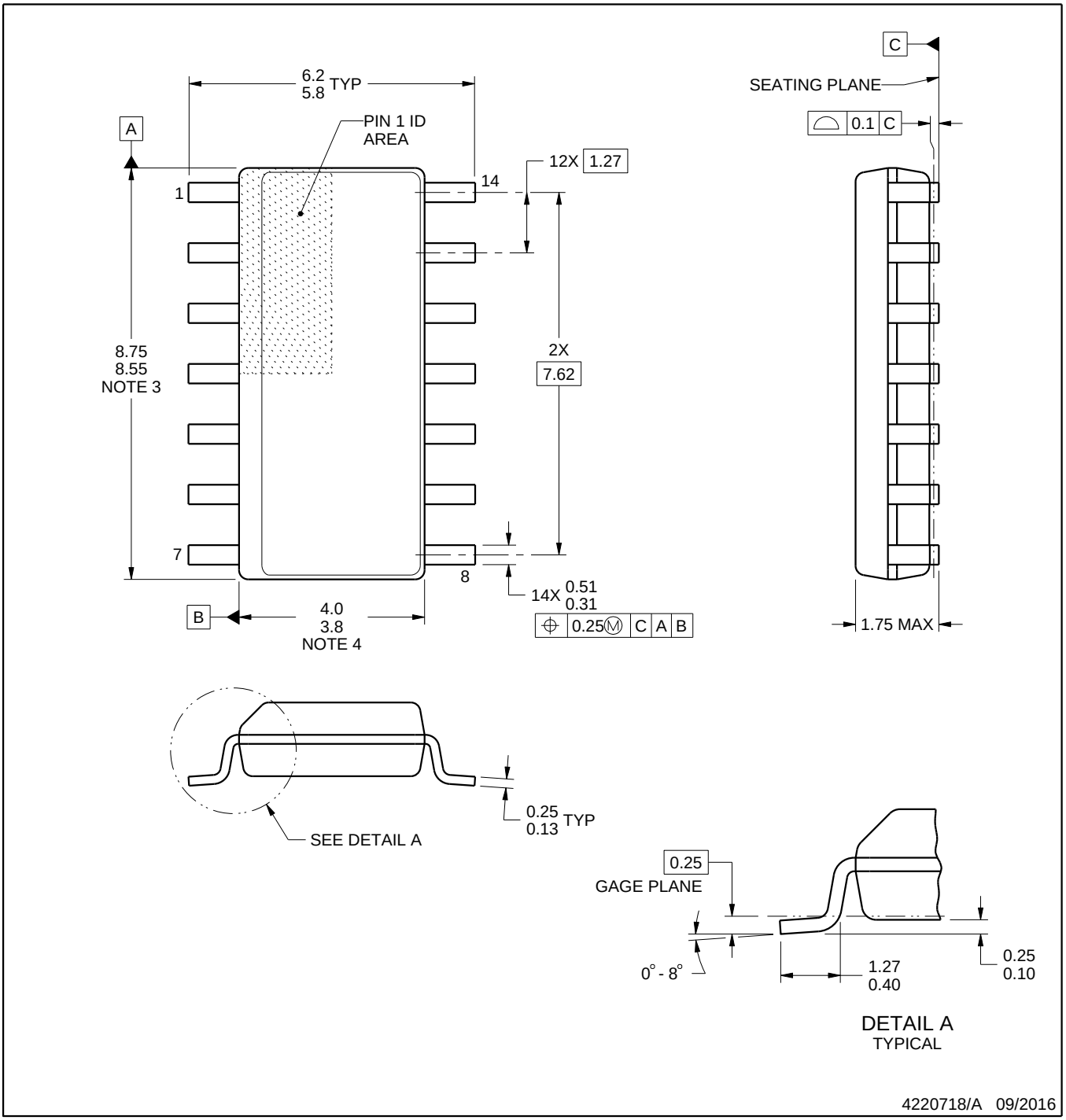


PACKAGE OUTLINE

D0014A

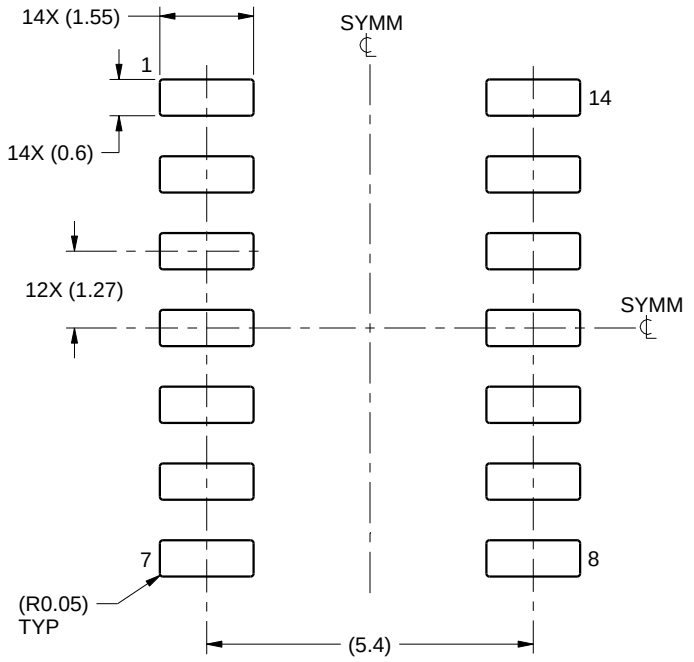
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

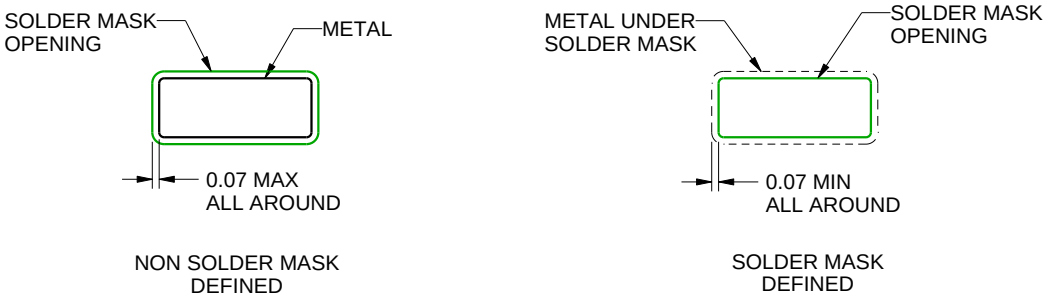


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

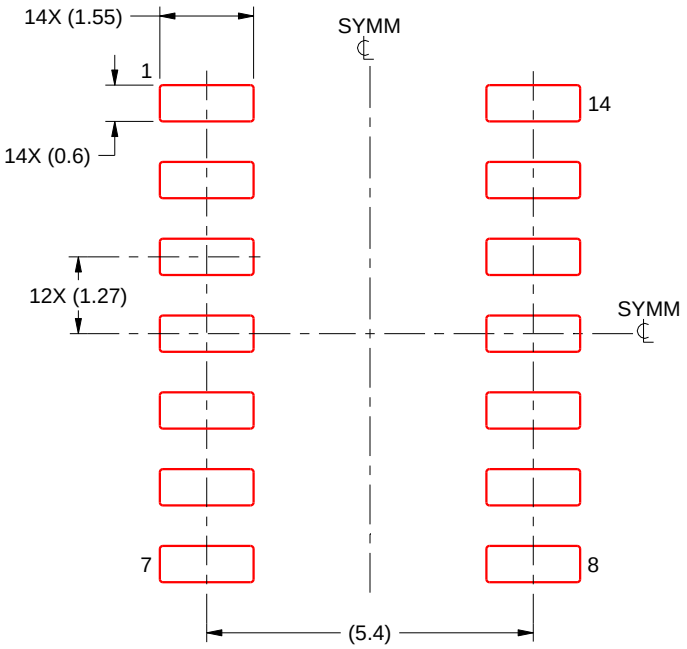
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

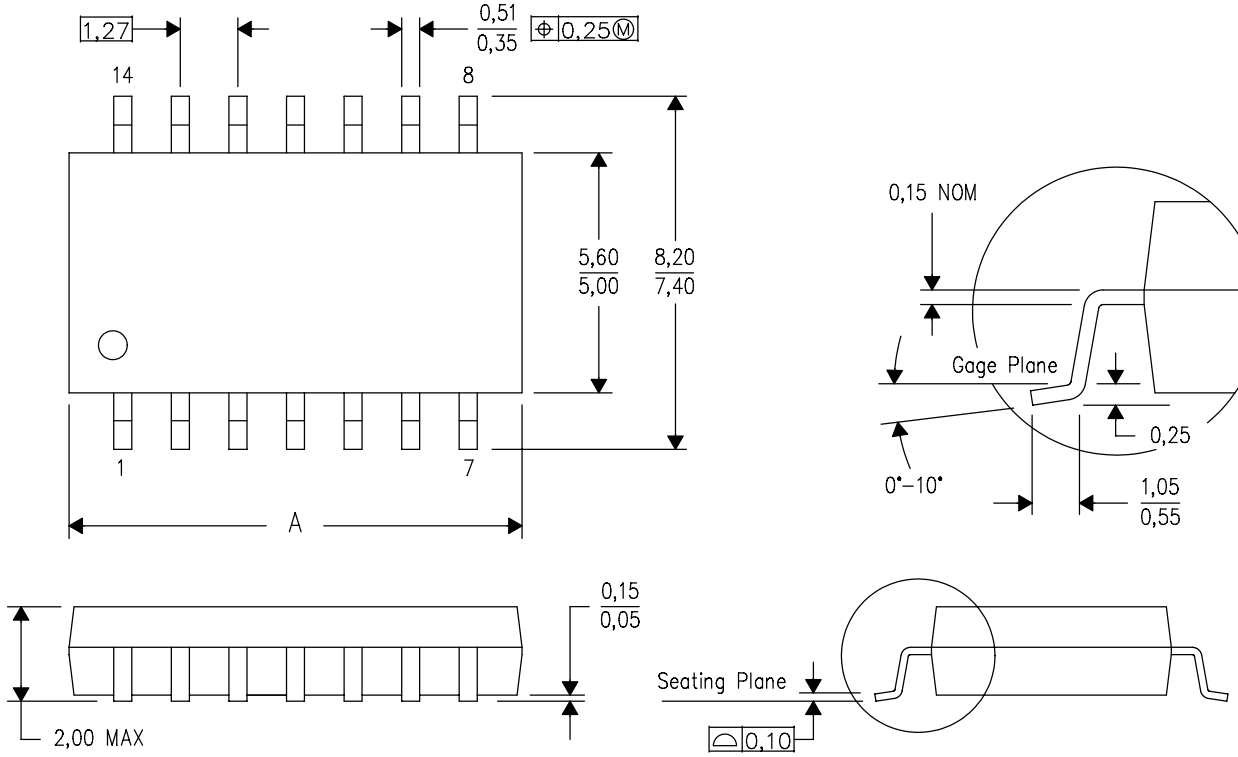
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

GENERIC PACKAGE VIEW

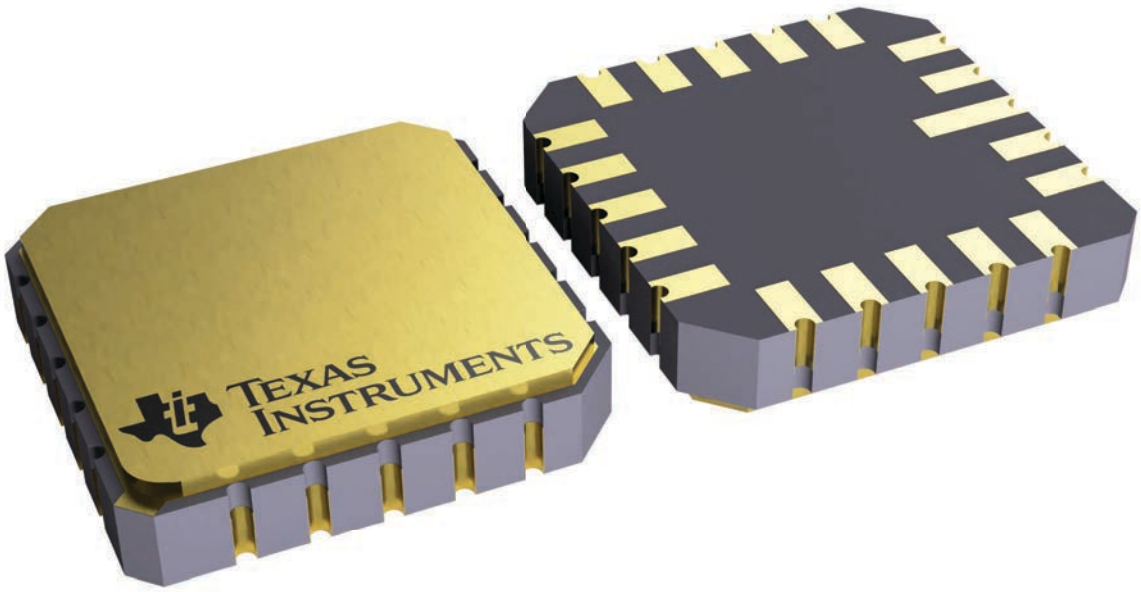
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

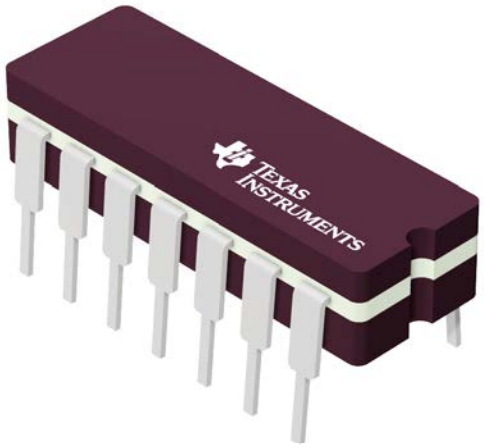


4229370VA\

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

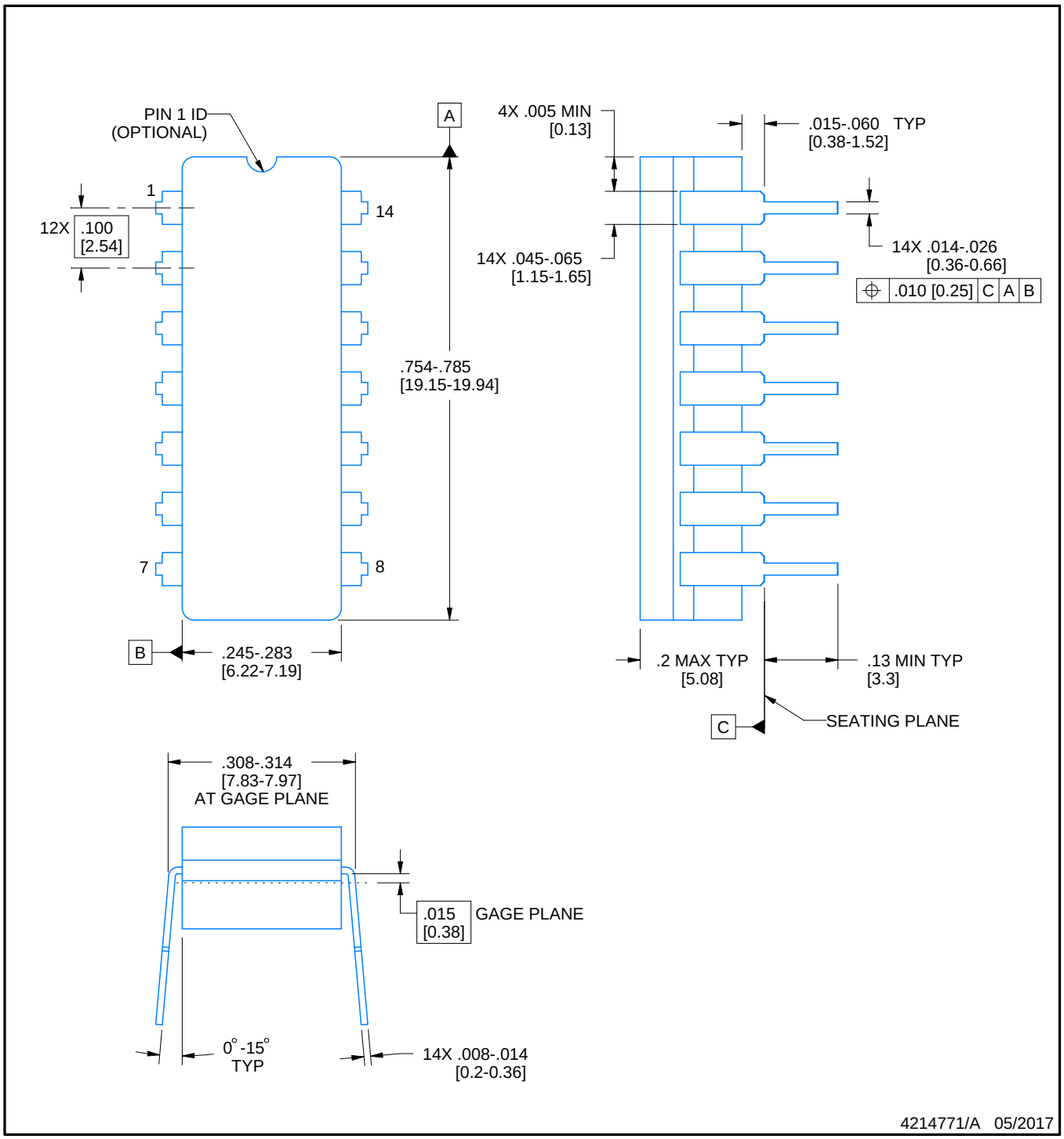
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

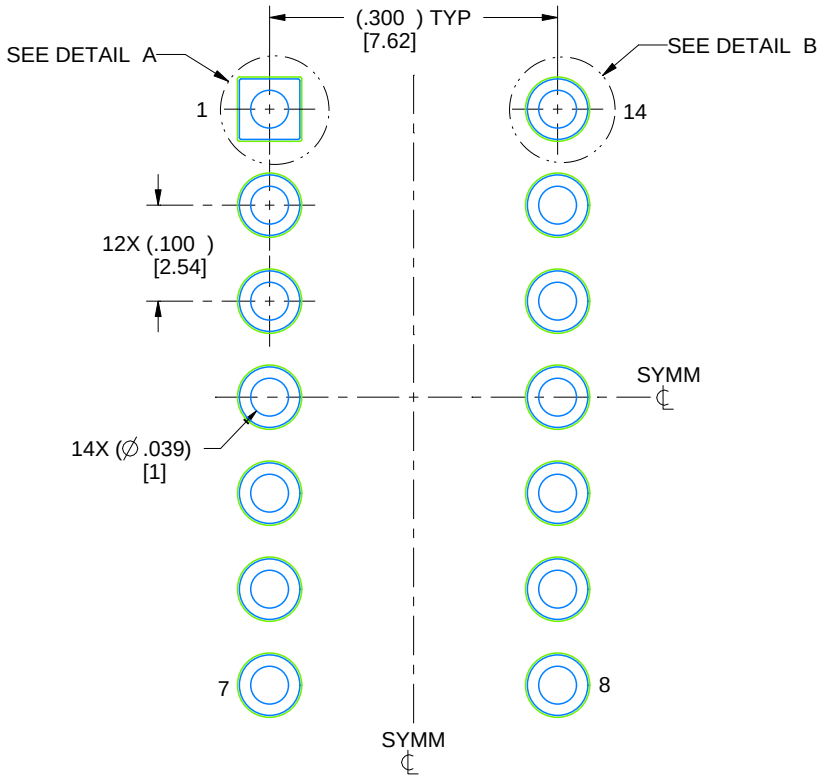
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

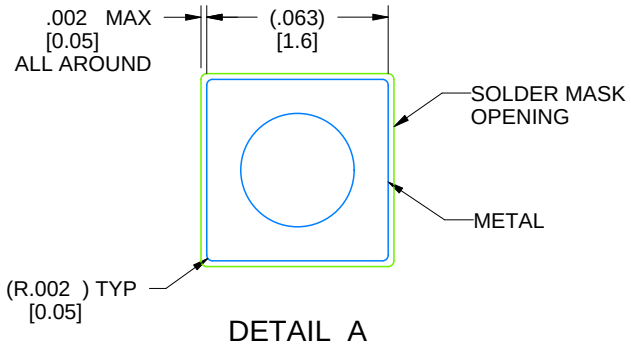
J0014A

CDIP - 5.08 mm max height

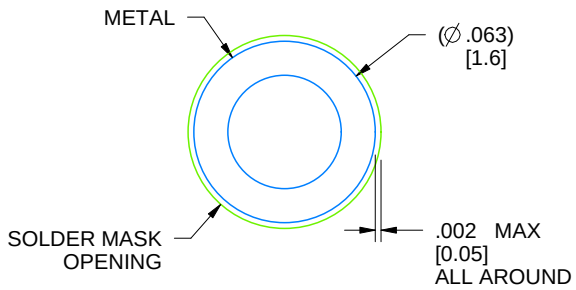
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

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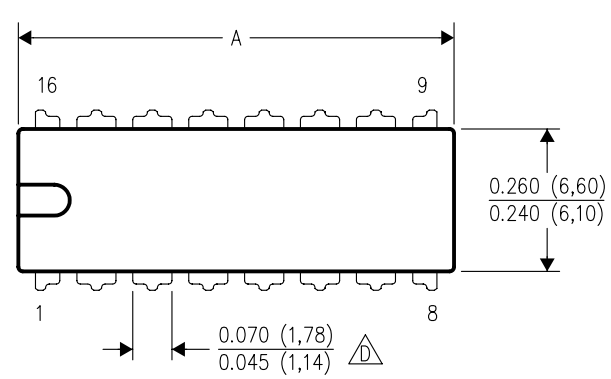
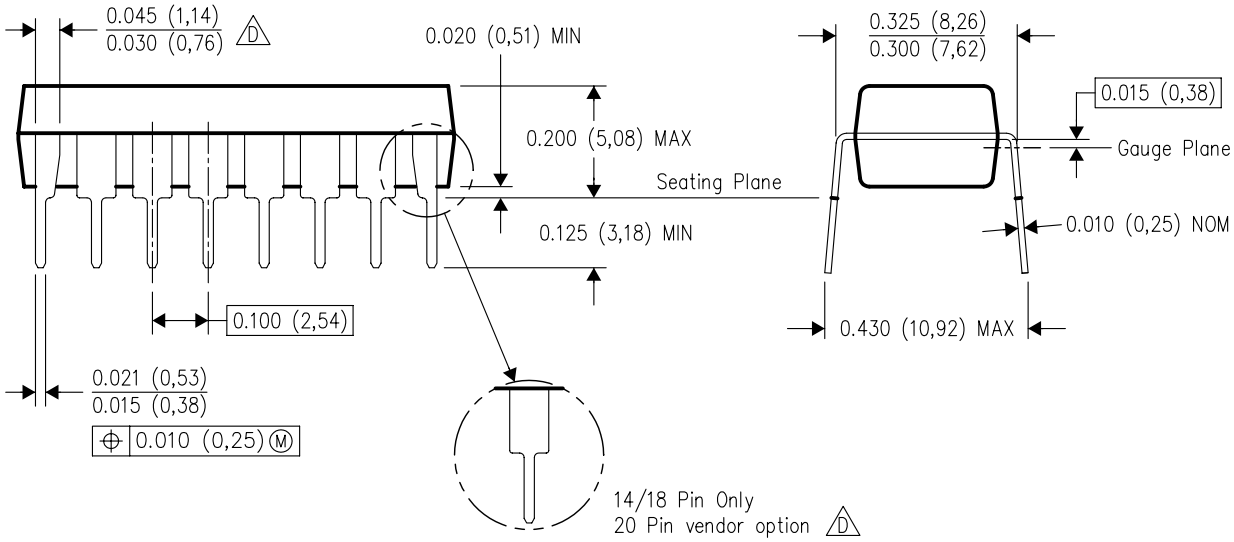
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



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NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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