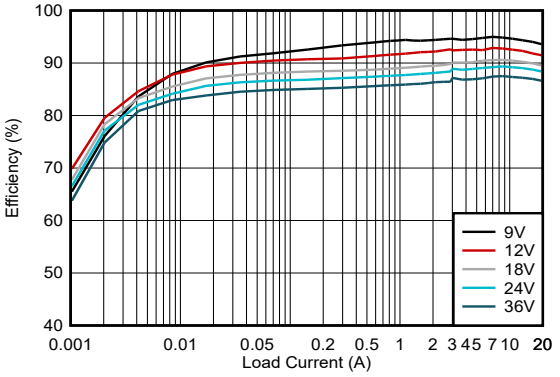
LM25192-Q1 42V, Automotive, High-Efficiency CC-CV Buck Controller With I2C

1 Features

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade 1: –40°C to +125°C ambient operating temperature
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Synchronous CC-CV buck controller with I^2C
  - Wide input voltage range: 4.5V to 42V
  - 1% accurate V_{OUT}, programmable from 1V to 24V(10mV steps) or 3.3V to 24V (20mV steps)
  - 4% accurate $I_{LIM(avg)}$, programmable from 0.5A to 7.5A in 50mA steps (8mΩ R_{SENSE}), 2A to 30A in 200mA steps (2mΩ R_{SENSE})
  - Output slew rate: 0.5mV/µs to 40mV/µs
  - Adjustable cable drop compensation (CDC)
  - Output active discharge
- Optimized for CISPR 25 Class 5 EMI requirements
  - ±5% dual-random spread spectrum (DRSS)
  - Programmable f_{SW}: 200kHz to 2.2MHz
  - Programmable PFM or FPWM operation
- Programmable protection features
  - UV/OV (PG) warning: ±5% or ±10%
  - OVP warning, fault: 105% to 136% in 1% steps
  - Internal hiccup-mode overcurrent protection
  - Enable, interrupt, and thermal shutdown
- Analog current monitoring pin (IMON)
- 3.5mm × 4.5mm QFN-19 wettable flanks package
- Create a custom design using the LM25192-Q1 device with the WEBENCH® Power Designer

2 Applications

- Automotive electronic systems
- Infotainment and cluster
- Power distribution board with 12V input
- Automotive lighting



LM25192-Q1 Efficiency, Vout = 6V

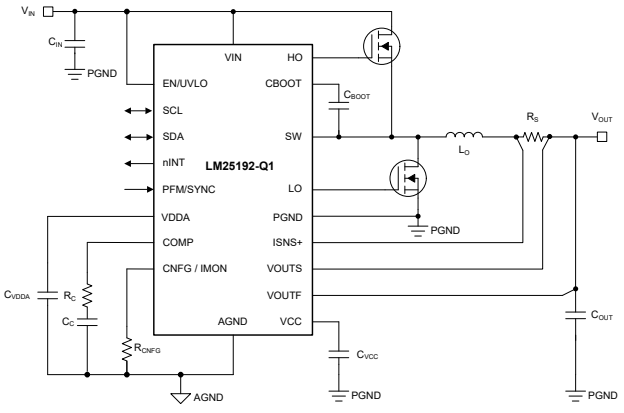
3 Description

The LM25192-Q1 is a 42V, high-efficiency, synchronous buck controller with constant-current constant-voltage (CC-CV) regulation and I^2C interface.

The current-mode control architecture with a 30ns typical minimum on-time allows high conversion ratios at high frequencies coupled with a fast transient response and excellent load and line regulation. The highly accurate CC-CV operation enables seamless transition between constant-current and constant-voltage modes. The I^2C interface allows programming of output voltage in 10mV or 20mV steps, average output current limit in 50mA to 200mA steps, as well as output voltage slew rate, switching frequency, soft-start slew rate, mode of operation, current loop compensation, output active discharge strength, and cable drop compensation gain.

The LM25192-Q1 also features an array of safety features including undervoltage and overvoltage protection with programmable thresholds, overcurrent protection with programmable hiccup mode, and thermal shutdown.

Additional features of the LM25192-Q1 include programmable diode emulation(PFM) for lower current consumption at light-load conditions, open-drain nINT flag for fault reporting and output monitoring, precision enable input, monotonic start-up into prebiased load, integrated dual input (VIN and VOUTF) VCC supply regulator, and oversized VDDA regulator for powering external loads, such as companion microcontrollers.



Typical Application Circuit

The LM25192-Q1 includes several features to simplify compliance with CISPR 25 emissions requirements. First, a symmetrical pinout provides excellent input capacitor placement and enables an ultra-low effective value for the power-loop parasitic inductance, which reduces switching losses and improves EMI performance at high input voltage and high switching frequency. A pin-selectable switch-node slew-rate control feature further reduces emissions at high frequencies. An I2C programmable switching frequency as high as 2.2MHz can be synchronized to an external clock source to eliminate beat frequencies in noise-sensitive applications. Finally, the LM25192-Q1 has an I2C selectable ±5% dual-random spread spectrum (DRSS) significantly reduces peak emissions through a combination of triangular and pseudo-random modulation while keeping output voltage ripple very low.

The LM25192-Q1 controller comes in a 3.5mm × 4.5mm thermally-optimized, 19-pin QFN package. The large PGND die-attach pad improves thermal performance and board level reliability (BLR). Also included are wettable-flank pins to facilitate optical inspection during manufacturing. The 19-pin QFN packaging with useable current, lifetime reliability, and cost advantages targets applications requiring high power density. The wide input voltage range, low quiescent current consumption, high-temperature operation, cycle-by-cycle current limit, low EMI signature, and small design size provide an excellent point-of-load regulator design for applications requiring enhanced robustness and durability.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LM25192-Q1	RGY (VQFN, 19)	4.5mm × 3.5mm

(1) For more information, see *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

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4 Related Products

DEVICE OPTION	V_{IN} (Max)	V_{OUT} (Max)	I_{OUT} (Max)	$I_{LIM(avg)}$ (Max)
LM25192-Q1	42V	24V	5A (R_S = 8mΩ)	7.5A
			20A (R_S = 2mΩ)	30A
LM5192-Q1	80V	48V	5A (R_S = 8mΩ)	7.5A
			20A (R_S = 2mΩ)	30A
LM5192	80V	48V	5A (R_S = 8mΩ)	7.5A
			20A (R_S = 2mΩ)	30A

5 Pin Configuration and Functions

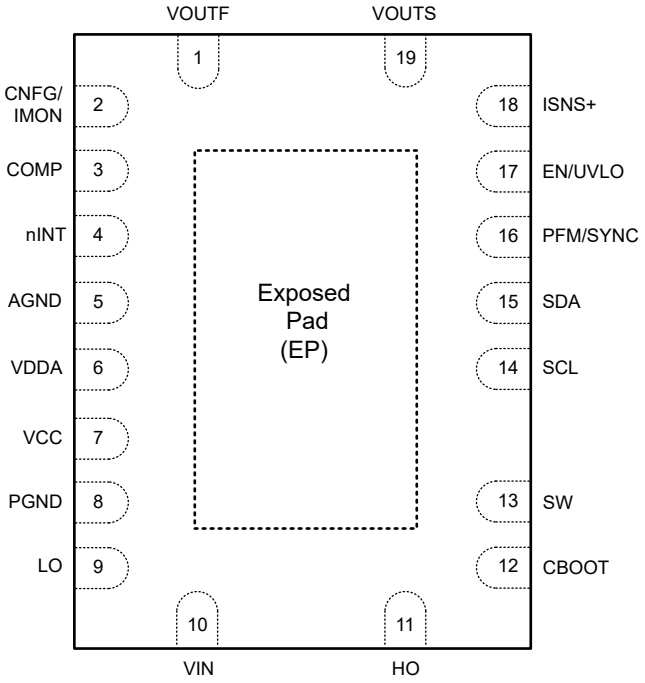


Figure 5-1. RGY 19-Pin VQFN (Top View)

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
1	VOUTF	P	Output voltage discharge pin and the VCC bias regulator input. Connect the VOUTF pin to the output side of the respective output capacitor.
2	CNFG/ IMON	I	Configuration and output current monitoring pin. Connect a resistor to ground to set the I^2C address. Keep the total capacitance on this pin less than 200pF.
3	COMP	O	External compensation pin. This pin is the output of the transconductance amplifier. Connect a compensation network from the COMP pin to AGND.
4	nINT	O	Interrupt pin. This pin is an open-collector output that toggles low in case of a status register change.
5	AGND	G	Analog ground pin. Ground return for the internal voltage reference and analog circuits.
6	VDDA	P	Internal analog bias regulator output pin. Connect a 22µF ceramic decoupling capacitor from VDDA to AGND as close as possible to the pins.
7	VCC	P	VCC bias supply pin. Connect a 4.7µF ceramic capacitors between VCC and PGND as close as possible to the pins.
8	PGND	G	Controller power ground pin. Connect to the system ground.
9	LO	O	Low-side power MOSFET gate driver output.
10	VIN	P	Controller input pin to the VCC regulator. Connect to the input supply, input filter capacitors and drain of the high side FET. Place input capacitors close to VIN pin.
11	HO	O	High-side power MOSFET gate driver output.
12	CBOOT	P	High-side driver supply for the bootstrap gate drive. Connect a 47nF bootstrap capacitor between the CBOOT and SW pins.
13	SW	P	Switch node pin and the high-side gate driver return. Connect a 47nF bootstrap capacitor between the CBOOT and SW pins, the source terminal of the high-side MOSFET, and the drain terminal of the low-side MOSFET.
14	SCL	I/O	I^2C clock pin.
15	SDA	I/O	I^2C data pin.

Table 5-1. Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
16	PFM / SYNC	I	PFM / FPWM mode selection and synchronization input pin. Connect the PFM / SYNC pin to VDDA to enable diode emulation mode. Connect the PFM / SYNC pin to AGND to operate in forced PWM (FPWM) mode with continuous conduction at light loads. The PFM / SYNC pin can also be used as a synchronization input to synchronize the internal oscillator to an external clock.
17	EN / UVLO	I	Enable / undervoltage lockout pin. Drive this pin high to place the device into the ready mode. When in ready mode, the I^2C interface is available and the controller can be enabled by setting the CONTROLLER_EN bit in the OPERATIONOPERATION register. If the EN/UVLO function is not needed, tie this pin to VIN. Connect an external resistor divider network to set the UVLO threshold.
18	ISNS+	I	Current sense amplifier input. Connect the ISNS+ pin to the inductor side of the external current sense resistor using a low-current Kelvin connection.
19	VOUTS	I	Output voltage sense and the current sense amplifier input. Connect the VOUTS pin to the output side of the respective current sense resistor using a low-current Kelvin connection.
—	EP	—	Exposed thermal pad. Connect to the system ground using multiple vias.

(1) P = Power, G = Ground, I = Input, O = Output.

6 Specifications

6.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input Voltage	VIN to PGND	–0.3	47	V
Input Voltage	SW to VIN		0.6	V
Input Voltage	SW to VIN transients < 40ns		10	V
Input Voltage	SW to PGND	–0.3	47	V
Input Voltage	SW to PGND transient < 20ns	–5	50	V
Input Voltage	EN/UVLO to PGND	–0.3	47	V
Input Voltage	VOUTF, VOUTS, ISNS+ to PGND	–0.3	30	V
Input Voltage	VOUTS to ISNS+	–0.3	0.3	V
Input Voltage	VDDA, SDA, SCL, nINT, CNFG, PFM/SYNC, COMP to AGND	–0.3	6.5	V
Input Voltage	PGND to AGND	–0.3	0.3	V
Output Voltage	CBOOT to SW, transient < 20ns	–2		V
Output Voltage	CBOOT to SW	–0.3	10	V
Output Voltage	VCC to AGND	–0.3	10	V
Output Voltage	HO to SW	–0.3	V_{CBOOT} + 0.3	V
Output Voltage	HO to SW transient < 20ns	–5		V
Output Voltage	LO to PGND	–0.3	V_{VCC} + 0.3	V
Output Voltage	LO to PGND transient < 20ns	–1.5		V
Operating junction temperature, T_J	Operating junction temperature, T_J	-40	150	°C
Storage temperature, T_{stg}	Storage temperature, T_{stg}	–55	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 (1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (1, 2, 9, 10, 11, 12, 18 and 19)	±750	
			Other pins	±750	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage range		4.5		42	V
V_{OUT}	Output voltage range (10mV step)		1		24	V
V_{OUT}	Output voltage range (20mV step)		3.3		24	V
	VIN, EN/UVLO, SW to PGND	VIN, EN/UVLO, SW to PGND	0		42	V
	SDA, SCL, PFM/SYNC, nINT to AGND	SDA, SCL, PFM/SYNC, nINT to AGND	0		5.25	V
	VOUTF, VOUTS, ISNS+ to PGND	VOUTF, VOUTS, ISNS+ to PGND	0		24	V
	PGND to AGND		0		0.3	V
T_J	Operating junction temperature		–40		150	°C

6.4 Thermal Information

THERMAL METRIC[1]		LM25192-Q1 RGY (VQFN) 19 PINs	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	44.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	40.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	21.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	21.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

6.5 Electrical Characteristics

T_J = –40°C to +150°C. Typical values are at T_J = 25°C V_{IN} = 24V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY (VIN)						
I_{Q-SD}	V_{IN} shutdown current	Non-switching, V_{IN} = 12V, V_{EN} = 0V, V_{FB} = V_{REF} + 50mV		2.4	5	µA
I_{Q-SBY}	V_{IN} standby current [1]	Non-switching, V_{IN} = 12V, 0.5V ≤ V_{EN} ≤ 1V		310		µA
$I_{Q-READY}$	V_{IN} ready current [1]	Non-switching, V_{IN} = 12V, V_{EN} ≥ 1V		1		mA
$I_{Q-SLEEP}$	V_{IN} sleep current, 5V output, no load	V_{IN} = 12V, V_{EN} = 5V, V_{VOUTF} = V_{VOUTS} = 5V, no-load, non-switching, $V_{PFM/SYNCIN}$ = 5V		150	250	µA
ENABLE (EN / UVLO)						
V_{SBY-TH}	Shutdown-to-standby threshold voltage	$V_{EN/UVLO}$ rising		0.55		V
V_{EN-TH}	Enable voltage rising threshold	$V_{EN/UVLO}$ rising	0.95	1.0	1.05	V
INTERNAL LDO (VCC)						
V_{VCC1}	VCC regulation voltage	I_{VCC} = 50mA	4.5	5	5.5	V
V_{VCC2}	VCC regulation voltage	I_{VCC} = 50mA	7.5	8	8.5	V
$V_{VCC(DO1)}$	VIN to VCC dropout voltage	V_{IN} = 5V, I_{VCC} = 50mA		130		mV
$V_{VCC(DO2)}$	BIAS to VCC dropout voltage	V_{VOUTF} = 5V, I_{VCC} = 50mA		110		mV
$I_{VCC(LIM)}$	VCC current limit	V_{CC} = 4V	100	185	348	mA
INTERNAL LDO (VDDA)						
V_{VDDA}	VDDA regulation voltage	I_{VDD} = 5mA	4.75	5	5.25	V
$V_{VDDA(DO)}$	VCC to VDDA dropout voltage	V_{IN} = 5V, I_{VDD} = 30mA		125		mV
$I_{VDDA-CL}$	VDDA current limit	V_{DDA} = 4.5V	36	50	71	mA
EXTERNAL BIAS (VOUTF)						
$V_{BIAS-TH}$	V_{IN} to V_{VOUTF} switchover rising threshold		4.83	4.9	4.973	V
$V_{BIAS-HYS}$	V_{IN} to V_{VOUTF} switchover hysteresis			140		mV
ACTIVE DISCHARGE (VOUTF)						
$I_{DISCHARGE}$	Output discharge current	0xD2[2:1] = 01b		24		mA
		0xD2[2:1] = 10b		48		mA
		0xD2[2:1] = 11b		72		mA
OUTPUT VOLTAGE (VOUTS)						
$V_{OUT(MIN)}$	Minimum output voltage setpoint - 10mV step	0xD1[7] = 0b, 0x21 = 0x64h, T_J = –40°C to +85°C	0.96	1	1.04	V
$V_{OUT(MIN)}$	Minimum output voltage setpoint - 20mV step	0xD1[7] = 1b, 0x21 = 0xA5h, T_J = –40°C to +85°C	3.24	3.3	3.36	V
$V_{OUT(DEFAULT)}$	Default output voltage setpoint	0xD1[7] = 1b, 0x21 = 0xFAh, T_J = –40°C to +85°C	4.95	5.0	5.05	V
$V_{OUT(MAX)}$	Maximum output voltage setpoint	0xD1[7] = 1b, 0x21 = 0x480h, T_J = –40°C to +85°C	23.76	24	24.24	V

6.5 Electrical Characteristics (continued)

T_J = –40°C to +150°C. Typical values are at T_J = 25°C V_{IN} = 24V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OUT(MAX)}$	Maximum output voltage setpoint	0xD1[7] = 0b, 0x21 = 0x960h, T_J = –40°C to +85°C	23.76	24	24.24	V
ERROR AMPLIFIER (COMP)						
$g_{m-EXTERNAL}$	EA transconductance external compensation		650	1000		µS
PULSE FREQUENCY MODULATION (PFM/SYNC)						
$V_{IL-SYNC}$	PFM/SYNC input threshold low		0.8			V
$V_{IH-SYNC}$	PFM/SYNC input threshold high				1.17	V
Δf_{SYNC}	Synchronization frequency range		–20		20	%
$t_{SYNC-TON-MIN}$	Minimum positive pulse width of external synchronization signal				25	ns
$t_{SYNC-TOFF-MIN}$	Minimum negative pulse width of external synchronization signal				250	ns
SWITCHING FREQUENCY (SW)						
f_{SW1}	Switching frequency 1	0xD1[4:3] = 00b	180	200	228	kHz
f_{SW2}	Switching frequency 2	0xD1[4:3] = 01b	360	400	446	kHz
f_{SW3}	Switching frequency 3	0xD1[4:3] = 10b	540	600	660	kHz
f_{SW4}	Switching frequency 4	0xD1[4:3] = 11b	1.98	2.2	2.42	MHz
t_{ON-MIN}	Minimum on-time(1)			25		ns
$t_{OFF-MIN}$	Minimum off-time			80	126	ns
DUAL RANDOM SPREAD SPECTRUM (DRSS)						
Δf_{SS}	Modulation range			10		%
f_m	Modulation frequency	0xD1[5] = 0b		10		kHz
POWER GOOD						
V_{PG-UV}	Power-Good UV trip level	Falling with respect to the set V_{OUT}, 0xD9[3] = 0b, T_J = –40°C to +85°C	93	95	97.5	%
		Falling with respect to the set V_{OUT}, 0xD9[3] = 1b	88	90	92	%
V_{PG-OV}	Power-Good OV trip level	Rising with respect to the set V_{OUT}, 0xD9[3] = 0b, T_J = –40°C to +85°C	103	105	107	%
		Rising with respect to the set V_{OUT}, 0xD9[3] = 1b	108	110	112	%
$V_{PG-UV-HYST}$	Power-Good UV hysteresis	Falling with respect to the regulated output		1.1		%
$V_{PG-OV-HYST}$	Power-Good OV hysteresis	Raising with respect to the regulated output		1.1		%
$t_{PG-DEGLITCH}$	Power-Good deglitch filter time	V_{OUT} falling or rising		30		µs
OVERVOLTAGE PROTECTION (nINT)						
V_{OVP}	Overvoltage protection	Rising with respect to the set V_{OUT}, 0xD5 = 60h		105		%
V_{OVP}	Overvoltage protection	Rising with respect to the set V_{OUT}, 0xD5 = 7Fh		136		%
V_{OVP_HYST}	Overvoltage protection hysteresis	Rising with respect to the set V_{OUT}		2		%
V_{OL_nINT}	nINT voltage low	Open collector, I_{nFAULT} = 2mA			0.4	V
STARTUP (SOFT START)						
SR_{SS}	Internal soft-start slew rate	0xD2[0] = 0b		5		V/ms
		0xD2[0] = 1b		2.5		V/ms
INTERNAL HICCUP MODE						
$t_{HIC-DLY}$	HICCUP mode activation delay	V_{ISNS+} – V_{VOUT} > 60mV		512		CYCLES
$t_{HIC-DURATION}$	HICCUP mode fault duration	V_{ISNS+} – V_{VOUT} > 60mV		16384		CYCLES
HIGH-SIDE GATE DRIVER (HO)						
$V_{HO-HIGH}$	HO high-state output voltage	I_{HO} = –100mA, $V_{HO-HIGH}$ = V_{CBOOT} – V_{HO}		370		mV
V_{HO-LOW}	HO low-state output voltage	I_{HO} = 100mA		75		mV

6.5 Electrical Characteristics (continued)

T_J = –40°C to +150°C. Typical values are at T_J = 25°C V_{IN} = 24V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{HO-RISE}$	HO rise time (10% to 90%)	C_{LOAD} = 2.7nF		27		ns
$V_{HO-FALL}$	HO fall time (90% to 10%)	C_{LOAD} = 2.7nF		8		ns
LOW-SIDE GATE DRIVER (LO)						
$V_{LO-HIGH}$	LO high-state output voltage	I_{LO} = –100mA		340		mV
V_{LO-LOW}	LO low-state output voltage	I_{LO} = 100mA		75		mV
$V_{LO-RISE}$	LO rise time (10% to 90%)	C_{LOAD} = 2.7nF		20		ns
$V_{LO-FALL}$	LO fall time (90% to 10%)	C_{LOAD} = 2.7nF		8		ns
ADAPTIVE DEADTIME CONTROL						
t_{DEAD1}	HO off to LO on deadtime			25		ns
t_{DEAD2}	LO off to HO on deadtime			15		ns
OVERCURRENT PROTECTION (OCP)						
V_{CS-TH}	CS voltage threshold	Measured from ISNS+ to VOUTS	54	60	66	mV
$t_{DELAY-CS}$	CS delay to output			85		ns
A_{CS}	CS amplifier gain (1)			10		V/V
$I_{BIAS-CS}$	CS amplifier input bias current (1)			0.3		µA
$V_{CS-TH-NEG}$	CS negative voltage threshold	Measured from VOUT to ISNS+		30		mV
AVERAGE OUTPUT CURRENT LIMIT						
$I_{LIM(MIN)}$	Minimum constant current setpoint	R_{SENSE} = 2mΩ, 0xD0 = 0Ah		2		A
$I_{LIM(MIN)}$	Minimum constant current setpoint	R_{SENSE} = 8mΩ, 0xD0 = 0Ah		0.5		A
$I_{LIM(TYP)}$	Maximum constant current setpoint	R_{SENSE} = 2mΩ, 0xD0 = 64h, T_J = –40°C to +85°C	19.2	20	20.8	A
$I_{LIM(TYP)}$	Maximum constant current setpoint	R_{SENSE} = 8mΩ, 0xD0 = 64h, T_J = –40°C to +85°C	4.8	5	5.2	A
$I_{LIM(MAX)}$	Maximum constant current setpoint	R_{SENSE} = 2mΩ, 0xD0 = 96h		30		A
$I_{LIM(MAX)}$	Maximum constant current setpoint	R_{SENSE} = 8mΩ, 0xD0 = 96h		7.5		A
I_{LIM_STEP}	Constant current step size	R_{SENSE} = 2mΩ		200		mA
I_{LIM_STEP}	Constant current step size	R_{SENSE} = 8mΩ		50		mA
OUTPUT CURRENT MONITOR (IMON)						
A_{IMON}	I_{OUT} monitor amplifier gain from V_{CS} to V_{OUT}	V_{CS} = 60mV	24.5	25	25.51	V/V
V_{OFFSET}	I_{OUT} monitor amplifier offset voltage	V_{CS} = 0 mV	0.98	1	1.02	V
CABLE DROP COMPENSATION						
A_{CDC}	Maximum cable drop compensation gain	0xD8[5:0] = 3Fh		62		V/V
A_{CDC_STEP}	Cable drop compensation gain step size			2		V/V
SERIAL CONTROL BUS (SCL, SDA)						
V_{IH}	Input high level				2	V
V_{IL}	Input low level		0.8			V
V_{HYST}	Input hysteresis			320		mV
V_{OL}	Output low level	I_{OL} = 3mA, standard-mode/fast-mode	0		0.4	V
V_{OL}	Output low level	I_{OL} = 20mA, fast-mode plus	0		0.4	V
I_{IH}	Input high current	Pin connected to V_{I2C}	–10		10	µA
I_{IL}	Input low current	Pin connected to GND	–10		10	µA
C_{IN}	Input capacitance			5		pF
THERMAL SHUTDOWN (TSD)						
T_{J-SD}	Thermal shutdown threshold (1)	Temperature rising		175		°C
T_{J-HYS}	Thermal shutdown hysteresis (1)			15		°C

(1) Specified by design. Not production tested.

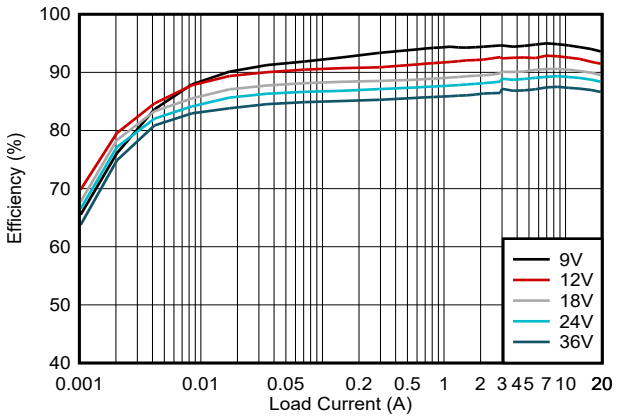
6.6 Timing Requirements for the Serial Control Bus

Over I^2C supply and temperature ranges unless otherwise specified.

			MIN	TYP	MAX	UNIT
f_{SCL}	SCL clock frequency	Standard-mode	> 0		100	kHz
		Fast-mode	> 0		400	kHz
		Fast-mode Plus	> 0		1	MHz
t_{LOW}	SCL low period	Standard-mode	4.7			µs
		Fast-mode	1.3			µs
		Fast-mode Plus	0.5			µs
t_{HIGH}	SCL high period	Standard-mode	4.0			µs
		Fast-mode	0.6			µs
		Fast-mode Plus	0.26			µs
$t_{HD;STA}$	Hold time for a start or a repeated start condition	Standard-mode	4.0			µs
		Fast-mode	0.6			µs
		Fast-mode Plus	0.26			µs
$t_{SU;STA}$	Setup time for a start or a repeated start condition	Standard-mode	4.7			µs
		Fast-mode	0.6			µs
		Fast-mode Plus	0.26			µs
$t_{HD;DAT}$	Data hold time	Standard-mode	0			µs
		Fast-mode	0			µs
		Fast-mode Plus	0			µs
$t_{SU;DAT}$	Data setup time	Standard-mode	250			ns
		Fast -mode	100			ns
		Fast-mode Plus	50			ns
$t_{SU;STO}$	Setup time for STOP condition	Standard-mode	4.0			µs
		Fast-mode	0.6			µs
		Fast-mode Plus	0.26			µs
t_{BUF}	Bus free time between STOP and START	Standard-mode	4.7			µs
		Fast-mode	1.3			µs
		Fast-mode Plus	0.5			µs
t_r	SCL and SDA rise time	Standard-mode			1000	ns
		Fast-mode			300	ns
		Fast-mode Plus			120	ns
t_f	SCL and SDA fall time	Standard-mode			300	ns
		Fast-mode			300	ns
		Fast-mode Plus			120	ns
C_b	Capacitive load for each bus line	Standard-mode			400	pF
		Fast-mode			400	pF
		Fast-mode Plus			550	pF
$t_{VD;DAT}$	Data valid time	Standard-mode			3.45	µs
		Fast-mode			0.9	µs
		Fast-mode Plus			0.45	µs
$t_{VD;ACK}$	Data valid acknowledge time	Standard-mode			3.45	µs
		Fast-mode			0.9	µs
		Fast-mode Plus			0.45	µs
t_{SP}	Input filter	Fast-mode			50	ns
		Fast-mode Plus			50	ns

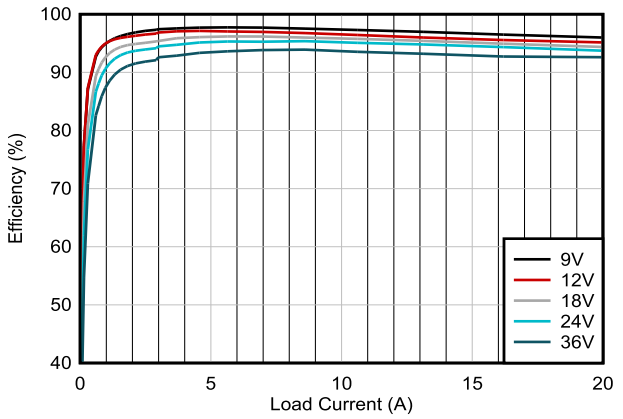
6.7 Typical Characteristics

T_J = 25°C, unless otherwise stated.



V_{OUT} = 6V PFM mode
f_{SW} = 400kHz L_O = 2.2µH

Figure 6-1. Efficiency PFM Mode



V_{OUT} = 6V FPWM mode
f_{SW} = 400kHz L_O = 2.2µH

Figure 6-2. Efficiency FPWM Mode

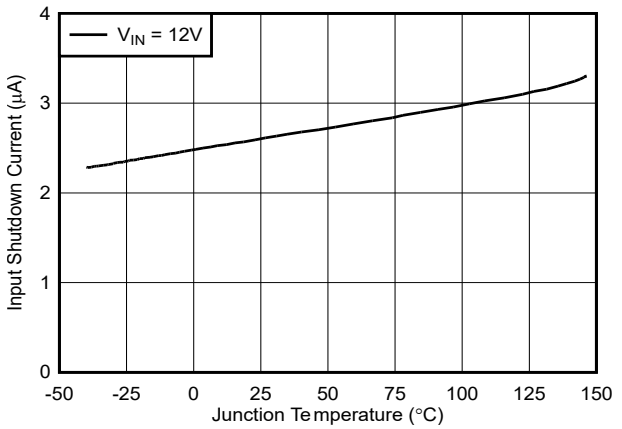


Figure 6-3. Input Shutdown Current vs Temperature

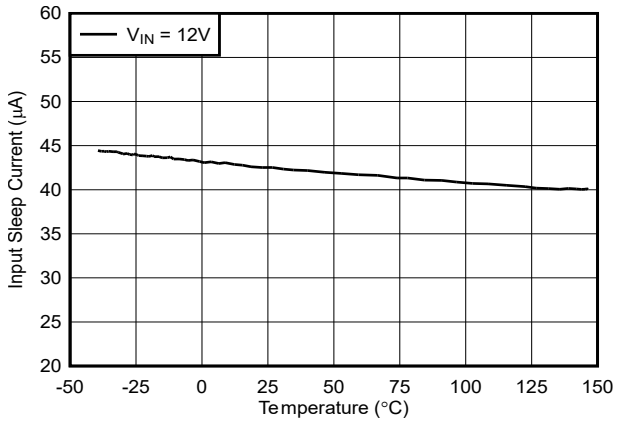


Figure 6-4. Input Sleep Current vs Temperature, V_{OUT} = 5V

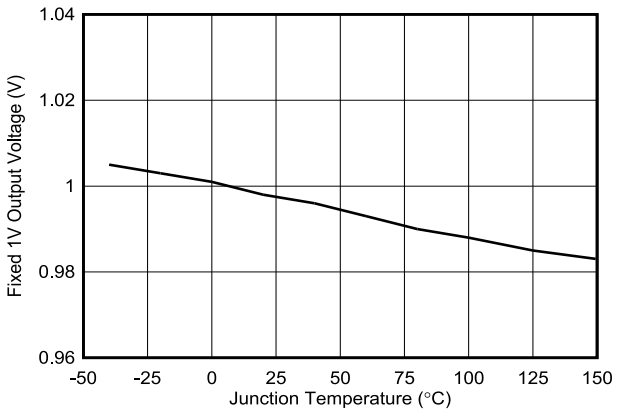


Figure 6-5. Fixed Output Voltage vs Temperature, V_{OUT} = 1V

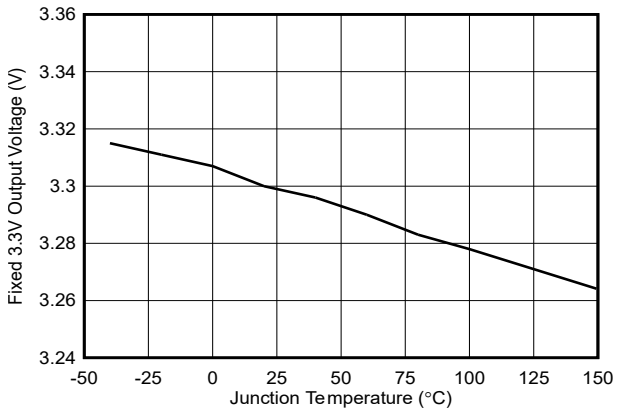


Figure 6-6. Fixed Output Voltage vs Temperature, V_{OUT} = 3.3V

6.7 Typical Characteristics (continued)

T_J = 25°C, unless otherwise stated.

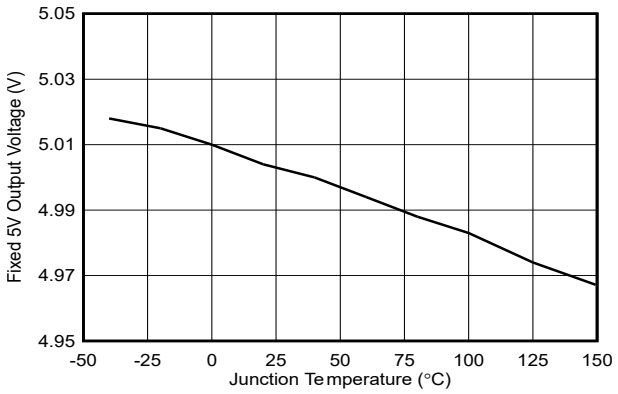


Figure 6-7. Fixed Output Voltage vs Temperature, V_{OUT} = 5V

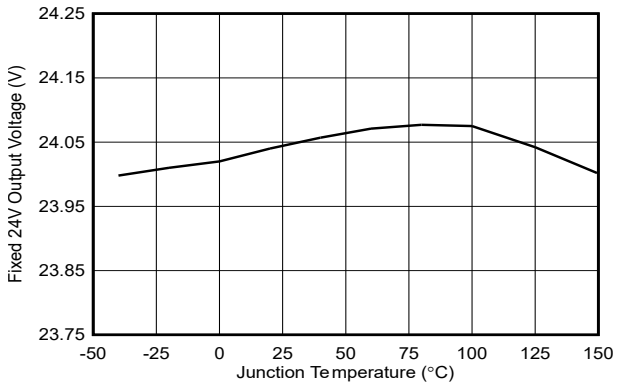


Figure 6-8. Fixed Output Voltage vs Temperature, V_{OUT} = 24V

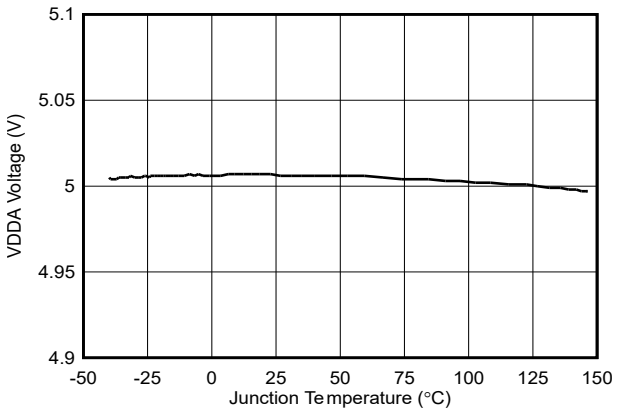


Figure 6-9. VDDA vs Temperature

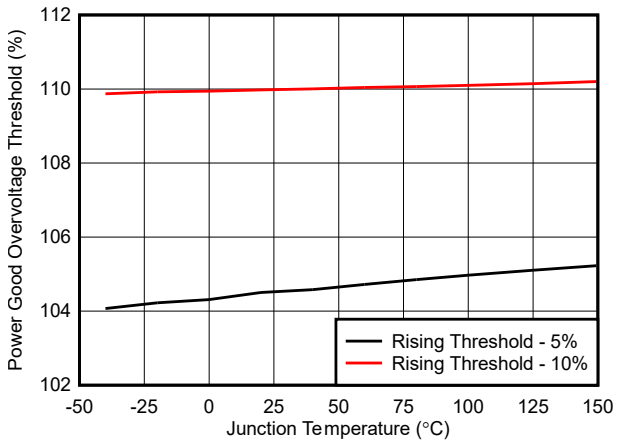


Figure 6-10. PG Overvoltage Threshold vs Temperature

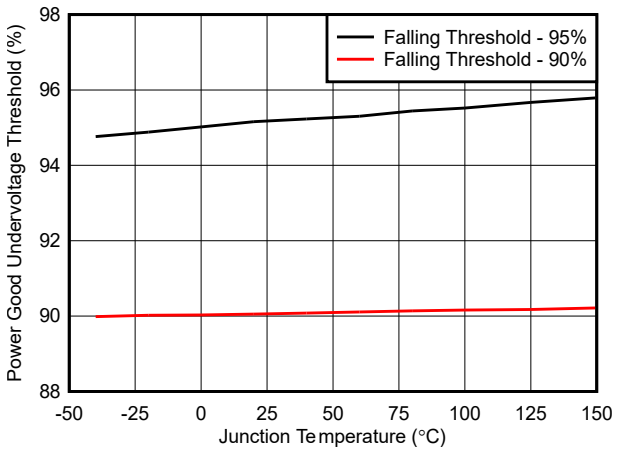


Figure 6-11. PG Undervoltage Threshold vs Temperature

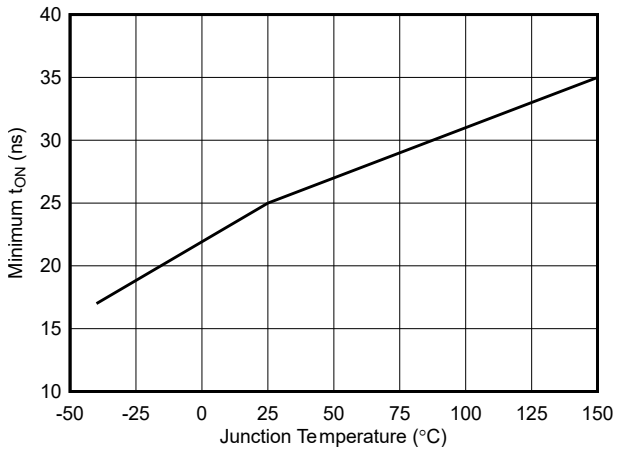


Figure 6-12. Minimum On-Time vs Temperature

6.7 Typical Characteristics (continued)

T_J = 25°C, unless otherwise stated.

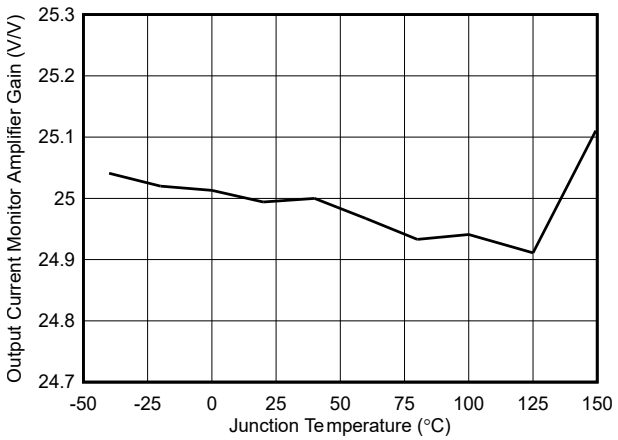


Figure 6-13. IMON Amplifier Gain vs Temperature

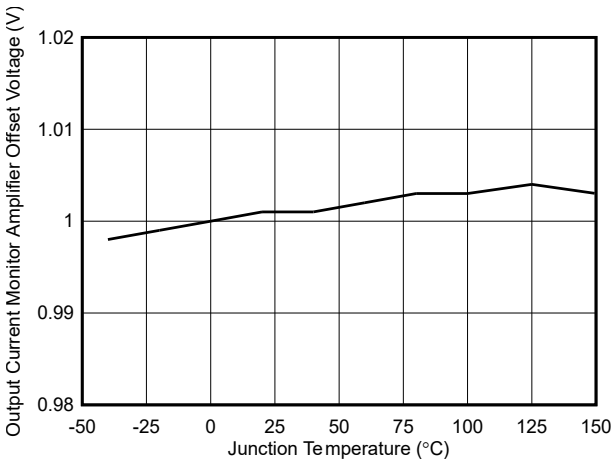


Figure 6-14. IMON Amplifier Voltage Offset vs Temperature

7 Detailed Description

7.1 Overview

The LM25192-Q1 is a 42V, high-efficiency, synchronous buck controller with constant-current constant-voltage (CC-CV) regulation and I^2C interface.

The controller uses a peak current-mode control architecture for easy loop compensation, fast transient response, and excellent load and line regulation. The highly accurate CC-CV operation enables seamless transition between constant-current and constant-voltage modes. The device features integrated dual input (VIN and VOUTF) VCC supply regulator, and oversized VDDA regulator for powering external loads such as companion USB PD controllers. The I^2C interface allows programming of output voltage in 10mV or 20mV steps, average output current limit in 50mA to 200mA steps, as well as output voltage slew rate, switching frequency, soft-start slew rate, mode of operation, current loop compensation, output active discharge strength, and cable drop compensation gain.

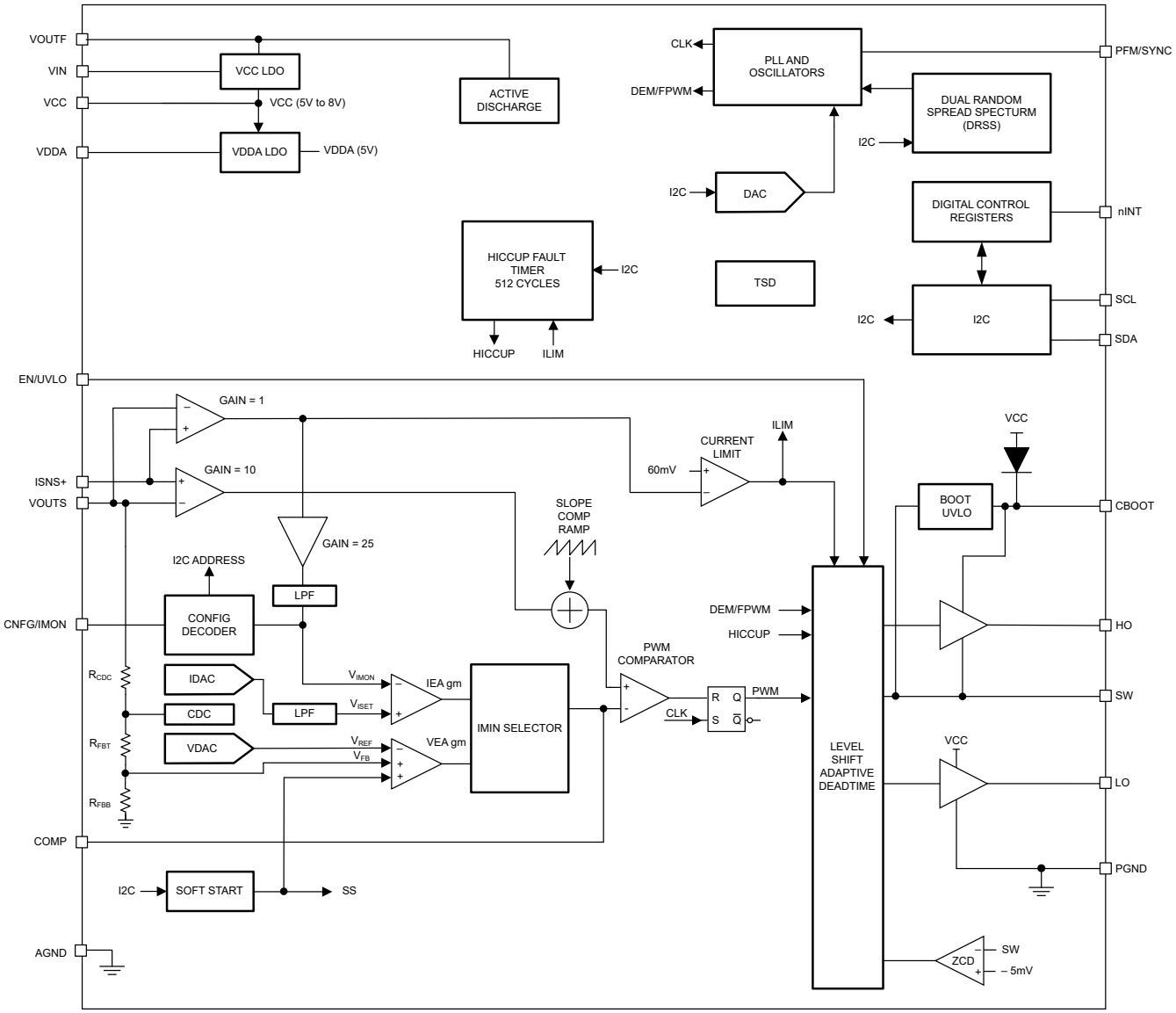
The output can be connected to the VOUTF pin to maximize efficiency in high input voltage applications. A programmable diode emulation feature enables discontinuous conduction mode (DCM) operation to further improve efficiency and reduce power dissipation during light-load conditions.

The LM25192-Q1 also features an array of safety features including output undervoltage and overvoltage protection with programmable thresholds, overcurrent protection with programmable hiccup mode, thermal shutdown, precision enable, and open-drain nINT flag for fault and status reporting.

The LM25192-Q1 incorporates features to simplify the compliance with various EMI standards including CISPR 25 Class 5 that defines automotive EMI requirements. Dual Random Spread Spectrum (DRSS) technique reduces the peak harmonic EMI signature.

LM25192-Q1 is provided in a 19-pin QFN package with the exposed PGND pad to maximize thermal dissipation.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Voltage Range (V_{IN})

The LM25192-Q1 operational input voltage range is from 4.5V to 42V. The device is intended for step-down conversions from 12V and 24V automotive supply rails. The LM25192-Q1 uses internal LDOs to provide a 5V to 8V VCC bias rail and a 5V VDDA rail for the gate drive and control circuits.

In high input voltage applications, make sure that the VIN and SW pins do not exceed the absolute maximum voltage rating of 47V during line or load transient events. Voltage excursions that exceed the absolute maximum ratings of these pins can damage the IC. Follow PCB board layout recommendations and use high-quality input bypass capacitors to minimize voltage overshoot and ringing.

As V_{IN} approaches V_{OUT}, the LM25192-Q1 skips t_{OFF} cycles to allow the controller to extend the duty cycle up to approximately 99%. See also *Input Voltage Range (V_{IN})*.

Use Equation 1 to calculate when the LM25192-Q1 enters dropout mode.

$$V_{IN} = V_{OUT} \times \left(\frac{t_P}{t_P - t_{OFF}}\right) \quad (1)$$

- t_P is the oscillator period
- t_{OFF} is the minimum off time

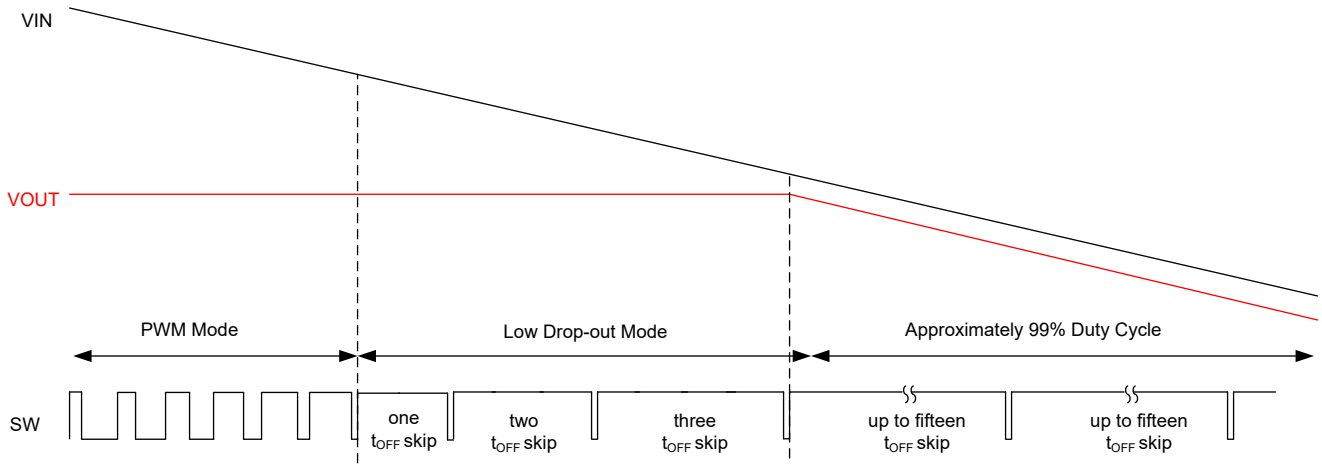


Figure 7-1. Dropout Mode Operation

7.3.2 High-Voltage Bias Supply Regulators (VCC, VDDA)

The LM25192-Q1 contains an internal high-voltage VCC bias regulator that provides the bias supply for the gate drivers for the power MOSFETs. The input voltage pin (VIN) can be connected directly to an input voltage source up to 42V. However, when the input voltage is below the VCC setpoint level, the VCC voltage tracks VIN minus a small voltage drop.

When the output voltage is ≤ 5V, the VCC bias regulator output voltage is 8V. When the output voltage is between 5V and 8V the VCC bias regulator output voltage is tracking the output voltage. When the output voltage is ≥ 8V, the VCC bias regulator output is 8V. TI recommends that a 4.7µF capacitor is connected from the VCC pin to PGND.

The LM25192-Q1 also contains a linear regulator, VDDA, that takes the VCC regulator output as an input, and generates a 5V output. The VDDA powers internal control circuitry including the digital block. The VDDA can also power external companion USB Type-C controller device. Bypass VDDA with a 22µF ceramic capacitor to achieve a low-noise internal bias rail.

7.3.3 Enable (EN)

The enable pin can be connected to a voltage as high as 42V. If the EN pin is pulled below 0.55V, the LM25192-Q1 is in shutdown mode with an I_Q of 2.4µA (typical) current draw from V_{IN}. When the enable voltage is between 0.55V < EN < 1V, the LM25192-Q1 is in standby mode. When in standby mode, the VCC regulator is enabled, default registers and trim bits loaded, the digital block is disabled, the device is not switching, and the I_Q current is 310µA (typical). When the enable voltage is above 1V, the LM25192-Q1 is in ready mode after the 100µs (typical) enable to ready delay. When in ready mode, the I^2C interface is available, the device is not switching, and the I_Q current is 1mA (typical). The LM25192-Q1 starts up and enters active mode, when the CONTROLLER_EN bit in the OPERATION register is set.

7.3.4 Switching Frequency

The LM25192-Q1 oscillator is programmed by setting the FREQ bits in the MFG_DEVICE_CFG_D1 device configuration register according to the following table.

Table 7-1. Switching Frequency Selection

MFG_DEVICE_CFG_D1[4:3]	SWITCHING FREQUENCY SELECTION
0b00	200kHz
0b01	400kHz (default)
0b10	600kHz
0b11	2.2MHz

Under low V_{IN} conditions when the high-side MOSFETs on-time exceeds the programmed oscillator period, the LM25192-Q1 extends the switching period of that channel until the PWM latch is reset by the current sense ramp exceeding the controller compensation voltage. In such an event, the oscillators operate independently and asynchronously until the channel can maintain output regulation at the programmed frequency. Equation 2 gives the approximate input voltage level below which this phenomenon occurs, where t_{SW} is the switching period and $t_{OFF(min)}$ is the minimum off-time of 80ns.

$$V_{IN(min)} = V_{OUT} \times \left(\frac{t_{SW}}{t_{SW} - t_{OFF(min)}} \right) \quad (2)$$

7.3.5 Dual Random Spread Spectrum (DRSS)

The LM25192-Q1 provides a Dual Random Spread Spectrum (DRSS) function, which reduces the EMI of the power supply over a wide frequency range. The DRSS function combines a low-frequency triangular modulation profile with a high frequency cycle-by-cycle random modulation profile. The low frequency triangular modulation improves performance in the lower radio frequency bands, while the high frequency random modulation improves performance in the higher radio frequency bands.

Spread spectrum works by converting a narrowband signal into a wideband signal which spreads the energy over multiple frequencies. Industry standards require different spectrum analyzer resolution bandwidth (RBW) settings for different frequency bands. The RBW has an impact on the spread spectrum performance. For example, the CISPR-25 requires 9kHz RBW for the 150kHz to 30MHz frequency band. For frequencies greater than 30MHz, the required RBW is 120kHz. DRSS is able to simultaneously improve the EMI performance in the high and low RBWs with the low-frequency triangular modulation and high-frequency cycle-by-cycle random modulation as shown in Figure 7-2. In the low-frequency band (150kHz – 30MHz), the DRSS function can reduce the conducted emissions by as much as 15dBµV, and in the high-frequency band (30MHz – 108MHz) by as much as 5dBµV.

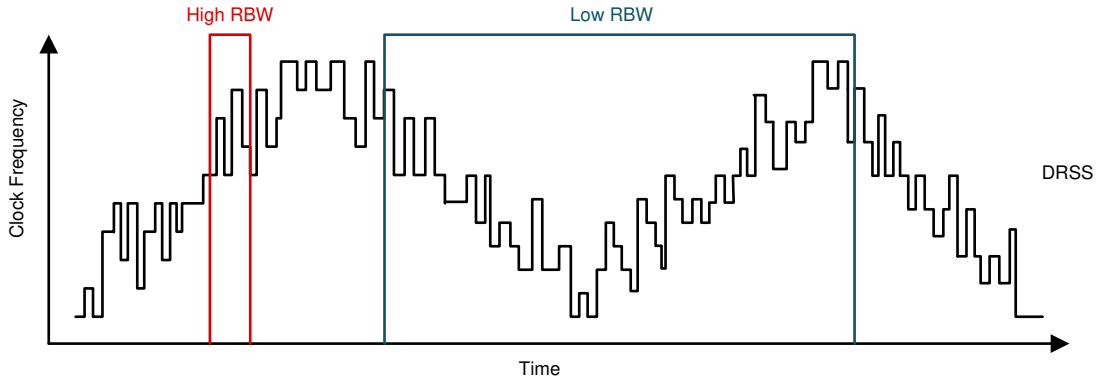


Figure 7-2. Dual Random Spread Spectrum Implementation

Enable the DRSS function by setting the EN_DRSS bit in the MFG_DEVICE_CFG_D1 device configuration register. Note that the external clock synchronization through the PFM/SYNCIN pin is not possible when the DRSS function is enabled.

The LM25192-Q1 also supports two modulation frequencies that can be selected by setting the DRSS_FMOD bit in the MFG_DEVICE_CFG_D1 device configuration register according to Table 7-2.

Table 7-2. DRSS Modulation Frequency Selection

DRSS_FMOD	MODULATION FREQUENCY
0b0	10kHz
0b1	2.5kHz

7.3.6 Soft Start

The LM25192-Q1 has a programmable soft-start slew rate. The soft-start feature allows the regulator to gradually reach the steady-state operating point, therefore reducing start-up stresses and surges.

The soft-start slew rate can be selected using the SOFT_START_TIME bit in the MFG_DEVICE_CFG_D2 device configuration register according to Table 7-3.

Table 7-3. Soft-Start Slew Rate Selection

SOFT_START_TIME	SOFT-START SLEW RATE	
	20mV VOUT STEP SIZE	10mV VOUT STEP SIZE
0b0	5V/ms	2.5V/ms
0b1	2.5V/ms	1.25V/ms

7.3.7 Output Voltage

The LM25192-Q1 output voltage can be programmed from 1V to 24V in 10mV steps or from 3.3V to 24V in 20mV steps by setting bits in the VOUT_COMMAND register. Prior to programming the output voltage, select the output voltage step size and range by setting the SEL_FB_DIV20 bit in the MFG_DEVICE_CFG_D1 device configuration register according to Table 7-4.

Table 7-4. Output Voltage Step Size and Range Selection

SEL_FB_DIV20	OUTPUT VOLTAGE STEP SIZE	OUTPUT VOLTAGE RANGE
0b0	10mV	1V – 24V
0b1	20mV	3.3V – 24V

7.3.8 Minimum Controllable On-Time

There are two limitations to the minimum output voltage adjustment range: the LM25192-Q1 voltage reference and the minimum controllable switch-node pulse width, $t_{ON(min)}$.

$t_{ON(min)}$ effectively limits the voltage step-down conversion ratio V_{OUT}/V_{IN} at a given switching frequency. For fixed-frequency PWM operation, the voltage conversion ratio must satisfy Equation 3.

$$\frac{V_{OUT}}{V_{IN}} > t_{ON(min)} \times F_{SW} \quad (3)$$

where

- $t_{ON(min)}$ is 25ns (typical).
- F_{SW} is the switching frequency.

If the desired voltage conversion ratio does not meet the above condition, the LM25192-Q1 transitions from a fixed switching frequency operation mode to a pulse-skipping mode to maintain output voltage regulation.

For wide V_{IN} applications and low output voltages, an alternative is to reduce the LM25192-Q1 switching frequency to meet the requirement of Equation 3.

7.3.9 Dual Loop Architecture

The LM25192-Q1 has two control loops, a voltage loop and a current loop, and an IMIN selector block that compares output currents from the voltage loop error amplifier and the current loop error amplifier. The IMIN selector block selects the lower current to take the control of the constant voltage (CV) or constant current (CC) regulation. The block enables seamless transition between CC an CV operation, and is shown in the following figure.

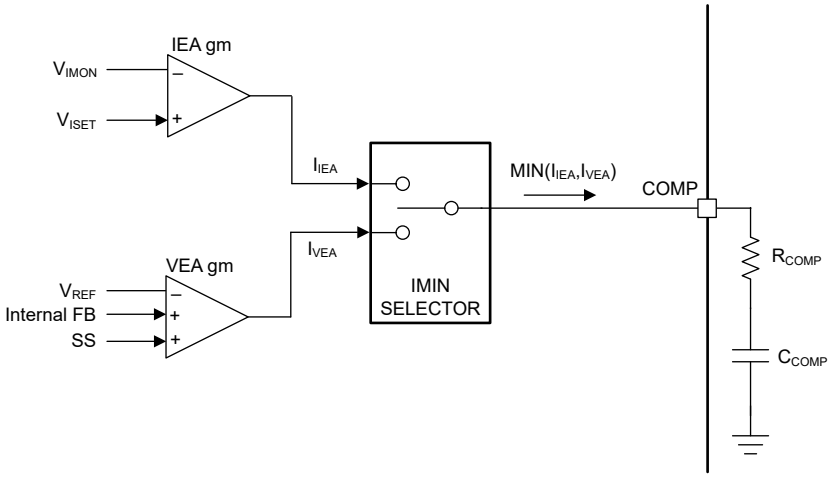


Figure 7-3. Dual Loop Architecture Block Diagram

7.3.9.1 Voltage Loop Error Amplifier

In the voltage control loop, the LM25192-Q1 has a high-gain transconductance amplifier that generates an error current proportional to the difference between the internal feedback voltage and a programmable precision reference, V_{REF}. The transconductance of the amplifier is 1000µS. The voltage loop error amplifier takes the control when the internal minimum function block, IMIN SELECTOR, selects the current from the voltage loop error amplifier as shown in the following figure.

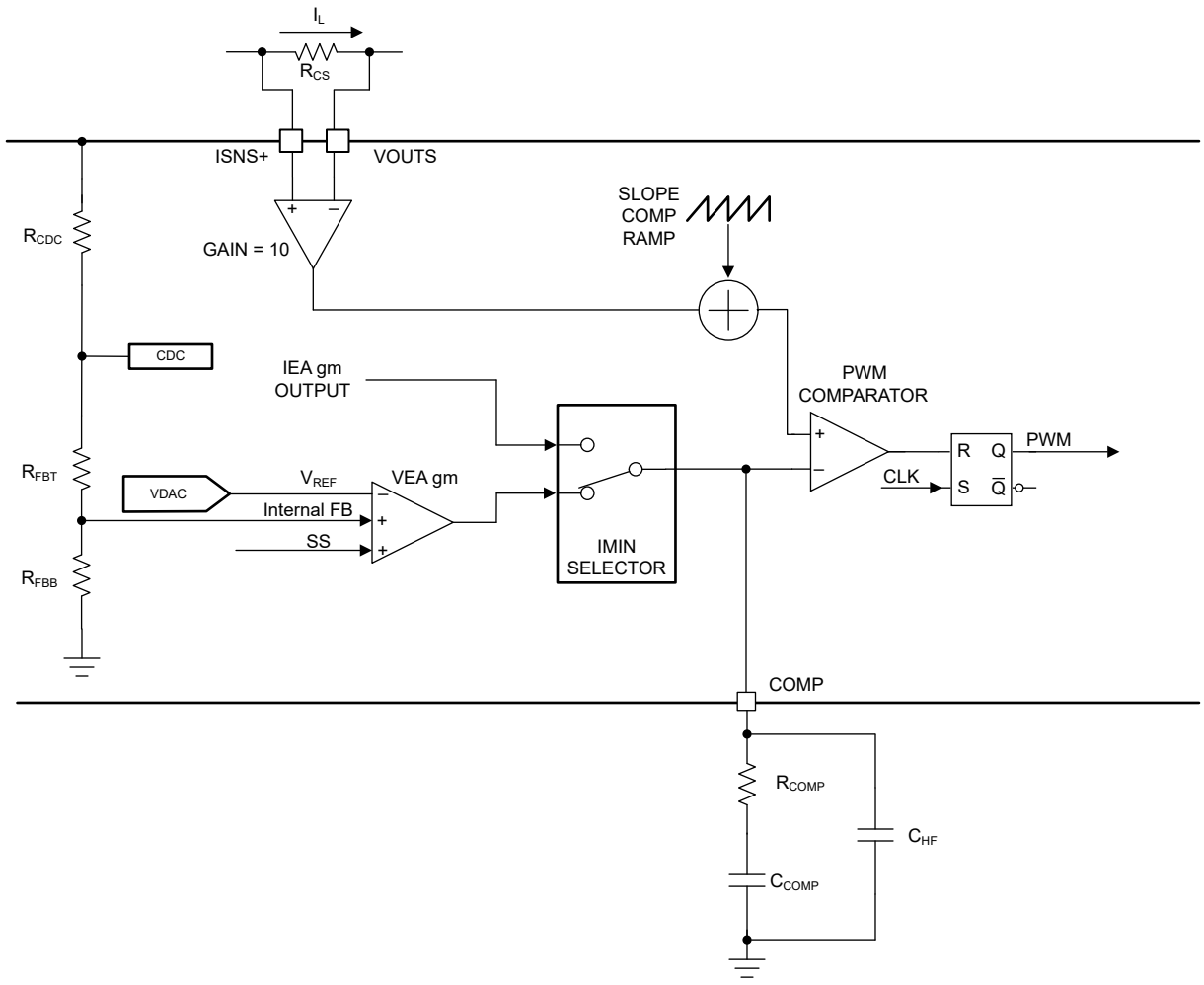


Figure 7-4. Voltage Loop Functional Block Diagram

The voltage control loop requires an external compensation network. TI generally recommends a type-II compensation network for peak current-mode control.

7.3.9.2 Current Loop Error Amplifier

In the current control loop, the LM25192-Q1 has a high-gain transconductance amplifier that generates an error current proportional to the difference between the IMON voltage, V_{IMON}, and the programmable ISET reference voltage, V_{ISET}. The transconductance of the amplifier is 1000µS. The current loop error amplifier takes the control when the internal minimum function block, IMIN SELECTOR, selects the current from the current loop error amplifier as shown in the following figure.

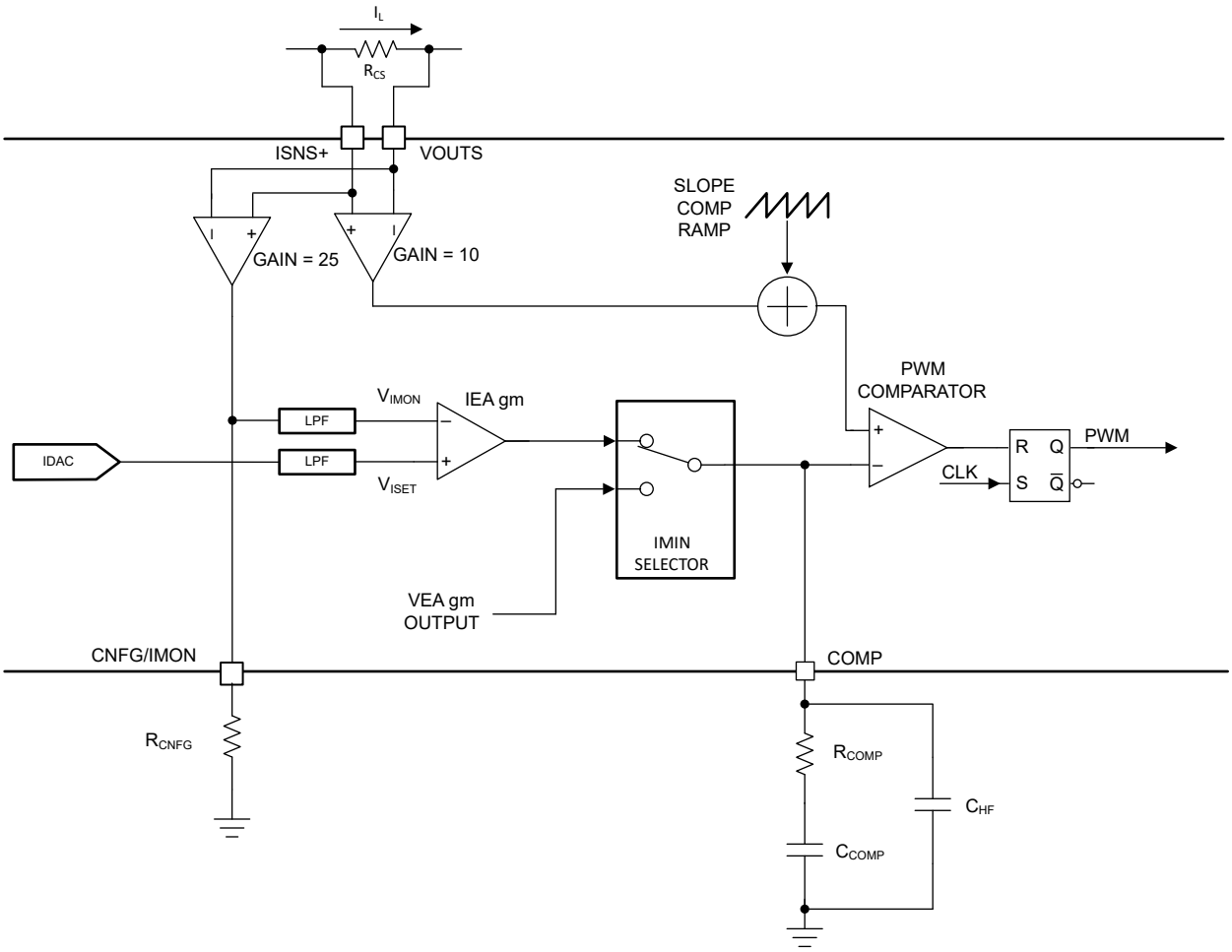


Figure 7-5. Current Loop Functional Block Diagram

7.3.10 Programmable ILIM

The LM25192-Q1 has a programmable average output current limit.

The average output current limit is set by programming an internal 8-bit DAC. Use the AVG_ILIM_THRESHOLD field in the register 0xD0 to set the average output current limit between 0.5A – 2A and 7.5A – 30A in 50mA – 200mA steps with a recommended 8mΩ – 2mΩ sense resistor.

7.3.11 IOUT Monitor

The LM25192-Q1 has the IMON pin that can be used as the average inductor current or regulator output current monitor when the regulator is operating in the constant voltage control loop. The average inductor current can be read from the voltage on the IMON pin by using Equation 4.

$$I_{AVG} = \frac{V_{IMON} - V_{OFFSET}}{A_{IMON} \times R_S} \quad (4)$$

where

- V_{IMON} is the voltage on the IMON pin.
- V_{OFFSET} is the output current monitor amplifier offset voltage of 1V (typical).
- A_{IMON} is the output current monitor amplifier gain of 25V/V (typical).
- R_S is the sense resistor of 8mΩ (typical).

7.3.12 Cable Drop Compensation

The LM25192-Q1 has a cable drop compensation (CDC) feature. The CDC feature increases the output voltage based on the output current and the programmable CDC gain to offset the voltage drop across a USB cable. The CDC gain is programmable from 0V/V to 62V/V in 2V/V steps. Set the CDC gain to a value closest to the ratio of the cable resistance and the sense resistor, R_S. For example, if the cable resistance is 150mΩ and the selected sense resistor is 8mΩ, the desired CDC gain is calculated as 150mΩ / 8mΩ = 18.75. The closest programmable CDC gain value is 18V/V.

Use the CDC_EN bit in the register 0xD8 to enable the cable drop compensation. Set the CDC gain using the CDC_GAIN_CFG field in the 0xD8 register. For example, to set the CDC gain to 18V/V, set the CDC_GAIN_CFG field to 18V/V / 2V/V(LSB) = 9h.

7.3.13 Slope Compensation

The LM25192-Q1 provides internal slope compensation for stable operation with peak current-mode control and a duty cycle greater than 50%. Calculate the buck inductance to provide a slope compensation contribution equal to one times the inductor downslope using the following equation.

$$L_{O(sc)} = \frac{V_{OUT}[V] \times R_S[m\Omega]}{24 \times F_{SW}[MHz]} \quad (5)$$

- A lower inductance value increases the peak-to-peak inductor current, which typically minimizes size and cost, and improves transient response at the cost of reduced light-load efficiency due to higher cores losses and peak currents.
- A higher inductance value decreases the peak-to-peak inductor current, which typically increases the full-load efficiency by reducing switch peak and RMS currents at the cost of requiring larger output capacitors to meet load-transient specifications.

7.3.14 Shunt Current Sensing

Figure 7-6 shows inductor current sensing using a shunt resistor. This configuration continuously monitors the inductor current to provide accurate overcurrent protection across the operating temperature range. For optimal current sense accuracy and overcurrent protection, use a low inductance ±1% tolerance shunt resistor between the inductor and the output, with a Kelvin connection to the LM25192-Q1 current sense amplifier.

If the peak differential current signal sensed from ISNS+ to VOUT exceeds the current limit threshold of 60mV, the current limit comparator immediately terminates the high-side gate driver output for cycle-by-cycle current limiting. Use the following equation to calculate the shunt resistance.

$$R_S = \frac{V_{CS(TH)}}{I_{OUT(CL)} + \frac{\Delta I_L}{2}} \quad (6)$$

where

- $V_{CS(TH)}$ is current sense threshold of 60mV.
- $I_{OUT(CL)}$ is the overcurrent setpoint that is set higher than the maximum load current to avoid tripping the overcurrent comparator during load transients.
- ΔI_L is the peak-to-peak inductor ripple current.

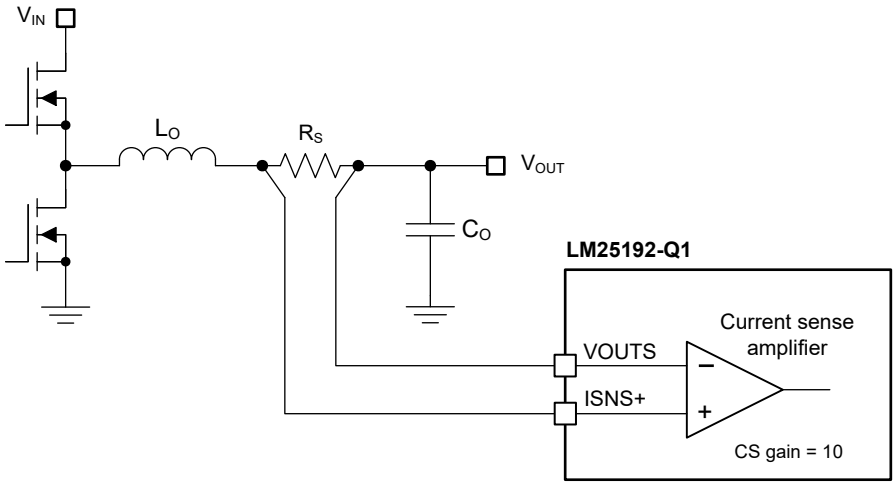


Figure 7-6. Shunt Current Sensing Implementation

The typical current sense delay ($t_{DELAY(CS)}$) is 85ns. Use the following equation to calculate the resultant inductor current overshoot above the overcurrent threshold.

$$I_{L(overshoot)} = \frac{(V_{IN} - V_{OUT}) \times t_{DELAY(CS)}}{L_O} \quad (7)$$

The respective SS voltage is clamped 75mV above FB during an overcurrent condition. 8x overcurrent events must occur before the SS clamp is enabled. This requirement makes sure that SS can be pulled low during brief overcurrent events, preventing output voltage overshoot during recovery.

7.3.15 Hiccup Mode Current Limiting

The LM25192-Q1 includes an internal hiccup mode protection function. When an overload condition occurs, a 512-cycle counter starts counting consecutive cycle-by-cycle current limit incidents after the internal soft-start sequence is completed. The 512-cycle counter is reset if four consecutive switching cycles occur without exceeding the current limit threshold. If after 512-cycle counts are completed, the internal soft start is pulled low and the internal high-side and low-side drivers are disabled. Then, a 16384 counter is enabled. After the counter reaches 16384, the internal soft start is enabled, and the output restarts. Note the hiccup mode current limit is not enabled during soft start and until the output voltage exceeds 50% of the set voltage.

The hiccup mode can be enabled or disabled using the HICCUP_EN bit.

7.3.16 Device Configuration (CNFG)

The LM25192-Q1 I2C address is configured as detailed in Table 7-5.

After VDDA is above 3.8V (typical), the CNFG pin is sampled and latched. The configuration cannot be changed easily. The LM25192-Q1 input voltage must be recycled and VCC must drop below 3.65V before the device can be reconfigured. Figure 7-7 shows the configuration timing diagram.

Table 7-5. Device Configuration

I2C ADDRESS	R_{CNFG}		
	MIN	TYP	MAX
0x6A	40.2kΩ	49.9kΩ	57.6kΩ
0x6C	18.2kΩ	25kΩ	31kΩ

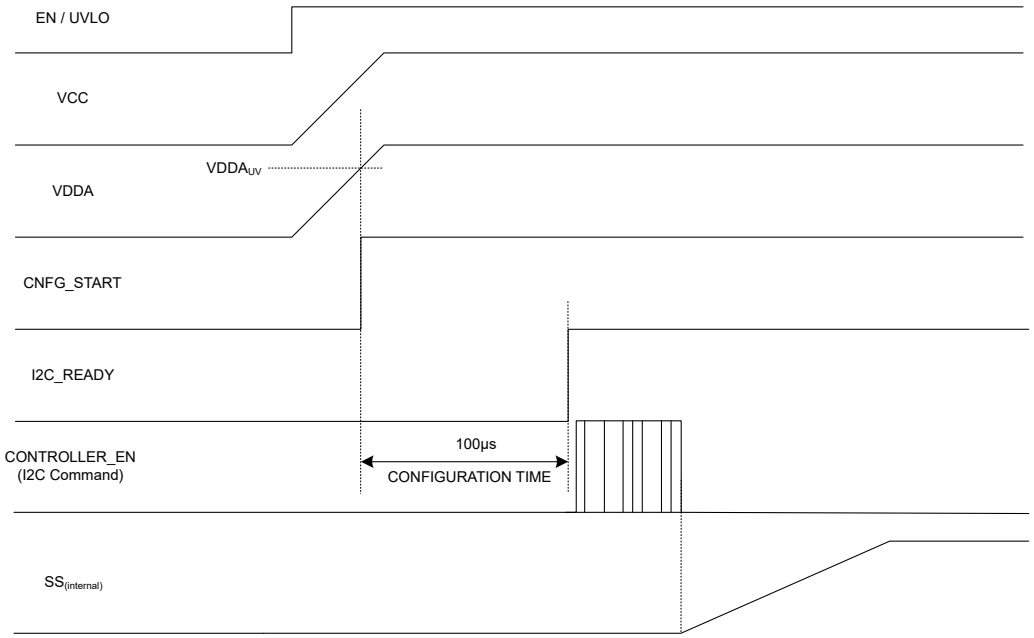


Figure 7-7. Configuration Timing

7.3.17 Pulse Frequency Modulation (PFM) / Synchronization

The LM25192-Q1 provides a diode emulation feature that can be enabled to prevent reverse (drain-to-source) current flow in the low-side MOSFET. When configured for Pulse Frequency Modulation(PFM), the low-side MOSFET is switched off when reverse current flow is detected by sensing of the SW voltage using a zero-cross comparator. The benefit of this configuration is lower power loss during light load operation. Note that configuring the device for PFM has an effect of slower response to load transients during light load operation.

The diode emulation feature is configured with the PFM / SYNC pin. To enable diode emulation and achieve discontinuous conduction mode (DCM) operation at light loads, connect PFM / SYNC to VDDA. If forced pulse-width modulation (FPWM) or continuous conduction mode (CCM) operation is desired, tie PFM / SYNC to AGND. Note that diode emulation is automatically engaged to prevent reverse current flow during a prebias start-up in PFM. During start-up, when the output voltage approaches the regulation set point a gradual change from DCM to CCM occurs, preventing the output voltage overshoot. Changing the mode of operation dynamically is possible, however, the rate of change must be < 10Hz. The time to transition from PFM to FPWM operation is dependent on the output load current. In a typical application, the transition from PFM to FPWM operation occurs in less than 1ms if the output current is greater than 100mA. Similarly, for the output currents of around 1mA, the transition generally occurs in tens of milliseconds. This transition can be sped up by enabling output active discharge during the transition between PFM and FPWM by setting the ACTIVE_DISCHARGE_CFG2 bit high in register 0xD2. This output active discharge current can be set from

24mA – 72mA through register 0xD2 and is only enabled until the transition to FPWM is complete, which typically takes several hundred microseconds.

To synchronize the LM25192-Q1 to an external source, apply a logic-level clock (greater than 2V) to the PFM / SYNC pin. The LM25192-Q1 can be synchronized to ±20% of the programmed frequency up to a maximum of 2.2MHz. Under low V_{IN} conditions when the minimum off-time is reached, the synchronization signal is ignored, allowing the switching frequency to be reduced to maintain output voltage regulation.

When operating in PFM mode, TI does not recommend to operate the part with an output voltage above 22V when the SEL_FB_DIV20 bit is set low.

7.3.18 Out-of-Audio Operation

When operating in PFM mode under light load conditions, the effective switching frequency can be in the audible frequency range (<20kHz). For applications requiring switching frequency to be outside of the audible range (>20kHz), the LM25192-Q1 provides an out-of-audio feature that can limit the switching frequency to 20kHz with minimal load.

Enable the out-of-audio operation while in PFM mode by setting the OUT_OF_AUDIO bit to high (0xD9[2] = 1b). With the out-of-audio enabled, the minimum inductor peak current criteria for PFM switching is disabled allowing much less energy to be delivered to the output each cycle. This dramatically reduces the minimum output current required to switch continuously at the nominal switching frequency. Additionally, the maximum number of skipped off times while in dropout is reduced from 16x to 8x when the switching frequency is set to 200kHz.

7.3.19 Thermal Shutdown (TSD)

The LM25192-Q1 includes an internal junction temperature monitor. If the temperature exceeds 175°C (typical), thermal shutdown occurs. When entering thermal shutdown, the device:

1. Turns off the high-side and low-side MOSFETs
2. Turns off the VCC regulator
3. Sets the TEMPERATURE bit in the STATUS_BYTE and STATUS_WORD registers
4. Initiates a soft-start sequence when the die temperature decreases by the thermal shutdown hysteresis of 15°C (typical).

This protection is a non-latching protection, therefore, the device cycles into and out of thermal shutdown if the fault persists. If VCC or VDDA fall below the respective UVLO thresholds while in thermal shutdown, the LM25192-Q1 clears the STATUS_BYTE and STATUS_WORD registers upon exiting thermal shutdown.

7.4 Device Functional Modes

7.4.1 Shutdown Mode

The EN / UVLO pin provides ON and OFF control for the LM25192-Q1. When V_{EN} is below 0.55V, the device is in shutdown mode. Both the internal LDO and the switching regulator are off. The quiescent current in shutdown mode drops to 2.4µA (typical). The LM25192-Q1 also includes undervoltage (UV) protection of the internal bias LDO. If the internal bias supply voltage is below the UV threshold level, the switching regulator remains off.

7.4.2 Standby Mode

The internal bias LDO has a lower enable threshold than the switching regulator. When V_{EN} is above 0.55V and below the precision enable threshold (1V typical), the internal VCC and VDDA LDOs are enabled and regulating, the default register values and trim bits are loaded, the digital block is disabled, the device is not switching, and the I_Q current is 310µA (typical).

7.4.3 Ready Mode

When the enable voltage is above 1V and after the 100µs (typical) enable to ready delay, the LM25192-Q1 is in ready mode. When in ready mode, the I^2C interface is available, the device is not switching, and the I_Q current is 1mA (typical).

7.4.4 Active Mode

The LM25192-Q1 is in active mode when V_{EN} is above the precision enable threshold, the internal bias rail is above the UV threshold level, and when the CONTROLLER_EN bit in the OPERATION register is set. In active mode, the device operates in one of two modes depending on the load current, input voltage, output voltage, and PFM / SYNC pin configuration:

1. Forced pulse width modulation (FPWM) mode. This mode of operation is configured by tying the PFM / SYNC pin to GND or driving with an external clock source. The device operates in continuous conduction mode (CCM) with fixed switching frequency regardless of the load current.
2. Pulse frequency modulation (PFM) mode. This mode of operation is configured by tying the PFM / SYNC pin to VDDA. The device operates in discontinuous conduction mode (DCM) if the load current is less than half of the peak-to-peak inductor current, otherwise the device operates in continuous conduction mode (CCM). The transition between CCM and DCM is automatic.

7.4.5 Sleep Mode

The LM25192-Q1 operates with peak current-mode control such that the compensation voltage is proportional to the peak inductor current. During no-load or light-load conditions, the output capacitor discharges slowly. As a result, the compensation voltage goes low and the switching is stopped. When the LM25192-Q1 controller detects 16 missed switching cycles, the LM25192-Q1 enters sleep mode and switches to a low $I_{Q\text{-}SLEEP}$ state to reduce the current drawn from the input. For the LM25192-Q1 to go into sleep mode, the device must be programmed for PFM mode.

8 Programming

8.1 I²C Bus Operation

The I 2 C bus is a communications link between a controller and a series of target devices. The link is established using a two-wired bus consisting of a serial clock signal (SCL) and a serial data signal (SDA). The serial clock is sourced from the controller in all cases where the serial data line is bi-directional for data communication between the controller and the target terminals. Each device has an open-drain output to transmit data on the serial data line (SDA). Place an external pullup resistor on the serial data line to pull the drain output high during data transmission. The device hosts a target I 2 C that supports standard-mode, fast-mode and fast-mode plus operation with data rates up to 100kbit/s, 400kbit/s and 1000kbit/s respectively and auto-increment addressing compatible to I 2 C standard 3.0.

The 7 bit target address of this device is set by CNFG pin according to Table 7-5.

Data transmission is initiated with a start bit from the controller as shown in the figure below. The start condition is recognized when the SDA line transitions from high to low during the high portion of the SCL signal. Upon reception of a start bit, the device receives serial data on the SDA input and checks for a valid address and control information. If the target address bits are set for the device, then the device issues an acknowledge pulse and prepares to receive the register address and data. Data transmission is completed by either the reception of a stop condition or the reception of the data word sent to the device. A stop condition is recognized as a low to high transition of the SDA input during the high portion of the SCL signal. All other transitions of the SDA line targeted to occur during the low portion of the SCL signal for valid communication. An acknowledge is issued after the reception of valid address, sub-address, and data words. The I 2 C interfaces auto-sequence through register addresses, to send multiple data words for a given I 2 C transmission.

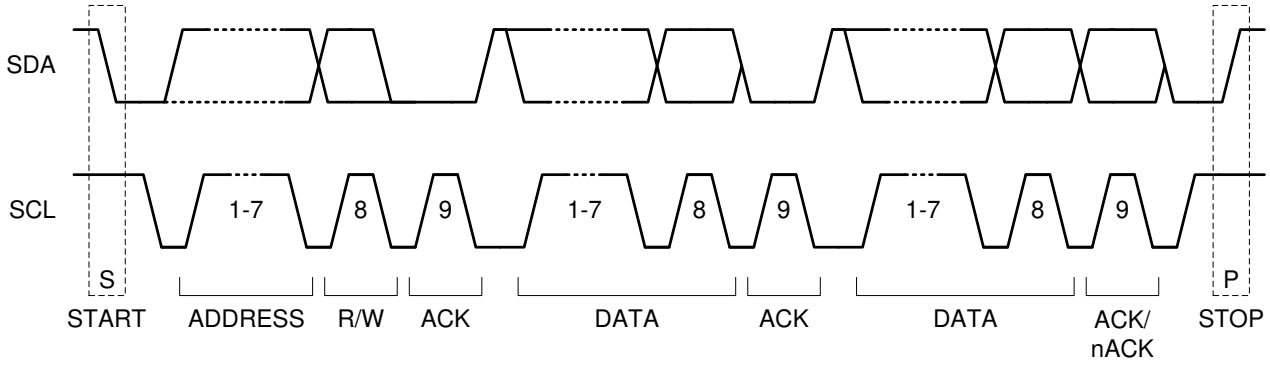


Figure 8-1. I 2 C START / STOP / ACKNOWLEDGE Protocol

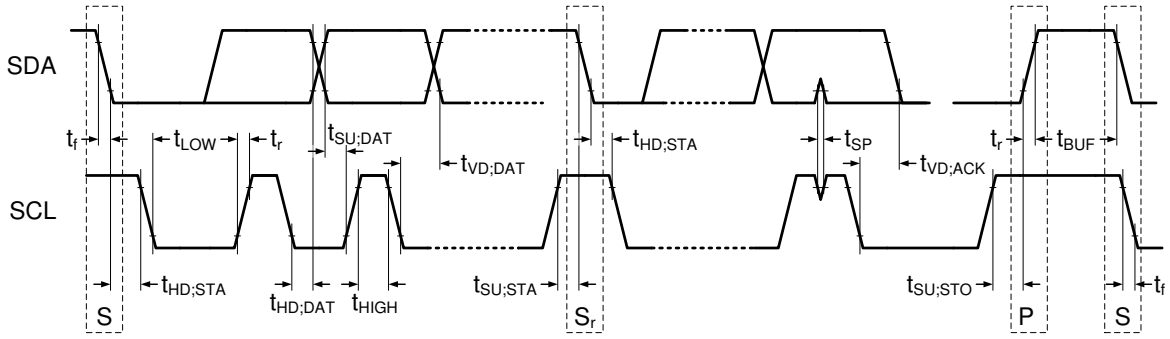


Figure 8-2. I 2 C Data Transmission Timing

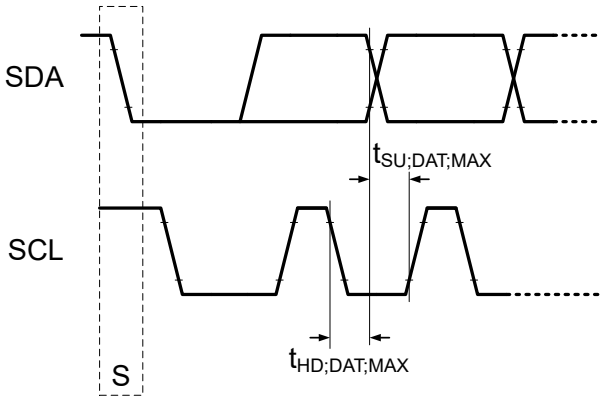


Figure 8-3. I 2 C Data Transmission Timing for Maximum Rise and Fall Times

8.2 Clock Stretching

Clock stretching is not supported. If the device is addressed while busy and not able to process the received data, the transaction is not acknowledged. TI recommends using this device in I2C systems with an I2C timeout feature.

8.3 Data Transfer Formats

The device supports four different read/write operations:

- Single read from a defined register address
- Single write to a defined register address
- Sequential read starting from a defined register address
- Sequential write starting from a defined register address

8.4 Single READ from a Defined Register Address

Figure 8-4 shows the format of a single read from a defined register address. First, the controller issues a start condition followed by a seven-bit I 2 C address. Next, the controller writes a zero to signify that the controller is conducting a write operation. Upon receiving an acknowledge from the target the controller sends the eight-bit register address across the bus. Following a second acknowledge the device sets the internal I 2 C register number to the defined value. Then the controller issues a repeat start condition and the seven-bit I 2 C address followed by a one to signify that the controller is conducting a read operation. Upon receiving a third acknowledge, the controller releases the bus to the device. The device then returns the eight-bit data value from the register on the bus. The controller does not acknowledge (nACK) and issues a stop condition. This action concludes the register read.

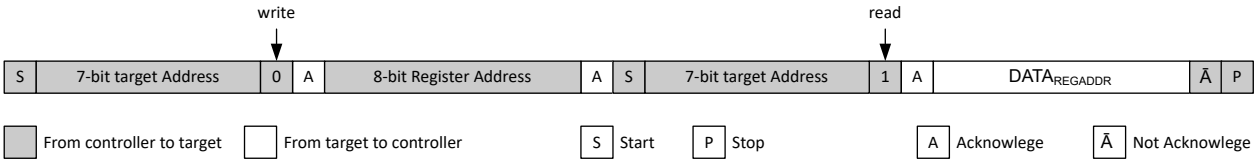


Figure 8-4. Single READ From a Defined Register Address

8.5 Sequential READ Starting from a Defined Register Address

A sequential read operation is an extension of the single read protocol and shown in Figure 8-5. The controller acknowledges the reception of a data byte, and the device auto increments the register address and returns the data from the next register. The data transfer is stopped by the controller not acknowledging the last data byte and sending a stop condition.

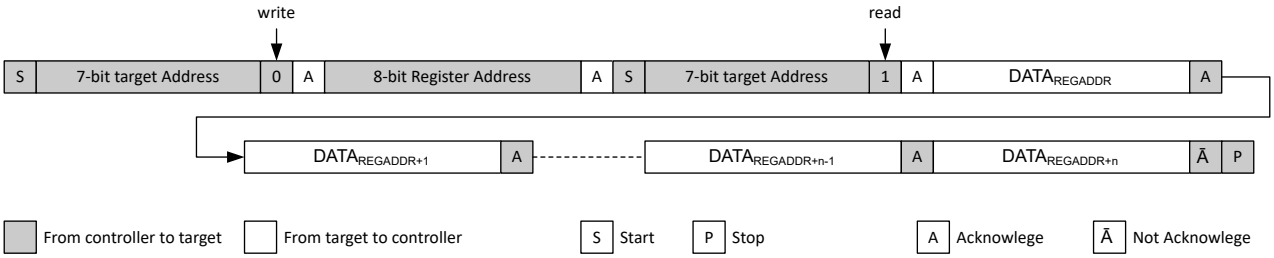


Figure 8-5. Sequential READ Starting from a Defined Register Address

8.6 Single WRITE to a Defined Register Address

Figure 8-6 shows the format of a single write to a defined register address. First, the controller issues a start condition followed by a seven-bit I ^{2} C address. Next, the controller writes a zero to signify that the controller is trying to conduct a write operation. Upon receiving an acknowledge from the target, the controller sends the eight-bit register address across the bus. Following a second acknowledge the device sets the I ^{2} C register address to the defined value and the controller writes the eight-bit data value. Upon receiving a third acknowledge the device auto increments the I ^{2} C register address by one and the controller issues a stop condition. This action concludes the register write.

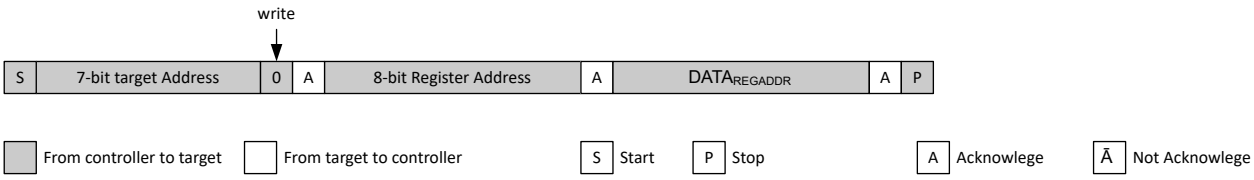


Figure 8-6. Single WRITE to Defined Register Address

8.7 Sequential WRITE Starting at a Defined Register Address

A sequential write operation is an extension of the single write protocol and shown in Figure 8-7. If the controller does not send a stop condition after the device has issued an ACK, the device auto increments the register address by one and the controller is able to write to the next register.

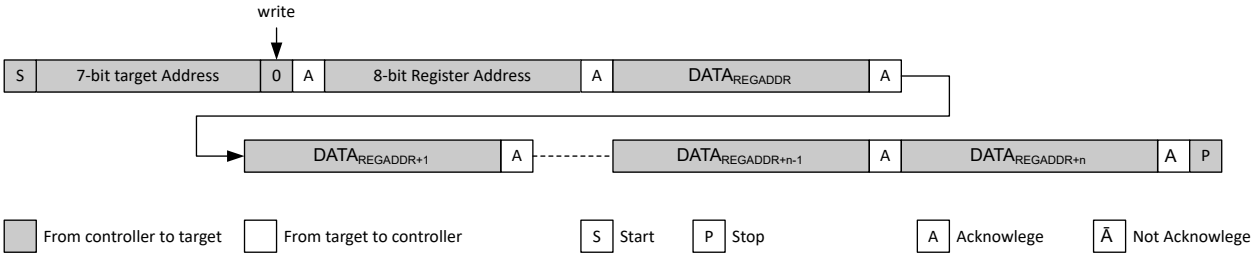


Figure 8-7. Sequential WRITE Starting at a Defined Register Address

9 LM25192-Q1 Registers

Table 9-1 lists the memory-mapped registers for the LM25192-Q1 registers. All register offset addresses not listed in Table 9-1 should be considered as reserved locations and the register contents should not be modified.

Table 9-1. LM25192-Q1 Registers

Address	Acronym	Register Name	Section
1h	OPERATION	Operation register	Section 9.1
3h	CLEAR_FAULTS	Clear faults register	Section 9.2
21h	VOUT_COMMAND	Set output voltage register	Section 9.3
78h	STATUS_BYTE	Device status register	Section 9.4
79h	STATUS_WORD	Device status word	Section 9.5
D0h	MFG_DEVICE_CFG_D0	Set average output current limit register	Section 9.6
D1h	MFG_DEVICE_CFG_D1	Device configuration register 1	Section 9.7
D2h	MFG_DEVICE_CFG_D2	Device configuration register 2	Section 9.8
D5h	MFG_DEVICE_CFG_D5	Device configuration register 3	Section 9.9
D8h	MFG_DEVICE_CFG_D8	Device configuration register 4	Section 9.10
D9h	MFG_DEVICE_CFG_D9	Device configuration register 5	Section 9.11

Complex bit access types are encoded to fit into small table cells. Table 9-2 shows the codes that are used for access types in this section.

Table 9-2. LM25192-Q1 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

9.1 OPERATION Register (Address = 1h) [Reset = 00h]

OPERATION is shown in Table 9-3.

Return to the Summary Table.

Operation register is used to enable or disable the device.

Table 9-3. OPERATION Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CONTROLLER_EN	R/W	0h	Controller enable bit. 0h = Disabled 1h = Enabled
6-0	RESERVED	R	0h	Reserved. This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations the value of 0 is returned.

9.2 CLEAR_FAULTS Register (Address = 3h) [Reset = 00h]

CLEAR_FAULTS is shown in Table 9-4.

Return to the Summary Table.

Clear faults register is used to clear the fault bits in the status register 0x78h.

Table 9-4. CLEAR_FAULTS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CLEAR_FAULTS	R	0h	Clear faults bit. A READ operation clears STATUS_BYTE and STATUS_WORD registers. Note, each individual STATUS_BYTE or STATUS_WORD bit can also be cleared by setting it to a 1 with a WRITE operation. Recycling power or toggling EN pin clears STATUS_BYTE and STATUS_WORD registers as well.

9.3 VOUT_COMMAND Register (Address = 21h) [Reset = 00FAh]

VOUT_COMMAND is shown in Table 9-5.

Return to the Summary Table.

Set output voltage register is used to set the target output voltage.

Table 9-5. VOUT_COMMAND Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved. This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations the value of 0 is returned.
11-8	VOUT_MSB	R/W	0h	Output voltage setting upper byte. Lower limit: 3.3V (1V) Upper limit: 24V Step size: 20mV (10mV) SEL_FB_DIV20 =1 (SEL_FB_DIV20 =0) 0000h = 3.3V (1V) 0064h = 3.3V (1V) 00A5h = 3.3V (1.65V) 00FAh = 5V (2.5V) 01C2h = 9V (4.5V) 02EEh = 15V (7.5V) 03E8h = 20V (10V) 04B0h = 24V (12V) 0708h = 24V (18V) 0960h = 24V (24V) FFFFh = 24V (24V)
7-0	VOUT_LSB	R/W	FAh	Output voltage setting lower byte. Lower limit: 3.3V (1V) Upper limit: 24V Step size: 20mV (10mV) SEL_FB_DIV20 =1 (SEL_FB_DIV20 =0) 0000h = 3.3V (1V) 0064h = 3.3V (1V) 00A5h = 3.3V (1.65V) 00FAh = 5V (2.5V) 01C2h = 9V (4.5V) 02EEh = 15V (7.5V) 03E8h = 20V (10V) 04B0h = 24V (12V) 0708h = 24V (18V) 0960h = 24V (24V) FFFFh = 24V (24V)

9.4 STATUS_BYTE Register (Address = 78h) [Reset = 00h]

STATUS_BYTE is shown in Table 9-6.

Return to the Summary Table.

Device status register.

Table 9-6. STATUS_BYTE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUSY	R/W	0h	Device busy status bit. If set, the device is busy and unable to respond. 0h = No fault 1h = Fault
6	OFF	R/W	0h	Device on/off status bit. If set, the device is disabled / off. 0h = No fault 1h = Fault
5	VOUT_OV	R/W	0h	Device output overvoltage status bit. If set, the voltage on the device output has exceeded the set OVP threshold. 0h = No fault 1h = Fault
4	IOUT_OC	R/W	0h	Device output overcurrent status bit. Is set, the cycle-by-cycle current limit has been triggered. 0h = No fault 1h = Fault
3	RESERVED	R	0h	Reserved. This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations the value of 0 is returned.
2	TEMPERATURE	R/W	0h	Device overtemperature status bit. If set, the device temperature has triggered the thermal shut down (TSD) threshold. 0h = No fault 1h = Fault
1	CML	R/W	0h	Device communication, memory, or logic fault status bit. If triggered, the device memory (parity) error has occurred. 0h = No fault 1h = Fault
0	NONE_OF_THE_ABOVE	R/W	0h	Device other fault or warning status bit. If set, a fault or warning listed in the 0x79[15:8] byte has occurred. 0h = No fault 1h = Fault

9.5 STATUS_WORD Register (Address = 79h) [Reset = 0000h]

STATUS_WORD is shown in Table 9-7.

Return to the Summary Table.

Device status word.

Table 9-7. STATUS_WORD Register Field Descriptions

Bit	Field	Type	Reset	Description
15	VOUT	R/W	0h	Device output voltage status bit. If set, the voltage on the device output has exceeded the set OVP threshold or PG OV threshold. 0h = No fault 1h = Fault
14	IOUT_POUT	R/W	0h	Output current or output power warning. 0h = No fault 1h = Fault
13	RESERVED	R	0h	Reserved. This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations the value of 0 is returned.
12	CC_STATUS	R/W	0h	Constant current (CC) status bit. If set, the device operates in CC regulation mode. Otherwise, the device operates in constant voltage (CV) regulation mode. 0h = CV regulation 1h = CC regulation
11	nPG_STATUS	R/W	0h	Power not good status bit. If set, the voltage on the output of the device has triggered either PG UV or PG OV threshold. 0h = No fault 1h = Fault
10	RESERVED	R	0h	Reserved. This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations the value of 0 is returned.
9	RESERVED	R	0h	Reserved. This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations the value of 0 is returned.
8	RESERVED	R	0h	Reserved. This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations the value of 0 is returned.
7	BUSY	R/W	0h	Device busy status bit. If set, the device is busy and unable to respond. 0h = No fault 1h = Fault
6	OFF	R/W	0h	Device on/off status bit. If set, the device is disabled / off. 0h = No fault 1h = Fault
5	VOUT_OV	R/W	0h	Device output overvoltage status bit. If set, the voltage on the device output has exceeded the set OVP threshold. 0h = No fault 1h = Fault
4	IOUT_OC	R/W	0h	Device output overcurrent status bit. Is set, the cycle-by-cycle current limit has been triggered. 0h = No fault 1h = Fault
3	RESERVED	R	0h	Reserved. This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations the value of 0 is returned.
2	TEMPERATURE	R/W	0h	Device overtemperature status bit. If set, the device temperature has triggered the thermal shut down (TSD) threshold. 0h = No fault 1h = Fault

Table 9-7. STATUS_WORD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CML	R/W	0h	Device communication, memory, or logic fault status bit. If triggered, the device memory (parity) error has occurred. 0h = No fault 1h = Fault
0	NONE_OF_THE_ABOVE	R/W	0h	Device other fault or warning status bit. If set, a fault or warning listed in the 0x79[15:8] byte has occurred. 0h = No fault 1h = Fault

9.6 MFG_DEVICE_CFG_D0 Register (Address = D0h) [Reset = 0Ah]

MFG_DEVICE_CFG_D0 is shown in Table 9-8.

Return to the Summary Table.

Set average output current limit register.

Table 9-8. MFG_DEVICE_CFG_D0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	AVG_ILIM_THRESHOLD	R/W	Ah	Set average output current limit threshold. Assumes 8mΩ (2mΩ) sense resistor is selected. Lower limit: 0.5A (2A) Upper limit: 7.5A (30A) Step size: 50mA (200mA) 0h = 0.5A (2A) Ah = 0.5A (2A) 3Ch = 3A (12A) 64h = 5A (20A) 96h = 7.5A (30A) FFh = 7.5A (30A)

9.7 MFG_DEVICE_CFG_D1 Register (Address = D1h) [Reset = 8Ah]

MFG_DEVICE_CFG_D1 is shown in Table 9-9.

Return to the Summary Table.

Device configuration register 1 is used to select FB divider, configure DRSS function, set the switching frequency, and select compensation for the constant current loop.

Table 9-9. MFG_DEVICE_CFG_D1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SEL_FB_DIV20	R/W	1h	Select FB divider. The selection determines the output voltage range and step size. 0h = DIV10 (10mV step size, 1V-24V range) 1h = DIV20 (20mV step size, 3.3V-24V range)
6	DRSS_EN	R/W	0h	Enable DRSS function. 0h = DRSS disabled 1h = DRSS enabled
5	DRSS_FMOD	R/W	0h	Select DRSS triangular modulation frequency. 0h = 10kHz 1h = 2.5kHz
4-3	FREQ	R/W	1h	Select switching frequency. 0h = 200kHz 1h = 400kHz 2h = 600kHz 3h = 2.2MHz
2-1	CC_COMP	R/W	1h	Select CC compensation time constant. 0h = 0.1ms 1h = 0.2ms 2h = 0.3ms 3h = 0.4ms
0	RESERVED	R	0h	Reserved. This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations the value of 0 is returned.

9.8 MFG_DEVICE_CFG_D2 Register (Address = D2h) [Reset = C9h]

MFG_DEVICE_CFG_D2 is shown in Table 9-10.

Return to the Summary Table.

Device configuration register 2 is used to configure output active discharge, output voltage slew rate, and select soft-start time.

Table 9-10. MFG_DEVICE_CFG_D2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ACTIVE_DISCHARGE_CFG1	R/W	1h	Enable active discharge during VOUT high to low transition. 0h = Disabled 1h = Enabled
6	ACTIVE_DISCHARGE_CFG2	R/W	1h	Enable active discharge during PFM to FPWM transition. 0h = Disabled 1h = Enabled
5	ACTIVE_DISCHARGE_CFG3	R/W	0h	Enable continuous active discharge. 0h = Disabled 1h = Enabled
4-3	VOUT_SLEW_RATE	R/W	1h	Select output voltage slew rate. SEL_FB_DIV20 =1 (SEL_FB_DIV20 =0) 0h = 40mV/us (20mV/us) 1h = 20mV/us (10mV/us) 2h = 1mV/us (0.5mV/us) 3h = 0.5mV/us (0.25mV/us)
2-1	ACTIVE_DISCHARGE_STRENGTH	R/W	0h	Select active discharge strength. 0h = Disabled 1h = 24mA 2h = 48mA 3h = 72mA
0	SOFT_START_TIME	R/W	1h	Select soft-start ramp time. SEL_FB_DIV20 =1 (SEL_FB_DIV20 =0) 0h = 5V/ms (2.5V/ms) 1h = 2.5V/ms (1.25 V/ms)

9.9 MFG_DEVICE_CFG_D5 Register (Address = D5h) [Reset = 65h]

MFG_DEVICE_CFG_D5 is shown in Table 9-11.

Return to the Summary Table.

Device configuration register 3 is used to enable and configure overvoltage protection (OVP) function and set OVP thresholds.

Table 9-11. MFG_DEVICE_CFG_D5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved. This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations the value of 0 is returned.
6	OVP_EN	R/W	1h	Enable OVP detection. 0h = Disabled 1h = Enabled
5	OVP_CFG	R/W	1h	Configure OVP detection. 0h = OVP detection only results in the Status register update 1h = OVP detection interrupts switching, discharges VOUT, sets the VOUT_OV bit in the Status register
4-0	OVP_THRESHOLD	R/W	5h	Select OVP rising threshold. Lower limit: 105% Upper limit: 136% Step size: 1% 0h = 105% 5h = 110% Ah = 115% 1Fh = 136%

9.10 MFG_DEVICE_CFG_D8 Register (Address = D8h) [Reset = CAh]

MFG_DEVICE_CFG_D8 is shown in Table 9-12.

Return to the Summary Table.

Device configuration register 4 is used to set the NINT mask, enable a connection from the VCC and VDD regulator inputs to the VOUTF pin, enable and configure gain of the cable drop compensation function.

Table 9-12. MFG_DEVICE_CFG_D8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	NINT_MASK	R/W	1h	Mask NINT for all STATUS register bits except the CC_STATUS bit. 0h = NINT for most STATUS BYTE/WORD faults. 1h = NINT for only MFG_SPECIFIC bit (CC regulation) in the STATUS register
6	BIAS_EN	R/W	1h	Enable connection from the VCC regulator bias inputs to the VOUTF pin. 0h = Disabled 1h = Enabled
5	CDC_EN	R/W	0h	Enable cable drop compensation. 0h = Disabled 1h = Enabled
4-0	CDC_GAIN	R/W	Ah	Configure CDC gain. Lower limit: 0V/V Upper limit: 62V/V Step size: 2V/V 0h = 0V/V 1h = 2V/V Ah = 20V/V 1Fh = 62V/V

9.11 MFG_DEVICE_CFG_D9 Register (Address = D9h) [Reset = 00h]

MFG_DEVICE_CFG_D9 is shown in Table 9-13.

Return to the Summary Table.

Device configuration register 5 is used to enable MFI function, enable HICCUP mode, override mode selection of the PFM pin, select MODE, and power good (PG) detection window.

Table 9-13. MFG_DEVICE_CFG_D9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MFI_EN	R/W	0h	Enable MFI CC regulation (1.6xILIM for the 1ms of CC regulation). 0h = Disabled 1h = Enabled
6	HICCUP_EN	R/W	0h	Enable HICCUP operation. 0h = Disabled 1h = Enabled
5	OVERRIDE_PFM	R/W	0h	Override PFM pin setting. 0h = PFM pin sets the mode of operation 1h = MODE bit sets the mode of operation
4	MODE	R/W	0h	Select mode of operation. 0h = FPWM 1h = PFM
3	PG_10PCT	R/W	0h	Select PG window. 0h = 5% 1h = 10%
2	OUT_OF_AUDIO	R/W	0h	Enable OUT_OF_AUDIO operation while in PFM mode. 0h = Disabled 1h = Enabled
1	SPARE1	R/W	0h	Spare bit#1 0h = Disabled 1h = Enabled
0	SPARE0	R/W	0h	Spare bit#0 0h = Disabled 1h = Enabled

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Powertrain Components

A comprehensive understanding of the buck regulator power train components is critical to successfully completing a synchronous buck regulator design. The following sections discuss the output inductor, input and output capacitors, power MOSFETs, and EMI input filter.

10.1.1.1 Buck Inductor

For most applications, select a buck inductance such that the inductor ripple current, ΔI_L, is between 30% to 50% of the maximum DC output current at typical input voltage. Select the inductance using Equation 8.

$$L_O = \frac{V_{OUT}}{\Delta I_L \times f_{SW}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

Check the inductor data sheet to make sure that the saturation current of the inductor is above the peak inductor current of a particular design. Ferrite cores have very low core loss and are preferred at high switching frequencies, so design goals can then concentrate on copper loss and preventing saturation. Low inductor core loss is evidenced by reduced no-load input current and higher light-load efficiency. However, ferrite core materials exhibit a hard saturation characteristic and the inductance collapses abruptly when the saturation current is exceeded. This action results in an abrupt increase in inductor ripple current and higher output voltage ripple, not to mention reduced efficiency and compromised reliability. Note that the saturation current of an inductor generally decreases as the core temperature increases.

10.1.1.2 Output Capacitors

The output capacitors combined with the control loop response make sure the output voltage stays within the dynamic transient tolerance specifications. The usual boundaries restricting the output capacitor are driven by finite available PCB area, component size, and cost. The equivalent series resistance (ESR) and equivalent series inductance (ESL) of the output capacitor dominates shaping the load transient response as the load step amplitude and slew rate increase.

The output capacitor, C_{OUT}, filters the inductor ripple current and provides a reservoir of charge for load transient events. Typically, ceramic capacitors provide low ESR to reduce the output voltage ripple and noise spikes, while tantalum or electrolytic capacitors provide a large bulk capacitance in a relatively compact footprint for transient loading events.

Figure 10-1 conceptually illustrates the relevant current waveforms during both load step-down and step-up transitions. As shown, the large-signal slew rate of the inductor current is limited as the inductor current ramps to match the new load-current level following a load transient. This slew-rate limiting exacerbates the deficit of charge in the output capacitor, which must be replenished as fast as possible during and after the load step-up transient. Similarly, during and after a load step-down transient, the slew rate limiting of the inductor current adds to the surplus of charge in the output capacitor that must be depleted as quickly as possible.

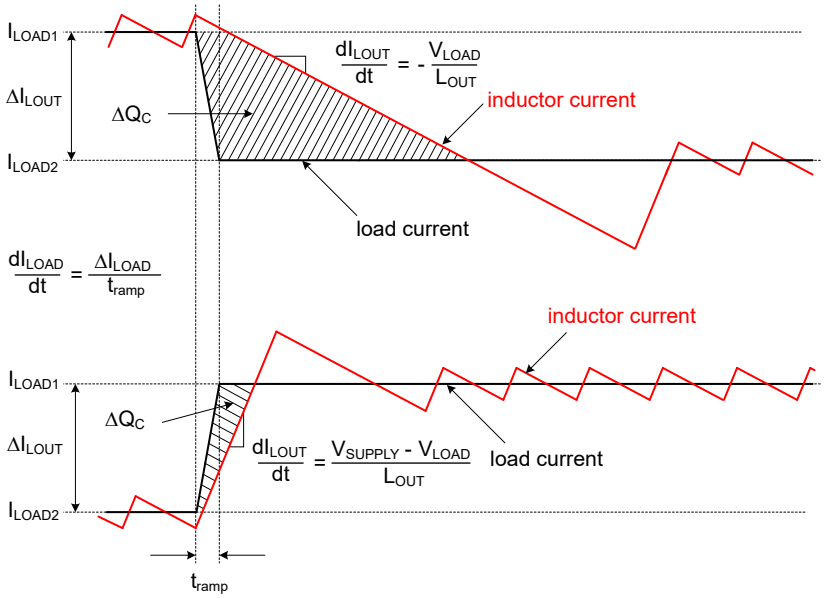


Figure 10-1. Load Transient Response Representation Showing C_{OUT} Charge Surplus or Deficit

For example, in a typical regulator application of 12V input to 3.3V output voltage, the load-off transient represents the worst case in terms of output voltage transient deviation. In that conversion ratio application, the steady-state duty cycle is approximately 28% and the large-signal inductor current slew rate when the duty cycle collapses to zero is approximately $-V_{LOAD} / L_{OUT}$. Compared to a load-on transient, the inductor current takes much longer to transition to the required level. The surplus of charge in the output capacitor causes the output voltage to overshoot. In fact, to deplete this excess charge from the output capacitor as quickly as possible, the inductor current must ramp below the nominal level following the load step. In this scenario, a large output capacitance can be advantageously employed to absorb the excess charge and minimize the voltage overshoot.

To meet the dynamic specification of output voltage overshoot during such a load-off transient (denoted as $\Delta V_{OVERSHOOT}$ with step reduction in output current given by ΔI_{LOAD}), the output capacitance must be larger than:

$$C_{OUT} \geq \frac{L_{OUT} \times \Delta I_{LOAD}^2}{(V_{LOAD} + \Delta V_{OVERSHOOT})^2 - V_{LOAD}^2} \quad (9)$$

Based on the static specification of peak-to-peak output voltage ripple denoted by ΔV_{LOAD}, select an output capacitance that is larger than that given by Equation 10.

$$C_{OUT} \geq \frac{\Delta I_{LOUT}}{8 \times f_{SW} \times \sqrt{\Delta V_{LOAD}^2 - (R_{ESR} \times \Delta I_{LOUT})^2}} \quad (10)$$

The ESR of a capacitor is provided in the manufacturer datasheet, either explicitly as a specification or implicitly in the impedance versus frequency curve. Depending on type, size, and construction, electrolytic capacitors have significant ESR, 5mΩ and above, and relatively large ESL, 5nH to 20nH. PCB traces contribute some parasitic resistance and inductance as well. Ceramic output capacitors have low-ESR and ESL contributions at the switching frequency, and the capacitive impedance component dominates. However, depending on package and voltage rating of the ceramic capacitor, the effective capacitance can drop quite significantly with applied DC voltage and operating temperature.

Ignoring the ESR term in Equation 10 gives a quick estimation of the minimum ceramic capacitance necessary to meet the output ripple specification. Use Equation 9 to determine if additional capacitance is necessary to meet the load-off transient overshoot specification.

A composite implementation of ceramic and electrolytic capacitors highlights the rationale for paralleling capacitors of dissimilar chemistries yet complementary performance. The frequency response of each capacitor is accretive in that each capacitor provides desirable performance over a certain portion of the frequency range. While the ceramic provides excellent mid- and high-frequency decoupling characteristics with the low ESR and ESL to minimize the switching frequency output ripple, the electrolytic device with the large bulk capacitance provides low-frequency energy storage to cope with load transient demands.

10.1.1.3 Input Capacitors

Input capacitors are necessary to limit the input ripple voltage to the buck power stage due to switching-frequency AC currents. TI recommends using X7S or X7R dielectric ceramic capacitors to provide low impedance and high RMS current rating over a wide temperature range. To minimize the parasitic inductance in the switching loop, position the input capacitors as close as possible to the drain of the high-side MOSFET and the source of the low-side MOSFET. Equation 11 gives the input capacitor RMS current for a single-channel buck regulator.

$$I_{CIN,rms} = \sqrt{D \times \left({I_{LOAD}}^2 \times (1 - D) + \frac{{\Delta I_{LOUT}}^2}{12} \right)} \tag{11}$$

The highest input capacitor RMS current occurs at D = 0.5, at which point, the RMS current rating of the input capacitors must be greater than half the output current.

Ideally, the DC component of input current is provided by the input voltage source and the AC component by the input filter capacitors. Neglecting inductor ripple current, the input capacitors source current of amplitude (I_{LOAD} − I_{SUPPLY}) during the D interval and sinks I_{SUPPLY} during the 1−D interval. Therefore, the input capacitors conduct a square-wave current of peak-to-peak amplitude equal to the output current. The resultant capacitive component of AC ripple voltage is a triangular waveform. Together with the ESR-related ripple component, Equation 12 gives the peak-to-peak ripple voltage amplitude.

$$\Delta V_{SUPPLY} = \frac{I_{LOAD} \times D \times (1 - D)}{f_{SW} \times C_{IN}} + I_{LOAD} \times R_{ESR} \tag{12}$$

Equation 13 gives the input capacitance required for a particular load current, based on an input voltage ripple specification of ΔV_{SUPPLY}.

$$C_{IN} \geq \frac{D \times (1 - D) \times I_{LOAD}}{f_{SW} \times (\Delta V_{SUPPLY} - I_{LOAD} \times R_{ESR})} \tag{13}$$

Low-ESR ceramic capacitors can be placed in parallel with higher valued bulk capacitance to provide optimized input filtering for the regulator and damping to mitigate the effects of input parasitic inductance resonating with high-Q ceramics. Select the input bulk capacitor based on the ripple current rating and operating temperature range.

10.1.1.4 Power MOSFETs

The choice of power MOSFETs has significant impact on DC/DC regulator performance. A MOSFET with low on-state resistance, $R_{DS(on)}$, reduces conduction loss, whereas low parasitic capacitances enable faster transition times and reduced switching loss. Normally, the lower the $R_{DS(on)}$ of a MOSFET, the higher the gate charge and output charge (Q_G and Q_{OSS}, respectively), and vice versa. As a result, the product of $R_{DS(on)}$ and Q_G is commonly specified as a MOSFET figure-of-merit. Low thermal resistance of a given package makes sure that the MOSFET power dissipation does not result in excessive MOSFET die temperature.

The main parameters affecting power MOSFET selection are as follows:

- $R_{DS(on)}$ at VCC
- Drain-source voltage rating, BV_{DSS}
- Gate charge parameters at VCC
- Output charge, Q_{OSS}, at the relevant input voltage

- Body diode reverse recovery charge, Q_{RR}
- Gate threshold voltage, $V_{GS(th)}$, derived from the Miller plateau evident in the Q_G versus V_{GS} plot in the MOSFET datasheet. To enhance MOSFET adequately, the miller plateau voltage must be 2V to 3V lower than the gate drive amplitude, especially at the minimum input voltage.

The MOSFET-related power losses for one channel are summarized by the equations presented in Table 10-1, where suffixes one and two represent high-side and low-side MOSFET parameters, respectively. While the influence of inductor ripple current is considered, second-order loss modes, such as those related to parasitic inductances and SW node ringing, are not included.

Table 10-1. MOSFET Power Losses

POWER LOSS MODE	HIGH-SIDE MOSFET	LOW-SIDE MOSFET
MOSFET conduction (2) (3)	$P_{cond1} = D \times \left({I_{LOAD}}^2 + \frac{{\Delta I_{LOUT}}^2}{12} \right) \times R_{DS(on)1}$ (14)	$P_{cond2} = D' \times \left({I_{LOAD}}^2 + \frac{{\Delta I_{LOUT}}^2}{12} \right) \times R_{DS(on)2}$ (15)
MOSFET switching	$P_{sw1} = \frac{V_{SUPPLY} \times f_{SW}}{2} \times \left[\left(I_{LOAD} - \frac{\Delta I_{LOUT}}{2} \right) \times t_R + \left(I_{LOAD} + \frac{\Delta I_{LOUT}}{2} \right) \times t_F \right]$ (16)	Negligible
MOSFET gate drive(1)	$P_{gate1} = V_{CC} \times f_{SW} \times Q_{G1}$ (17)	$P_{gate2} = V_{CC} \times f_{SW} \times Q_{G2}$ (18)
MOSFET output charge(4)	$P_{Coss} = f_{SW} \times (V_{SUPPLY} \times Q_{OSS2} + E_{oss1} - E_{oss2})$ (19)	
Body diode conduction	N/A	$P_{condBD} = V_F \times f_{SW} \times \left[\left(I_{LOAD} + \frac{\Delta I_{LOUT}}{2} \right) \times t_{dt1} + \left(I_{LOAD} - \frac{\Delta I_{LOUT}}{2} \right) \times t_{dt2} \right]$ (20)
Body diode reverse recovery(5)	$P_{RR} = V_{SUPPLY} \times f_{SW} \times Q_{RR2}$ (21)	

(1) Gate drive loss is apportioned based on the internal gate resistance of the MOSFET, externally added series gate resistance and the relevant driver resistance of the device.
(2) MOSFET $R_{DS(on)}$ has a positive temperature coefficient of approximately 4500ppm/°C. The MOSFET junction temperature, T_J, and the rise over ambient temperature is dependent upon the device total power dissipation and the thermal impedance. When operating at or near minimum input voltage, make sure that the MOSFET $R_{DS(on)}$ is rated for the available gate drive voltage.
(3) D' = 1–D is the duty cycle complement.
(4) MOSFET output capacitances, C_{oss1} and C_{oss2}, are highly non-linear with voltage. These capacitances are charged losslessly by the inductor current at high-side MOSFET turn-off. During turn-on, however, a current flows from the input to charge the output capacitance of the low-side MOSFET. E_{oss1}, the energy of C_{oss1}, is dissipated at turn-on, but this dissipation is offset by the stored energy E_{oss2} on C_{oss2}.
(5) MOSFET body diode reverse recovery charge, Q_{RR}, depends on many parameters, particularly forward current, current transition speed, and temperature.

The high-side (control) MOSFET carries the inductor current during the PWM on-time (or D interval) and typically incurs most of the switching losses. Choosing a high-side MOSFET that balances conduction and switching loss contributions is imperative. The total power dissipation in the high-side MOSFET is the sum of the losses due to conduction, switching (voltage-current overlap), output charge, and typically two-thirds of the net loss attributed to body diode reverse recovery.

The low-side (synchronous) MOSFET carries the inductor current when the high-side MOSFET is off (or 1–D interval). The low-side MOSFET switching loss is negligible as the low-side MOSFET switching loss is switched at zero voltage – current just communicates from the channel to the body diode or vice versa during the

transition dead-times. The device, with the adaptive gate drive timing, minimizes body diode conduction losses when both MOSFETs are off. Such losses scale directly with switching frequency.

In high step-down ratio applications, the low-side MOSFET carries the current for a large portion of the switching period. Therefore, to attain high efficiency, optimizing the low-side MOSFET for low $R_{DS(on)}$ is critical. In cases where the conduction loss is too high or the target $R_{DS(on)}$ is lower than available in a single MOSFET, connect two low-side MOSFETs in parallel. The total power dissipation of the low-side MOSFET is the sum of the losses due to channel conduction, body diode conduction, and typically one-third of the net loss attributed to body diode reverse recovery.

10.1.1.5 EMI Filter

Switching regulators exhibit negative input impedance, which is lowest at the minimum input voltage. An underdamped LC filter exhibits a high output impedance at the resonant frequency of the filter. For stability, the filter output impedance must be less than the absolute value of the converter input impedance.

$$Z_{IN} = \left| -\frac{V_{SUPPLY(MIN)}^{2}}{P_{SUPPLY}} \right| \tag{22}$$

The passive EMI filter design steps are as follows:

- Calculate the required attenuation of the EMI filter at the switching frequency, where C_{IN} represents the existing capacitance at the input of the switching converter.
- Input filter inductor L_F is typically selected between 1µH and 10µH, but can be lower to reduce losses in a high-current design.
- Calculate input filter capacitor C_F.

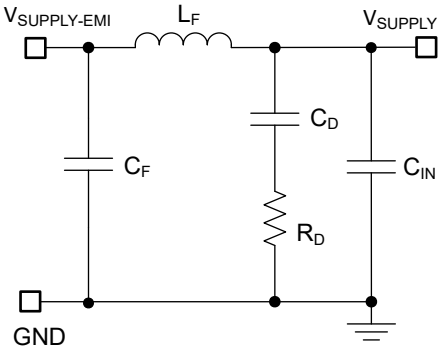


Figure 10-2. Passive π-Stage EMI Filter for Buck Regulator

By calculating the first harmonic current from the Fourier series of the input current waveform and multiplying by the input impedance (the impedance is defined by the existing input capacitor C_{IN}), a formula is derived to obtain the required attenuation as shown by Equation 23.

$$Attn = 20\log\left(\frac{I_{LOUT(PEAK)}}{\pi^2 \times f_{SW} \times C_{IN}} \times \sin(\pi \times D_{MAX}) \times \frac{1}{1\mu V}\right) - V_{MAX} \tag{23}$$

where

- V_{MAX} is the allowed dBµV noise level for the applicable conducted EMI specification.
- C_{IN} is the existing input capacitance of the buck regulator.
- D_{MAX} is the maximum duty cycle.
- $I_{LOUT(PEAK)}$ is the peak inductor current.

For filter design purposes, the current at the input can be modeled as a square-wave. Use Equation 24 to determine the passive EMI filter capacitance C_F.

$$C_F = \frac{1}{L_F}\left(\frac{10^{\frac{|Attn|}{40}}}{2\pi \times f_{SW}}\right)^2 \quad (24)$$

Adding an input filter to a switching regulator modifies the control-to-output transfer function. The output impedance of the filter must be sufficiently small so that the input filter does not significantly affect the loop gain of the buck converter. The impedance peaks at the filter resonant frequency. Equation 25 gives the resonant frequency of the passive filter.

$$f_{res} = \frac{1}{2\pi \times \sqrt{L_F \times C_F}} \quad (25)$$

The purpose of R_D is to reduce the peak output impedance of the filter at the resonant frequency. Capacitor C_D blocks the DC component of the input voltage to avoid excessive power dissipation in R_D. Capacitor C_D must have lower impedance than R_D at the resonant frequency with a capacitance value greater than that of the input capacitor C_{IN}. This requirement prevents C_{IN} from interfering with the cutoff frequency of the main filter. Added input damping is needed when the output impedance of the filter is high at the resonant frequency (Q of filter formed by L_F and C_{IN} is too high). An electrolytic capacitor C_D can be used for input damping with a value that Equation 26 gives.

$$C_D \geq 4 \times C_{IN} \quad (26)$$

Use Equation 27 to select the input damping resistor R_D.

$$R_D = \sqrt{\frac{L_F}{C_{IN}}} \quad (27)$$

10.1.2 Error Amplifier and Compensation

Figure 10-3 shows a type-II compensator using a transconductance error amplifier (EA). The dominant pole of the EA open-loop gain is set by the EA output resistance, $R_{O(EA)}$, and effective bandwidth-limiting capacitance, C_{BW}, as shown by Equation 28.

$$G_{EA}(s) = -\frac{g_{m(EA)} \times R_{O(EA)}}{1 + s \times R_{O(EA)} \times C_{BW}} \quad (28)$$

The EA high-frequency pole is neglected in the above expression. Equation 29 calculates the compensator transfer function from output voltage to COMP node, including the gain contribution from the (internal or external) feedback resistor network.

$$G_{COMP}(s) = \frac{V_{COMP}(s)}{V_{LOAD}(s)} = -\frac{V_{REF}}{V_{LOAD}} \times \frac{g_m \times R_{O(EA)} \times \left(1 + \frac{s}{\omega_{Z1}}\right)}{\left(1 + \frac{s}{\omega_{P1}}\right) \times \left(1 + \frac{s}{\omega_{P2}}\right)} \quad (29)$$

where

- V_{REF} is the feedback voltage reference.
- $g_{m(EA)}$ is the EA gain transconductance of 1mS.
- $R_{O(EA)}$ is the error amplifier output impedance of 70MΩ.

$$\omega_{Z1} = \frac{1}{R_{COMP} \times C_{COMP}} \quad (30)$$

$$\omega_{P1} = \frac{1}{R_{O(EA)} \times (C_{COMP} + C_{HF} + C_{BW})} \cong \frac{1}{R_{O(EA)} \times C_{COMP}} \quad (31)$$

$$\omega_{P2} = \frac{1}{R_{COMP} \times (C_{COMP} || (C_{HF} + C_{BW}))} \cong \frac{1}{R_{COMP} \times C_{HF}} \quad (32)$$

The EA compensation components create a pole close to the origin, a zero, and a high-frequency pole. Typically, R_{COMP} << $R_{O(EA)}$ and C_{COMP} >> C_{BW} and C_{HF}, so the approximations are valid.

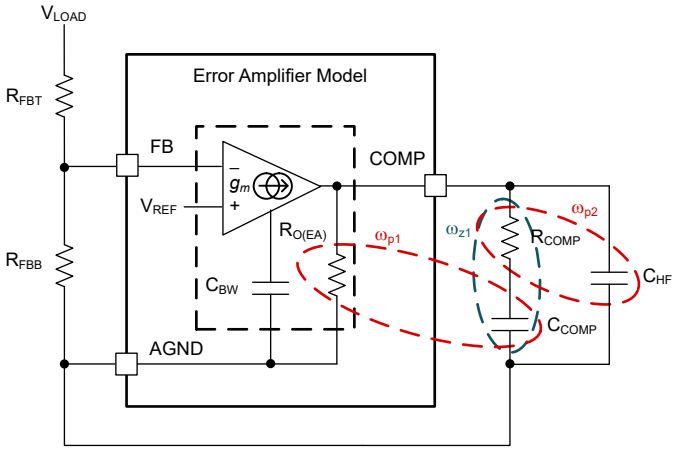


Figure 10-3. Error Amplifier and Compensation Network

10.2 Typical Application

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation and test results, refer to *TI Designs* reference design library.

10.2.1 High Efficiency, Wide Input, 400kHz, Synchronous Buck Regulator

Figure 10-4 shows the schematic diagram of a single-output, synchronous, buck regulator with I²C interface, which provides maximum output voltages of 6V and a rated load current of 20A. In this example, the target full-load efficiencies at 16V input is 94.9%. The regulator is designed for 400kHz switching frequency.

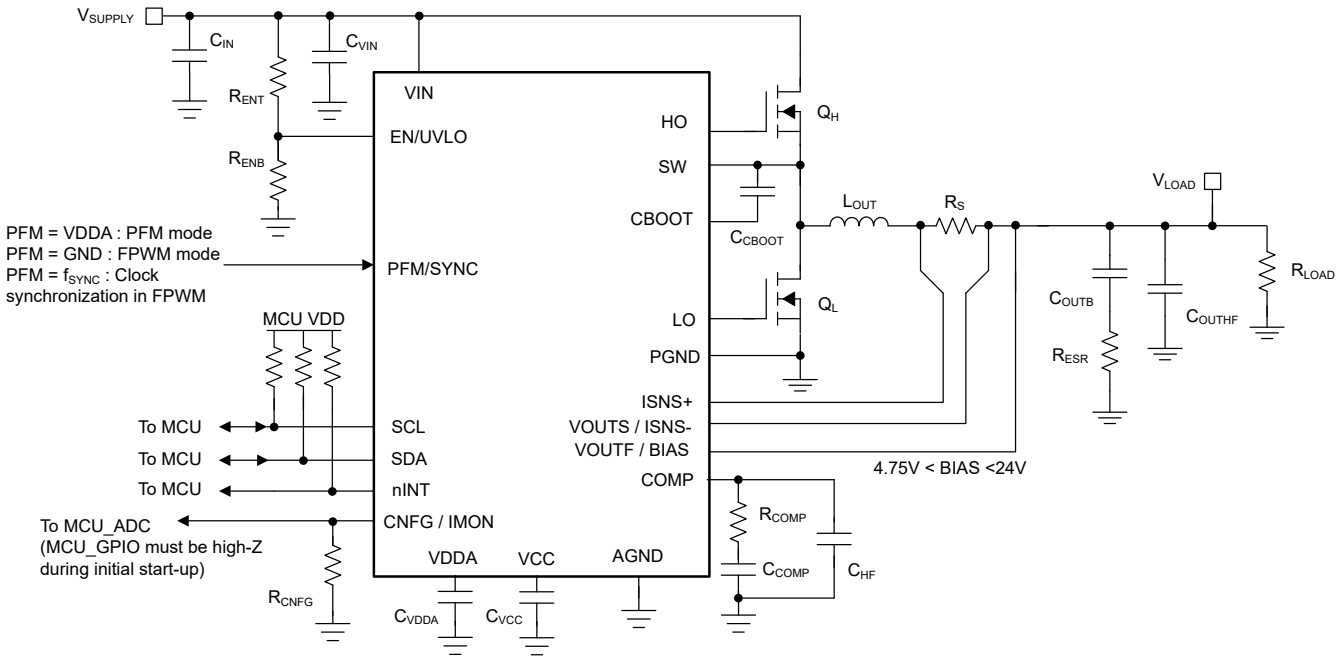


Figure 10-4. Application Circuit With I²C Interface

Note

Depending on the source impedance of the input supply bus, an electrolytic capacitor can be required at the input to make sure of stability, particularly at low input voltage and high output current operating conditions.

10.2.1.1 Design Requirements

Table 10-2 shows the intended input, output, and performance parameters for this design example.

Table 10-2. Design Parameters

DESIGN PARAMETER	VALUE
Input operating range	9V, 16V, 36V (minimum, typical, maximum)
CV regulation target	6V
CC regulation target	20A
Switching frequency	400kHz

The switching frequency is set at 400kHz by I^2C. In terms of control loop performance, the target loop crossover frequency is 40kHz with a phase margin greater than 60°.

10.2.1.2 Detailed Design Procedure

Use the Quick Start Calculator to expedite the process of designing a regulator for a given application based on the device specifications. Download the *LM5192-LM25192-DESIGN-CALC* Quick Start Calculator for a detailed design procedure.

10.2.1.2.1 Buck Inductor

1. Use Equation 33 to calculate the required buck inductance based on a 40% inductor ripple current at nominal input voltages.

$$L_O = \frac{V_{OUT}}{\Delta I_L \times f_{SW}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) = \frac{6}{8 \times 400k} \times \left(1 - \frac{6}{16}\right) = 1.17\mu H \quad (33)$$

2. Select a standard inductor value of 2.2µH to account for effective inductance derating with current of molded inductors. Use Equation 34 to calculate the peak inductor currents at maximum steady-state input voltage.

$$I_{LO(PK)} = I_{LOAD} + \frac{\Delta I_L}{2} = I_{LOAD} + \frac{V_{OUT}}{2 \times L_O \times f_{SW}} \times \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) = 20 + \frac{5.682}{2} = 22.84A \quad (34)$$

3. Subharmonic oscillation occurs with a duty cycle greater than 50% for peak current-mode control if no slope compensation. For design simplification, the device has an internal slope compensation ramp proportional to the switching frequency that is added to the current sense signal to damp any tendency toward subharmonic oscillation. Use Equation 35 to cross-check the inductance to set a slope compensation close to the ideal one times the inductor current downslope.

$$L_{O(MIN)} = \frac{V_{OUT} \times R_S}{0.04 \times f_{SW}} = \frac{6 \times 2m}{0.04 \times 400k} = 0.75\mu H \quad (35)$$

10.2.1.2.2 Current-Sense Resistance

1. Calculate the current-sense resistance based on a maximum peak current capability of at least 20% higher than the peak inductor current at full load to provide sufficient margin during start-up and load-on transients. Use Equation 36 to calculate the current sense resistances.

$$R_S = \frac{V_{CS-TH}}{1.2 \times I_{LO(PK)}} = \frac{60m}{1.2 \times 22.84} = 2.19m\Omega \quad (36)$$

2. Select a standard resistance value of 2mΩ for the shunt. Carefully adhere to the layout guidelines in Section 10.4.1 to make sure that noise and DC errors do not corrupt the differential current-sense voltages measured at the ISNS+ and VOUTS pins.
3. Place the shunt resistor close to the inductor.

4. Use Kelvin-sense connections, and route the sense lines differentially from the shunt to the device.
5. The CS-to-output propagation delay (related to the current limit comparator, internal logic, and power MOSFET gate drivers) causes the peak current to increase above the calculated current limit threshold. For a total propagation delay t_{DELAY} of 105ns, use Equation 37 to calculate the worst-case peak inductor current with the output shorted.

$$I_{LO-PK(SC)} = \frac{V_{CS-TH(MAX)}}{R_S} + \frac{V_{IN(MAX)} \times t_{DELAY}}{L_O} = \frac{66m}{2m} + \frac{36 \times 105n}{2.2\mu} = 34.7A \quad (37)$$

6. Based on this result, select an inductor with saturation current greater than 34A across the full operating temperature range.

10.2.1.2.3 Output Capacitors

1. Use Equation 38 to estimate the output capacitance required to manage the output voltage overshoot during a load-off transient (from full load to no load) assuming 10% overshoot is allowed.

$$C_{OUT} \geq \frac{L_O \times \Delta I_{LOAD}^2}{(V_{LOAD} + \Delta V_{OVERSHOOT})^2 - V_{LOAD}^2} = \frac{2.2\mu \times 20^2}{(6 + 6 \times 0.1)^2 - 6^2} = 116\mu F \quad (38)$$

2. Noting the voltage coefficient of ceramic capacitors where the effective capacitance decreases significantly with applied voltage, select four 10µF, 25V, X7R ceramic output capacitors, and one 100µF, 35V, hybrid aluminum polymer capacitor. Generally, when sufficient capacitance is used to satisfy the load-off transient response requirement, the voltage undershoot during a no-load to full-load transient is also satisfactory.
3. Use Equation 39 to estimate the peak-peak output voltage ripple at nominal input voltage.

$$\Delta V_{OUT} = \sqrt{\left(\frac{\Delta I_L}{8 \times f_{SW} \times C_{OUT}}\right)^2 + (R_{ESR} \times \Delta I_L)^2} = \sqrt{\left(\frac{4.26}{8 \times 400k \times 128u}\right)^2 + (3.2m \times 4.26)^2} = 17mV \quad (39)$$

where

- R_{ESR} is the effective equivalent series resistance (ESR) of the output capacitors.
- 128µF is the total effective (derated) ceramic output capacitance at 6V.

4. Use Equation 40 to calculate the output capacitor RMS ripple current and verify that the ripple current is within the capacitor ripple current rating.

$$I_{CO(RMS)} = \frac{\Delta I_{LOUT}}{\sqrt{12}} = \frac{4.26}{\sqrt{12}} = 1.23A \quad (40)$$

10.2.1.2.4 Input Capacitors

A power supply input typically has a relatively high source impedance at the switching frequency. Good-quality input capacitors are necessary to limit the input ripple voltage. In general, the ripple current splits between the input capacitors based on the relative impedance of the capacitors at the switching frequency.

1. Select the input capacitors with sufficient voltage and RMS ripple current ratings.
2. Use Equation 41 to calculate the input capacitor RMS ripple current assuming a worst-case duty-cycle operating point of 50%.

$$I_{CIN,rms} = \sqrt{D \times \left(I_{LOAD}^2 \times (1 - D) + \frac{\Delta I_{LOUT}^2}{12}\right)} = \sqrt{0.5 \times \left(20^2 \times (1 - 0.5) + \frac{4.26^2}{12}\right)} = 10A \quad (41)$$

3. Use Equation 42 to find the required input capacitance.

$$C_{IN} \geq \frac{D \times (1 - D) \times I_{LOAD}}{f_{SW} \times (\Delta V_{SUPPLY} - I_{LOAD} \times R_{ESR})} = \frac{0.5 \times (1 - 0.5) \times 20}{400k \times (0.25 - 20 \times 1m)} = 54\mu F \quad (42)$$

where

- ΔV_{SUPPLY} is the input peak-to-peak ripple voltage specification.
- R_{ESR} is the input capacitor ESR.

4. Recognizing the voltage coefficient of ceramic capacitors, select six 4.7µF, 100V, X7R ceramic input capacitors. Place these capacitors adjacent to the power MOSFETs.
5. Use six 10nF, 100V, X7R, 0603 ceramic capacitors near the high-side MOSFET to supply the high di/dt current during MOSFET switching transitions. Such capacitors offer high self-resonant frequency (SRF) and low effective impedance above 100MHz. The result is lower power loop parasitic inductance, thus minimizing switch-node voltage overshoot and ringing for lower conducted and radiated EMI signature.

10.2.1.2.5 Compensation Components

Select compensation components for a stable control loop using the procedure outlined as follows.

1. Based on a specified loop gain crossover frequency, f_C, of 40kHz, use Equation 43 to calculate R_{COMP}, assuming an effective output capacitance of 128µF. Choose a standard value for R_{COMP} of 13kΩ. V_{REF} is $V_{OUT}/10$ if V_{STEP} is 10mV. V_{REF} is $V_{OUT}/20$ if V_{STEP} is 20mV.

$$R_{COMP} = 2 \times \pi \times f_C \times \frac{V_{OUT}}{V_{REF}} \times \frac{R_S \times G_{CS}}{gm} \times C_{OUT} = 2 \times \pi \times 40kHz \times \frac{6V}{0.3V} \times \frac{2m\Omega \times 10}{1000\mu S} \times 128\mu F = 12.9k\Omega \quad (43)$$

2. To provide adequate phase boost at crossover while also allowing a fast settling time during a load or line transient, select C_{COMP} to place a zero at the higher (1) one tenth of the crossover frequency, or (2) the load pole. Choose a standard value for C_{COMP} of 5.6nF .

$$C_{COMP} = \frac{10}{2 \times \pi \times f_C \times R_{COMP}} = \frac{10}{2 \times \pi \times 40kHz \times 13k\Omega} = 3.1nF \quad (44)$$

3. Calculate C_{HF} to create a pole at the ESR zero and to attenuate high-frequency noise on the COMP pin. C_{BW} is the bandwidth-limiting capacitance of the error amplifier. 1pF C_{HF} can be ignored in this design. However, in noisy environments, especially at high V_{IN} and high load currents, additional capacitance can help filter out the noise.

$$C_{HF} = \frac{1}{2 \times \pi \times f_{ESR} \times R_{COMP}} - C_{BW} = \frac{1}{2 \times \pi \times 311kHz \times 13k\Omega} - 15pF = 24pF \quad (45)$$

Note

Set a fast loop with high R_{COMP} and low C_{COMP} values to improve the response when recovering from operation in dropout.

10.2.1.3 Application Curves

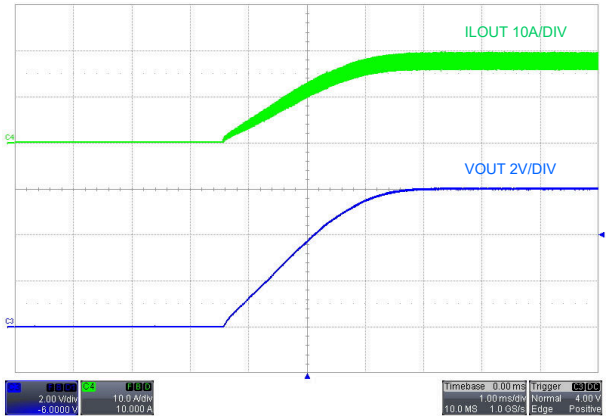


Figure 10-5. Start-Up, EN ON, V_{SUPPLY} = 12V, I_{LOAD} = 18A Resistive Load

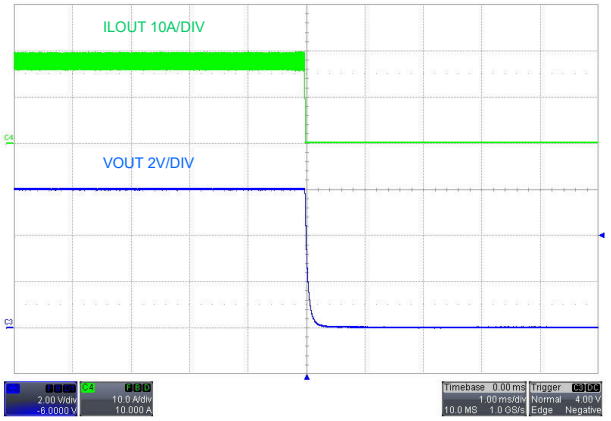


Figure 10-6. Shutdown, EN OFF, V_{SUPPLY} = 12V, I_{LOAD} = 18A Resistive Load

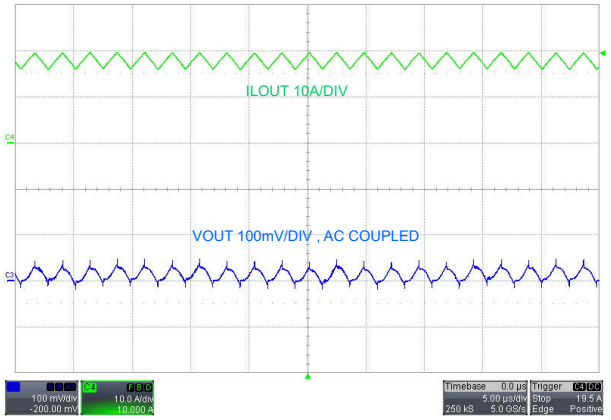


Figure 10-7. Output Ripple, , V_{SUPPLY} = 12V, I_{LOAD} = 18A

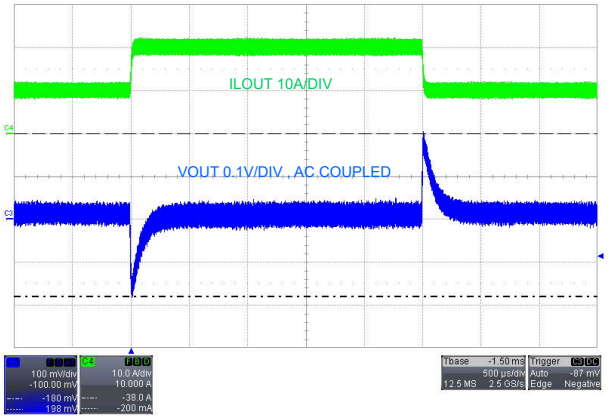


Figure 10-8. Load Transient Response, V_{SUPPLY} = 12V, FPWM, 10A to 20A

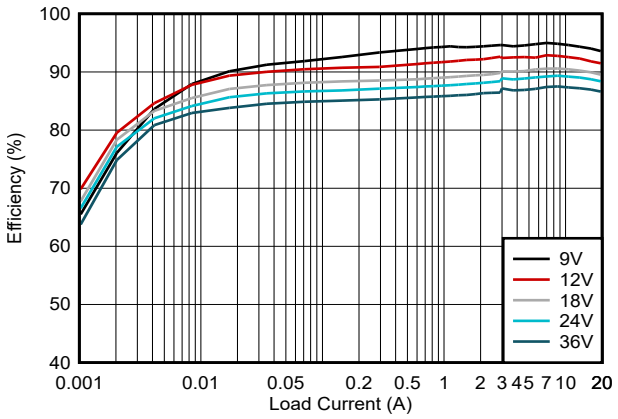


Figure 10-9. PFM Mode Efficiency, Log Scale

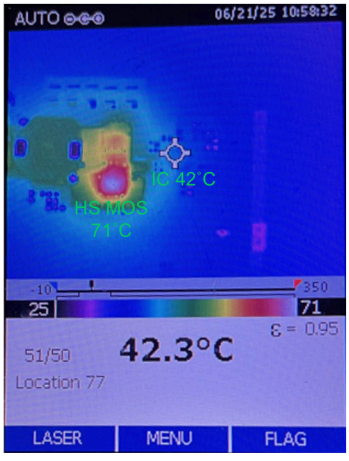


Figure 10-10. V_{SUPPLY} = 16V, I_{LOAD} = 20A, T_A = 25°C, No Airflow

10.3 Power Supply Recommendations

The device is designed to operate from a wide input supply voltage range . The input supply must be capable of delivering the required input supply current to the fully loaded regulator over the wide input voltage range. Estimate the average input supply current using Equation 46.

$$I_{SUPPLY} = \frac{V_{LOAD} \times I_{LOAD}}{V_{SUPPLY} \times \text{Efficiency}} \quad (46)$$

If the regulator is connected to an input supply through long wires or PCB traces with a large impedance, take special care to achieve stable performance. The parasitic inductance and resistance of the input cables can have an adverse affect on converter operation. The parasitic inductance in combination with the low-ESR ceramic input capacitors form an underdamped resonant circuit. This circuit can cause overvoltage transients at the regulator input each time the input supply is cycled ON and OFF. The parasitic resistance causes the input supply voltage to dip during a load transient. The best way to solve such issues is to reduce the distance from the input supply to the regulator and use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of the electrolytic capacitors helps damp the input resonant circuit and reduce any voltage overshoots.

An EMI input filter is often used in front of the regulator that, unless carefully designed, can lead to instability as well as some of the effects mentioned above. The *AN-2162 Simple Success With Conducted EMI From DCDC Converters* application note provides helpful suggestions when designing an input filter for any switching regulator.

10.4 Layout

10.4.1 Layout Guidelines

Proper PCB design and layout is important in a high-current, fast-switching circuit to achieve a robust and reliable design. The high power switching loop of a buck regulator power stage is denoted by loop 1 in the shaded area of Figure 10-11. The topological architecture of a buck regulator means that particularly high di/dt current flows in the components of loop 1, reducing the parasitic inductance of this loop by minimizing the effective loop area becomes mandatory. Also important are the gate drive loops of the high-side and low-side MOSFETs, denoted by 3 and 4, respectively.

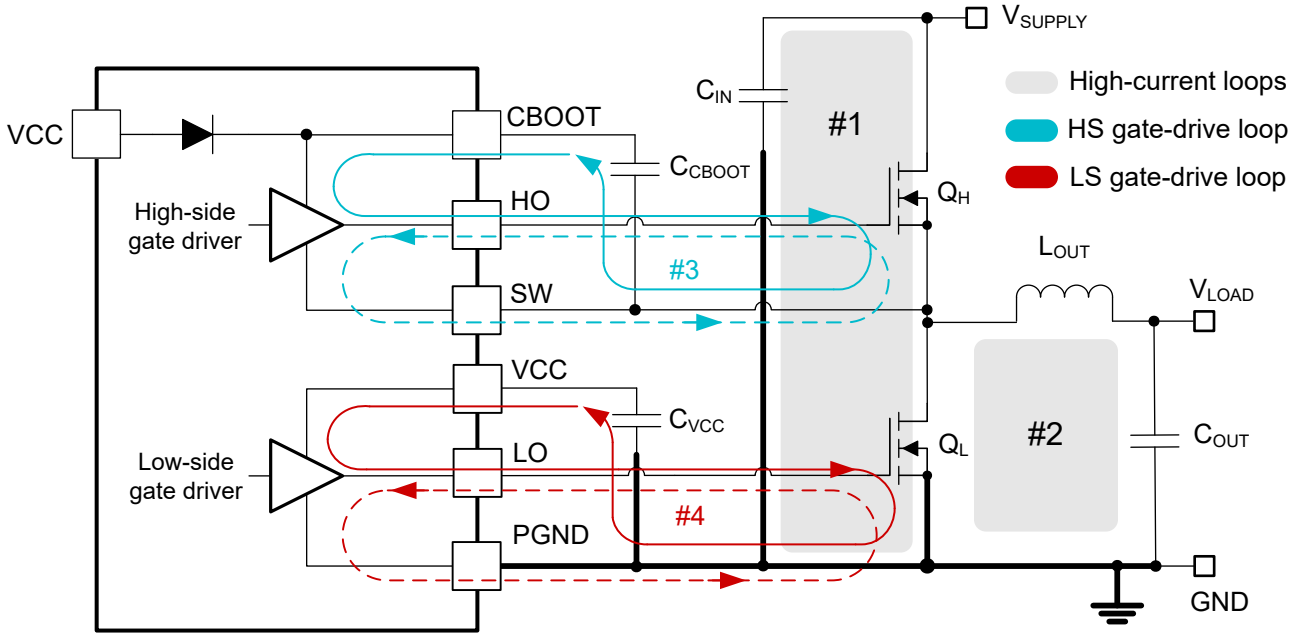


Figure 10-11. DC/DC Regulator Ground System With Power Stage and Gate Drive Circuit Switching Loops

10.4.1.1 Power Stage Layout

- Input capacitors, output capacitors, and MOSFETs are the constituent components of the power stage of a buck regulator and are typically placed on the top side of the PCB. The benefits of convective heat transfer are maximized because of leveraging any system-level airflow. In a two-sided PCB layout, small-signal components are typically placed on the bottom side. Insert at least one inner plane, connected to ground, to shield and isolate the small-signal traces from noisy power traces and lines.
- The DC/DC regulator has several high-current loops. Minimize the area of these loops to suppress generated switching noise and optimize switching performance.
  - Loop 1: the most important loop area to minimize. The path is from the input capacitor or capacitors through the high- and low-side MOSFETs, and back to the capacitor or capacitors through the ground connection. Connect the input capacitor or capacitors negative terminal close to the source of the low-side MOSFET. Similarly, connect the input capacitor or capacitors positive terminal close to the drain of the high-side MOSFET.
  - Loop 2: loop 2 is not as critical as loop 1. The path is from the low-side MOSFET through the inductor and output capacitor or capacitors, and back to source of the low-side MOSFET through ground. Connect the source of the low-side MOSFET and negative terminal of the output capacitor or capacitors at ground as close as possible.
- The PCB trace defined as SW node, which connects to the source of the high-side MOSFET, the drain of the low-side MOSFET and the high-voltage side of the inductor, must be short and wide. However, the SW connection is a source of injected EMI and thus must not be too large.
- Follow any layout considerations of the MOSFETs as recommended by the MOSFET manufacturer, including pad geometry and solder paste stencil design.
- The SW pin connects to the switch node of the power conversion stage and acts as the return path for the high-side gate driver. The parasitic inductance inherent to loop 1 and the output capacitance (C_{OSS}) of both power MOSFETs form a resonant circuit that induces high frequency (> 50MHz) ringing at the SW node. The voltage peak of this ringing, if not controlled, can be significantly higher than the input voltage. Make sure that the peak ringing amplitude does not exceed the absolute maximum rating limit for the SW pin. In many cases, a series resistor and capacitor snubber network connected from the SW node to GND damps the ringing and decreases the peak amplitude. If testing reveals that the ringing amplitude at the SW pin is excessive, then include snubber components as needed.

10.4.1.2 Gate-Drive Layout

Minimizing stray or parasitic gate loop inductance is key to optimizing gate drive switching performance. The following loops are important:

- Loop 3: high-side MOSFET, Q_H. During the high-side MOSFET turn-on, high current flows from the bootstrap capacitor through the gate driver and high-side MOSFET, and back to the negative terminal of the boot capacitor through the SW connection. Conversely, to turn off the high-side MOSFET, high current flows from the gate of the high-side MOSFET through the gate driver and SW, and back to the source of the high-side MOSFET through the SW trace.
- Loop 4: low-side MOSFET, Q_L. During the low-side MOSFET turn-on, high current flows from the VCC decoupling capacitor through the gate driver and low-side MOSFET, and back to the negative terminal of the capacitor through ground. Conversely, to turn off the low-side MOSFET, high current flows from the gate of the low-side MOSFET through the gate driver and GND, and back to the source of the low-side MOSFET through ground.

TI recommends following circuit layout guidelines when designing with high-speed MOSFET gate drive circuits.

- Connections from gate driver outputs, HO and LO, to the respective gates of the high-side or low-side MOSFETs must be as short as possible to reduce series parasitic inductance. Be aware that peak gate drive currents can be as high as a few amperes. Use 0.65mm (25mils) or wider traces. Use via or vias, if necessary, of at least 0.5mm (20 mils) diameter along these traces. Route HO and SW traces as a differential pair from the device to the high-side MOSFET, taking advantage of flux cancellation. Also, route LO trace and PGND trace/copper area as a differential pair from the device to the low-side MOSFET, taking advantage of flux cancellation.

- Locate the bootstrap capacitor, C_{CBOOT}, close to the CBOOT and SW pins of the device to minimize the area of loop 3 associated with the high-side driver. Similarly, locate the VCC capacitor, C_{VCC}, close to the VCC and PGND pins of the device to minimize the area of loop 4 associated with the low-side driver.

10.4.1.3 PWM Controller Layout

Locate the device as close as possible to the power MOSFETs to minimize gate driver trace runs, the components related to the analog and feedback signals as well as current sensing are considered in the following:

- Separate power and signal, analog traces, and use a ground plane to provide noise shielding.
- Place all sensitive analog traces and components related to COMP, ISNS+, VOUTS, and IMON away from high-voltage switching nodes such as SW, HO, LO, or CBOOT to avoid mutual coupling. Use internal layer or layers as ground plane or planes.
- Route the ISNS+ and VOUT sense traces as differential pairs to minimize noise pickup and use Kelvin connections to the applicable shunt resistor. Shield the current sense (ISNS+ and VOUTS) traces from power traces and components.
- Minimize the loop area from the VCC and VIN pins through the respective decoupling capacitors to the PGND pin. Locate these capacitors as close as possible to the device.

10.4.1.4 Thermal Design and Layout

The operating temperature range of a PWM controller with integrated gate drivers and bias supply LDO regulator is greatly affected by the following:

- Average gate drive current requirements of the power MOSFETs
- Switching frequency
- Operating input supply voltage (affecting bias regulator LDO voltage drop and hence the power dissipation)
- Thermal characteristics of the package and operating environment

For a PWM controller to be useful over a particular temperature range, the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits.

The VQFN package offers a means of removing heat from the semiconductor die through the exposed thermal pad at the base of the package. The exposed pad of the package is thermally connected to the substrate of the device. This connection allows a significant improvement in heat sinking and becomes imperative that the PCB is designed with thermal lands, thermal vias, and a ground plane to complete the heat removal subsystem. The exposed pad of the device is soldered to the ground-connected copper land on the PCB directly underneath the device package, reducing the thermal resistance to a low value.

Numerous vias with a 0.3mm diameter connected from the thermal land to the internal and solder-side ground plane or planes are vital to help dissipation. In a multi-layer PCB design, a solid ground plane is typically placed on the PCB layer below the power components. Not only does this placement provide a plane for the power stage currents to flow but this placement also represents a thermally conductive path away from the heat generating devices.

The thermal characteristics of the MOSFETs also are significant. The drain pads of the high-side MOSFETs are normally connected to a VIN plane for heat sinking. The drain pads of the low-side MOSFETs are tied to the SW plane, but the SW plane area is purposely kept as small as possible to mitigate EMI concerns.

10.4.1.5 Ground Plane Design

TI recommends using one or more of the inner PCB layers as a solid ground plane. A ground plane offers shielding for sensitive circuits and traces and also provides a quiet reference potential for the control circuitry. In particular, a full ground plane on the layer directly underneath the power stage components is essential. Connect the source terminal of the low-side MOSFET and return terminals of the input and output capacitors to this ground plane. Connect the PGND and AGND pins of the device at the exposed pad and then connect to the system ground plane using an array of vias under the exposed pad. The PGND nets contain noise at the switching frequency and can bounce because of load current variations. The power traces for PGND, VIN, and

SW can be restricted to one side of the ground plane, for example, on the top layer. The other side of the ground plane contains much less noise and is designed for sensitive analog trace routes.

10.4.2 Layout Example

Figure 10-12 shows a layout example of a synchronous buck regulator with discrete power MOSFETs. The design uses an inner layer as a power-loop return path directly underneath the top layer to create a low-area switching power loop. This loop area, and hence parasitic inductance, must be as small as possible to minimize EMI as well as switch-node voltage overshoot and ringing.

The high-frequency power loop current flows through MOSFETs, through the power ground plane on the inner layer, and back to VIN through the ceramic capacitors .

Multiple ceramic capacitors are placed in parallel close to the drain of the high-side MOSFET. The low equivalent series inductance (ESL) and high self-resonant frequency (SRF) of the small footprint capacitors yield excellent high-frequency performance. The negative terminals of these capacitors are connected to the inner layer ground plane with multiple vias, further minimizing parasitic loop inductance.

Additional guidelines to improve noise immunity and reduce EMI are as follows:

- Connect PGND directly to the low-side MOSFET and power ground. Connect AGND directly to an analog ground plane for sensitive analog components. The analog ground plane for AGND and the power ground plane for PGND must be connected at a single point directly under the device at the exposed pad.
- Connect the MOSFETs directly to the inductor terminal with short copper connections (without vias) as this net has high dv/dt and contributes to radiated EMI. The single-layer routing of the switch-node connection means that switch-node vias with high dv/dt do not appear on the bottom side of the PCB. This event avoids e-field coupling to the reference ground plane during the EMI test. VIN and PGND plane copper pours shield the polygon connecting the MOSFETs to the inductor terminal, further reducing the radiated EMI signature.
- Place the EMI filter components on the bottom side of the PCB so that the components are shielded from the power stage components on the top side.

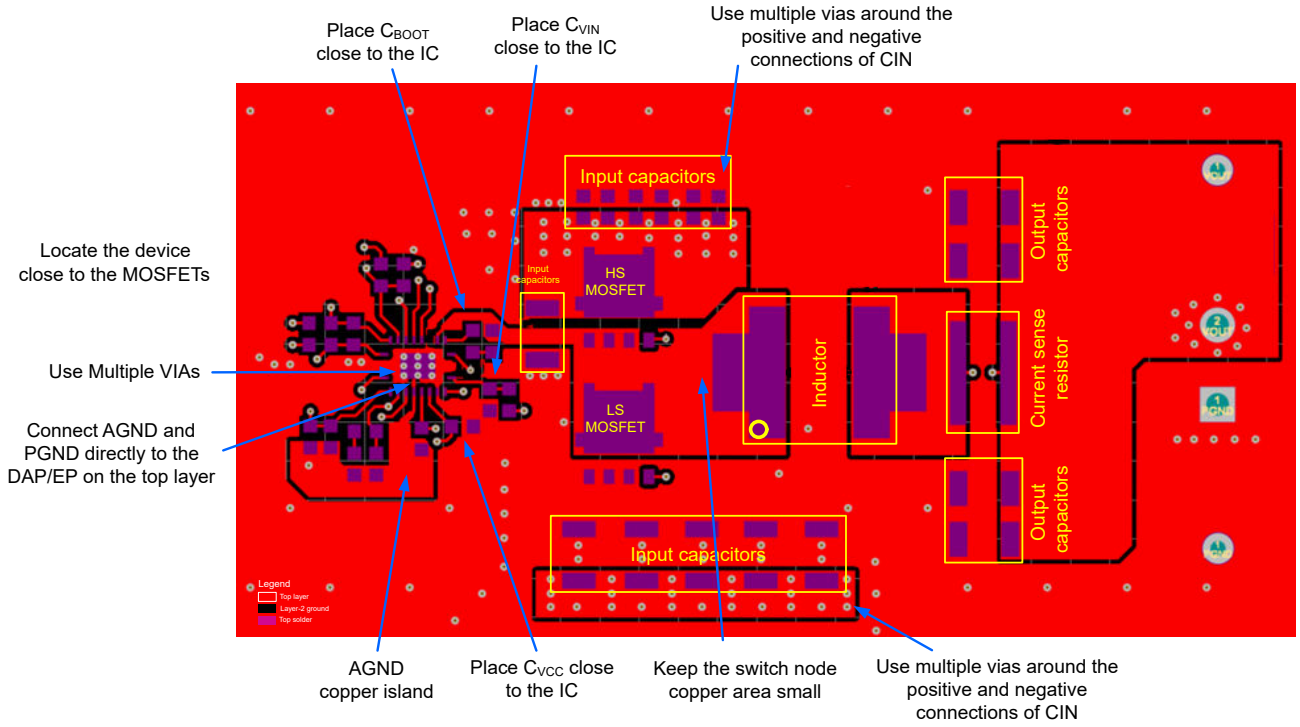


Figure 10-12. PCB Top Layer

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

For development support, see the following:

- For TI's reference design library, visit TI Designs
- TI designs:
  - *ADAS 8-Channel Sensor Fusion Hub Reference Design with Two 4-Gbps Quad Deserializers*
  - *Automotive EMI and Thermally Optimized Synchronous Buck Converter Reference Design*
  - *Automotive High Current, Wide V_{IN} Synchronous Buck Controller Reference Design Featuring LM5141-Q1*
  - *25W Automotive Start-Stop Reference Design Operating at 2.2MHz*
  - *Synchronous Buck Converter for Automotive Cluster Reference Design*
  - *137W Holdup Converter for Storage Server Reference Design*
  - *Automotive Synchronous Buck With 3.3V at 12.0A Reference Design*
  - *Wide Input Synchronous Buck Converter Reference Design With Frequency Spread Spectrum*
  - *Automotive Wide V_{IN} Front-end Reference Design for Digital Cockpit Processing Units*
- Technical articles:
  - *High-Density PCB Layout of DC/DC Converters*
  - *Synchronous Buck Controller Solutions Support Wide V_{IN} Performance and Flexibility*
  - *How to Use Slew Rate for EMI Control*

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Improve High-current DC/DC Regulator Performance for Free with Optimized Power Stage Layout* application brief
- Application notes:
  - Texas Instruments, *AN-2162 Simple Success with Conducted EMI from DC-DC Converters*
  - Texas Instruments, *Maintaining Output Voltage Regulation During Automotive Cold-Crank with LM5140-Q1 Dual Synchronous Buck Controller*
- Texas Instruments, *Reduce Buck Converter EMI and Voltage Stress by Minimizing Inductive Parasitics* analog design journal
- White papers:
  - Texas Instruments, *An Overview of Conducted EMI Specifications for Power Supplies*
  - Texas Instruments, *An Overview of Radiated EMI Specifications for Power Supplies*
  - Texas Instruments, *Valuing Wide V_{IN}, Low EMI Synchronous Buck Circuits for Cost-driven, Demanding Applications*

11.2.1.1 PCB Layout Resources

- Application notes:
  - Texas Instruments, *AN-1149 Layout Guidelines for Switching Power Supplies*
  - Texas Instruments, *AN-1229 SIMPLE SWITCHER® PCB Layout Guidelines*
  - Texas Instruments, *Low Radiated EMI Layout Made SIMPLE with LM4360x and LM4600x*
- Texas Instruments, *Constructing Your Power Supply – Layout Considerations* seminar

11.2.1.2 Thermal Design Resources

- Application notes:
  - Texas Instruments, *AN-2020 Thermal Design by Insight, Not Hindsight*
  - Texas Instruments, *AN-1520 A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages*
  - Texas Instruments, *Semiconductor and IC Package Thermal Metrics*

  - Texas Instruments, *Thermal Design Made Simple with LM43603 and LM43602*
  - Texas Instruments, *PowerPAD™ Thermally Enhanced Package*
  - Texas Instruments, *Using New Thermal Metrics*
- Texas Instruments, *PowerPAD™ Made Easy* application brief

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.5 Trademarks

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11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

12 Revision History

DATE	REVISION	NOTES
June 2026	*	Initial Release

13 Mechanical, Packaging, and Orderable Information

The following pages show mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM25192QRGYRQ1	Active	Production	VQFN (RGY) | 19	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	25192Q A1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

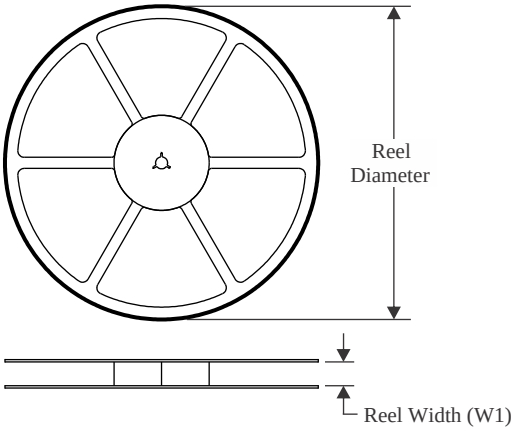
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

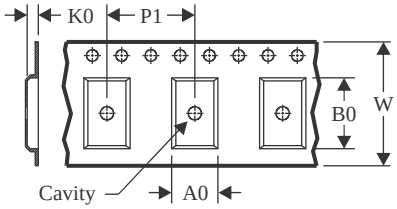
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

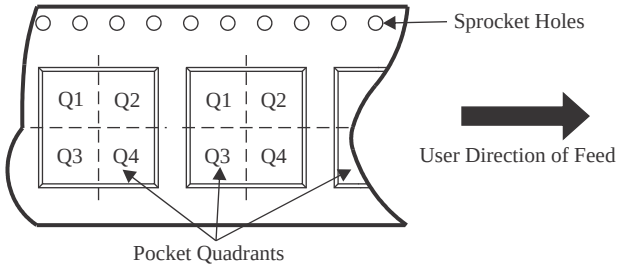


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

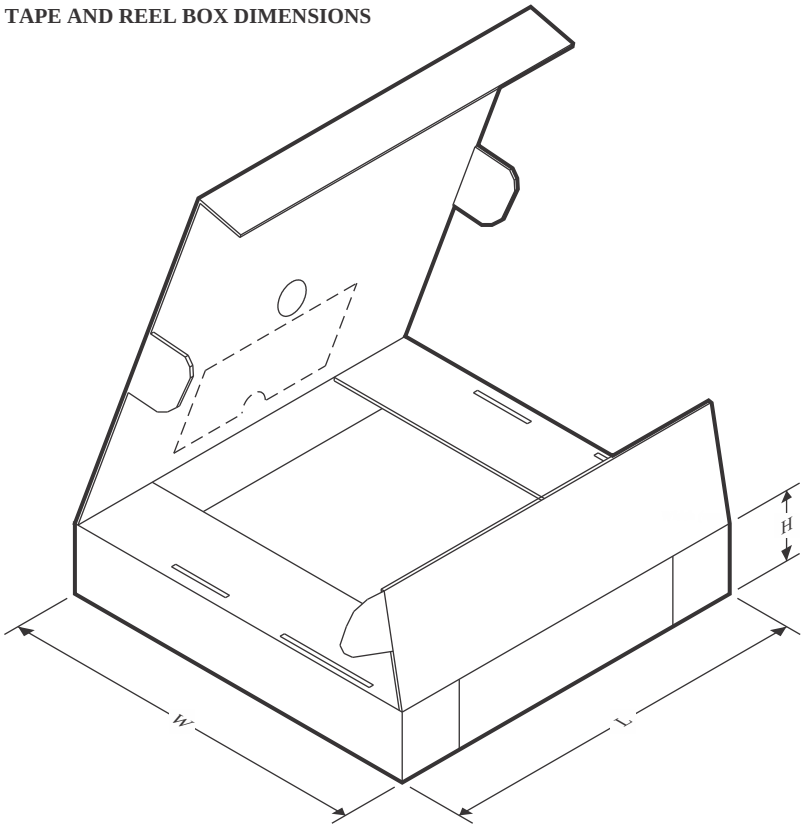
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM25192QRGYRQ1	VQFN	RGY	19	3000	330.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM25192QRGYRQ1	VQFN	RGY	19	3000	360.0	360.0	36.0

GENERIC PACKAGE VIEW

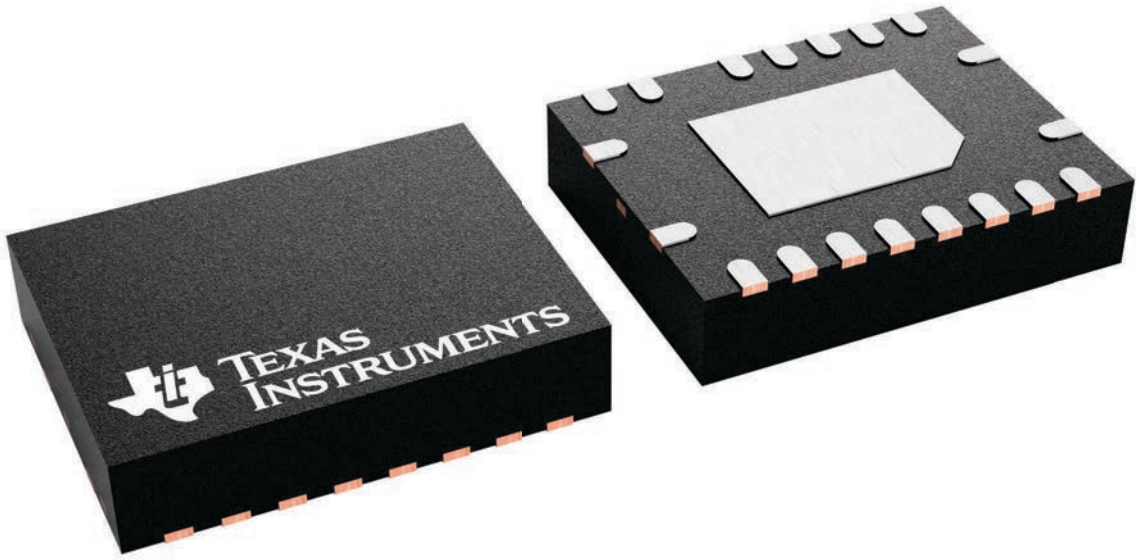
RGY 19

VQFN - 1 mm max height

3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



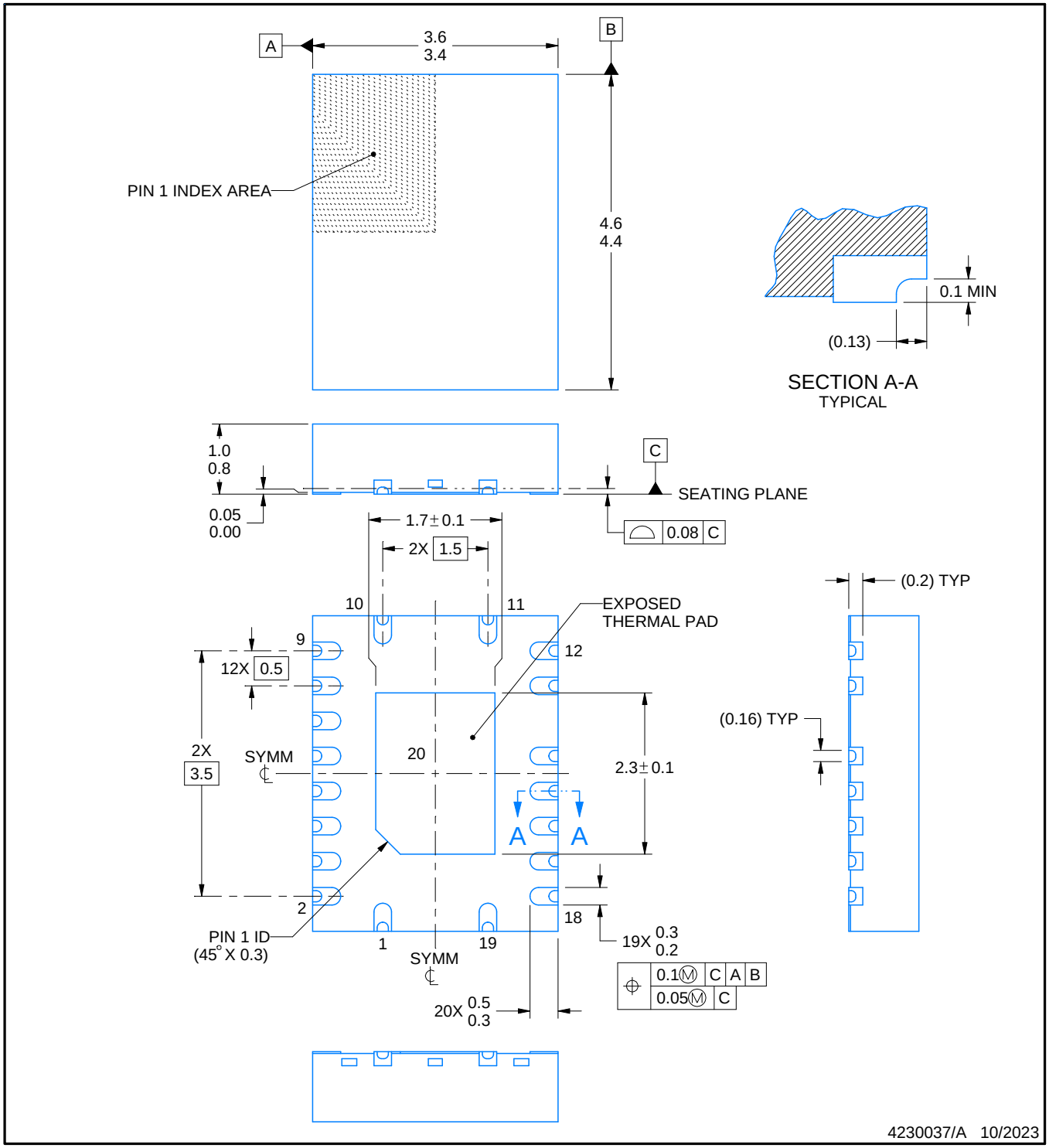
4230073/A

PACKAGE OUTLINE

RGY0019B

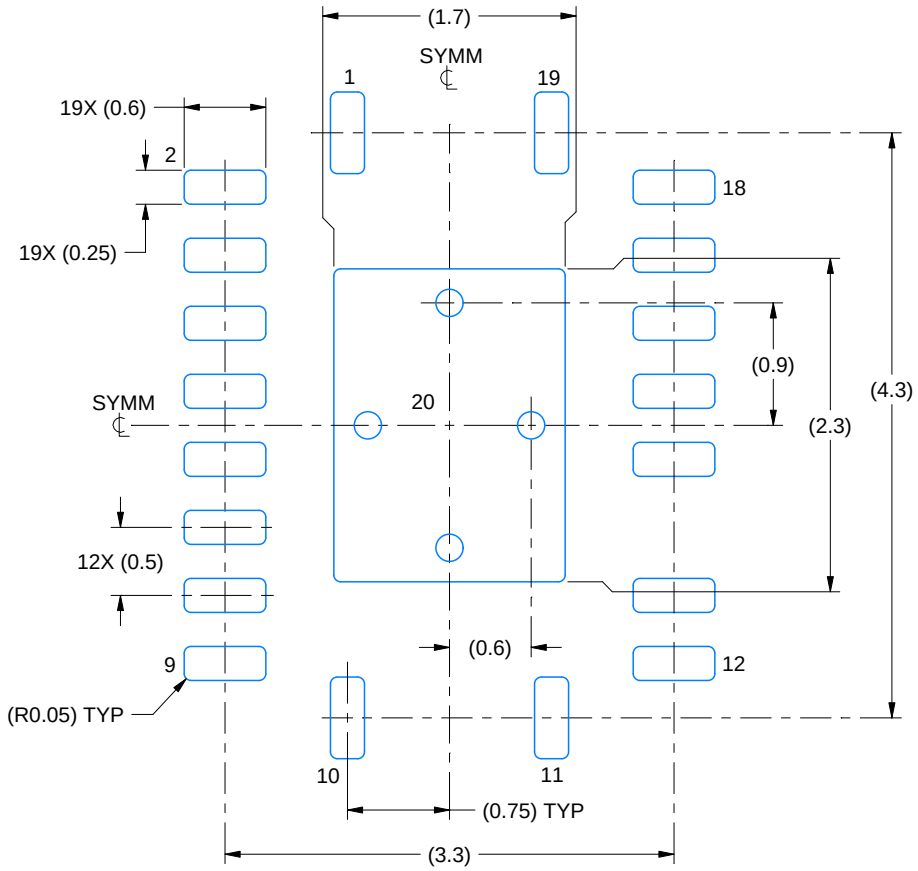
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

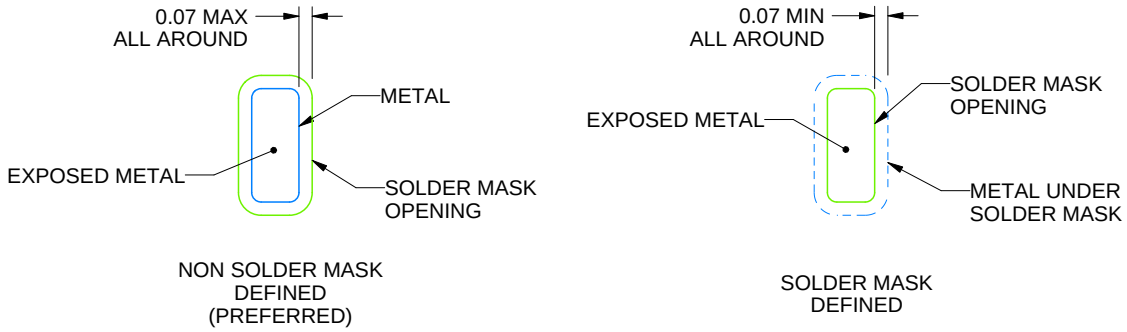


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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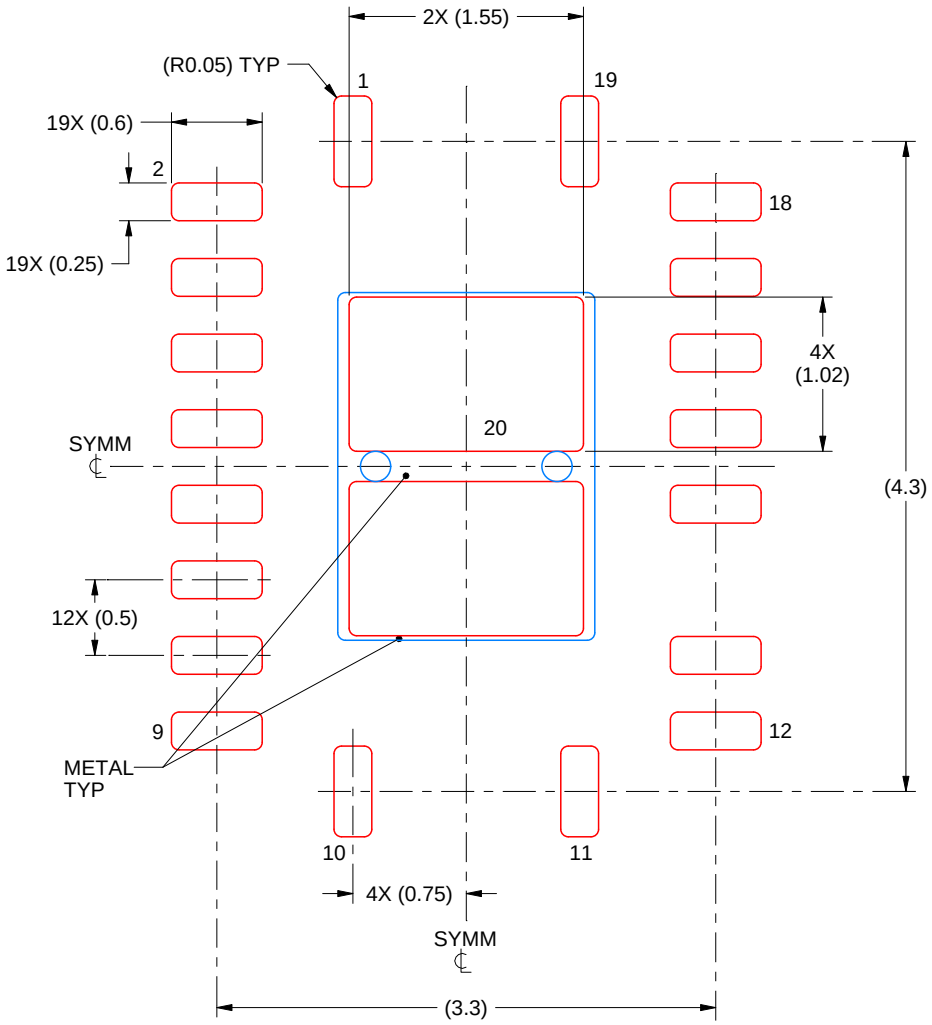
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 21
81% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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