LM25139-Q1 Automotive, 42V, Synchronous Buck DC/DC Controller With Dual Random Spread Spectrum for Advanced EMI Mitigation

1 Features

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade 1: –40°C to 125°C ambient operating temperature
- Versatile synchronous buck DC/DC controller
  - Wide input voltage range of 4V to 42V
  - Fixed 3.3V, 5V or adjustable output voltage from 0.8V to 36V
  - –40°C to 150°C junction temperature range
  - Integrated high-current MOSFET gate drivers with 1.65A source and 2.4A sink capability
  - Lossless inductor DCR or shunt current sensing
  - 25ns $t_{ON(min)}$ for high V_{IN} to V_{OUT} conversion
  - 80ns $t_{OFF(min)}$ for high duty-cycle applications
  - No-load sleep quiescent current of 10µA
  - Shutdown quiescent current of 2.3µA
- Optimized for CISPR 25 Class 5 EMI requirements
  - Dual Random Spread Spectrum (DRSS) with 5% or 10% frequency modulation
  - Switching frequency from 100kHz to 3.2MHz
  - Optional synchronization to an external clock
  - Selectable PFM or FPWM operation
- Inherent protection features for robust design
  - Hiccup-mode overcurrent protection
  - Precision enable input and open-drain PGOOD indicator for sequencing and control
  - VCC and gate-drive UVLO protection
  - Fixed 3ms output voltage soft start
  - Thermal shutdown protection with hysteresis
- 16-pin, 3mm × 3mm package with wettable flanks
- Create a custom design using the LM25139-Q1 with WEBENCH® Power Designer

2 Applications

- Automotive electronic systems
- Infotainment systems and instrument clusters
- Advanced driver assistance systems (ADAS)
- Body electronics and lighting

3 Description

The LM25139-Q1 is a 42V, synchronous, buck DC/DC controller with ultra-low I_Q for single-output, high-current regulator circuits. Deriving from a family of wide-V_{IN} range automotive controllers, the device uses a peak current-mode control architecture for fast transient response, convenient loop compensation, and excellent load and line regulation performance.

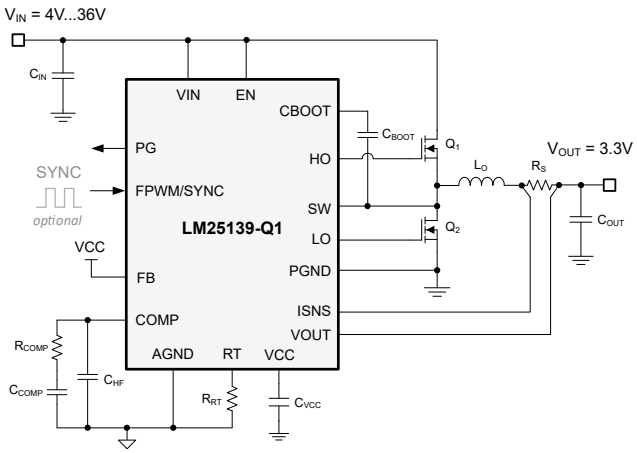
A high-side switch minimum on time of 25ns provides large step-down ratios, enabling the direct conversion from 12V and 24V automotive inputs to low-voltage rails for reduced system design cost and complexity. The LM25139-Q1 continues to operate during input voltage dips as low as 4V, at nearly 100% duty cycle if needed, making the device an excellent choice for high-performance, automotive battery applications.

The LM25139-Q1 comes in a thermally enhanced, 16-pin VQFN package with wettable flank pins and an exposed pad to aid in thermal dissipation.

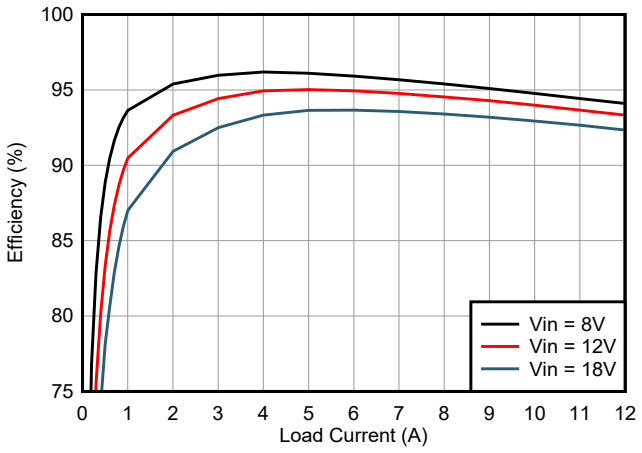
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LM25139-Q1	RGT (VQFN, 16)	3mm × 3mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Schematic



Typical Efficiency, V_{OUT} = 3.3V, F_{SW} = 440kHz

Several features are included to simplify compliance with CISPR 25 automotive EMI requirements. Adaptively timed, high-current MOSFET gate drivers minimize body diode conduction during switching transitions, reducing switching losses while also improving thermal and EMI performance at high input voltage and high switching frequency. Resistor-adjustable switching frequency as high as 3.2MHz can be synchronized to an external clock source to eliminate beat frequencies in noise-sensitive applications.

To further improves the EMI signature, the LM25139-Q1 controller has a unique feature known as dual random spread spectrum (DRSS). Combining low-frequency triangular and high-frequency random modulations mitigates EMI disturbances across lower and higher frequency bands, respectively. This hybrid technique aligns with the multiple resolution bandwidth (RBW) settings specified in industry-standard EMC tests.

Additional features of the LM25139-Q1 include –40°C to 150°C junction temperature operation, user-selectable PFM mode for lower current consumption at light-load conditions, open-drain power-good indicator for fault reporting and output monitoring, precision enable input, monotonic start-up into prebiased load, integrated VCC bias supply regulator and bootstrap diode, internal 3ms soft-start time, hiccup-mode overload protection, and thermal shutdown protection with automatic recovery.

The LM25139-Q1 controller is qualified to AEC-Q100 grade 1 for automotive applications. The wide input voltage range, low quiescent current consumption, high-temperature operation, low minimum on-time, low EMI signature, low component count, and 9mm^2 IC size provide an excellent point-of-load regulator choice for applications requiring enhanced robustness and cost advantages.

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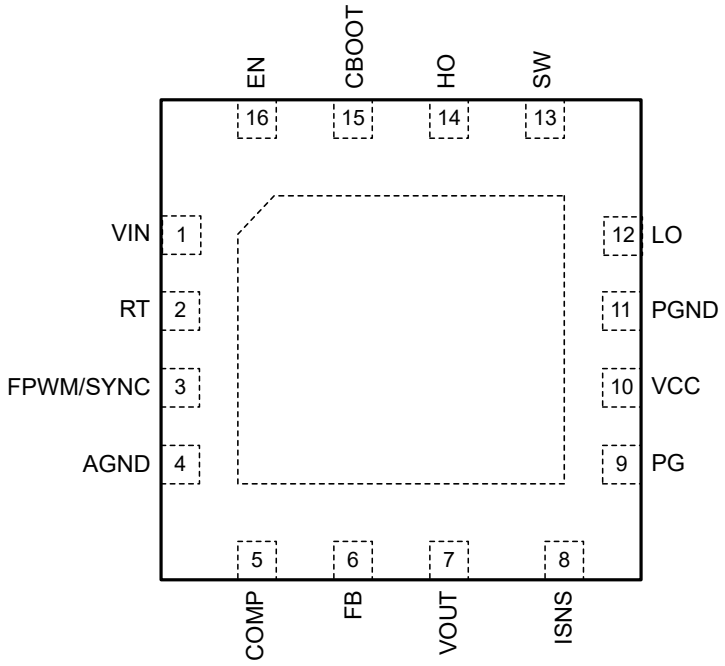
4 Pin Configuration and Functions



Connect the exposed pad to AGND and PGND on the PCB.

Figure 4-1. 16-Pin RGT Package VQFN (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
1	VIN	P	Supply voltage input source for the VCC regulator
2	RT	I	Frequency programming pin. A resistor from RT to AGND sets the oscillator frequency between 100kHz and 3.2MHz with DRSS disabled. A resistor from RT to VCC sets the oscillator frequency between 100kHz and 3.2MHz with DRSS enabled.
3	FPWM/SYNC	I	Connect FPWM/SYNC to GND to enable diode emulation mode. Connect FPWM/SYNC to VCC to operate the LM25139-Q1 in forced PWM (FPWM) mode with conduction at light load. FPWM/SYNC can also be used to synchronize the controller to an external clock. Place the LM25139-Q1 into standby mode by applying an external clock to FPWM/SYNC while EN is low.
4	AGND	P	Analog ground connection. Ground return for the internal voltage referenced analog circuits.
5	COMP	O	Transconductance error amplifier. Connect the compensation network for COMP to AGND.
6	FB	I	Connect FB to VCC to set the output voltage to 3.3V. Connect FB using a 24.9kΩ or 24kΩ to VCC to set the output voltage to 5V. Install a resistor divider from VOUT to AGND to set the output voltage set point between 0.8V and 36V. The regulation voltage at FB is 0.8V.
7	VOUT	I	Output voltage sense and the current sense amplifiers input. Connect V_{OUT} to the output side of the current sense resistor.
8	ISNS	I	Current sense amplifier input. Connect this pin to the inductor side of the external current sense resistor.
9	PG	O	An open collector output that goes low if V_{OUT} is outside the specified regulation window.
10	VCC	P	VCC bias pin. Connect a ceramic capacitor between VCC and PGND
11	PGND	G	Power ground connection pin for the low-side power MOSFET gate driver.
12	LO	O	Low-side power MOSFET gate driver output.
13	SW	P	Switch node of the buck regulator and high-side gate driver return. Connect to the bootstrap capacitor, the source terminal of the high-side MOSFT, and the drain terminal of the low-side MOSFET.
14	HO	O	High-side power MOSFET gate driver output.

Table 4-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
15	CBOOT	P	High-side driver supply for bootstrap gate driver.
16	EN	I	An active-high precision input with rising threshold of 1V and hysteresis current of 11µA. If the EN voltage is less than 0.5V, the LM25139-Q1 is in shutdown mode.

(1) P = Power, G = Ground, I = Input, O = Output

4.1 Wettable Flanks

100% automated visual inspection (AVI) post-assembly is typically required to meet requirements for high reliability and robustness. Standard quad-flat no-lead (QFN) packages do not have solderable or exposed pins and terminals that are easily viewed. Visually determining whether or not the package is successfully soldered onto the printed-circuit board (PCB) is therefore difficult. The wettable-flank process was developed to resolve the issue of side-lead wetting of leadless packaging. The LM25139-Q1 is assembled using a 36-pin VQFN package with wettable flanks to provide a visual indicator of solderability, which reduces inspection time and manufacturing costs.

5 Specifications

5.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted). (1)

		MIN	MAX	UNIT
Output voltage	VOUT to AGND	–0.3	36	V
	CBOOT to SW	–0.3	V_{SW} + 5.5	V
	CBOOT to SW, transient < 20ns	–2		V
	HO to SW	–0.3	V_{CBOOT} + 0.3	V
	HO to SW, transient < 20ns	–5		V
	LO to PGND	–0.3	V_{VCC} + 0.3	V
	LO to PGND, transient < 20ns	–1.5		V
Input voltage	AGND to PGND	–0.3	0.3	V
	VIN to PGND	–0.3	45	V
	SW to PGND	–0.3	45	V
	SW to PGND, transient < 20ns	–5		V
	EN, RT to PGND	–0.3	45	V
	VCC, PG, FB, COMP, FPWM/SYNC to AGND	–0.3	5.5	V
	ISNS to AGND	–0.3	45	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 (1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (1, 6, 7, 12)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

Over the operating junction temperature range of –40°C to 150°C (unless otherwise noted). (1)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage range	3.5		42	V
V_{OUT}	Output voltage range	0.8		36	V
	SW to PGND	–0.3		42	V
	CBOOT, HO to SW	–0.3	5	5.25	V
	FB, COMP to AGND	–0.3		5.25	V
	EN, RT to PGND	–0.3		42	V
	VCC, LO to PGND	–0.3	5	5.25	V
	VOUT, ISNS to PGND	–0.3		36	V
	PGND to AGND	–0.3		0.3	V
	FPWM/SYNC, PG to AGND	–0.3		5.25	V
T_J	Operating junction temperature	–40		150	°C

(1) Recommended operating conditions are conditions under which the device is intended to be functional. For specifications and test conditions, see the Electrical Characteristics.

5.4 Thermal Information

THERMAL METRIC[1]		LM25139-Q1 RGT (VQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	55.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	62.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	29.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	14.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

T_J = –40°C to 150°C. Typical values are at T_J = 25°C and V_{IN} = 12V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY (VIN)						
I_{Q-VIN1}	VIN shutdown current	V_{EN} = 0V		2.3	4	µA
I_{Q-VIN2}	VIN standby current	Non-switching, 0.5V ≤ V_{EN} ≤ 1V		30	48	µA
I_{SLEEP1}	Sleep current, 3.3V	V_{EN} = 5V, V_{VOUT} = 3.3V, in regulation, no load, not switching, $V_{FPWM/SYNC}$ = 0V		10	18	µA
I_{SLEEP2}	Sleep current, 5V	V_{EN} = 5V, V_{VOUT} = 5V, in regulation, no-load, not switching, $V_{FPWM/SYNC}$ = 0V		11	20	µA
PRECISION ENABLE (EN)						
V_{SDN}	Shutdown to standby threshold	V_{EN} rising		0.5		V
$V_{EN-HIGH}$	Enable voltage rising threshold	V_{EN} rising, enable switching	0.95	1.0	1.05	V
I_{EN-HYS}	Enable hysteresis	V_{EN} = 1.1V	–14	–11	–8	µA
INTERNAL LDO (VCC)						
$V_{VCC-REG}$	VCC regulation voltage	I_{VCC} = 0mA to 90mA	4.7	5	5.3	V
$V_{VCC-UVLO}$	VCC UVLO rising threshold		3.68	3.8	3.9	V
$V_{VCC-HYST}$	VCC UVLO hysteresis			300		mV
$I_{VCC-REG}$	Internal LDO short-circuit current limit			210		mA
REFERENCE VOLTAGE (FB)						
V_{REF}	Regulated FB voltage		792	800	808	mV
OUTPUT VOLTAGE (VOUT)						
$V_{OUT-3.3V–INT}$	3.3V output voltage setpoint	R_{FB} = 0Ω, V_{IN} = 4V to 42V	3.26	3.3	3.33	V
$V_{OUT-5V–INT}$	5V output voltage setpoint	R_{FB} = 24.9kΩ, V_{IN} = 5.5V to 42V	4.93	5.0	5.05	V
ERROR AMPLIFIER (COMP)						
g_m	EA transconductance			1.1		mS
I_{FB}	Error amplifier input bias current				100	nA
$V_{COMP-CLAMP=MAX}$	COMP clamp maximum voltage			2.1		V
$I_{COMP-SRC}$	EA source current	V_{COMP} = 1V, V_{FB} = 0.68V		115		µA
$I_{COMP-SINK}$	EA sink current	V_{COMP} = 1V, V_{FB} = 0.92V		115		µA
DUAL RANDOM SPREAD SPECTURM (DRSS)						
f_m	Modulation frequency		7.2		16.6	kHz
Δf_{C1}	Low-frequency spread spectrum modulation range 1	LM25139D5QRGTRQ1		±5		%
Δf_{C2}	Low-frequency spread spectrum modulation range 2	LM25139QRGTRQ1		±10		%
FORCED PWM (FPWM/SYNC)						
$V_{FPWM-HI}$	FPWM high detection threshold				1.2	V

5.5 Electrical Characteristics (continued)

T_J = –40°C to 150°C. Typical values are at T_J = 25°C and V_{IN} = 12V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{FPWM-LO}$	FPWM low detection threshold		0.8			V
V_{ZC-PFM}	Zero-cross threshold (LO off) in PFM			–5.5		mV
$V_{ZC-FPWM}$	Zero-cross threshold (LO off) in FPWM			30		mV
$t_{PFM-FILTER}$	SYNCIN to PFM mode		13		72	µs
SWITCHING FREQUENCY (RT)						
V_{RT}	RT pin regulation voltage	10kΩ < R_{RT} < 100kΩ		1		V
$F_{SW2-VCC}$	Switching frequency 2, RT to VCC	RT = 10.1kΩ to VCC		2.2		MHz
F_{SW1}	Switching frequency 1	R_{RT} = 53kΩ to AGND	396	440	484	kHz
F_{SW2}	Switching frequency 2	R_{RT} = 10.1kΩ to AGND		2.2		MHz
F_{SW3}	Switching frequency 3	R_{RT} = 237kΩ to AGND		100		kHz
$SLOPE_1$	Internal slope compensation 1	R_{RT} = 10.1kΩ		1000		mV/µs
$t_{ON(min)}$	Minimum on-time	$V_{HO} – V_{SW} = V_{CBOOT} – V_{SW}$		25		ns
$t_{OFF(min)}$	Minimum off-time	$V_{HO} – V_{SW}$ = 0V		80		ns
POWER GOOD (PG)						
V_{PG-OV}	PG OV threshold level	Rising with respect to the regulation voltage	107	110	113.5	%
V_{PG-UV}	PG UV threshold level	Falling with respect to the regulated voltage	89	92	95	%
$V_{PG-UV-HYST}$	PG UV hysteresis	Rising with respect to the regulated output		3.6		%
$V_{PG-OV-HYST}$	PG OV hysteresis	Rising with respect to the regulation voltage		3.6		%
t_{OV-DLY}	PG OV filter time	V_{OUT} rising		25		µs
t_{UV-DLY}	PG UV filter time	V_{OUT} falling		25		µs
V_{PG-OL}	PG voltage	Open collector, I_{PG} = 4mA	0.04	0.14	0.8	V
STARTUP (Soft Start)						
t_{SS-INT}	Internal fixed soft-start time		1.5	3	4.2	ms
BOOT CIRCUIT (CBOOT)						
$V_{BOOT-DROP}$	Internal diode forward drop	I_{CBOOT} = 20mA, VCC to CBOOT		0.8		V
I_{BOOT}	CBOOT to SW quiescent current, not switching	V_{EN} = 5V, $V_{CBOOT} – V_{SW}$ = 5V			9	µA
$V_{BOOT-SW-UV-R}$	CBOOT to SW UVLO rising threshold	$V_{CBOOT} – V_{SW}$ rising		2.9		V
$V_{BOOT-SW-UV-F}$	CBOOT to SW UVLO falling threshold	$V_{CBOOT} – V_{SW}$ falling		2.6		V
$V_{BOOT-SW-UV-HYS}$	CBOOT to SW UVLO hysteresis			330		mV
HIGH-SIDE GATE DRIVER (HO)						
$V_{HO-HIGH}$	HO high-state output voltage	I_{HO} = –100mA, $V_{HO-HIGH} = V_{CBOOT} – V_{HO}$		120		mV
V_{HO-LOW}	HO low-state output voltage	I_{HO} = 100mA		60		mV
I_{HO-SRC}	HO peak source current	$V_{HO} = V_{SW}$ = 0V, $V_{CBOOT} = V_{VCC}$ = 5V		1.65		A
$I_{HO-SINK}$	HO peak sink current	V_{VCC} = 5V		2.4		A
LOW-SIDE GATE DRIVER (LO)						
$V_{LO-HIGH}$	LO high-state output voltage	I_{LO} = –100mA		124		mV
V_{LO-LOW}	LO low-state output voltage	I_{LO} = 100mA		60		mV
I_{LO-SRC}	LO peak source current	$V_{LO} = V_{SW}$ = 0V, V_{VCC} = 5V		1.65		A
$I_{LO-SINK}$	LO peak sink current	V_{VCC} = 5V		2.4		A
ADAPTIVE DEADTIME CONTROL						
t_{DEAD1}	HO off to LO on deadtime			18		ns
t_{DEAD2}	LO off to HO on deadtime			22		ns
INTERNAL HICCUP MODE						
HIC_{DLY}	Hiccup mode activation delay	$V_{ISNS} – V_{VOUT}$ > 60mV		512		cycles
HIC_{CYCLES}	HICCUP mode fault	$V_{ISNS} – V_{VOUT}$ > 60mV		16384		cycles
OVERCURRENT PROTECTION						
V_{CS-TH}	Current limit threshold	Measured from ISNS to VOUT	52	60	68	mV

5.5 Electrical Characteristics (continued)

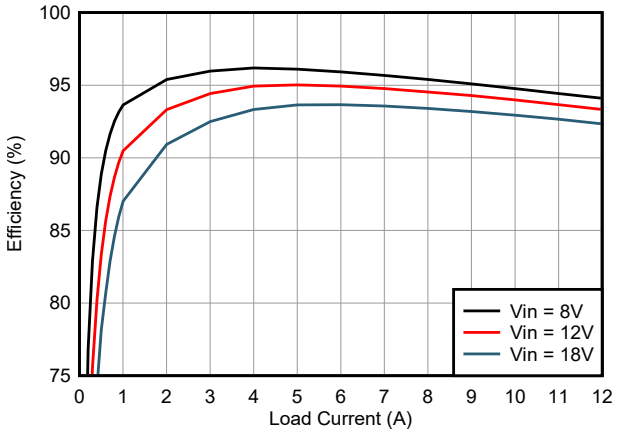
T_J = –40°C to 150°C. Typical values are at T_J = 25°C and V_{IN} = 12V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{DELAY-ISNS}$	ISNS delay to output			70		ns
G_{CS}	CS amplifier gain			10		V/V
$I_{BIAS-ISNS}$	CS amplifier input bias current				1.2	µA
THERMAL SHUTDOWN						
T_{J-SHD}	Thermal shutdown threshold (1)	Temperature rising		175		°C
T_{J-HYS}	Thermal shutdown hysteresis (1)			15		°C

(1) Specified by design. Not production tested.

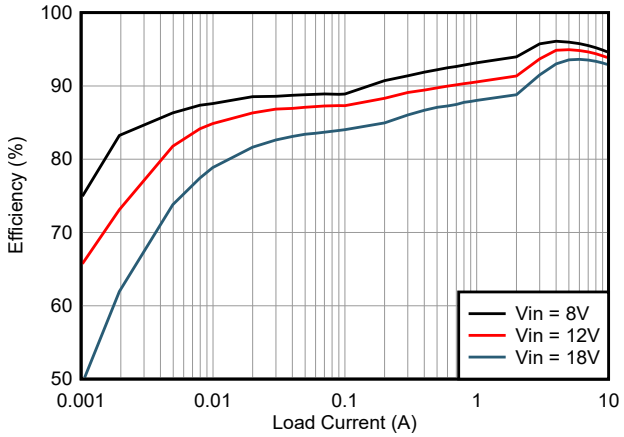
5.6 Typical Characteristics

V_{IN} = 12V, T_J = 25°C, unless otherwise stated.



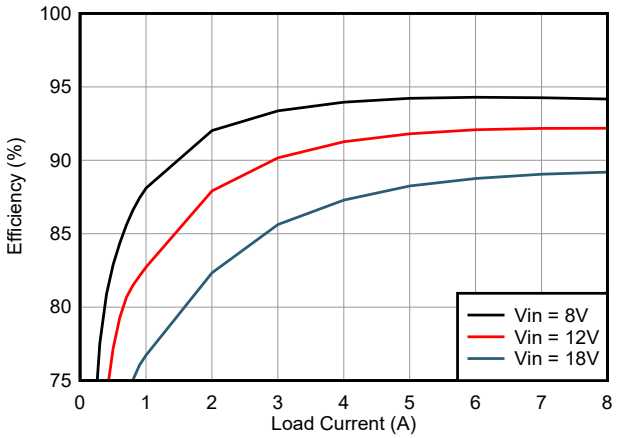
See Section 7.2.2 V_{OUT} = 3.3V F_{SW} = 440kHz

Figure 5-1. Efficiency vs Load, 3.3V Output, FPWM



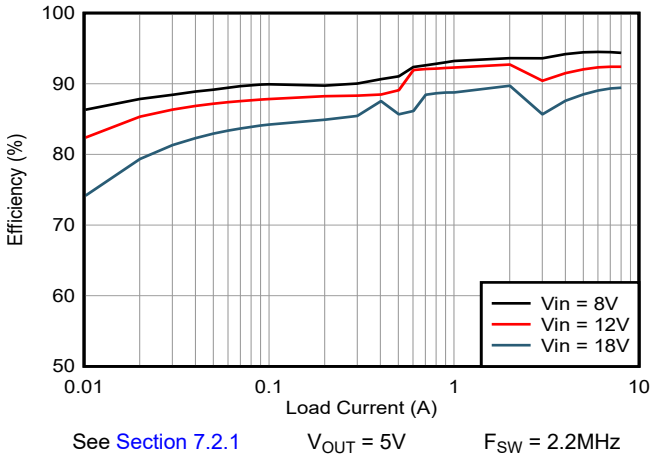
See Section 7.2.2 V_{OUT} = 3.3V F_{SW} = 440kHz

Figure 5-2. Efficiency vs Load, 3.3V Output, PFM



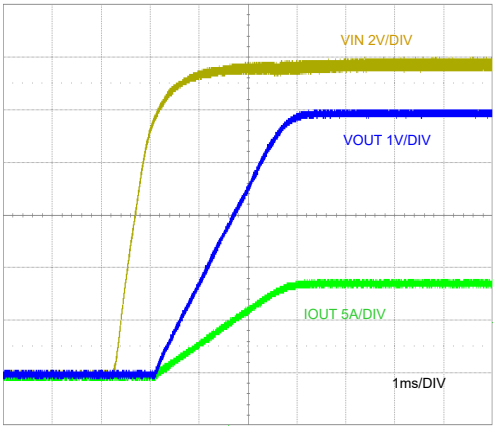
See Section 7.2.1 V_{OUT} = 5V F_{SW} = 2.2MHz

Figure 5-3. Efficiency vs Load, 5V Output, FPWM



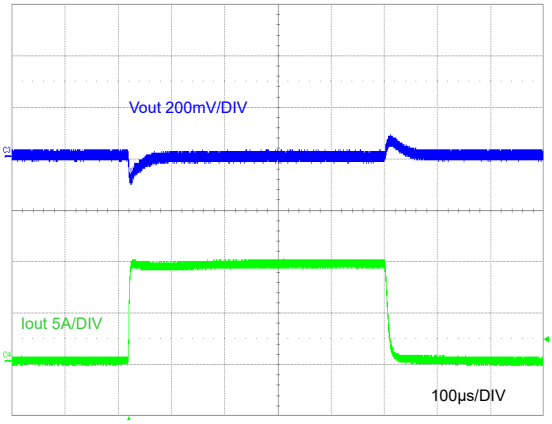
See Section 7.2.1 V_{OUT} = 5V F_{SW} = 2.2MHz

Figure 5-4. Efficiency vs Load, 5V Output, PFM



See Section 7.2.2 8A resistive load

Figure 5-5. Start-Up Characteristic



I_{OUT} = 0A to 10A V_{OUT} = 5V 2A/µs slew rate

Figure 5-6. Load Transient Response

5.6 Typical Characteristics (continued)

V_{IN} = 12V, T_J = 25°C, unless otherwise stated.

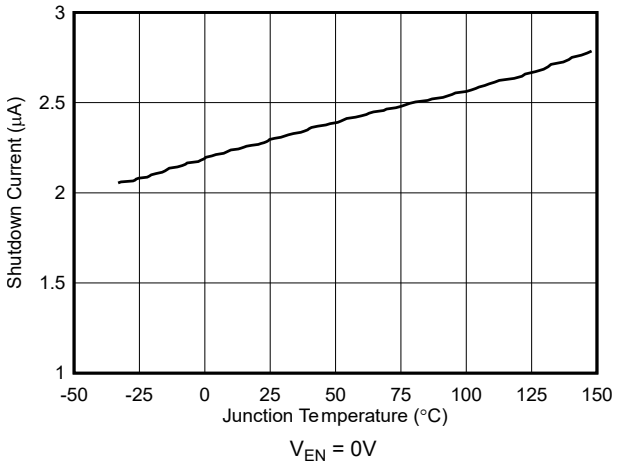


Figure 5-7. Shutdown Quiescent Current vs Temperature

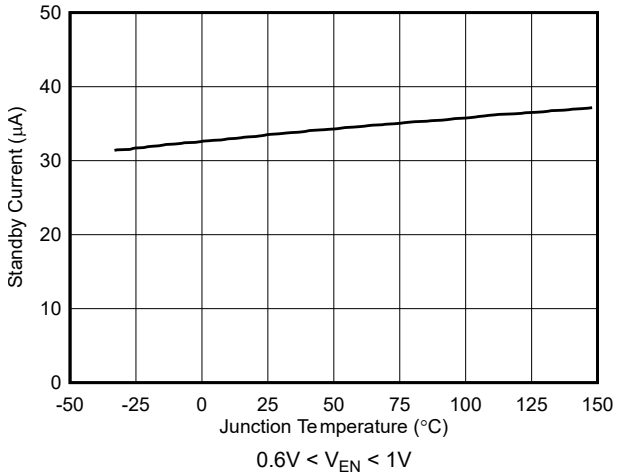


Figure 5-8. Standby Quiescent Current vs Temperature

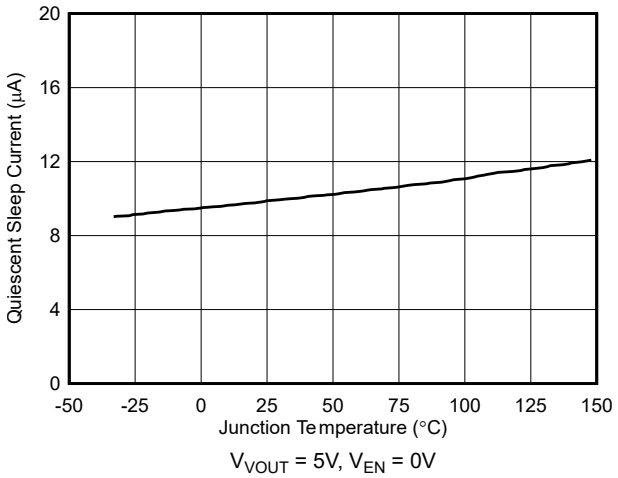


Figure 5-9. Sleep Quiescent Current vs Temperature

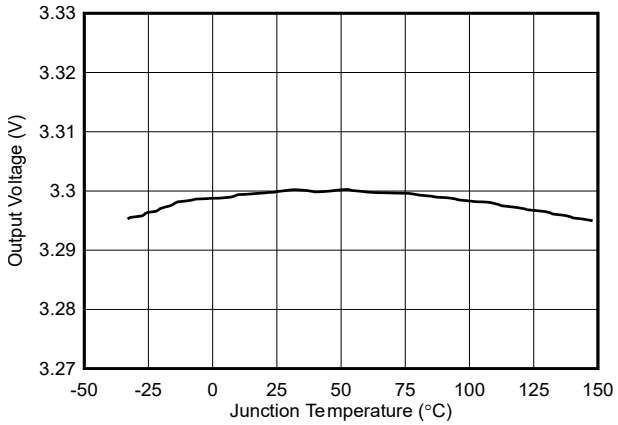


Figure 5-10. Fixed 3.3V Output Voltage vs Temperature

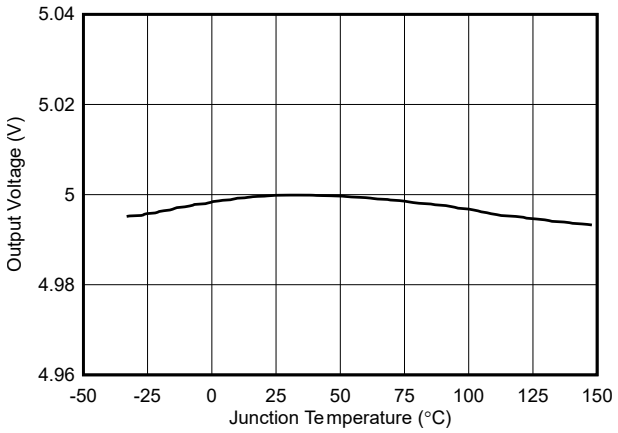


Figure 5-11. Fixed 5V Output Voltage vs Temperature

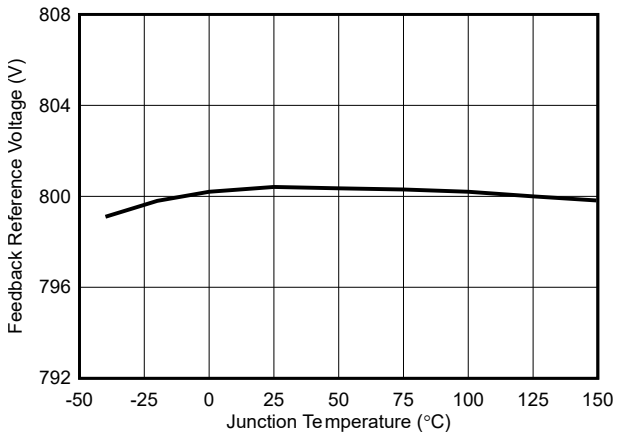


Figure 5-12. Feedback Voltage vs Temperature

5.6 Typical Characteristics (continued)

V_{IN} = 12V, T_J = 25°C, unless otherwise stated.

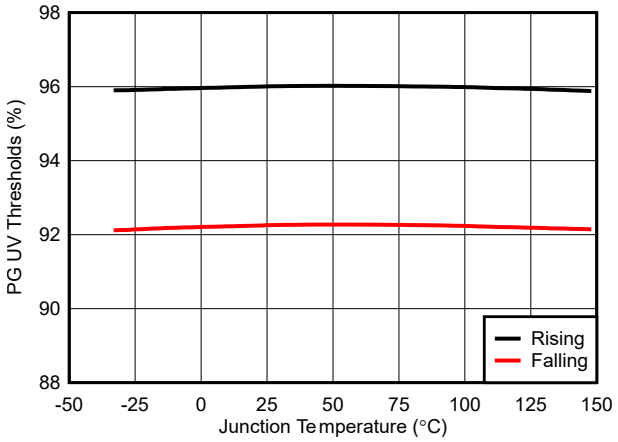


Figure 5-13. PG UV Thresholds vs Temperature

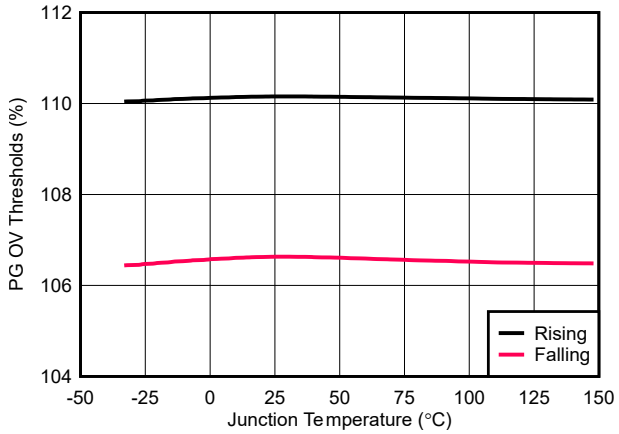
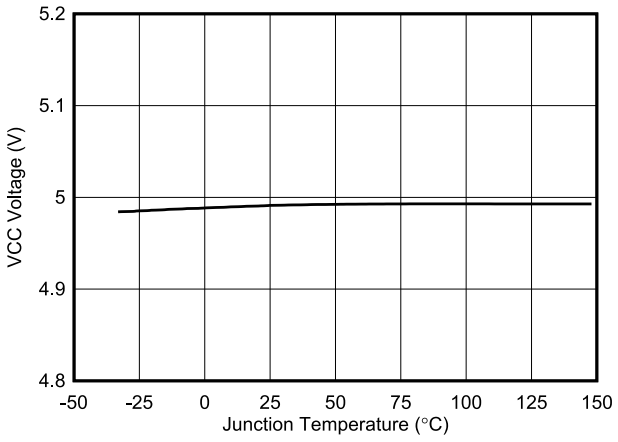


Figure 5-14. PG OV Thresholds vs Temperature



I_{VCC} = 20mA

Figure 5-15. VCC Regulation Voltage vs Temperature

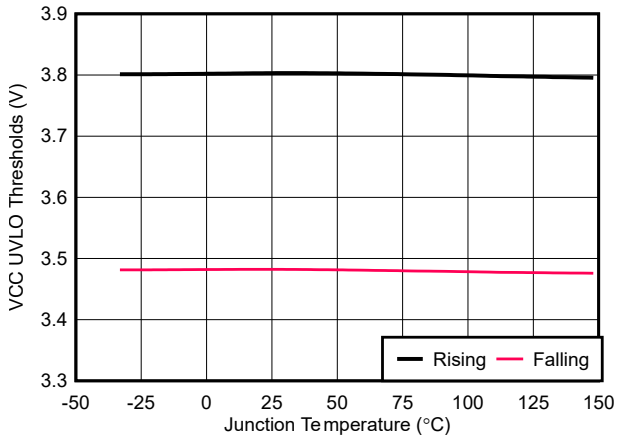


Figure 5-16. VCC UVLO Thresholds vs Temperature

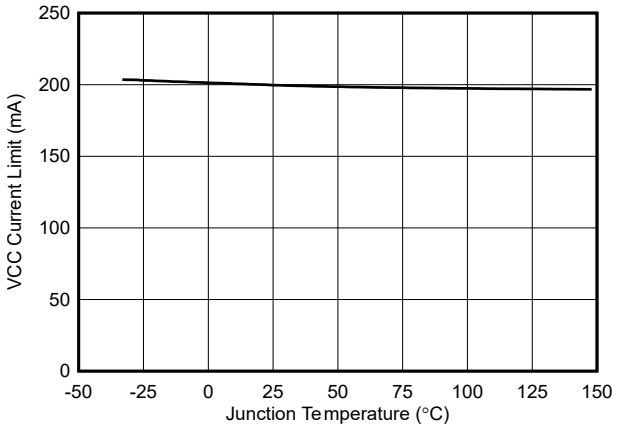


Figure 5-17. VCC Current Limit vs Temperature

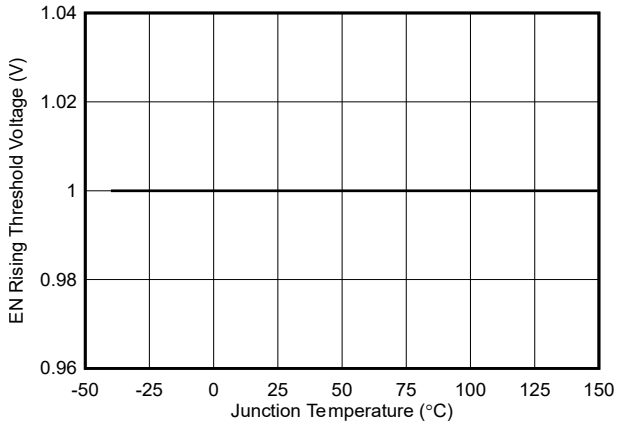


Figure 5-18. EN Rising Threshold Voltage vs Temperature

5.6 Typical Characteristics (continued)

V_{IN} = 12V, T_J = 25°C, unless otherwise stated.

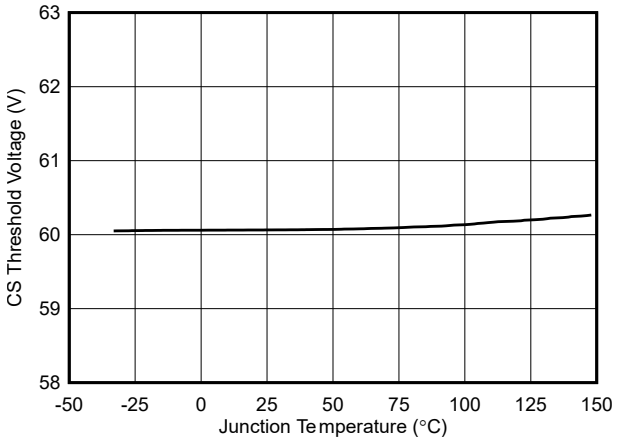


Figure 5-19. Current Sense Threshold vs Temperature

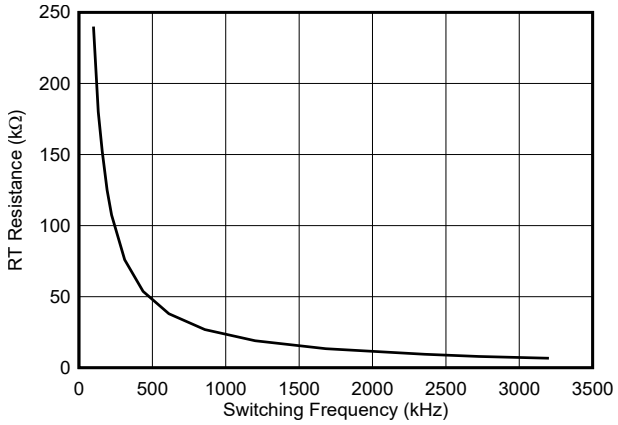


Figure 5-20. RT Resistance vs Switching Frequency

6 Detailed Description

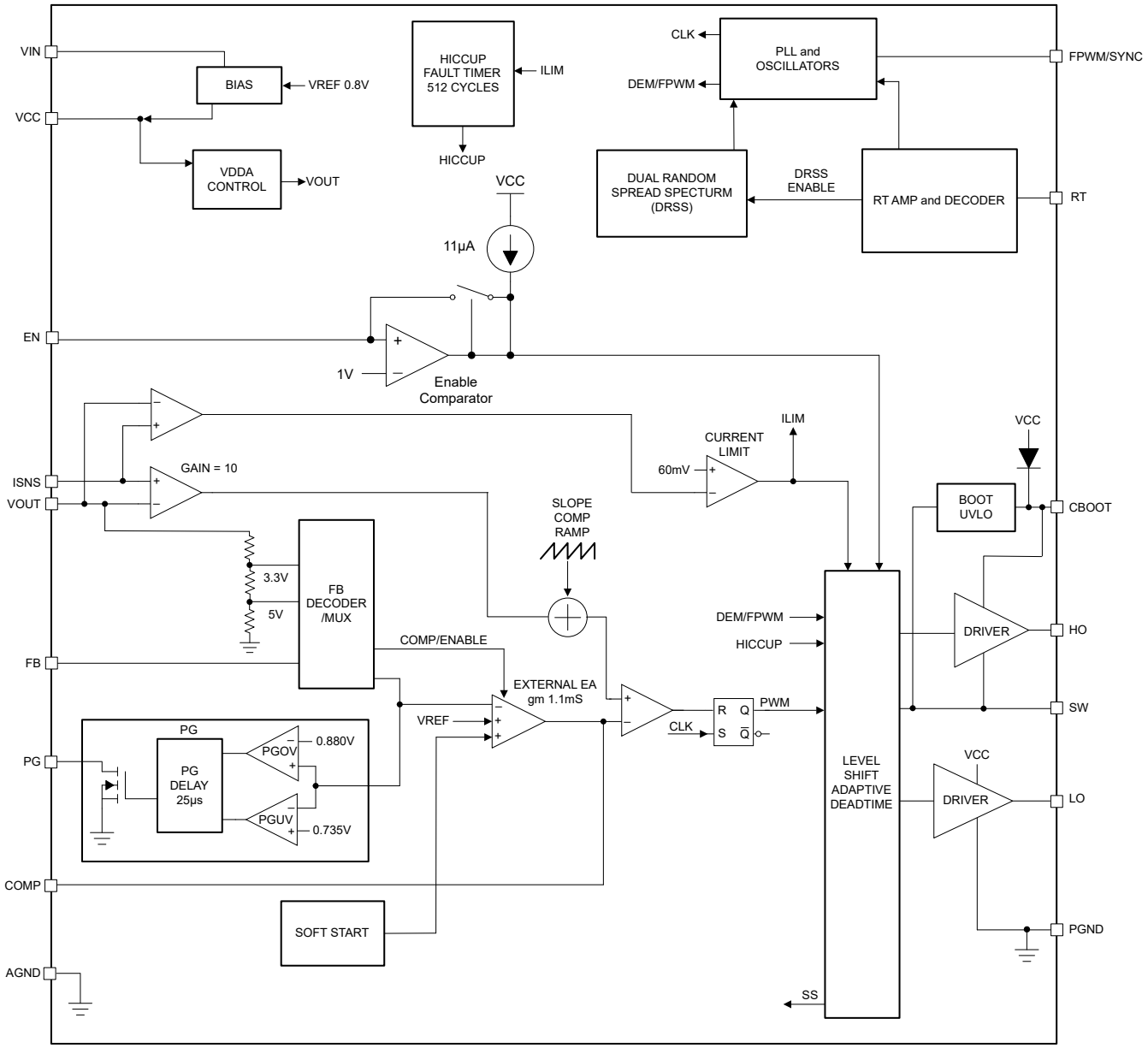
6.1 Overview

The LM25139-Q1 is a switching controller that features all of the functions necessary to implement a high-efficiency synchronous buck power supply operating over a wide input voltage range from 4V to 42V. The LM25139-Q1 is configured to provide a fixed 3.3V, 5V, or an adjustable output between 0.8V to 36V. This easy-to-use controller integrates high-side and low-side MOSFET gate drivers capable of sourcing and sinking peak currents of 1.65A and 2.4A, respectively. Adaptive dead-time control is designed to minimize body diode conduction.

Peak current-mode control using a shunt resistor or inductor DCR current sensing provides inherent line feedforward, cycle-by-cycle peak current limiting, and easy loop compensation. Current-mode control also supports a wide duty cycle range for high input voltage and low-dropout applications as well as when an application require a high step-down conversion ratio (for example, 10-to-1). The oscillator frequency is user-programmable between 100kHz to 3.2MHz, and the frequency can be synchronized as high as 3.2MHz by applying an external clock to FPWM/SYNC. A user-selectable PFM mode feature enables discontinuous conduction mode (DCM) operation to further improve efficiency and reduce power dissipation during light-load conditions.

The LM25139-Q1 incorporates features to simplify the compliance with various EMI standards, such as CISPR 25 Class 5 for automotive applications. DRSS techniques reduce the peak harmonic EMI signature. The LM25139-Q1 is provided in a 16-pin RGT package with an exposed pad to aid in thermal dissipation.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Input Voltage Range (V_{IN})

The LM25139-Q1 operational input voltage range is from 4V to 42V. The device is intended for step-down conversions from 12V and 24V automotive supply rails. The application circuit in Figure 6-1 shows all the necessary components to implement an LM25139-Q1 based wide-V_{IN} step-down regulator using a single supply. The LM25139-Q1 uses an internal LDO subregulator to provide a 5V VCC bias rail for the gate drive and control circuits (assuming the input voltage is higher than 5V plus the necessary subregulator dropout specification).

In high input voltage applications, make sure the VIN and SW pins do not exceed the absolute maximum voltage rating of 45V during line or load transient events. Voltage excursions that exceed the *Absolute Maximum Ratings* can damage the IC. Proceed carefully during PCB board layout and use high-quality input bypass capacitors to minimize voltage overshoot and ringing.

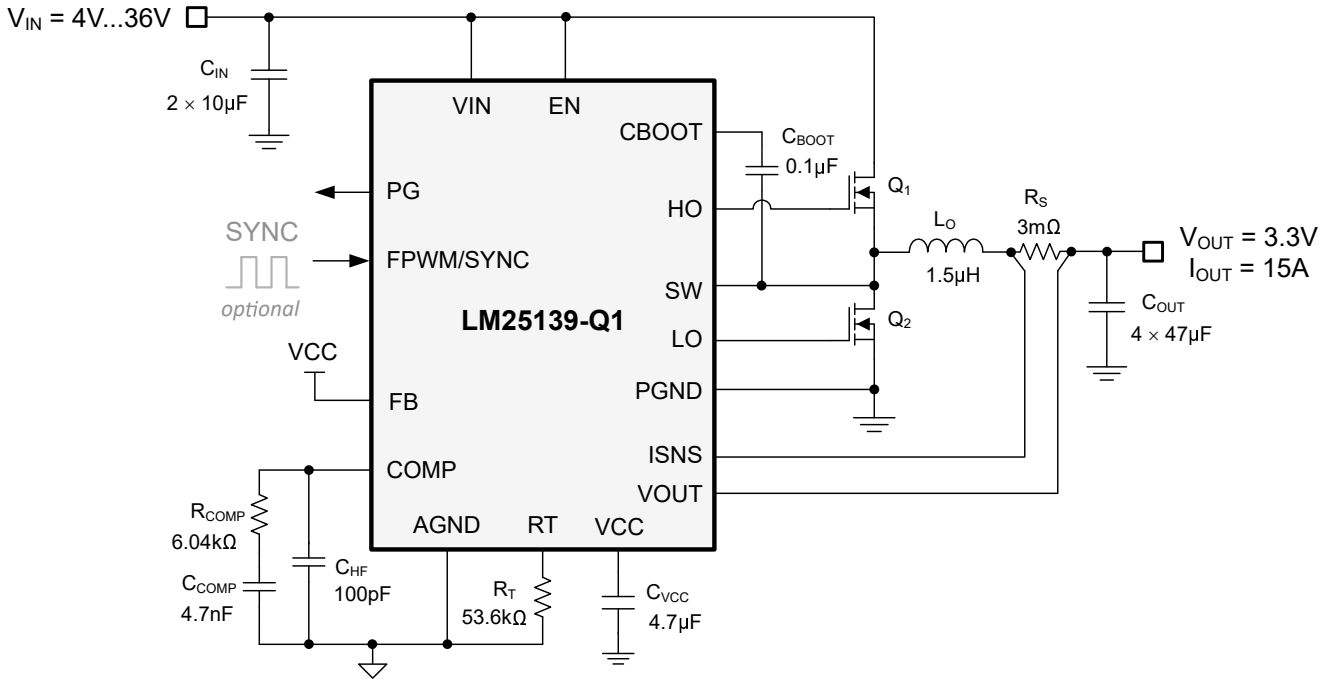


Figure 6-1. Typical Application Schematic

As V_{IN} approaches V_{OUT}, the LM25139-Q1 skips t_{OFF} cycles to allow the controller to extend the duty cycle up to approximately 99%. See also Figure 6-2.

Use Equation 1 to calculate when the LM25139-Q1 enters dropout mode.

- t_p is the oscillator frequency
- t_{OFF} is the minimum off time, typical 80ns

$$V_{IN(min)} = \frac{V_{OUT} \times t_{SW}}{t_{SW} + t_{OFF(min)}} \quad (1)$$

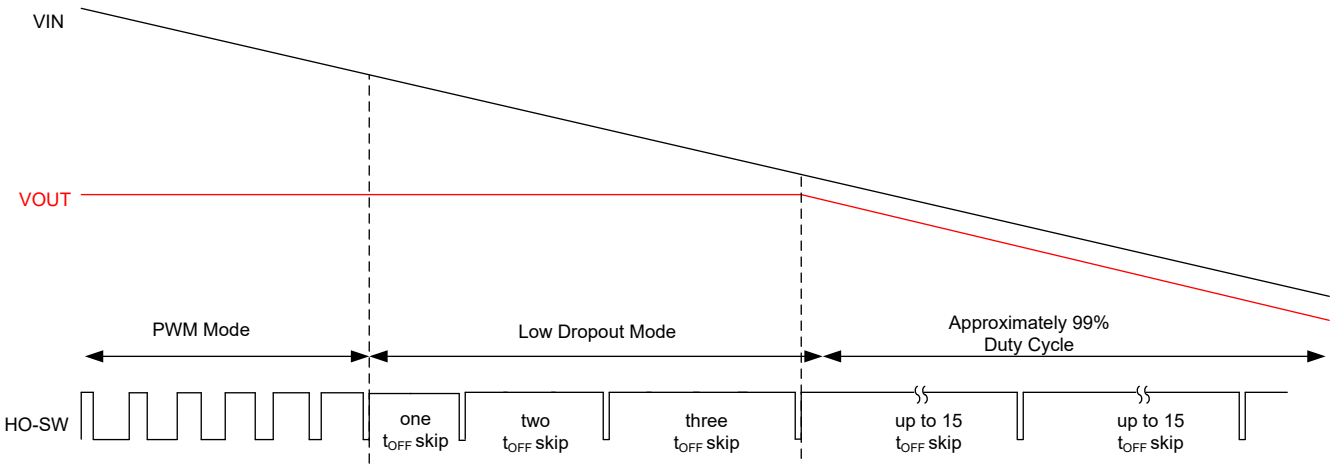


Figure 6-2. Dropout Mode Operation

6.3.2 High-Voltage Bias Supply Regulator (VCC)

The LM25139-Q1 contains an internal high-voltage VCC bias regulator that provides the bias supply for the PWM controller and the gate drivers for the external MOSFETs. The controller is rated to an input voltage up to 42V. However, when the input voltage is below the VCC setpoint level, the VCC voltage tracks V_{IN} minus a small voltage drop.

The VCC regulator output current limit is 210mA (typical). At power up, the controller sources current into the capacitor connected at the VCC pin. When the VCC voltage exceeds 3.8V (typical) and the EN pin is above 1V, the soft-start sequence begins. The output remains active unless the VCC voltage falls below the VCC UVLO falling threshold of 3.5V (typical) or EN is switched to a low state. Connect a ceramic capacitor from VCC to PGND. The recommended range of the VCC capacitor is from 2.2µF to 10µF.

6.3.3 Precision Enable (EN)

The EN pin can be connected to a voltage as high as 42V. The LM25139-Q1 has a precision enable function. When the EN voltage is greater than 1V, switching is enabled. If the EN voltage is below 0.5V, the LM25139-Q1 is in shutdown with an I_Q of 2.3µA (typical) current consumption from V_{IN}. When the EN voltage is between 0.5V and 1V, the LM25139-Q1 is in standby mode, the VCC regulator is active, and the controller is not switching. When the controller is in standby mode, the input quiescent current is 30µA (typical). Enable the LM25139-Q1 with a voltage greater than 1V. However, many applications benefit from using a resistor divider R_{UV1} and R_{UV2}, as shown in Figure 6-3, to establish a precision input UVLO. TI recommends to avoid leaving the EN pin floating.

Use Equation 2 and Equation 3 to calculate the UVLO resistors given the required input turn-on and turn-off voltages.

$$R_{UV1} = \frac{V_{IN(ON)} - V_{IN(OFF)}}{I_{HYS}} \quad (2)$$

$$R_{UV2} = \frac{R_{UV1} \times V_{EN}}{V_{IN(ON)} - V_{EN}} \quad (3)$$

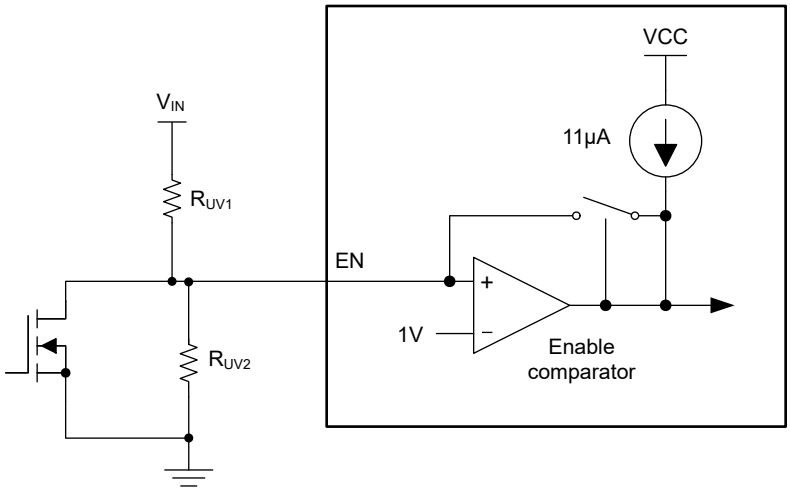


Figure 6-3. Programmable Input Voltage UVLO Turn-On

6.3.4 Power-Good Monitor (PG)

The LM25139-Q1 includes an output voltage monitoring signal for V_{OUT} to simplify sequencing and supervision. The power-good signal is used for start-up sequencing of downstream converters, fault protection, and output monitoring. The power-good output (PG) switches to a high impedance open-drain state when the output voltage is in regulation. The PG switches low when the output voltage drops below the lower power-good threshold (92% typical) or rises above the upper power-good threshold (110% typical). A 25µs deglitch filter prevents false tripping of the PG during transients. TI recommends a pullup resistor of 100kΩ (typical) from PG to the relevant logic rail.

6.3.5 Switching Frequency (RT)

Program the LM25139-Q1 oscillator with a resistor from RT to AGND to set an oscillator frequency between 100kHz and 3.2MHz. Use Equation 4 to calculate the RT resistance for a given switching frequency.

$$R_T\left(k\Omega\right) = \frac{23759}{F_{SW}(kHz)} - 0.72 \quad (4)$$

If the oscillator frequency is set with a resistor from RT to AGND, DRSS is disabled. To enable DRSS, use Equation 4 for the oscillator frequency and connect the resistor from RT to VCC.

6.3.6 Dual Random Spread Spectrum (DRSS)

LM25139-Q1 provides a digital spread spectrum, which reduces the EMI of the power supply over a wide frequency range. DRSS combines a low-frequency triangular modulation profile with a high frequency cycle-by-cycle random modulation profile. The low-frequency triangular modulation improves performance in lower radio-frequency bands, while the high-frequency random modulation improves performance in higher radio frequency bands.

Spread spectrum works by converting a narrowband signal into a wideband signal that spreads the energy over multiple frequencies. Because industry standards require different EMI receiver resolution bandwidth (RBW) settings for different frequency bands, the RBW has an impact on the spread spectrum performance. DRSS is able to simultaneously improve the EMI performance in the low and high RBWs using the low-frequency triangular modulation profile and at high frequency cycle-by-cycle random modulation, respectively. DRSS can reduce conducted emissions up to 15dBµV in the low-frequency band (150kHz to 30MHz) and 5dBµV in the high-frequency band (30MHz to 108MHz).

To enable DRSS, connect a resistor from RT pin to VCC.

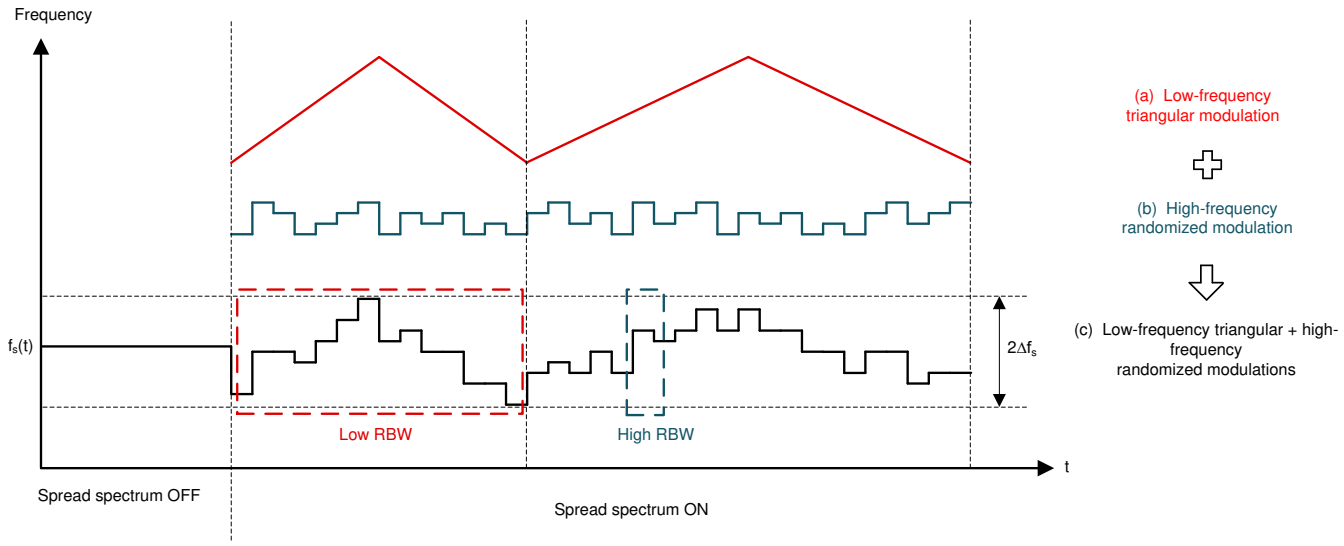


Figure 6-4. Dual Random Spread Spectrum Implementation

6.3.7 Soft Start

The LM25139-Q1 has an internal 3ms soft-start timer (typical). The soft-start feature allows the regulator to gradually reach the steady-state operating point, thus reducing start-up stresses and surges.

6.3.8 Output Voltage Setpoint (FB)

The LM25139-Q1 output can be independently configured for one of two fixed output voltages without external feedback resistors, or adjusted to the desired voltage using an external resistor divider. Set the output to 3.3V by connecting FB directly to VCC. Alternatively, set the output to 5V by installing a 24.9kΩ resistor between FB and VCC. See Table 6-1.

Table 6-1. Feedback Configuration Resistors

PULLUP RESISTOR TO VCC	V_{OUT} SETPOINT
0Ω	3.3V
24.9kΩ	5V
Not installed	External FB divider setting

Alternatively, set the output voltage with an external resistive divider from the output to AGND. The output voltage adjustment range is between 0.8V and 36V. The regulation voltage at FB is 0.8V (V_{REF}). Use Equation 5 to calculate the upper and lower feedback resistors, designated as R_{FB1} and R_{FB2}, respectively.

$$R_{FB1} = \left(\frac{V_{OUT} - 1}{V_{REF}}\right) \times R_{FB2} \quad (5)$$

The recommended starting value for R_{FB2} is between 10kΩ and 20kΩ.

If low-I_Q operation is required, take care when selecting the external feedback resistors. The current consumption of the external divider adds to the LM25139-Q1 sleep current (9.5µA typical). The divider current reflected to V_{IN} is scaled by the ratio of V_{OUT}/V_{IN}.

The FB settings are latched and cannot be changed until either the LM25139-Q1 is powered down (with the VIN voltage decreasing below 3V) and then powered up again. FB setting can also be reconfigured if EN pin going through a disable cycle with EN pin voltage going below 0.5V and then subsequentially rising above 0.5V.

6.3.9 Minimum Controllable On Time

There are two limitations to the minimum output voltage adjustment range: the LM25139-Q1 voltage reference of 0.8V and the minimum controllable switch-node pulse width, $t_{ON(min)}$.

$t_{ON(min)}$ effectively limits the voltage step-down conversion ratio V_{OUT} / V_{IN} at a given switching frequency. For fixed-frequency PWM operation, the voltage conversion ratio must satisfy Equation 6:

$$\frac{V_{OUT}}{V_{IN}} > t_{ON(min)} \times F_{SW} \quad (6)$$

where

- $t_{ON(min)}$ is 25ns (typical).
- F_{SW} is the switching frequency.

If the desired voltage conversion ratio does not meet the above condition, the LM25139-Q1 transitions from fixed switching frequency operation to a pulse-skipping mode to maintain output voltage regulation. For example, if the desired output voltage is 5V with an input voltage of 24V and switching frequency of 2.1MHz, use Equation 7 to verify that the conversion ratio.

$$\frac{5V}{24V} > 25ns \times 2.1MHz \quad (7)$$

$$0.208 > 0.0525 \quad (8)$$

For wide-V_{IN} applications and low output voltages, an alternative is to reduce the LM25139-Q1 switching frequency to meet the requirement of Equation 6.

6.3.10 Error Amplifier and PWM Comparator (FB)

The LM25139-Q1 has a high-gain transconductance amplifier that generates an error current proportional to the difference between the feedback voltage and an internal precision reference (0.8V). The output of the transconductance amplifier connects to the COMP pin, allowing the user to provide external control loop compensation. TI generally recommends a type-II compensation network for peak current-mode control.

In case the output voltage goes below -300mV, comp control of pwm pulses is stopped and low side drive is turned on until the output voltage goes above -300mV. At that point , comp reasserts control of the pwm pulses.

6.3.11 Slope Compensation

The LM25139-Q1 provides internal slope compensation for stable operation with peak current-mode control and a duty cycle greater than 50%. Use Equation 9 to calculate the buck inductance to provide a slope compensation contribution equal to one times the inductor down slope.

$$L_{O\text{-}IDEAL}(\mu H) = \frac{V_{OUT}(V) \times R_S(m\Omega)}{45 \times F_{SW}(MHz)} \quad (9)$$

- A lower inductance value generally increases the peak-to-peak inductor current, which minimizes size and cost, and improves transient response at the cost of reduced light-load efficiency due to higher cores losses and peak currents.
- A higher inductance value generally decreases the peak-to-peak inductor current, reducing switch peak and RMS currents at the cost of requiring larger output capacitors to meet load-transient specifications.

6.3.12 Inductor Current Sense (ISNS, VOUT)

There are two methods to sense the inductor current of the buck power stage. The first uses a current sense resistor (also known as a shunt) in series with the inductor, and the second avails of the DC resistance of the inductor (DCR current sensing).

6.3.12.1 Shunt Current Sensing

Shunt current sensing illustrates inductor current sensing using a shunt resistor. This configuration continuously monitors the inductor current to provide accurate overcurrent protection across the operating temperature range. For optimal current sense accuracy and overcurrent protection, use a low inductance ±1% tolerance shunt resistor between the inductor and the output, with a Kelvin connection to the LM25139-Q1 current sense amplifier.

If the peak voltage signal sensed from ISNS to VOUT exceeds the current limit threshold of 60mV, the current limit comparator immediately terminates the HO output for cycle-by-cycle current limiting. Use Equation 10 to calculate the shunt resistance.

$$R_S = \frac{V_{CS\text{-}TH}}{I_{OUT(CL)} + \frac{\Delta I_L}{2}} \quad (10)$$

where

- $V_{CS\text{-}TH}$ is current sense threshold of 60mV.
- $I_{OUT(CL)}$ is the overcurrent setpoint that is set higher than the maximum load current to avoid tripping the overcurrent comparator during load transients.
- ΔI_L is the peak-to-peak inductor ripple current.

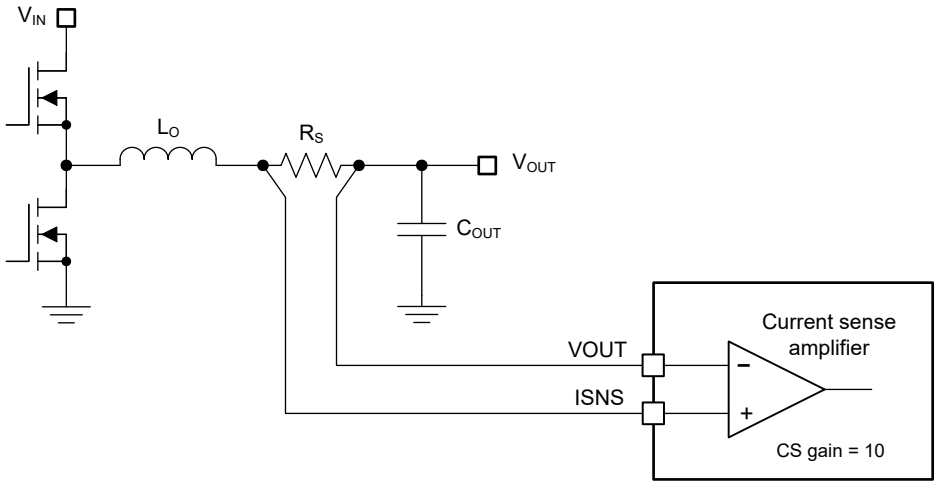


Figure 6-5. Shunt Current Sensing Implementation

The soft-start voltage is clamped 95mV above FB during an overcurrent condition and after soft-start is complete (8ms timer). 16 overcurrent events must occur before the SS clamp is enabled. This amount makes sure that SS can be pulled low during brief overcurrent events, preventing output voltage overshoot during recovery.

6.3.12.2 Inductor DCR Current Sensing

For high-power applications that do not require accurate current-limit protection, inductor DCR current sensing is preferable. This technique provides lossless and continuous monitoring of the inductor current using an RC sense network in parallel with the inductor. Select an inductor with a low DCR tolerance to achieve a typical current limit accuracy within the range of 10% to 15% at room temperature. Components R_{CS} and C_{CS} in Figure 6-6 create a low-pass filter across the inductor to enable differential sensing of the voltage across the inductor DCR.

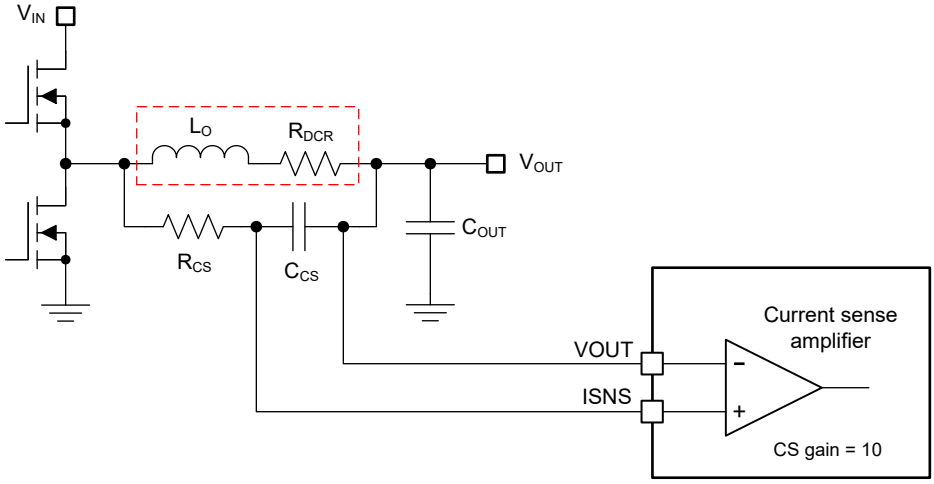


Figure 6-6. Inductor DCR Current Sensing Implementation

Equation 11 shows the voltage drop across the sense capacitor in the s-domain. When the $R_{CS}C_{CS}$ time constant is equal to L_O/R_{DCR}, the voltage developed across the sense capacitor, C_{CS}, is a replica of the inductor DCR voltage and accurate current sensing is achieved. If the $R_{CS}C_{CS}$ time constant is not equal to the L_O/R_{DCR} time constant, there is a sensing error as follows:

- $R_{CS}C_{CS} > L_O/R_{DCR}$ → the DC level is correct, but the AC amplitude is attenuated.
- $R_{CS}C_{CS} < L_O/R_{DCR}$ → the DC level is correct, but the AC amplitude is amplified.

$$V_{CS}(s) = \left(I_{OUT(CL)} + \frac{\Delta I}{2}\right) \times R_{DCR} \times \frac{\left(1 + s\frac{L_O}{R_{DCR}}\right)}{(1 + sR_{CS}C_{CS})} \quad (11)$$

Choose the C_{CS} capacitance greater than or equal to 0.1µF to maintain a low-impedance sensing network, thus reducing the susceptibility of noise pickup from the switch node. Carefully observe Section 7.4.1 to make sure that noise and DC errors do not corrupt the current sense signals applied between the ISNS and VOUT pins.

6.3.12.3 Hiccup-Mode Current Limiting

The LM25139-Q1 includes an internal hiccup-mode protection function. After an overload is detected, 512 cycles of cycle-by-cycle current limiting occurs. The 512-cycle counter is reset if four consecutive switching cycles occur without exceeding the current limit threshold. After the 512-cycle counter has expired, the internal soft start is pulled low, the HO and LO driver outputs are disabled, and the 16384-cycle hiccup counter is enabled. After the counter reaches 16384, the internal soft start is enabled and the output restarts. The hiccup-mode current limit is disabled during soft start until after soft start is complete (8ms) and the output voltage has reached half the regulation value.

6.4 Device Functional Modes

6.4.1 Sleep Mode

The LM25139-Q1 operates with peak current-mode control such that the COMP voltage is proportional to the peak inductor current. During no-load or light-load conditions, the output capacitor discharges very slowly. As a result, the COMP voltage does not demand the driver output pulses on a cycle-by-cycle basis. When the LM25139-Q1 controller detects 16 missed switching cycles, the LM25139-Q1 enters sleep mode and switches to a low I_Q state to reduce the current drawn from the input. The typical controller I_Q in sleep mode is 10µA with a 3.3V output.

6.4.2 Forced PWM and Synchronization (FPWM/SYNC)

A synchronous buck regulator implemented with a low-side synchronous MOSFET rather than a diode has the capability to sink negative current from the output during conditions of, light-load, output overvoltage, and prebias start-up conditions. The LM25139-Q1 provides a diode emulation feature, also called PFM mode, that can be enabled to prevent reverse (drain-to-source) current flow in the low-side MOSFET. When configured for PFM mode, the low-side MOSFET is switched off when reverse current flow is detected by sensing the inductor current ($V_{ISNS} – V_{OUT}$) using either current sense resistor or inductor DCR sensing method. The sensed inductor current is compared against a zero-cross threshold (5.5mV) to indicate reverse current flow. In PFM mode, the peak inductor current is forced to be at a minimum of 20% of the current limit. The benefit of this configuration is lower power loss during light-load conditions; the disadvantage of PFM mode is slower light-load transient response.

Configure PFM using the FPWM/SYNC pin. To enable PFM and thus achieve low-I_Q current at light loads, connect FPWM/SYNC to GND. If FPWM with continuous conduction mode (CCM) operation is desired, tie FPWM/SYNC to VCC. Note that PFM mode is automatically engaged to prevent reverse current flow during a prebias start-up. If the device has been configured to operate in FPWM mode, the device still starts up in PFM mode and takes 1000 cycles of switching pulses to transition from PFM to FPWM mode during start-up.

The LM25139-Q1 has a 35µs typical deglitch filter to transition from FPWM to PFM mode. After the deglitch filter expires, the peak inductor current is forced to be at a minimum of 20% of the current limit and a zero current threshold of 5.5mV is enabled. The transition from PFM mode to FPWM mode is in two stages. In first stage the minimum peak current limit of 20% is removed immediately. Subsequently, the 5.5mV zero current threshold is linearly reduced to a negative current limit of 30mV over 1000 high-side FET switching cycles.

To synchronize the LM25139-Q1 to an external source, apply a logic-level clock to FPWM/SYNC. The LM25139-Q1 can be synchronized to ±20% of the RT programmed frequency up to a maximum of 3.2MHz. If there is an RT resistor and a synchronization signal, the LM25139-Q1 ignores the RT resistor and synchronizes to the external clock. Under low-V_{IN} conditions when the minimum off time is reached, the synchronization signal is ignored, allowing the switching frequency to be reduced to maintain output voltage regulation.

The LM25139-Q1 can be placed into standby mode by applying an external clock on the FPWM/SYNC while the EN voltage is low. This action turns on the VCC regulator to allow for a faster turn-on time when EN is driven above 1V.

6.4.3 Thermal Shutdown

The LM25139-Q1 includes an internal junction temperature monitor. If the temperature exceeds 175°C (typical), thermal shutdown occurs. When entering thermal shutdown, the device:

1. Turns off the high-side and low-side MOSFETs
2. PG switches low
3. Turns off the VCC regulator
4. Initiates a soft-start sequence when the die temperature decreases by the thermal shutdown hysteresis of 15°C (typical)

This protection is a non-latching protection and as such, the device cycles into and out of thermal shutdown if the fault persists.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Power Train Components

A comprehensive understanding of the buck regulator power train components is critical to successfully completing a synchronous buck regulator design. The following sections discuss the output inductor, input and output capacitors, power MOSFETs, and EMI input filter.

7.1.1.1 Buck Inductor

For most applications, choose a buck inductance such that the inductor ripple current, ΔI_L, is between 30% to 50% of the maximum DC output current at nominal input voltage. Use Equation 12 to choose the inductance based on a peak inductor current given by Equation 13.

$$L = \frac{V_{OUT}}{\Delta I_L \times F_{SW}} \times \left(1 - \frac{V_{OUT}}{V_{IN(nom)}}\right) \quad (12)$$

$$I_{L(peak)} = I_{OUT} + \frac{\Delta I_L}{2} \quad (13)$$

Check the inductor data sheet to make sure that the saturation current of the inductor is well above the peak inductor current of a particular design. Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can then concentrate on copper loss and preventing saturation. Low inductor core loss is evidenced by reduced no-load input current and higher light-load efficiency. However, ferrite core materials exhibit a hard saturation characteristic and the inductance collapses abruptly when the saturation current is exceeded. This action results in an abrupt increase in inductor ripple current and higher output voltage ripple, not to mention reduced efficiency and compromised reliability. Note that the saturation current of an inductor generally decreases as the core temperature increases. Of course, accurate overcurrent protection is key to avoiding inductor saturation.

7.1.1.2 Output Capacitors

Ordinarily, the output capacitor energy storage of the regulator combined with the control loop response are prescribed to maintain the integrity of the output voltage within the dynamic (transient) tolerance specifications. The usual boundaries restricting the output capacitor in power management applications are driven by finite available PCB area, component footprint and profile, and cost. The capacitor parasitics—equivalent series resistance (ESR) and equivalent series inductance (ESL)—take greater precedence in shaping the load transient response of the regulator as the load step amplitude and slew rate increase.

The output capacitor, C_{OUT}, filters the inductor ripple current and provides a reservoir of charge for step-load transient events. Typically, ceramic capacitors provide extremely low ESR to reduce the output voltage ripple and noise spikes, while tantalum and electrolytic capacitors provide a large bulk capacitance in a relatively compact footprint for transient loading events.

Based on the static specification of peak-to-peak output voltage ripple denoted by ΔV_{OUT}, choose an output capacitance that is larger than that shown with Equation 14.

$$C_{OUT} \geq \frac{L_O \times \Delta I_{OUT}^2}{\left(V_{OUT} + \Delta V_{OVERSHOOT}\right)^2 - V_{OUT}^2} \quad (14)$$

Figure 7-1 conceptually illustrates the relevant current waveforms during both load step-up and step-down transitions. As shown, the large-signal slew rate of the inductor current is limited as the inductor current ramps to match the new load-current level following a load transient. This slew-rate limiting exacerbates the deficit of charge in the output capacitor, which must be replenished as fast as possible during and after the load step-up transient. Similarly, during and after a load step-down transient, the slew rate limiting of the inductor current adds to the surplus of charge in the output capacitor that must be depleted as quickly as possible.

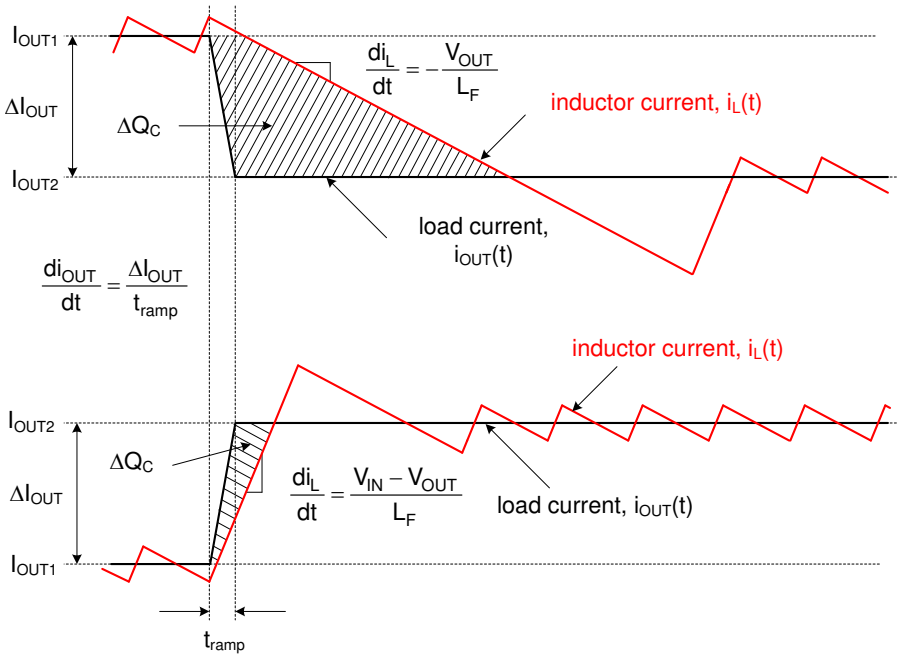


Figure 7-1. Load Transient Response Representation Showing C_{OUT} Charge Surplus or Deficit

In a typical regulator application of 12V input to low output voltage (for example, 3.3V), the load-off transient represents the worst case in terms of output voltage transient deviation. In that conversion ratio application, the steady-state duty cycle is approximately 28% and the large-signal inductor current slew rate when the duty cycle collapses to zero is approximately $-V_{OUT}$ / L. Compared to a load-on transient, the inductor current takes much longer to transition to the required level. The surplus of charge in the output capacitor causes the output voltage to significantly overshoot. In fact, to deplete this excess charge from the output capacitor as quickly as possible, the inductor current must ramp below the nominal level following the load step. In this scenario, a large output capacitance can be advantageously employed to absorb the excess charge and minimize the voltage overshoot.

To meet the dynamic specification of output voltage overshoot during such a load-off transient (denoted as $\Delta V_{OVERSHOOT}$ with step reduction in output current given by ΔI_{OUT}), the output capacitance must be larger than:

$$C_{OUT} \geq \frac{L_O \times \Delta I_{OUT}^2}{(V_{OUT} + \Delta V_{OVERSHOOT})^2 - V_{OUT}^2} \quad (15)$$

The ESR of a capacitor is provided in the manufacturer data sheet either explicitly as a specification or implicitly in the impedance versus frequency curve. Depending on type, size, and construction, electrolytic capacitors have significant ESR, 5mΩ and above, and relatively large ESL, 5nH to 20nH. PCB traces contribute some parasitic resistance and inductance as well. Ceramic output capacitors have low ESR and ESL contributions at the switching frequency, and the capacitive impedance component dominates. However, depending on package and voltage rating of the ceramic capacitor, the effective capacitance can drop quite significantly with applied DC voltage and operating temperature.

Ignoring the ESR term in Equation 14 gives a quick estimation of the minimum ceramic capacitance necessary to meet the output ripple specification. Two to four 47µF, 10V, X7R capacitors in 1206 or 1210 footprint is a

common choice for a 5V output. Use Equation 15 to determine if additional capacitance is necessary to meet the load-off transient overshoot specification.

A composite implementation of ceramic and electrolytic capacitors highlights the rationale for paralleling capacitors of dissimilar chemistries yet complementary performance. The frequency response of each capacitor is accretive in that each capacitor provides desirable performance over a certain portion of the frequency range. While the ceramic provides excellent mid and high-frequency decoupling characteristics with the low ESR and ESL to minimize the switching frequency output ripple, the electrolytic device with the large bulk capacitance provides low-frequency energy storage to cope with load transient demands.

7.1.1.3 Input Capacitors

Input capacitors are necessary to limit the input ripple voltage to the buck power stage due to switching-frequency AC currents. TI recommends using X7S or X7R dielectric ceramic capacitors to provide low impedance and high RMS current rating over a wide temperature range. To minimize the parasitic inductance in the switching loop, position the input capacitors as close as possible to the drain of the high-side MOSFET and the source of the low-side MOSFET. Use Equation 16 to calculate the input capacitor RMS current for a single-channel buck regulator.

$$I_{CIN(RMS)} = \sqrt{D \times \left(I_{OUT}^2 \times (1 - D) + \frac{\Delta I_L^2}{12} \right)} \tag{16}$$

The highest input capacitor RMS current occurs at D = 0.5, at which point the RMS current rating of the input capacitors must be greater than half the output current.

Ideally, the DC component of input current is provided by the input voltage source and the AC component by the input filter capacitors. Neglecting inductor ripple current, the input capacitors source current of amplitude (I_{OUT} − I_{IN}) during the D interval and sinks I_{IN} during the 1−D interval. Thus, the input capacitors conduct a square-wave current of peak-to-peak amplitude equal to the output current. Following, the resultant capacitive component of AC ripple voltage is a triangular waveform. Together with the ESR-related ripple component, use Equation 17 to calculate the peak-to-peak ripple voltage amplitude.

$$\Delta V_{IN} = \frac{I_{OUT} \times D \times (1 - D)}{F_{SW} \times C_{IN}} + I_{OUT} \times R_{ESR} \tag{17}$$

Equation 18 calculates the input capacitance required for a particular load current, based on an input voltage ripple specification of ΔV_{IN}.

$$C_{IN} \geq \frac{D \times (1 - D) \times I_{OUT}}{F_{SW} \times (\Delta V_{IN} - R_{ESR} \times I_{OUT})} \tag{18}$$

Low-ESR ceramic capacitors can be placed in parallel with higher valued bulk capacitance to provide optimized input filtering for the regulator and damping to mitigate the effects of input parasitic inductance resonating with high-Q ceramics. One bulk capacitor of sufficiently high current rating and four 10µF, 50V X7R ceramic decoupling capacitors are usually sufficient for 12V battery automotive applications. Select the input bulk capacitor based on the ripple current rating and operating temperature range.

7.1.1.4 Power MOSFETs

The choice of power MOSFETs has significant impact on DC/DC regulator performance. A MOSFET with low on-state resistance, $R_{DS(on)}$, reduces conduction loss, whereas low parasitic capacitances enable faster transition times and reduced switching loss. Normally, the lower the $R_{DS(on)}$ of a MOSFET, the higher the gate charge and output charge (Q_G and Q_{OSS}, respectively), and vice-versa. As a result, the product of $R_{DS(on)}$ and Q_G is commonly specified as a MOSFET figure-of-merit. Low thermal resistance of a given package make sure that the MOSFET power dissipation does not result in excessive MOSFET die temperature.

The main parameters affecting power MOSFET selection in an LM25139-Q1 application are as follows:

- $R_{DS(on)}$ at V_{GS} = 5V
- Drain-source voltage rating, BV_{DSS}, typically 40V or 60V, depending on the maximum input voltage
- Gate charge parameters at V_{GS} = 5V
- Output charge, Q_{OSS}, at the relevant input voltage
- Body diode reverse recovery charge, Q_{RR}
- Gate threshold voltage, $V_{GS(th)}$, derived from the Miller plateau evident in the Q_G versus V_{GS} plot in the MOSFET data sheet. With a Miller plateau voltage typically in the range of 2V to 3V, the 5V gate drive amplitude of the LM25139-Q1 provides an adequately enhanced MOSFET when on and a margin against Cdv/dt shoot-through when off.

The MOSFET-related power losses for one channel are summarized by the equations presented in Table 7-1, where suffixes one and two represent high-side and low-side MOSFET parameters, respectively. While the influence of inductor ripple current is considered, second-order loss modes, such as those related to parasitic inductances and SW node ringing, are not included.

Table 7-1. MOSFET Power Losses

POWER LOSS MODE	HIGH-SIDE MOSFET	LOW-SIDE MOSFET
MOSFET conduction(2) (3)	$P_{cond1} = D \times \left(I_{OUT}^2 + \frac{\Delta I_L^2}{12} \right) \times R_{DS(on)1}$	$P_{cond2} = D' \times \left(I_{OUT}^2 + \frac{\Delta I_L^2}{12} \right) \times R_{DS(on)2}$
MOSFET switching	$P_{sw1} = \frac{V_{IN} \times F_{SW}}{2} \times \left[\left(I_{OUT} - \frac{\Delta I_L}{2} \right) \times t_R + \left(I_{OUT} + \frac{\Delta I_L}{2} \right) \times t_F \right]$	Negligible
MOSFET gate drive(1)	$P_{Gate1} = V_{CC} \times F_{SW} \times Q_{G1}$	$P_{Gate2} = V_{CC} \times F_{SW} \times Q_{G2}$
MOSFET output charge(4)	$P_{Coss} = F_{SW} \times (V_{IN} \times Q_{oss2} + E_{oss1} - E_{oss2})$	
Body diode conduction	N/A	$P_{condBD} = V_F \times F_{SW} \times \left[\left(I_{OUT} + \frac{\Delta I_L}{2} \right) \times t_{dt1} + \left(I_{OUT} - \frac{\Delta I_L}{2} \right) \times t_{dt2} \right]$
Body diode reverse recovery(5)	$P_{RR} = V_{IN} \times F_{SW} \times Q_{RR2}$	

(1) Gate drive loss is apportioned based on the internal gate resistance of the MOSFET, externally added series gate resistance and the relevant driver resistance of the LM25139-Q1.
(2) MOSFET $R_{DS(on)}$ has a positive temperature coefficient of approximately 4500ppm/°C. The MOSFET junction temperature, T_J, and the rise over ambient temperature is dependent upon the device total power dissipation and the thermal impedance. When operating at or near minimum input voltage, make sure that the MOSFET $R_{DS(on)}$ is rated for the available gate drive voltage.
(3) D' = 1–D is the duty cycle complement.
(4) MOSFET output capacitances, C_{oss1} and C_{oss2}, are highly non-linear with voltage. These capacitances are charged losslessly by the inductor current at high-side MOSFET turn-off. During turn-on, however, a current flows from the input to charge the output capacitance of the low-side MOSFET. E_{oss1}, the energy of C_{oss1}, is dissipated at turn-on, but this is offset by the stored energy E_{oss2} on C_{oss2}.
(5) MOSFET body diode reverse recovery charge, Q_{RR}, depends on many parameters, particularly forward current, current transition speed and temperature.

The high-side (control) MOSFET carries the inductor current during the PWM on time (or D interval) and typically incurs most of the switching losses. Choosing a high-side MOSFET that balances conduction and switching loss contributions is therefor imperative. The total power dissipation in the high-side MOSFET is the sum of the losses due to conduction, switching (voltage-current overlap), output charge, and typically two-thirds of the net loss attributed to body diode reverse recovery.

The low-side (synchronous) MOSFET carries the inductor current when the high-side MOSFET is off (or during the 1–D interval). The low-side MOSFET switching loss is negligible as the low-side MOSFET switching loss is switched at zero voltage – current just communicates from the channel to the body diode or vice versa during the transition dead times. The LM25139-Q1, with the adaptive gate drive timing, minimizes body diode conduction losses when both MOSFETs are off. Such losses scale directly with switching frequency.

In high step-down ratio applications, the low-side MOSFET carries the current for a large portion of the switching period. Therefore, to attain high efficiency, optimizing the low-side MOSFET for low $R_{DS(on)}$ is critical. In cases where the conduction loss is too high or the target $R_{DS(on)}$ is lower than available in a single MOSFET, connect two low-side MOSFETs in parallel. The total power dissipation of the low-side MOSFET is the sum of the losses due to channel conduction, body diode conduction, and typically one-third of the net loss attributed to body diode reverse recovery. The LM25139-Q1 is well-designed to drive TI's portfolio of NexFET™ power MOSFETs.

7.1.1.5 EMI Filter

Switching regulators exhibit negative input impedance, which is lowest at the minimum input voltage. An underdamped LC filter exhibits a high output impedance at the resonant frequency of the filter. For stability, the filter output impedance must be less than the absolute value of the converter input impedance.

$$Z_{IN} = \left| -\frac{V_{IN(min)}^2}{P_{IN}} \right| \tag{19}$$

The passive EMI filter design steps are as follows:

- Calculate the required attenuation of the EMI filter at the switching frequency, where C_{IN} represents the existing capacitance at the input of the switching converter.
- Input filter inductor L_{IN} is usually selected between 1µH and 10µH, but can be lower to reduce losses in a high-current design.
- Calculate input filter capacitor C_F.

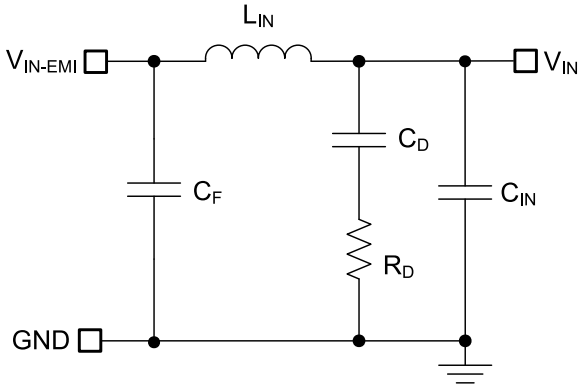


Figure 7-2. Passive π-Stage EMI Filter for Buck Regulator

By calculating the first harmonic current from the Fourier series of the input current waveform and multiplying by the input impedance (the impedance is defined by the existing input capacitor C_{IN}), use Equation 20 to show a formula derived to obtain the required attenuation.

$$Attn = 20\log\left(\frac{I_{L(PEAK)}}{\pi^2 \times F_{SW} \times C_{IN}} \times \sin(\pi \times D_{MAX}) \times \frac{1}{1\mu V}\right) - V_{MAX} \tag{20}$$

where

- V_{MAX} is the allowed dBµV noise level for the applicable conducted EMI specification, for example CISPR 32 Class B.
- C_{IN} is the existing input capacitance of the buck regulator.
- D_{MAX} is the maximum duty cycle.
- I_{PEAK} is the peak inductor current.

For filter design purposes, the current at the input can be modeled as a square-wave. Use Equation 21 to determine the passive EMI filter capacitance C_F.

$$C_F = \frac{1}{L_{IN}} \times \left(\frac{10^{\frac{|Attn|}{40}}}{2\pi \times F_{SW}} \right)^2 \quad (21)$$

Adding an input filter to a switching regulator modifies the control-to-output transfer function. The output impedance of the filter must be sufficiently small so that the input filter does not significantly affect the loop gain of the buck converter. The impedance peaks at the filter resonant frequency. Use Equation 22 to calculate the resonant frequency of the passive filter.

$$f_{res} = \frac{1}{2\pi \times \sqrt{L_{IN} \times C_F}} \quad (22)$$

The purpose of R_D is to reduce the peak output impedance of the filter at the resonant frequency. Capacitor C_D blocks the DC component of the input voltage to avoid excessive power dissipation in R_D. Capacitor C_D must have lower impedance than R_D at the resonant frequency with a capacitance value greater than that of the input capacitor C_{IN}. This requirement prevents C_{IN} from interfering with the cutoff frequency of the main filter. Added input damping is needed when the output impedance of the filter is high at the resonant frequency (Q of filter formed by L_{IN} and C_{IN} is too high). An electrolytic capacitor C_D can be used for input damping with a value shown using Equation 23.

$$C_D \geq 4 \times C_{IN} \quad (23)$$

Use Equation 24 to select the input damping resistor R_D.

$$R_D = \sqrt{\frac{L_{IN}}{C_{IN}}} \quad (24)$$

7.1.2 Error Amplifier and Compensation

Figure 7-3 shows a type-II compensator using a transconductance error amplifier (EA). The dominant pole of the EA open-loop gain is set by the EA output resistance, $R_{O\text{-}EA}$, and effective bandwidth-limiting capacitance, C_{BW}, as shown by Equation 25.

$$G_{EA(openloop)}(s) = -\frac{g_m \times R_{O-EA}}{1 + s \times R_{O-EA} \times C_{BW}} \quad (25)$$

The EA high-frequency pole is neglected in the above expression. Equation 26 calculates the compensator transfer function from output voltage to COMP node, including the gain contribution from the (internal or external) feedback resistor network.

$$G_c(s) = \frac{\hat{v}_c(s)}{\hat{v}_{out}(s)} = -\frac{V_{REF}}{V_{OUT}} \times \frac{g_m \times R_{O-EA} \times \left(1 + \frac{s}{\omega_{z1}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right) \times \left(1 + \frac{s}{\omega_{p2}}\right)} \quad (26)$$

where

- V_{REF} is the feedback voltage reference of 0.8V.
- g_m is the EA gain transconductance of 1.1mS.
- $R_{O\text{-}EA}$ is the error amplifier output impedance of 10MΩ.

$$\omega_{z1} = \frac{1}{R_{COMP} \times C_{COMP}} \quad (27)$$

$$\omega_{p1} = \frac{1}{R_{O-EA} \times (C_{COMP} + C_{HF} + C_{BW})} \cong \frac{1}{R_{O-EA} \times C_{COMP}} \quad (28)$$

$$\omega_{p2} = \frac{1}{R_{COMP} \times (C_{COMP} || (C_{HF} + C_{BW}))} \cong \frac{1}{R_{COMP} \times C_{COMP}} \quad (29)$$

The EA compensation components create a pole close to the origin, a zero, and a high-frequency pole. Typically, R_{COMP} << R_{O-EA} and C_{COMP} >> C_{BW} and C_{HF}, so the approximations are valid.

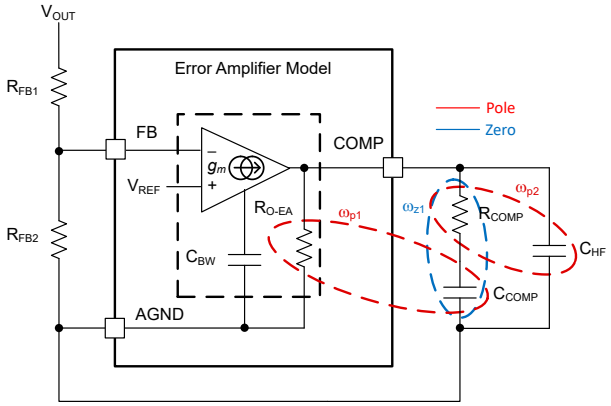


Figure 7-3. Error Amplifier and Compensation Network

7.2 Typical Applications

7.2.1 Design 1 – High Efficiency 2.2MHz Synchronous Buck Regulator

Figure 7-4 shows the schematic diagram of a single-output synchronous buck regulator with an output voltage of 5V and a rated load current of 8A. In this example, the current limit is monitored across the DCR of the output inductor. The switching frequency is set at 2.2MHz by resistor R_T pulled up to VCC to enable spread spectrum. The 5V output voltage is set with FB connected to VCC with a 24.9kΩ resistor. An output voltage of 3.3V is also feasible simply by connecting FB to VCC.

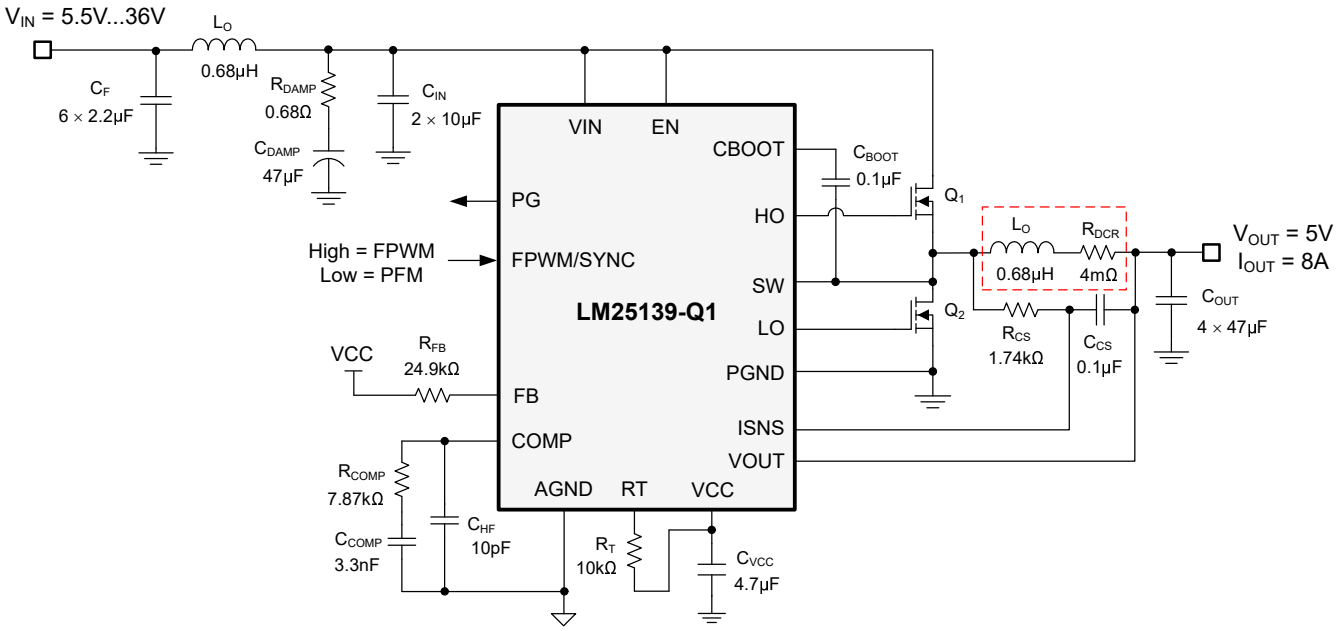


Figure 7-4. Application Circuit 1 With the LM25139-Q1 Buck Regulator at 2.2MHz

Note

This and subsequent design examples are provided herein to showcase the LM25139-Q1 controller in several different applications. Depending on the source impedance of the input supply bus, an electrolytic capacitor can be required at the input to provide stability, particularly at low input voltage and high output current operating conditions. See also Section 7.3.

7.2.1.1 Design Requirements

The following table shows the intended input, output, and performance parameters for this design example.

Table 7-2. Design Parameters

DESIGN PARAMETER	VALUE
Input voltage range (steady-state)	8V to 18V
Minimum input voltage	5.5V
Maximum input voltage	36V
Output voltage	5V
Output current	8A
Switching frequency	2.2MHz
Output voltage regulation	±1%
Soft-start time	3ms

The switching frequency is set at 2.2MHz by resistor R_T. In terms of control loop performance, the target loop crossover frequency is 55kHz with a phase margin greater than 50°.

Table 7-3 cites the selected buck regulator powertrain components, and many of the components are available from multiple vendors. The MOSFETs in particular are chosen for both lowest conduction and switching power loss, as discussed in detail in Section 7.1.1.4. This design uses a low-DCR metal-powder composite inductor and ceramic output capacitor implementation.

Table 7-3. List of Materials for Application Circuit 1

REFERENCE DESIGNATOR	QTY	SPECIFICATION	MANUFACTURER	PART NUMBER
C_{IN}	2	10µF, 50V, X7R, 1210, ceramic	AVX	12105C106K4Z2A
C_O	4	47µF, 10V, X7R, 1210, ceramic	Murata	GRM32ER71A476KE15L
L_O	1	0.68µH, 4mΩ, 26A, 6.6 × 6.6 × 5.8mm	Würth Elektronik	744373490068
Q_1, Q_2	2	40V, 4.6mΩ, 7 nC, SON 5 × 6	Infineon	IAUC60N04S6L039
U_1	1	LM25139-Q1 42V synchronous buck controller	Texas Instruments	LM25139QRGTRQ1

7.2.1.2 Detailed Design Procedure

7.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM25139-Q1 device with the WEBENCH Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

7.2.1.2.2 Buck Inductor

1. Use Equation 30 to calculate the required buck inductance based on a 30% inductor ripple current at nominal input voltages.

$$L_O = \frac{V_{OUT}}{\Delta I_{LO} \times F_{SW}} \times \left(1 - \frac{V_{OUT}}{V_{IN(nom)}}\right) = \frac{5V}{2.4A \times 2.2MHz} \times \left(1 - \frac{5V}{12V}\right) = 0.55\mu H \quad (30)$$

2. Select a standard inductor value of 0.56µH or use a 0.68µH to account for effective inductance derating. In this example, 0.68µH is chosen. Use Equation 31 to calculate the peak inductor current at maximum steady-state input voltage. Subharmonic oscillation occurs with a duty cycle greater than 50% for peak current-mode control. For design simplification, the LM25139-Q1 has an internal slope compensation ramp proportional to the switching frequency that is added to the current sense signal to damp any tendency toward subharmonic oscillation.

$$I_{LO(PK)} = I_{OUT} + \frac{\Delta I_{LO}}{2} = I_{OUT} + \frac{V_{OUT}}{2 \times L_O \times F_{SW}} \times \left(1 - \frac{V_{OUT}}{V_{IN(max)}}\right) = 8 + \frac{5V}{2 \times 0.68\mu H \times 2.2MHz} \times \left(1 - \frac{5V}{18V}\right) = 9.2A \quad (31)$$

7.2.1.2.3 Current-Sense Components

This design example senses the output current across the DCR of the inductor. When using DCR current sensing, matching the time constant of the sense network with the time constant of the inductor such that the voltage across the isense capacitor replicates the voltage across the inductor is important. Use the following steps to achieve accurate DCR sensing:

1. Use Equation 32 to calculate the sense resistor by matching the inductor time constant to the sensing time constant.

$$R_{cs} = \frac{L_O}{C_{CS} \times R_{DcR}} = \frac{0.68\mu H}{0.1\mu F \times 4m\Omega} = 1.7k\Omega \quad (32)$$

2. Use Equation 33 to calculate the current limit given the DCR of the inductor.

$$I_{CL} = \frac{V_{CS-TH}}{R_{DCR}} = \frac{60mV}{4m\Omega} = 15A \quad (33)$$

where

- V_{CS-TH} is the 60mV current limit threshold.

3. Place the sense resistor and capacitor close to the inductor.
4. Use Kelvin-sense connections, and route the sense lines differentially from the sense network to the LM25139-Q1.

5. The CS-to-output propagation delay (related to the current limit comparator, internal logic, and power MOSFET gate drivers) causes the peak current to increase above the calculated current limit threshold. For a total propagation delay $t_{DELAY-ISNS}$ of 70ns, use Equation 34 to calculate the worst-case peak inductor current with the output shorted.

$$I_{LO-PK(SC)} = \frac{V_{CS-TH}}{R_{DCR}} + \frac{V_{IN(max)} \times t_{DELAY-ISNS}}{L_O} = \frac{60mV}{4m\Omega} + \frac{18V \times 70ns}{0.68\mu H} = 16.8A \quad (34)$$

6. Based on the result, choose an inductor with a saturation current of 18A or greater across the full operating temperature range.

The DCR current sense configuration is dependent on the inductor DCR, therefore, choosing an inductor with DCR characteristics which align with the desired current limit of the application is important. The saturation current of the inductor also must be greater than the expected current limit.

When using a series sense resistor, use the following procedure instead:

1. Calculate the current-sense resistance based on a maximum peak current capability of at least 25% higher than the peak inductor current at full load to provide sufficient margin during start-up and load-on transients. Use Equation 35 to calculate the current sense resistances.

$$R_S = \frac{V_{CS-TH}}{1.25 \times I_{LO(PK)}} = \frac{60mV}{1.25 \times 9.2A} = 5.2m\Omega \quad (35)$$

2. Select a standard resistance value of 5mΩ for the shunt. An 0508 footprint component with wide aspect ratio termination design provides 1W power rating, low parasitic series inductance, and compact PCB layout. Carefully adhere to the layout guidelines in Section 7.4.1 to make sure that noise and DC errors do not corrupt the differential current-sense voltages measured at the ISNS+ and VOUT pins.
3. Place the shunt resistor close to the inductor.
4. Use Kelvin-sense connections, and route the sense lines differentially from the shunt to the LM25139-Q1.
5. The CS-to-output propagation delay (related to the current limit comparator, internal logic, and power MOSFET gate drivers) causes the peak current to increase above the calculated current limit threshold. For a total propagation delay $t_{DELAY-ISNS}$ of 70ns, use Equation 36 to calculate the worst-case peak inductor current with the output shorted.

$$I_{LO-PK(SC)} = \frac{V_{CS-TH}}{R_S} + \frac{V_{IN(max)} \times t_{DELAY-ISNS}}{L_O} = \frac{60mV}{5m\Omega} + \frac{18V \times 70ns}{0.68\mu H} = 13.8A \quad (36)$$

6. Based on this result, select an inductor with saturation current greater than 16A across the full operating temperature range.

7.2.1.2.4 Output Capacitors

1. Use Equation 37 to estimate the output capacitance required to manage the output voltage overshoot during a load-off transient (from full load to no load) assuming a load transient deviation specification of 1.5% (75mV for a 5V output).

$$C_{OUT} \geq \frac{L_O \times \Delta I_{OUT}^2}{(V_{OUT} + \Delta V_{OVERSHOOT})^2 - V_{OUT}^2} = \frac{0.68\mu H \times 8A^2}{(5V + 75mV)^2 - 5V^2} = 57.6\mu F \quad (37)$$

2. Noting the voltage coefficient of ceramic capacitors where the effective capacitance decreases significantly with applied voltage, select four 47µF, 10V, X7R, 1210 ceramic output capacitors. Generally, when sufficient capacitance is used to satisfy the load-off transient response requirement, the voltage undershoot during a no-load to full-load transient is also satisfactory.
3. Use Equation 38 to estimate the peak-peak output voltage ripple at nominal input voltage.

$$\Delta V_{OUT} = \sqrt{\left(\frac{I_{LO}}{8 \times F_{SW} \times C_{OUT}}\right)^2 + (R_{ESR} \times \Delta I_{LO})^2} = \sqrt{\left(\frac{2.4A}{8 \times 2.2MHz \times 44\mu F}\right)^2 + (1m\Omega \times 2.4A)^2} = 4mV \quad (38)$$

where

- R_{ESR} is the effective equivalent series resistance (ESR) of the output capacitors.
- 44µF is the total effective (derated) ceramic output capacitance at 5V.

4. Use Equation 39 to calculate the output capacitor RMS ripple current using and verify that the ripple current is within the capacitor ripple current rating.

$$I_{CO(RMS)} = \frac{\Delta I_{LO}}{\sqrt{12}} = \frac{2.4}{\sqrt{12}} = 0.69A \quad (39)$$

7.2.1.2.5 Input Capacitors

A power supply input typically has a relatively high source impedance at the switching frequency. Good-quality input capacitors are necessary to limit the input ripple voltage. In general, the ripple current splits between the input capacitors based on the relative impedance of the capacitors at the switching frequency.

1. Select the input capacitors with sufficient voltage and RMS ripple current ratings.
2. Use Equation 40 to calculate the input capacitor RMS ripple current assuming a worst-case duty-cycle operating point of 50%.

$$I_{CIN(RMS)} = I_{OUT} \times \sqrt{D \times (1 - D)} = 8A \times \sqrt{0.5 \times (1 - 0.5)} = 4A \quad (40)$$

3. Use Equation 41 to find the required input capacitance.

$$C_{IN} \geq \frac{D \times (1 - D) \times I_{OUT}}{F_{SW} \times (\Delta V_{IN} - R_{ESR} I_{OUT})} = \frac{0.5 \times (1 - 0.5) \times 8A}{2.2MHz \times (120mV - 2m\Omega \times 8A)} = 8.7\mu F \quad (41)$$

where

- ΔV_{IN} is the input peak-to-peak ripple voltage specification.
- R_{ESR} is the input capacitor ESR.

4. Recognizing the voltage coefficient of ceramic capacitors, select two 10µF, 50V, X7R, 1210 ceramic input capacitors. Place these capacitors adjacent to the power MOSFETs. See also Section 7.4.1.1.
5. Use four 10nF, 50V, X7R, 0603 ceramic capacitors near the high-side MOSFET to supply the high di/dt current during MOSFET switching transitions. Such capacitors offer high self-resonant frequency (SRF) and low effective impedance above 100MHz. The result is lower power loop parasitic inductance, thus minimizing switch-node voltage overshoot and ringing for lower conducted and radiated EMI signature. See also Section 7.4.1.

7.2.1.2.6 Frequency Set Resistor

Use Equation 42 to calculate the RT resistance for a switching frequency of 2.2MHz. Choose a standard E96 value of 10kΩ.

$$R_T = \frac{23759}{F_{SW(kHz)}} - 0.72 = \frac{23759}{2200kHz} - 0.72 = 10k\Omega \quad (42)$$

7.2.1.2.7 Feedback Resistors

If an output voltage setpoint other than 3.3V or 5V is required (or to measure a bode plot when using either of the fixed output voltage options), use Equation 43 to determine the feedback resistances.

$$R_{FB1} = R_{FB2} \times \left(\frac{V_{OUT}}{V_{REF}} - 1\right) = 15k\Omega \times \left(\frac{5V}{0.8V} - 1\right) = 78.7k\Omega \quad (43)$$

7.2.1.2.8 Compensation Components

Choose compensation components for a stable control loop using the procedure outlined as follows:

1. Based on a specified loop gain crossover frequency, f_C, of 55kHz, use Equation 44 to calculate R_{COMP}, assuming an effective output capacitance of 100µF. Choose a standard value for R_{COMP} of 7.87kΩ.

$$R_{COMP} = 2\pi \times f_C \times \frac{V_{OUT}}{V_{REF}} \times \frac{R_S \times G_{CS}}{g_m} \times C_{OUT} = 2\pi \times 55kHz \times \frac{5V}{0.8V} \times \frac{4m\Omega \times 10}{1100\mu S} \times 100\mu F = 7.85k\Omega \quad (44)$$

2. To provide adequate phase boost at crossover while also allowing a fast settling time during a load or line transient, select C_{COMP} to place a zero at the higher of (1) one tenth of the crossover frequency, or (2) the load pole. Use Equation 45 to calculate the C_{COMP} value. Choose a standard value for C_{COMP} of 3.3nF.

$$C_{COMP} = \frac{10}{2\pi \times f_C \times R_{COMP}} = \frac{10}{2\pi \times 55kHz \times 7.87k\Omega} = 3.68nF \quad (45)$$

   Such a low capacitance value also helps to avoid output voltage overshoot when recovering from dropout (when the input voltage is less than the output voltage setpoint and V_{COMP} is railed high).
3. Calculate C_{HF} to create a pole at the ESR zero and to attenuate high-frequency noise at COMP using Equation 46. C_{BW} is the bandwidth-limiting capacitance of the error amplifier. C_{HF} can not be significant enough to be necessary in some designs. For this design, select a standard value for C_{HF} of 10pF.

$$C_{HF} = \frac{1}{2\pi \times f_{ESR} \times R_{COMP}} - C_{BW} = \frac{1}{2\pi \times 500kHz \times 7.87k\Omega} - 31 = 9.44pF \quad (46)$$

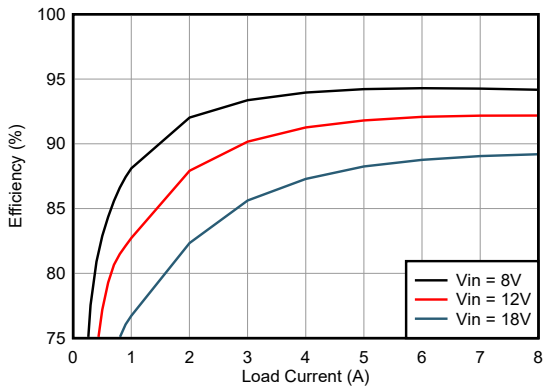
Note

Set a fast loop with high R_{COMP} and low C_{COMP} values to improve the response when recovering from operation in dropout.

Note

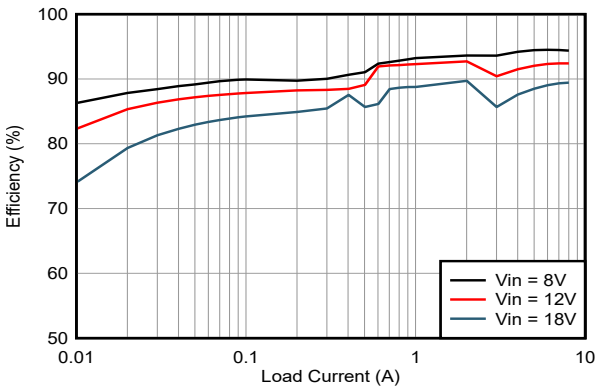
For technical designs, industry trends, and insights for designing and managing power supplies, see also TI's technical articles.

7.2.1.3 Application Curves



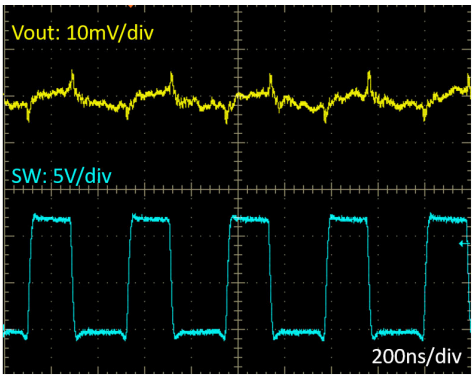
5V output

Figure 7-5. FPWM Efficiency vs I_{OUT}



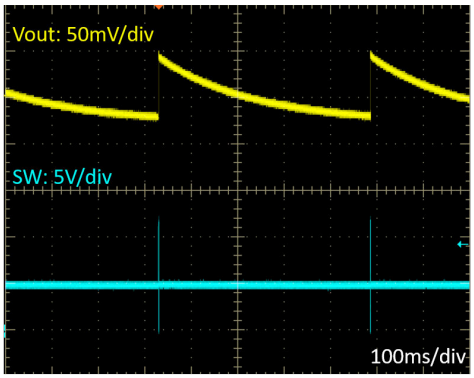
5V output

Figure 7-6. PFM Efficiency vs I_{OUT}, Log Scale



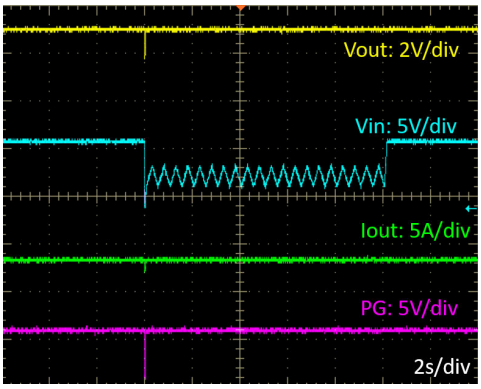
8A resistive load

Figure 7-7. Full-load Switching



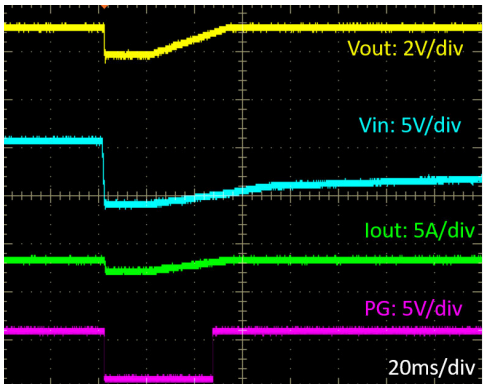
No load

Figure 7-8. PFM Switching



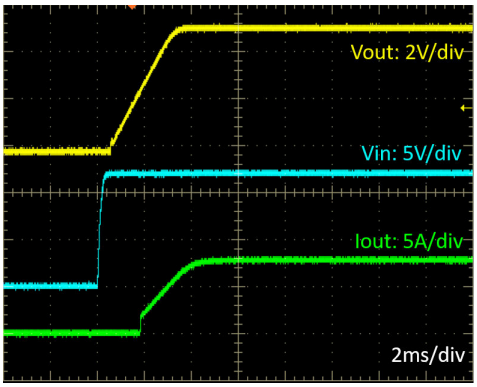
Cold Crank 5A load

Figure 7-9. Cold Crank Response



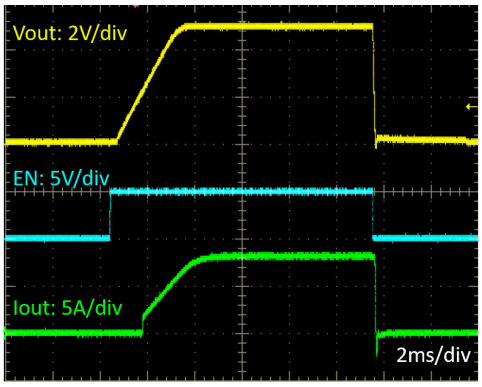
Cold Crank 5A load

Figure 7-10. Cold Crank Response at Lowest Vin



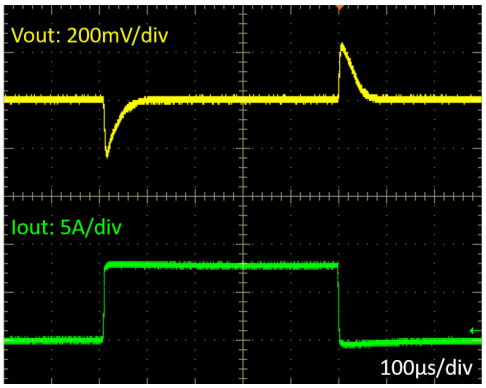
V_{IN} step to 12V 8A resistive load

Figure 7-11. Start-Up Characteristic



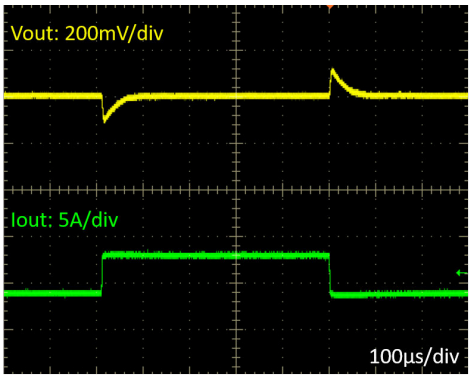
V_{IN} = 12V 8A resistive load

Figure 7-12. ENABLE ON and OFF Characteristic



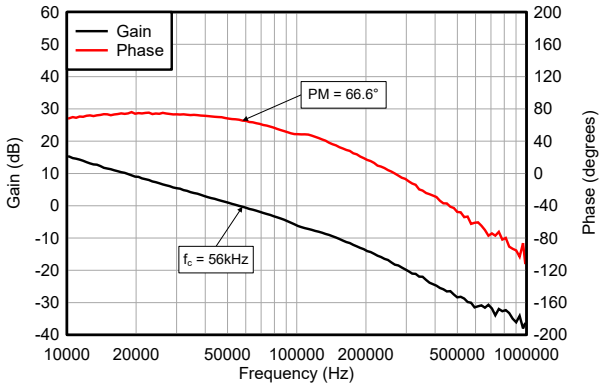
V_{IN} = 12V FPWM

Figure 7-13. Load Transient, 0A to 8A



V_{IN} = 12V FPWM

Figure 7-14. Load Transient, 4A to 8A



V_{IN} = 12V 8A resistive load

Figure 7-15. Bode Plot, 5V Output

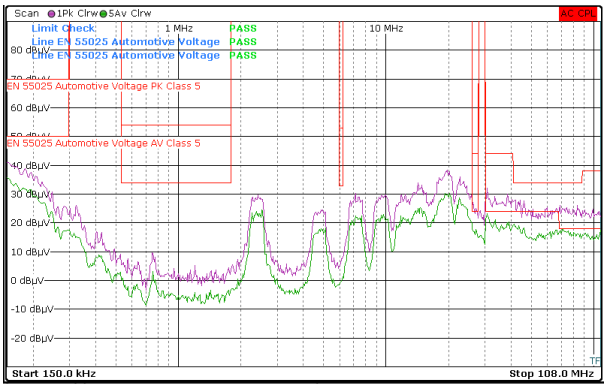


Figure 7-16. CISPR 25 Class 5 Conducted EMI

7.2.2 Design 2 – High-Efficiency, 440kHz, Synchronous Buck Regulator

The following figure shows the schematic diagram of a single-output synchronous buck regulator with an output voltage of 3.3V and a rated load current of 12A. In this example, the current is sensed using a resistor placed in series with the output inductor. The switching frequency is set at 440kHz by resistor R_T. The 3.3V output voltage is achieved by connecting FB directly to VCC.

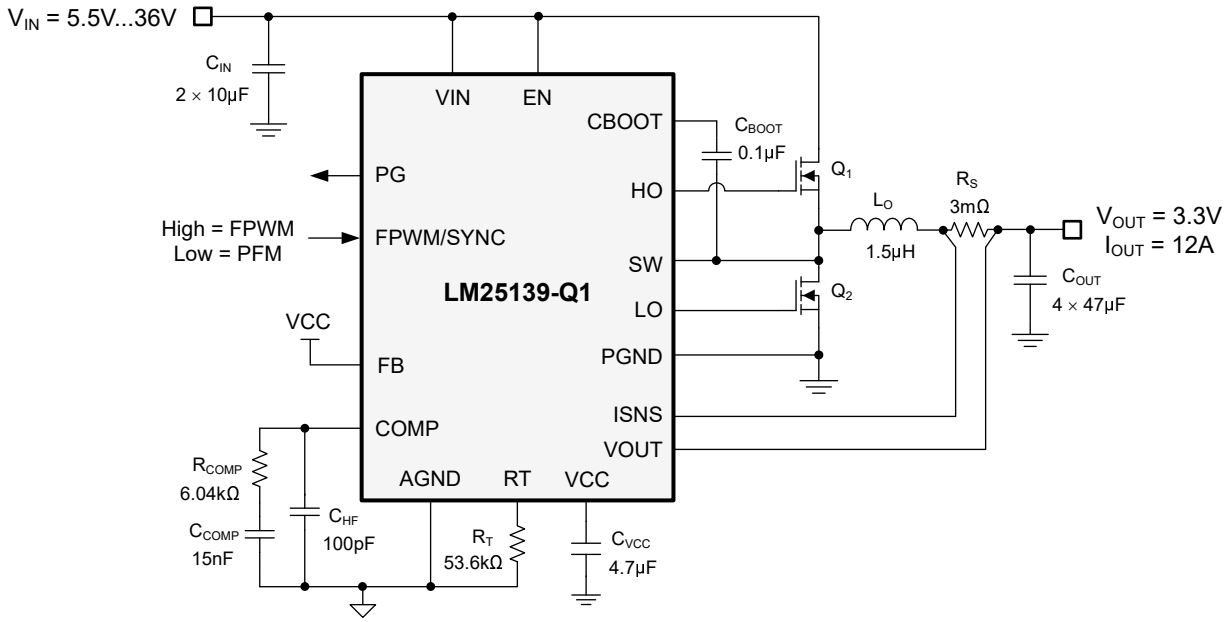


Figure 7-17. Application Circuit 2 With LM25139-Q1 Buck Regulator at 440kHz

7.2.2.1 Design Requirements

The following table shows the intended input, output, and performance parameters for this design example.

Table 7-4. Design Parameters

DESIGN PARAMETER	VALUE
Input voltage range (steady-state)	8V to 36V
Min input voltage	5.5V
Max input voltage	36V
Output voltage	3.3V
Output current	12A
Switching frequency	440kHz
Output voltage regulation	±1%
Soft-start time	3ms

The switching frequency is set at 440kHz by resistor R_T. Table 7-5 cites the selected buck regulator powertrain components, and many of the components are available from multiple vendors. The MOSFETs in particular are chosen for both lowest conduction and switching power loss, as discussed in detail in Section 7.1.1.4.

Table 7-5. List of Materials for Application Circuit 2

REFERENCE DESIGNATOR	QTY	SPECIFICATION	MANUFACTURER	PART NUMBER
C_{IN}	2	10µF, 50V, X7R, 1210, ceramic	AVX	12105C106K4Z2A
C_O	4	47µF, 10V, X7R, 1210, ceramic	Murata	GRM32ER71A476KE15L
L_O	1	1.5µH, 2.91mΩ, 32A, 8.8 × 8.3 × 7.8mm	Würth Elektronik	74439358015
R_S	1	3mΩ ±1% 1W shunt, 0508, AEC-Q200	Susumu	KRL2012E-M-R003-F-T5
Q_1, Q_2	2	40V, 4.6mΩ, 7nC, SON 5 × 6	Infineon	IAUC60N04S6L039
U_1	1	LM25139-Q1 synchronous buck controller	Texas Instruments	LM25139QRGTRQ1

7.2.2.2 Detailed Design Procedure

See Section 7.2.1.2.

7.2.2.3 Application Curves

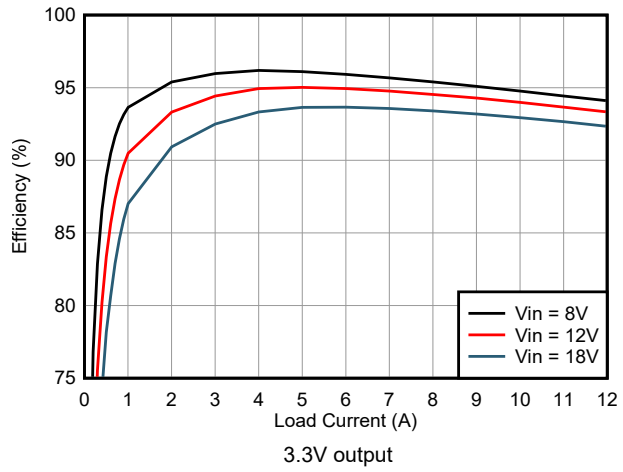


Figure 7-18. FPWM Efficiency vs I_{OUT}

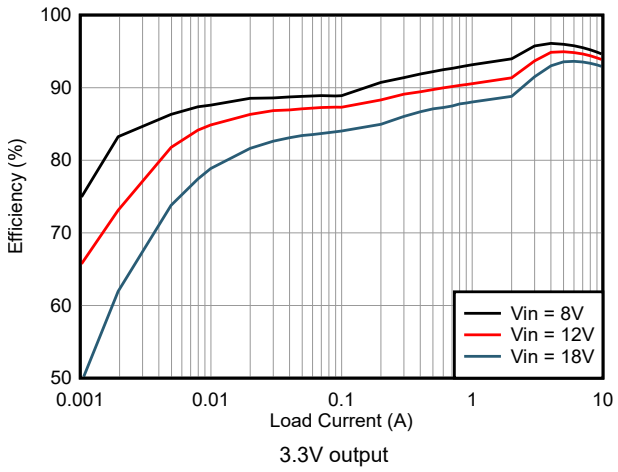


Figure 7-19. PFM Efficiency vs I_{OUT}, Log Scale

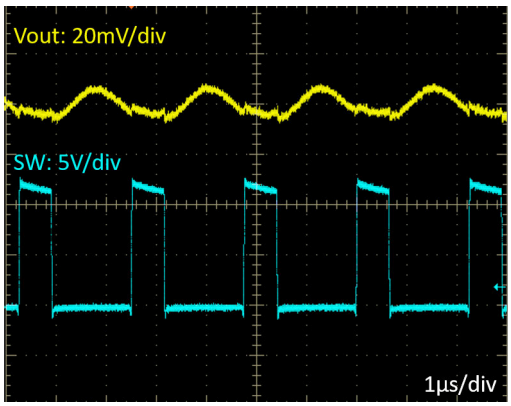


Figure 7-20. Full-load Switching

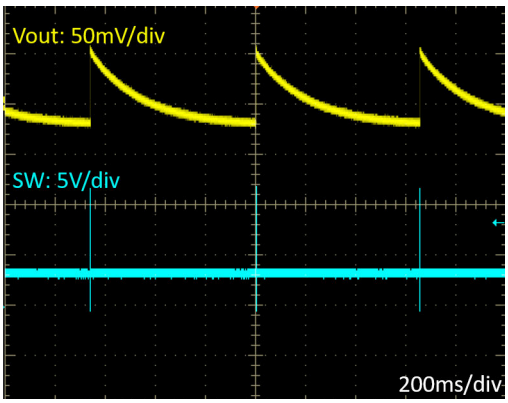


Figure 7-21. PFM Switching

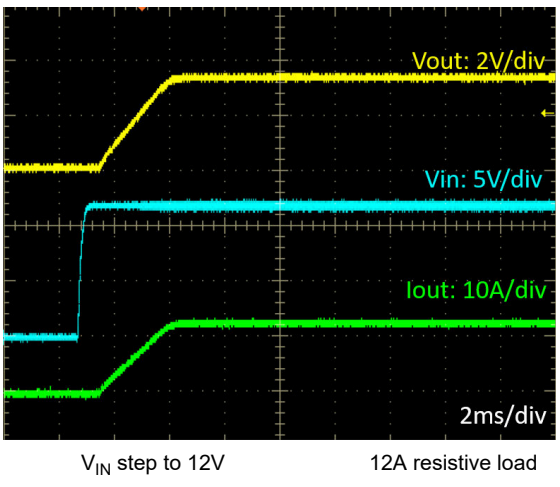


Figure 7-22. Start-Up Characteristic

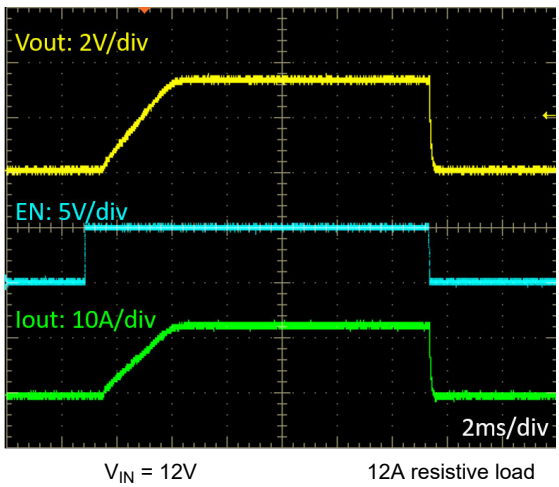


Figure 7-23. ENABLE ON and OFF Characteristic

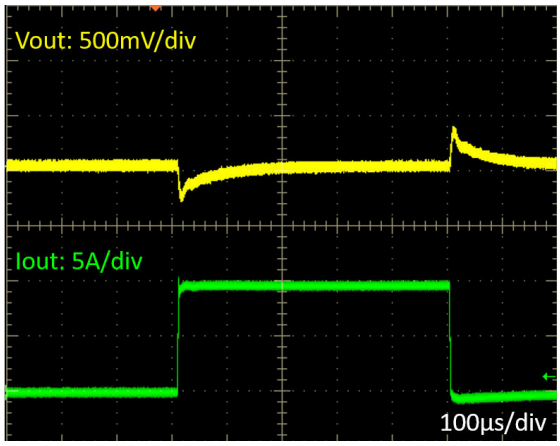


Figure 7-24. Load Transient, 0A to 10A

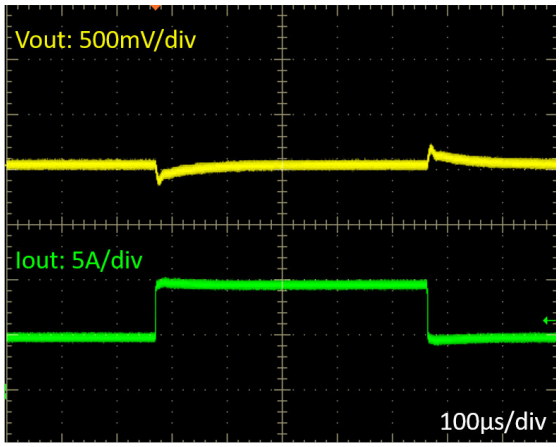


Figure 7-25. Load Transient, 5A to 10A

7.3 Power Supply Recommendations

The LM25139-Q1 buck controller is designed to operate from a wide input voltage range of 3.5V to 42V. The characteristics of the input supply must be compatible with the *Absolute Maximum Ratings* and the *Recommended Operating Conditions*. In addition, the input supply must be capable of delivering the required input current to the fully loaded regulator. Use Equation 47 to estimate the average input current.

$$I_{IN} = \frac{P_{OUT}}{V_{IN} \times \eta} \tag{47}$$

where

η is the efficiency.

If the regulator is connected to an input supply through long wires or PCB traces with a large impedance, take special care to achieve stable performance. The parasitic inductance and resistance of the input cables can have an adverse affect on converter operation. The parasitic inductance in combination with the low-ESR ceramic input capacitors form an underdamped resonant circuit. This circuit can cause overvoltage transients at VIN each time the input supply is cycled ON and OFF. The parasitic resistance causes the input voltage to dip during a load transient. The best way to solve such issues is to reduce the distance from the input supply to the regulator and use an aluminum or polymer input capacitor in parallel with the ceramics. The moderate ESR of the electrolytic capacitors helps damp the input resonant circuit and reduce any voltage overshoots. A capacitance in the range of 10µF to 47µF is usually sufficient to provide parallel input damping and helps to hold the input voltage steady during large load transients.

An EMI input filter is often used in front of the regulator that, unless carefully designed, can lead to instability as well as some of the effects mentioned above. The *AN-2162 Simple Success With Conducted EMI From DCDC Converters* application note provides helpful suggestions when designing an input filter for any switching regulator.

7.4 Layout

7.4.1 Layout Guidelines

Proper PCB design and layout is important in a high-current, fast-switching circuit (with high current and voltage slew rates) to achieve a robust and reliable design. As expected, certain issues must be considered before designing a PCB layout using the LM25139-Q1. The high-frequency power loop of a buck regulator power stage is denoted by loop 1 in the shaded area of Figure 7-26. The topological architecture of a buck regulator means that particularly high di/dt current flows in the components of loop 1, and reducing the parasitic inductance of this loop by minimizing the effective loop area becomes mandatory. Also important are the gate drive loops of the high-side and low-side MOSFETs, denoted by 2 and 3, respectively, in Figure 7-26.

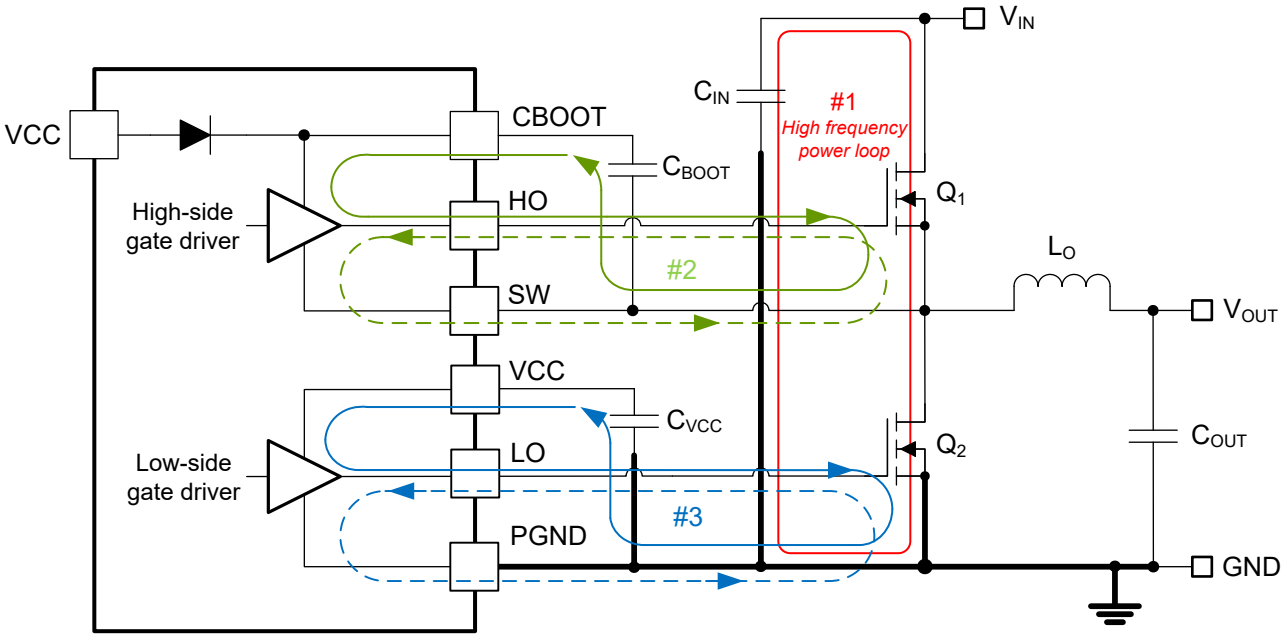


Figure 7-26. DC/DC Regulator Ground System With Power Stage and Gate Drive Circuit Switching Loops

7.4.1.1 Power Stage Layout

1. Input capacitors, output capacitors, and MOSFETs are the constituent components of the power stage of a buck regulator and are typically placed on the top side of the PCB (solder side). The benefits of convective heat transfer are maximized because of leveraging any system-level airflow. In a two-sided PCB layout, small-signal components are typically placed on the bottom side (component side). Insert at least one inner plane, connected to ground, to shield and isolate the small-signal traces from noisy power traces and lines.
2. The DC/DC regulator has several high-current loops. Minimize the area of these loops to suppress generated switching noise and optimize switching performance.
   - Loop 1: the most important loop area to minimize is the path from the input capacitor or capacitors through the high- and low-side MOSFETs, and back to the capacitor or capacitors through the ground connection. Connect the input capacitor or capacitors negative terminal close to the source of the low-side MOSFET (at ground). Similarly, connect the input capacitor or capacitors positive terminal close to the drain of the high-side MOSFET (at VIN). Refer to loop 1 of Figure 7-26.
   - Another loop, not as critical as loop 1, is the path from the low-side MOSFET through the inductor and output capacitor or capacitors, and back to source of the low-side MOSFET through ground. Connect the source of the low-side MOSFET and negative terminal of the output capacitor or capacitors at ground as close as possible.
3. The PCB trace defined as SW node, which connects to the source of the high-side (control) MOSFET, the drain of the low-side (synchronous) MOSFET and the high-voltage side of the inductor, must be short and wide. However, the SW connection is a source of injected EMI and thus must not be too large.

4. Follow any layout considerations of the MOSFETs as recommended by the MOSFET manufacturer, including pad geometry and solder paste stencil design.
5. The SW pin connects to the switch node of the power conversion stage and acts as the return path for the high-side gate driver. The parasitic inductance inherent to loop 1 in Figure 7-26 and the output capacitance (C_{OSS}) of both power MOSFETs form a resonant circuit that induces high frequency (greater than 50MHz) ringing at the SW node. The voltage peak of this ringing, if not controlled, can be significantly higher than the input voltage. Make sure that the peak ringing amplitude does not exceed the absolute maximum rating limit for the SW pin. In many cases, a series resistor and capacitor snubber network connected from the SW node to GND damps the ringing and decreases the peak amplitude. Provide provisions for snubber network components in the PCB layout. If testing reveals that the ringing amplitude at the SW pin is excessive, then include snubber components as needed.

7.4.1.2 Gate Drive Layout

The LM25139-Q1 high-side and low-side gate drivers incorporate short propagation delays, adaptive dead time control, and low-impedance output stages capable of delivering large peak currents with very fast rise and fall times to facilitate rapid turn-on and turn-off transitions of the power MOSFETs. Very high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled.

Minimization of stray or parasitic gate loop inductance is key to optimizing gate drive switching performance, whether series gate inductance resonates with MOSFET gate capacitance or common source inductance (common to gate and power loops) provides a negative feedback component opposing the gate drive command, thereby increasing MOSFET switching times. The following loops are important:

- Loop 2: high-side MOSFET, Q_1. During the high-side MOSFET turn-on, high current flows from the bootstrap (boot) capacitor through the gate driver and high-side MOSFET, and back to the negative terminal of the boot capacitor through the SW connection. Conversely, to turn off the high-side MOSFET, high current flows from the gate of the high-side MOSFET through the gate driver and SW, and back to the source of the high-side MOSFET through the SW trace. See also "loop 2" of Figure 7-26.
- Loop 3: low-side MOSFET, Q_2. During the low-side MOSFET turn-on, high current flows from the VCC decoupling capacitor through the gate driver and low-side MOSFET, and back to the negative terminal of the capacitor through ground. Conversely, to turn off the low-side MOSFET, high current flows from the gate of the low-side MOSFET through the gate driver and GND, and back to the source of the low-side MOSFET through ground. See also "loop 3" of Figure 7-26.

TI strongly recommends following circuit layout guidelines when designing with high-speed MOSFET gate drive circuits.

- Connections from gate driver outputs, HO and LO, to the respective gates of the high-side or low-side MOSFETs must be as short as possible to reduce series parasitic inductance. Be aware that peak gate drive currents can be as high as 3A. Use 0.65mm (25mils) or wider traces. Use via or vias, if necessary, of at least 0.5mm (20mils) diameter along these traces. Route the HO, SW gate traces as differential pairs from the LM25139-Q1 to the applicable high-side MOSFETs, taking advantage of flux cancellation.
- Minimize the current loop path from the VCC and CBOOT pins through the respective capacitors as these provide the high instantaneous current, up to 3A, to charge the MOSFET gate capacitance. Specifically, locate the bootstrap capacitor, C_{BOOT}, close to the respective CBOOT, SW pin pair of the LM25139-Q1 to minimize the areas of "loop 2" associated with the high-side drivers. Similarly, locate the VCC capacitor, C_{VCC}, close to the VCC and PGND pins of the LM25139-Q1 to minimize the areas of "loop 3" associated with the low-side drivers.

7.4.1.3 PWM Controller Layout

With the provision to locate the controller as close as possible to the power MOSFETs to minimize gate driver trace runs, the components related to the analog and feedback signals as well as current sensing are considered in the following:

- Separate power and signal traces, and use a ground plane to provide noise shielding.
- Place all sensitive analog traces and components related to COMP, FB, ISNS+, and RT away from high-voltage switching nodes such as SW, HO, LO, or CBOOT to avoid mutual coupling. Use internal layer or

layers as ground plane or planes. Pay particular attention to shielding the feedback (FB) and current sense (ISNS+ and VOUT) traces from power traces and components.
- Locate the upper and lower feedback resistors (if required) close to the FB pin, keeping the FB trace as short as possible. Route the trace from the upper feedback resistor to the required output voltage sense point at the load.
- Route the ISNS+ and VOUT sense traces as differential pairs to minimize noise pickup and use Kelvin connections to the applicable shunt resistor (if shunt current sensing is used) or to the sense capacitor (if inductor DCR current sensing is used).
- Minimize the loop area from the VCC and VIN pins through the respective decoupling capacitors to the PGND pin. Locate these capacitors as close as possible to the LM25139-Q1.

7.4.1.4 Thermal Design and Layout

The useful operating temperature range of a PWM controller with integrated gate drivers and bias supply LDO regulator is greatly affected by the following:

- Average gate drive current requirements of the power MOSFETs
- Switching frequency
- Operating input voltage (affecting bias regulator LDO voltage drop and hence the power dissipation)
- Thermal characteristics of the package and operating environment

For a PWM controller to be useful over a particular temperature range, the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The LM25139-Q1 controller is available in a small, 3mm × 3mm 16-pin RGT PowerPAD™ integrated circuit package to cover a range of application requirements. Section 7.4.1.4 summarizes the thermal metrics of this package.

The 16-pin RGT package offers a means of removing heat from the semiconductor die through the exposed thermal pad at the base of the package. While the exposed pad of the package is not directly connected to any leads of the package, the exposed pad of the package is thermally connected to the substrate of the LM25139-Q1 device (ground). This connection allows a significant improvement in heat sinking, and the PCB designed with thermal lands, thermal vias, and a ground plane to complete the heat removal subsystem becomes imperative. The exposed pad of the LM25139-Q1 is soldered to the ground-connected copper land on the PCB directly underneath the device package, reducing the thermal resistance to a very low value.

Numerous vias with a 0.3mm diameter connected from the thermal land to the internal and solder-side ground plane or planes are vital to help dissipation. In a multi-layer PCB design, a solid ground plane is typically placed on the PCB layer below the power components. Not only does this action provide a plane for the power stage currents to flow but this action also represents a thermally conductive path away from the heat generating devices.

The thermal characteristics of the MOSFETs also are significant. The drain pads of the high-side MOSFETs are normally connected to a VIN plane for heat sinking. The drain pads of the low-side MOSFETs are tied to the SW plane, but the SW plane area is purposely kept as small as possible to mitigate EMI concerns.

7.4.1.5 Ground Plane Design

As mentioned previously, TI recommends using one or more of the inner PCB layers as a solid ground plane. A ground plane offers shielding for sensitive circuits and traces and also provides a quiet reference potential for the control circuitry. In particular, a full ground plane on the layer directly underneath the power stage components is essential. Connect the source terminal of the low-side MOSFET and return terminals of the input and output capacitors to this ground plane. Connect the PGND and AGND pins of the controller at the DAP and then connect to the system ground plane using an array of vias under the DAP. The PGND nets contain noise at the switching frequency and can bounce because of load current variations. The power traces for PGND, VIN, and SW can be restricted to one side of the ground plane, for example on the top layer. The other side of the ground plane contains much less noise and is an excellent choice for sensitive analog trace routes.

7.4.2 Layout Example

Figure 7-27 shows a single-sided layout of a synchronous buck regulator with discrete power MOSFETs, Q1 and Q2, in SON 5mm × 6mm case size. The power stage is surrounded by a GND pad geometry to connect an EMI shield if needed. The design uses layer 2 of the PCB as a power-loop return path directly underneath the top layer to create a low-area switching power loop of approximately 2mm². This loop area, and hence parasitic inductance, must be as small as possible to minimize EMI as well as switch-node voltage overshoot and ringing.

The high-frequency power loop current flows through MOSFETs Q1 and Q2, through the power ground plane on layer 2, and back to VIN through the 0402 ceramic capacitors C14 through C19. The currents flowing in opposing directions in the vertical loop configuration provide field self-cancellation, reducing parasitic inductance. Figure 7-29 shows a side view to illustrate the concept of creating a low-profile, self-canceling loop in a multilayer PCB structure. The layer 2 GND plane layer, shown in Figure 7-28, provides a tightly-coupled current return path directly under the MOSFETs to the source terminals of Q2.

Six 10nF input capacitors with small 0402 or 0603 case size are placed in parallel very close to the drain of Q1. The low equivalent series inductance (ESL) and high self-resonant frequency (SRF) of the small footprint capacitors yield excellent high-frequency performance. The negative terminals of these capacitors are connected to the layer-2 GND plane with multiple 12mil (0.3mm) diameter vias, further minimizing parasitic loop inductance.

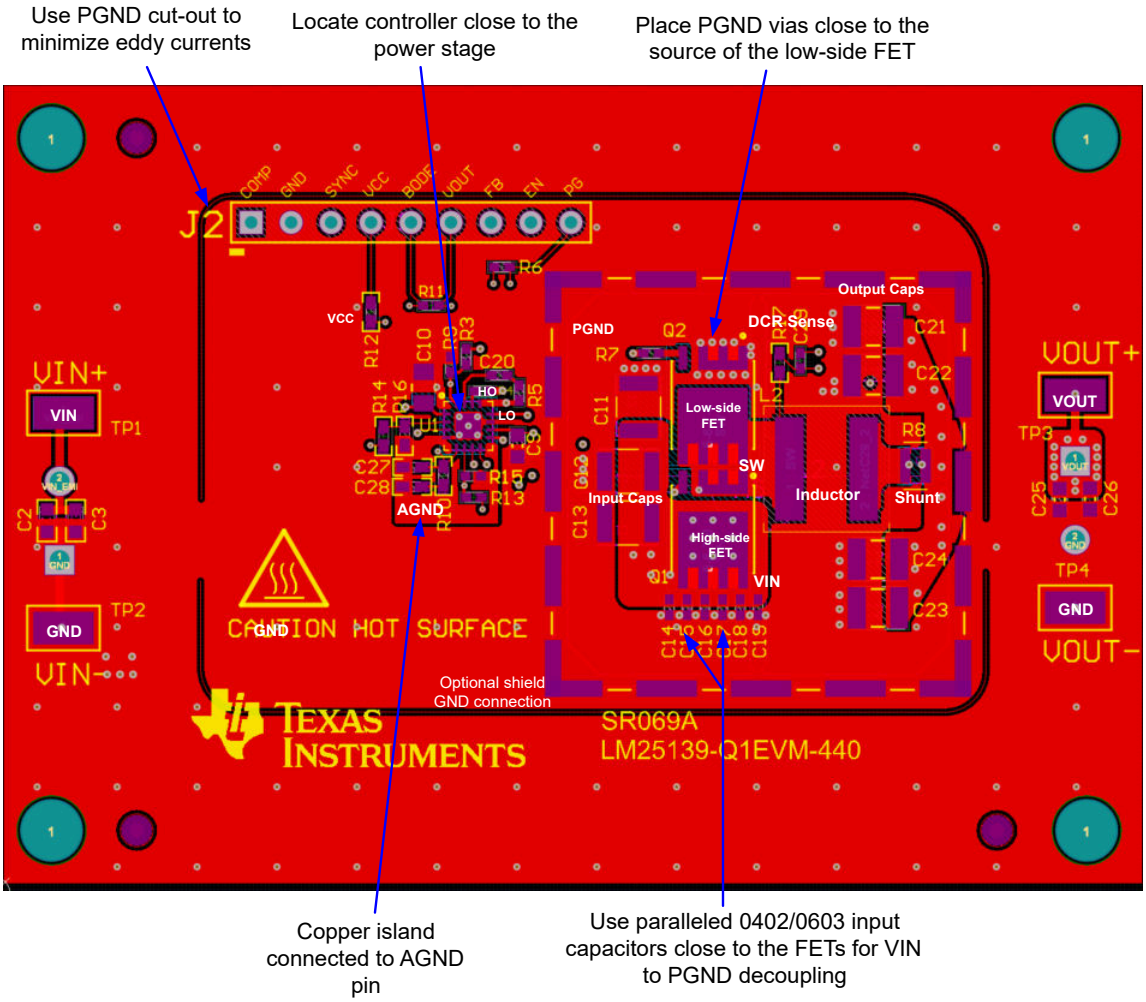


Figure 7-27. PCB Top Layer – High Density, Single-sided Design

Additional guidelines to improve noise immunity and reduce EMI are as follows:

- Make the ground connections to the LM25139-Q1 controller as shown in Figure 7-27. Create a power ground directly connected to all high-power components and an analog ground plane for sensitive analog components. The analog ground plane for AGND and power ground plane for PGND must be connected at a single point directly under the IC – at the die attach pad (DAP).
- Connect the MOSFETs (switch node) directly to the inductor terminal with short copper connections (without vias) as this net has high dv/dt and contributes to radiated EMI. The single-layer routing of the switch-node connection means that switch-node vias with high dv/dt do not appear on the bottom side of the PCB. This avoids e-field coupling to the reference ground plane during the EMI test. VIN and PGND plane copper pours shield the polygon connecting the MOSFETs to the inductor terminal, further reducing the radiated EMI signature.
- Place the *EMI filter* components on the bottom side of the PCB so that the components are shielded from the power stage components on the top side.

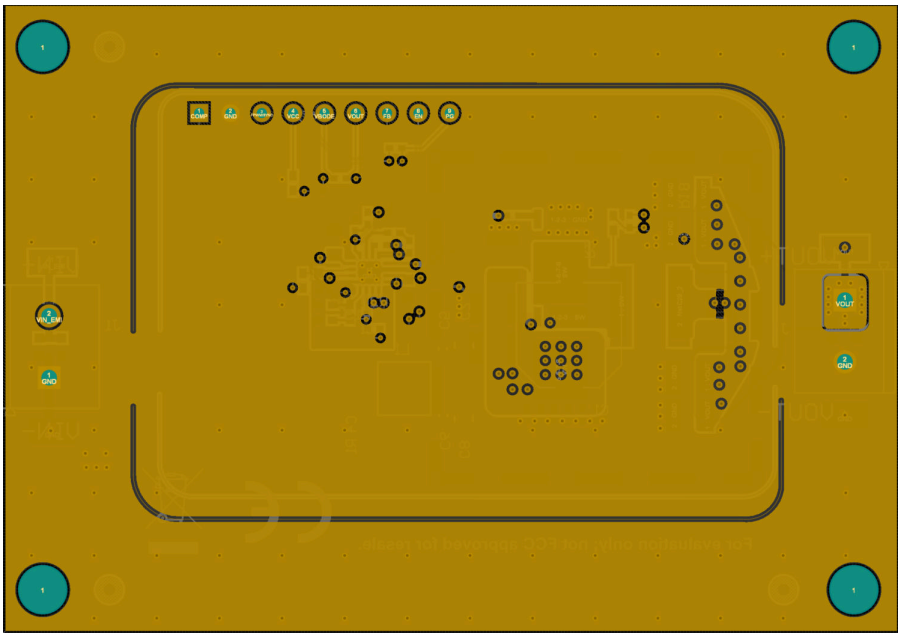
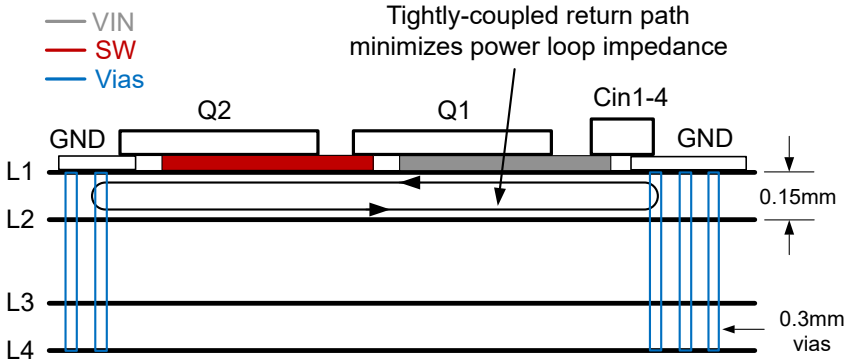


Figure 7-28. Layer 2 Full Ground Plane Directly Under the Power Components



See also *Improve High-Current DC/DC Regulator EMI Performance for Free With Optimized Power Stage Layout* application brief

Figure 7-29. PCB Stack-Up Diagram With Low L1-L2 Intra-layer Spacing

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

With an input operating voltage as low as 3.5V and up to 100V as specified in Table 8-1, the LM(2)514x/-Q1 family of synchronous buck controllers from TI provides flexibility, scalability and optimized design size for a range of applications. These controllers enable DC/DC designs with high density, low EMI and increased flexibility. Available EMI mitigation features include dual-random spread spectrum (DRSS) or triangular spread spectrum (TRSS), split gate driver outputs for slew rate (SR) control, and integrated active EMI filtering (AEF). All controllers are rated for a maximum operating junction temperature of 150°C and have AEC-Q100 grade 1 qualification.

Table 8-1. Automotive Synchronous Buck DC/DC Controller Family

DC/DC CONTROLLER	SINGLE or DUAL	V_{IN} RANGE	CONTROL METHOD	GATE DRIVE VOLTAGE	SYNC OUTPUT	KEY FEATURE
LM5137-Q1	Dual	4V to 80V	Peak current mode	5V	90° phase shift	100% duty cycle
LM5137F-Q1	Dual	4V to 80V	Peak current mode	5V	90° phase shift	ASIL B or D
LM25137-Q1	Dual	4V to 42V	Peak current mode	5V	90° phase shift	100% duty cycle
LM25137F-Q1	Dual	4V to 42V	Peak current mode	5V	90° phase shift	ASIL B or D
LM5141-Q1	Single	3.8V to 65V	Peak current mode	5V	N/A	Split gate drive
LM25141-Q1	Single	3.8V to 42V	Peak current mode	5V	N/A	Split gate drive
LM5143A-Q1	Dual	3.5V to 65V	Peak current mode	5V	90° phase shift	Split gate drive
LM25143-Q1	Dual	3.5V to 42V	Peak current mode	5V	90° phase shift	Split gate drive
LM5145-Q1	Single	5.5V to 75V	Voltage mode	7.5V	180° phase shift	No shunt
LM5146-Q1	Single	5.5V to 100V	Voltage mode	7.5V	180° phase shift	100V input capability
LM5148-Q1	Single	3.5V to 80V	Peak current mode	5V	180° phase shift	DRSS
LM25148-Q1	Single	3.5V to 42V	Peak current mode	5V	180° phase shift	DRSS
LM5149-Q1	Single	3.5V to 80V	Peak current mode	5V	180° phase shift	AEF
LM25149-Q1	Single	3.5V to 42V	Peak current mode	5V	180° phase shift	AEF
LM5190-Q1	Single	5V to 80V	Peak current mode	7.5V	N/A	CC/CV
LM25190-Q1	Single	5V to 42V	Peak current mode	7.5V	N/A	CC/CV

For development support, see the following:

- LM25139-Q1 Simulation Models
- For TI's reference design library, visit TI Designs.
- For TI's WEBENCH Design Environment, visit the WEBENCH® Design Center
- TI designs:
  - *ADAS 8-Channel Sensor Fusion Hub Reference Design with Two 4Gbps Quad Deserializers*
  - *Automotive EMI and Thermally Optimized Synchronous Buck Converter Reference Design*
  - *Automotive High Current, Wide V_{IN} Synchronous Buck Controller Reference Design Featuring LM5141-Q1*
  - *25W Automotive Start-Stop Reference Design Operating at 2.2MHz*
  - *Synchronous Buck Converter for Automotive Cluster Reference Design*
  - *137W Holdup Converter for Storage Server Reference Design*
  - *Automotive Synchronous Buck With 3.3V at 12.0A Reference Design*
  - *Automotive Synchronous Buck Reference Design*
  - *Wide Input Synchronous Buck Converter Reference Design With Frequency Spread Spectrum*
  - *Automotive Wide V_{IN} Front-end Reference Design for Digital Cockpit Processing Units*
- To view a related device of this product, see the LM25148-Q1.

8.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM25139-Q1 device with the WEBENCH Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer gives a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

- User's guides:
  - Texas Instruments, *LM5137F-Q1 12V, 20A Single-Output Evaluation Module*
  - Texas Instruments, *LM25137-Q1 Evaluation Module*
  - Texas Instruments, *LM5143-Q1 EVM User's Guide*
  - Texas Instruments, *LM5141-Q1 EVM User's Guide*
  - Texas Instruments, *LM5146-Q1 EVM User's Guide*
  - Texas Instruments, *LM5145EVM-HD-20A High Density Evaluation Module*
  - Texas Instruments, *LM5149-Q1 Buck Converter Evaluation Module User's Guide*
  - Texas Instruments, *LM5190-Q1 CC-CV Buck Controller Evaluation Module*
- Application notes:
  - Texas Instruments, *LM5143-Q1 4-phase Buck Regulator Design for Automotive ADAS Applications*
  - Texas Instruments, *Maintaining Output Voltage Regulation During Automotive Cold-Crank with LM5140-Q1 Dual Synchronous Buck Controller*

8.2.1.1 Low-EMI Design Resources

- Texas Instruments, *Low EMI* landing page
- Texas Instruments, *Tackling the EMI challenge* company blog
- Texas Instruments, *An Engineer's Guide to Low EMI in DC/DC Regulators* e-book
- Texas Instruments, *Designing a low-EMI power supply* video series
- White papers:
  - Texas Instruments, *An Overview of Conducted EMI Specifications for Power Supplies*
  - Texas Instruments, *An Overview of Radiated EMI Specifications for Power Supplies*
  - Texas Instruments, *Time-Saving and Cost-Effective Innovations for EMI Reduction in Power Supplies*
  - Texas Instruments, *Valuing Wide V_{IN}, Low EMI Synchronous Buck Circuits for Cost-driven, Demanding Applications*
- Texas Instruments, *Improve High-Current DC/DC Regulator EMI for Free With Optimized Power Stage Layout* application brief
- Texas Instruments, *Reduce Buck Converter EMI and Voltage Stress by Minimizing Inductive Parasitics* analog design journal

8.2.1.2 Thermal Design Resources

- White paper:
  - Texas Instruments, *Improving Thermal Performance in High Ambient Temperature Environments With Thermally Enhanced Packaging*
- Applications notes:
  - Texas Instruments, *Thermal Design by Insight, Not Hindsight*
  - Texas Instruments, *A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages*
  - Texas Instruments, *Semiconductor and IC Package Thermal Metrics*
  - Texas Instruments, *PowerPAD™ Thermally Enhanced Package*
  - Texas Instruments, *Using New Thermal Metrics*

8.2.1.3 PCB Layout Resources

- Applications notes:
  - Texas Instruments, *Improve High-Current DC/DC Regulator EMI Performance for Free With Optimized Power Stage Layout*
  - Texas Instruments, *AN-1149 Layout Guidelines for Switching Power Supplies*
- Seminar:
  - Texas Instruments, *Constructing Your Power Supply – Layout Considerations*

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

DATE	REVISION	NOTES
July 2025	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages show mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM25139QRGTRQ1	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	25139Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

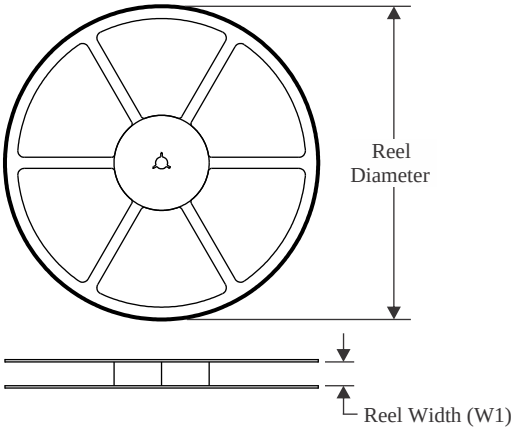
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

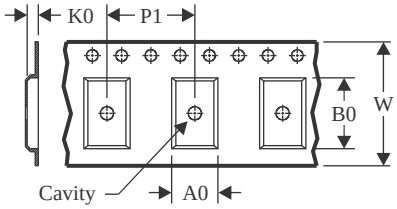
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

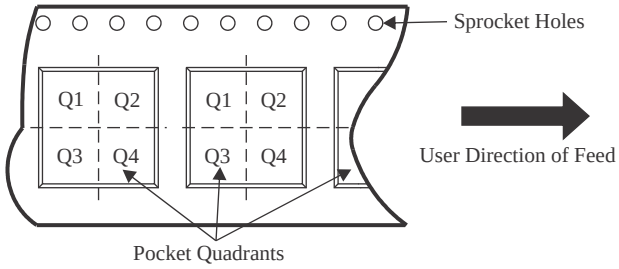


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

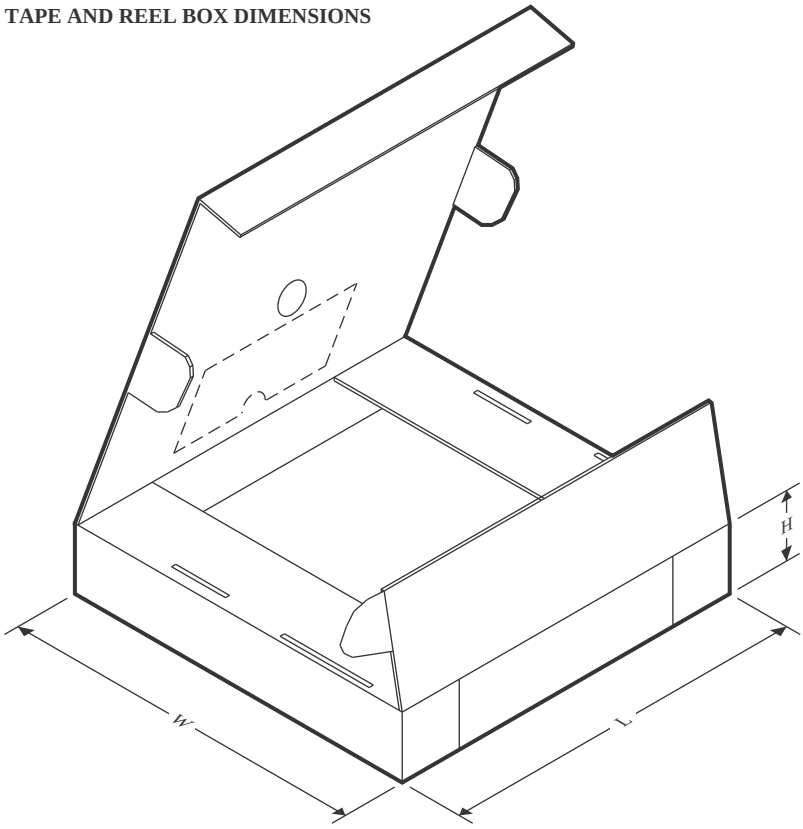
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM25139QRGTRQ1	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

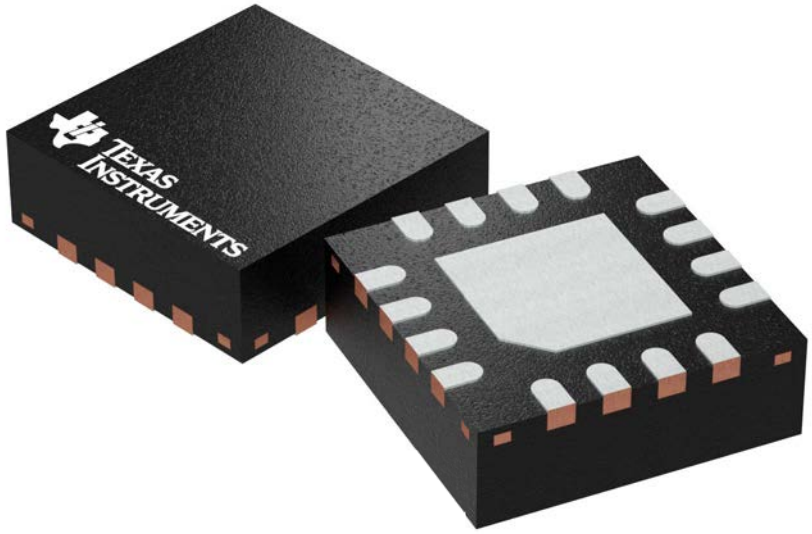


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM25139QRGTRQ1	VQFN	RGT	16	3000	367.0	367.0	35.0

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



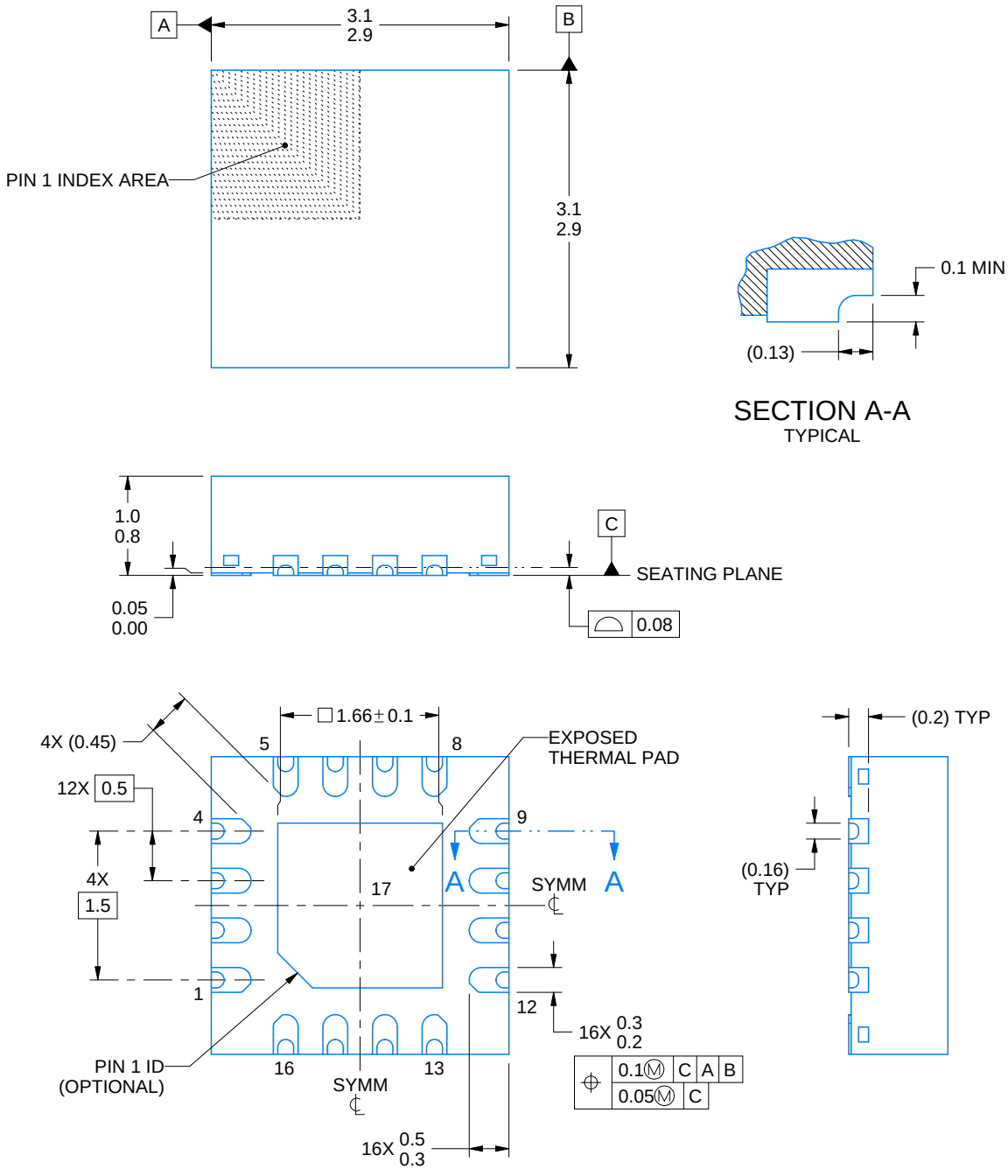
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

RGT0016K

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



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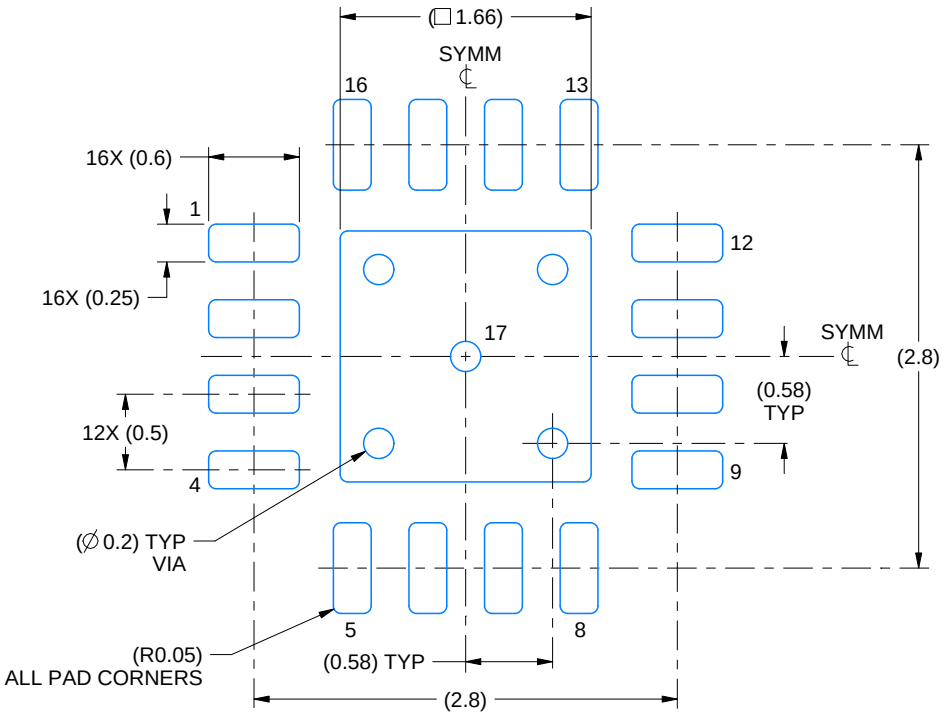
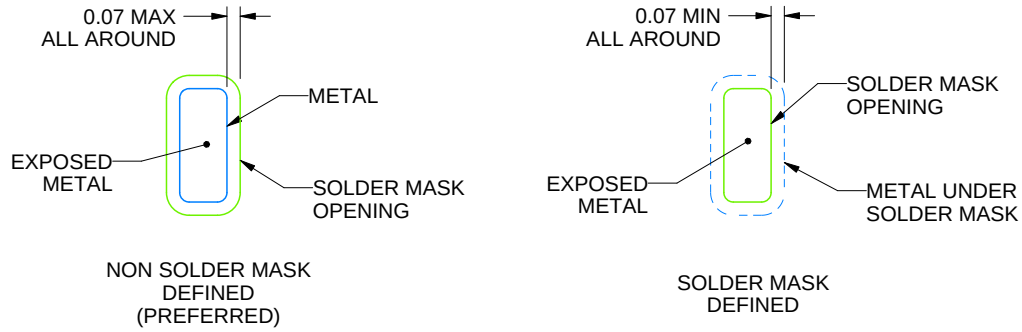
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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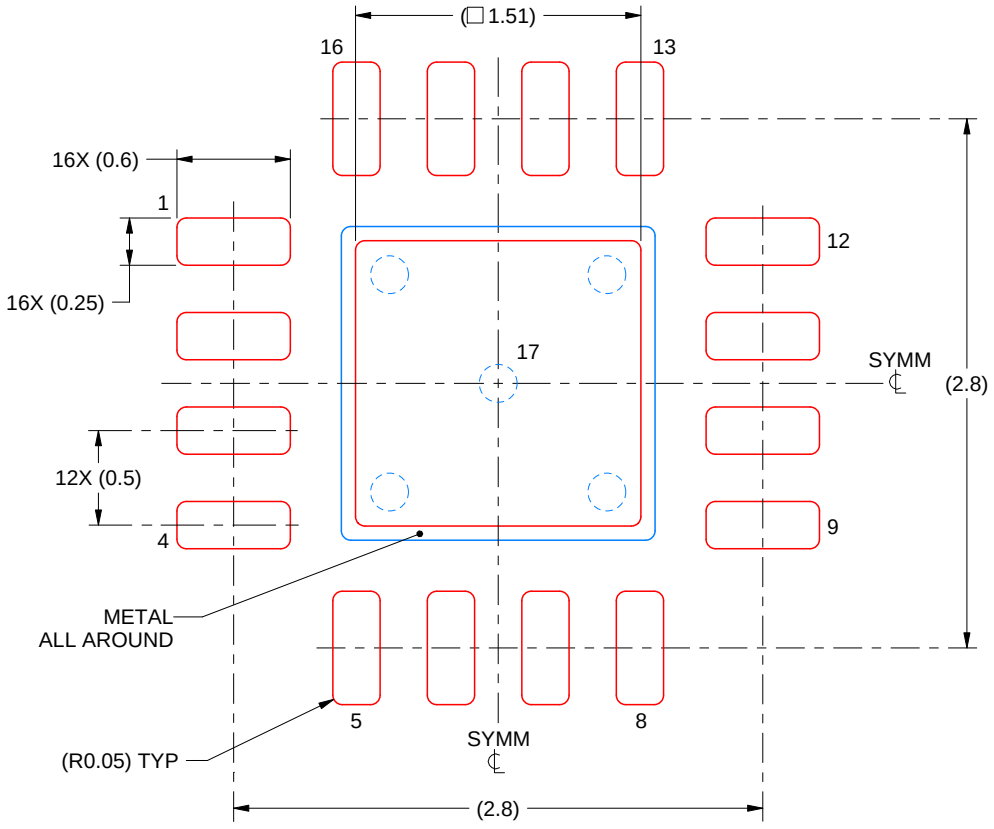
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
84% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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