SCLS513B - JULY 2003 - REVISED FEBRUARY 2008

- Qualified for Automotive Applications
- ESD Protection Exceeds 1000 V Per MIL-STD-883, Method 3015; Exceeds 100 V Using Machine Model (C = 200 pF, R = 0); Exceeds 2000 V Charged Device Model
- Single Supply or Dual Supplies
- Wide Range of Supply Voltage ... 2 V to 36 V
- Low Supply-Current Drain Independent of Supply Voltage . . . 0.8 mA Typ
- Low Input Bias Current . . . 25 nA Typ
- Low Input Offset Current . . . 5 nA Typ
- Low Input Offset Voltage . . . 2 mV Typ
- Common-Mode Input Voltage Range Includes Ground
- Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . ±36 V
- Low Output Saturation Voltage
- Output Compatible With TTL, MOS, and CMOS

D PACKAGE (TOP VIEW) 10UT [14 NOUT3 20UT 1 2 13 OUT4 V_{CC} [] з 12 GND 2IN- **1** 4 11 **∏** 4IN+ 2IN+ **1** 5 1IN- 6 1IN+ 7 8 3IN−

description/ordering information

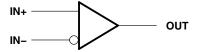
This device consists of four independent voltage comparators that are designed to operate from a single power supply over a wide range of voltages. Operation from dual supplies also is possible as long as the difference between the two supplies is 2 V to 36 V, and V_{CC} is at least 1.5 V more positive than the input common-mode voltage. Current drain is independent of the supply voltage. The outputs can be connected to other open-collector outputs to achieve wired-AND relationships.

ORDERING INFORMATION†

T _A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	SOP – D	Tape and reel	LM239AQDRQ1§	LM239AQ1

[†] For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at http://www.ti.com.

symbol (each comparator)





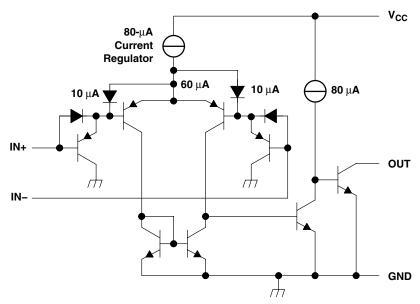
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



[‡] Package drawings, thermal data, and symbolization are available at http://www.ti.com/packaging.

[§] This package is only available taped and reeled, with standard quantities of 2500 pieces per reel.

schematic (each comparator)



All current values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V _{CC} (see Note 1)	36 V
Differential input voltage, V _{ID} (see Note 2)	
Input voltage range, V _I (either input)	
Output voltage, V _O	36 V
Output current, Io	20 mA
Duration of output short circuit to ground (see Note 3)	Unlimited
Package thermal impedance, θ _{JA} (see Note 4)	86°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Maximum operating junction temperature, T _J	136°C
Storage temperature range, T _{stq}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
 - 2. Differential voltages are at IN+ with respect to IN-.
 - 3. Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.
 - 4. The package thermal impedance is calculated in accordance with JESD 51-7.



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electrical characteristics at specified free-air temperature, $V_{CC} = 5 \text{ V}$ (unless otherwise noted)

	PARAMETER	TEST CONDIT	TIONS†	T _A ‡	MIN	TYP	MAX	UNIT	
	hand effect with an	$V_{CC} = 5 \text{ V to } 30 \text{ V, } V_{IC} =$	V _{ICR} (min),	25°C		1	2.5		
V _{IO}	Input offset voltage	$V_0 = 1.4 \text{ V}$		Full range			5.5	mV	
	hand effect account	V 44V		25°C		5	50	4	
I _{IO}	Input offset current	$V_0 = 1.4 \text{ V}$		Full range			150	nA	
	Input bigg guyyant		25°C		-25	-250	4		
I _{IB}	Input bias current	V _O = 1.4 V	Full range			-400	nA		
	0	ge range		25°C	0 to V _{CC} -1.5				
V _{ICR}	Common-mode input-voltage range			Full range	0 to V _{CC} -2			V	
A _{VD}	Large-signal differential-voltage amplification	V_{CC} = 15 V, V_{O} = 1.4 V $R_{L} \ge$ 15 k Ω to V_{CC}	V_{CC} = 15 V, V_{O} = 1.4 V to 11.4 V, $R_{L} \ge 15 \text{ k}\Omega$ to V_{CC}			200		V/mV	
	Library Laurent and American Community	V 4V	V _{OH} = 5 V	25°C		0.1	50	nA	
l _{OH}	High-level output current	V_{ID} = 1 V V_{OH} = 30 V		Full range			1	μΑ	
.,		$V_{ID} = -1 V$, $I_{OL} = 4 \text{ mA}$		25°C		150	400		
V _{OL}	Low-level output voltage			Full range			700	mV	
I _{OL}	Low-level output current	$V_{ID} = -1 V$,	V _{OL} = 1.5 V	25°C	6	16		mA	
Icc	Supply current (four comparators)	V _O = 2.5 V,	No load	25°C		8.0	2	mA	

[†] All characteristics are measured with zero common-mode input voltage, unless otherwise specified.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CON	MIN	TYP	MAX	UNIT	
Dooponoo timo	ponse time R_L connected to 5 V through 5.1 k Ω , $C_L = 15 \text{ pF}^\S$, See Note 5	100-mV input step with 5-mV overdrive		1.3		
nesponse time					0.3	

 $[\]S$ C_L includes probe and jig capacitance.

NOTE 5: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.



[‡] Full range (MIN to MAX) for LM239AQ is -40°C to 125°C. All characteristics are measured with zero common-mode input voltage, unless otherwise specified.

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
	(1)	(2)			(0)	(4)	(5)		(0)
LM239AQDRG4Q1	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM239AQ1
LM239AQDRG4Q1.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM239AQ1
LM239AQDRQ1	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM239AQ1
LM239AQDRQ1.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM239AQ1

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF LM239A-Q1:

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

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● Enhanced Product : LM239A-EP

NOTE: Qualified Version Definitions:

Catalog - TI's standard catalog product

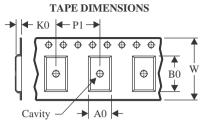
• Enhanced Product - Supports Defense, Aerospace and Medical Applications

PACKAGE MATERIALS INFORMATION

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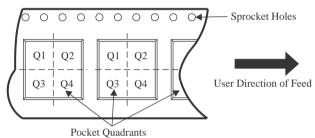
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM239AQDRG4Q1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM239AQDRQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

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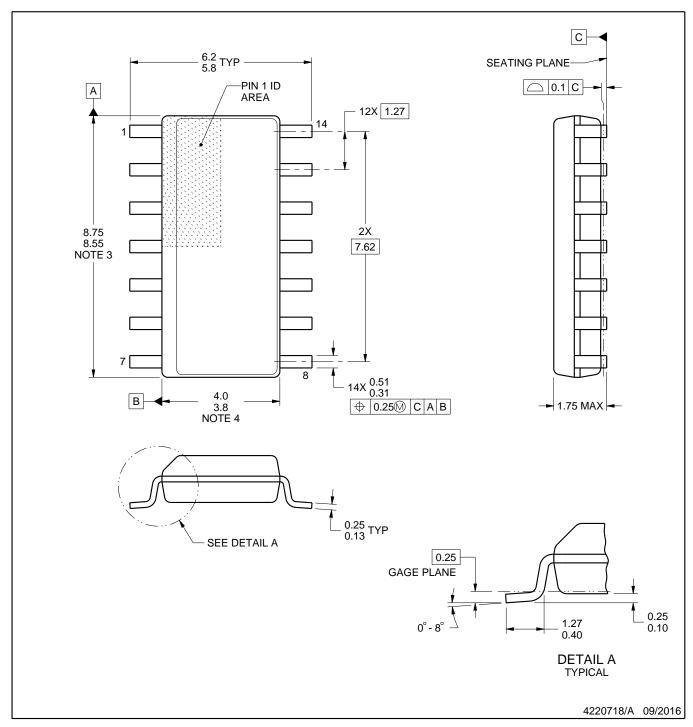


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM239AQDRG4Q1	SOIC	D	14	2500	353.0	353.0	32.0
LM239AQDRQ1	SOIC	D	14	2500	353.0	353.0	32.0



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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