LF444 Quad Low Power JFET Input Operational Amplifier

Check for Samples: LF444

FEATURES

- **¼ Supply Current of a LM148: 200 µA/Amplifier (max)**
- **Low Input Bias Current: 50 pA (max)**
- **High Gain Bandwidth: 1 MHz**
- **High Slew Rate: 1 V/µs**
- **Low Noise Voltage for Low Power 35 nV/$\sqrt{Hz}$**
- **Low Input Noise Current 0.01 pA/$\sqrt{Hz}$**
- **High Input Impedance: $10^{12}\Omega$**
- **High Gain: 50k (min)**

DESCRIPTION

The LF444 quad low power operational amplifier provides many of the same AC characteristics as the industry standard LM148 while greatly improving the DC characteristics of the LM148. The amplifier has the same bandwidth, slew rate, and gain (10 kΩ load) as the LM148 and only draws one fourth the supply current of the LM148. In addition the well matched high voltage JFET input devices of the LF444 reduce the input bias and offset currents by a factor of 10,000 over the LM148. The LF444 also has a very low equivalent input noise voltage for a low power amplifier.

The LF444 is pin compatible with the LM148 allowing an immediate 4 times reduction in power drain in many applications. The LF444 should be used wherever low power dissipation and good electrical characteristics are the major considerations.

Simplified Schematic

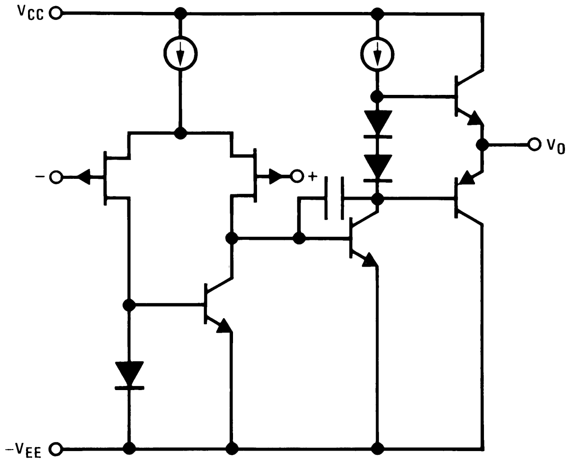


Figure 1. 1/4 Quad

Connection Diagram

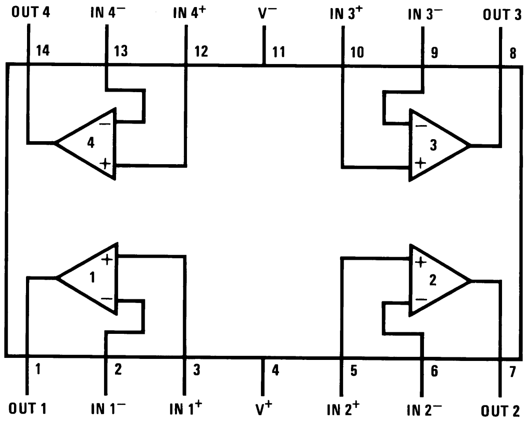


Figure 2. PDIP/SOIC Package
Top View
See Package Number NAK0014D, D0014A or NFF0014A

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)(3)

			LF444A	LF444
Supply Voltage			±22V	±18V
Differential Input Voltage			±38V	±30V
Input Voltage Range(4)			±19V	±15V
Output Short CircuitDuration(5)			Continuous	Continuous
			NAK Package	**D, NFF Packages**
Power Dissipation(6)(7)			900 mW	670 mW
T_j max			150°C	115°C
θ_{jA} (Typical)			100°C/W	85°C/W
			LF444A/LF444	
Operating Temperature Range			See(8)	
ESD Tolerance(9)			Rating to be determined	
Storage Temperature Range			$-65°C \le T_A \le 150°C$	
Soldering Information	Dual-In-Line Packages (Soldering, 10 sec.)		260°C	
	Small Outline Package	Vapor Phase (60 sec.)	215°C	
		Infrared (15 sec.)	220°C	

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) Refer to RETS444X for LF444MD military specifications.
(4) Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.
(5) Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.
(6) For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_{jA}.
(7) Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside ensured limits.
(8) The LF444A is available in both the commercial temperature range $0°C \le T_A \le 70°C$ and the military temperature range $-55°C \le T_A \le 125°C$. The LF444 is available in the commercial temperature range only. The temperature range is designated by the position just before the package type in the device number. A “C” indicates the commercial temperature range and an “M” indicates the military temperature range. The military temperature range is available in “NAK” package only.
(9) Human body model, 1.5 kΩ in series with 100 pF.

DC Electrical Characteristics (1)

Symbol	Parameter	Conditions		LF444A			LF444			Units
				Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S = 10k$, $T_A = 25°C$			2	5		3	10	mV
		$0°C \le T_A \le +70°C$				6.5			12	mV
		$-55°C \le T_A \le +125°C$				8				mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10\ k\Omega$			10			10		μV/°C
I_{OS}	Input Offset Current	$V_S = \pm 15V$(1) (2)	$T_j = 25°C$		5	25		5	50	pA
			$T_j = 70°C$			1.5			1.5	nA
			$T_j = 125°C$			10				nA
I_B	Input Bias Current	$V_S = \pm 15V$(1) (2)	$T_j = 25°C$		10	50		10	100	pA
			$T_j = 70°C$			3			3	nA
			$T_j = 125°C$			20				nA

(1) Unless otherwise specified the specifications apply over the full temperature range and for $V_S = \pm 20V$ for the LF444A and for $V_S = \pm 15V$ for the LF444. V_{OS}, I_B, and I_{OS} are measured at $V_{CM} = 0$.
(2) The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

DC Electrical Characteristics (1) (continued)

Symbol	Parameter	Conditions	LF444A			LF444			Units
			Min	Typ	Max	Min	Typ	Max	
R_{IN}	Input Resistance	T_j = 25°C		10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S = ±15V, V_O = ±10V	50	100		25	100		V/mV
		R_L = 10 kΩ, T_A = 25°C							
		Over Temperature	25			15			V/mV
V_O	Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ	±12	±13		±12	±13		V
V_{CM}	Input Common-Mode Voltage Range		±16	+18 −17		±11	+14 −12		V V
CMRR	Common-Mode Rejection Ratio	R_S ≤ 10 kΩ	80	100		70	95		dB
PSRR	Supply Voltage Rejection Ratio	See (3)	80	100		70	90		dB
I_S	Supply Current			0.6	0.8		0.6	1.0	mA

(3) Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice from ±15V to ±5V for the LF444 and from ±20V to ±5V for the LF444A.

AC Electrical Characteristics (1)

Symbol	Parameter	Conditions	LF444A			LF444			Units
			Min	Typ	Max	Min	Typ	Max	
	Amplifier-to-Amplifier Coupling			−120			−120		dB
SR	Slew Rate	V_S = ±15V, T_A = 25°C		1			1		V/μs
GBW	Gain-Bandwidth Product	V_S = ±15V, T_A = 25°C		1			1		MHz
e_n	Equivalent Input Noise Voltage	T_A = 25°C, R_S = 100Ω, f = 1 kHz		35			35		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	T_A = 25°C, f = 1 kHz		0.01			0.01		$pA/\sqrt{Hz}$

(1) Unless otherwise specified the specifications apply over the full temperature range and for V_S = ±20V for the LF444A and for V_S = ±15V for the LF444. V_{OS}, I_B, and I_{OS} are measured at V_{CM} = 0.

Typical Performance Characteristics

Input Bias Current

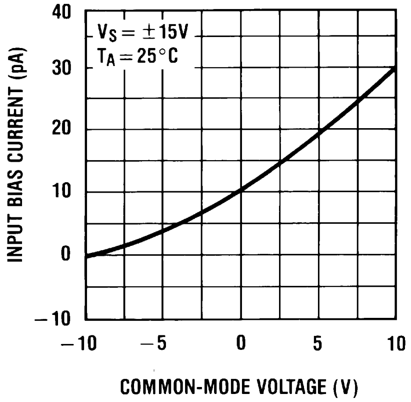


Figure 3.

Input Bias Current

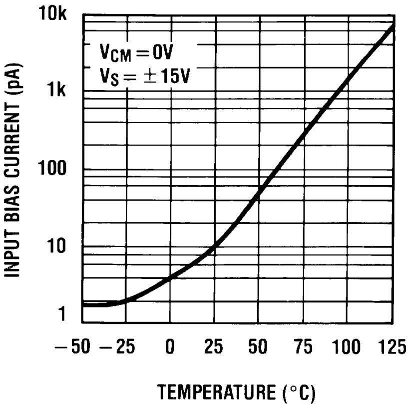


Figure 4.

Supply Current

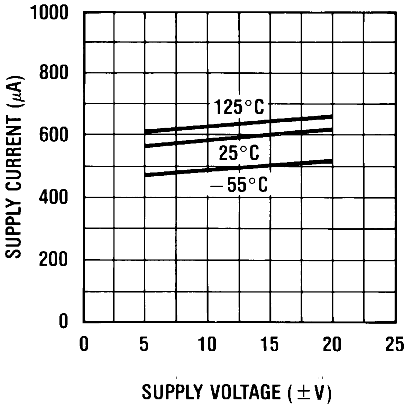


Figure 5.

Positive Common-Mode Input Voltage Limit

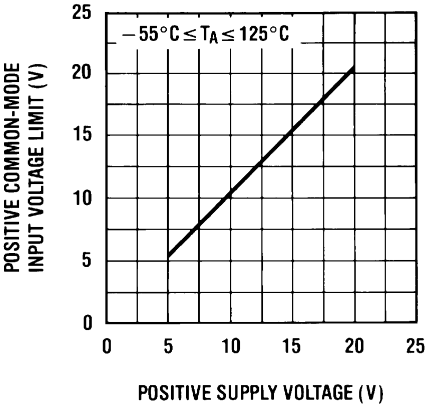


Figure 6.

Negative Common-Mode Input Voltage Limit

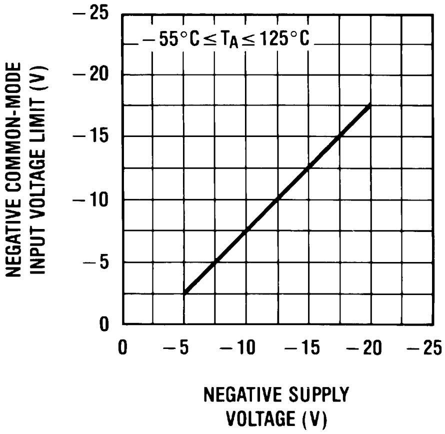


Figure 7.

Positive Current Limit

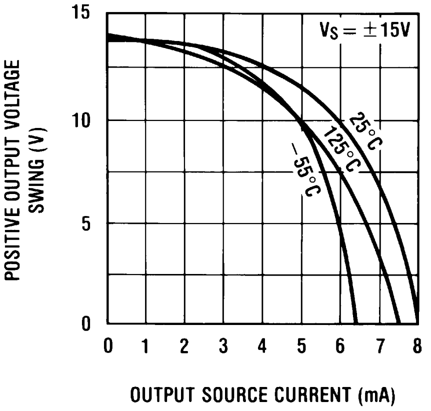


Figure 8.

Typical Performance Characteristics (continued)

Negative Current Limit

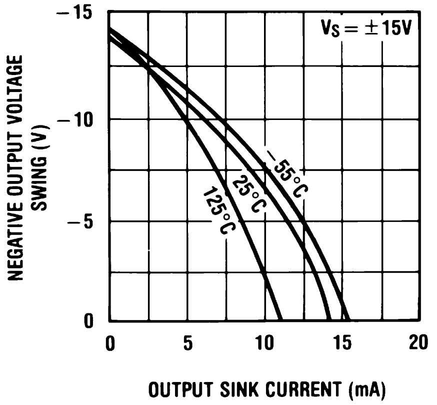


Figure 9.

Output Voltage Swing

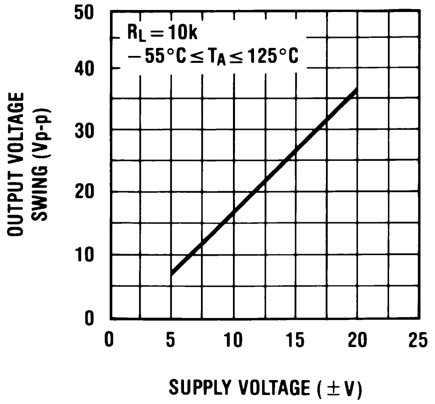


Figure 10.

Output Voltage Swing

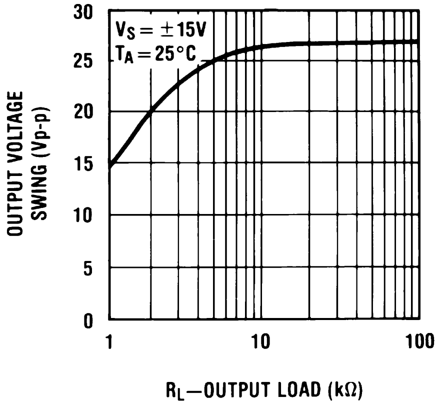


Figure 11.

Gain Bandwidth

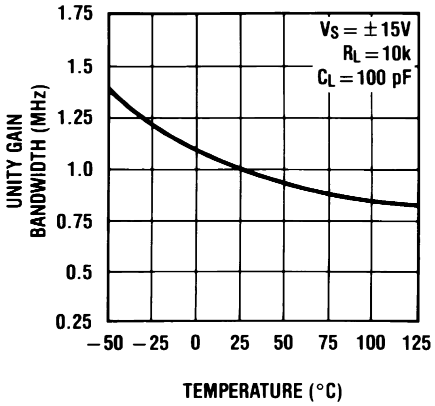


Figure 12.

Bode Plot

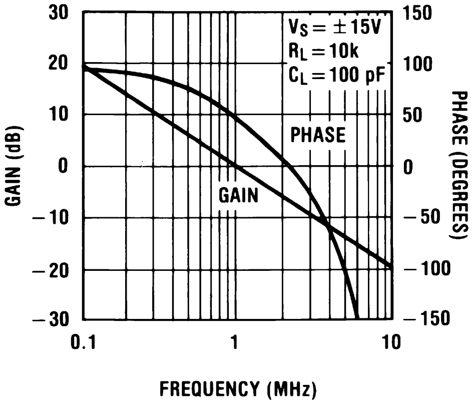


Figure 13.

Slew Rate

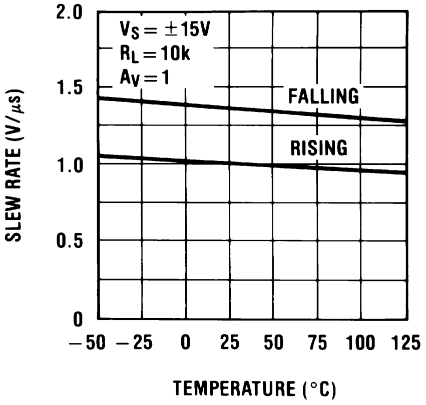


Figure 14.

Typical Performance Characteristics (continued)

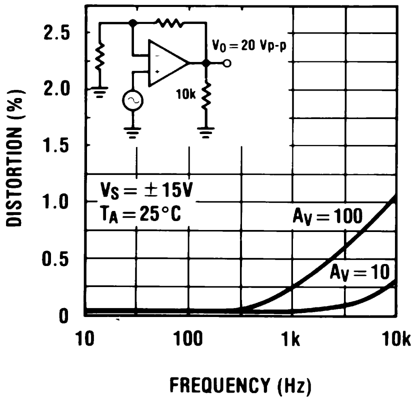

Distortion vs Frequency

Figure 15.

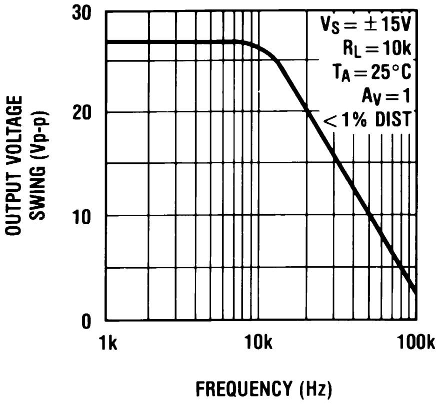

Undistorted Output Voltage Swing

Figure 16.

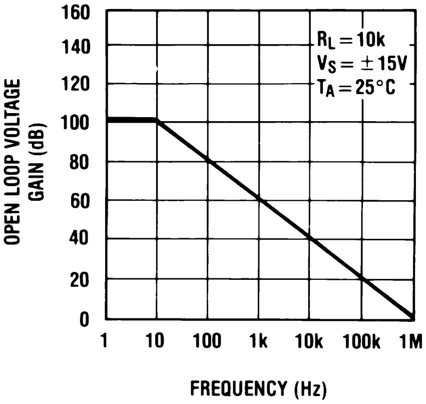

Open Loop Frequency Response

Figure 17.

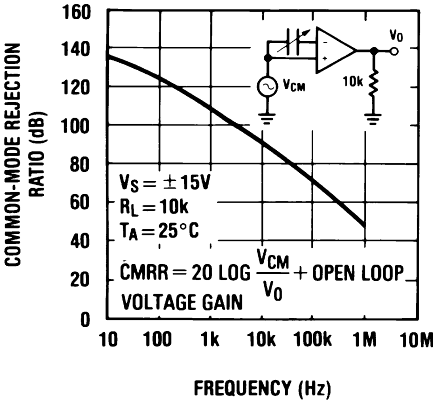

Common-Mode Rejection Ratio

Figure 18.

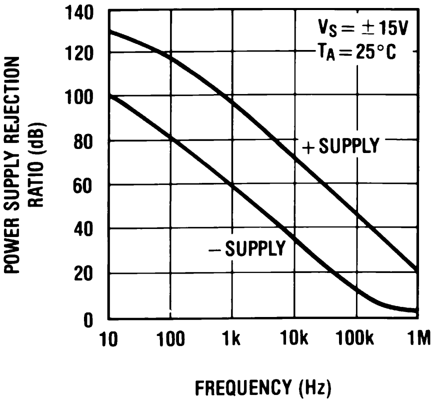

Power Supply Rejection Ratio

Figure 19.

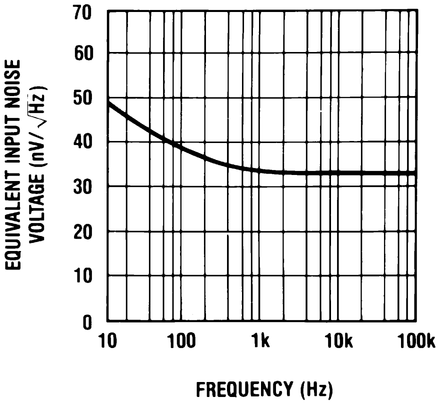

Equivalent Input Noise Voltage

Figure 20.

Typical Performance Characteristics (continued)

Open Loop Voltage Gain

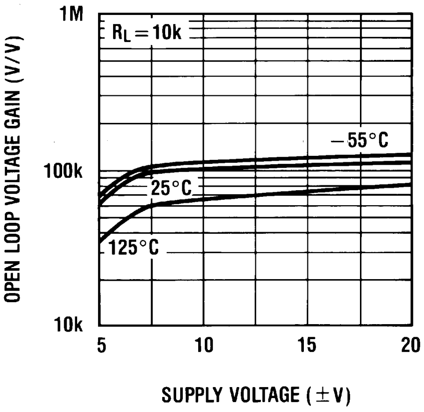


Figure 21.

Output Impedance

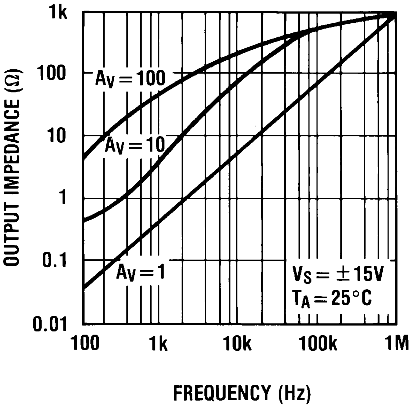


Figure 22.

Inverter Settling Time

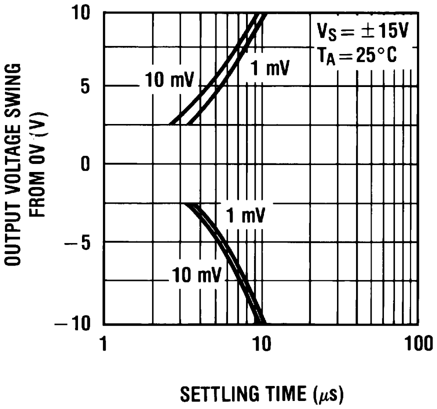


Figure 23.

Pulse Response

R_L = 10 kΩ, C_L = 10 pF

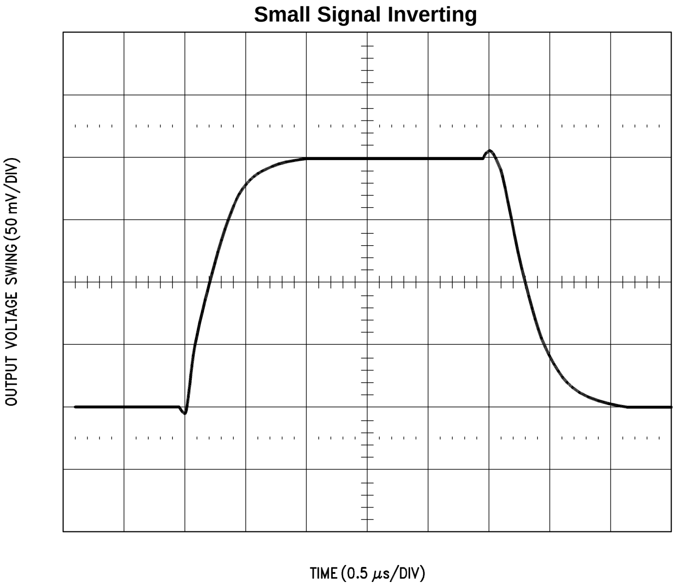


Figure 24.

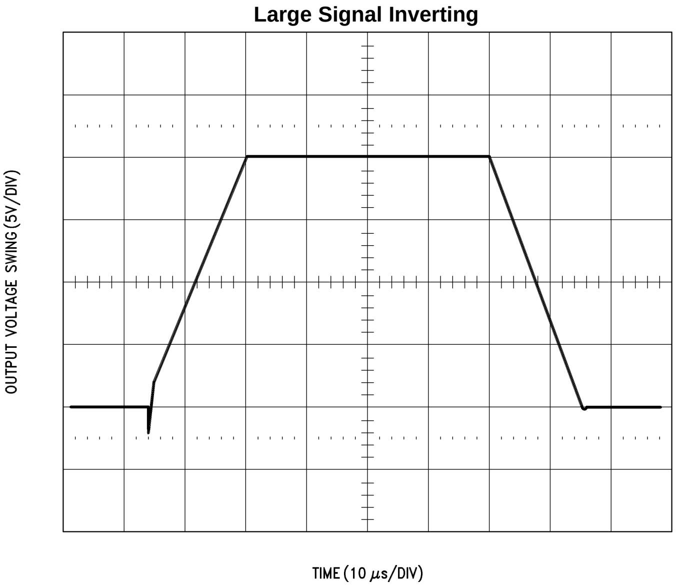


Figure 25.

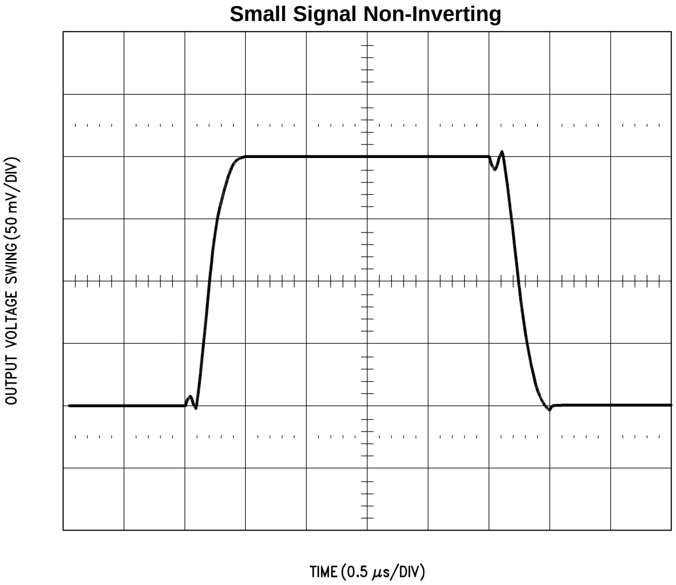


Figure 26.

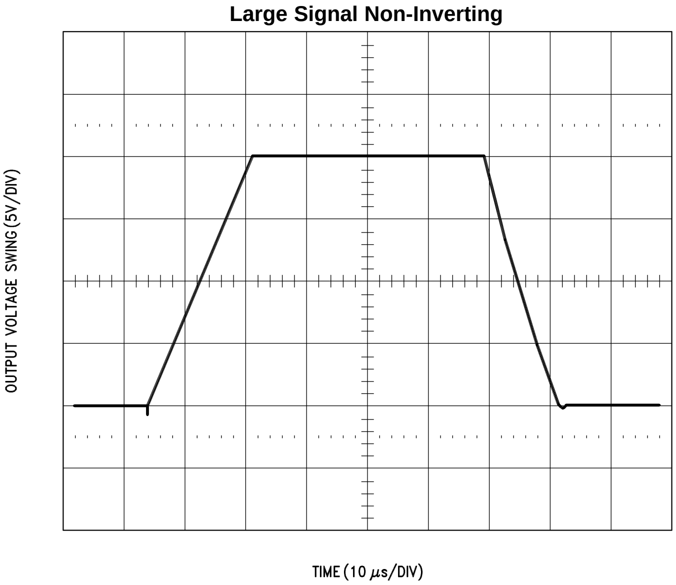


Figure 27.

APPLICATION HINTS

This device is a quad low power op amp with JFET input devices (BI-FET™). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased to allow normal circuit operation with power supplies of ±3.0V. Supply voltages less than these may degrade the common-mode rejection and restrict the output voltage swing.

The amplifiers will drive a 10 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

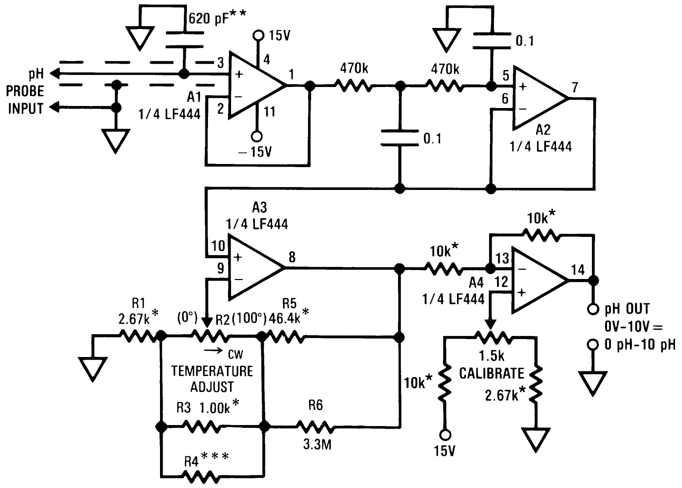
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pick-up” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Application

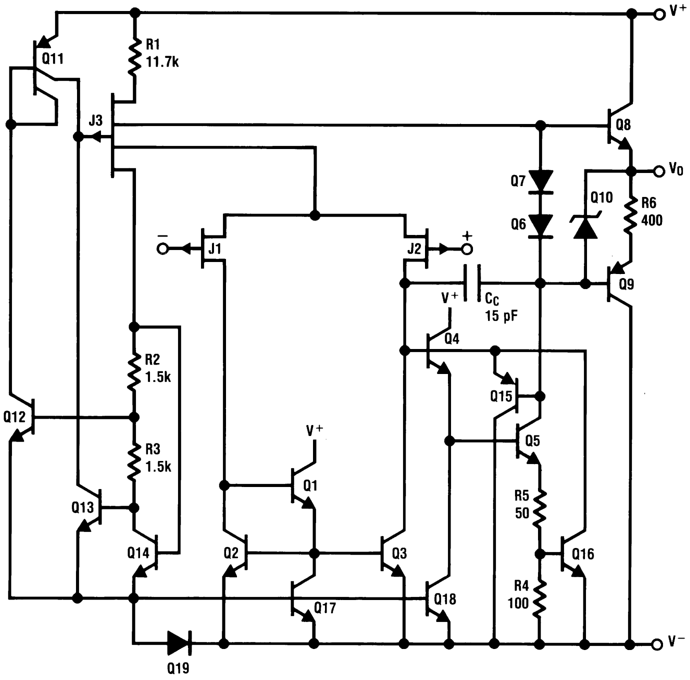
Figure 28. pH Probe Amplifier/Temperature Compensator



***For R2 = 50k, R4 = 330k ±1%
For R2 = 100k, R4 = 75k ±1%
For R2 = 200k, R4 = 56k ±1%
**Polystyrene
*Film resistor type RN60C
To calibrate, insert probe in pH =7 solution. Set the “TEMPERATURE ADJUST” pot, R2, to correspond to the solution temperature: full clockwise for 0°C, and proportionately for intermediate temperatures, using a turns-counting dial.
Then set “CALIBRATE” pot so output reads 7V.
Typical probe = Ingold Electrodes #465-35

Detailed Schematic

Figure 29. 1/4 Quad



REVISION HISTORY

Changes from Revision C (March 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	10

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LF444ACN/NOPB	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	0 to 70	LF444ACN
LF444ACN/NOPB.B	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	0 to 70	LF444ACN
LF444CM/NOPB	Active	Production	SOIC (D) | 14	55 | TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 70	LF444CM
LF444CM/NOPB.B	Active	Production	SOIC (D) | 14	55 | TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 70	LF444CM
LF444CMX/NOPB	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	LF444CM
LF444CMX/NOPB.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	LF444CM
LF444CN/NOPB	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	0 to 70	LF444CN
LF444CN/NOPB.B	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	0 to 70	LF444CN

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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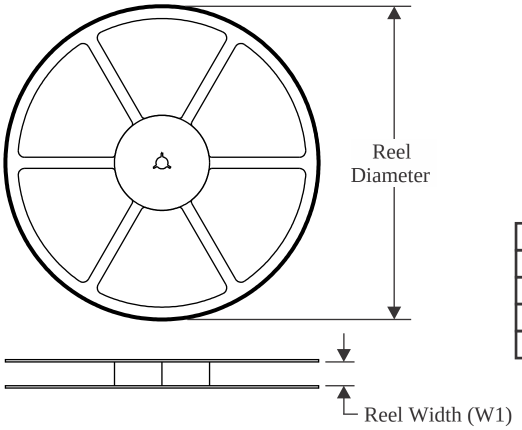
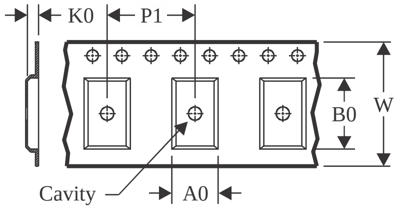
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

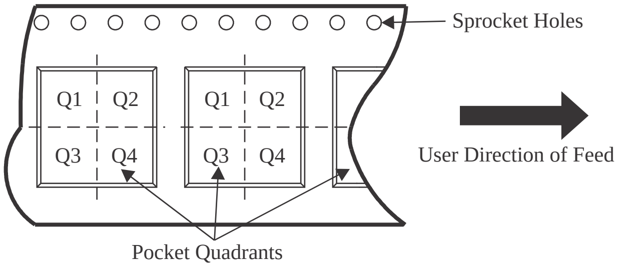


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

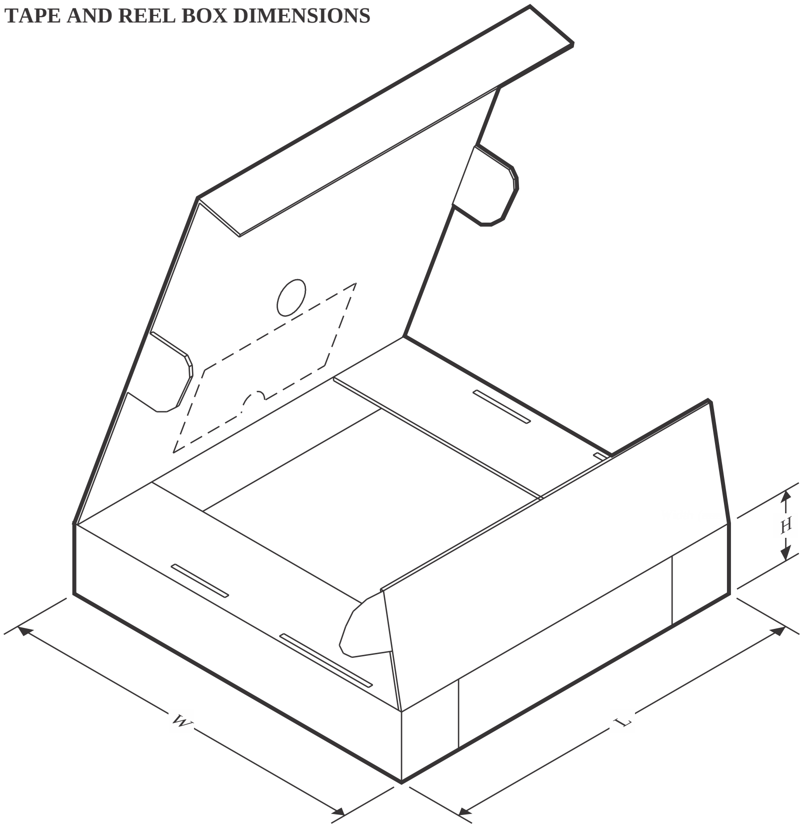
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LF444CMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

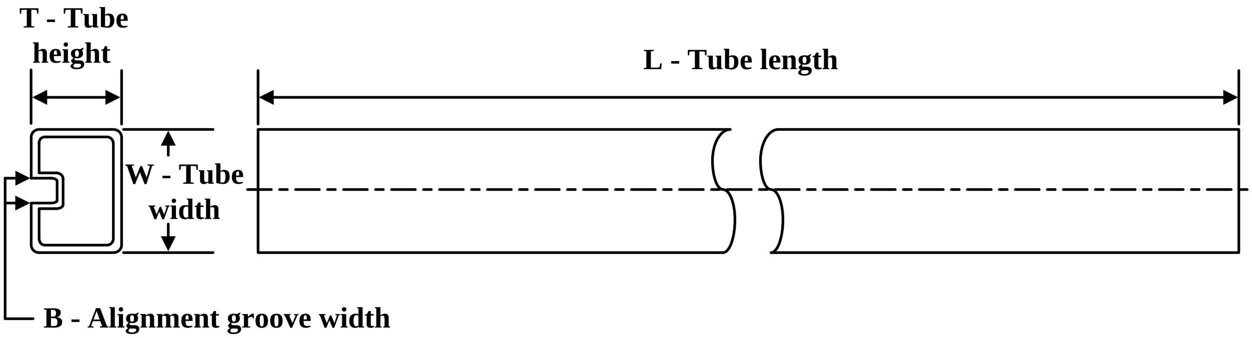
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LF444CMX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0

TUBE

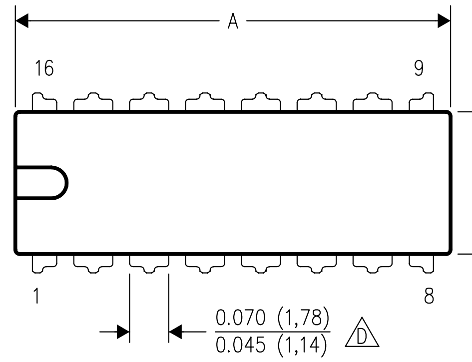


*All dimensions are nominal

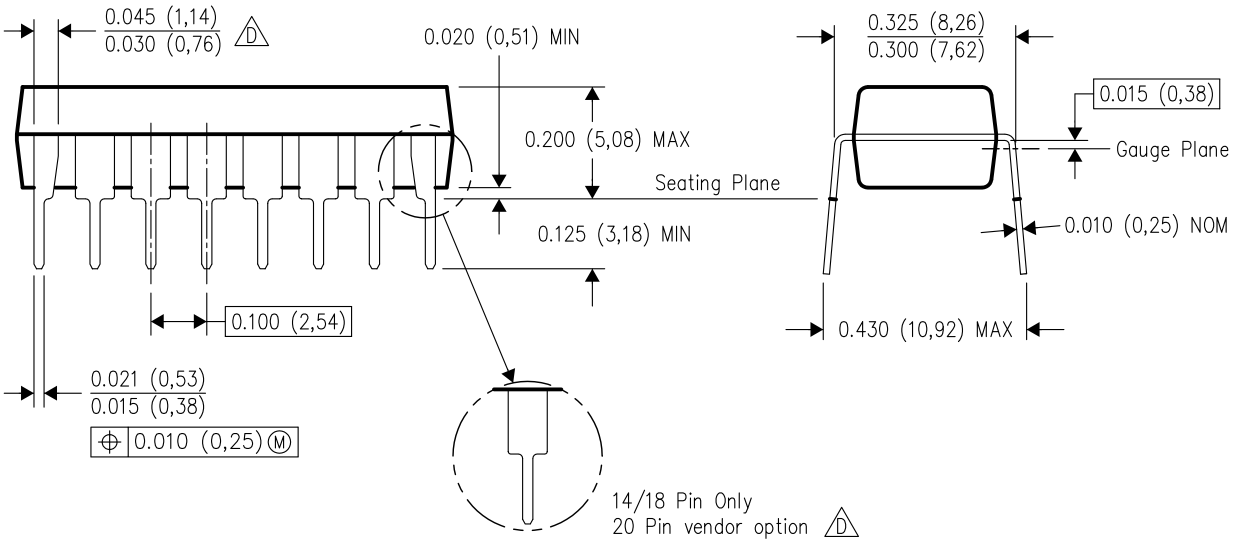
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LF444ACN/NOPB	N	PDIP	14	25	502	14	11938	4.32
LF444ACN/NOPB.B	N	PDIP	14	25	502	14	11938	4.32
LF444CM/NOPB	D	SOIC	14	55	495	8	4064	3.05
LF444CM/NOPB.B	D	SOIC	14	55	495	8	4064	3.05
LF444CN/NOPB	N	PDIP	14	25	502	14	11938	4.32
LF444CN/NOPB.B	N	PDIP	14	25	502	14	11938	4.32

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

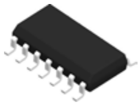


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
△C MS–001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- △C Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
- △D The 20 pin end lead shoulder width is a vendor option, either half or full width.

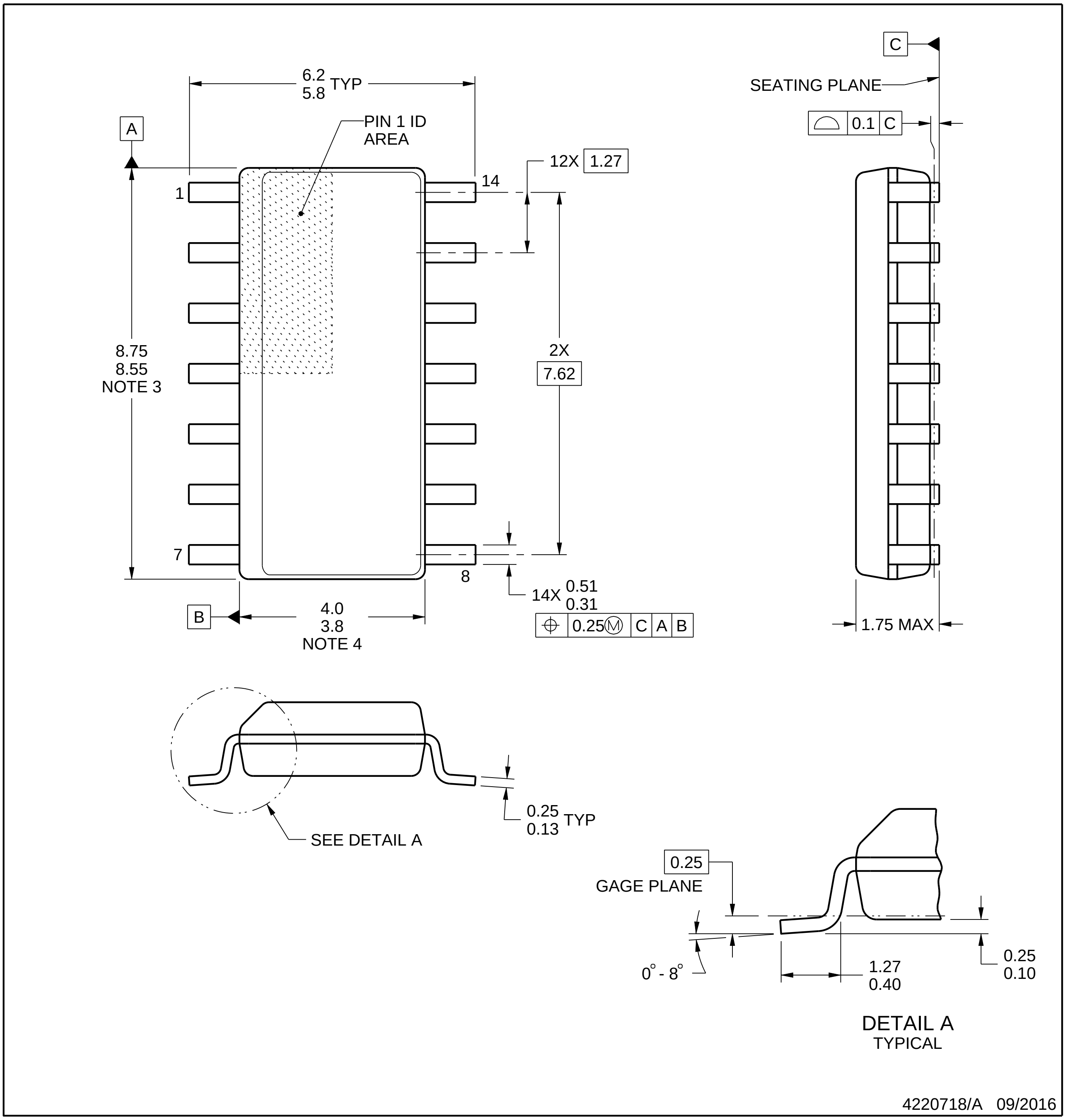


PACKAGE OUTLINE

D0014A

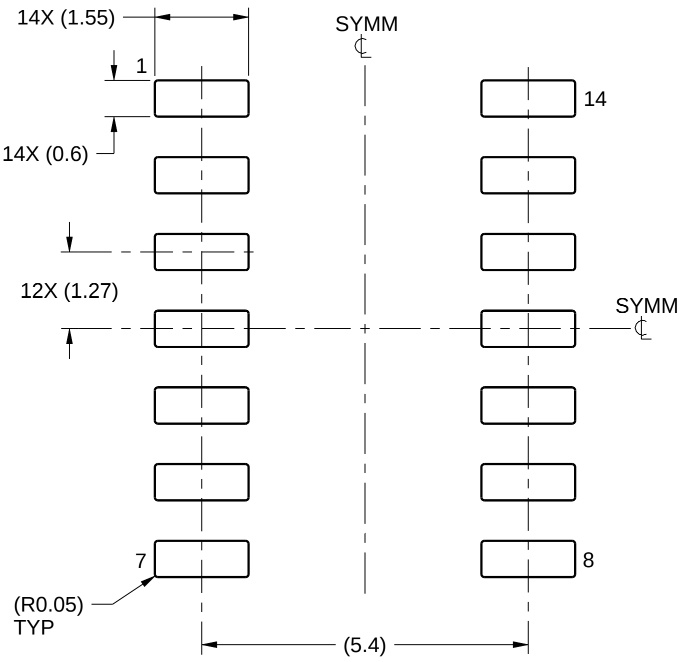
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

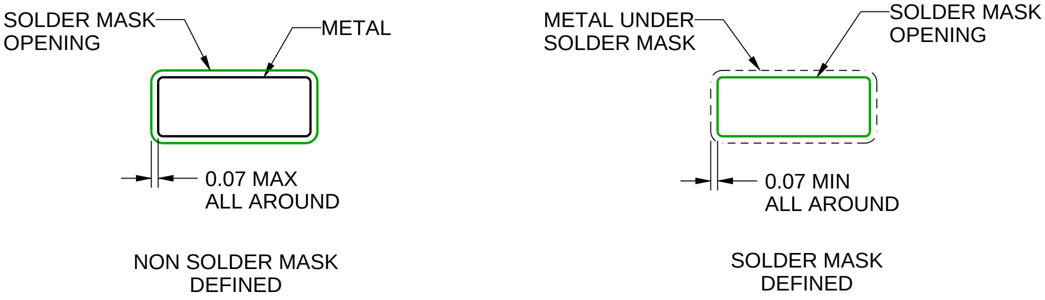


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X

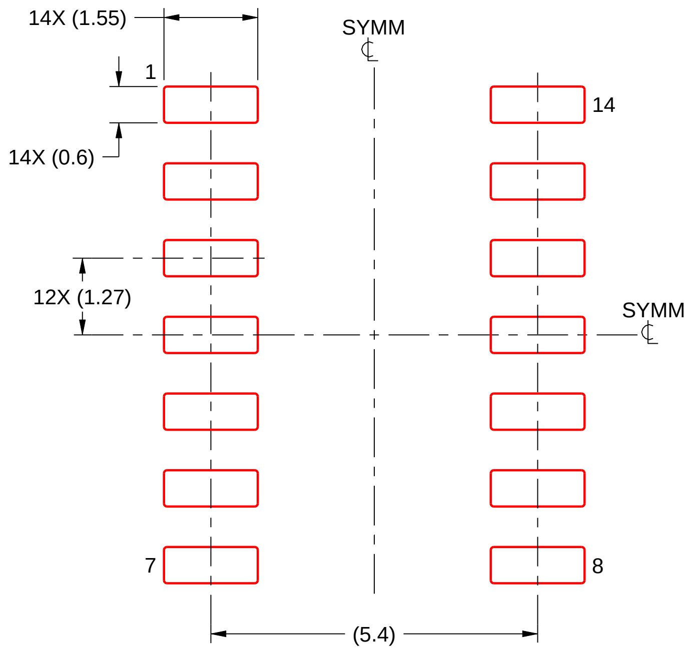


SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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