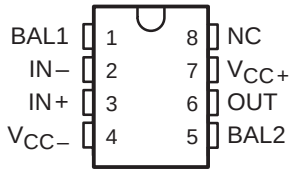
SLOS011C – MARCH 1987 – REVISED OCTOBER 1997

- **Low Input Bias Current, 50 pA Typ**
- **Low Input Noise Current, 0.01 pA/$\sqrt{\text{Hz}}$ Typ**
- **Low Supply Current, 2 mA Typ**
- **High Input impedance, 10^{12} Ω Typ**
- **Low Total Harmonic Distortion**
- **Low 1/f Noise Corner, 50 Hz Typ**
- **Package Options Include Plastic Small-Outline (D) and Standard (P) DIPs**

D OR P PACKAGE
(TOP VIEW)



NC – No internal connection

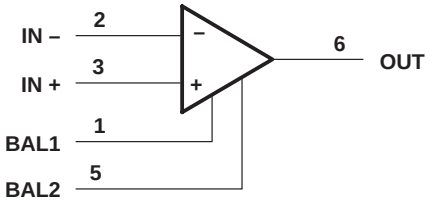
description

This device is a low-cost, high-speed, JFET-input operational amplifier with very low input offset voltage and a maximum input offset voltage drift. It requires low supply current, yet maintains a large gain-bandwidth product and a fast slew rate. In addition, the matched high-voltage JFET input provides very low input bias and offset currents.

The LF411 can be used in applications such as high-speed integrators, digital-to-analog converters, sample-and-hold circuits, and many other circuits.

The LF411C is characterized for operation from 0°C to 70°C. The LF411I is characterized for operation from –40°C to 85°C.

symbol



AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGE	
		SMALL OUTLINE (D)	PLASTIC DIP (P)
0°C to 70°C	2 mV	LF411CD	LF411CP
–40°C to 85°C	2 mV	LF411ID	LF411IP

The D packages are available taped and reeled. Add the suffix R to the device type (i.e., LF411CDR).

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} . . . . . 18 V
Supply voltage, V_{CC-} . . . . . –18 V
Differential input voltage, V_{ID} . . . . . ±30 V
Input voltage, V_I (see Note 1) . . . . . ±15 V
Duration of output short circuit . . . . . Unlimited
Continuous total power dissipation . . . . . 500 mW
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . . 197°C/W
P package . . . . . 104°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

	C SUFFIX		I SUFFIX		UNIT
	MIN	MAX	MIN	MAX	
Supply voltage, V_{CC+}	3.5	18	3.5	18	V
Supply voltage, V_{CC-}	–3.5	–18	–3.5	–18	V
Operating free-air temperature, T_A	0	70	–40	–85	°C

electrical characteristics over operating free-air temperature range, $V_{CC\pm}$ = ±15 V (unless otherwise specified)

PARAMETER		TEST CONDITIONS		T_A		MIN	TYP	MAX	UNIT
				LF411C	LF411I				
V_{IO}	Input offset voltage	V_{IC} = 0,	R_S = 10 kΩ	25°C	25°C		0.8	2	mV
α_{VIO}	Average temperature coefficient of input offset voltage	V_{IC} = 0,	R_S = 10 kΩ				10	20†	µV/°C
I_{IO}	Input offset current‡	V_{IC} = 0		25°C	25°C		25	100	pA
				70°C	85°C			2	nA
I_{IB}	Input bias current‡	V_{IC} = 0		25°C	25°C		50	200	pA
				70°C	85°C			4	nA
V_{ICR}	Common-mode input voltage range					±11	–11.5 to 14.5		V
V_{OM}	Maximum peak output-voltage swing	R_L = 10 kΩ				±12	±13.5		V
A_{VD}	Large-signal differential voltage	V_O = ±10 V,	R_L = 2 kΩ	25°C	25°C	25	200		V/mV
				0°C to 70°C	–40°C to 85°C	15	200		
r_i	Input resistance	T_J = 25°C					10^{12}		Ω
CMRR	Common-mode rejection ratio	R_S ≤ 10 kΩ				70	100		dB
k_{SVR}	Supply-voltage rejection ratio	See Note 3				70	100		dB
I_{CC}	Supply current						2	3.4	mA

† At least 90% of the devices meet this limit for α_{VIO}.
‡ Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperatures as close to the ambient temperature as possible.
NOTE 3: Supply-voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate		8	13		V/μs
B_1	Unity-gain bandwidth		2.7	3		MHz
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 20 Ω		18		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz		0.01		pA/√Hz

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LF411CD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	LF411C
LF411CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LF411C
LF411CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LF411C
LF411CDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	0 to 70	
LF411CP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	LF411CP
LF411CP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	LF411CP
LF411CPE4	Active	Production	PDIP (P) | 8	50 | TUBE	-	Call TI	Call TI	0 to 70	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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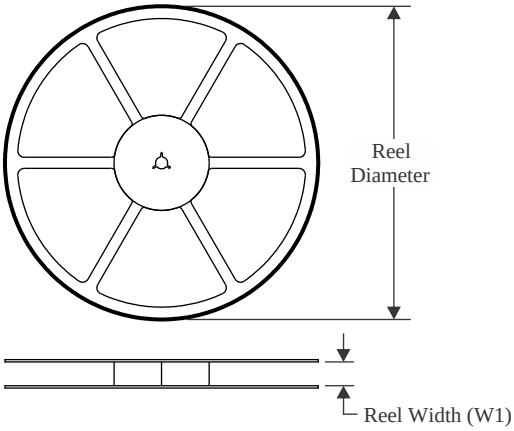
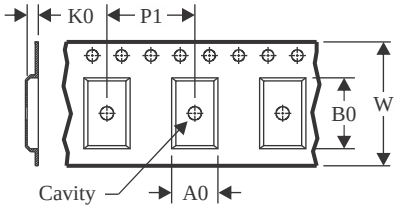
TAPE AND REEL INFORMATION

REEL DIMENSIONS

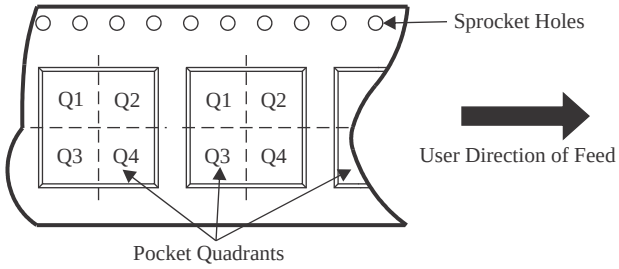


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

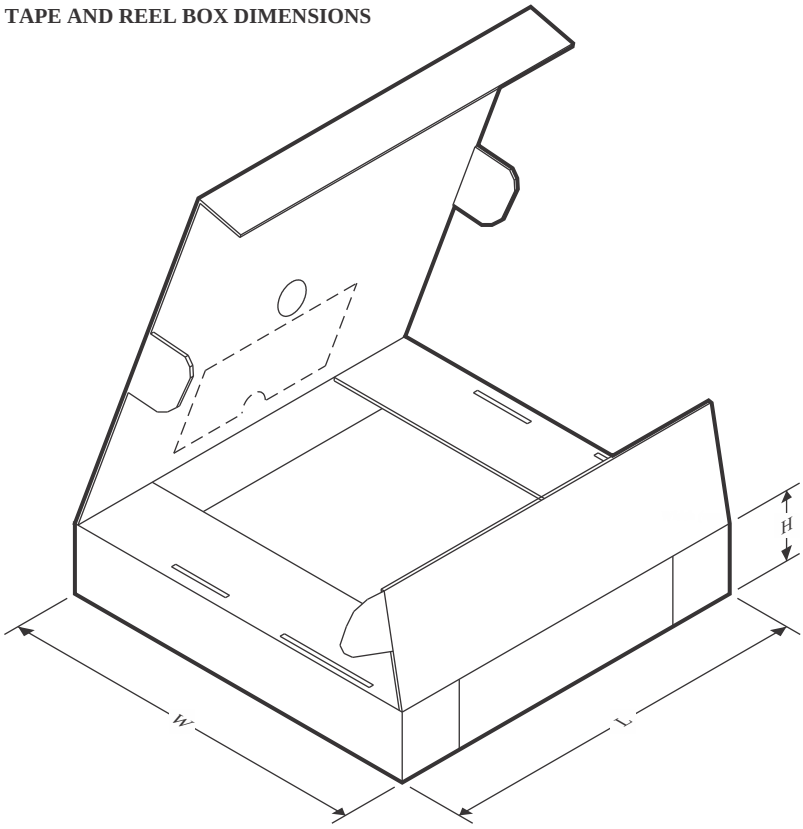
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LF411CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

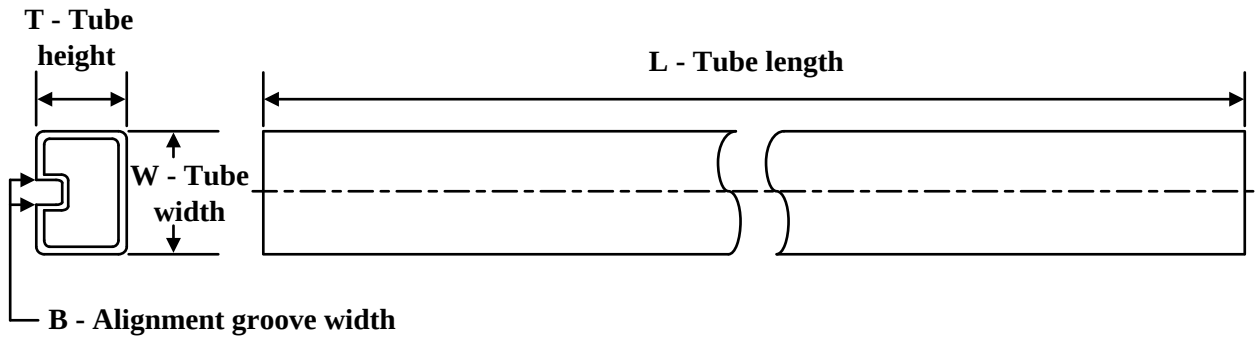
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

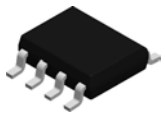
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LF411CDR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LF411CP	P	PDIP	8	50	506	13.97	11230	4.32
LF411CP.A	P	PDIP	8	50	506	13.97	11230	4.32

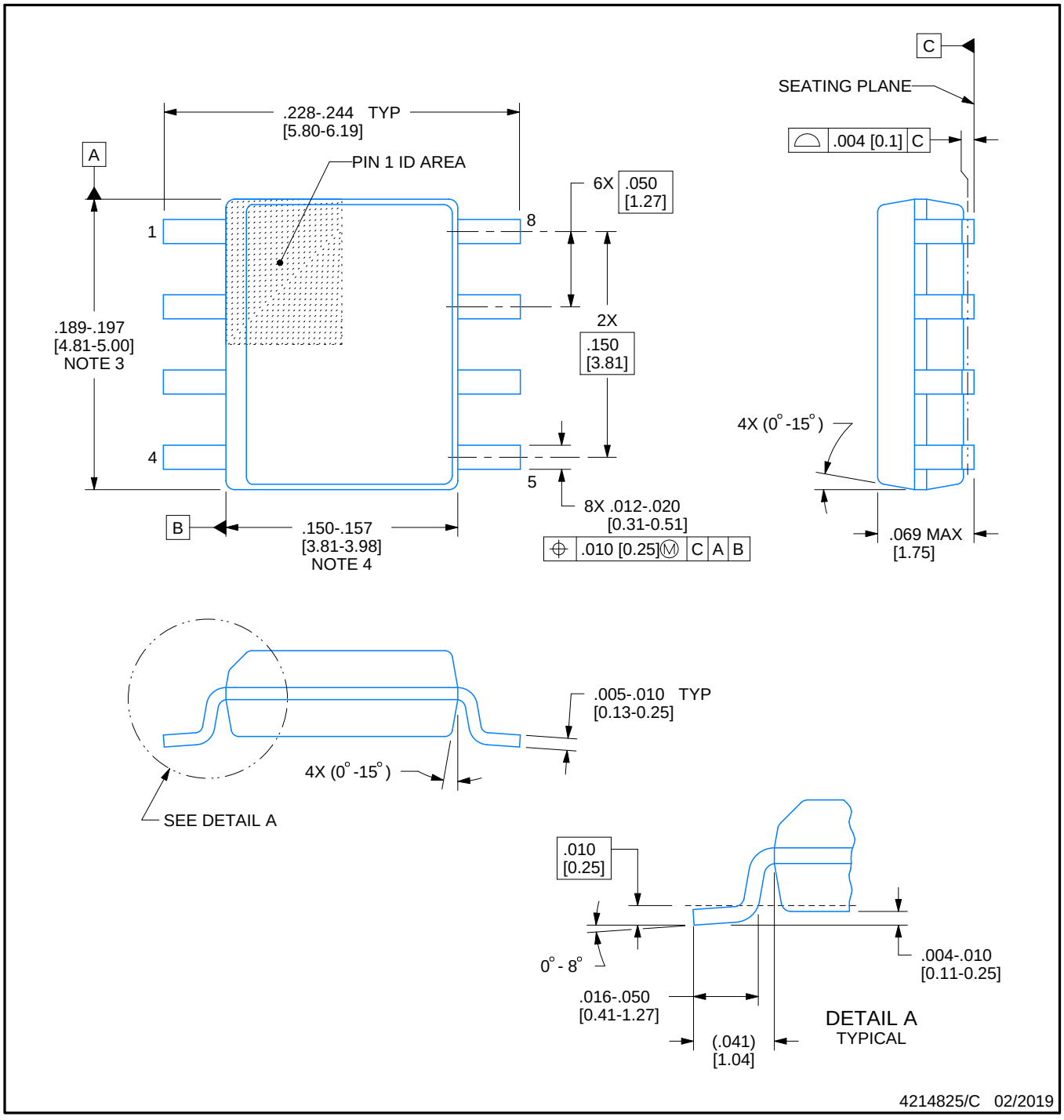


PACKAGE OUTLINE

D0008A

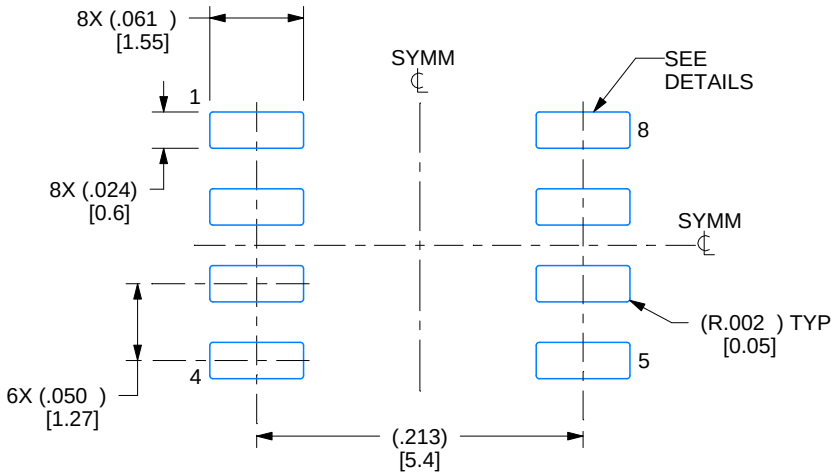
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

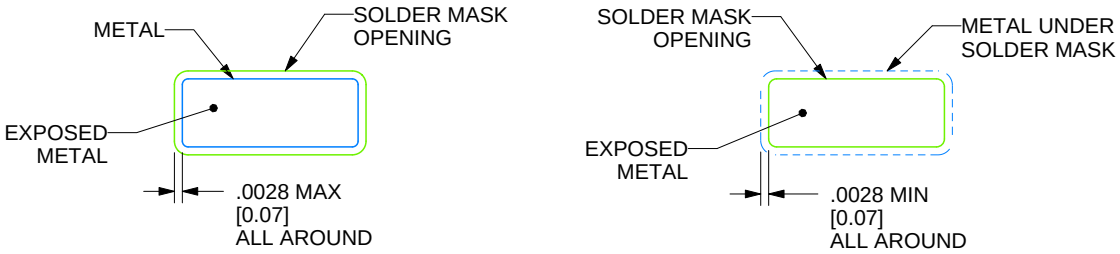


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

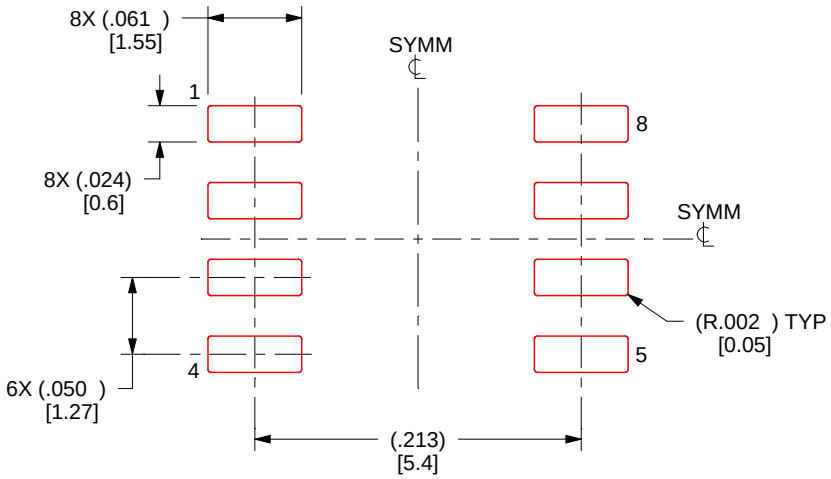
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



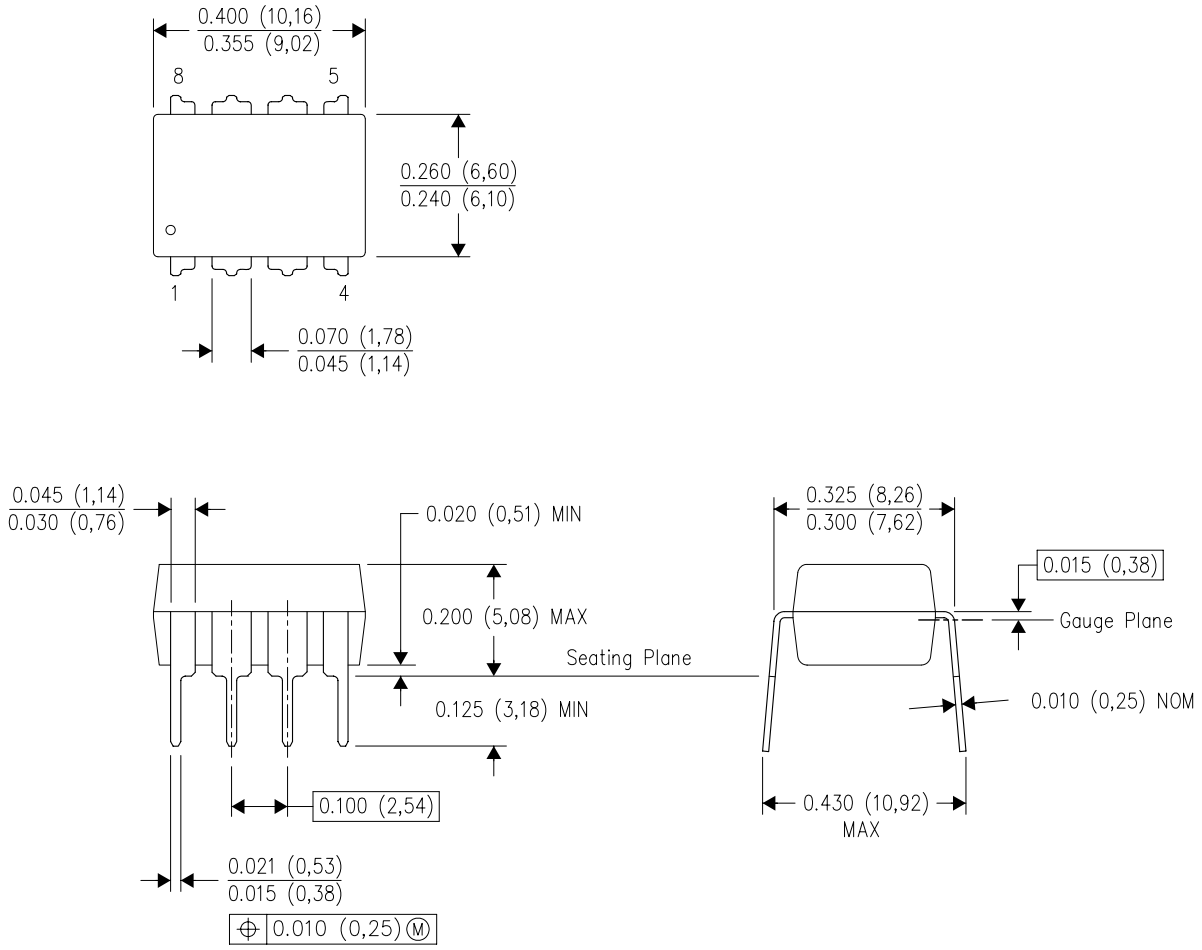
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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