LF353-N Wide Bandwidth Dual JFET Input Operational Amplifier

Check for Samples: LF353-N

FEATURES

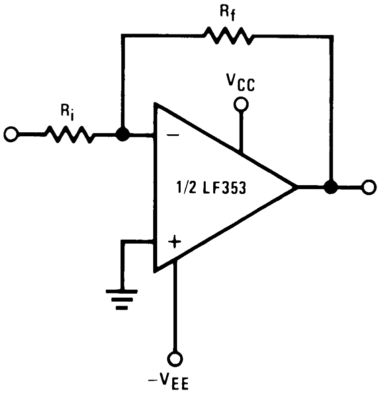
- **Internally Trimmed Offset Voltage: 10 mV**
- **Low Input Bias Current: 50pA**
- **Low Input Noise Voltage: 25 nV/√Hz**
- **Low Input Noise Current: 0.01 pA/√Hz**
- **Wide Gain Bandwidth: 4 MHz**
- **High Slew Rate: 13 V/μs**
- **Low Supply Current: 3.6 mA**
- **High Input Impedance: $10^{12}\Omega$**
- **Low Total Harmonic Distortion : ≤0.02%**
- **Low 1/f Noise Corner: 50 Hz**
- **Fast Settling Time to 0.01%: 2 μs**

DESCRIPTION

These devices are low cost, high speed, dual JFET input operational amplifiers with an internally trimmed input offset voltage (BI-FET II technology). They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF353-N is pin compatible with the standard LM1558 allowing designers to immediately upgrade the overall performance of existing LM1558 and LM358 designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The devices also exhibit low noise and offset voltage drift.

Typical Connection



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Simplified Schematic

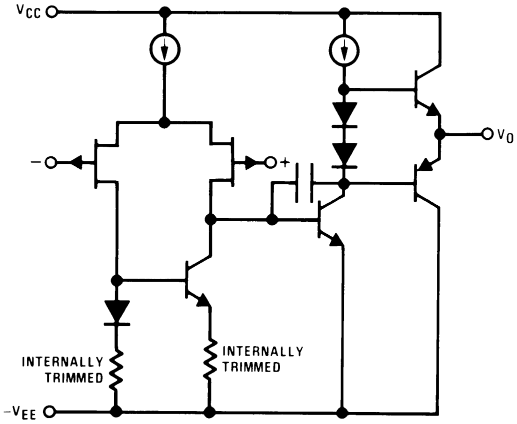


Figure 1. 1/2 Dual

Dual-In-Line Package
Top View

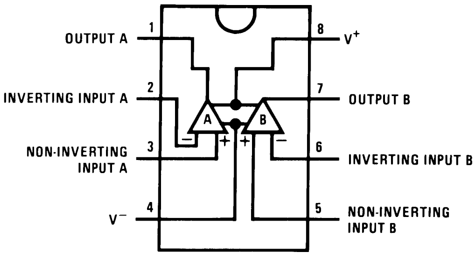


Figure 2. 8-Pin SOIC (See D Package)
8-Pin PDIP (See P Package)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

Supply Voltage		±18V
Power Dissipation		See(3)
Operating Temperature Range		0°C to +70°C
T_j(MAX)		150°C
Differential Input Voltage		±30V
Input Voltage Range(4)		±15V
Output Short Circuit Duration		Continuous
Storage Temperature Range		−65°C to +150°C
Lead Temp. (Soldering, 10 sec.)		260°C
Soldering Information: Dual-In-Line Package Soldering (10 sec.)		260°C
Small Outline Package	Vapor Phase (60 sec.)	215°C
	Infrared (15 sec.)	220°C
ESD Tolerance(5)		1000V
θ_{JA} D Package		TBD

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) For operating at elevated temperatures, the device must be derated based on a thermal resistance of 115°C/W typ junction to ambient for the P package, and 160°C/W typ junction to ambient for the D package.
(4) Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.
(5) Human body model, 1.5 kΩ in series with 100 pF.

DC Electrical Characteristics

Symbol	Parameter	Conditions	LF353-N			Units
			MIn	Typ	Max	
V_{OS}	Input Offset Voltage	R_S=10kΩ, T_A=25°C Over Temperature		5	10	mV
					13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S=10 kΩ		10		μV/°C
I_{OS}	Input Offset Current	T_j=25°C (1)(2)		25	100	pA
		T_j≤70°C			4	nA
I_B	Input Bias Current	T_j=25°C (1)(2)		50	200	pA
		T_j≤70°C			8	nA
R_{IN}	Input Resistance	T_j=25°C		10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S=±15V, T_A=25°C	25	100		V/mV
		V_O=±10V, R_L=2 kΩ				
		Over Temperature	15			V/mV
V_O	Output Voltage Swing	V_S=±15V, R_L=10kΩ	±12	±13.5		V
V_{CM}	Input Common-Mode Voltage	V_S=±15V	±11	+15		V
	Range			−12		V
CMRR	Common-Mode Rejection Ratio	R_S≤ 10kΩ	70	100		dB
PSRR	Supply Voltage Rejection Ratio	See (3)	70	100		dB
I_S	Supply Current			3.6	6.5	mA

(1) These specifications apply for V_S=±15V and 0°C≤T_A≤+70°C. V_{OS}, $I_B$and I_{OS} are measured at V_{CM}=0.

(2) The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. T_j=T_A+θ_{jA} P_D where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

(3) Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. V_S = ±6V to ±15V.

AC Electrical Characteristics (1)

Symbol	Parameter	Conditions	LF353-N			Units
			Min	Typ	Max	
	Amplifier to Amplifier Coupling	T_A=25°C, f=1 Hz−20 kHz (Input Referred)		−120		dB
SR	Slew Rate	V_S=±15V, T_A=25°C	8.0	13		V/μs
GBW	Gain Bandwidth Product	V_S=±15V, T_A=25°C	2.7	4		MHz
e_n	Equivalent Input Noise Voltage	T_A=25°C, R_S=100Ω, f=1000 Hz		16		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	T_j=25°C, f=1000 Hz		0.01		$pA/\sqrt{Hz}$
THD	Total Harmonic Distortion	A_V=+10, RL=10k, V_O=20Vp−p, BW=20 Hz-20 kHz		<0.02		%

(1) These specifications apply for V_S=±15V and 0°C≤T_A≤+70°C. V_{OS}, $I_B$and I_{OS} are measured at V_{CM}=0.

Typical Performance Characteristics

Input Bias Current

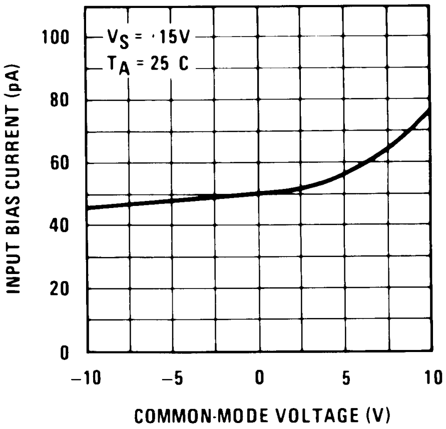


Figure 3.

Input Bias Current

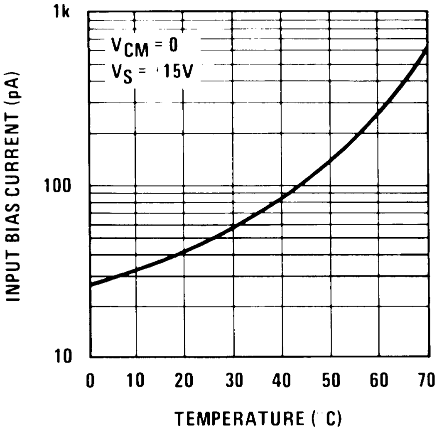


Figure 4.

Supply Current

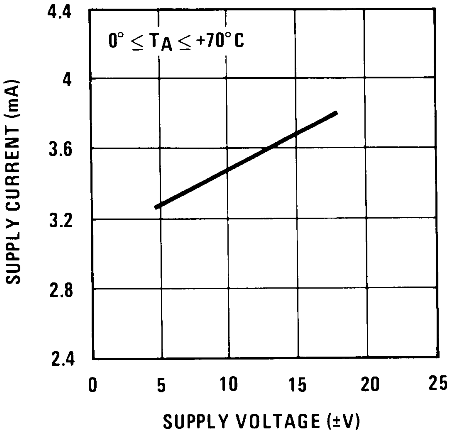


Figure 5.

Positive Common-Mode Input Voltage Limit

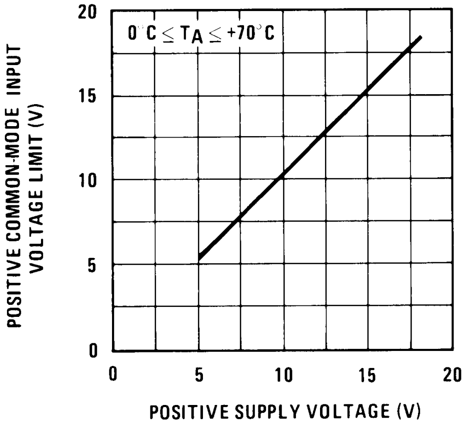


Figure 6.

Negative Common-Mode Input Voltage Limit

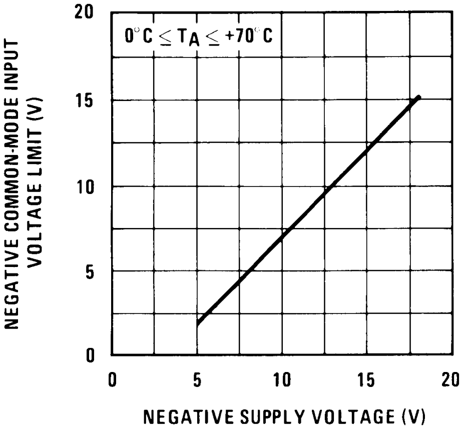


Figure 7.

Positive Current Limit

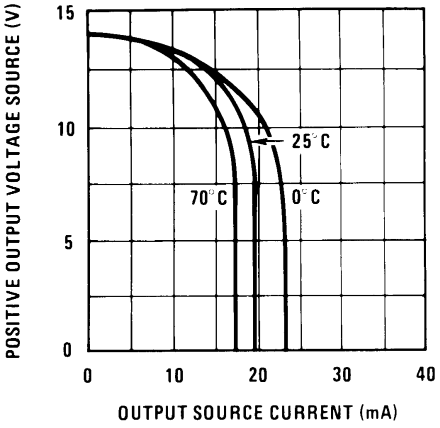


Figure 8.

Typical Performance Characteristics (continued)

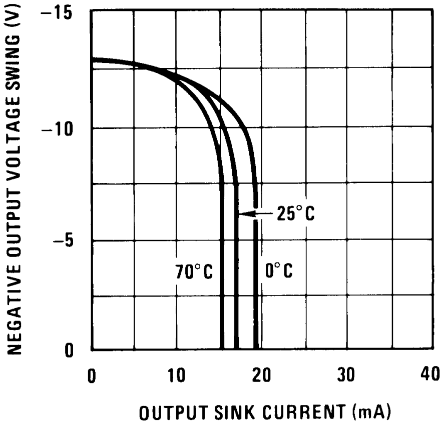

Negative Current Limit

Figure 9.

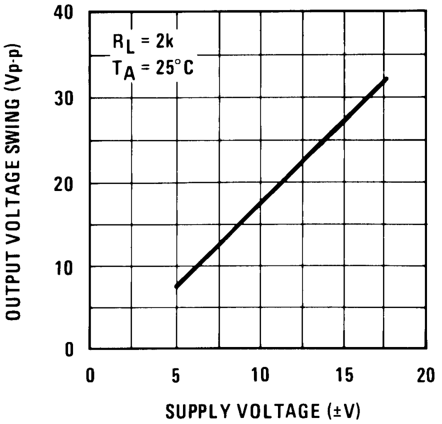

Voltage Swing

Figure 10.

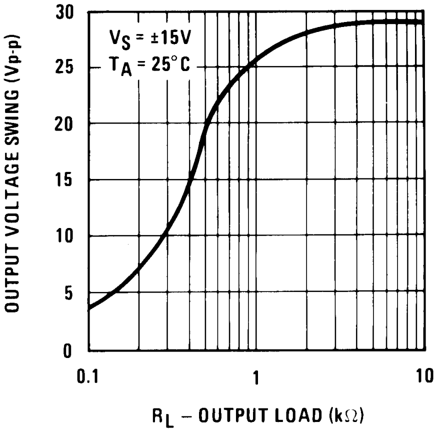

Output Voltage Swing

Figure 11.

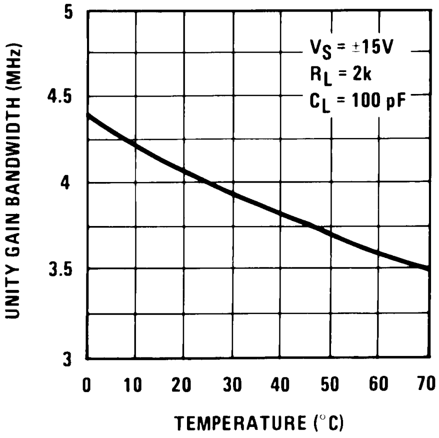

Gain Bandwidth

Figure 12.

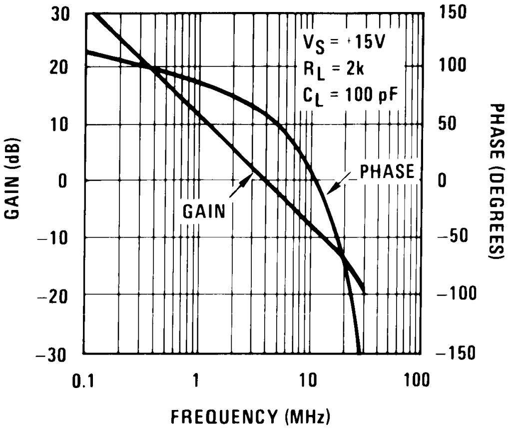

Bode Plot

Figure 13.

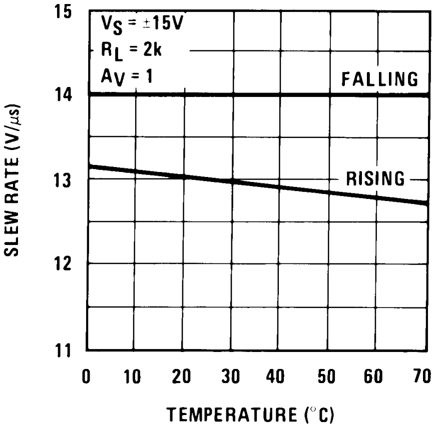

Slew Rate

Figure 14.

Typical Performance Characteristics (continued)

Distortion vs. Frequency

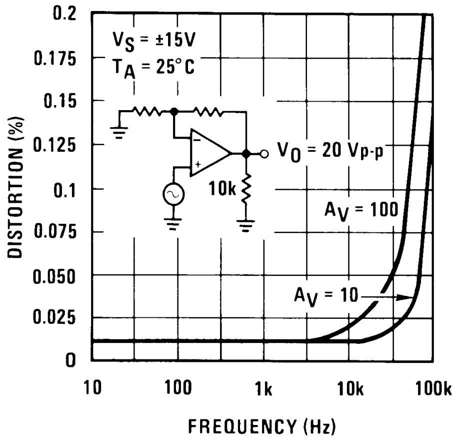


Figure 15.

Undistorted Output Voltage Swing

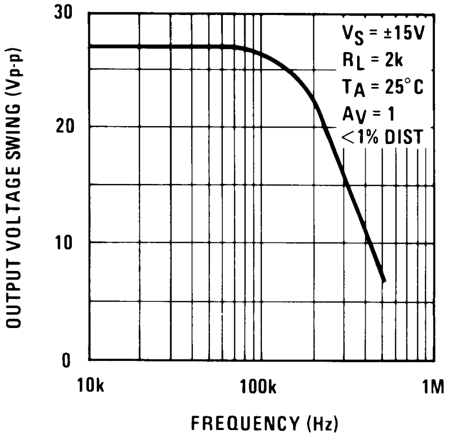


Figure 16.

Open Loop Frequency Response

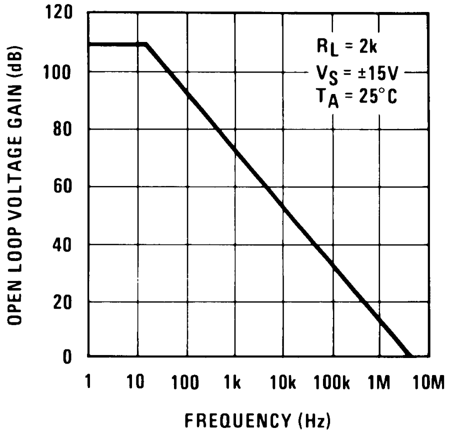


Figure 17.

Common-Mode Rejection Ratio

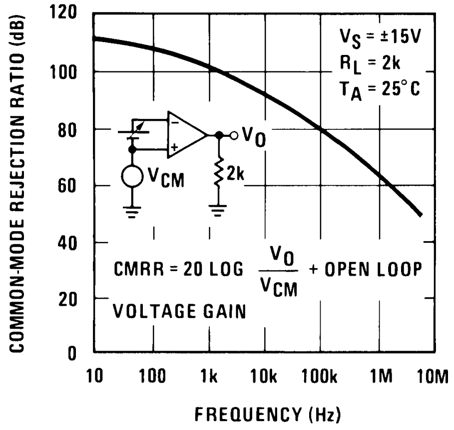


Figure 18.

Power Supply Rejection Ratio

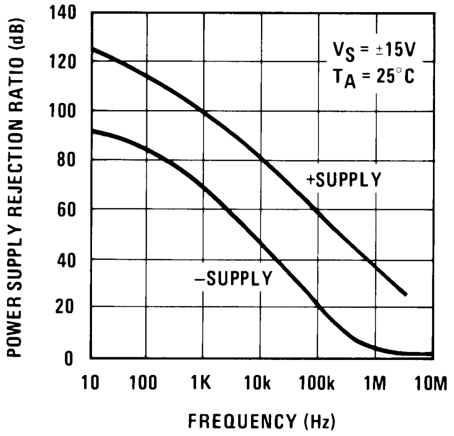


Figure 19.

Equivalent Input Noise Voltage

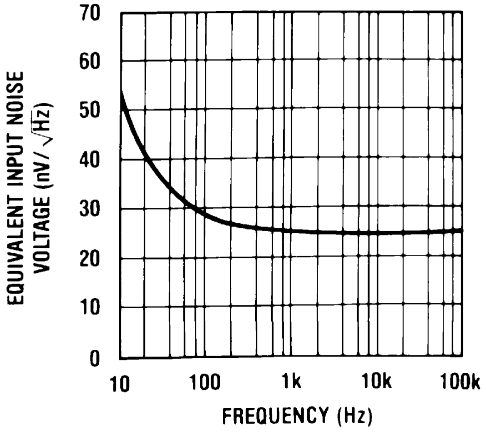


Figure 20.

Typical Performance Characteristics (continued)

Open Loop Voltage Gain (V/V)

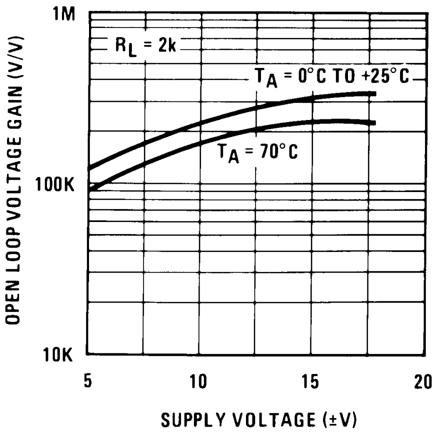


Figure 21.

Output Impedance

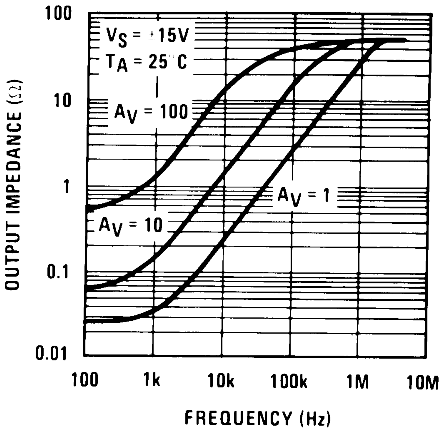


Figure 22.

Inverter Settling Time

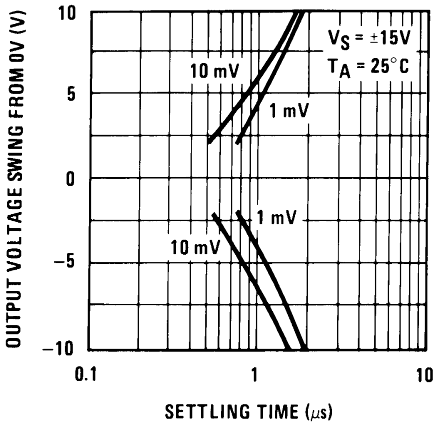


Figure 23.

Pulse Response

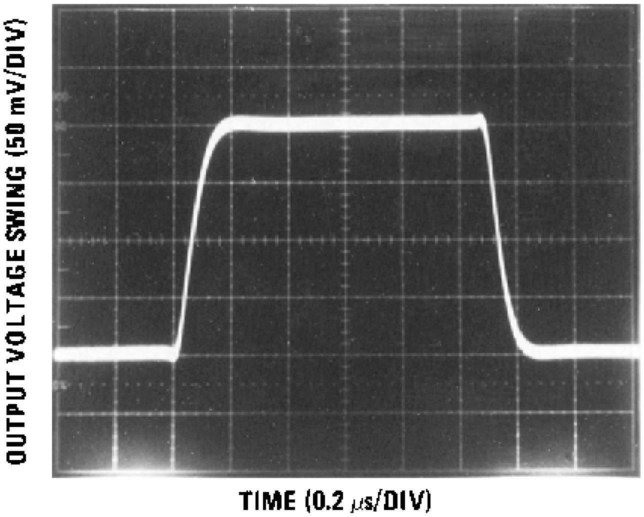


Figure 24. Small Signaling Inverting

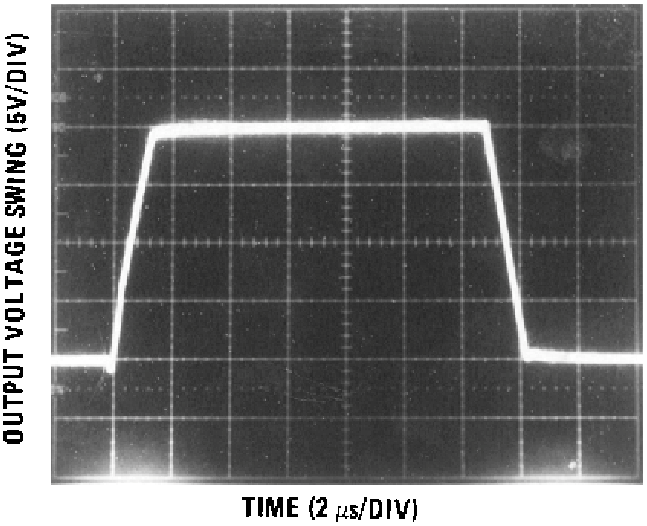


Figure 25. Large Signal Inverting

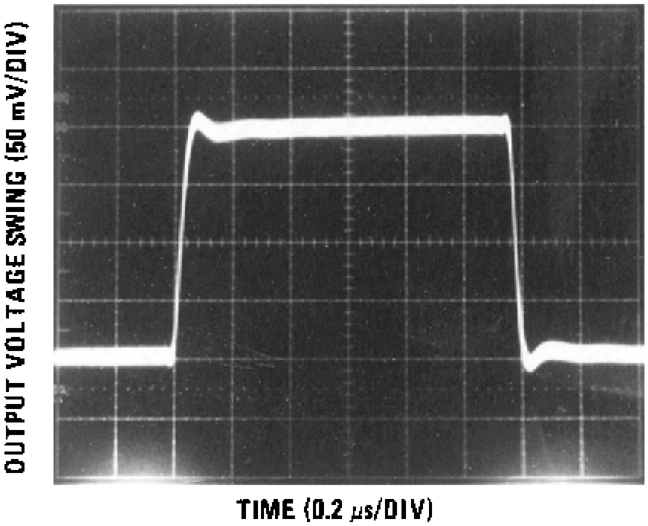


Figure 26. Small Signal Non-Inverting

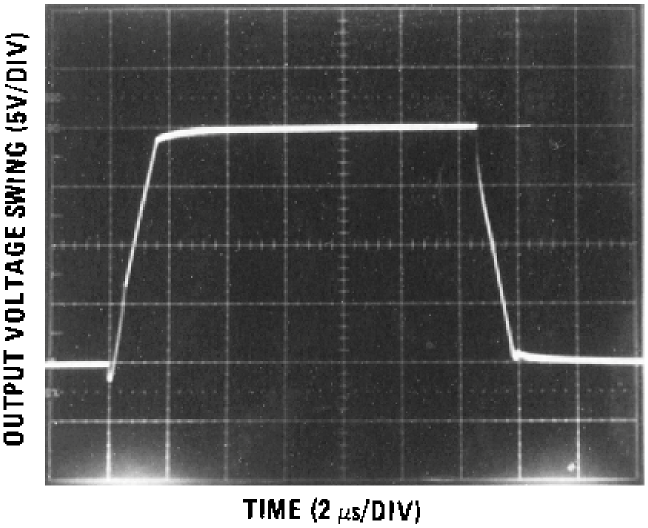


Figure 27. Large Signal Non-Inverting

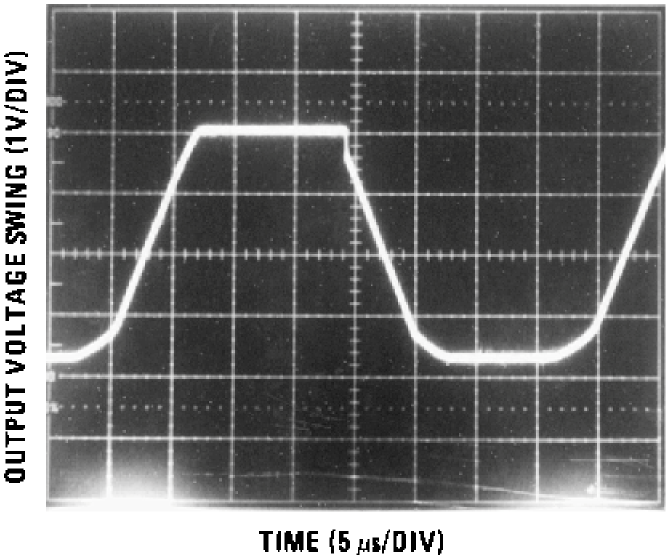


Figure 28. Current Limit (R_L = 100Ω)

APPLICATION HINTS

These devices are op amps with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±6V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

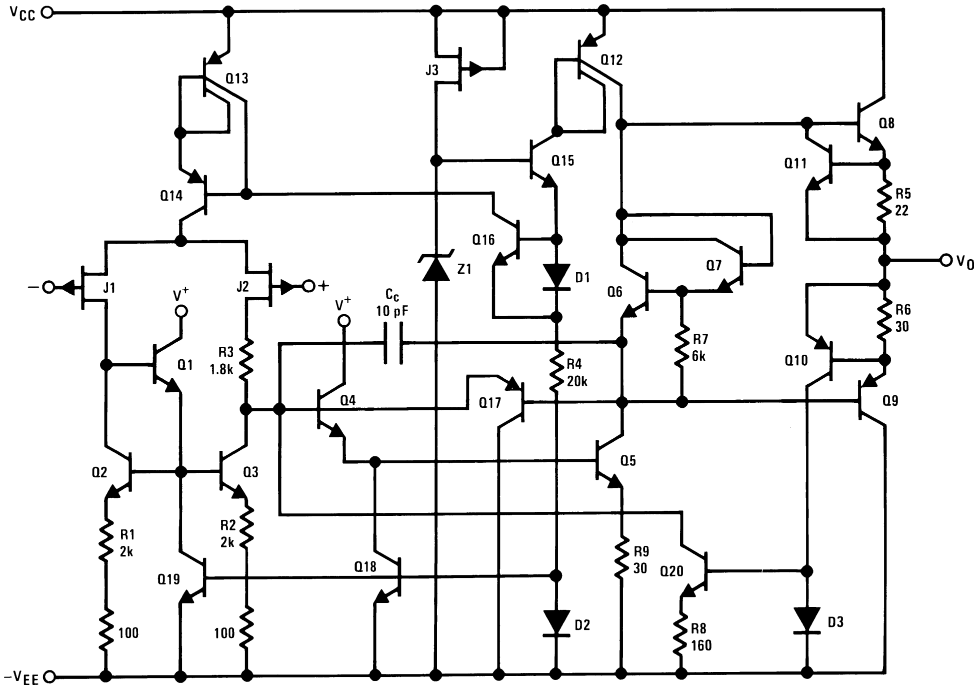
The amplifiers will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pick-up” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

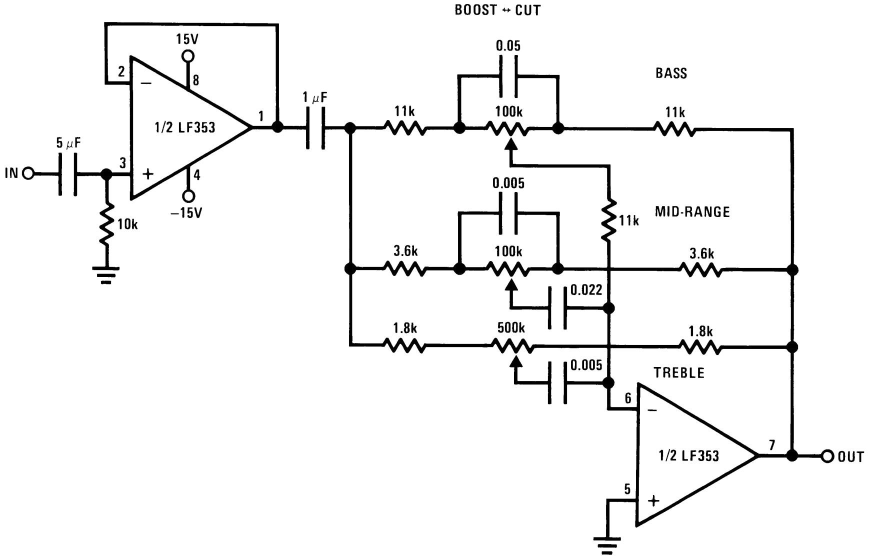
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

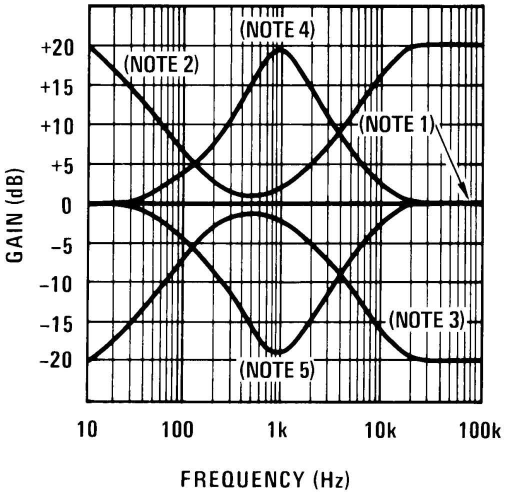
Detailed Schematic



Typical Applications

Three-Band Active Tone Control





(1) All controls flat.

(2) Bass and treble boost, mid flat.

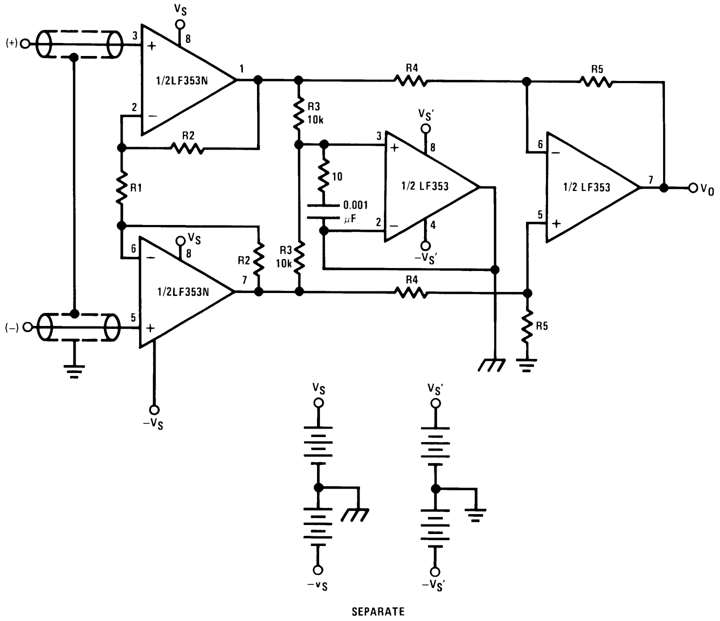
(3) Bass and treble cut, mid flat.

(4) Mid boost, bass and treble flat.

(5) Mid cut, bass and treble flat.

- All potentiometers are linear taper
- Use the LF347 Quad for stereo applications

Improved CMRR Instrumentation Amplifier



$$A_V = \left(\frac{2R2}{R1} + 1\right)\frac{R5}{R4}$$

⊥ and ⏚ are separate isolated grounds

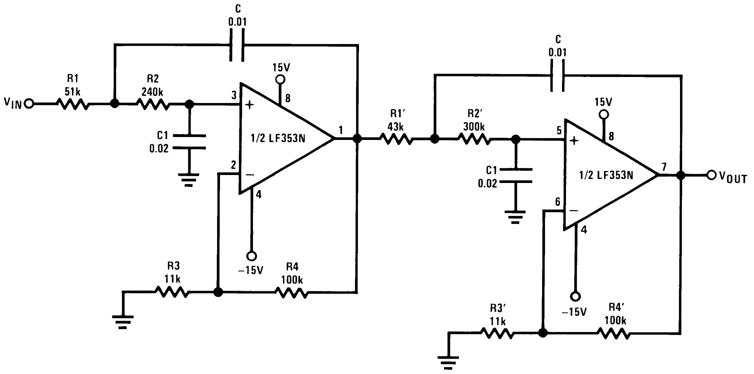
Matching of R2's, R4's and R5's control CMRR

With A_{V_T} = 1400, resistor matching = 0.01%: CMRR = 136 dB

- Very high input impedance
- Super high CMRR

(1)

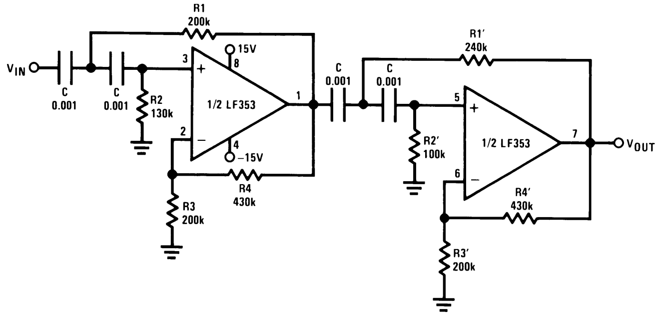
Fourth Order Low Pass Butterworth Filter



- Corner frequency $(f_C) = \sqrt{\frac{1}{R1R2CC1}} \cdot \frac{1}{2\pi} = \sqrt{\frac{1}{R1'R2'CC1}} \cdot \frac{1}{2\pi}$
- Passband gain (H_O) = (1 + R4/R3) (1 + R4′/R3′)
- First stage Q = 1.31
- Second stage Q = 0.541
- Circuit shown uses nearest 5% tolerance resistor values for a filter with a corner frequency of 100 Hz and a passband gain of 100
- Offset nulling necessary for accurate DC performance

(2)

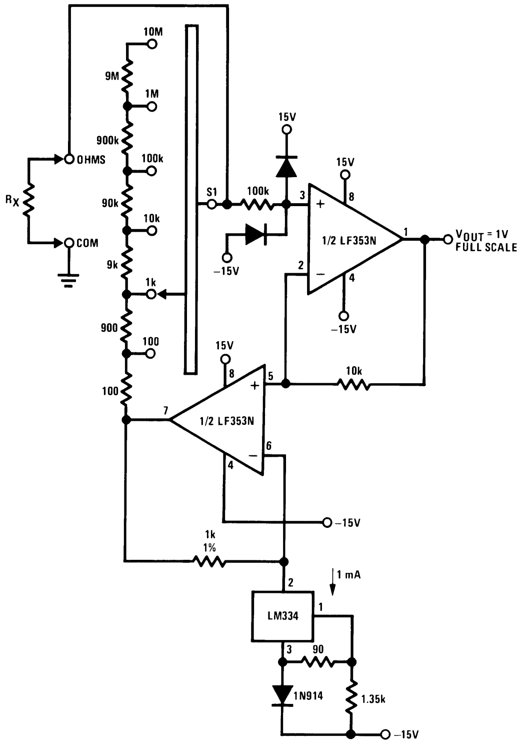
Fourth Order High Pass Butterworth Filter



- Corner frequency $(f_C) = \sqrt{\frac{1}{R1R2C^2}} \bullet \frac{1}{2\pi} = \sqrt{\frac{1}{R1'R2'C^2}} \bullet \frac{1}{2\pi}$
- Passband gain $(H_O) = (1 + R4/R3)\ (1 + R4'/R3')$
- First stage $Q = 1.31$
- Second stage $Q = 0.541$
- Circuit shown uses closest 5% tolerance resistor values for a filter with a corner frequency of 1 kHz and a passband gain of 10.

(3)

Ohms-to-Volts Converter



$$V_O = \frac{1V}{R_{LADDER}} \times R_X$$

Where R_{LADDER} is the resistance from switch S1 pole to pin 7 of the LF353.

(4)

REVISION HISTORY

Changes from Revision E (March 2013) to Revision F	Page
• Changed layout of National Data Sheet to TI format	15

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LF353M/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 70	LF353 M
LF353M/NOPB.B	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 70	LF353 M
LF353MX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	LF353 M
LF353MX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	LF353 M
LF353N/NOPB	Active	Production	PDIP (P) | 8	40 | TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	0 to 70	LF 353N
LF353N/NOPB.B	Active	Production	PDIP (P) | 8	40 | TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	0 to 70	LF 353N

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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