LF198QML Monolithic Sample-and-Hold Circuits

Check for Samples: LF198QML

FEATURES

- **Operates from ±5V to ±18V supplies**
- **Less than 10 µs acquisition time**
- **TTL, PMOS, CMOS compatible logic input**
- **0.5 mV typical hold step at C_h = 0.01 µF**
- **Low input offset**
- **0.002% gain accuracy**
- **Low output noise in hold mode**
- **Input characteristics do not change during hold mode**
- **High supply rejection ratio in sample or hold**
- **Wide bandwidth**

DESCRIPTION

The LF198 is a monolithic sample-and-hold circuit which utilizes BI-FET technology to obtain ultra-high dc accuracy with fast acquisition of signal and low droop rate. Operating as a unity gain follower, dc gain accuracy is 0.002% typical and acquisition time is as low as 6 µs to 0.01%. A bipolar input stage is used to achieve low offset voltage and wide bandwidth. Input offset adjust is accomplished with a single pin, and does not degrade input offset drift. The wide bandwidth allows the LF198 to be included inside the feedback loop of 1 MHz op amps without having stability problems. Input impedance of $10^{10}\Omega$ allows high source impedances to be used without degrading accuracy.

P-channel junction FET's are combined with bipolar devices in the output amplifier to give droop rates as low as 5 mV/min with a 1 µF hold capacitor. The JFET's have much lower noise than MOS devices used in previous designs and do not exhibit high temperature instabilities. The overall design specifies no feed-through from input to output in the hold mode, even for input signals equal to the supply voltages.

Logic inputs on the LF198 are fully differential with low input current, allowing direct connection to TTL, PMOS, and CMOS. Differential threshold is 1.4V. The LF198 will operate from ±5V to ±18V supplies.

Connection Diagrams

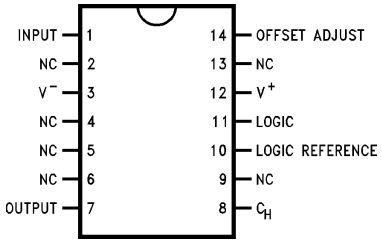


Figure 1. Small-Outline Package (CGLA)
See Package Number NAC0014A

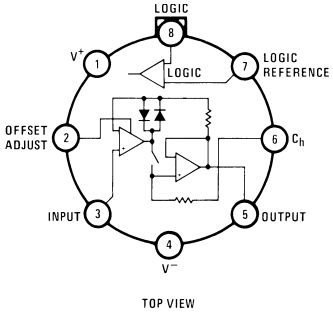


Figure 2. Metal Can Package (TO-99)
See Package Number LMC0008C

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Typical Connection and Performance Curve

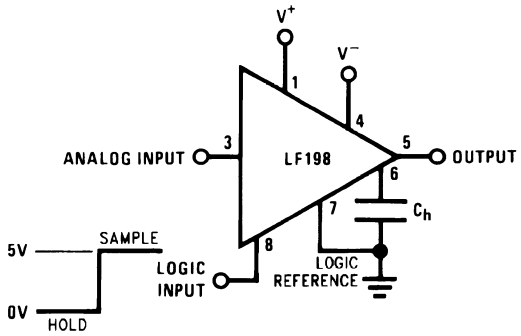


Figure 3.

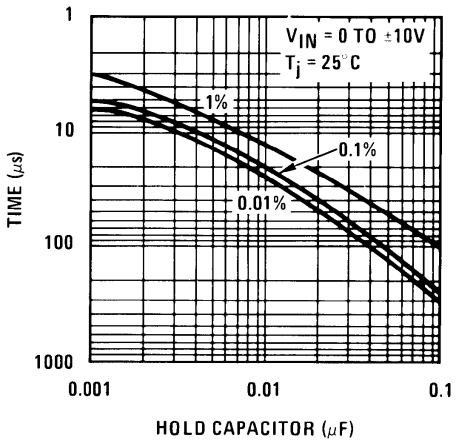
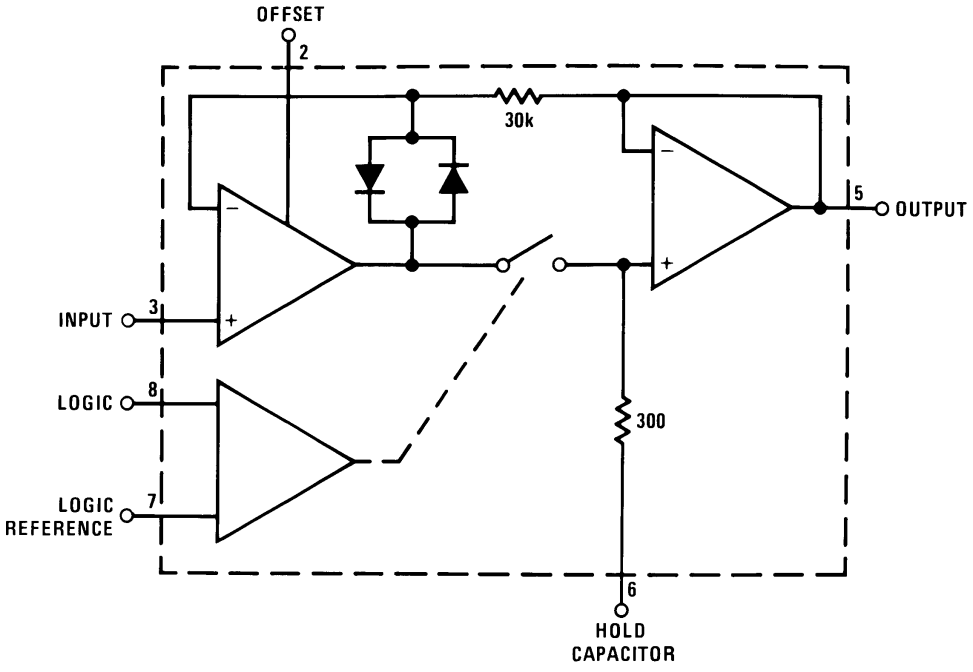


Figure 4. Acquisition Time

Functional Diagram



Absolute Maximum Ratings (1)

Supply Voltage	±18V
Power Dissipation (Package Limitation) (2)	500 mW
Operating Ambient Temperature Range	−55°C to +125°C
Maximum Junction Temperature (T_{Jmax})	+150°C
Input Voltage	Equal to Supply Voltage
Logic To Logic Reference Differential Voltage (3)	+7V, −30V
Output Short Circuit Duration	Indefinite
Hold Capacitor Short Circuit Duration	10 sec
Lead Temperature (Soldering, 10 sec.)	260°C
Thermal Resistance, θ_{JA}	
Metal Can (Still Air at 0.5W)	160°C/W
Metal Can (500 LF/Min Air at 0.5W)	84°C/W
Ceramic SOIC (Stil Air at 0.5W)	140°C/W
Ceramic SOIC (500 LF/Min Air Flow at 0.5W)	95°C/W
θ_{JC}	
Metal Can	48°C/W
Ceramic SOIC	20°C/W
Package Weight (typical)	
Metal Can	TBD
Ceramic SOIC	415mg
ESD Tolerance (4)	500V

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For specifications and test conditions, see the Electrical Characteristics. The specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions

(2) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$, or the number given in the Absolute Maximum Ratings, whichever is lower. .

(3) Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.

(4) Human body model, 100pF discharged through 1.5KΩ

Quality Conformance Inspection

Mil-Std-883, Method 5005 — Group A

Subgroup	Description	Temperature (°C)
1	Static tests at	+25°C
2	Static tests at	+125°C
3	Static tests at	−55°C
4	Dynamic tests at	+25°C
5	Dynamic tests at	+125°C
6	Dynamic tests at	−55°C
7	Functional tests at	+25°C
8A	Functional tests at	+125°C
8B	Functional tests at	−55°C
9	Switching tests at	+25°C
10	Switching tests at	+125°C
11	Switching tests at	−55°C

Electrical Characteristics

The following specifications apply unless otherwise specified.
V_{CC} = ±15V, R_L = 10KΩ, V_{IN} = 0V, C_{HOLD} = 0.01 µF, Logic Reference Pin = 0V, Logic Pin = 4V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
I_{CC}+	Positive Supply Current	+V_{CC} = 15V, -V_{CC} = -15V			5.5	mA	1, 2
					6.5	mA	3
		+V_{CC} = 18V, -V_{CC} = -18V, Mode = "Sample"			5.5	mA	1, 2
					6.5	mA	3
		+V_{CC} = 18V, -V_{CC} = -18V, Mode = "Hold"			5.5	mA	1, 2
					6.5	mA	3
I_{CC}-	Negative Supply Current	+V_{CC} = 15V, -V_{CC} = -15V		-5.5		mA	1, 2
				-6.5		mA	3
		+V_{CC} = 18V, -V_{CC} = -18V, Mode = "Sample"		-5.5		mA	1, 2
				-6.5		mA	3
		+V_{CC} = 18V, -V_{CC} = -18V, Mode = "Hold"		-5.5		mA	1, 2
				-6.5		mA	3
V_{OS}	Input Offset Voltage	+V_{CC} = 3V, -V_{CC} = -7V		-3.0	3.0	mV	1
				-5.0	5.0	mV	2, 3
		+V_{CC} = 15V, -V_{CC} = -15V		-3.0	3.0	mV	1
				-5.0	5.0	mV	2, 3
		+V_{CC} = 3.5V, -V_{CC} = -26.5V		-3.0	3.0	mV	1
				-5.0	5.0	mV	2, 3
		+V_{CC} = 18V, -V_{CC} = -18V		-3.0	3.0	mV	1
				-5.0	5.0	mV	2, 3
		+V_{CC} = 3.5V, -V_{CC} = -32.5V		-3.0	3.0	mV	1
				-5.0	5.0	mV	2, 3
		+V_{CC} = 26.5V, -V_{CC} = -3.5V		-3.0	3.0	mV	1
				-5.0	5.0	mV	2, 3
		+V_{CC} = 32.5V, -V_{CC} = -3.5V, Logic = 2.5V		-3.0	3.0	mV	1
				-5.0	5.0	mV	2, 3
		+V_{CC} = 7V, -V_{CC} = -3V		-3.0	3.0	mV	1
				-5.0	5.0	mV	2, 3
I_{IB}	Input Bias Current	+V_{CC} = 3V, -V_{CC} = -7V		-25	25	nA	1
				-75	75	nA	2, 3
		+V_{CC} = 15V, -V_{CC} = -15V		-25	25	nA	1
				-75	75	nA	2, 3
		+V_{CC} = 3.5V, -V_{CC} = -32.5V		-25	25	nA	1
				-75	75	nA	2, 3
		+V_{CC} = 32.5V, -V_{CC} = -3.5V		-25	25	nA	1
				-75	75	nA	2, 3
		+V_{CC} = 7V, -V_{CC} = -3V		-25	25	nA	1
				-75	75	nA	2, 3
$I_{Leak(Cap)}$	Leakage Current into Hold Capacitor	+V_{CC} = 3V, -V_{CC} = -7V	See (1)	-100	100	pA	1
		+V_{CC} = 3.5V, -V_{CC} = -32.5V		-100	100	pA	1
		+V_{CC} = 32.5V, -V_{CC} = -3.5V	See (1)	-100	100	pA	1
		+V_{CC} = 7V, -V_{CC} = -3V		-100	100	pA	1

(1) Leakage current is measured at a junction temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is specified over full input signal range.

Electrical Characteristics (continued)

The following specifications apply unless otherwise specified.
V_{CC} = ±15V, R_L = 10KΩ, V_{IN} = 0V, C_{HOLD} = 0.01 µF, Logic Reference Pin = 0V, Logic Pin = 4V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{HS}	Hold Step	$+V_{CC}$ = 15V $-V_{CC}$ = -15V	See (2)	-2.0	2.0	mV	1
				-5.6	5.6	mV	2, 3
		$+V_{CC}$ = 3.5V, $-V_{CC}$ = -26.5V	See (2)	-2.5	2.5	mV	1
				-5.6	5.6	mV	2, 3
		$+V_{CC}$ = 26.5V, $-V_{CC}$ = -3.5V	See (2)	-2.5	2.5	mV	1
				-5.6	5.6	mV	2, 3
A_E	Gain Error	$+V_{CC}$ = 7V, $-V_{CC}$ = -3V			0.02	%	1
					0.06	%	2, 3
		$+V_{CC}$ = 3.5V, $-V_{CC}$ = -26.5V			0.005	%	1
					0.02	%	2, 3
		$+V_{CC}$ = 32.5V, $-V_{CC}$ = -3.5V			0.005	%	1
					0.06	%	2, 3
		$+V_{CC}$ = 26.5V, $-V_{CC}$ = -3.5V			0.005	%	1
					0.02	%	2, 3
Z_I	Input Impedance	$+V_{CC}$ = 8V, $-V_{CC}$ = -28V		10.0		GΩ	1
				0.8		GΩ	2, 3
		$+V_{CC}$ = 28V, $-V_{CC}$ = -8V		10.0		GΩ	1
				0.8		GΩ	2, 3
Z_O	Output Impedance	$+V_{CC}$ = 18V, $-V_{CC}$ = -18V			2.0	Ω	1
					4.0	Ω	2, 3
I_{Charge}	Capacitor Charging Current	$+V_{CC}$ = 8V, $-V_{CC}$ = -28V		-25	-4.5	mA	1
				-25	-3.0	mA	2, 3
		$+V_{CC}$ = 28V, $-V_{CC}$ = -8V		4.5	25	mA	1
				3.0	25	mA	2, 3
Logic	Logic Pin Current	$+V_{CC}$ = 18V, $-V_{CC}$ = -18V, Mode = "Sample", Logic = 7V			10	µA	1, 2, 3
		$+V_{CC}$ = 18V, $-V_{CC}$ = -18V, Mode = "Hold", Logic = -30V			1.0	µA	1
					0.5	µA	2, 3
V_{OS}	Input Offset Voltage	$+V_{CC}$ = 15V, $-V_{CC}$ = -15V, I_{Drive} = +1mA		-3.5	3.5	mV	1
				-6.0	6.0	mV	2, 3
Delta V_{OS}	Input Offset Voltage	$+V_{CC}$ = 15V, $-V_{CC}$ = -15V, I_{Drive} = +1mA to -1mA		-1.1	1.1	mV	1
				-2.0	2.0	mV	2, 3
I_{OS}+	Output Short Circuit Current	$+V_{CC}$ = 18V, $-V_{CC}$ = -18V		7.0	20	mA	1
I_{OS}-	Output Short Circuit Current	$+V_{CC}$ = 18V, $-V_{CC}$ = -18V		-25	-7.0	mA	1
$I_{LogicRef}$	Logic Reference Pin Current	$+V_{CC}$ = 18V, $-V_{CC}$ = -18V, Mode = "Sample", Logic = 7V		-1.0	1.0	µA	1
				-0.5	5.0	µA	2, 3
		$+V_{CC}$ = 18V, $-V_{CC}$ = -18V, Mode = "Hold", Logic = -30V			10	µA	1, 2, 3

(2) Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1 pF, for instance, will create an additional 0.5 mV step with a 5V logic swing and a 0.01µF hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.

Electrical Characteristics (continued)

The following specifications apply unless otherwise specified.
V_{CC} = ±15V, R_L = 10KΩ, V_{IN} = 0V, C_{HOLD} = 0.01 µF, Logic Reference Pin = 0V, Logic Pin = 4V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
PSRR	Power Supply Rejection Ratio			80		dB	1
		$+V_{CC}$ = 10V, $-V_{CC}$ = -15V		74		dB	2, 3
				80		dB	1
		$+V_{CC}$ = 15V, $-V_{CC}$ = -10V		74		dB	2, 3
FTRR	Feed Through Rejection Ratio			86		dB	1
		$+V_{CC}$ = 3.5V, $-V_{CC}$ = -32.5V		74		dB	2, 3
				86		dB	1
		$+V_{CC}$ = 32.5V, $-V_{CC}$ = -3.5V		74		dB	2, 3
V_{TH}	Differential Logic Level		See (3)	0.8	2.4	V	1
V_{OS} (2nd Stg)	2nd Stage V_{OS}	$+V_{CC}$ = 3.5V, $-V_{CC}$ = -32.5V		-35	+35	mV	1
				-50	+50	mV	2, 3
		$+V_{CC}$ = 3V, $-V_{CC}$ = -7V		-35	+35	mV	1
				-50	+50	mV	2, 3
		$+V_{CC}$ = 32.5V, $-V_{CC}$ = -3.5V		-35	+35	mV	1
				-50	+50	mV	2, 3
		$+V_{CC}$ = 7V, $-V_{CC}$ = -3V		-35	+35	mV	1
				-50	+50	mV	2, 3

(3) Parameter tested go no go only for Vth test.

AC Parameters

The following specifcations apply unless otherwise specified.
V_{CC} = ±15V, R_L = 10KΩ, V_{IN} = 0V, C_{Hold} = 0.01 µF, Logic Reference Pin = 0V, Logic Pin = 4V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
T_{AQ}	Acquisition Time	Delta V_{OUT} = 10V, C_{Hold} = 1000pF			6.0	µS	4
		Delta V_{OUT} = 10V, C_{Hold} = 0.01µF			25	µS	4

DC Parameters: Drift Values

The following conditions apply to all the following parameters, unless otherwise specified.
V_{CC} = ±15V, R_L = 10KΩ, V_{IN} = 0V, C_{Hold} = 0.01 µF, Logic Reference Pin = 0V, Logic Pin = 4V
Deltas required for S-Level product ONLY.

Symbol	Parameters	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{OS}	Input Offset Voltage	$+V_{CC}$ = 15V, $-V_{CC}$ = -15V		-0.5	0.5	mV	1
I_{IB}	Input Bias Current	$+V_{CC}$ = 15V, $-V_{CC}$ = -15V		-2.5	2.5	nA	1

Typical Performance Characteristics

Aperture Time
(See the Definition of Terms)

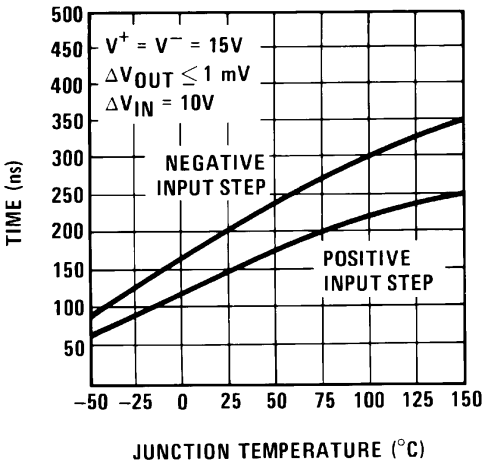


Figure 5.

Dielectric Absorption
Error in Hold Capacitor

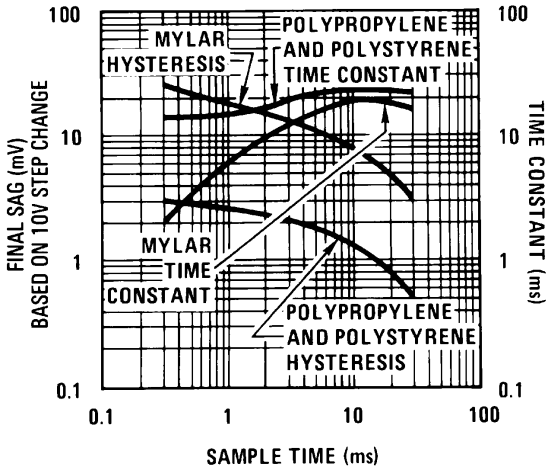


Figure 6.

Dynamic Sampling Error

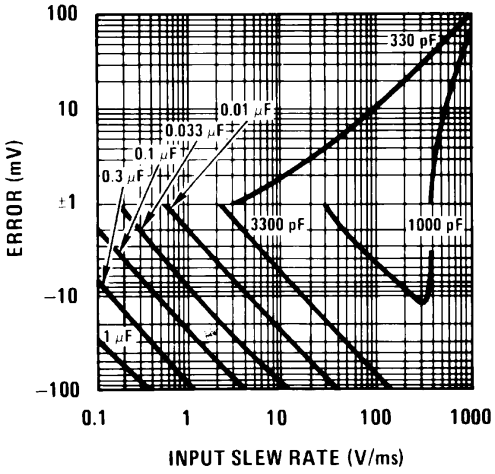


Figure 7.

Output Droop Rate

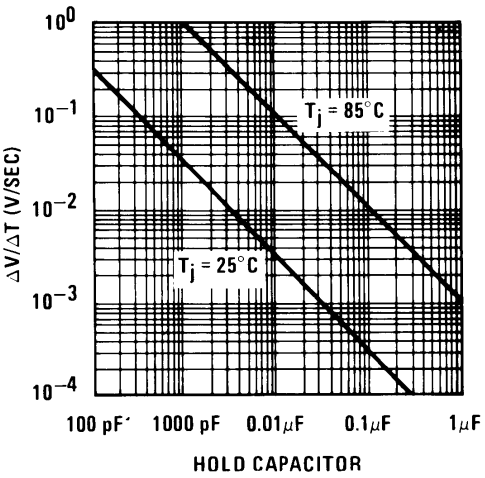


Figure 8.

Hold Step

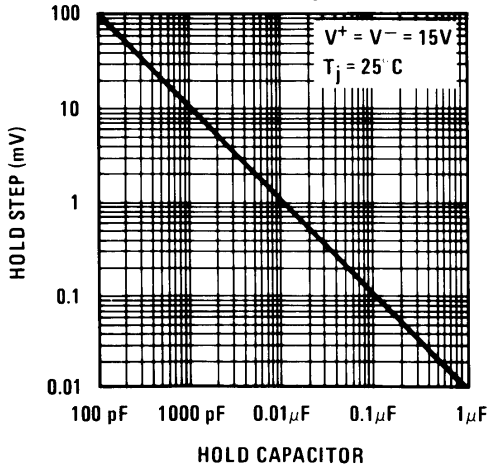


Figure 9.

"Hold" Settling Time
(See the Definition of Terms)

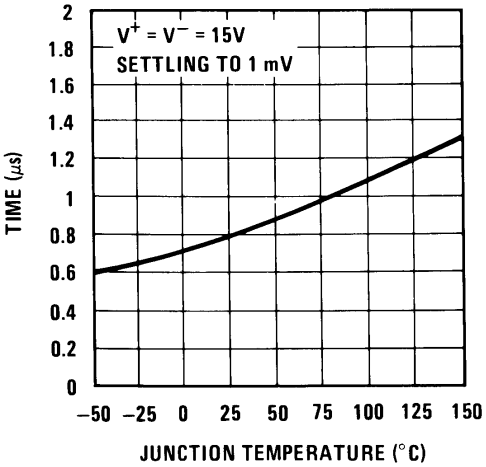


Figure 10.

Typical Performance Characteristics (continued)

Leakage Current into Hold Capacitor

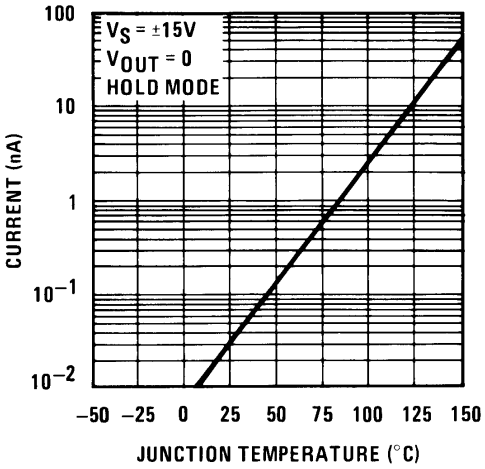


Figure 11.

Phase and Gain (Input to Output, Small Signal)

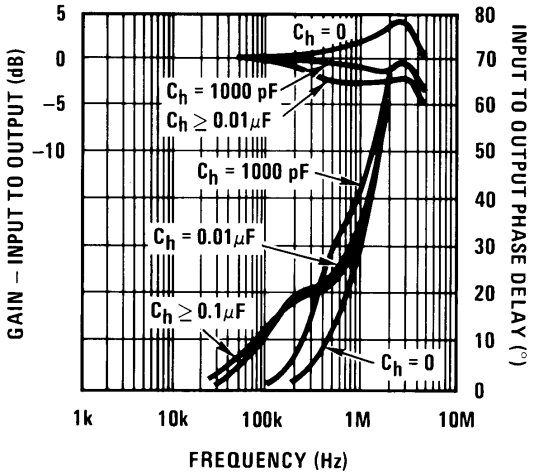


Figure 12.

Gain Error

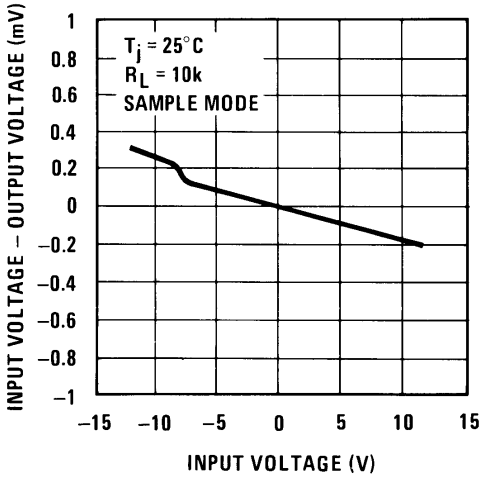


Figure 13.

Power Supply Rejection

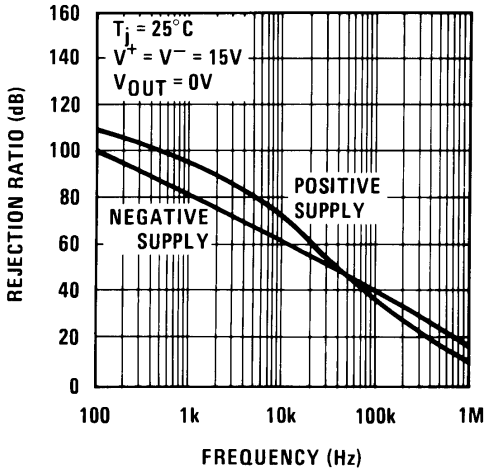


Figure 14.

Output Short Circuit Current

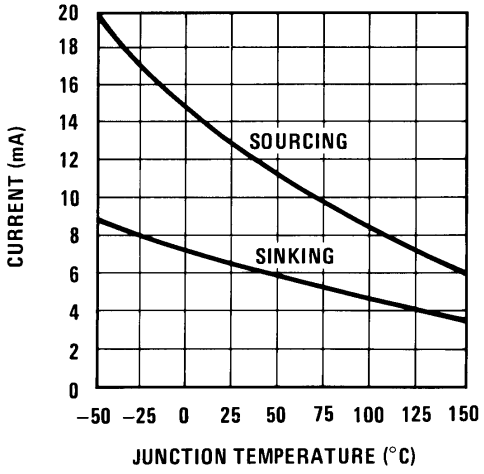


Figure 15.

Output Noise (See the Definition of Terms)

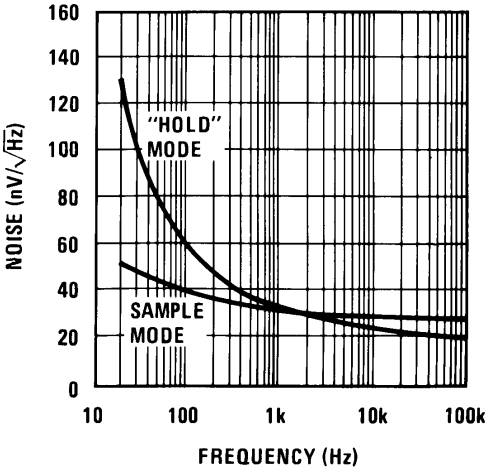


Figure 16.

Typical Performance Characteristics (continued)

Input Bias Current

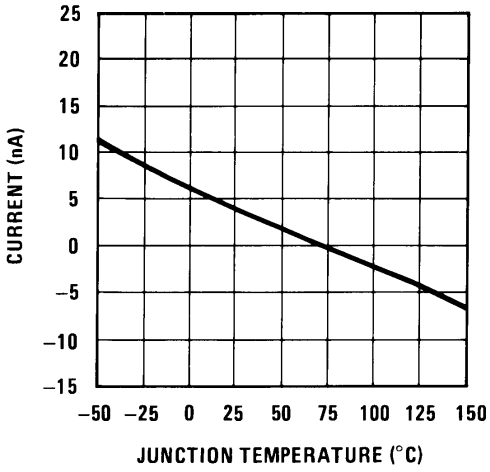


Figure 17.

Feedthrough Rejection Ratio (Hold Mode)

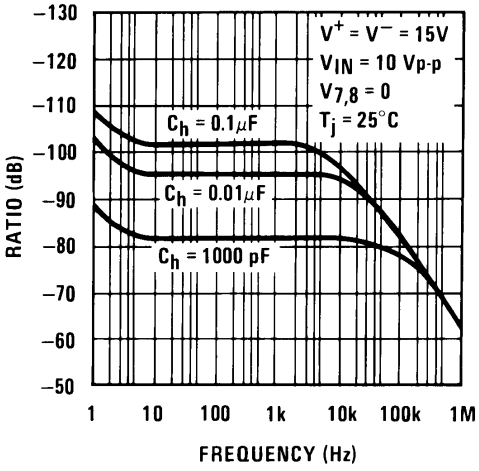


Figure 18.

Hold Step vs Input Voltage

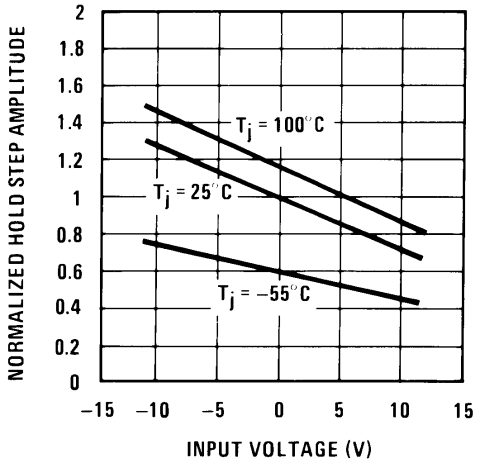


Figure 19.

Output Transient at Start of Sample Mode

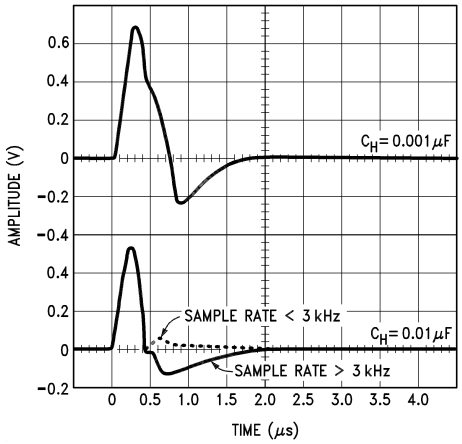


Figure 20.

Output Transient at Start of Hold Mode

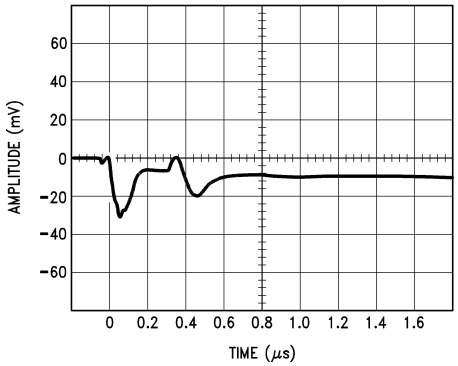
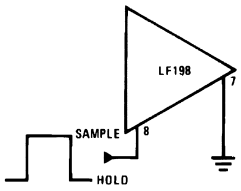


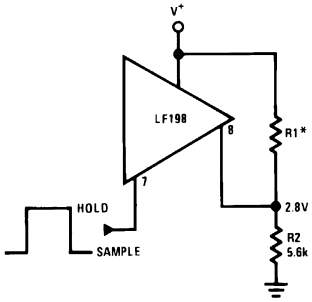
Figure 21.

Logic Input Configurations

TTL & CMOS
3V ≤ V_{LOGIC} (Hi State) ≤ 7V

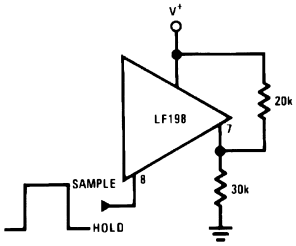


Threshold = 1.4V

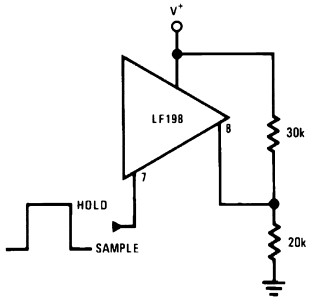


Threshold = 1.4V*Select for 2.8V at pin 8

CMOS
7V ≤ V_{LOGIC} (Hi State) ≤ 15V

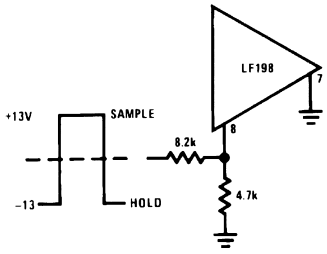


Threshold = 0.6 (V^+) + 1.4V

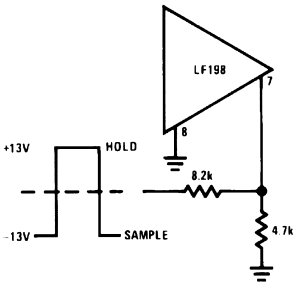


Threshold = 0.6 (V^+) − 1.4V

Op Amp Drive



Threshold ≈ +4V



Threshold = −4V

APPLICATION INFORMATION

HOLD CAPACITOR

Hold step, acquisition time, and droop rate are the major trade-offs in the selection of a hold capacitor value. Size and cost may also become important for larger values. Use of the curves included with this data sheet should be helpful in selecting a reasonable value of capacitance. Keep in mind that for fast repetition rates or tracking fast signals, the capacitor drive currents may cause a significant temperature rise in the LF198.

A significant source of error in an accurate sample and hold circuit is dielectric absorption in the hold capacitor. A mylar cap, for instance, may "sag back" up to 0.2% after a quick change in voltage. A long sample time is required before the circuit can be put back into the hold mode with this type of capacitor. Dielectrics with very low hysteresis are polystyrene, polypropylene, and Teflon. Other types such as mica and polycarbonate are not nearly as good. The advantage of polypropylene over polystyrene is that it extends the maximum ambient temperature from 85°C to 100°C. Most ceramic capacitors are unusable with > 1% hysteresis. Ceramic "NPO" or "COG" capacitors are now available for 125°C operation and also have low dielectric absorption. For more exact data, see the curve *Dielectric Absorption Error.* The hysteresis numbers on the curve are final values, taken after full relaxation. The hysteresis error can be significantly reduced if the output of the LF198 is digitized quickly after the hold mode is initiated. The hysteresis relaxation time constant in polypropylene, for instance, is 10—50 ms. If A-to-D conversion can be made within 1 ms, hysteresis error will be reduced by a factor of ten.

DC AND AC ZEROING

DC zeroing is accomplished by connecting the offset adjust pin to the wiper of a 1 kΩ potentiometer which has one end tied to V^+ and the other end tied through a resistor to ground. The resistor should be selected to give ≈0.6 mA through the 1k potentiometer.

AC zeroing (hold step zeroing) can be obtained by adding an inverter with the adjustment pot tied input to output. A 10 pF capacitor from the wiper to the hold capacitor will give ±4 mV hold step adjustment with a 0.01 µF hold capacitor and 5V logic supply. For larger logic swings, a smaller capacitor (< 10 pF) may be used.

LOGIC RISE TIME

For proper operation, logic signals into the LF198 must have a minimum dV/dt of 1.0 V/µs. Slower signals will cause excessive hold step. If a R/C network is used in front of the logic input for signal delay, calculate the slope of the waveform at the threshold point to ensure that it is at least 1.0 V/µs.

SAMPLING DYNAMIC SIGNALS

Sample error to moving input signals probably causes more confusion among sample-and-hold users than any other parameter. The primary reason for this is that many users make the assumption that the sample and hold amplifier is truly locked on to the input signal while in the sample mode. In actuality, there are finite phase delays through the circuit creating an input-output differential for fast moving signals. In addition, although the output may have settled, the hold capacitor has an additional lag due to the 300Ω series resistor on the chip. This means that at the moment the "hold" command arrives, the hold capacitor voltage may be somewhat different than the actual analog input. The effect of these delays is opposite to the effect created by delays in the logic which switches the circuit from sample to hold. For example, consider an analog input of 20 Vp-p at 10 kHz. Maximum dV/dt is 0.6 V/µs. With no analog phase delay and 100 ns logic delay, one could expect up to (0.1 µs)(0.6V/µs)= 60 mVerror if the "hold" signal arrived near maximum dV/dt of the input. A positive-going input would give a +60 mV error. Now assume a 1 MHz (3 dB) bandwidth for the overall analog loop. This generates a phase delay of 160 ns. If the hold capacitor sees this exact delay, then error due to analog delay will be (0.16 µs) (0.6 V/µs) = −96 mV. Total output error is +60 mV (digital) −96 mV (analog) for a total of −36 mV. To add to the confusion, analog delay is proportioned to hold capacitor value while digital delay remains constant. A family of curves (dynamic sampling error) is included to help estimate errors.

A curve labeled *Aperture Time* has been included for sampling conditions where the input is steady during the sampling period, but may experience a sudden change nearly coincident with the "hold" command. This curve is based on a 1 mV error fed into the output.

A second curve, *Hold Settling Time* indicates the time required for the output to settle to 1 mV after the "hold" command.

DIGITAL FEEDTHROUGH

Fast rise time logic signals can cause hold errors by feeding externally into the analog input at the same time the amplifier is put into the hold mode. To minimize this problem, board layout should keep logic lines as far as possible from the analog input and the C_h pin. Grounded guarding traces may also be used around the input line, especially if it is driven from a high impedance source. Reducing high amplitude logic signals to 2.5V will also help.

Guarding Technique

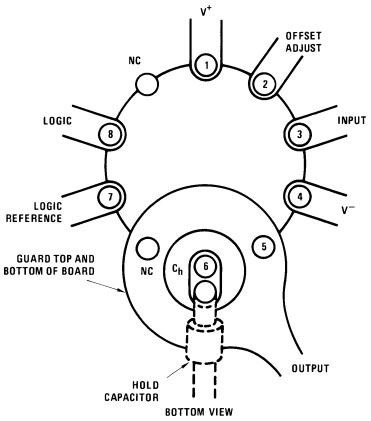
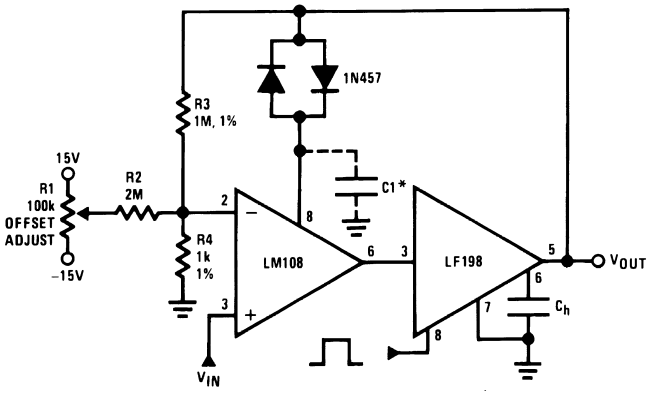


Figure 22. Use 10-pin layout. Guard around C_h is tied to output.

Typical Applications

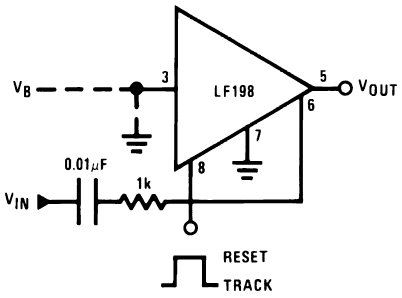
X1000 Sample & Hold



*For lower gains, the LM108 must be frequency compensated

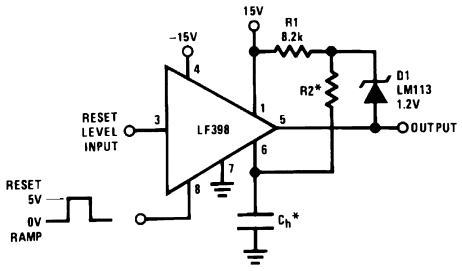
Use $\approx \frac{100}{A_V}$ pF from comp 2 to ground

Sample and Difference Circuit (Output Follows Input in *Hold* Mode)



$V_{OUT} = V_B + \Delta V_{IN}$(HOLD MODE)

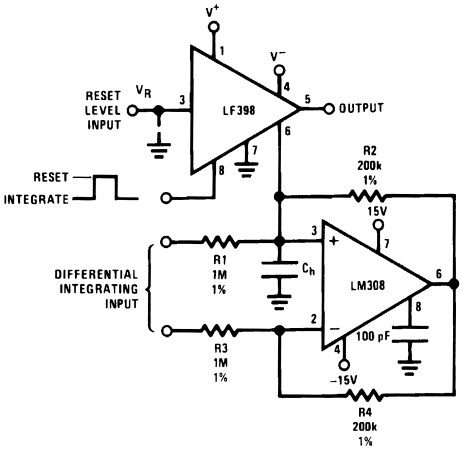
Ramp Generator with Variable Reset Level



*Select for ramp rate R2 ≥ 10k

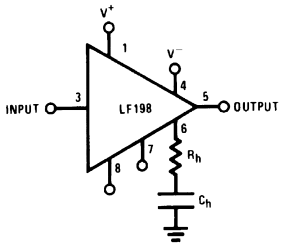
$$\frac{\Delta V}{\Delta T} = \frac{1.2V}{(R2)\,(C_h)}$$

Integrator with Programmable Reset Level



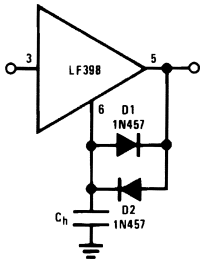
$$V_{OUT}\ (\text{Hold Mode}) = \left[\frac{1}{(R1)\,(C_h)}\int_0^t V_{IN}\,dt\right] + \left[V_R\right]$$

Output Holds at Average of Sampled Input

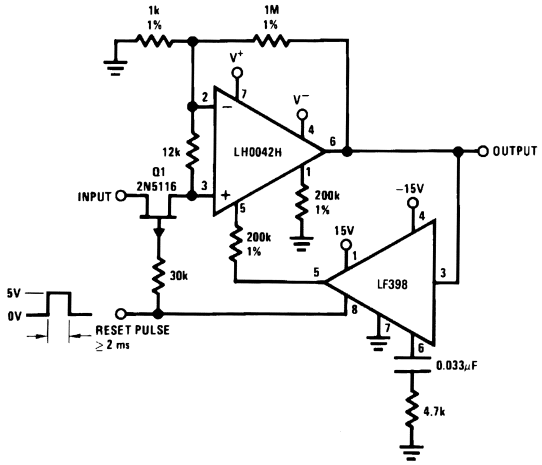


$$\text{Select } (R_h)\,(C_h) \gg \frac{1}{2\pi f_{IN}\,(\text{Min})}$$

Increased Slew Current



Reset Stabilized Amplifier (Gain of 1000)



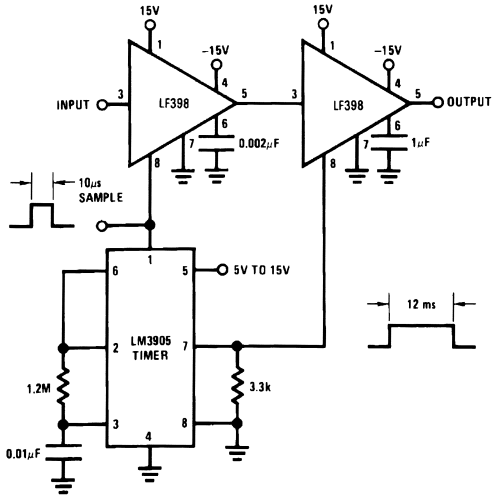
$V_{OS} \leq 20\mu V$ (No trim)

$Z_{IN} \approx 1\ M\Omega$

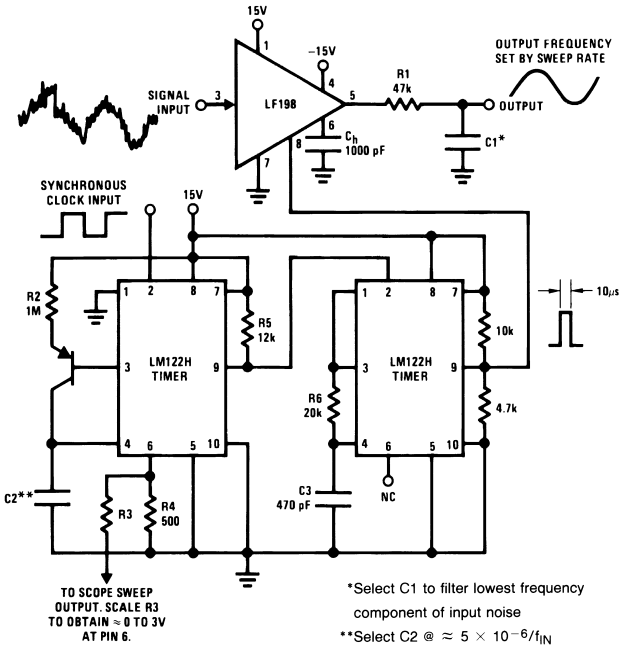
$\frac{\Delta V_{OS}}{\Delta t} \approx 30\mu V/sec$

$\frac{\Delta V_{OS}}{\Delta T} \approx 0.1\mu V/°C$

Fast Acquisition, Low Droop Sample & Hold



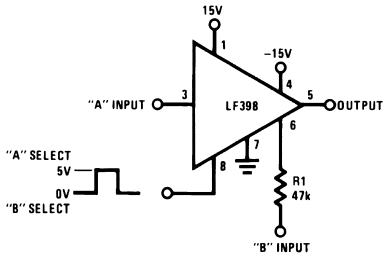
Synchronous Correlator for Recovering Signals Below Noise Level



*Select C1 to filter lowest frequency component of input noise

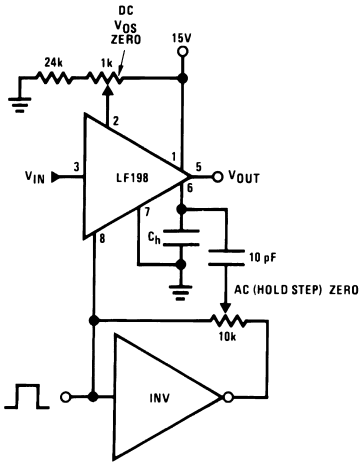
**Select C2 @ $\approx 5 \times 10^{-6}/f_{IN}$

2–Channel Switch

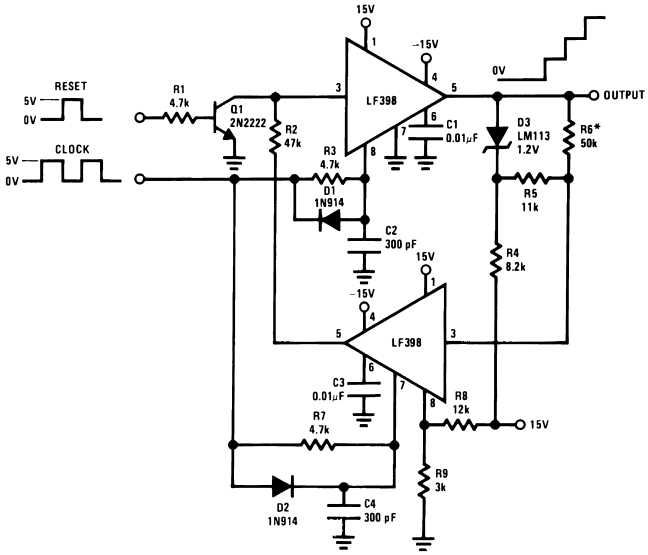


	A	B
Gain	1 ± 0.02%	1 ± 0.2%
Z_{IN}	$10^{10}\Omega$	47 kΩ
BW	≃ 1 MHz	≃ 400 kHz
Crosstalk	−90 dB	−90 dB
@ 1 kHz		
Offset	≤ 6 mV	≤ 75 mV

DC & AC Zeroing

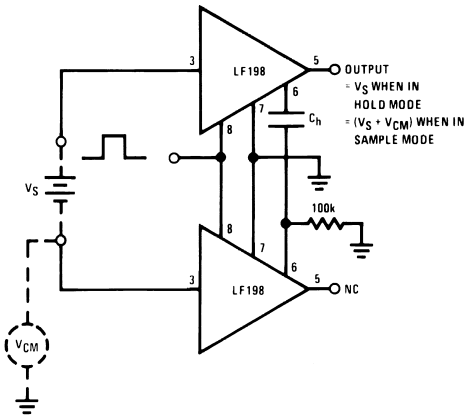


Staircase Generator

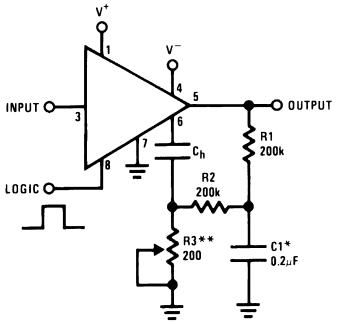


*Select for step height
50k → ≅ 1V Step

Differential Hold



Capacitor Hysteresis Compensation



*Select for time constant C1 = $\frac{\tau}{100k}$

**Adjust for amplitude

Definition of Terms

Hold Step: The voltage step at the output of the sample and hold when switching from sample mode to hold mode with a steady (dc) analog input voltage. Logic swing is 5V.

Acquisition Time: The time required to acquire a new analog input voltage with an output step of 10V. Note that acquisition time is not just the time required for the output to settle, but also includes the time required for all internal nodes to settle so that the output assumes the proper value when switched to the hold mode.

Gain Error: The ratio of output voltage swing to input voltage swing in the sample mode expressed as a per cent difference.

Hold Settling Time: The time required for the output to settle within 1 mV of final value after the “hold” logic command.

Dynamic Sampling Error: The error introduced into the held output due to a changing analog input at the time the hold command is given. Error is expressed in mV with a given hold capacitor value and input slew rate. Note that this error term occurs even for long sample times.

Aperture Time: The delay required between “Hold” command and an input analog transition, so that the transition does not affect the held output.

REVISION HISTORY SECTION

Date Released	Revision	Section	Originator	Changes
02/25/05	A	New release, Corporate format	L. Lytle	1 MDS converted to corp. datasheet format. MNLF198–X Rev 3B0 MDS to be archived. Change has been made to Electrical Section, Parameter I_{OS}- . Max limit was 7.0 now is −7.0 confirmed with SG. Added note Parameter tested go no go to V_{TH} test.
03/20/2013	A	All Sections		Changed Layout of National Data Sheet to TI format

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-8760801GA	Active	Production	TO-99 (LMC) | 8	20 | JEDEC TRAY (5+1)	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	LF198H/883 5962-8760801GA Q A CO 5962-8760801GA Q > T
5962-8760801VZA	Active	Production	CFP (NAC) | 14	88 | JEDEC TRAY (5+1)	No	Call TI	Level-1-NA-UNLIM	-55 to 125	LF198WG-QMLV Q 5962-87608 01VZA ACO 01VZA >T
LF198H/883	Active	Production	TO-99 (LMC) | 8	20 | JEDEC TRAY (5+1)	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	LF198H/883 5962-8760801GA Q A CO 5962-8760801GA Q > T
LF198WG-QMLV	Active	Production	CFP (NAC) | 14	88 | JEDEC TRAY (5+1)	No	Call TI	Level-1-NA-UNLIM	-55 to 125	LF198WG-QMLV Q 5962-87608 01VZA ACO 01VZA >T

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

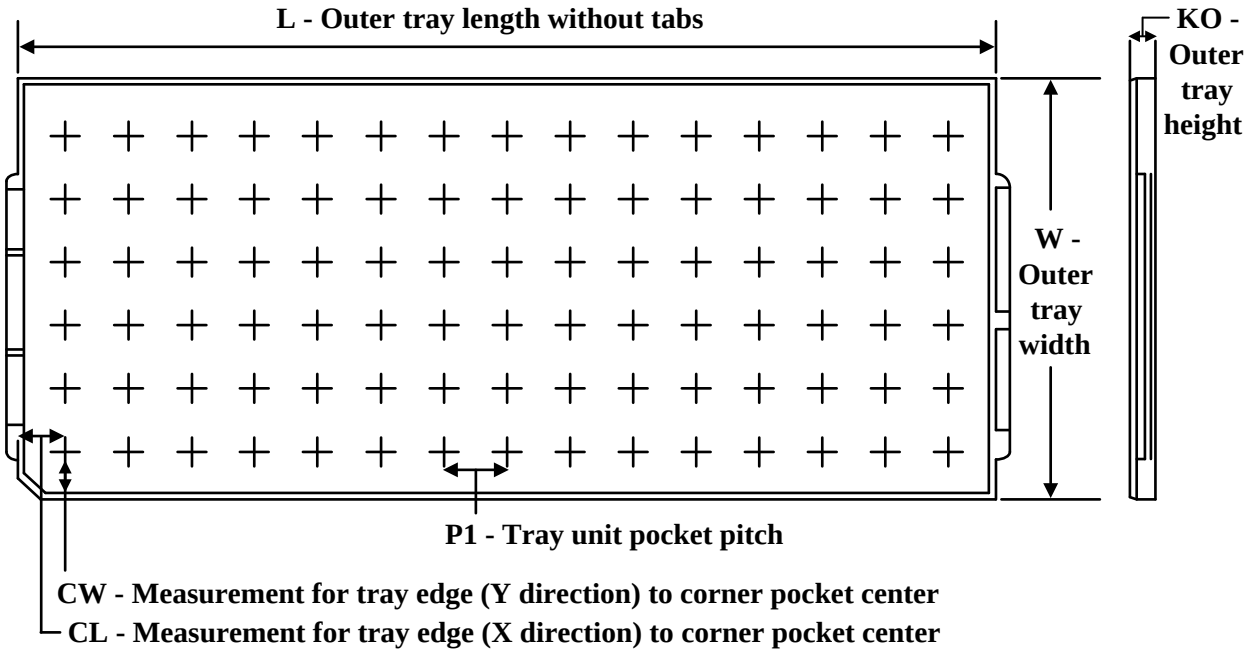
OTHER QUALIFIED VERSIONS OF LF198QML, LF198QML-SP :

- Military : LF198QML
- Space : LF198QML-SP

NOTE: Qualified Version Definitions:

- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

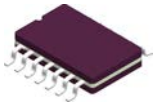
TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
5962-8760801GA	LMC	TO-CAN	8	20	2 X 10	150	126.49	61.98	8890	11.18	12.95	18.54
LF198H/883	LMC	TO-CAN	8	20	2 X 10	150	126.49	61.98	8890	11.18	12.95	18.54

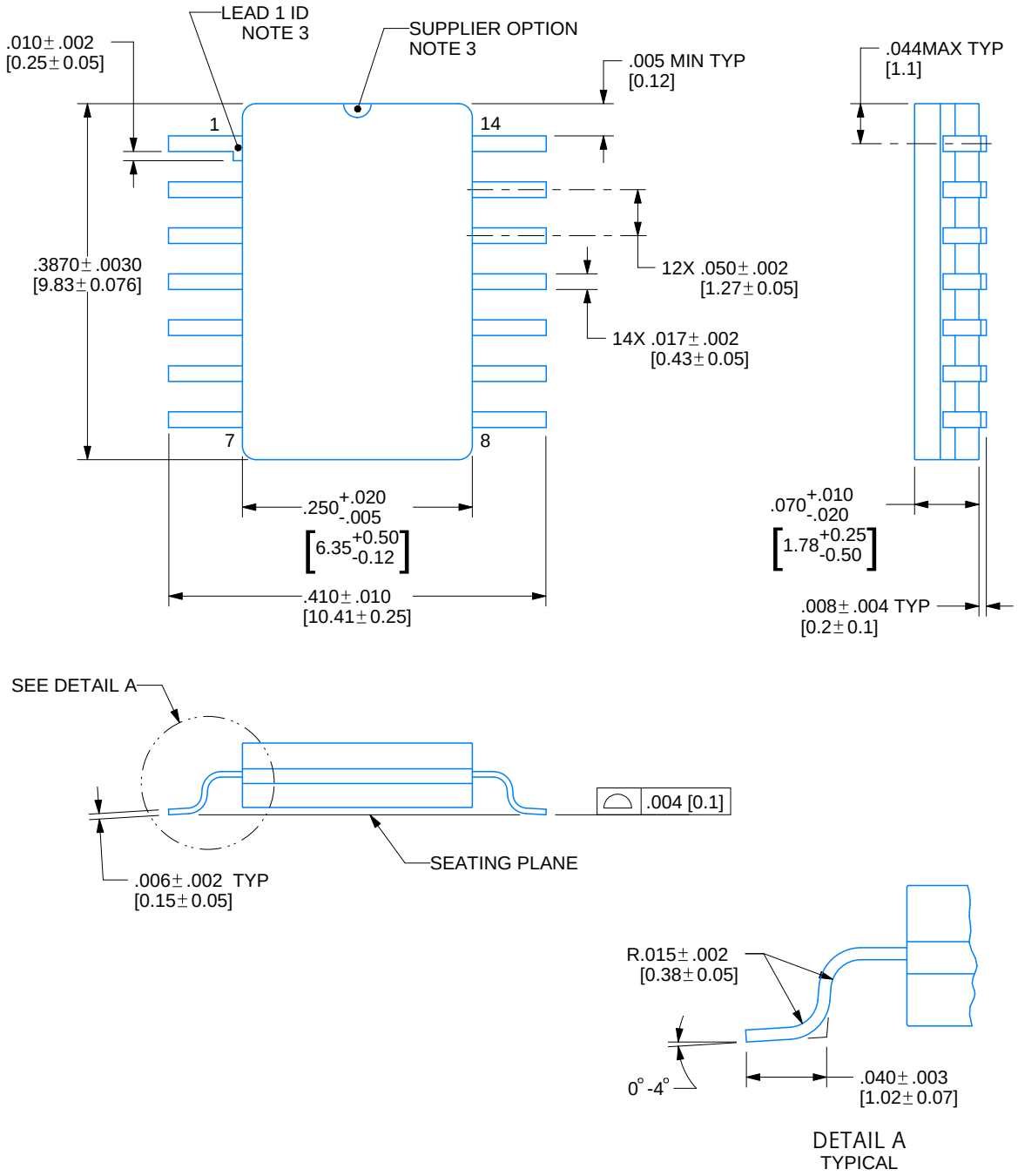


PACKAGE OUTLINE

NAC0014A

CERPACK

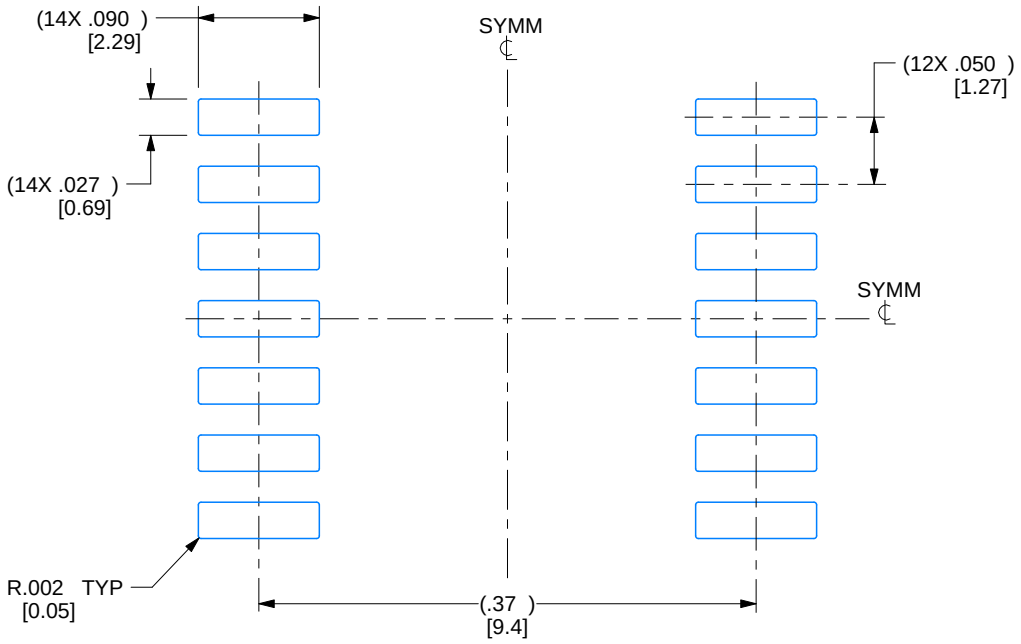
CERAMIC FLATPACK



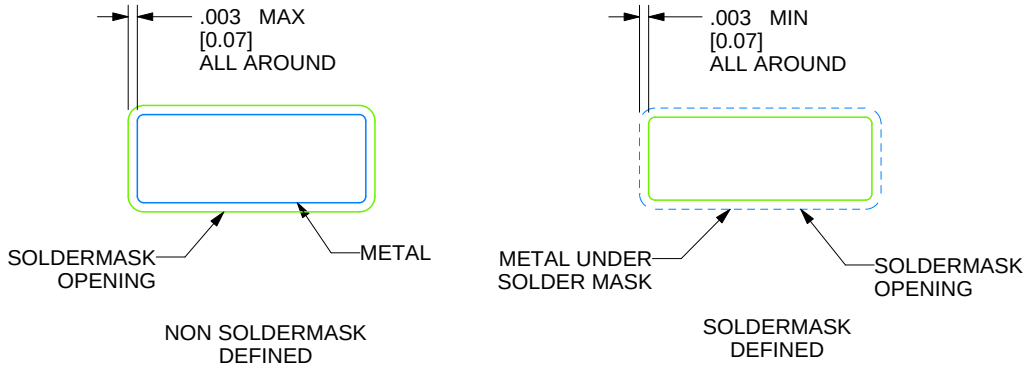
4215197/C 08/2022

NOTES:

1. Controlling dimension is Inch. Values in [ ] are milimeters. Dimensions in ( ) for reference only.
2. For solder thickness and composition, see the "Lead Finish Composition/Thickness" link in the packaging section of the Texas Instruments website
3. Lead 1 identification shall be:
   a) A notch or other mark within this area
   b) A tab on lead 1, either side
4. No JEDEC registration as of December 2021



RECOMMENDED LAND PATTERN



4215197/C 08/2022

REVISIONS

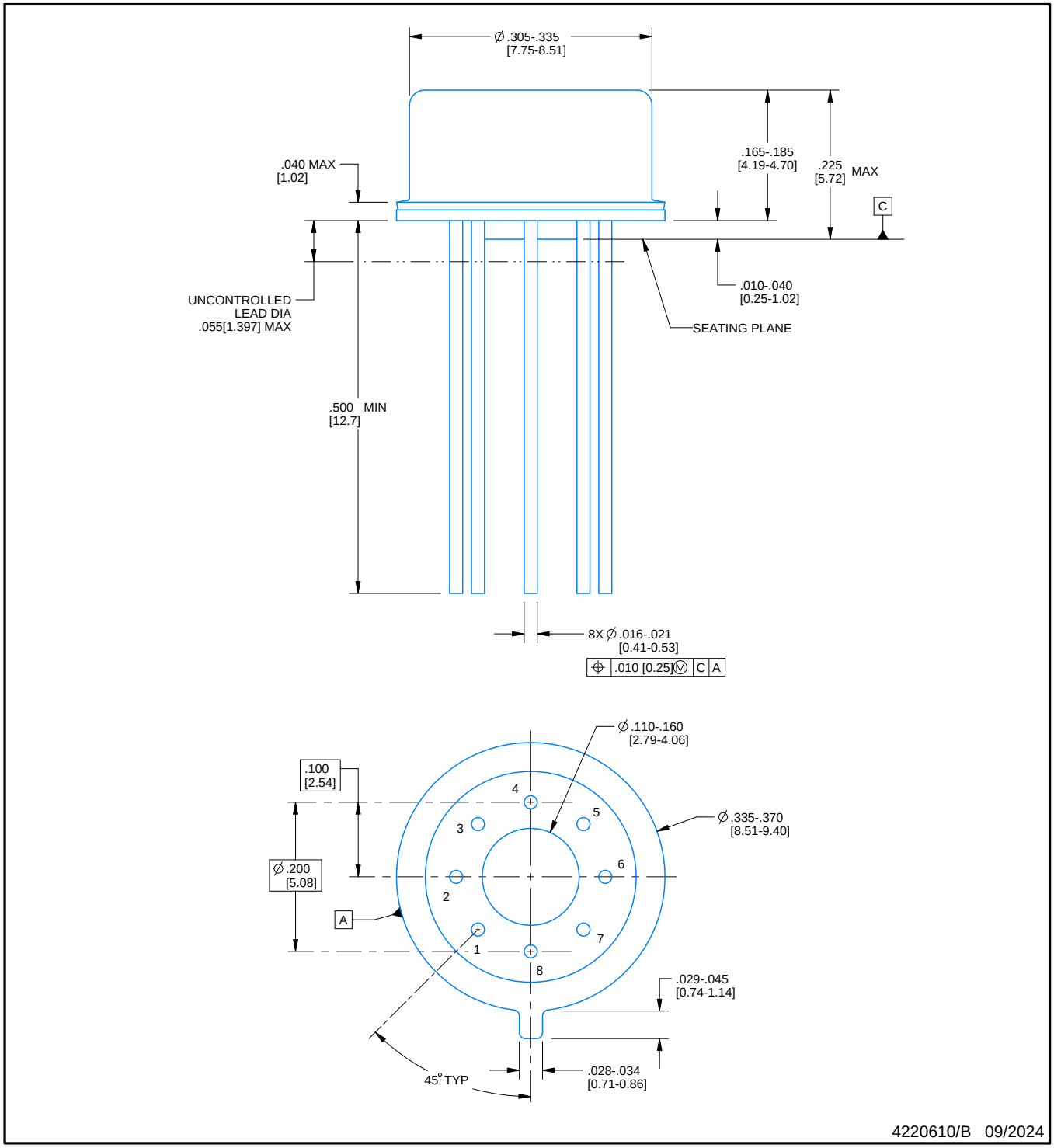
REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	2197878	12/30/2021	DAVID CHIN / ANIS FAUZI
B	NO CHANGE TO DRAWING; REVISION FOR YODA RELEASE;	2198833	02/15/2022	K. SINCERBOX
C	.3870± .0030 WAS .39000± .00012;	2200916	08/08/2022	D. CHIN / K. SINCERBOX

PACKAGE OUTLINE

LMC0008A

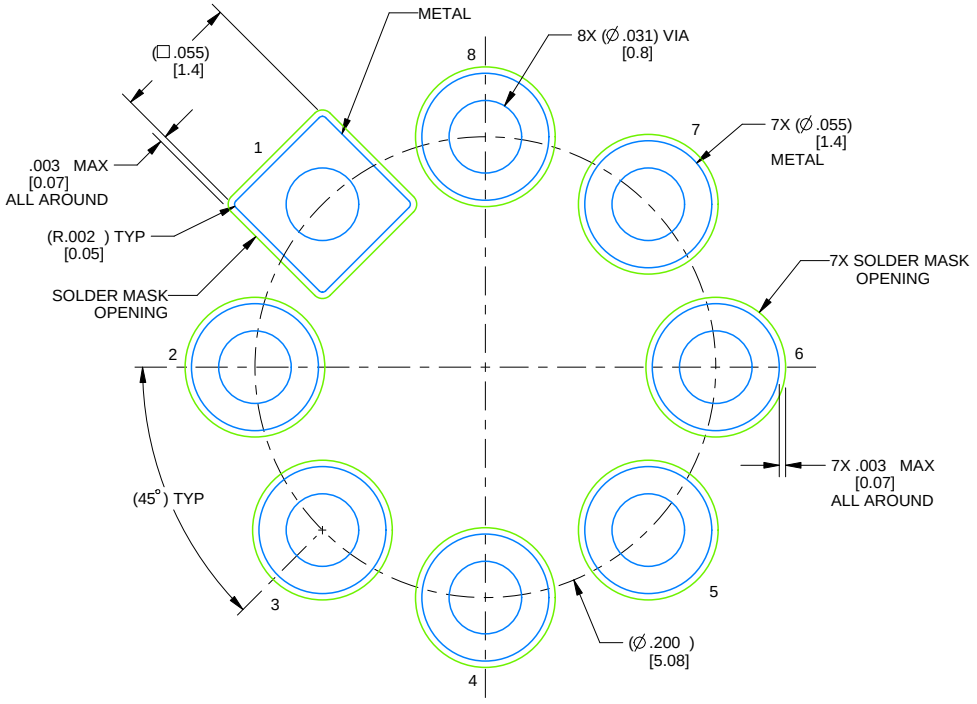
TO-CAN - 5.72 mm max height

TRANSISTOR OUTLINE



NOTES:

1. All linear dimensions are in inches [millimeters]. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pin numbers shown for reference only. Numbers may not be marked on package.
4. Reference JEDEC registration MO-002/TO-99.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 12X

4220610/B 09/2024

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265